ALGORITHM OPTIMIZATION AND LOW COST BIT-SERIAL ARCHITECTURE DESIGN FOR INTEGER-PIXEL AND SUB-PIXEL MOTION ESTIMATION IN H.264/AVC

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Abstract

H.264/AVC employs variable block-size motion estimation (VBSME) with quarter-pixel accuracy, which significantly improves its coding performance. However, the higher coding performance comes at the price of huge computational complexity and memory bandwidth. Therefore, acceleration of the motion estimation (ME) in H.264/AVC with efficient algorithms and architectures is essential for real-time applications. This thesis is concerned with algorithm optimization and efficient low cost architecture design for integer motion estimation (IME) and sub-pixel motion estimation (SME) of H.264/AVC.

Regarding the IME of H.264/AVC, we introduce two low cost bit-serial architectures, which are based on full search (FS) algorithm due to its regularity and coding performance. Both architectures benefit from sum of absolute differences (SAD) and data reusing techniques to reduce their memory bandwidth. The first design has a two-dimensional (2-D) structure featured with broadcasting of reference pixel data and propagating of partial sum and SAD results. The second design uses a 2-D bit-serial adder tree connected to a reconfigurable reference buffer making it suitable for hardware parallelism. To improve the overall performances of our designs, we propose several optimization techniques. By using a pixel truncation method and presenting a word length reduction technique, 68.75% of power consumption and the required time for processing of each search point are saved, where the latency, silicon area, and memory bandwidth are decreased as well. Besides, we employ 1/2-subsampling and mode reduction techniques to reduce the hardware cost further. In addition, a power saving method is contributed to decrease the power consumption of the proposed bit-serial reconfigurable reference buffer. Both designs can support VBSME of 720×480 resolution with 30 frames per second (fps), two reference frames and [-16, 15] search range at a clock frequency of 414 MHz with 29.28 K and 31.5 K gates, respectively.

To address the computational complexity and memory bandwidth requirement problems of interpolate and search method in the SME of H.264/AVC, we introduce a low complexity algorithm and its hardware architecture for SME with quarter-pixel accuracy that is based on parabolic interpolation free algorithms. According to our analysis, the proposed algorithm reduces the computational budget by 94.35% and the memory access requirement by 98.5% in comparison to the standard interpolate and search method with an acceptable video quality. In addition, a fast version of the proposed algorithm is presented that reduces the computational budget 46.28% further while maintaining the video quality. For the hardware architecture design, we choose bit-serial structure for implementing our algorithm to benefit from its advantages. Moreover, we use SAD truncation, reusability, source sharing, and power saving techniques in our architecture, which lead to area saving and power consumption reduction. Furthermore, by using the mode reduction technique, 39% of the required time for processing of each macroblock (MB) is saved. Compared with previous designs, our architecture shows a better performance in terms of silicon area, throughput, latency, and memory bandwidth. Implementation results show that our design can support real-time HD1080 format with 20.3 K gates at the operation frequency of 88.3 MHz.

Abstrak

H.264/AVC menggunakan anggaran gerak saiz blok boleh ubah (VBSME) dengan ketepatan suku-piksel, yang dapat meningkatkan prestasi pengekodan. Namun begitu, prestasi pengekodan yang lebih baik dicapai dengan harga yang mahal iaitu melibatkan jumlah besar kiraan yang kompleks dan lebar jalur ingatan yang besar. Oleh kerana itu, mempercepatkan anggaran gerak (ME) dalam H.264/AVC dengan algoritma dan senibina yang cekap sangat penting untuk aplikasi masa nyata. Penyelidikan ini berkaitan dengan pengoptimuman algoritma dan merekabentuk senibina perkakasan dengan kos yang lebih rendah untuk anggaran gerak integer (IME) dan anggaran gerak sub-pixel (SME) bagi H.264/AVC.

Berkaitan dengan IME bagi H.264/AVC, kami memperkenalkan dua senibina bit-siri kos rendah, yang didasarkan pada algoritma pencarian penuh (FS) disebabkan oleh kelebihan ketetapan dan prestasi pengekodan. Kedua-dua senibina mendapat manfaat dari jumlah perbezaan mutlak (SAD) dan teknik menggunakan semula data untuk mengurangkan lebar jalur ingatan. Rekabentuk pertama mempunyai struktur dua dimensi (2-D) dengan ciri-ciri penyiaran rujukan data piksel, dan penyebaran jumlah separa dan keputusan SAD. Rekabentuk kedua menggunakan pohon penambah bit-siri 2-D bersambung ke penimbal rujukan boleh dikonfigurasi sehingga sesuai untuk perkakasan selari. Untuk meningkatkan prestasi keseluruhan rekabentuk ini, kami mencadangkan beberapa teknik pengoptimuman. Dengan menggunakan kaedah pemangkasan piksel dan teknik pengurangan panjang kata, 68.75% dari penggunaan kuasa dan masa yang diperlukan untuk memproses setiap titik carian dapat dijimatkan, di mana pemendaman, keluasan silikon, dan lebar jalur ingatan juga menurun. Selain itu, kami menggunakan 1/2-subsampling dan teknik mode pengurangan untuk mengurangkan kos perkakasan dengan lebih lanjut. Selain itu, metod penjimatan kuasa dapat mengurangkan penggunaan kuasa bagi penimbal rujukan boleh dikonfigurasi

yang dicadangkan ini. Kedua-dua rekabentuk dapat menyokong VBSME dengan resolusi 720 × 480 untuk 30 bingkai per detik (fps), dua rujukan bingkai dan julat carian[-16, 15] pada frekuensi jam 414 MHz dengan get bersaiz 29.28 K dan 31.5 K, masing-masing.

Untuk mengatasi kekompleksan pengiraan dan masalah keperluan ingatan bagi sisipan dan metod carian dalam SME bagi H.264/AVC, kami mengemukakan suatu algoritma yang kurang kompleks dan senibina perkakasan untuk SME dengan ketepatan satu perempat-piksel yang didasarkan pada algoritma parabola sisipan bebas. Menurut analisis kami, algoritma yang dikemukakan dapat mengurangkan anggaran pengkomputeran sebanyak 94.35% dan keperluan capaian ingatan sebanyak 98.5% jika dibandingkan dengan piawai sisipan dan kaedah pencarian, disamping kualiti video yang boleh diterima. Selain itu, versi algoritma lebih cepat yang dicadangkan dapat mengurangkan lagi anggaran pengkomputeran sebanyak 46.28% di samping dapat mengekalkan kualiti video. Untuk rekabentuk senibina perkakasan, kami telah memilih struktur bit-siri untuk melaksanakan algoritma ini dengan memanafaatkan kelebihan struktur bit-siri tersebut. Selain itu, kami menggunakan pemangkasan SAD, kebolehgunaan, sumber berkongsi, dan teknik penjimatan kuasa dalam senibina ini, yang menyebabkan penjimatan keluasan dan pengurangan pengambilan kuasa. Selain itu, dengan menggunakan teknik mode pengurangan, 39% dari jumlah masa yang diperlukan untuk memproses setiap macroblock (MB) dapat dijimatkan. Berbanding dengan kajian sebelumnya, rekabentuk ini menunjukkan prestasi yang lebih baik dalam masalah keluasan silikon, daya pemprosesan, pendaman, dan lebar jalur ingatan. Keputusan implementasi menunjukkan bahawa rekabentuk ini telah dapat menyokong format masa nyata HD1080 dengan jumlah get sebanyak 20.3 K pada frekuensi operasi 88.3 MHz.

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1-D	One-Dimensional
2-D	Two-Dimensional
ASIC	Application Specific Integrated Circuit
ASP	(MPEG-4) Advanced Simple Profile
AVC	Advanced Video Coding
BR	Bit Rate
CAVLC	Context-Adaptive Variable Length Coding
CC	Computational Complexity
CS	Certain Specification
CIF	Common Intermediate Format
DRC	Demultiplexers-Registers Combination
DVD	Digital Versatile Disc
FA	Full Adder
FIR	Finite Impulse Response
NFM	Nine-Five Model (Algorithm)
FNFM	Fast Five-Nine Model (Algorithm)
FPGA	Field-Programmable Gate Array
fps	Frames per Second
FS	Full Search
FSM	Finite State Machine
GBPS	Giga-Bytes per Second
GIPS	Giga-Instructions per Second
HA	Half Adder
HDL	Hardware Description Language
HDTV	High-Definition TV
HLP	(H.263++) High Latency Profile
HSAD	Half-Pixel Sum of Absolute Difference
IEC	International Electro Technical Commission
IME	Integer Motion Estimation
IMV	Integer Motion Vector
ISAD	Integer Sum of Absolute Difference
ISO	International Organization for Standardization
ITU	International Telecommunication Union

ITU-T	ITU - Telecommunication Standardization Sector
JM	Joint Model
JVT	(MPEG/VCEG) Joint Video Team
LSB	Least Significant Bit
LSI	Large Scale Integration
MA	Memory Access
MB	Macroblock
ME	Motion Estimation
MP@ML	(MPEG-2) Main Profile at Main Level
MPEG	(ISO/IEC) Moving Picture Experts Group
MRF	Multiple Reference Frames
MSB	Most Significant Bit
MSE	Mean Square Error
MV	Motion Vector
NAL	Network Abstraction Layer
PE	Processing Element
PSNR	Peak Signal-to-Noise Ratio
PU	Processing Unit
QCIF	Quarter Common Intermediate Format
QFHD	Quad Full HD
QSAD	Quarter-Pixel Sum of Absolute Difference
QP	Quantization Parameter
RD	Rate-Distortion
RGB	Red-Green-Blue
SAD	Sum of Absolute Differences
SATD	Sum of Absolute Transformed Differences
SDTV	Standard-Definition TV
SIF	Source Input Format
SME	Sub-Pixel Motion Estimation
SMV	Sub-Pixel Motion Vector
SP	Simple Profile
SR	Search Range
SRAR	Shift Right Arithmetic Register
SRR	Shift Right Register
SSD	Sum of Square Differences

UD	Ultra-High Definition
VCEG	(ITU-T) Video Coding Experts Group
VCL	Video Coding Layer
VBS	Variable Block-Size
VBSME	Variable Block-Size Motion Estimation
VLSI	Very Large Scale Integration
xDSL	(Different variants of) Digital Subscriber Line