DESIGN OF CAPACITIVE SENSOR INTERFACING CIRCUIT USING 0.18 µm COMPLEMENTARY METAL OXIDE SEMICONDUCTOR TECHNOLOGY

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ABSTRAK

Semenjak beberapa tahun kebelakangan ini, kita dapat melihat dengan jelas bahawa sensor digunakan dalam beberapa bidang terkenal seperti industri otomotif, elektronik pengguna dan peralatan perubatan. Fungsi sensor ini adalah untuk menukar tenaga domain kepada bentuk tenaga lain seperti (magnetik, kimia, terma, mekanik atau optik) ke dalam kuasa domain. Antara sensor yang terpenting adalah sensor kapasitif. Projek ini adalah bertujuan untuk menunjukkan kebaikan atau kelebihan sensor ini apabila diaplikasikan di dalam suis RF MEMS dimana suis tersebut mempunyai aplikasi tanpa wayar seperti antena, penapis, pengubah fasa dan sebagainya. Litar yang direkabentuk didalam projek ini menggunakan 0.18μM Silterra teknologi CMOS dan disimulasikan dalam Mentor Graphic DA-IC. Sensor kapasitif yang dicadangkan merangkumi dua blok utama, dimana salah satunya adalah arus cermin ayunan-lebar dengan galangan keluaran yang telah dimodifikasi. Penguat transkonduktansi operasi (OTA) merupakan bahagian kedua bagi litar ini. OTA yang dicadangkan dalam projek ini adalah OTA teleskop dua-tahap. Jika dibandingkan OTA teleskop dua-tahap ini dengan beberapa konfigurasi OTA yang lain, ia mempunyai kelebihan dari segi gandaan yang lebih tinggi, ayunan keluaran yang lebih tinggi dan hingar yang lebih rendah. Ini menjadikan ianya sangat sesuai digunakan dan memenuhi spesifikasi yang ditetapkan untuk projek ini. Kerja-kerja baru-baru ini menggunakan penyelesaian yang berbeza untuk mengukur sensor kemuatan. beberapa karya meliputi pelbagai kemuatan yang cukup besar tetapi keputusan yang tidak tepat dan beberapa karya-karya lain memberikan hasil yang tepat tetapi dalam lingkungan yang terhad. Sesuatu karya yang sama menggunakan teknologi CMOS 0.8-um dengan bekalan kuasa 5 volt. Ia juga menggunakan sumber yang mudah semasa tidak tepat. Dalam projek ini, konfigurasi sumber semasa yang lebih tepat telah dipilih dan direka. Juga, 78 dB-

keuntungan 6-mW OTA telah direkabentuk dan dioptimumkan. Litar antara muka adalah kombinasi sumber semasa makan kapasitor MEMS mengukur dan kapasitor rujukan CMOS, dan OTA yang meningkatkan isyarat langkah ke tahap yang sesuai untuk membaca. Selain itu, projek ini meliputi pelbagai kapasitif 1000 dan seterusnya yang lebih luas daripada kerja-kerja yang sama. Reka bentuk manfaat teknologi CMOS,18-um yang membawa kepada cip saiz yang lebih kecil daripada kerja-kerja yang serupa.

ABSTRACT

In recent years, sensors are becoming ubiquitous in several fields such as automotive industry, consumer electronics and medical equipment. The function of the sensor is to convert energy from other energy domain like (magnetic, chemical, thermal, mechanical or optical) into the electrical domain. One of the important sensors is the capacitive sensor. The aim of this project is to show the advantages of this circuit while it is applied in the RF MEMS switches, which have wireless applications such as antennas, filters, and phase shifters, and so on. In this project, the circuits are designed using 0.18µm Silterra CMOS technology and simulated in Mentor Graphic DA–IC. The proposed capacitive sensor includes two major building blocks. One of them is a wide–swing current mirror with enhanced output impedance. The second part of the circuit is an operational transconductance amplifier (OTA). The proposed OTA in this project is a two–stage telescopic OTA that compared to the other types of OTA, it has higher gain, highest output swing and lower noise which are suitable for our target. It has been concluded that, our proposed project will be compared with some other capacitive MEMS sensor interface circuits which are presented in other papers. The recent works use different solutions to measure the capacitance sensor. Some works covers large enough capacitance range but inaccurate results and some other works give a precise result but in a limited range. A similar work used a 0.8-um CMOS technology with a 5-volt power supply. Also it uses a simple inaccurate current source. In this project, a more accurate current source configuration was selected and designed. Also, an 78dB-gain 6mW OTA was designed and optimized. The interface circuit is a combination of current source feeding the MEMS measure capacitor and CMOS reference capacitor, and an OTA which boost the measure signal to a suitable level for reading. Also, this project covers a capacitive range of 1000 fF

which is more extensive than similar works.The design benefits a 0.18-um CMOS technology, which leads to a smaller chip size than similar works.

ACKNOWLEDGEMENTS

I would like to thank my supervisor, Dr.Norhayatison , Associate Professor of the faculty of Electrical Engineering, for her guidance during this research. Without her guidance in choosing the Title , planning the experimental work, providing facilities, and preparation of the manuscript, this work would never have been done.

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I would like to express my appreciation to Puteri Fasaya and Jeffry Lee for providing me with the use of the measurement facilities from their experiment stations. Without their assistance, the experimental work could not be done. Also, I am indebted to the Emerald system group for their support.

Finally, I want to thank my parents for their constant support and encouragement

Throughout the courses of this work, and especially through the harder times.

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CHAPTER I: INTRODUCTION

1.1 MOTIVATION

The first integrated circuit (IC) logic for business was born in 1960. Rapidly after that Moore law (Rabaey,et.al, 1996) predicted that the number of transistors that can be integrated on a particular die would develop exponentially by time. As he predicted, the number of logic gates for each IC chip has increased from a single digital to multi-million and the price of chip has dropped radically (Rabaey, et al., 1996).

Following IC development in 1960s, "Micro Electro Mechanical System" (MEMS) technology has emerged. By applying particular silicon etching technology, three-dimensional micro sensors were successfully shaped. Since early 1997, this sort of etching technology was named as "micromachining". It was extensively being used for neural probes, pressure sensors, gas chromatography columns and other devices (Wise, 1998).

It is apparent that for many years, IC and MEMS technologies were implemented separately; but recently it has been considered that these two technologies can be combined on a common substrate such as micro-sensors, micro-actuators and microelectronics. This is the reason that electronic world has led to high performance and low cost devices. Also, spread data assembly and control have become ever more developed.

One of the important applications of MEMS is the RF MEMS switch which has widespread use in wireless telecom, automotive and industrial applications; in this project, RF MEMS switches are briefly discussed. This project aimed to design the capacitive sensor interfacing circuit for the output monitoring of the RF MEMS switches.

RF MEMS switch is a switching device that is created in the micromachining process. Mechanical dislocation of a deliberately moving structure leads to the turning between the on and off status. (Patranabis, 2004)

It is known that, the function of sensor element is to convert the energy from any energy domain to electrical domain; this project is aimed to change the energy from output RF MEMS switch to voltage using one capacitive sensor interfacing circuit. The mentioned circuit has been designed in a 0.18 μm CMOS technology and simulated in Mentor Graphic DA-IC software.

1.2 OBJECTIVE

The major goal in this project is to design and optimize a single-ended to differential capacitive sensor interface circuit. A topology that was chosen contains two main building blocks. So, the project is listed as the following steps:

To select the configuration of interface circuit for capacitive MEMS sensor application,design a precise current mirror (CM) to feed measure and reference capacitors ,design a high-gain operational transconductance amplifier (OTA),combine CM, OTA and capacitors to design a single-ended to differential capacitive sensor interface circuit; so the common-mode interferences can be easily removed and gain is doubled and achieve a higher capacitive range and a more precise measure from interface circuit.

Problem Statement:

- Is the accuracy of interface circuit output affected by the accuracy of current source?
- Is output resolution affected by OTA gain?

- Is the output result affected by common-mode noises? If so, is a single-ended to differential configuration useful?
- Is the selected configuration reasonable in size and power consumption for mobile applications?

What are the advantages of using a more modern CMOS technology for this project?

The main goal in this project to configure a topology for a single-ended to differential capacitive sensor interface circuit with new CMOS technology. In addition, each block of this topology is designed with a different circuit configuration.

1.3 BACKGROUND OF STUDY

Measurement is essential for observing and testing scientific and technological investigation. Instruments are developed for monitoring the condition of physical variables and converting them into symbolic output forms. They are designed to relationship between the parameters being measured and the physical variables under investigation. The physical parameter being measured is known as "measured". The sensors and transducers are primary sensing elements in the measuring systems. Sensors sense the physical parameters to produce an output. The output formed by a sensor is supplied to a transducer which converts energy from one form to another. Therefore, a transducer is a device that is capable of transferring energy between two physical systems.

The sensors and transducers can be categorized in a number of ways depending on the energy input and output, input variable, sensing elements and electrical or physical principle, for example, from an energy input and output. From a point of view, there are three fundamental types of transducers: modifiers, self-generators, and modulators. (Pallas-Areny, et.al, 2001)

A brief expression about the importance of sensors in recent technology was mentioned above. The major purpose of this project is to design a sensor interface. Therefore capacitive sensors have been selected. This project contains the study about types of capacitive sensors and also their advantages and disadvantages.

Figure 1.1 shows the overview of main block of, this circuit which is a simple schematic that can explain the main work of this project. There are three main building blocks in this circuit:

- Current source
- Capacitor for sensing
- Operational transconductance amplifier (OTA)

According to mention blocks which are needed in order to design this capacitive sensor interface circuit, the backgrounds of this study are as follow:

1. Study of current mirror, compare the types of current mirror and finally design of most suitable current mirror. This part of our project has the duty of the charging and discharging of sensing capacitors.
2. Study of amplifiers and specially OTAs (operational transconductance amplifiers), select the most appropriate topology and design, simulate and optimize the proposed circuit.
3. Study of capacitive sensors and achieve the principles in this field.

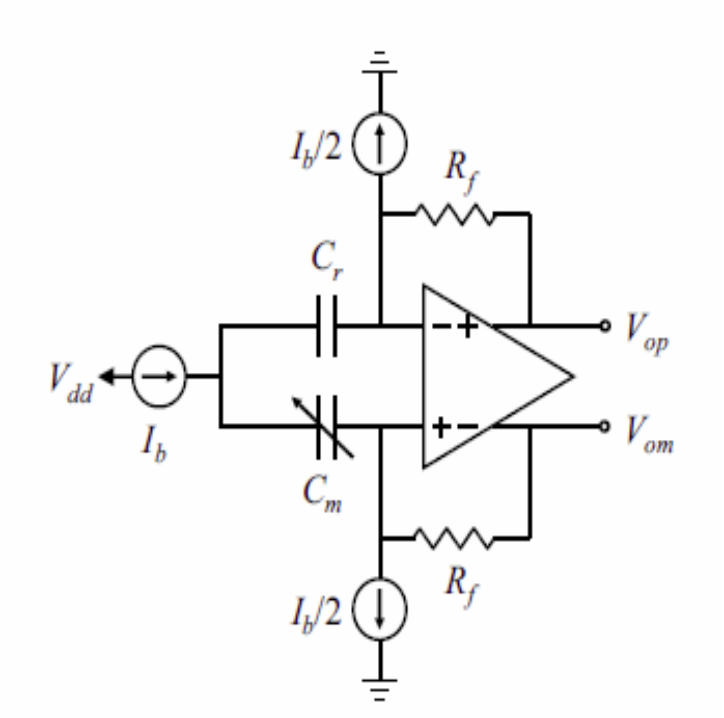

Figure 1.1 Overview of main block (Singh & Ytterdal, 2004)

The circuit was simulated in Mentor Graphics Design Architect IC (DA-IC) using 0.18 µm CMOS technologie.

1.4 ORGANIZATION OF THE CHAPTERS

Chapter two contains the literature review that represents recent related works and theoretical descriptions.

Chapter three discusses the methodologies and circuit configurations that have been used in this project; the design and optimization theories will be stated in this chapter.

The achieved simulation results from Mentor Graphics DA-IC are discussed in details and the optimization procedure for the circuit will presented in chapter four.

Chapter five presents the obtained results, conclusions and the future works for this circuit in RF MEMS switches application.

CHAPTER II: REVIEW OF RELATED LITERATURE

2.1 INTRODUCTION

The importance of capacitive sensor is obvious. Also, much work on MEMS sensors and their interface components has been done until now. The interface circuits use different circuit topologies depending on the specified applications.

2.2 RELATED WORKS

This project will tend to some works where was recently proposed. A similar work used a 0.8-um CMOS technology with a 5-volt power supply. Also it uses a simple inaccurate current source. In our project, a more accurate current source configuration was selected and designed a 89-dB-gain 10-mW OTA was designed and optimized. These modification and optimization are on the following issues :

- Single –ended to differential capacitive sensor interface circuit
- Current-Mode Capacitive Sensor Interface Circuit
- Real-Time Monitoring of Contact Behavior of RF MEMS Switches With a Very Low Power CMOS Capacitive Sensor Interface

2.2.1 Single–Ended–To–Differential Capacitive Sensor Interface Circuit

A single–ended–to–differential capacitive sensor interface circuit is significant for designing this circuit. This circuit is also simulates in Mentor Graphic software using a 0.8–μm CMOS technology. This circuit is focused on the converting single-ended to differential input.

2.2.1.1 Main Equation in This Circuit

The concept of their single-ended to differential capacitive sensor is based on the simple equation for the current in a capacitor as follows (Singh & Ytterdal, 2004):

$$I = C\frac{dV}{dt} \tag{2.1}$$

A simple diagram of the circuit input is shown in figure 2.1. Here, a sensing capacitor C_m and a reference capacitor C_r are presented. The current source I_b acts as the DC bias current in order to charge both capacitors. Throughout this work, the bias current is a DC mirror current.

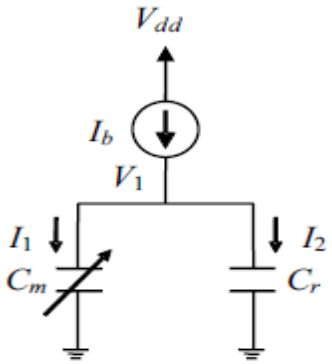

Figure 2.1 single–ended–to–differential capacitive sensor interface circuit (Singh & Ytterdal, 2004)

At Nominal, $C_m = C_r$ and$I_1 = I_2$, that increase of C_m with respect to C_r causes, increase in I_1 and a decrease in I_1. The sensed signal current is produced by difference of the two currents. This is the method that is applied throughout our work.

The following equation shows currents that flow through the two capacitors in this circuit(Singh & Ytterdal, 2004):

$$I_{1=C_m}\frac{dV_1}{dt} = \frac{I_b}{2} + \frac{i}{2} \tag{2.2}$$

$$I_{2=C_r}\frac{dV_1}{dt} = \frac{I_b}{2} - \frac{i}{2} \tag{2.3}$$

where I_b is a DC current. (Singh & Ytterdal, 2004):

$$\frac{dV_1}{dt} = \frac{I_b}{C_m + C_r} \tag{2.4}$$

Let's assume that the two capacitors can be matched. That means that a unit capacitance equal to C can be chosen for both capacitors. So, C_m =(C+ΔC) and C_r = C, where ΔC is the capacitance variation of the sensing capacitor around its nominal value of C.

By combining equations (2.3) and (2.4) (Singh & Ytterdal, 2004) using the assumptions mentioned above, the following equation is obtainable for the difference $I_1 - I_2$, the current I which is identical to: (Singh & Ytterdal, 2004)

$$\mathrm{I} = \frac{I_b \Delta C}{2C + \Delta C} \tag{2.5}$$

The advantage of this circuit is the main topology that maintained; but the signal current can be measured differentially in order to produce a differential output voltage. Therefore, the voltage at the bottom plates of the measurement capacitance and the reference capacitance is maintained at the common mode voltage using the feedback loop.

2.2.1.2 CMOS DESIGN

The interface circuit was designed using a 0.8µm CMOS process. The schematics of the interface circuit and the amplifier can be respectively seen in figure 2.2 and 2.3.

A fully differential miller OTA was used to realize the transimpedance amplifier. The current mirror below (M21–M29), which is providing the charging current to the capacitors, uses an enhanced output impedance wide-swing current mirror topology to achieve the high output impedance; therefore, as the voltage across the capacitors rises, it ensures that the charging current remains relatively constant regardless of growing drain voltage of the current mirror transistors.

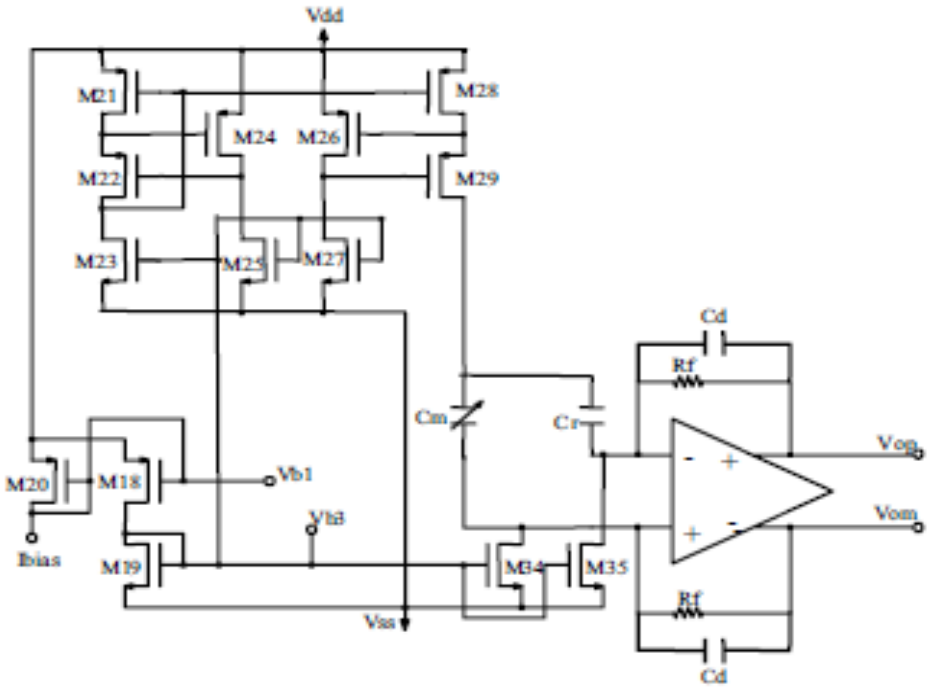

Figure 2.2 Schematic of the CMOS interface circuit (Singh & Ytterdal, 2004)

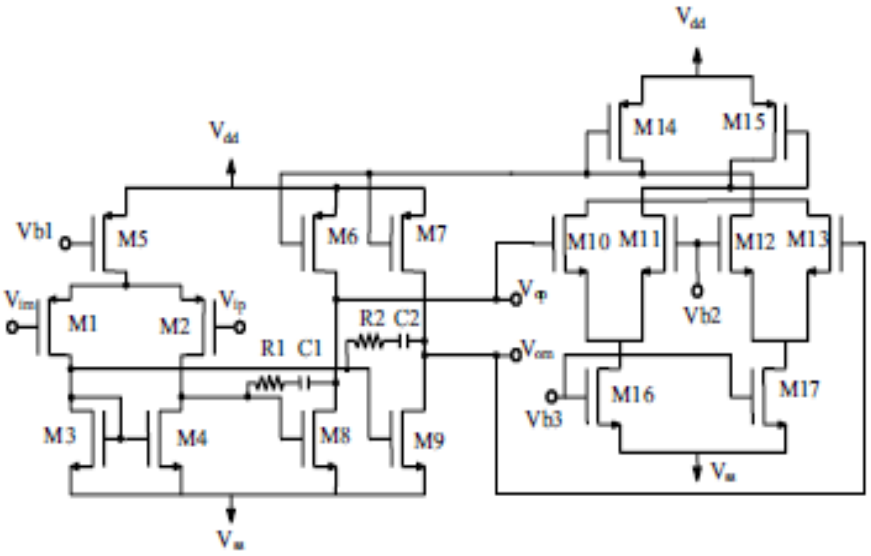

Figure 2.3 Schematic showing the fully differential Miller OTA(Singh & Ytterdal, 2004)

All the simulations were performed with the Eldo from Mentor Graphics using AMS 0.8µm CMOS device models. DC supply voltages, V_{dd} and V_{ss} were got 5 volt and 0 volt, respectively. Moreover , the nominal charging current was about 2.5 µA. Note that it does not matter to set the charging current to a specific value as long as it is stable over time; because the system can take the enough reset time for avoiding the current–mirror transistors to enter the linear region . (Singh & Ytterdal, 2004)

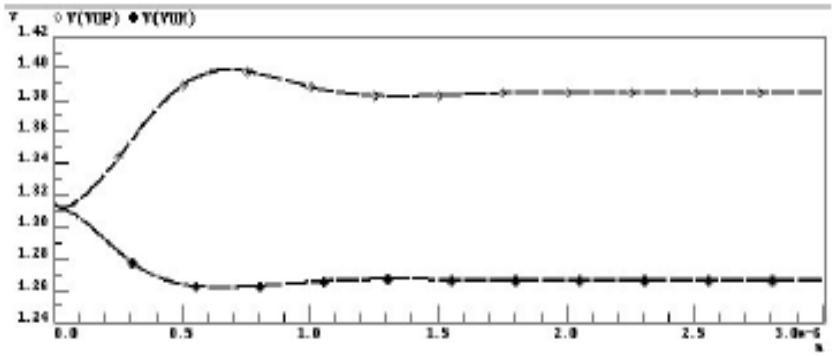

Figure 2.4 Reported transient output voltage waveforms(Singh & Ytterdal, 2004)

Table 2.1 Summary of results (Singh & Ytterdal, 2004)

Maximum output swing	118.5mV
RMS output noise voltage relative to full scale	0.28%
Maximum static error in the output voltage (caused by mismatch and finite output resistance of the current mirrors)	0.026%
Total current consumption	125μA

There are other papers which follows similar approach such as the one described above; one of them is explained here. Actually the following paper is the optimized version of the above circuit. This paper uses the capacitive sensor interface circuit as the current mode. Also, It uses the same single–ended to differential output capability as the previous paper described.

2.2.2 Current-Mode Capacitive Sensor Interface Circuit

Since the principle and equations are the same as previous discussion, about the new circuit, briefly. Differential configuration are commonly used in signal shaping by reason of their ability to reject common–mode effects such as supply and bias variations, interference, and substrate noise. Since the signal is injected and also the output is read out through two balanced paths, the common mode rejection is achieved. In the case of fully differential circuits, since signals were defined relative to each other, errors cancelation is achieved; because they are common to both paths. However, fully differential circuit is obtained the cost of approximately doubling the chip area and power consumption as compared to the equivalent signal–ended configuration. Differential realizations and their other advantages are covered in detail in the literatures (Graeb,et.al, 2001; Hu,et.al, 2002).

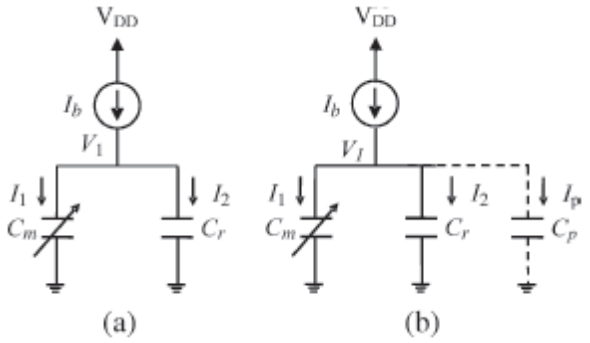

Figure 2.5 (a) a simple schematic of how a differential signal is obtained from single ended sensor capacitance. (Singh,et.al, 2009).

The sensor capacitance and a fixed reference capacitor are represented by C_m andC_r, respectively. Both capacitors are equal to a nominal capacitance value C. Thus, C_m=C_r=C; Therefore, the charging current I_b equally branches between C_m andC_r. Let's assume that C_m strays from its nominal value by a time-invariant shift while measurement (ΔC). The equation for I_1 and I_2 become the same as previous expression (2.2) and (2.3).

The only difference between these two theories is that the Stray capacitance C_p at nod V_1 modifies the transfer function, as shown in figure2.6.

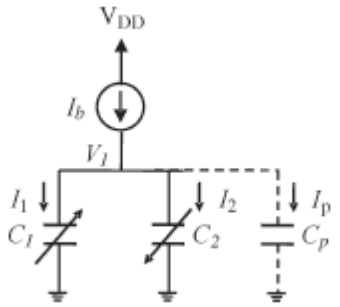

Figure 2.6 The stray capacitance C_p at node V_1 (Singh, et .al, 2009).

This capacitance is the sum of plate stray capacitance of C_m andC_r, routing capacitance, and the output capacitance of the current sourceI_b. The equation is modified for the signal current due to C_p as follows (Singh, et.al, 2009).:

$$i = \frac{I_b \Delta C}{2C + \Delta C + C_p} \tag{2.6}$$

Capacitors $C_1 and\ C_2$ have same nominal value C. It can simply be shown that the differential signal current is now represented by:

$$i = \frac{I_b \Delta C}{2C + C_p} \tag{2.7}$$

Where ΔC is the deviation from nominal value for each C_1 and C_2, so that C_1=$C + \Delta C$ and C_1=$C - \Delta C$.

2.2.2.1 Circuit realization

Reference (Singh & Ytterdal, 2004) presents a possible circuit realization using a fully differential TIA and related simulation results. A fully differential configuration was selected because of its advantages which are discussed earlier. Figure 2.7 shows the block diagram for such a realization.

A fully differential operational transconductance amplifier (OTA) with feedback resistors *Rf*1 = *Rf*2 (with a nominal value *Rf)* were used to realize the differential TIA. A circuitry to drive the components off chip was added in the prototype which can be seen as the dotted portion. Accordingly, the output voltage of the prototype *V*out_*b* was experimentally measured.

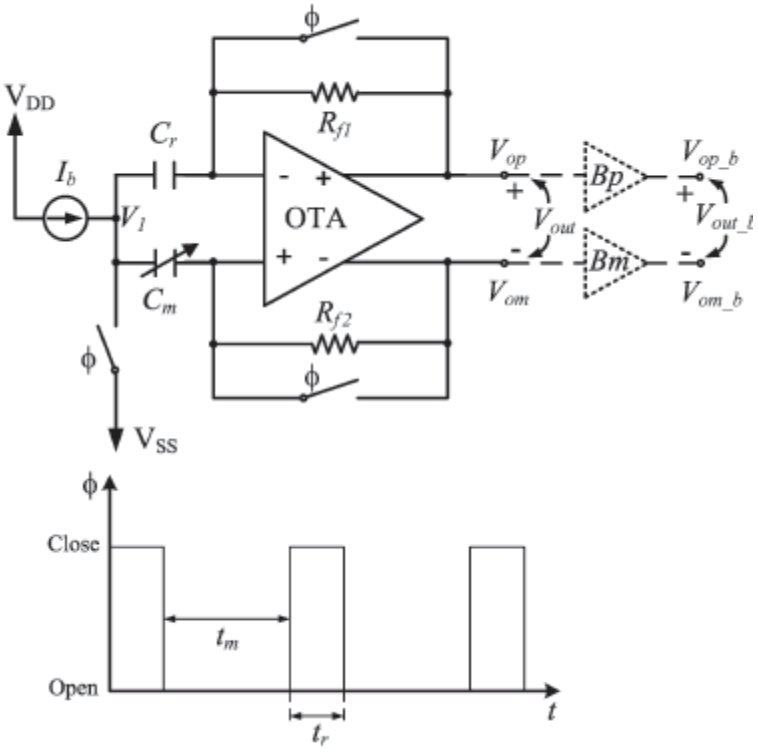

Figure 2.7 Block diagram of interface circuit (Singh et al., 2009).

Three switches were realized by MOS transistors. The FET switched were driven by the clock phase φ and used periodically to reset the circuit after each measurement. The supply voltages V_{DD} and V_{SS} are 5 and 0 volts, respectively. In the amplifier, the common–mode voltage (analog ground) was set to 1.2 volt as band-gap reference level. The node *V*1 is periodically reset to *VSS* after each measurement by the switch on that node.

The circuit operation is as follows. The switch at node *V*1 reset that node to V_{SS} during the reset period "t_r". Following the reset period, all switches are opened during the measurement period "t_m". The charging current I_b is disported between C_m and C_r, depending on ΔC; Accordingly, this creates a differential signal current as expressed in equation (2.7) (Singh & Ytterdal, 2004). An output voltage is created by passing this signal current through the feedback resistors, along with the common-mode current. Reading the output differentially causes that the common-mode effects are rejected. The output is read

just before the measurement period finishes (or after settling of the amplifier output). The circuit is reset once again to make it ready for the next measurement period.

Let's assume an ideal amplifier; the differential output voltage which is result of the input signal current can be given as: (Singh, et al., 2009).

$$V_{out} = V_{op} - V_{om} = R_f \cdot i = R_f \, I_b \frac{\Delta C}{2C + \Delta C} \tag{2.8}$$

And after solving above equation, the below equation is obtained: (Singh, et al., 2009).

$$\Delta C = \frac{2C.V_{out}}{R_f I_b - V_{out}} \tag{2.9}$$

This equation is used to calculate ΔC depending on the measured output voltage.

2.2.2.2 CMOS Realization

Figure 2.8 shows the final realization of the prototype in a 0.8-µm CMOS technology excluding reset switches. Transistors M21–M29 form an enhanced output resistance current mirror (Martin & Johns, 1997) which is providing charging current to capacitors C_m and C_r. A common two-stage Miller OTA (Laker & Sansen, 1994) is implemented with 90-dB open-loop gain, 490-kHz gain-bandwidth product (GBW), and 80° phase margin. The resulting 3-dB cut-off frequency of the TIA was about 400 kHz. The capacitors C_d parallel to resistors R_{f1} and R_{f2} are due to compensating lag in order to improve the transient response of the TIA (Hoyle & Peyton, 2002). The accuracy

requirement dictates the most important OTA parameters for this application such as the open-loop gain, GBW, settling time, and slew rate (Laker & Sansen, 1994). A nominal value equal to 1 pF was chosen for C_m and C_r. The feedback resistors determine the transimpedance gain figure2.8. 200-kΩ resistors were used for the prototype. There were prime compromises for determining the resistor value between high gain and output swing on one hand and among the input resistance, noise, and chip area on the other hand. Determining charging current basically depends on the voltage allowance at *V*1, the size of capacitors *Cm* and *Cr*, and the measurement period. According to these conditions, a charging current equal to 2.5 μA was considered.

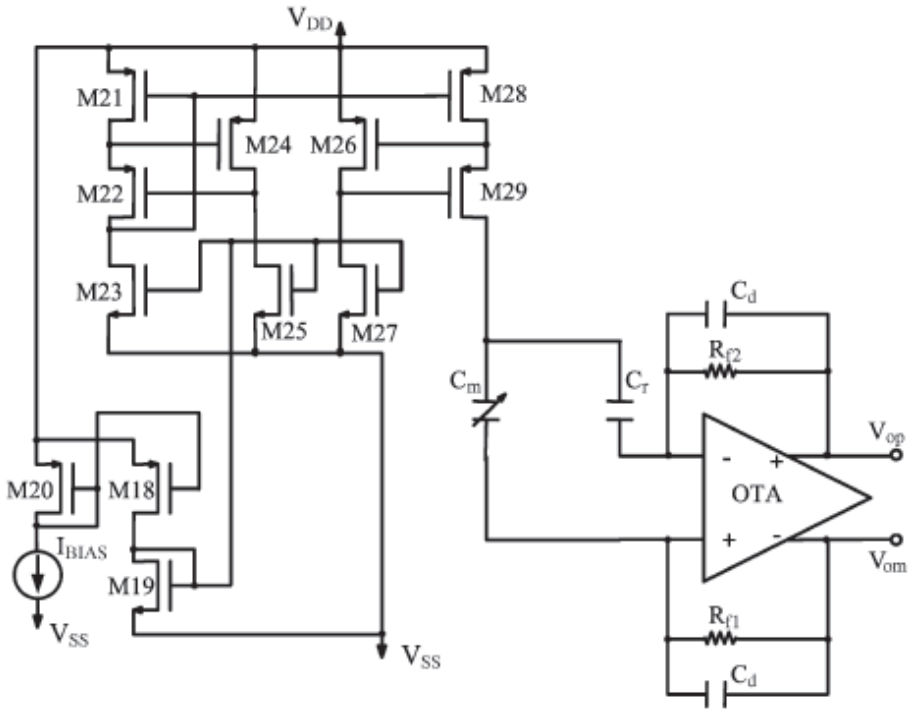

Figure 2.8 Capacitive sensor interfacing circuit CMOS realization (Singh et al., 2009).

Being stable over time for the charging current source is more important rather than being accurate to a specific value; because a constant offset in the current value will produce just a gain error; and it is possible to easily remove this error with applying

calibration. In addition, note that the current source which is supplying current should represent acceptably low reliance on the voltage V_1; So that the δI term does not impose more nonlinearity to the output than tolerable. As discussed above, the complexity of the proposed circuit is restricted to the enhanced output–resistance current–mirror and fully differential OTA designs; both configurations are widely discussed in the literature.

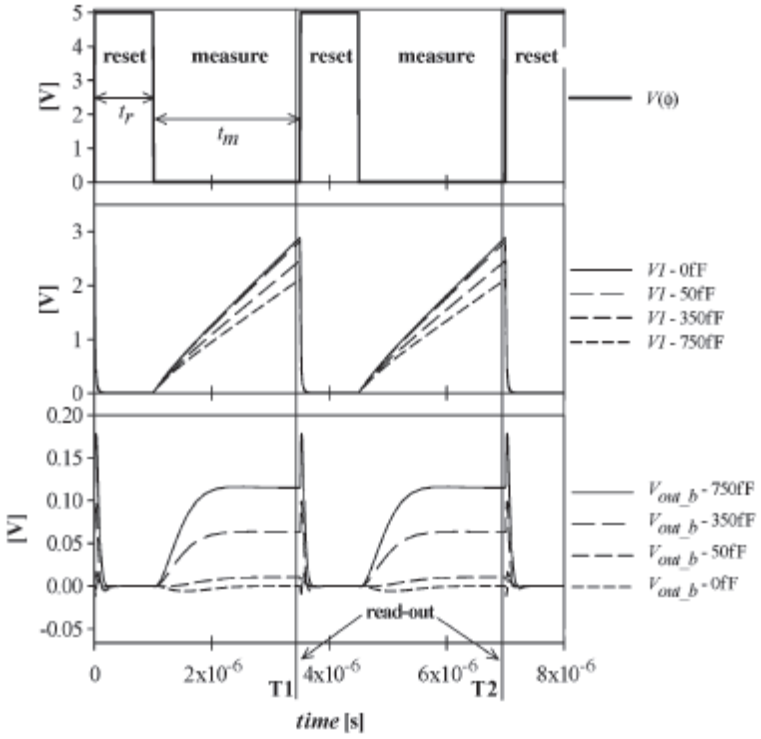

Figure 2.9 Simulated transient response for different value of ΔC (Singh et al., 2009).

The transient response of the prototype circuit is shown in figure 2.9. Clock timings that are used to control the reset switches, were optimized during simulations so that there was enough reset time to discharge the capacitors and enough measurement time to settle the system output. The reset switches are driven by a clock frequency of 285 KHz with a duty cycle of 28.57% and t_m equal to 2.5 μs and t_r equal to 1 μs. At the end of the measurement period t_m, the output is read out. Notice that the major requirement for the clock is to provide enough time such that the capacitors can be fully discharged in the reset

period and amplifier is allowed to settle in the measurement period. After the amplifier is settled, the output can be read out at any time. (Singh, et al., 2009)

2.2.3 Real-Time Monitoring of Contact Behavior of RF MEMS Switches With a Very Low Power CMOS Capacitive Sensor Interface

Another article is discussed that has also worked on capacitive interface circuit. Capacitive sensor interface is used in this paper to read out from RF MEMS switch. The pulse-width-modulated signal (PWM) block acts as a semi-digital readout circuit of capacitance. The pulse width is a function of the RC time constant. The resistance is a constant and determined value, and the capacitance rises as the switch are short. Consequently, the circuit is intrinsically linear. Due to the digital configuration of the circuit, it is allowed to directly connect the output to a microprocessor to collect the real–time data.

The input voltage is compared with the supply voltage $V_{DD}/_2$ by low-power-consumption self-tuning comparator. As soon as the voltage across the capacitance is more than 2 volts, the output of the sensor interface circuit sets low. The voltage across the capacitor (V_C) can be found out as shown in equation (2.10). (Fruehling, et.al, 2010).

$$V_c = V_{DD} e^{-t/RC} \tag{2.10}$$

$$V_C = \frac{V_{DD}}{2} = V_{DD} e^{\frac{-T}{RC}} \tag{2.11}$$

From Equation (2.10) and (2.11), T can be easily solved as shown in equation (2.12) (Fruehling, et al., 2010).

$$T = RC\ln(2) \tag{2.12}$$

It can be seen that timing differences as measured by the circuit are linearly dependent on the measured capacitance changes. Such as, the circuit's readout is independent of parasitic or reference capacitances. In order to eliminate any DC offset due to charge buildup over time, the transistor connected in parallel with the sensed capacitance is used to reset the voltage across the capacitor (Fruehling, et al., 2010). The maximum capacitance that can be read is limited by the clock high time (T_{HIGH}) and clock low time (T_{LOW}). Mathematically, this is represented in Equations (2.12) and (2.13) (Fruehling, et al., 2010).

$$C_{MAX} = \frac{T_{HIGH}}{R\ln(2)} \tag{2.12}$$

$$C_{MAX} = \frac{T_{LOW}}{5(r_{ON} \| R)} \tag{2.13}$$

2.2.3.1 Experiments and Results

The electronic measurements are obtained while the sensor is in connection with to the interface circuit as can be seen in figure 2.10. The raw output signal of the circuit is shown in figure 2.11 with a biasing time- synchronized waveform. While the bias is at zero potential, the gap is at its maximum value (in the off state); therefore, the capacitance at the contact has a minimum value; this value is approximately equal to 1 fF. At this status, the output pulse width is around 50% duty cycle. Since the beam moves toward the contact

upon actuation and the capacitance rises, this results in a rise in the duty cycle until contact. This transition between increasing and decreasing duty cycles happens plenty of times during a switching episode as the beam jumps up repeatedly. Since the beam relaxes in the closed state and is kept in contact, the duty cycle is fixed at 80%. This value is result of the crystal oscillator so that the output duty cycle cannot go beyond the clock duty cycle. Also, the reading of parasitic of the circuit and setup determines the minimum duty cycle which is approximately 50%.(Fruehling, et. al, 2010)

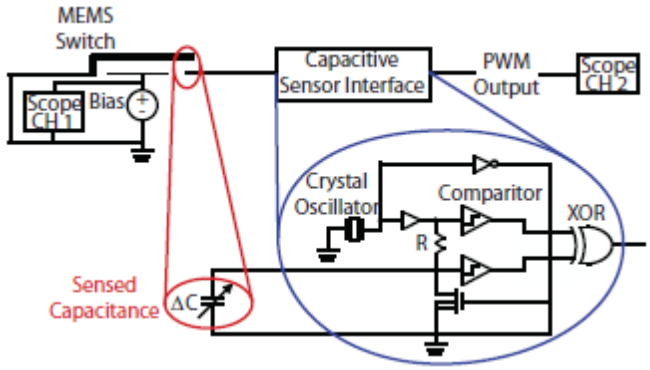

Figure 2.10 Experimental setup for measuring capacitance change of device in motion. (Fruehling ,et .al, 2010).

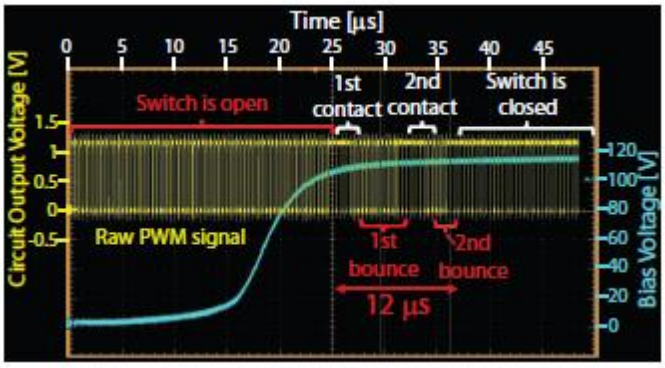

Figure 2.11 Oscilloscope capture of raw pulse-width modulated data and biasing for switch bouncing event with a synchronized time scale. (Fruehling ,et .al, 2010).

2.3 CAPACITIVE SENSOR

However this kind of sensors (capacitive sensor) are classified in two categories: (1) single capacitive sensors, which include only one sensing element and, (2) differential capacitive sensor (also known as push-pull half-bridge sensor) which have two sensing elements. The latter represents intrinsic advantages: for example, the effect of unwanted inputs (e.g. temperature) which are affecting both sensing elements in equal, are rejected. Because of this, the differential capacitive sensors are extensively applied to measurement acceleration, pressure, strain, linear and angular positions, and displacement.

Differential capacitive sensors typically contents three parallel plates with central plate being movable and the outer plates being immovable). These sensors can be characterized by two sensing capacitances (i.e. C_1 and C_2) using a common electrode as shown in figure 2.12.

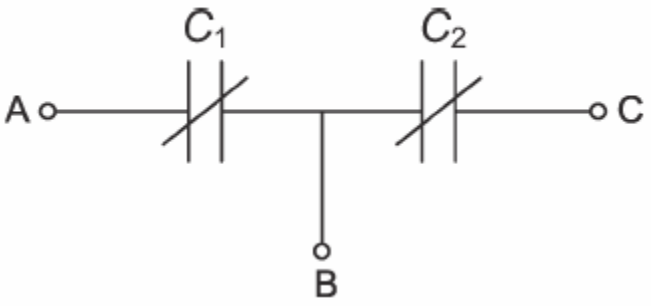

Figure 2.12 Equivalent circuit of differential capacitive sensor (Reverter & Casas,2010).

At rest time, the central plate is geometrically placed at center such that C_1 and C_2 are equal to the nominal valueC_0. For a parallel plate arrangement, $C_0$is equal (Reverter & Casas,2010):

$$C_0 = \varepsilon_0 \, \varepsilon_r \, \frac{A_0}{d_0} \qquad (2.14)$$

Where ε_0 represents the electric permittivity of vacuum, ε_r represents the relative permittivity of the dielectric between plates, A_0 represents the nominal area of the plates, and d_0 represents nominal distance between plates. In practice, however, the central plate of the sensor moves. As a result, either the area or the distance between electrodes changes, and henceforth, both C_1 and C_2 change, but in opposite directions; such an effect can be due to differential variations of permittivity as well, though these are less common. If the area is changed , then C_1 and C_2 change linearly; therefore :(Reverter & Casas)

$$C_1 = C_0 \, (1 + x) \qquad (2.15)$$

$$C_2 = C_0 \, (1 - x) \qquad (2.16)$$

It is allowed to sense many different variables via measuring capacitance in capacitive sensors. These are variables like position, motion, acceleration, proximity, fluid level, humidity, and material composition. A capacitive sensor is a sensor that can directly detects proximity of objects according to their effect on the self-created electrical field by capacitive coupling of sensor. For many years, simple capacitive sensors has been using in marketing. Capacitive sensors are capable of detecting all objects which have conductivity or dielectric properties. Since the mechanical buttons can be substituted with capacitive sensing alternatives, capacitive sensing applications can be combined with other technologies such as multi-touch and gesture-based touch screens.

The capacitive sensors can be categorized in three groups as listed below:

1. Variable capacitance type: the distance between parallel electrodes is variable.
2. Variable capacitance which is result of variable area between the electrodes. A motivating variation of this is achieved by creating saw-like electrodes or electrodes with teeth and one with moves.
3. Variable capacitive which is result of variable dielectric constant of the intervening material. To achieve this, the material has to travel between the pair of electrodes. This results the change in capacitance which can be measured.
4. The variable capacitive which is result of the piezoelectric. This variable depends on the piezoelectric properties of specific sort of dielectrode materials. As shown in figure 2.13, the moving electrode of this type is controlled to have a short movement while movement of the dielectric material like an insulation tape is not controlled.

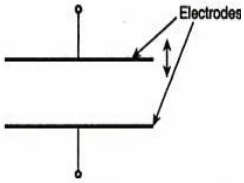

Figure 2.13 Simple capacitive (Reverter & Casas).

2.3.1 Basic Principle

In capacitive sensor, there are basic equations which are used for measuring the physical parameters while one of them or more is varying. The equation that is applied for capacitance: (Patranabis, 2004)

$$c = \varepsilon \frac{A}{d} \tag{2.17}$$

Where (ε) is as permittivity of the dielectric, (A) is as overlap area of the capacitor plate and (*d)* is as symbol for distance between two parallel plates.

It is interesting to note that for each application of capacitive sensor, one of these parameters is important and only that one is varying; for example, humidity sensors typically work based on varying the permittivity (ε), pressure sensor are based on varying distance (*d*) and position sensors are based on varying (*A)* or sometimes(*d).*

In this project, since this sensor application is for RF MEMS switch and it is required to sense the switch output. Hence, that type of sensing can be applied which is based on varying distance.

Three major types of capacitor sensor and basic equations are described briefly in this part.

2.3.2 The Parallel Plate Capacitive Sensor

In this type as shown in figure 2.14, a pair of parallel plates is used with a solid dielectric of a specific thickness x_s and air gap x_a . The capacitance C can be expressed as: (Patranabis, 2004)

$$c = \frac{a}{\left(\frac{x_a}{\varepsilon_a}\right) + \left(\frac{x_s}{\varepsilon_s}\right)} \tag{2.18}$$

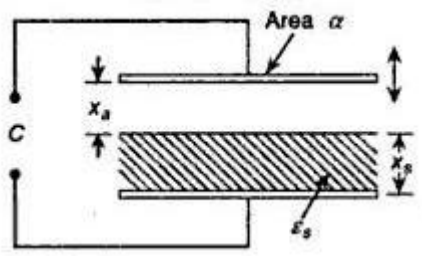

Figure 2.14 Parallel paite sensor with different dielectric materials (Patranabis, 2004).

While the plate is moving, a decrease in x_a causes an increase C and vice versa. So the below equation is applied : (Patranabis, 2004)

$$C + \partial C = \frac{a}{\left(\frac{x_a + \partial x_a}{\varepsilon_a} + \frac{x_s}{\varepsilon_s}\right)} \tag{2.19}$$

With considering $\varepsilon_a = 1$, for simplicity, then below equation is obtained: (Patranabis, 2004)

$$\pm\frac{\partial C}{C} = \pm\left(\frac{\partial x_a}{x_a + x_s}\right)\left(\frac{1}{\frac{1 + \frac{x_s}{x_a\,\varepsilon_s}}{1 + \frac{x_s}{x_a}} \mp \frac{\partial x_a}{x_a + x_s}}\right) \tag{2.20}$$

In equation (2.20), the significant factor for determining the value $+\partial c\,/\,c$ is the quantity of $(1 + x_s/(x_a\varepsilon_s))/(1 + x_s/x_a)$ .This quantity is denoted as 1/β where β is frequently referred to as the sensitivity factor; but it can also influence the nonlinearity.

expression $\left(\partial x_a/x_a\right)\Big/(1 + x_s/x_a) = \partial x_a/x_a/(1+\lambda)_0 \pm \partial C/C$ can be extended as: (Patranabis, 2004)

$$\pm\frac{\partial C}{C} = \pm\left(\frac{\partial x_a}{x_a}\right)\left(\frac{\beta}{1+\lambda}\right)\left[1 \pm \left(\frac{\partial x_a}{x_a}\,\frac{\beta}{1+\lambda}\right) + \left(\frac{\partial x_a}{x_a}\frac{\beta}{1+\lambda}\right)^2 \pm \cdots\right] \tag{2.21}$$

Since β is a function of x_a , x_s and ε_s , the plots of β versus λ with ε_s as a parameter show that while λ increases, β increases with its minimum value being 1 for ε_s =1.

Here, notice that capacitors have fringing effect which it should be usually avoided of plate both from being at the same potential.

2.3.3 Serrated plate capacitive sensor

According to earlier discussion, a change in capacitance is shown by a pair of flat serrated plates; one of the plates is fixed in position and the other has a small relative movement. This principle is employed in some cases to make us capable to measure small angular changes. The relative movement must be small for the measurement to be of any concept. Figure 2.15 shows the active tooth where *L* denotes as length (on the fixed plate, *x* denotes as air gap, and *w* represents as tooth width. if number of teeth-pair is as *n* and air permittivity is as ε_a, the capacitance C is expressed as: (Patranabis, 2004)

$$c = \frac{\varepsilon_{a\ lwn}}{x} \tag{2.22}$$

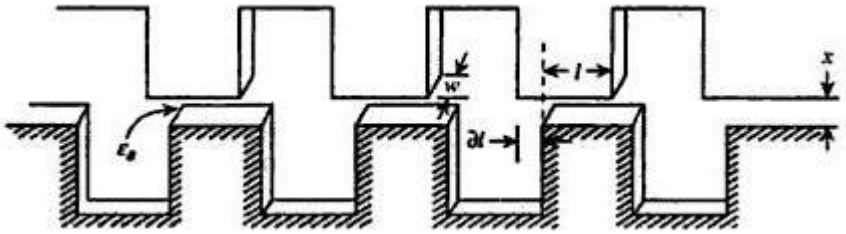

Figure 2.15 serrated electrode capacitance sensor with changing active length. (Patranabis, 2004).

Thus the below equation can be derived for small relative movement ∂l of moving plate: (Patranabis, 2004)

$$\frac{\partial C}{C} = \frac{\partial l}{l} \tag{2.23}$$

No fringing effect is assumed in this simplified relation. Nevertheless, the leakage can be allowed in the relation below by sketching real equipotential lines and parallel flux lines between the pair of teeth, so: (Patranabis, 2004)

$$\frac{\partial C}{C} = \frac{\partial l}{l}\left(\frac{1}{1+\frac{kx}{l}}\right) \tag{2.24}$$

Where the expression within the brackets can be termed as the sensitivity factor, βs , which decrease with increasing x/l as shown in figure 2.16. This factor βs is actually the ratio of nonleakage to total flux.

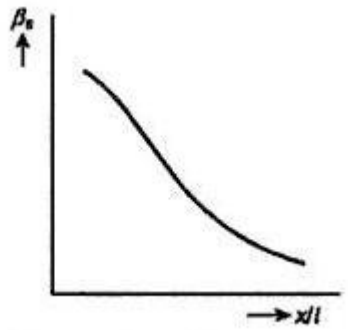

Figure 2.16 sensitivity versus normalized gap curve(Patranabis, 2004).

2.3.4 Variable Permittivity or Thickness Dielectric Capacitive Sensor

Figure 2.17 represents this type of capacitive with plate effective area α and other dimensions as shown in the figure2.17. The capacitance C is obtained by: (Patranabis, 2004)

$$c = \frac{\alpha}{l - x + \frac{x}{\varepsilon_d}} \tag{2.25}$$

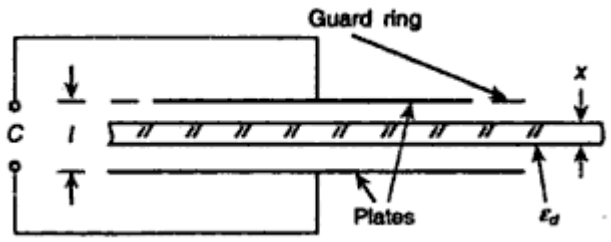

Figure 2.17 Scheme of variable permittivity (or thickness) dielectric type sensor (Patranabis, 2004).

Where ε_d is the permittivity of the dielectric material. Following the development in section 2.3.1 one, the normalized change in capacitance is obtained: (Patranabis, 2004)

$$\left(\frac{\partial C}{C}\right) = \pm\frac{\partial \varepsilon_d}{\varepsilon_d}\frac{1/1+\varepsilon_d((1-x)/x)}{1 \pm \frac{1}{1+x/\left(\varepsilon_d\,(1-x)\right)}.\frac{\partial \varepsilon_d}{\varepsilon_d}} \tag{2.26}$$

Here, $1/1+\varepsilon_d(1-x)/x$ is the sensivity factor β_s and the nonlinearity factor is $\eta_n = 1/\left(1+x/\left(\varepsilon_d(1-x)\right)\right)$. If $\eta_n \partial\, \varepsilon_d/\varepsilon_d$ is small, with first order approximation it can be obtained: (Patranabis, 2004)

$$\left(\frac{\partial C}{C}\right) = \frac{\partial x}{x}\,\frac{\frac{\varepsilon_{d-1}}{1+\varepsilon_{d(1-x)/x}}}{1 \pm \frac{\varepsilon_d - 1}{1+\varepsilon_d(1-x)/_x}\frac{\partial x}{x}} \tag{2.27}$$

And if $[(\varepsilon_d - 1)/1+\varepsilon_d(1-x)/x] << 1$, taking the first order term only, the equation for $(\partial C/C)$ is obtained as: (Patranabis, 2004)

$$\left(\frac{\partial C}{C}\right) = \frac{\partial x}{x}\frac{\varepsilon_{d-1}}{1+\varepsilon_{d(1-x)/x}}\left[\,1+\frac{\varepsilon_d - 1}{1+\varepsilon_d(1-x)/_x}\frac{\partial x}{x}\right] \tag{2.28}$$

The sensitivity factor and the nonlinearity factor are identical and equal to $(\varepsilon_d - 1)/1 + \varepsilon_d(1 - x)/x$ .Patranabis claimed that the sensitivity is acceptable with high $x/(1 - x)$ as also ε_d but the nonlinearity also growths.(Patranabis, 2004)

2.3.5 Capacitive Sensor Application

Unintentionally, all these sort of capacitive sensors have very extensive usage and have a lot of applications, for example:

- Flow – flow is transformed to pressure or displacement by many sorts of flow meters; such that a cavity or Coriolis Effect force is employed for volume flow or mass flow, respectively. Capacitive sensors can measure the changing in distance.
- Pressure – Employing a diaphragm with constant deflection characteristic, pressure can be measured by a detector that can sense changing in space.
- Liquid level – there are capacitive liquid level detectors which sense the liquid level in a tank; for this case, they measure changes in capacitance between conducting plates. These plates are plunge in the liquid, or applied to the outside of a non-conduct tank.
- Spacing – approaching a metal object to a capacitor electrode, the common capacitance is very sensitive for measuring the space.
- Scanned multi-plate sensor – by extending single-plate spacing measurement to contour measurement with use many plates, each of plates can be separately addressed; and they can measure both conductive and dielectric surfaces.
- Thickness measurement – using two plates in contact with an insulator will help measuring the insulator thickness while its dielectric constant is known or the dielectric constant while the thickness is known.

- Ice detector in airplane – by employing insulated metal in wings edges; airplane wing icing can be detected at wing leading edges.
- Shaft angle or linear position – Capacitive sensors are capable to measure angle or position using a multi-plate design that gives high accuracy and digital output, or with an analog output with less absolute accuracy but faster reply and simpler circuitry.
- Lamp dimmer switch – The common metal-plate soft-touch lamp dimmer uses 60–Hz excitation and senses the capacitance to a human body.
- Key switch – Capacitive key switches employs the shielding effect of an adjacent finger or a touching conductive plunger to interfere the coupling between two small plates.
- Limit switch – The proximity of a metal machine component or a plastic component can be detected as an increase in capacitance by limit switches using virtue of its increased dielectric constant over air.
- X-Y tablet – computer mouse as an x-y coordinate input device can be replaced by capacitive graphic input tablets with different sizes. However, finger-touch-sensitive, z-axis-sensitive and stylus-activated devices are available.
- Accelerometers – Analog Devices has introduced integrated accelerometer ICs with a sensitivity of 1.5g. The device can be used as a tilt-meter with this sensitivity.

2.4 CURRENT MIRROR

2.4.1 Basic current mirrors

The principle of current sources in analog circuits is based on "copying" current from a reference, with the assumption of availability of precisely–defined reference current source. Since this method may seem to involve an infinite cycle, it is implemented as illustrated in figure 2.18.

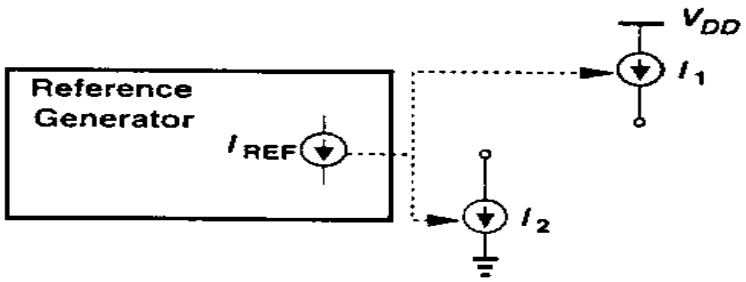

Figure 2.18 Use of a reference to generate various currents (Razavi, 2000).

For a MOSFET, if $I_D = \mathcal{F}(V_{GS})$, where $\mathcal{F}(0)$ denotes the

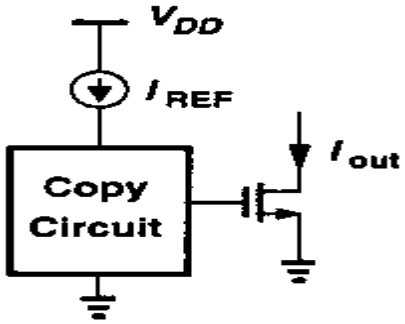

Figure 2.19 Conceptual means of copying currents (Razavi, 2000).

V_{GS} is a function of I_D as $V_{GS} = f^{-1}(I_d)$. This means, since a transistor bias current is equal to I_{REF} , Then the transistor produces $V_{GS} = f^{-1}(I_{ref})$, as shown in figure 2.20.(a). Hence, if the same voltage is applied to the gate and source terminals of another MOSFET, the output current results as $I_{out} = f(f^{-1}(I_{REF})) = I_{REF}$ figure 2.20.(b). From another point of view, two identical MOS devices with the same gate-source voltages and operation in saturation region carry equal currents (if $\lambda = 0$).

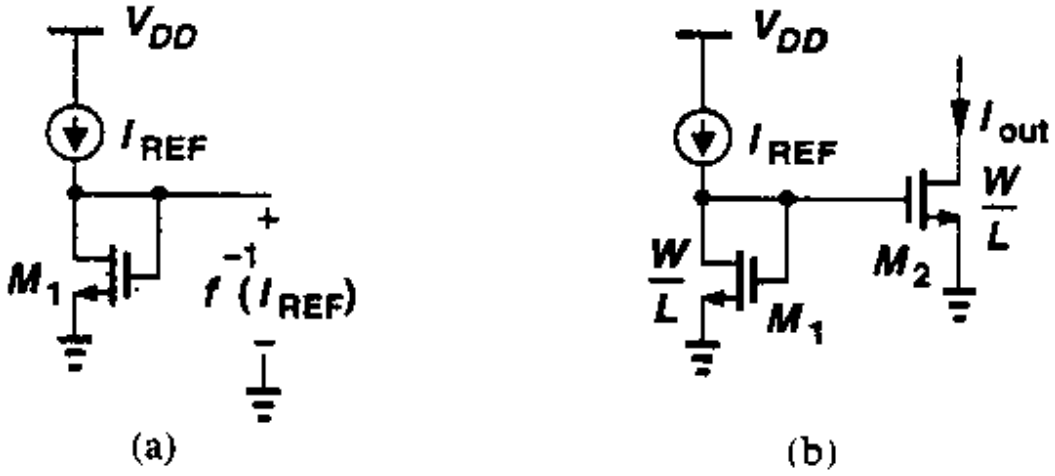

Figure 2.20 Conceptual means of copying currents (Razavi, 2000).

The structure including M_1 and M_2 as shown in figure 2.20.(b) is known as a "current mirror". In general, the devices need not be identical. Ignoring channel-length modulation that obtained:

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2 \tag{2.29}$$

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2 \tag{2.30}$$

Then obtained:

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF} \tag{2.31}$$

The major feature of this topology is that it allows accurate copying of the current with independency of process and temperature. The ratio of I_{out} and I_{REf} can be given by the ratio of device dimension; this is a quantity that is controllable with reasonable precision.

Figure 2.21 shows a simple current mirror in which it is assumed that both transistors operate in the active region. If the finite output impedance of the transistors were neglected and both transistor can be assumed with identical size, then Q_1 and Q_2 will have identical current since they both have identical gate–source voltage, V_{GS} .

Nevertheless, while finite output impedance is considered, the larger the drain-source voltage of each transistor is the larger current it will have. Moreover, the finite output impedance of transistors will result that the small–signal output impedance of the current mirror to be less than infinite; the small – signal impedance is the impedance looking in to the drain ofQ_2. The output impedance of the current mirror is needed to find, r_{out} , the small signal circuit was analyzed once , and a signal source is located, V_x , at the output node. Now by definition, r_{out} is calculated by ratio V_x/i_x where i_x denotes the current that flows out of the source and into the drain of Q_2.

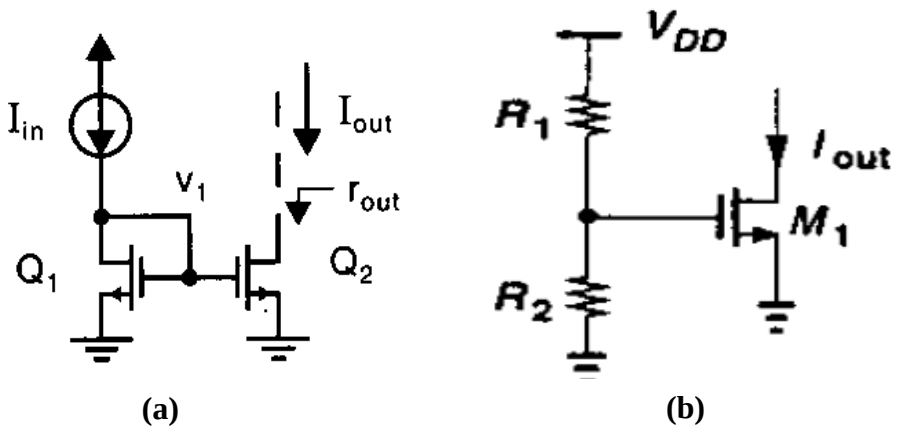

Figure 2.21 (a) Simple schematic of cascade current mirror , (b) Definition current by resistive divider (Razavi, 2000).

To obtain a better view, let's consider the simple resistive biasing shown in figure 2.21, assume that M_1 is in saturation region. The below results is obtained:(Figure 2.21 (b))

$$I_{out} \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\frac{R_2}{R_1+R_2}V_{DD} - V_{TH}\right)^2 \tag{2.32}$$

This equation represents various dependencies of I_{out} upon the supply voltage, process, and temperature. The overdrive voltage is a function of V_{DD} and V_{TH} ; the threshold voltage may vary by 100 mV from wafer to wafer. Furthermore, both μ_n and V_{TH} reveal temperature dependence. Hence, I_{out} is well defined.

2.4.2 Cascode Current Mirror

In previous discussion of current mirrors, channel length modulation can be neglected. In practice, this effect causes a significant error in copying currents, particularly if minimum length transistors are employed; so as to minimize the width and therefore the output capacitance of current source. For the simple mirror figure 2.22, that consist fowling equation :(Razavi, 2000)

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS1}) \tag{2.33}$$

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS2}) \tag{2.34}$$

And therefore: (Razavi, 2000)

$$\frac{I_{D1}}{I_{D2}} = \frac{(W/L)_2}{(W/L)_1} \cdot \frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}} \tag{2.35}$$

While $V_{DS1} = V_{GS1} = V_{GS2}$ may not equal V_{GS2} because of the circuitry fed by M_2.

In order to cancel the effect of channel–length modulation, a cascode current source can be employed. As shown in figure 2. 22(a), if V_b such that V_Y=V_x is chosen, then I_{out} tracks I_{REF} in close. This means that V_Y stays close to V_x and thus $I_{D2} \approx I_{D1}$ with high accuracy. Accuracy at the cost of the voltage headroom consumed by M_3 is obtained.

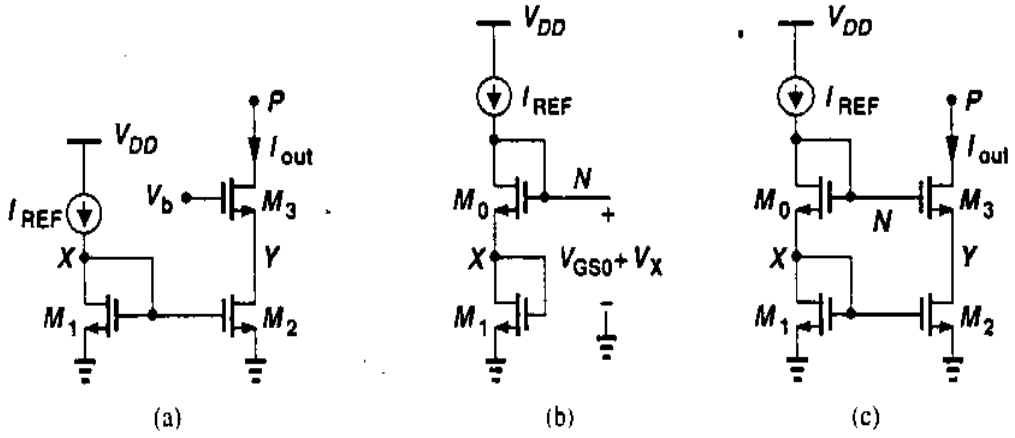

Figure 2.22 (a) cascade current source . (b) modification of mirror circuit to generate the cascade bias voltage. (c) cascade current mirror (Razavi, 2000).

Since the purpose is to guarantee $V_Y = V_x$, $V_b - V_{GS3} = V_x$ or $V_b = V_{GS3} + V_x$ should be guaranteed. This result proposes that if a gate-source voltage is added to V_x , the required value of V_b can be obtained. In figure 2.22(b), the idea is to locate another diode-connected device, M_0, in series with M_1. Thus, this cause generating a voltage $V_N = V_{GS0} + V_x$. Properly selecting the dimensions of M_0 with respect to dimensions of M_3 results in $V_{GS0} = V_{GS3}$. Once node N was connected to the gate of M_3 as shown in figure 2.22(c), $V_{GS0} + V_x = V_{GS3} V_Y$ was obtained. Hence, if $(W/L)_2 / (W/L)_1$, then $V_{GS3} = V_{GS0}$ and $V_x = V_Y$. Notice that this result is established even if M_0 *and* M_3 are influenced by body effect.

2.4.3 Advanced current mirror

2.4.3.1 Wide –swing current mirrors

Since more recent technologies with shorter channel length are employed, it becomes more difficult to obtain proper op-amps gain because of transistor output–impedance degradation which is result of short – channel effect. Consequently, designers have often no option unless to use cascade current mirrors. Unfortunately, the signal swings available is limited

by the use of conventional cascade current mirror; hence, this may not be tolerated in particular applications. Fortunately, there are circuits that do not limit the output signal swing as much as the current mirrors discussed in above. One of such circuits is shown in figure 2.23, so-called the "wide-swing cascade current mirror"(Minch, 2003)

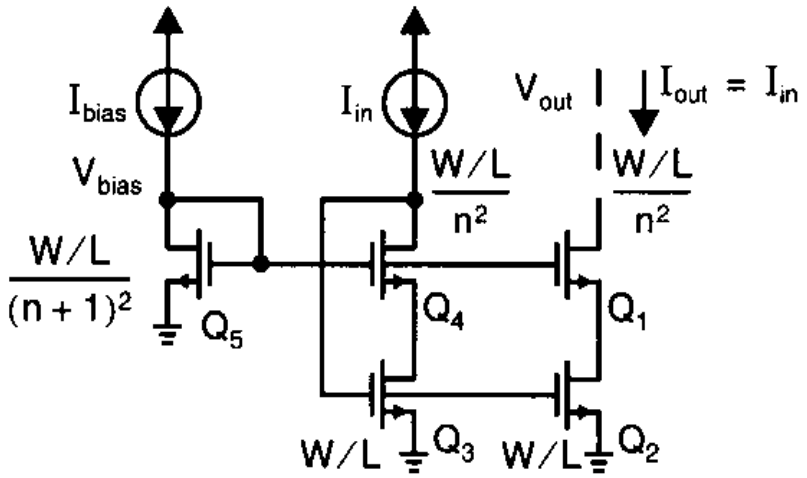

Figure 2.23 Simple schematic for wide –swing current mirror (Minch, 2003).

This current mirror is based on the idea that is to bias the drain-source voltages of transistors Q_2 and Q_3 to be near the minimum possible value without letting them go into the triode region. Specially, using the size shown in figure 2.24, and assuming the classical square-law equation are valid for long channel-length devices, transistors Q_2 and Q_3 are biased exactly at the edge of saturation region. Before describing how these bias voltages of transistors are selected, notice that the transistor pair Q_2, Q_3 plays a role of a single diode–connected transistor to create the gate – source voltage forQ_3 . These pair of transistors act very similarly to the status in which Q_3 would alone operate once its gate and source was connected together. The aim for presence of Q_4 is to decrease the drain–source voltage of Q_3 ; it causes that it becomes matched to the drain– source voltage of Q_2 . This makes the output current, I_{out} , match the input current, I_{in} , more precisely. If Q_4 were excluded, the

output current would be a little less than the input current; this usually happens because of the finite output impedances of Q_2 andQ_3. Beside this, Q_4 , has slight effect on the circuit operation.

2.4.3.2 Enhanced output-impedance current mirror

Another change on the cascade current mirror is often denoted as the enhanced output –impedance current mirror. Figure 2.24 shows a simplified form of this circuit. This circuit is employed to gain the output impedance. Using a feedback amplifier comes from the idea which aims to retain the drain–source voltage Q_2 as stable as possible, regardless of the output voltage. Adding this amplifier typically gain the output impedance by a factor equal to 1 + A where A denotes the loop gain over that which would happen for a traditional cascade current mirror.(Martin & Johns, 1997)

$$R_{out} \cong g_{m1} r_{ds1} r_{ds0} (1 + A) \tag{2.36}$$

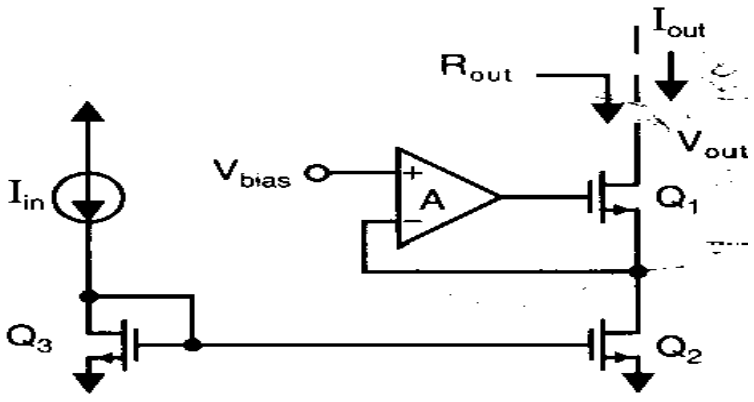

Figure 2.24 The enhanced output –impedance current mirror (Martin & Johns, 1997)

The enhanced output-impedance current mirror seems to have been first proposed in (Hosticka, 2002) for single-ended input amplifier and more lately discussed almost simultaneously in (Bult, et. al, 1990)and (Sackinger & Guggenbuhl, 2002)for differential input amplifier.

This current mirror was originally described in (Fiocchi & Gatti, 2002) , for use in current–mode continuous-time filter and was afterward used in the wide–signal-swing op amps design. It is very similar to the enhanced output–impedance current mirror of (Sackinger & Guggenbuhl, 2002), expect that diode–connected transistors employed as level shifter have been added in front of common–source enhancement amplifiers, which is shown in figure 2.25.

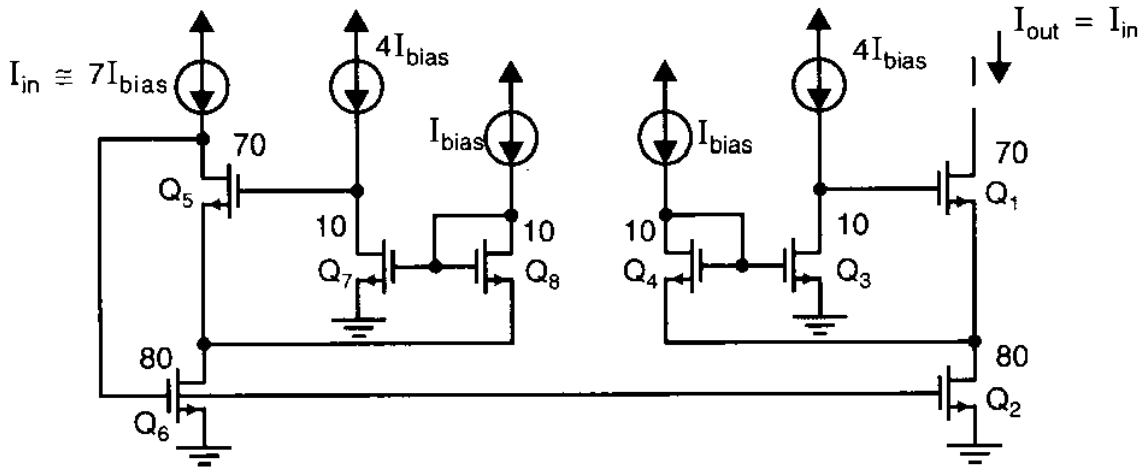

Figure 2.25 A wide –swing current mirror with enhanced output impedance . (Martin & Johns, 1997)

At the output side, the diode–connected transistor, Q_4 , acts as the level shifter which is biased with current I_{bias}. The circuitry at the input principally plays a role of an

output circuitry such that I_{out} exactly matches I_{in}. Each transistor represents a reasonable width in μm. Notice that for the following case: (Martin & Johns, 1997)

$$I_{bias} = {I_{in}}/{7} \tag{2.37}$$

All transistor are biased with approximately identical current density, excluding for Q_3 and Q_7.

Accordingly, all transistors content identical effective gate–source voltages,V_{eff}, excluding for $Q_3 \ and \ Q_7$, which have gate-source voltage equal to 2 V_{eff} ; since they are biased at four time the current density. Hence, obtain the gate voltage of Q_3 is obtained as follows: (Martin & Johns, 1997)

$$V_{G3} = 2V_{eff} + V_{tn} \tag{2.38}$$

And the drain-source voltage of Q_2 is given by : (Martin & Johns, 1997)

$$V_{DS2} = V_{S4} = V_{G3} - V_{GS4} = (2V_{eff} + V_{tn}) - (V_{eff} + V_{tn}) = V_{eff} \tag{2.39}$$

As a result, Q_2 is biased on the margin of the triode region; so, the minimum output voltage is obtained by: (Razavi, 2000) (Martin & Johns, 1997)

$$V_{out} > V_{DS2} + V_{eff} = 2V_{eff} \tag{2.40}$$

2.5 OPERATION AMPLIFIER

The current Integrated circuit design process hast three new challenges.

1) Portable equipment with a minimum volume and minimum number of batteries to reduce weight and easy transportation Transport.
2) Voltage limited resources of small size transistors is so significant these days.
3) Less power consumption to no longer require batteries and is leading this charge. High performance analog a circuit was designed according to the supply voltage reduction that is very significant.

At the time, operational amplifiers design is very important. Operational Amplifier or so-called Op–Amp is employed in a lot of analog and mixed–signal circuits such as voltage regulators, active filters and data converters, buffers, and the highly dependent (SC) discrete time circuits. For instance, the performance of switch capacitor circuits is a function of the one for operational amplifiers. Lots of recent mixed–signal circuits are data converters that convert analog signal to digital values and vice versa.

Totally, performance of these systems is highly dependent on circuit performance such as converter. The converters need data accuracy and speed for applications such as digital signal processing applications as well as general industry such as multimedia which is growing intensely. Lower power devices with lower supply voltage levels are considered as the major challenge of new technologies. This is a significant factor while designing. Operational amplifiers which act as the core of data converters are not exempt from this. However, high-power design and implementation of operational amplifiers with broad bandwidth are as well as interest in special applications. The minimum of the main goals is as interest.

In case of an operational amplifier design, the following characteristics should be defined before they are carefully designed and analyzed for Advantages:

- Small signal bandwidth.
- Large signal bandwidth.
- Output Swing
- Amplifier linearity.
- Noise and offset.
- Power Supply Rejection Ratio (PSRR).

Operation amplifiers (op-amps) are an integral part of many mixed –signal and analog system. Op-amps with different configurations are employed to realize various functions which are ranging from dc bias generation through high–speed amplification or filtering. The designs of op-amps are still posing a challenge since supply voltage and transistor channel lengths drops with each generation of CMOS technologies.

2.5.1 General Considerations

An op-amp usually is defined as a "high-gain differential amplifier". "high gain" play main role in high- gain differential amplifier ,the gain value is suitable for the application is usually in the range of 10^1 to10^5.Op-amps are usually used to apply a feedback system, their open-loop gain is chosen corresponding to the accuracy required of the closed–loop circuit.

In past two decades, most op-amps were designed to work as "general-purpose" building blocks such that they were satisfying the requirement of different sort of applications. Such efforts pursued to implement an "ideal" op-amp.

New days, op-amp designers release the trade-offs among the parameters that require a comprehensive compromise in the overall implementation, therefore it is for knowing the proper value that must be obtained for each parameter.

2.5.2 One-Stage Op-Amp

All the differential amplifiers can be considered as operational amplifiers. Two such topologies with single–ended and differential output are shown in figure 2.26 and 2.27, respectively. The small-signal low-frequency gain for both circuits is identical to $g_{m\,N}$ $(r_{ON} \parallel r_{OP})$, where the subscripts N and P represents NMOS and PMOS, respectively. Such value rarely goes above 20 in submicron devices with typical current levels. The bandwidth is usually determined by the load capacitance (C_L).

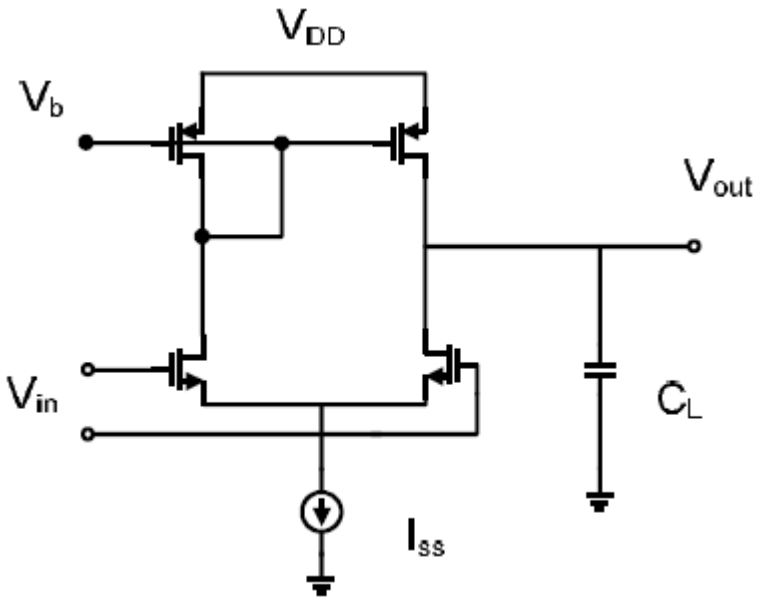

Figure 2.26 Single–Ended Amplifier.

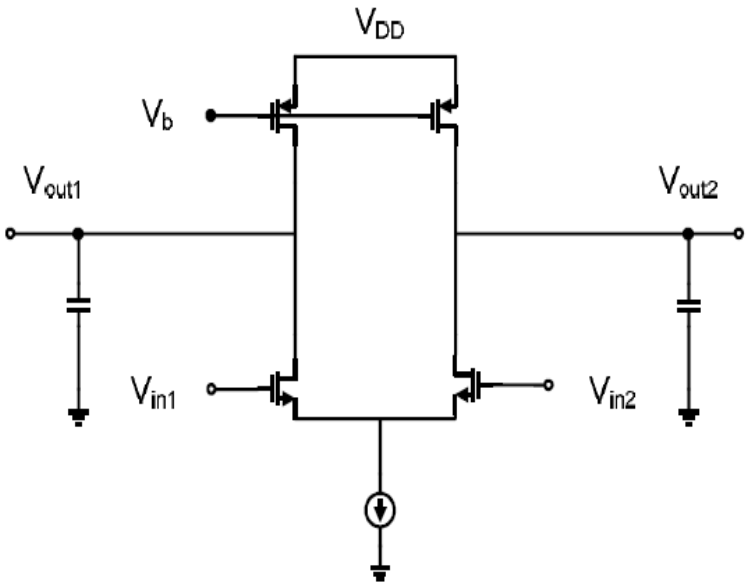

Figure 2.27 differential amplifier.

To increase the gain, cascading amplifiers can be used in cost of degrading output swing. To overcome this problem, folded transistors can be employed as an effective method figure 2.28.

Also, gain boosting is another method to improve gain for these amplifiers. In practice, gain boosting method is employed due to low gain in one-stage amplifiers and speed-problems in two-stage amplifiers. In one-single amplifiers, the major challenge is to maximize the output resistance such that can obtain the required gain. The idea on improving gain is based on increasing the output resistance without adding any further cascode stage figure 2.29 adding further cascode stages decreases output voltage swing .(Razavi, 2000)

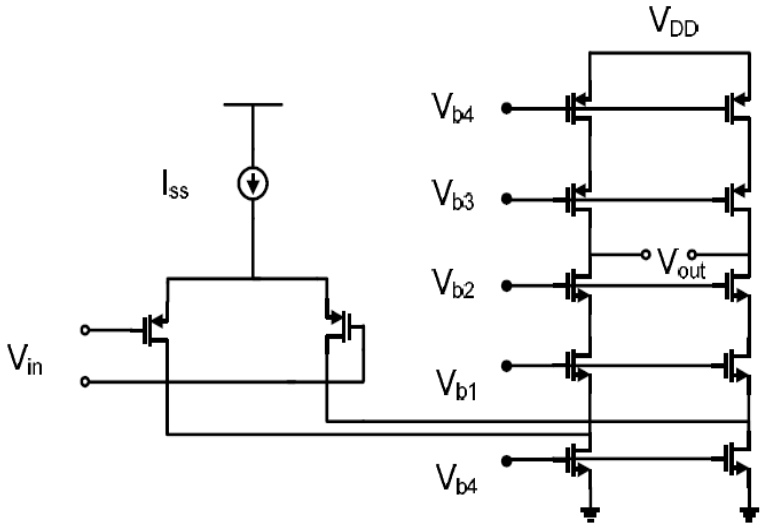

Figure 2.28 folded cascode Op Amp(Razavi, 2000).

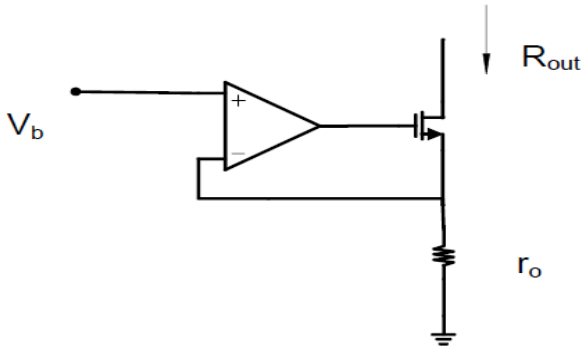

Figure 2.29 Improve methods for increasing the output resistance(Razavi, 2000).

2.5.3 Two–stage Operational Amplifiers

Two-stage amplifier configuration is a common structure for BJT-based designs and CMOS-based designs. In some applications, the achieved gain and swing by cascode amplifiers are not adequate. In these cases, one high-gain stage followed by one high-swing stage is employed figure 2.30. Each stage may have different topologies; but usually the

second stage is considered as a typical common-source amplifier in order to obtain maximum output swing.

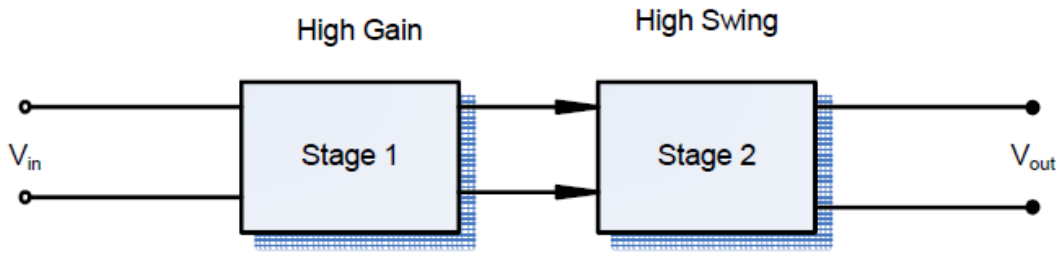

Figure 2.30 Two-stage structure Amplifier(Razavi, 2000).

A simple example for two-stage op-amp is shown in figure 2.31:

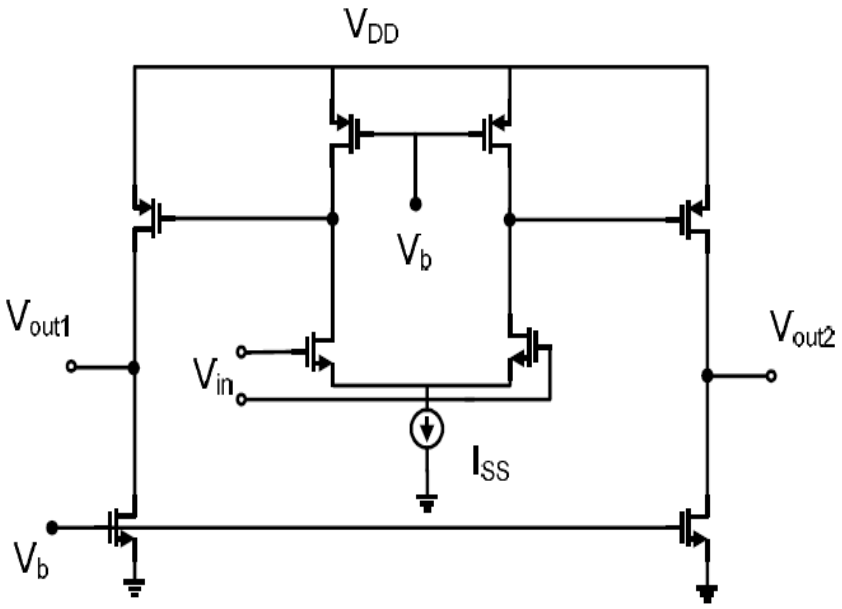

Figure 2.31 Simple two stage amplifier (Razavi, 2000).

Considering the different presented structures for operational amplifiers, a comparison between these structures is significant table 2.2.(Razavi, 2000)

Table 2.2 Comparison of methods for implementing the operational amplifiers (Razavi, 2000).

	Gain	Output Swing	Speed	Power Dissipation	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded Cascode	Medium	Medium	High	Medium	Medium
Two Stage	High	Highest	Low	Meduim	Low
Gain Boosted	High	Medium	Medium	High	Medium

According to the above discussion, the most common amplifiers nowadays, are two–stage amplifiers. This type of amplifiers has high swing up and acceptable gain. The most important issue of these amplifiers is compensation.

According the enormous application of two-stage operational amplifiers and the necessity of compensation (to guarantee its stability for closed-loop arrangement), different compensation methods are proposed. Considering the complexity of some of these methods, it is necessary to provide a systematic method to obtain the final transistors sizes for designing an operational amplifier.

2.5.4 Miller Compensation

Two-stage operational amplifiers are used for applications that high voltage gain and high swing are required. In such amplifiers, frequency compensation is important. Consider figure 2.32; X node pole is high frequency pole, but A and E node poles are closer to the origin. It can be said that this system has two dominant poles. Since A and E pole nodes are close together, the phase value for the frequencies under the third pole reach –180 degree. This means that the phase limit is almost zero. To overcome this problem, one of the poles

has to approach to the origin such that the phase limit for system rises to an acceptable value. Figure 2.33 shows a proper example of such case.

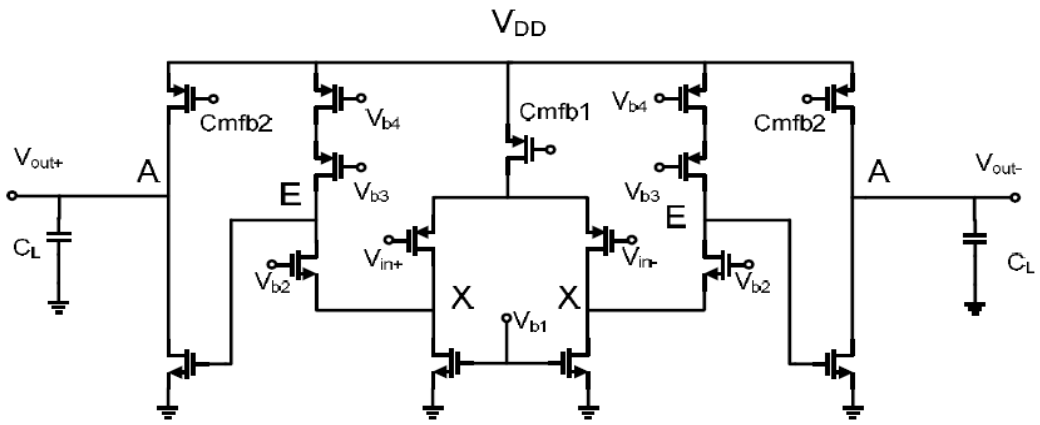

Figure 2.32 Operational amplifier without Miller compensation (Razavi, 2000).

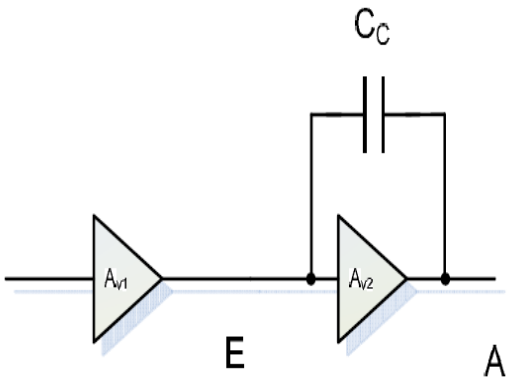

Figure 2.33 Operational amplifier without Miller compensation (Razavi, 2000).

In this example, first stage represents a high–output–impedance amplifier followed by a medium–gain amplifier that satisfies the conditions to apply Miller theory (Miller capacitance multiplication). This happens once a large capacitance equal to $(1+A_{v2})C_C$ is

created in node E such that transfer the desired pole to $R_{out}^{-1}(C_E + (1 + A_{v2})C_C)$ where C_E is the capacitance in node E before placing C_C).

At brief, a pole is approached to the origin by Miller compensation and second pole is taken far away from the origin; hence, adding a capacitor from node to ground results in better effect. In the analysis, the effect of generated zero in the transfer function is neglected in the analysis. In two–stage op-amps with Miller compensation there is a zero close to the origin on the right side. The right-sided zero acts similar to the left-sided pole such that it decreases the amount of system phase and takes the phase transit point closer to the origin. In the other hand, zero causes a decrease in gain drop speed. (Razavi, 2000) This causes that gain transition point is avoided from the origin; hence, this cause a decrease in stability.

The effects of right-handed zero in the two–stage amplifiers are very destructive. There are proposed methods to cancel out the harmful effects of this zero. One of these methods uses a resistance in series with compensation capacitor that moves the zero location figure 2.34.

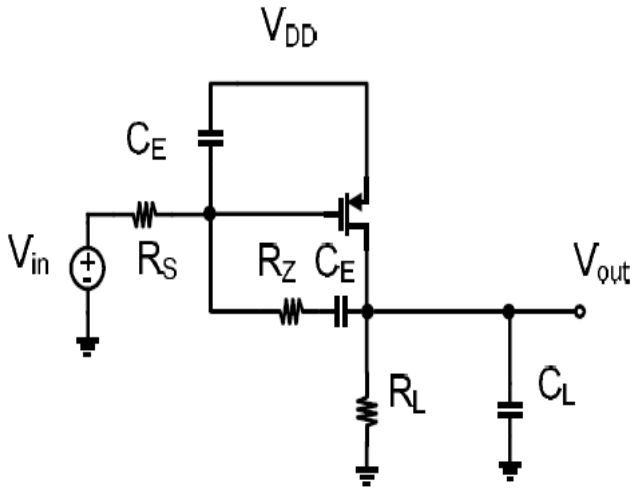

Figure 2.34 the use of series resistance for the transfer of a left zero (Razavi, 2000).

In the other hand, using this resistance can move the generated zero to the left. In the other hand, the left-sided zero can be used to remove a pole. Implementing this resistor in integrated circuits produces new problems that there are proposed solutions in.

The major disadvantage of Miller Compensation is the generated direct path between input and output. If it was possible that there was a path from output capacitor to input one, but not the vice versa, the generated zero would move to very high frequencies.(Razavi, 2000)

2.5.5 Compensation cascade

Miller Compensation seems to be a suitable method for compensating two-stage amplifiers. Beside all its advantages, there are two major disadvantages which are as follows:

- Low supply variations cancelation rate.
- Presence of right-sided Zero which acts similar to a pole and impact the characteristics of amplifier.

Right-sided zero is generated due to the direct path between input and output caused by the compensation capacitor. If it was possible for signal to pass from the output and not to pass the reverse path (the input to the output), the right-sided zero would move to the high frequencies. One of the ways to solve this problem is to use a common-drain amplifier in series with the compensation capacitor. Since gate–source capacitance in transistor is too low in compare with compensation capacitance, the right–handed zero is expected to occur in high frequencies. The simplified equivalent circuit is as figure 2.35.

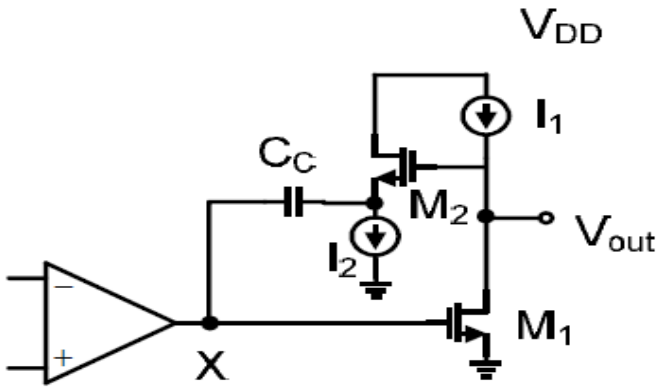

Figure 2.35 Use buffered voltage to eliminate zero(Razavi, 2000).

The right-sided zero has been moved to the left such that can be employed to remove a pole. The values of the first and second pole are identical to the calculated poles in Miller compensation. One of disadvantages for these methods is that the lowest output voltage is limited to $V_{GS2} + V_{I2}$ where V_{I2} is the required voltage of the current source to continue operation in linear region. In order to solve this issue, compensation capacitors are used to for input and output dc–voltage isolation. This structure is shown in figure 2.36.

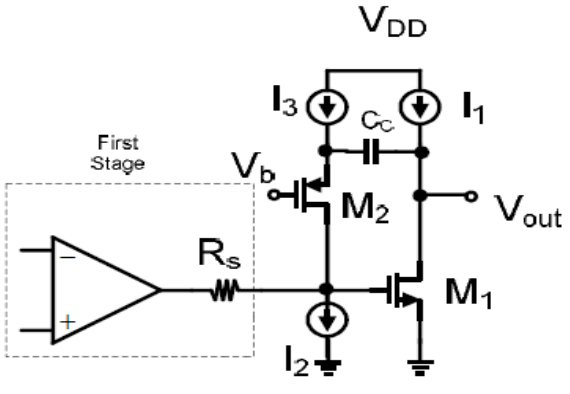

Figure 2.36 use buffered stream to kill the right of zero (Razavi, 2000).

In the figure 2.36, the variations in output voltage is converted to current by capacitor C_C and common–gate transistor (M2), and transferred to the gate of M1.

Assuming that V1 changes equal to ΔV, then the Vout changes equal to $A_v \Delta V$, such that causes a flowing current equal to $A_v.\Delta V.C_C.s$ in capacitor. Therefore, assuming $1/g_{m2}$ is small enough, the capacitance product is equal to A_v.

The circuit has a right-sided zero. It can be observed that the second pole has become $g_{m2}R_S$ larger relative to the initial status. This is because of considering the compensation capacitor as short circuit due to high frequencies; the output resistance is degraded by the R_S and M_2 loop to the same value.

All discussions above were, in fact, a new method for compensation. (Razavi, 2000) The idea comes from Miller compensation (capacitive multiplication) that is used to create one pole closer to and one father from the origin relative to the initial status. In addition to degrading the effect of right-sided zero in Miller Compensation, This method gives a better power supply rejection ratio (PSRR) than the Miller compensation.

2.5.6 Complex Cascode Compensation

Miller Compensation has a pole break affect such that moves a pole to higher frequencies and other one to lower frequencies. This creates a dominant pole. The major disadvantage of this method is the lower speed and lower PSRR compared to Cascode method. In the Miller compensation, a compensation resistance in series with compensation capacitance is also required to transfer the right–sided zero to the left. The value of such resistance varies intensively with temperature and fabrication process; this directly effects on the system frequency response, causes the system frequency response be affected. This resistance is usually implemented using a transistor which is biased in linear; however, the design itself can be a major problem since the circuit supply voltage is low.

Cascode compensation partially solves the above problems. In this method, a transistor is placed between a node with low impedance at input and output of second stage. This results in a higher speed and higher PSRR.

Complex cascode compensation is a new method. In this method, two separated capacitors are placed between low–impedance nodes of the first stage and output node. In fact, two methods of cascode compensation and enhanced cascode compensation are combined. This cause a wider bandwidth compared to conventional Miller and cascode methods. However, this is achieved in the cost of more complexity in process.

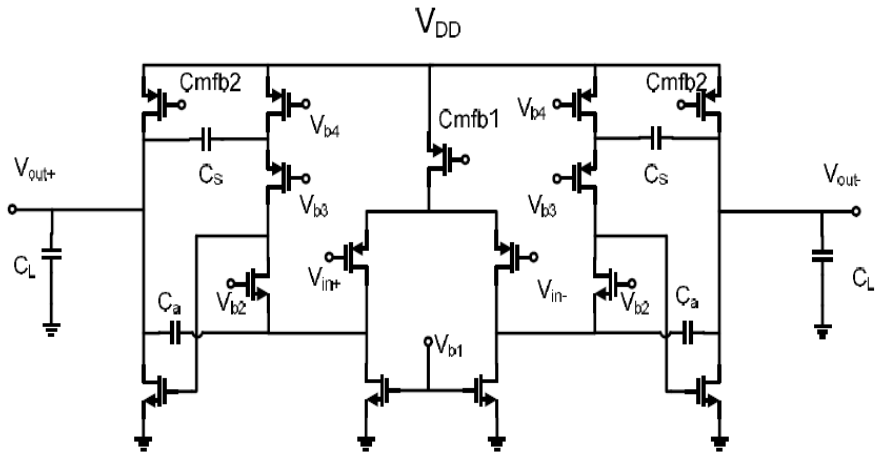

Figure 2.37 Compensation Amplifier with Mixed cascade (Razavi, 2000).

Figure 2.37 shows a two-stage operational amplifier. The first stage is folded-cascode and second stage is a simple common–source amplifier. These kinds of amplifiers are used in capacitive switch circuits. Note that the proposed topology has been chosen only for simplicity and the compensation method is applicable to any other two-stage operational amplifiers with different configurations. As shown in figure, two distinct

capacitors C_a and C_s are used for compensation, such that C_a is placed at signal transition path and C_s is placed at signal stop-path.

System has two zero on the left and one on the right. Since right–handed zero is a high frequency, so it does not impress the system performance. The dominant pole of such compensation is as common as the dominant pole in Miller and cascode compensation methods.Sum of two capacitors instead of one capacitor present at Miller and cascode compensation is only difference.

Cascode compensation method has same advantages more than other methods which are summarized as follows:

1) This method includes one more of zero and pole while by choosing $C_a = C_s$ and $g_{m2} = g_{m3}$, the second pole is canceled with the first zero. This cause that system degrades to the third nominal.
2) Size of non-dominant poles and zeros increase 1.4 times that causes an increase in bandwidth while the phase limit is constant.
3) The first Zero in complex cascode compensation is almost double the zero in enhanced cascode compensation. While $C_a = C_s$ and $g_{m2} = g_{m3}$, Zeros in complex cascode compensation are much larger; because the first zero is canceled with the second pole.(Yavari, et.al, 2006)

CHAPTER III: DESIGN AND METHODOLOGY

3.1 INTRODUCTION

As mentioned in previous chapter, two-tiered assessment probe and interview are used in capacitive sensor interfacing circuits that are applied in many MEMS-based wireless and biomedical applications. In this chapter, the circuit's configurations structures and any details required to design a capacitive sensor interfacing circuit are described. It is clear that the interfacing circuits can be used in RF MEMS switches.

Three main building blocks of this circuit will be described in this part, also each block will be compared with other topologies in the same area; for instance, there are many topologies for current mirror and certainly, each one has some advantages and disadvantages. In this study, the most suitable topology of our purpose is chosen.

First of all, an overview of the whole circuit will be presented, and then a detailed description about each block of the circuit will be discussed. All designs are in 0.18μm CMOS technology and simulations are performed using Mentor Graphic Eldo software.

Figure 3.1 shows the flow chart of design process and all the related works for this study.

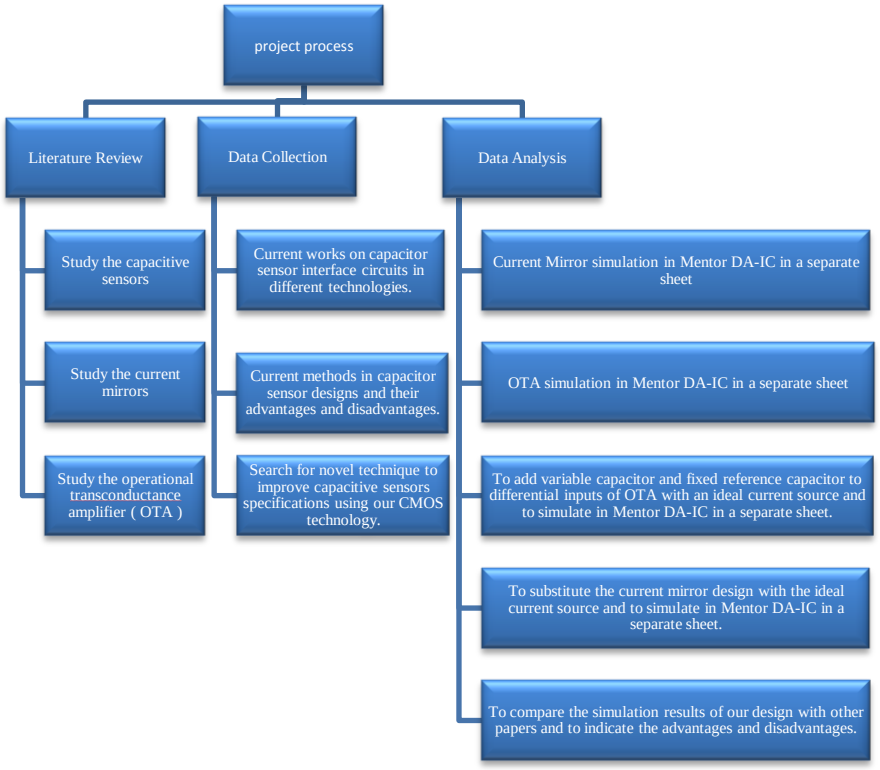

Figure 3.1 Flow Chart of project process.

3.2 CAPACITIVE SENSOR INTERFACE CIRCUIT

Figure 3.2 shows an overview for capacitive sensor interfacing circuit topology that is used in this project. Some of the advantages for this circuit in compare with other topologies led us to choose this topology and will be described later.

By noting to the figure 3.2; the RF MEMS switch with different position of switch changes the distance of two plates. The interfacing circuit senses the distance variations as a variation in capacitance; hence, the MEMS capacitance acts as a varying capacitance which is in parallel with a fabricated fixed-in-value capacitor. Using two capacitors, one fixed and one varying, which both have an identical nominal value C, provides the symmetry for these complementary capacitors.

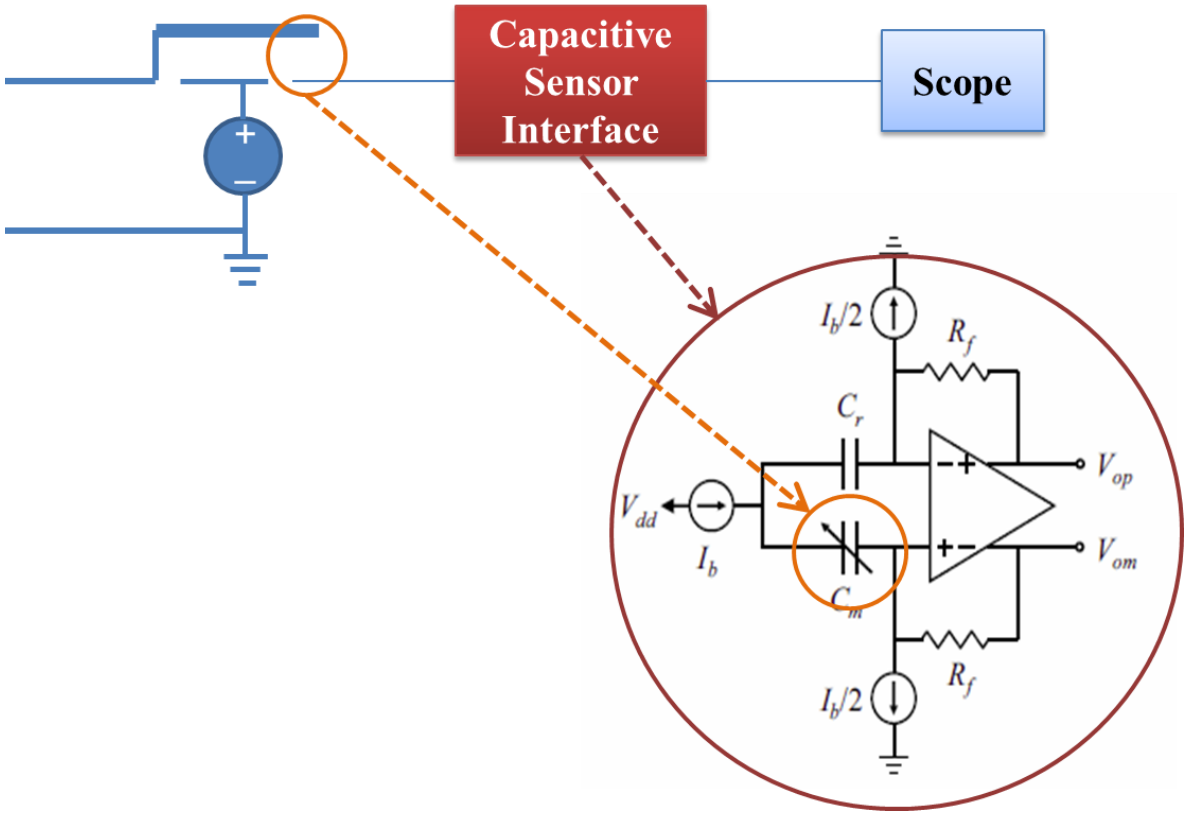

Figure 3.2 The overview of application circuit and main block of circuit .

Using the capacitance as a sensing parameter, any change in the measured physical parameters of the sensing capacitor can be recognized in differential mode such that a positive or a negative change in the varying capacitance relative to the fixed capacitance result a positive or negative output voltage, respectively. Such capacitance detection circuit proposes the usage of advantages of differential design. But, in many sensor systems, such a sensor with opposite capacitance might not be available.

In this case, this method proposes using a single measuring capacitance which changes identical to the variation in the sensing parameter. The sensed signal will be compared with a reference capacitance, which is typically equal to nominal value of the

sensing capacitance. Such system are mainly established on comparison methods (Amendola, Lu, & Babadjian, 2001), (Iordanov, Meijer, & Nihtianov, 2002)

C_m and C_r denotes the sensing and reference capacitors respectively . One of the advantages of the proposed circuit is that while maintaining the main topology, the signal current is measured differentially; this creates a differential output voltage. The other advantage is that the voltage at bottom plate of the sensing capacitance and the reference capacitance is kept at the common–mode voltage by the feedback loop.

Beside these two capacitors, there are two other blocks in this topology. One of them is current source which feeds the capacitors and the other one is an operational amplifier which boosts the measurement signal.

Types of current mirror were described in detail in chapter two. Two sorts of these structures were chosen to design a current mirror; both of them are a type of wide swing current mirror with enhanced impedance. In addition, operational amplifier that was also explained previously will be a two–stage op–amp to provide a high gain.

The calculations of parameters which are required for design and simulations for each block will be shown in this chapter.

3.3 WIDE–SWING CURRENT MIRROR WITH HIGH IMPEDANCE

There are several topologies for designing a current mirror which are compared with each other in table 3.1; it can be seen that wide–swing current mirror represents an excellent accuracy with high output swing. Structure with high output impedance is the purposed design; so it is more convenient.

Table 3.1 Comparison of main type of current mirror

Current Mirror	Accuracy	Output Resistance	Input Resistance	Minimum Output voltage	Minimum Input Voltage
Simple	Poor	r_{ds}	$1/g_m$	V_{ON}	$V_T + V_{ON}$
Cascode	Excellent	$g_m r_{ds}^2$	$2/g_m$	$V_T + 2 V_{ON}$	$2(V_T + V_{ON})$
Wide output swing cascode	Excellent	$g_m r_{ds}^2$	$1/g_m$	$2 V_{ON}$	$V_T + V_{ON}$
Self-biased cascode	Excellent	$g_m r_{ds}^2$	$R + 1/g_m$	$2 V_{ON}$	$V_T + 2 V_{ON}$

Figure 2.25 shows the topology of our proposed current mirror. For this project, due to the input in the capacitive interface sensor circuit and direction of capacitors, in our proposed interface, the current mirror needs to source the current rather than sink the current; hence, the NMOS transistor configuration is replaced by the PMOS transistor one. This causes the output current direction to change in opposite direction.(Razavi, 2000)

3.3.1 Design Methodology of Current Mirror

In this section, the W and L will be calculated for each transistor from the size ratios that is mentioned in the main topology. All transistors are operating in saturation region as Vgs-Vt for all transistors are equal to Veff (close to the edge of triode region) excluding Q3 and Q7 which have a Vgs-Vt equal to 2Veff(Martin & Johns, 1997); hence, the required gate-source voltage relative to threshold voltage is estimated such that guarantees transistor to work in saturation region. In addition, the required drain current I_D of each transistor is estimated and then the transistors' W/L ratio can calculated by parameters that obtained from I_D. By assuming a value for L, W is determined. It is obvious that L cannot be less than the minimum length of process.(Martin & Johns, 1997)

3.3.1.1 Current Drain (I_D) Relation for MOSFETs

In the mentioned current mirror circuit, all transistors must be on saturation region; so, the following equation is used for I_D to obtain unknown parameters :(Martin & Johns, 1997)

$$I_D = \frac{\mu_n \, Co_x}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{th})^2 \tag{3.1}$$

3.3.1.2 Determining Bias Voltages and Currents, V_{GS} and I_D

As mentioned in chapter 2, all transistors content identical effective gate–source voltages,V_{eff}, excluding for $Q_3 \ and \ Q_7$, which have gate-source voltage equal to 2 V_{eff} ; since they are biased at four time the current density (Martin & Johns, 1997).

Hence, Q3 and Q7 are in the saturation mode far from triode region. All other transistors are close to the edge of triode region, but still in the saturation region. If V_{eff} is more than 100mV, it would be normally in a safe value for strong inversion operation, but in the cost of higher current mismatch. It seems that a value of 50mV for V_{eff} would be a proper value that avoid from strong inversion and high current mismatch. So:

$$V_{DS} > V_{GS} - V_{TH} \tag{3.2}$$

If transistors are in saturation region, then their current I_D will be almost constant.

In the above equation, there are some known parameters that their value is determined by the specific CMOS technology. Some of these parameters are given in table 3.2.

Table 3.2 Main value of transistor that has been used in this circuit

Parameter	L_{eff}	t_{ox}	V_{sat}	V_T	C_{ox}
Units	µm	nm	m/s	V	fF/µm
Value	0.18	3.65	113700	0.415	9.4604

Table 3.3 Value of power supply in current mirror circuit

V1 (V)	V3 (V)	VDD(V)
0.9	0.57	1.8

3.3.1.3 Determining Size of the Device

After finding the values of W and L for each transistor, the transistor was placed in the current source circuit; the I_D equation (3.1) should be calculated for new transistor again and then replace the current source by transistors.

Table 3.4 Shows the final design of our current mirror.

# / size	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12	M13
L μm	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.36	1.8	1.8
W μm	14.4	12.6	1.8	10	18	1.8	12.6	14.4	0.36	0.9	0.36	1.8	1.8

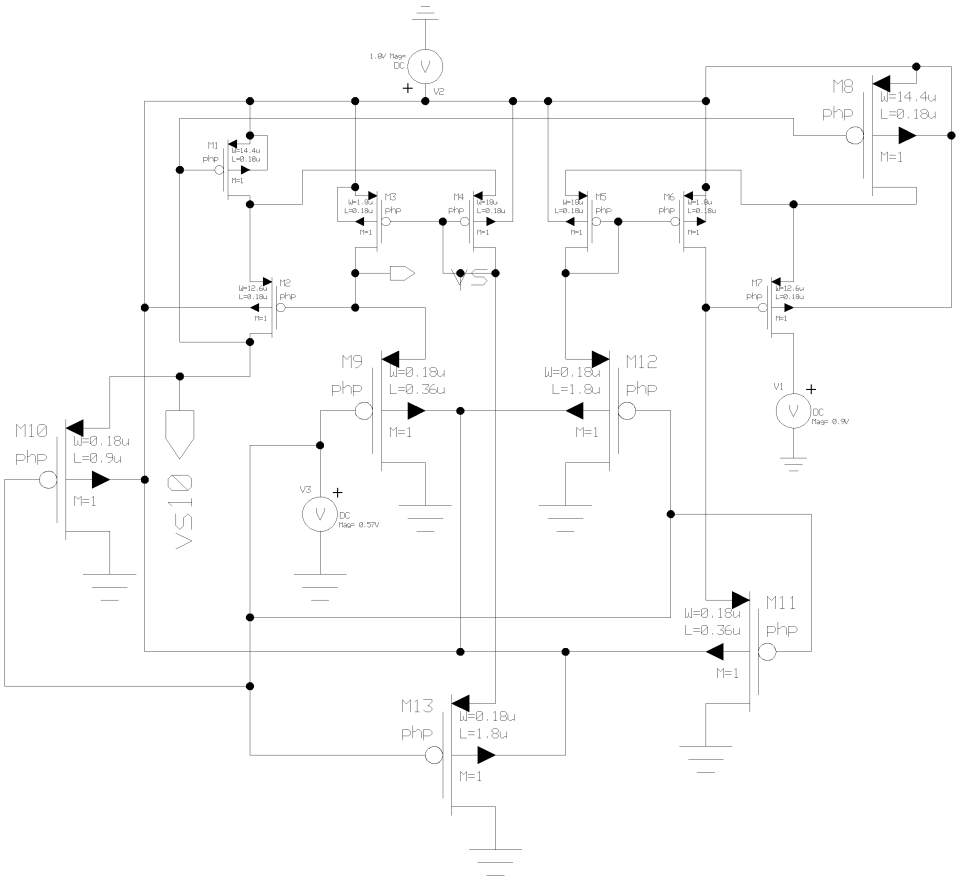

Figure 3.3 The main current mirror designed

This circuit is designed to provide a 1 µA current at the output. It is not important to fix the charging current to a specific value as long as it is stable over time because the system can be easily calibrated; however it should be noted that reset time is set appropriately for not allowing the current–mirror transistors to go into the linear region.

3.4 TWO STAGE OPERATION TRANSCONDUCTANCE (OTA)

The two–stage operation transconductance amplifier (OTA) is shown in figure 2.31 that extensively employed in analog and mixed signal circuits. Certainly, a very simple and robust topology is identified by values for most of its electrical parameters such as DC gain, output swing, linearity, CMRR and so on. Frequency compensation is necessary in op–amp

design to avoid closed-loop instability. For a two–stage CMOS op–amp, one of simplest compensation techniques is to attach a capacitor across the high–gain stage.

3.4.1 Design Methodology of OTA

The basic topology that OTA design was based on figure 3.4. After determining the values of parameters for this topology, the circuit was optimized and then the second stage was added to this circuit in order to boost the gain.

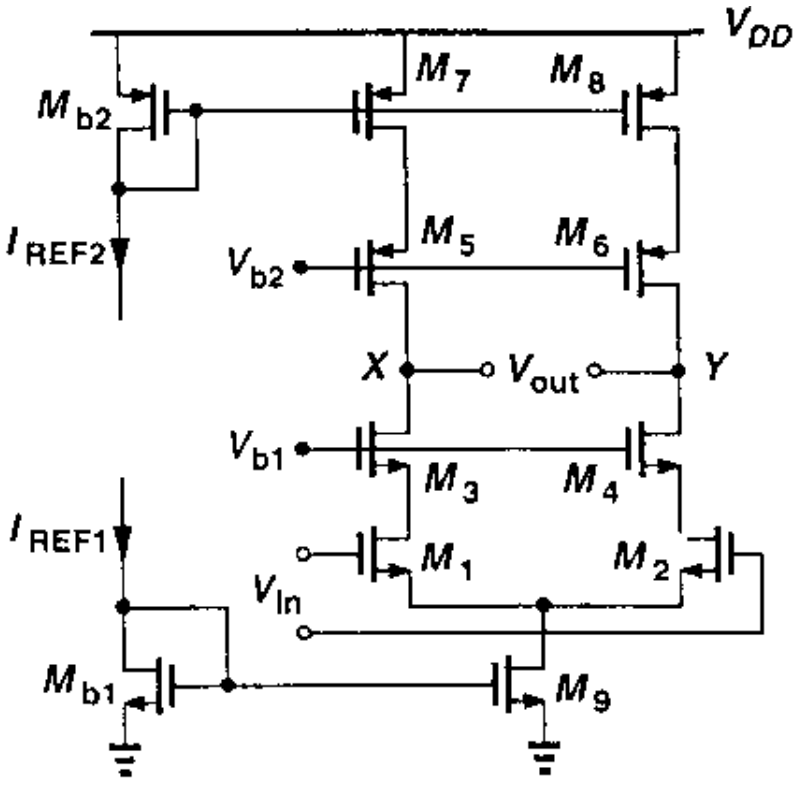

Figure 3.4 Basic topology of OTA circuit (Razavi, 2000).

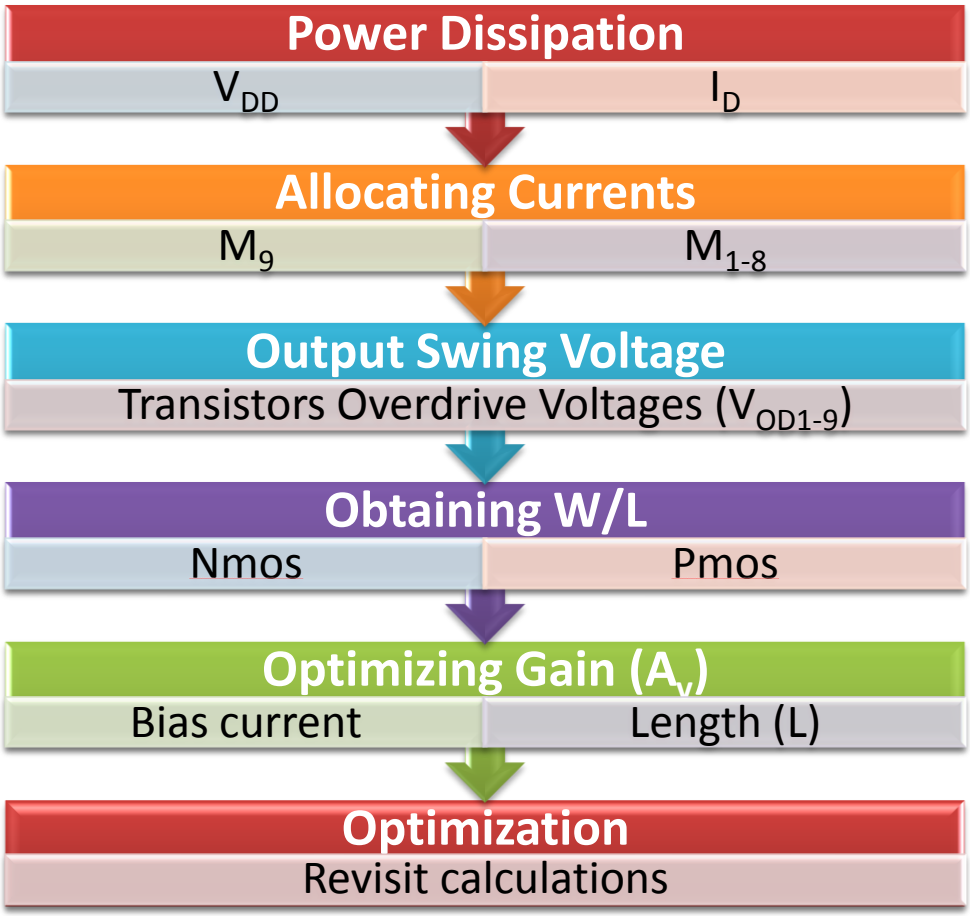

Figure 3.5 OTA design methodology

In figure 3.5 the op-amp topology along with two current mirrors defining the drain current of M_7 -M_9 are shown. Power for step one is used for calculating the unknown value, in hence one value as a current of M_9 is considered; certainly each cascade branch's part has half of main current.

The second step is considered as the required output swing ,for example each node X and Y must be able to swing by 1.5 V without driving M_3 - M_6 in to the triode region with 3 V supply , therefore the total voltage available for M_9 and each cascade branch is equal to 1.5 V.

Seeing as M_9 carries the largest current value of course, and V_{OD} ≈0.5 V should be allocated. Leaving 1 V for transistors in the cascade .Moreover, since M_5 -M_8 suffer from low mobility , an overdrive of around 300 mV was chosen for obtaining 400 mV from equation of $V_{OD1} - v_{OD3}$ .As an initial guess $V_{OD1} = v_{OD3}$ =200mV.

When the bias current and overdrive voltage of each transistor known then the aspect ratio by this formula can be easily determined: $I_D = \frac{\mu_n Co_x}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{th})^2$. to minimize the device capacitances ,$(W/L) = 1250(W/L) = 1111.(W/L)_9 = 400$.

The value of W and L can be found for each transistor by applying this procedure. After these steps, the value of A_v (gain) is found. (Razavi, 2000)

3.5 DESIGN OPTIMIZATION APPROACH

Different solution can be applied in compensation for achieving optimizing. The basic circuit in figure 3.5 different solution can be applied for compensation, some of these compensations are used for this project and be will described below (Razavi, 2000):

- Change the value of W and L
- Making the stage by adding the transistors
- Add resistors for output compensation

In first step after designing and calculating the basic topology that has been described, the gain was measured that gain is equal to ratio of output voltage on input voltage, so in first step our gain was very low.

The first technique that changes the value of W and L is used as shown in figure 3.5, NMOS and PMOS are presented in figure 3.5.

Note that the size of NMOS transistors has major effect on improving gain. However increasing the size of NMOS transistors may take the transistors status from the saturation region to triadic region (or ohmic region in this region transistor work as a resistor) which is not acceptable .In order to compensate for this unwanted event, size of PMOS transistors should be reduced; hence, the overdriving voltages between all NMOS and PMOS transistors could be split such that all transistors operate in saturation region. (Razavi, 2000)

In the second step, more transistors were added to make stages (Razavi, 2000); also the result of output was compared to first step that it is nearly two times bigger than first step.

That was the main solution for obtaining more gain in output that could be added four NMOS transistor and also after adding those transistor, the value of the W and L should be changed like previous step until the best result is gained.

The resistors in source of new transistors could be added to find high gain (Razavi, 2000). As shown in figure 4.6, the resistor was added to M13 and M12 sources. From the principle of transistor by adding the resistor that causes limiting the emitter current, thus bigger current were obtained in collector and also better result was gained in output. These are most of the solutions that have been done in this project to optimize the OTA (Razavi, 2000).

CHAPTER IV: SIMULATION RESULT, ANALYSES AND DISCUSSION

4.1 INTRODUCTION

In this chapter, the final design for each block of the circuit and also their simulation results will be presented; then, the results of optimized blocks will be compared with those before optimizations.

As discussed in previous chapter, each part of main circuit was explained. Here two main blocks is optimized, one of which is the current mirror and the other one is OTA (operation transconductance amplifier).

4.2 SIMULATION RESULT

4.2.1 Final Design for Current Mirror

As explained in chapter 3, a topology for current mirror was selected, a design that gives more benefits to reach the main aim. This topology is called as “wide-swing current mirror with high impedance”. In this circuit, output current was set equal to 1 µA; so, the values of W and L of each transistor are changed since the proposed value is obtained for output current. At the first, from the calculation by the equations which was explained in chapter three, output current was found more than 1µA; the output was near to 3µA so the values of W and L were optimized until the suitable value was obtained.

In table 4.1, the final values for size of transistors in the current mirror design is given to achieve a 1µA output current. Also in figure 4.1 you can see the output current in simulation result.

Table 4.1 Final value for all transistors in current mirror.

	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	M_9	M_{10}	M_{11}	M_{12}	M_{13}
W	14.4	12.60	1.8	10	18	1.8	12.6	14.4	0.18	0.18	0.18	0.18	0.18
L	0.18	0.18	0.18	0.38	0.18	0.18	0.18	0.18	0.36	0.9	0.36	1.8	1.8
V_{TH}	0.376	0.376	0.376	0.376	0.376	0.376	0.376	0.376	0.376	0.376	0.376	0.376	0.376
tech	0.18-um CMOS												

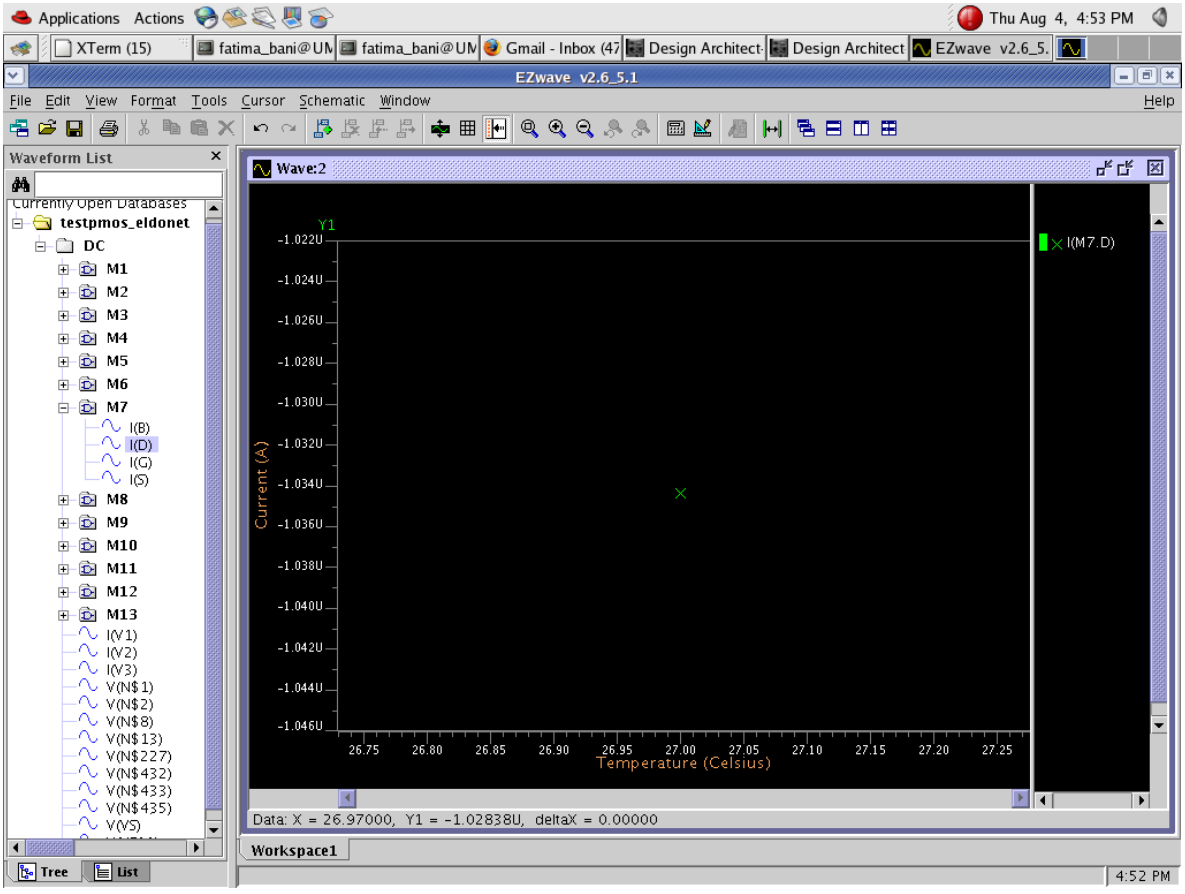

Figure 4.1 Output for wide-swing current mirror with high impedance

.

4.2.2 Final Design for OTA (operation transconductance amplifier)

In this section, there are several results achieved, because there is one main topology for this circuit which is optimized in three steps. Here, the result of each step will be shown so the amount of effect for each step will be realized in results.

Initial design with no optimization is given in Fig 3.4,the principle of our design is based on this configuration; this is the basic circuit that was designed from main topology by calculation of the values for each transistor biasing voltage and sizes as explained in chapter three.

In figure 4.2, the output of OTA was presented for the first optimization step. It can be seen that at this level, the amplifier has only around 40dB gain which is so far from our target.

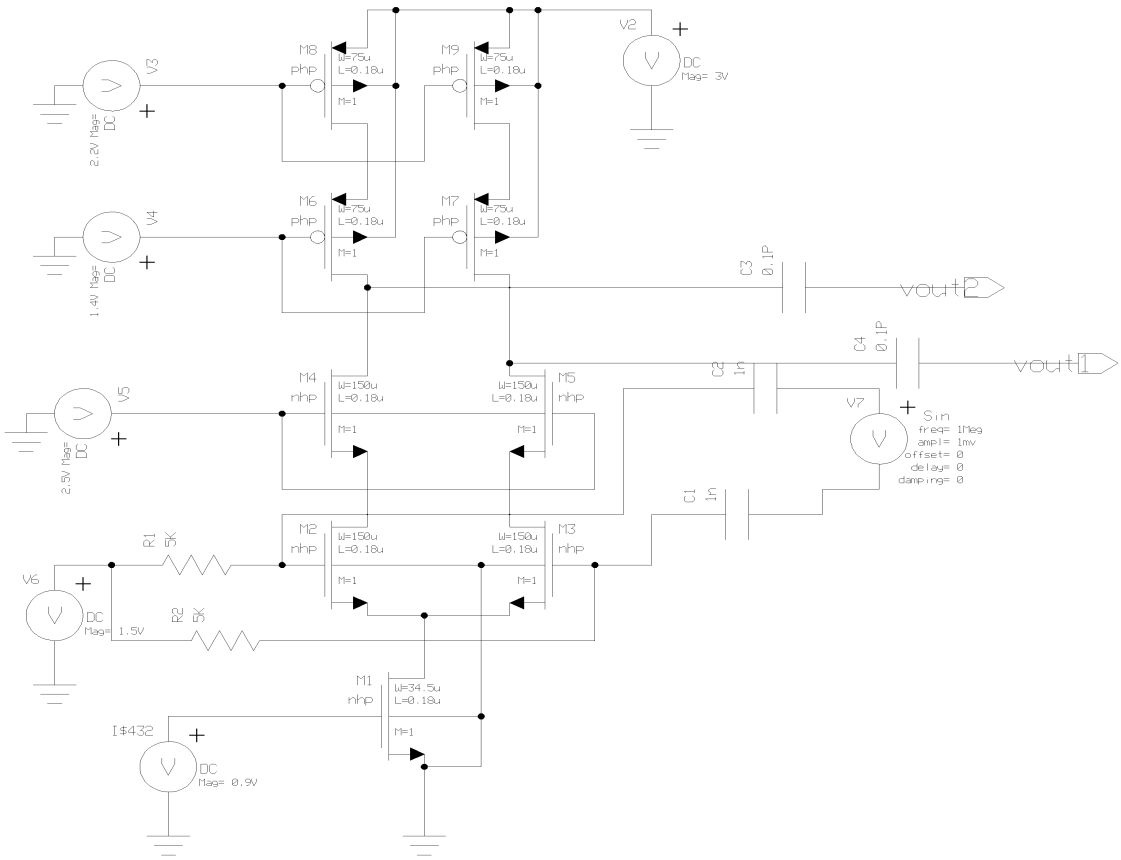

Figure 4.2 Schematic of OTA with 40 dB gain.

At the first step of optimization, by changing values of W and L, the OTA gain is improved as shown in figure 4.2; both circuits are achieved in the first step optimization.

After this step, another stage was added to our main circuit; the gain was shown also become well. Again, by changing W and L, much better result for gain would be obtained.

After this step, another stage was added to our main circuit that is shown in figure 4.3; the gain was improved more. Again, by optimizing W and L, better results for gain would be obtained.

There is an important point which was also mentioned in chapter 3. The point is that any change in the values of W and L for NMOS and PMOS transistors must be applied oppositely; so the value of W and L was changed in opposite way, which means any increase in size of NMOS transistors are followed by a decrease in size of PMOS transistors.

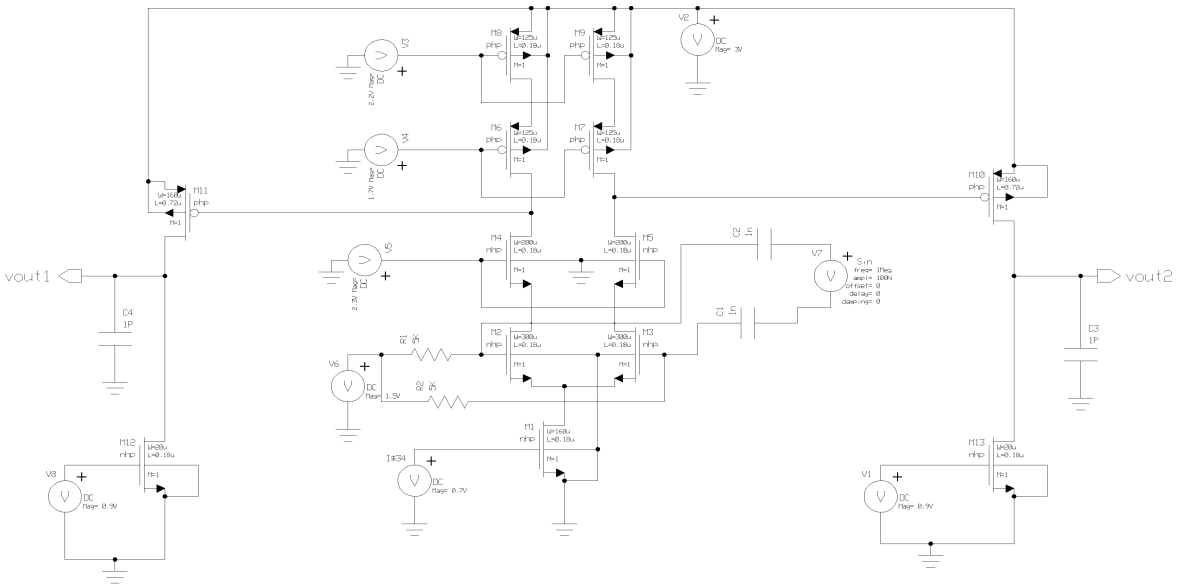

Figure 4.3 OTA Schematic after second step of optimization, 78dB.

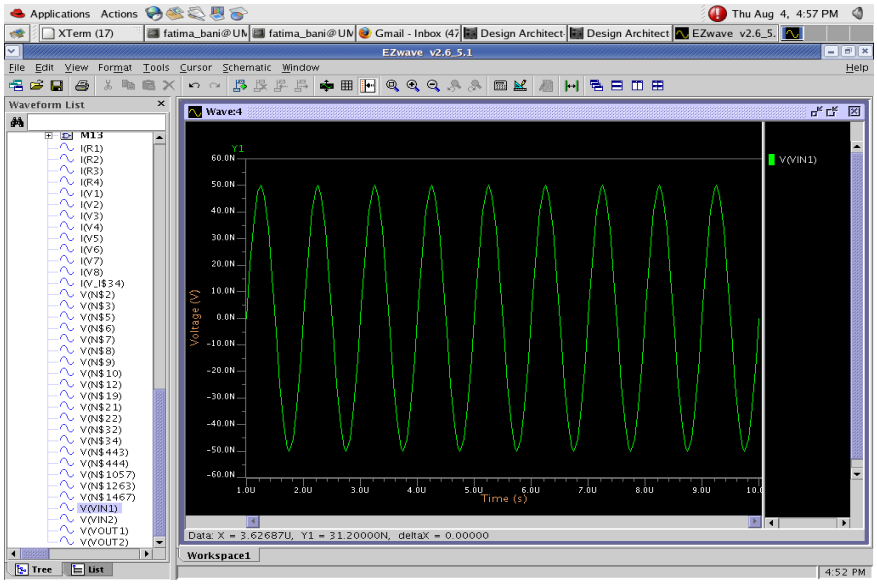

Figure 4.4 Input of signal that amplified by op-amp .

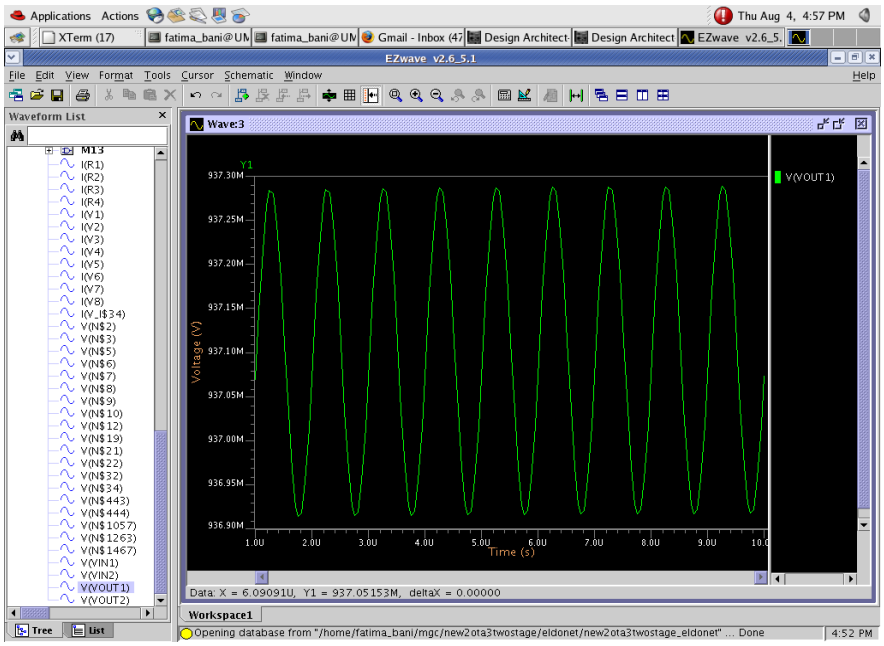

Figure 4.5 Final output for optimization op-amp.

The proposed OTA has 78 dB gain and in compare with Li Tianwang et .al with 59 dB gain in 0.18-um CMOS technology, it is much high (Tianwang,et.al, 2009). Also, our

proposed OTA has a gain identical to Rida Assaad et .al in 0.5-um CMOS technology, but 2.7-mW lower power dissipation (Assaad & Silva-Martinez, 2009). In comparison, a 1-volt 2.1-mW 70-dB OTA in 90-nm CMOS technology, our proposed 89-dB OTA has a higher power consumption equal to 9.9 mW (Mirhosseini & Ayatollahi, 2010).

4.2.3 Circuit Realization

After each block was designed individually, the blocks should be connected together to realize main target circuit which was described in chapter three, figure 3.2. Details of this circuit are shown in figure4.6.

In order to realize the differential TIA, a fully differential OTA with feedback resistors $Rf_1 = Rf_2$ (with a nominal value *Rf*) is used. To drive the signals off chip, circuitry must be included to the circuit of the prototype which is shown as dotted portion. Therefore, the output voltage *V*out_*b* will be measured experimentally as the output of the prototype. In this project, no prototype is implemented; so, the dotted portion is excluded.

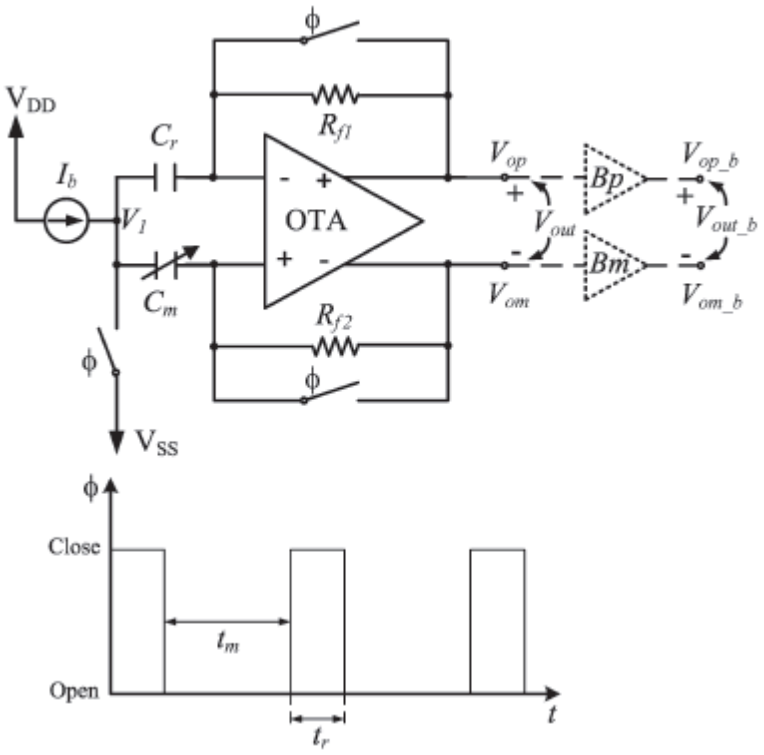

Figure 4.6 Reset and measurement during time, tr and tm for clock phase Ø.

Three MOSFET transistors which are driven by the clock phase φ are acting as the role of three switches. After each measurement period, these switches reset the circuit. The circuit contents the power supplies of V_{DD} and V_{SS}respectively equal to 5 and 0 V. The analog ground as the common-mode voltage of the amplifier forms the band-gap reference level and was set to 1.2 volt. The switch at node V_1 is used to reset that node to V_{SS} after each measurement period. The operation of the circuit is as follows. Node $V_1$is reset to V_{SS} during the reset period "*tr*". By following the reset period, the measurement period "*tm*" opens all switches. The charging current *Ib* splits between *Cm* and *Cr*, depending on Δ*C*; this causes to create a differential current signal as discussed in chapter 3. This signal current, passes over the feedback resistors along with the common-mode current; hence, an output voltage is created. Reading output differentially causes the common-mode effects to be rejected. The output is read just before the measurement period finishes (or when the

amplifier output has settled). To prepare circuit for the next measurement period, it is reset once again. Since an ideal amplifier was assumed, the differential output voltage created by the signal current can be given as:

$$V_{out} = V_{op} - V_{om} = R_f . i = R_f . i = R_f . I_b \frac{\Delta C}{2C + \Delta C} \quad (4.1)$$

By solving equation (4.1) (Singh, et al., 2009)with regard to ΔC is obtained:

$$\Delta C = \frac{2C . V_{out}}{R_f I_b - V_{out}} \quad (4.2)$$

This simulation was used in order to calculate ΔC according to the measured output voltage. To limit the voltage at nodeV_1, the capacitors $C_m \; and \;\; C_r$ are reset after each measurement; so, the transistors of the current source operate in the desired region at all time.

4.3 DISCUSSION

After connecting all blocks and applying the input, the output of the figure 4.17 is depicted in figure 4.8 and 4.9, so this is the main result that expected and main reason of choosing such a circuit design.

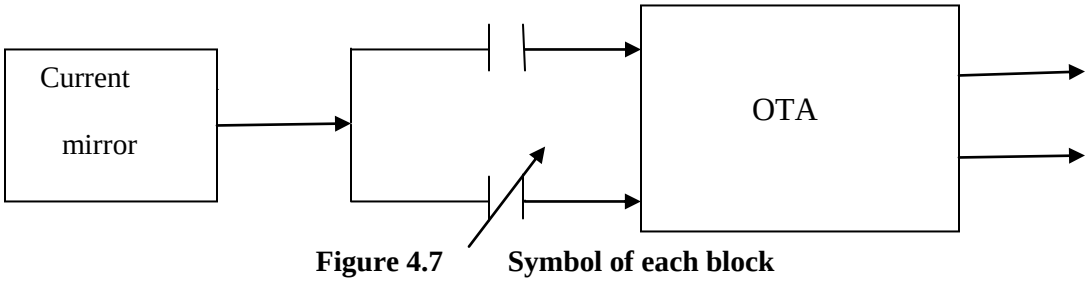

Figure 4.7 Symbol of each block

As can be seen in figure 4.7, the current mirror with a 1μA current is charging both fixed and measurement capacitance. Both capacitors have a nominal value of C (1 pF); however the measurement capacitance is varying in the range of C±ΔC. This makes a different charge relative to the constant capacitance which causes a differential voltage at the differential inputs of OTA. The capacitance difference of capacitors is translated into voltage value. Figure 4.8 shows that, as the measurement capacitance are deviated from its nominal value by a value of ΔC, the differential output value of OTA varies from 0 volt. A variation range equal to 0.5pF is considered in our simulation. As shown in this figure, the ΔC−Vout curve is not linear, which means that no linear relation can be found between ΔC and OTA output voltage.

Actually, as mentioned below, ΔC−Vout curve follows the equation (4.1). In this case, by knowing the output voltage of OTA, the amount of variation from nominal value in measurement capacitance can be easily found. It means that by measuring the Vout, ΔC can be calculated.

To achieve the figure 4.8, measurement capacitance was deviated from its nominal value by steps of 0.1pF and the circuit was simulated for each step of variation to obtain the output voltage. The results give a table with 2 parameters: capacitance variation vs. output voltage.

The equation (4.1) is plotted in figure 4.8 as a case of comparison with the simulation result. It can be seen that a close correlation is available between the simulation results and drawn equation. The little differences are caused by no ideal effects of capacitors (Singh, et .al, 2009; Singh & Ytterdal, 2004). In this simulation and equation, I_b = 2.7μA, R_f = 200KΩ, and C = 1pF.

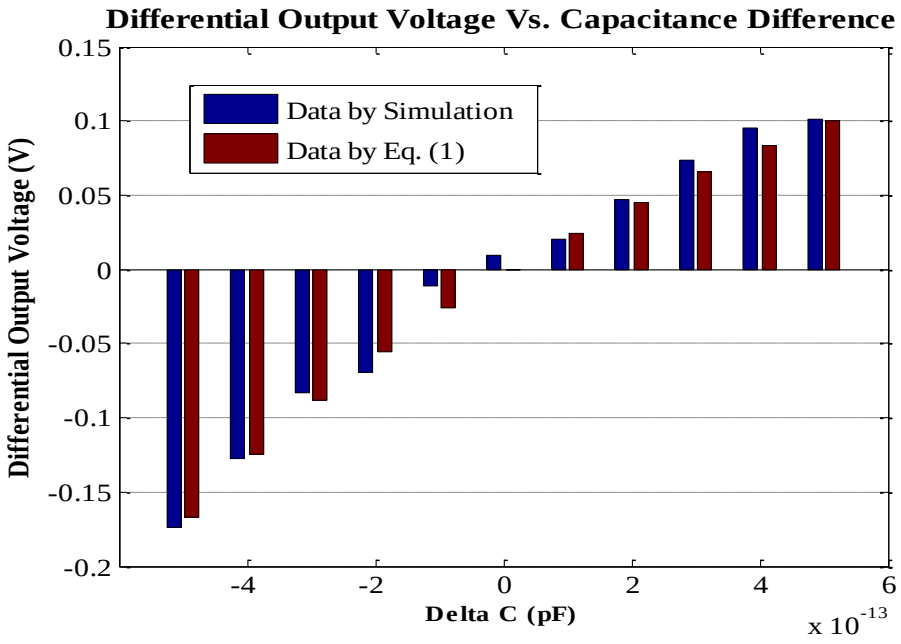

Figure 4.8 Simulation result for output voltage vs. ΔC

The major performance was obtained as figure 4.9. As mentioned before, V1 is reset during t_r applied to make the circuit ready for the next measurement; reset cause to set all the capacitors to zero value. The applied pulse to reset the circuit is so-called "clock phase Ø". The off-pulse t_m is the time that the measurement is done at end of it. That means the differential output voltage is read before this time ends.

As discussed above, three switches are considered as reset switches which cause the capacitors to discharge during reset pulse. These switches are realized by MOS transistors which are driven by clock phase Ø. This causes that V_1 is reset to Vss during reset time.

Figure 4.9 shows the transient simulation result of the circuit. It is considered that the timing must be optimized such that there is enough time for to the capacitors to become discharged and for the output to settle. In this case the clock frequency was set 250 KHz with a duty cycle of 25%. In this case, with a 4µs period, the t_r is 1µs and t_m is equal to 3µs.

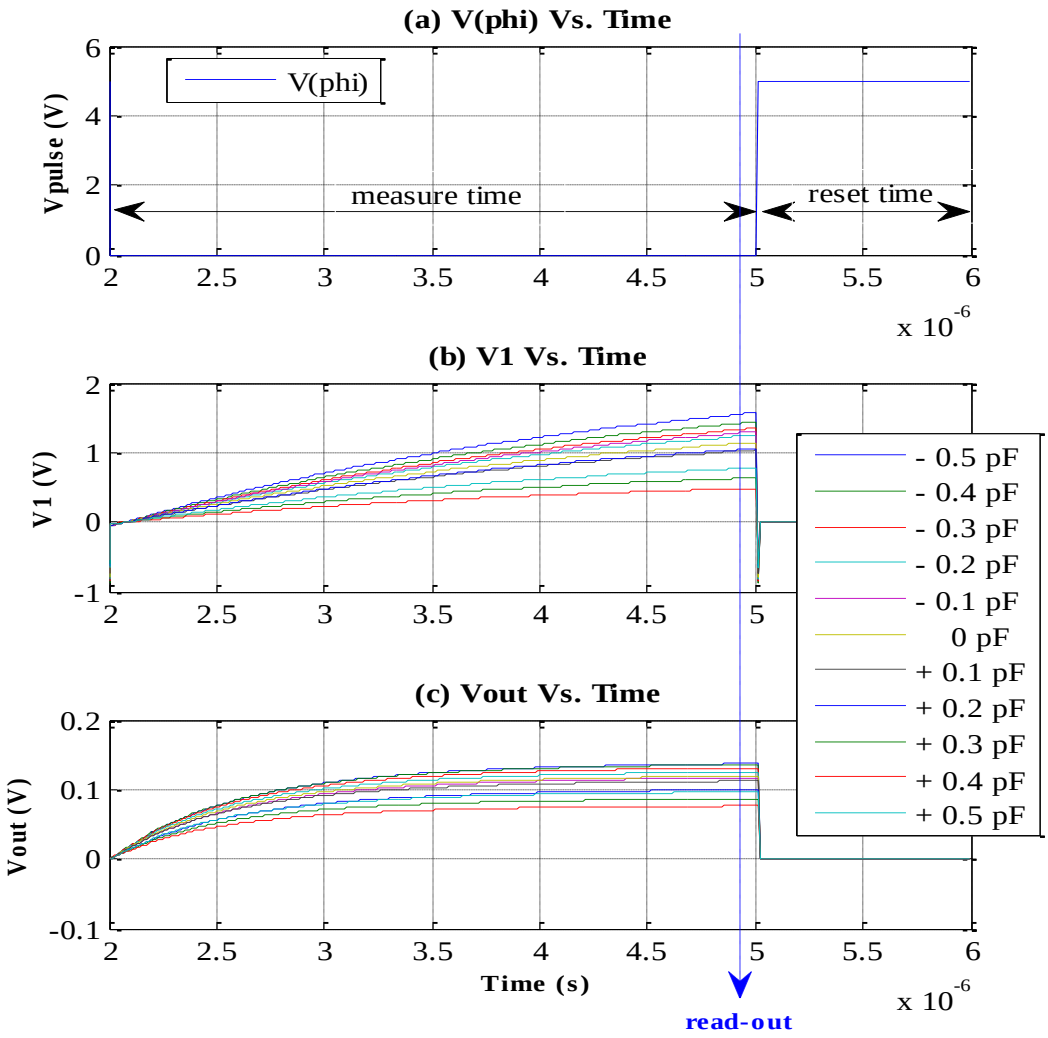

Figure 4.9 Input and output of OTA with different ΔC when the first pulse was given to each switch together.

The R_f value was decided such that the output voltage swing to be within a suitable range. In this case R_f is set equal to 200 KΩ. The figure 4.9 on the top shows the applied clock pulse to the switches. As the measure capacitance varies from its nominal value by a value of ΔC, the voltage at the nod V_1changes as shown in figure 4.9 in the middle. The more ΔC increase, the lower V_1 become. As can been in figure 4.9 in the bottom, voltage at node V_1 is rejected as common mode voltage. (Singh, et al., 2009) As both constant and

measure capacitor are equal to the nominal value, the output voltage is approximately equal to zero; because both are feeding an identical current in the differential input of OTA and the differential input current of OTA is equal to zero. As ΔC increases, the current of capacitors are not the same anymore. Any increase in ΔC has a direct relation with the differential input current. Since the differential input current rises, the differential output current goes up too. The read time is the time that the output is completely settled down. As can been seen in this figure, by measuring the voltage at read time, ΔC can be found easily.

The simulation was performed for different steps of ΔC to show the variation of output voltage clearly. As it is shown in this figure, the voltage at node V1 is completely isolated than the OTA; as it can be reset to a voltage lower the common-mode voltage of OTA.

The table 4.2 presents the performance of some similar projects relative to our work. As it can be seen, our OTA provided high enough gain relative to the others and preserving high output voltage swing beside that.

The power consumption of our work is inacceptable area; however it is not in the lowest rank, but in the middle range. The area occupied by this work after layout and fabrication is the least, because it benefits from a CMOS technology which its minimum length is about 0.18 μm.

Totally, the advantages of this work are dominant relative to its disadvantages; this causes that this work to be a suitable option as an interface circuit.

Table 4.2 Comparison of all works done for this circuit

	Nominal value for C	*ΔC*	*Feedback Resistor*	*Gain*	*Technology*	*Supply voltage*	*Power consumption*
our work 2011	1 pF	1000fF	200KΩ	78dB	0.18-µm CMOS	1.8 V	6 mW
2010	1 pF	1fF	100KΩ	–	0.18-µm CMOS	–	–
2009	1 pF	750fF	200KΩ	90dB	0.8-µm CMOS	5V	–
2006	1 pF	500fF	–	–	0.18-µm CMOS	–	–
2003	1 pF	–	–	80dB	0.25-µm CMOS	1.5V	18mW

As table 4.2 shows, the latest work is done in 2010 (Fruehling, et al., 2010), and before that in 2009 (Singh, et. al, 2009), (Singh & Ytterdal, 2004). These two articles are main references in this project. However, two other works were done in 2006 (Daphtary & Sonkusale, 2006) and 2003 (Lotfi, Taherzadeh-Sani, Azizi, & Shoaei, 2003).

In a paper by Daphtary & Sonkusale, the topology requires much more space as it contains more building blocks; however, the more precision is achieved in the cost of size. In Addition, in the journal paper by Lotfi, Taherzadeh-Sani, Azizi, & Shoaei, a large topology is applied to achieve the lowest power consumption. In this work, a trade-off between size, power consumption, gain, precision and simplicity of circuits is held.

CHAPTER V: CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

In this project, a new design for capacitive sensor interface circuit was proposed. All the circuits were designed in 0.18µm CMOS technology.

5.1 CONCLUSIONS

In this project, first, advantages and applications of capacitive sensor were discussed; then, according to our requirements, one topology was selected and its building blocks were studied, redesigned, optimized and simulated.

The main goal in this project was to design new circuit configurations. The new circuits were selected for current mirror with PMOS configuration and OTA with two stages. Both circuits were designed in 0.18µm CMOS technology; the current mirror is wide-swing current mirror with high impedance that supplies 1µA current and its accuracy is outstanding compared to previous research. The OTA was designed with a two-stage amplifier topology in 0.18 µm CMOS technology and achieved 89dB gain and 3-mW power consumption. After that, two above circuits with two 1-pF capacitors were combined together to develop the capacitive sensor interface. The simulation presented the output voltage versus measure capacitance variation.

This circuit has some advantages and disadvantage such as:

- The proposed solution can produce differential output from single-ended sensors. This differential signal is created at the input of the amplifier itself.
- The method can also be used for resistive sensors, without any need for discharging switches.

- The proposed idea is easy to develop. There is not any need to use the complex signal source, special amplifiers, or switched capacitor circuit.
- The method does not need precise clock phases. Since the amplifier is settled to the necessary precision within the measurement period, the output is not dependent of clock jitter.
- Since the output is measured at the end of t_m as the instantaneous value of the output voltage or signal current, the circuit is resistant to clock feed-through. The output has to settle during the period t_m.
- A standard fully differential amplifier has a benefit of a linear transfer function for differential sensors.

5.2 FUTURE WORK AND SUGGESTION

Further work based on this design, following improvement should be considered:

- layout and fabrication of this circuit
- using this circuit for other sensors rather than capacitive sensors
- improving the gain from OTA
- optimization of noise in the OTA

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