SIMULATION FRAMEWORK OF NBTI DEGRADATION IN NANO-SCALE P-MOSFETS FROM THE PERSPECTIVE OF HYDROGEN AND NON-HYDROGEN TRANSPORT FORMALISM

HANIM HUSSIN

FACULTY OF ENGINEERING
UNIVERSITY OF MALAYA
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ABSTRACT

The rapid downscaling of contemporary bulk CMOS devices has worsened the negative bias temperature instability (NBTI) of p-channel Metal-Oxide-Semiconductor-Field-Effect-Transistors (p-MOSFETs), which consequently degrades the performance and reduces the operational lifetime of the device. The main problem in assessing the level of degradation was due to the recovery components that underestimated the lifetime prediction and performance of the device. As the recovery component issues are solved by the implementation of ultra-fast technique measurement with the measurement done at ~100 ns delay, the reaction-diffusion (R-D) model was no longer reliable as the degradation does not obey the power law. The degradation accountable under the R-D model was only of that based on the generation of interface traps whereas the recoverable components had been glaringly ignored. Therefore, there is a need to accurately model the degradation components and understand their contribution to NBTI subsequently producing a reliable model to predict the lifetime of the devices.

A simulation framework was developed to investigate the recovery characteristics of dynamic NBTI effects in conventional silicon dioxide (SiO_2) dielectric p-MOSFETs based on the hydrogen diffusion and hole- trapping mechanisms. A sequence of train pulses were applied to the gate terminal of p-MOSFET in single and multiple runs, thus emulating repetitive cycles of stress and recovery. The characteristics of the recoverable component, R of dynamic NBTI are explained from the perspectives of the R–D model and hole-trapping mechanism. The understanding of the recovery and permanent components were further extended based on the simulation study on NBTI induced hole trapping in E’ center defects, which led to the de-passivation of interface trap precursors in high-k PMOSFET gate. The resulting degradation was characterized based on the

time evolution of the interface and hole trap densities as well as the resulting threshold voltage shift.

The simulation framework for probing the energy distribution of defect charges was developed by defining the effective energy distribution of defect charges to be distributed under, within and beyond the energy band gap. Under the stress condition, the hole traps were charged up and subsequently the recovery voltage was applied for the de-trapping process. The recovery voltage was applied in the positive direction in steps which permitted the Fermi level at the interface to move from below the valence band edge to above the conduction band edge thereby producing the requisite energy profile. The defect charges originated from different defects consisting of as grown hole traps (AHT), cyclic positive charges (CPC) and anti-neutralization positive charges (ANPC) as suggested by the experimental data. The CPC peak at $E_f - E_v = 1$ eV was apparent in the Fin Field Effect Transistor (FinFET) and planar hafnium, (Hf) based device, suggesting that it is Hf-related.

In conclusion, this work has characterized the defect component's behaviour and its origin, producing simulation results which were in qualitative agreement with published measurements by other researchers. It is important to understand and simulate accurately the influence of NBTI in the initial design phase to guarantee the reliable operation of devices and circuits within a specific lifetime criterion.

ABSTRAK

Pengecilan saiz peranti pukal kontemporari CMOS telah menyebabkan keadaan ketidakstabilan kepincangan negatif suhu (NBTI) p-saluran transistor kesan medan logam oksida semikonduktor (p-MOSFET) bertambah teruk, yang seterusnya mengurangkan prestasi dan jangka hayat operasi peranti. Masalah utama dalam menilai tahap kemerosotan adalah disebabkan oleh kewujudan komponen degradasi boleh pulih yang mempengaruhi ketepatan ramalan jangka-hayat dan penilaian prestasi peranti. Oleh kerana isu berkaitan komponen degradasi boleh pulih dapat diselesaikan dengan menjalankan teknik pengukuran ultra-laju iaitu pada kelewatan ~100 ns, model reaksi-resapan (RD) yang digunakan untuk menerangkan mekanisme NBTI tidak boleh digunapakai kerana tidak mematuhi aturan kuasa. Model RD hanya merujuk kepada degradasi berdasarkan generasi perangkap antara muka manakala komponen degradasi boleh pulih tidak diambil kira. Sehubungan itu terdapat keperluan untuk memodelkan dengan tepat komponen degradasi dan memahami sumbangan mereka dalam degradasi akibat NBTI seterusnya menghasilkan model NBTI yang boleh diterima pakai untuk meramal jangka hayat peranti.

Rangka kerja simulasi dibangunkan untuk mengkaji ciri-ciri pemulihan secara dinamik untuk ketidakstabilan kepincangan negatif suhu (NBTI) ke atas silikon dioksida konvensional (SiO_2) dielektrik p-MOSFET berdasarkan resapan hidrogen dan mekanisme perangkap cas. Satu simulasi jujukan nadi berpanjangan telah dikenakan secara tunggal dan berbilang ke atas terminal get p-MOSFET yang realistik dan telah ditentukur secara teliti lalu menghasilkan proses kitaran tekanan dan pemulihan yang berulang-ulang. Ciri-ciri komponen yang boleh dipulihkan semula, R bagi dinamik NBTI dijelaskan dari perspektif model RD dan mekanisme perangkap cas. Pemahaman ke atas komponen degradasi boleh pulih dan kekal ditingkatkan berdasarkan kajian

simulasi pada kesan ketidakstabilan kepincangan negatif suhu (NBTI) disebabkan perangkap cas dalam kecacatan pusat E', yang membawa kepada ketidakpasifan pemula antara muka perangkap ke atas peranti get jenis high-k. Degradasi yang berlaku dicirikan berdasarkan evolusi masa antara muka dan ketumpatan perangkap cas, serta peralihan voltan ambang yang berlaku.

Rangka kerja simulasi untuk mendapatkan agihan tenaga caj kecacatan dibangunkan dengan mendefinisikan tahap tenaga setiap cas-cas di bawah, antara dan di atas jurang jalur tenaga semikonduktor. Semasa di dalam keadaan tekanan, prosess pengecasan berlaku dan voltan pemulihan kemudiannya dikenakan bagi membolehkan proses penyahcasan berlaku. Voltan pemulihan diaplikasikan secara berperingkat bagi menghasilkan paras Fermi pada antara muka untuk bergerak dari bawah pinggir jalur valens ke atas pinggir jalur konduksi seterusnya profil tenaga yang diperlukan dapat diperolehi. Cas-cas kecacatan berasal daripada kecacatan yang berlainan yang terdiri daripada perangkap cas yang meningkat dari asalnya (AHT), kitaran cas positif (CPC) dan cas anti-peneutralan positif (ANPC) yang mana diterimapakai berdasarkan data eksperimen. Puncak CPC di E_f - E_v = 1 eV terhasil dengan jelas dalam peranti transistor kesan medan logam oksida semikonduktor berstruktur sirip (FinFET) dan peranti dua-dimensi (2D) hafnium, menunjukkan bahawa ia adalah terhasil disebabkan dielektrik hafnium.

Kesimpulannya, kerja penyelidikkan ini telah mencirikan kelakuan komponen kecacatan dan asal-usul mereka, di mana keputusan simulasi yang dihasilkan adalah menyokong secara kualitatif eksperimen yang dihasilkan oleh penyelidik lain. Kaedah simulasi yang tepat perlu dilakukan diperingkat awal rekabentuk dan proses penghasilan peranti p-MOSFET untuk menjamin daya-saing operasi bagi peranti dan litar tersebut serta memenuhi sasaran kriteria jangka-hayat yang diingini.

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μ_{eff}	:	Effective mobility
ε_{SiO2}	:	Dielectric constant of SiO_2
ε_{Si}	:	Dielectric constant of Si
ε_0	:	Electric permittivity of vacuum
ε_{IL}	:	Dielectric constant of the interfacial layer
C_{ox}	:	Oxide capacitance
E_f	:	Fermi level
E_{eff}	:	Effective surface field in the Si substrate
f	:	Frequency
I_d	:	Drain current
L	:	Mask channel length
L_D	:	Debye length
N_A	:	Substrate doping density
N_{it}	:	Interface trap density
n_i	:	Intrinsic carrier concentration in Si substrate
q	:	One electron charge
T	:	Temperature
V_d	:	Drain voltage
V_{fb}	:	Flat band voltage
V_g	:	Voltage applied on the gate
V_t	:	Threshold voltage
ΔV_t	:	Threshold voltage shift
W	:	Mask channel width
CV	:	Capacitance-Voltage

EOT	:	Equivalent Oxide Thickness
HCI	:	Hot Carrier Injection
HDD	:	Highly Doped Drain
HfO_2	:	Hafnium Oxide
IL	:	Interfacial Layer
MOSFET	:	Metal Oxide Semiconductor Field Effect Transistor
NBTI	:	Negative Bias Temperature instability
OTF	:	On-the-fly
R-D	:	Reaction-Diffusion
SCE	:	Short Channel Effect
SDE	:	Source/Drain Extension
SiON	:	Silicon Oxide Nitride
SRH	:	Shockley-Read-Hall Recombination
TaN	:	Tantalum Nitride
TiN	:	Titanium Nitride

CHAPTER 1: **INTRODUCTION**

1.1 Background

Negative Bias Temperature Instability (NBTI) is a degradation phenomenon occurring in p-channel MOSFET and has become an important reliability threat for nano-scaled complementary metal oxide (CMOS) devices. This degradation phenomenon manifests because of the shift in the threshold voltage which subsequently reduces the drain current and the lifetime of the p-channel MOSFET (Chakravarthi, Krishnan, Reddy, Machala, & Krishnan, 2004; S. Mahapatra et al., 2005; Schroder, 2007). This problem causes a time-dependent device variability which can lead to key threats to the reliability of CMOS circuits (M. A. Alam, 2003; S. Mahapatra et al., 2005; Schroder, 2007). NBTI is commonly known to occur due to two types of traps namely the interface trap (M. A. Alam, 2003; S. F. W. M. Hatta, Soin, Hadi, & Zhang, 2010; S. Mahapatra et al., 2005) and preexisting trap which contribute significantly to the degradation (Gao, Ang, Boo, & Teo, 2011; Gao, Boo, Teo, & Ang, 2011; Z. Q. Teo, Ang, & See, 2009; Zhi Qiang Teo, Ang, & Ng, 2010). The hydrogen and non-hydrogen transport formalism are known to be the mechanisms of NBTI degradation based on the contribution of interface traps and preexisting traps respectively.

This thesis highlights the issues in NBTI using a numerical simulation approach in the framework of a Reaction-Diffusion (R-D) Model using conventional SiO_2 dielectric metal-oxide-semiconductor field-effect transistors (MOSFETs). This implements the advanced defect framework of the Two-Stage NBTI model using different technology of p-MOSFET devices. The hydrogen transport formalism

presented by the R-D model was used to correlate the recoverable behavior with the interface trap upon the application of stress. Meanwhile, the non-hydrogen transport formalism is based on the experimental finding able to characterize the NBTI degradation based on the existence of preexisting traps. Those traps are filled upon the application of stress but emptied once the stress was removed. Hence, accurate modeling of the recoverable components is needed to produce reliable lifetime predictions of these devices. In addition to that, recent experimental works have found that the defect charge components contributing towards the degradation were distributed based on their energy levels and distinct properties (S. W. M. Hatta et al., 2013, 2014). Hence, it is important to understand the effects of inclusion of these defects components based on their respective distribution on the energy level in assessing the level of device degradation which will definitely affect the circuit performance over a period of time.

1.2 Motivation

The development of MOSFET technology was largely influenced by the development of integrated circuit (IC) technology where MOSFET integrated in IC is cheaper as compared to bipolar transistors. Using lesser area on the chip for MOSFET integration means that it is cheaper to fabricate. Furthermore, the invention of CMOSFET technology reduced the power consumption of the IC and realized the large scale integration technology (Iwai, Kakushima, & Wong, 2005). The scaling of the CMOS transistors then was most significant in the successful of the IC industry. In the last few decades, progressive scaling in transistor dimensions resulted in increased integration density as predicted by Moore's law (Schuegraf, Abraham, Brand, Naik, & Thakur, 2013). This has enhanced IC performance in terms of speed and functionality. However, as scaling enters the nanometer scale, fundamental

physical limits have started to affect the operational integrity of bulk MOSFETs. In the nanometer regime, the device design, via thinning of gate dielectric and shortening of channel length requires careful control of short-channel effects (SCE) and sub-threshold behaviour (Gusev, Narayanan, & Frank, 2006; Wong, 2002). This has resulted in the evolving need to replace the SiO_2 dielectric.

The revolution of new materials (high-k/metal gate) emerged as they have dielectric constants greater than the dielectric constants of SiO_2. This can contribute to a larger physical thickness dielectric to minimize the SCE while maintaining similar capacitance values (Gusev et al., 2006; Huang, Yang, & Chu, 2010). One of the major potential candidates is hafnium-based dielectrics (Huang et al., 2010). The integration of HfO_2 in high performance MOS devices involves the atomic layer deposition (ALD) process to form a HfO_2 layer upon a thin SiO_2 interfacial layer (IL) on the silicon substrate (Ryan, Lenahan, Bersuker, & Lysaght, 2007). This integration was overwhelmed by many reliability issues, particularly the NBTI (Ryan et al., 2007; Ryan, Lenahan, Robertson, & Bersuker, 2008). Recent studies using electron spin resonance (ESR) indicated that the high density of E' centers around interfacial SiO_2 layer of HfO_2-based MOS devices which contributed significantly to reliability issues. These electrically active defect centers which correlated with the quality and thickness of SiO_2 IL of the transistors exhibited the kinetics of charging and discharging behaviour that contributed to degradation performance (Liugi Pantisano, L-A. Ragnarsson, M. Houssa, R. Degraeve, G. Groeseneken, T. Schram, 2006). Recent NBTI studies involving dynamic NBTI stresses also suggested that the degradation mechanism was related to oxygen vacancy defect (E' center) (Boo, Ang, Teo, & Leong, 2012). These reports clearly indicated the need to investigate the properties of

SiO_2 IL further because of its effects on the resulting HfO_2 layer and the transistor reliability.

Meanwhile, the NBTI studies have been gaining a lot of attention from researchers due to the discrepancy related to the modeling of the kinetics and mechanism of the charges that contributed significantly to the degradation (D S Ang, Teo, Ho, & Ng, 2011; Brisbin & Chaparala, 2008; Maheta et al., 2008; Yang & Liu, 2008). The inconsistency was very much related to the recoverable component associated with the measurement and characterization method utilized during the investigation of the NBTI effects. The recoverable component was identified as the mechanism of hole trapping/de-trapping effect characterized in the ultrafast pulsed I-V method [4], and fast pulsed measurement (FPM) [6]. Two established models used widely in explaining the degradation mechanisms associated with NBTI are the Reaction-Diffusion (R-D) and the Two-stage models respectively which were originally developed by Jeppson et al (Kjell O. Jeppson and Christer M. Svensson, 2004) and (Chakravarthi et al., 2004), then further improvised by Alam et al (M. A. Alam, 2003)and Grasser et al (T. Grasser et al., 2009a) . The R-D model was developed based on the hydrogen diffusion transport mechanism while the Two-stage model was developed by taking into account the contribution of E'center kinetics. These two models were contradictory based on time exponent and the recoverable component behaviour (M.A. Alam & Mahapatra, 2005; D S Ang et al., 2011; Boo et al., 2012; Zhi Qiang Teo et al., 2010).

The recoverable component was associated with the dynamic experimental approach and it was reported recently that the generation is very much inter-related to the pre-existing defect namely, the as-grown hole trap (AHT) and a permanent

component also known as the anti-neutralization hole trap (ANHT) (S. W. M. Hatta et al., 2013). These recoverable component characteristics can be charged and discharged repetitively and are recognized as cyclic positive charges (CPC). The permanent component was found to have energy level close to or beyond energy band gap highlighted as the ANHT (S. W. M. Hatta et al., 2013) and deep level hole trap (DLHT) (D S Ang et al., 2011).

The dynamic experimental approaches which enabled the characterization of the recoverable component was very useful and more significant to the device when operated normally in a system or integrated circuit. The devices will experience either on or off conditions which means that they are in stress and recovery operation (inverter on off). Since the usual operating conditions of modern integrated systems employ a remarkable amount of stress on the transistor, this could contribute to device performance degradation which will eventually affect the circuit's reliability. It is therefore important to appropriately assess the performance and reliability of transistors, and of the systems involving them. To properly evaluate system performance, an accurate NBTI model must be used hence inclusion of the component of charges that contributed toward the degradation together with their distribution with respect to energy levels is necessary. Thus, a robust numerical simulation characterization framework needs to be employed in order to understand the transistor's NBTI with regards to the circuit's performance.

1.3 Aim and Objectives

The aim of this research is to examine the mechanism of NBTI degradation based on the contributions different components towards the degradation associated with R-D and Two-stage models respectively. The component that contributed towards the

degradation is the generated interface traps based on the R-D model. The two-stage model was based on the positively charged E'centres and interface traps with respect to the state occupation. The energy distribution of positive charges in the gate dielectric was redefined under the framework of the two-stage model. The capability of the two-stage NBTI model was enhanced in this study involving the components that contributed towards the degradation based on their energy distribution's profile. Hence, the specific objectives of this work are to:

- Develop a simulation framework to characterize the recoverable component of dynamic NBTI and investigate the NBTI static degradation in the framework of the hydrogen transport model
- Investigate and analyze the effects of gate structural and process defects on high-k dielectric dependence of NBTI in the framework of non-hydrogen transport model
- Develop a simulation framework for probing the energy distribution of positive charges in gate dielectrics by adopting the energy profiling approach

1.4 Scope of work

Prior to the objectives stated above, a simulation framework for characterizing the recoverable component of dynamic NBTI was developed. A systematic simulation setup was used to investigate the static degradation based on hydrogen transport formalism and hence validating the simulation approach. On the other hand, the implementation of the non-hydrogen transport model for NBTI characterization was conducted to investigate degradation issues related to gate structural and process defectivity on high-k dielectric. The probing and extraction method of energy distribution of positive charges in the high-k gate dielectrics was then carried out by

using the simulation framework based on non-hydrogen transport formalism. This probing and extraction method was further applied on conventional SiO_2 dielectric with and without strained technology to show the applicability of the method. The extraction of energy distribution of positive charges was also evaluated on 3D FinFET devices. Finally, the lifetime prediction of the high-k devices and the CMOS inverter performance with regards to NBTI degradation were demonstrated.

1.5 Project methodology

The development of the simulation framework to characterize static degradation and recoverable component of dynamic NBTI in the perspective of the hydrogen transport model was implemented using the Modeling Interface-defect Generation (MIG) software (A. E. Islam, 2014). The implementation of non-hydrogen transport model for NBTI characterization was conducted using the Synopsys Sentaurus TCAD tool ("Simulation of PMOS Degradation with Two-Stage NBTI Model," 2010). Using the non-hydrogen transport model with an energy profiling approach for NBTI-induced positive charges led to the development of the probing and an extraction simulation framework of energy distribution of positive charges in different technology of p-MOSFETs. The classical lifetime prediction approach was used to predict the maximum operating voltage of high-k devices. The mixed-mode simulation was used to demonstrate CMOS inverter performance with regards to NBTI degradation effects. Figure 1.1 shows the overview of the research methodology involved in this thesis.

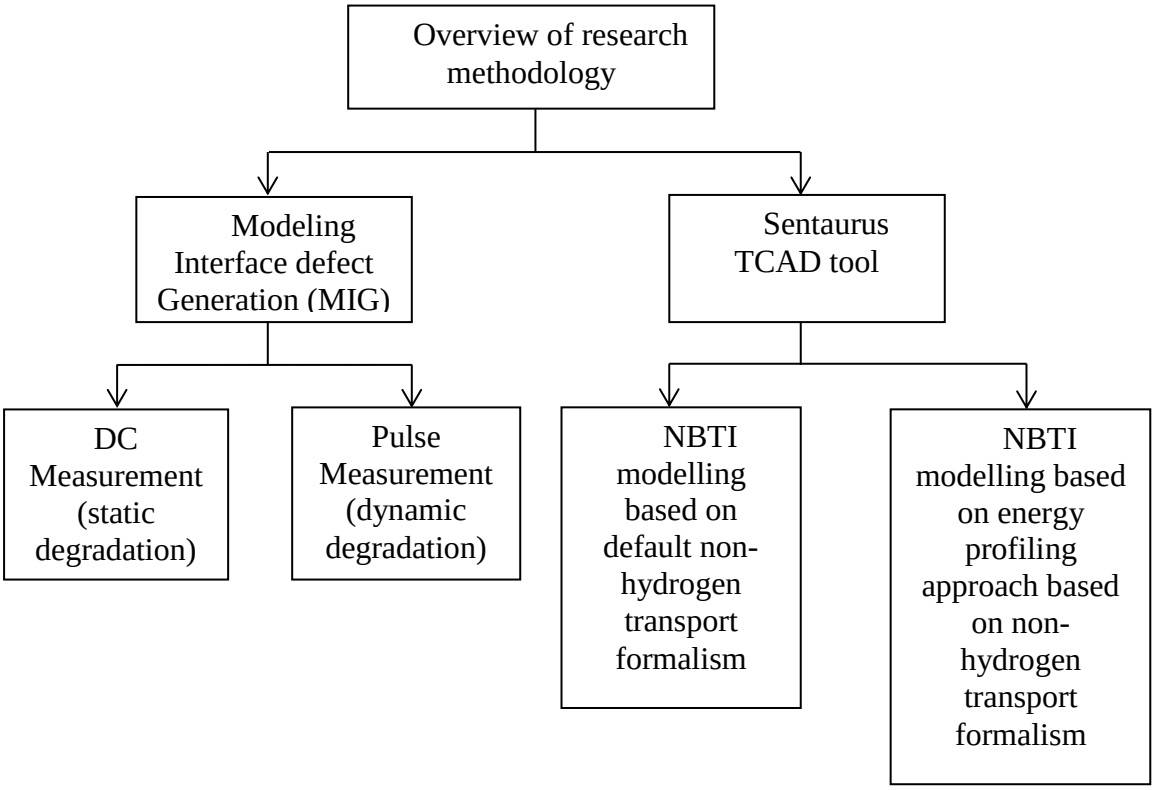


Figure 1.1 Block diagram showing the tools and the approach used in this work

1.6 Thesis outline

This thesis is structured as follows:

Chapter 2 - Literature review section details the essential background on the mechanism of NBTI degradation in the framework hydrogen and non-hydrogen transport formalism on the p-MOSFET. The origin and theory of the transport formalisms are described in detail from the view of measurement and characterization method that rendered each of the transport formalism towards the development of NBTI models.

Chapter 3 – Simulation framework section highlights the simulation framework engaged in this study. It starts with a description of Modeling Interface-defect Generation simulator employed for the R-D model study together with the simulated

device used in the simulator. The simulation methods used to carry out this research using the Sentaurus TCAD simulator are explained, together with the measures assimilated to guarantee trustworthy results. This chapter concludes with a description of the testbed devices used in this work and validated with the fabricated devices as in the literature.

Chapter 4 - Results and discussion section highlights the findings obtained from this work. The effect of static degradation and recoverable component characteristics in the framework of R-D model for conventional SiO2 dielectric p-MOSFETs is examined and presented. The impact of gate structural of HKMG p-MOSFETs and high-k integration issues on NBTI degradation which had been demonstrated based on the default non-hydrogen transport formalism is analyzed. This section also demonstrates the energy profiling approach where extracting the total positive charges and the Fermi level with respect to the valence band (E_f - E_v) is highlighted and validated against experimentally published data. It is presented that this approach is applicable to High-k Metal Gate (HKMG) devices, conventional SiO_2 both with and without strained technology and FinFET devices. Lastly, the default non-hydrogen transport formalism and energy profiling approach is compared based on the degradation level under sub-threshold operation, CMOS switching speed and lifetime prediction.

Chapter 5 – Summary and future work section. In this section, the work presented in this thesis is concluded and reaffirmed. Finally, the direction of future research is discussed.

CHAPTER 2: **LITERATURE REVIEW**

2.1 Introduction

This chapter discusses p-MOSFET reliability, particularly the negative bias temperature instability (NBTI) concerns associated with discrepancies of the defect mechanisms emphasizing on the hydrogen and non-hydrogen transport formalism. The classification, origins and effects of transport formalism are discussed in terms of the modeling approach, experimental method and time exponent inherent, resulting from the experimental methods. Following this, the types and energy distribution of defects are consolidated based upon the experimental approach. Finally, the underlying physics and origin of the two-stage NBTI model is discussed.

2.2 Negative Bias Temperature Instability

The negative bias temperature instability (NBTI) has become an important reliability concern for analog and digital circuits in CMOS technology. This is primarily due to the scaling of gate oxide thickness where the device experiences larger electric oxide fields. NBTI degradation can be observed particularly in p-MOSFET devices when the device is stressed with large negative voltage at temperature ranging from room level to elevated levels (100° C to 220° C) (D S Ang et al., 2011; Boo & Ang, 2012; Gao, Ang, et al., 2011; Gao, Boo, et al., 2011) . Typically, the oxide electric fields applied are within the range of 6 MV/cm to 10 MV/cm (D S Ang et al., 2011; Boo & Ang, 2012; Gao, Ang, et al., 2011; Gao, Boo, et al., 2011). After a certain stress time, the device characteristics are measured. Such fields and temperatures are normally encountered during burn in but are also encountered in high performance ICs during repetitive operation. Under such stressed condition, the detrimental effects contributing to this instability are that the threshold voltage may be deviated from its original values subsequently reducing the drive

current as shown in Figure 2.1. The degradation also affects several other parameters such as sub-threshold slope, the trans-conductance and mobility. This results in the degradation of the circuit performance and reduced lifetime.

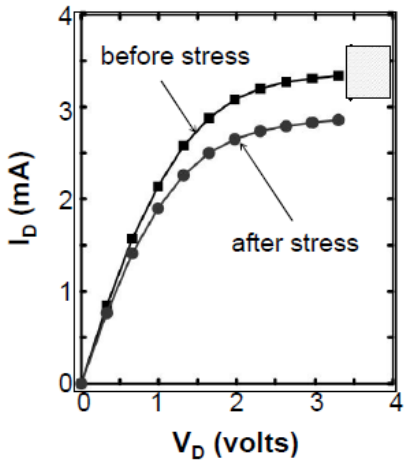


Figure 2.1 Comparison I_D vs V_D before and after stress (Muhammad A Alam & Lafayette, 2005)

There have been reports in literature that explained the physical mechanism behind NBTI. Most experimental works had suggested the reaction-diffusion (RD) model with atomic or molecular hydrogen as the degradation mechanism (M. A. Alam, 2003; Chakravarthi et al., 2004; S. Mahapatra et al., 2005). On the other hand, among recovery issues which cannot be explained by the RD model, the two independent recoverable and permanent components model were suggested by V. Huard et. al. (V. Huard, C. Parthasarathy, N. Rallet, C. Guerin, M. Mammase, D. Barge, 2007). Additionally, dynamic NBTI relates the oxygen vacancy as the source of trapping/de-trapping with inclusion of E'centres in its characterization as significant (D S Ang et al., 2011; Boo et al., 2012; Boo & Ang, 2012; Zhi Qiang Teo et al., 2010). Based on this approach, the NBTI was found to be a non-hydrogen mechanism. The kinetics of

NBTI was further elaborated based on the as-grown defects together with the generated defects known as the AG model, when NBTI was measured under the worst case condition, as proposed by Z. Ji et. al. (Ji, Lin, Zhang, Kaczer, & Groeseneken, 2010). Based on the discrepancy in explaining the physics behind NBTI mechanism, (A. E. Islam, S. Mahapatra, S. Deora, V. D. Maheta, 2011; Ahmad Ehteshamul Islam, Kufluoglu, Varghese, Mahapatra, & Alam, 2007) included the total resultant threshold voltage shift resulting of due to interface trap generation, hole trapping in pre-existing oxide defects and hole trapping in generated oxide defects. In this chapter, this understanding was developed based on the hydrogen transport formalism with the interface trap generation as the defects mechanism while the non-hydrogen transport formalism is indicated by the positive charges consisting of hole trapping in pre-existing oxide defects and hole trapping in generated oxide defects. The hydrogen transport formalism is explained based on the Reaction-Diffusion (R-D) model while the non-hydrogen transport formalism as explained based on experimental work by NBTI populist in recent years.

The R-D model which explained the transport formalism discussed in the following section emphasizes the static and dynamic study conducted by previous researchers. A firm conclusion widely, accepted with regard to the R-D model, is the generation of interface trap as the main contribution in the NBTI degradation. However, there were less work focusing on the relationship between permanent and recoverable component utilizing this model. Therefore, a systematic simulation approach is developed based on the discussion made throughout the hydrogen transport formalism section. Meanwhile, the discussion on the non-hydrogen transport formalism based on different NBTI groups leads to several discrepancies when modeling of this mechanism is not unified. Hence, the enhanced numerical

simulation method to unify the non-hydrogen transport formalism is given, based on the thorough discussion made in the hydrogen transport formalism section.

2.3 Hydrogen Transport Formalism

The hydrogen transport formalism discussed in this thesis is based on the Reaction-Diffusion (R-D) model. Most of the experimental works based on the conventional stress-measure-stress exhibited power-law dependence which is in agreement with the R-D model (M. A. Alam, 2003; Chakravarthi et al., 2004; S. Mahapatra et al., 2005). This model was widely accepted by most NBTI populists.

A recent publication utilizing Modeling Interface-defect Generation (MIG) by Z. Yue (Y. Zhang et al., 2013) based on the static degradation highlighted the exponent n of the generation of interface trap and the resulting exponent's time evolution with varying the stress voltage and stress temperature. Dynamic NBTI degradation, by previous researchers meanwhile focused mainly on the level of degradation by comparing the static and dynamic NBTI is identified. Thorough discussion is provided based on previous published works and the absent analysis based on static and dynamic NBTI will be identified. The following sub-section highlights the R-D model based on stress time dependence of the device degradation as well as the static and dynamic NBTI degradation respectively.

2.3.1 R-D model

It is well known that NBTI origin mechanism is due to the interface traps that are generated subsequent to the applied stress voltage. This mechanism was first proposed by Jeppson and Svensson in 1977 (Kjell O. Jeppson and Christer M. Svensson, 2004) which described degradation based on the reaction-diffusion (RD) model. This model produced the stress time dependence of the device degradation due to NBTI

subsequent to a wide range of stress voltages and temperatures. The degradation was observed to follow the power law dependence against time, with a power factor ranging from 0.16 to 0.3 subsequent to the type of hydrogen occurring during the NBTI degradation process (Chakravarthi et al., 2004).

Figure 2.2 shows the degradation mechanism which attributes the combination of electrochemical reaction and resulting of atomic and molecular hydrogen diffusion.

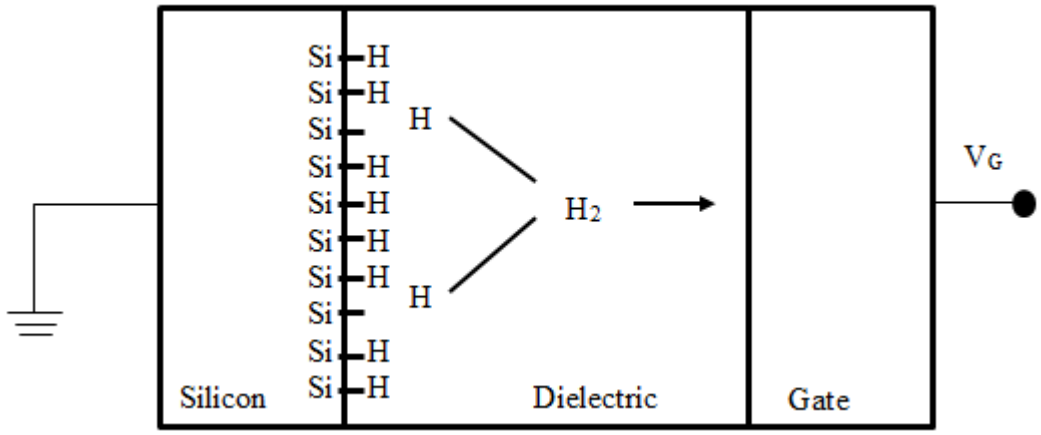


Figure 2.2 Schematic description of the RD model to explain the generation of electrically active interface traps due to NBTI (M. A. Alam, 2003) (S. W. M. Hatta, 2013)

This model provides a general picture where the mechanism of NBTI is contributed by interface states generation. It is an electrochemical reaction in which the S - H bond at Si/SiO_2 interface breaking and the released hydrogen diffuses away from the interface. General electrochemical reaction at Si/SiO_2 is explained in (2.1)

$$\{(Si - H + Y) + A^{+} \leftrightarrow B^{+} + Si^{*} + H\} \quad (2.1)$$

The electrochemical reaction occurs under the presence of A^+ species which produced an interface state Si^*, releases of hydrogen species, H and positive fixed charge B^+ due to the dissociation of the Si-H. The A^+ has been experimentally observed to be a hole in the inverted channel (S. Mahapatra et al., 2005; Yang & Liu, 2008). The generation of interface trap is controlled by a cold hole from inversion layer that tunnel to the oxide layer. It can be generally represented by (2.2)

$$Si - H + h \leftrightarrow Si^* + H \tag{2.2}$$

This electrochemical reaction will produce hydrogen diffusing species, H in the oxide layer together with the interface state, S^*. A lot of research has been conducted on the generation of the interface trap implying the rate equation as shown in (2.3) (Stathis & Zafar, 2006)

$$\frac{dN_{it}}{dt} = K_F(N_0 - N_{it}) - K_R N_{it}[N_{H*}]^{\frac{1}{\alpha}} \tag{2.3}$$

Where N_{it} is the number of interface traps generated, N_0 is the initial surface density of unbroken Si - H bonds with N_{H*} being the number of H^* at the interface. K_F and K_R are constant values which represent forward dissociation and repassivation rates respectively. These constant values are based on the reaction which are controlled by temperature and oxide field dependence. K_F is represented by (2.4) where the process is dependent on oxide field and temperature while K_R is dependent on temperature and represented by (2.5)

$$K_F \approx p_h \, x \, \sigma \, x \, exp \, (\gamma_T F_{ox} - \frac{E_{F0} - \gamma F_{ox}}{kT}) \tag{2.4}$$

$$K_R \approx \exp(\frac{E_R}{kT}) \tag{2.5}$$

Where;

p_h : holes concentration in the inversion channel

σ : cross section where hole tunneling through the Si/SiO2 interface captured

γF_{ox} : dipole binding energy reduction due to electric field F_{ox}

E_{F0} : forward thermal dissociation barrier

E_R : barrier for thermal repassivation

As the hydrogen species are released during the electrochemical process, they will diffuse away from interface Si/SiO_2 within the oxide towards the polysilicon gate. The transport mechanism of the hydrogen species will determine the degree of the degradation mechanism. As highlighted by the research conducted by A. Kerber et. al.(Kerber et al., 2003), the diffusive transport mechanism of hydrogen in the gate oxide is explained by the Fick's law as shown in (2.6)

$$D_{H*}^{ox} = \frac{d}{dx}\left[\left(\frac{dN_{H*}}{dx}\right) - \frac{qF_{ox}}{k_T}N_H\right] = \frac{dN_{H*}}{dt}(0 < x < T_{OX}) \quad (2.6)$$

Where the $D_{H*}{}^{ox}$ represent the diffusion coefficient in the gate oxide.

The hydrogen species will diffuse away from the interface and will recombine with atomic hydrogen to produce molecular hydrogen. Analysis by T. Yang et. al. (Yang & Liu, 2008) focused on the possible diffusing species that contributed to NBTI degradation. Simulation based on different models based on the analysis as shown in (2.7) and (2.8) gave different slopes for different processes. If the atomic hydrogen

model was used, the time dependent is $t^{0.25}$ while for molecular hydrogen, the time dependent is $t^{0.165}$ (M. A. Alam, 2003; Chakravarthi et al., 2004).

$$SiH + h^{+} <=> Si^{+} + H^{0} \tag{2.7}$$

$$SiH + h^{+} <=> Si^{+} + 0.5H_2^{0} \tag{2.8}$$

The interface generated, following the hydrogen diffusion process, is power-law stress time dependence as shown in Figure 2.3. It is clearly seen here that the interface traps are generated at different rates upon the applied stressing time.

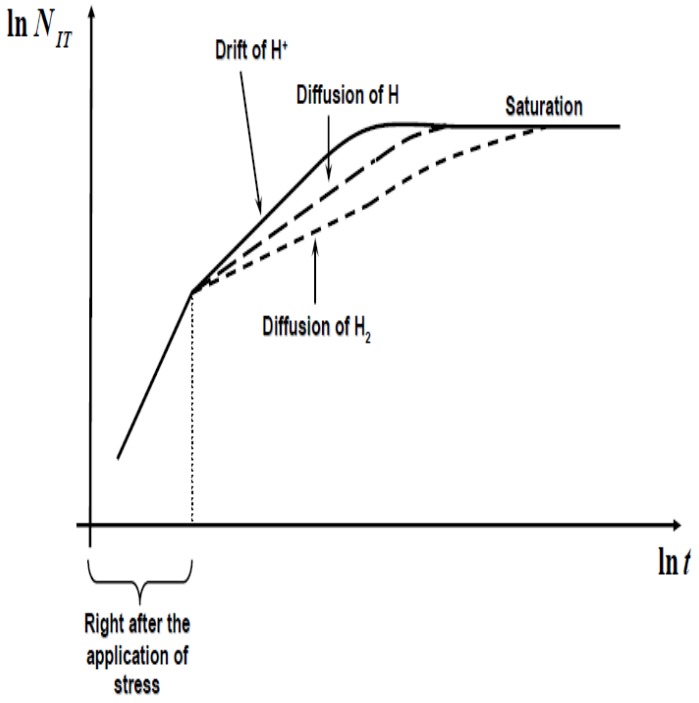


Figure 2.3 Interface trap generated based on reaction and diffusion regimes using R-D model (A. E. Islam, 2014)

Significant research on various aspects of NBTI degradation, based on the R-D model, has been reported. Most of this research was conducted to study the effect of

stress temperature and gate voltage on the NBTI degradation by experimental (Huard & Denais, 2004; Iwai et al., 2005; Schroder, 2007; Yang & Liu, 2008), analytical (A.E. Islam et al., 2007; Warren, 1995; Ce Z. Zhao et al., 2008) and simulation approaches (S. F. W. M. Hatta et al., 2010; Wan Muhamad Hatta, Abdul Hadi, & Soin, 2011). Additionally, the power-law time exponents reported, based on the literature exhibited, dependence experimental conditions such as the stress-measure-stress, on-the-fly and ultrafast pulse measurement techniques respectively. The recently reported time exponent of $n \sim 0.1$ by ultrafast switching measurements (D S Ang et al., 2011; Zhi Qiang Teo et al., 2010) cannot be explained by the hydrogen-transport mechanism of the R–D formalism. Most of the novel measurement method including on-the-fly (Kumar et al., 2007), ultrafast pulsed I–V(Boo & Ang, 2012; Du, Ang, Teo, & Hu, 2009), and fast-pulsed measurement (Yang & Liu, 2008) were developed to minimize the recovery effect.

2.3.2 Static degradation

The dependence of the static and dynamic degradation from the perspective of hydrogen transport formalism were studied based on different stress conditions, various process and device parameters (S. Mahapatra et al., 2005; Schroder & Babcock, 2003; Y. Zhang et al., 2013). The static degradation studied by Y. Zhang (Y. Zhang et al., 2013) found that the time evolution of the exponent n was found to rely on the stress conditions by means of the shift of the onset of the diffusion-limited phase was observed. Analysis on the diffusion profiles found that the atomic hydrogen species generated was highly correlated with the stress conditions which accurately matched the generation of interface trap. However, the diffusion of the hydrogen species was not affected by the stress voltage but had strong relationship with the stress temperature. Earlier reports on the static degradation emphasized that

the proper choice of stress gate bias was important to accurately characterize NBTI effects (S. Mahapatra et al., 2005). NBTI degradation must be assessed from low to moderate stress gate voltage to avoid impact ionization so that hot holes (HH) can be generated. The generation of HH during higher stress gate voltage can be injected back into the oxide and can contribute to the oxide trap generation. From the R-D model's viewpoint, the oxide trap is not accounted hence contribution of oxide trap in the degradation led to an invalid proposition of R-D model.

2.3.3 Dynamic degradation

Study of dynamic NBTI is more important as the actual functioning routine of most CMOS circuits, such as logic gates, has MOSFETs being constantly switched on and off upon the application of '0' and '1' voltage signals. During dynamic NBTI stress, the MOSFETs will recover straightaway from the degradation with the electrical parameters partially returning to the pre-stress value when the stress is removed. It is therefore important to understand the recovery mechanism as the recovery phase during degradation where characterization offers extra margin of lifetime as compared to the case where only static stress with no recovery phase is measured. Previous studies on dynamic NBTI degradation highlighted that the degradation is not frequency dependent (B. Kaczer, T. Grasser, J. Franco, 2011). Comparison between DC and AC stress exhibited threshold voltage shift for DC stress at approximately 2 times larger than AC stress as shown in Figure 2.4 (B. Kaczer, T. Grasser, J. Franco, 2011). Hence, the additional reliability margin can be considered when designing the circuit with the objective of obtaining more accurate projection of the circuit's functional lifetime.

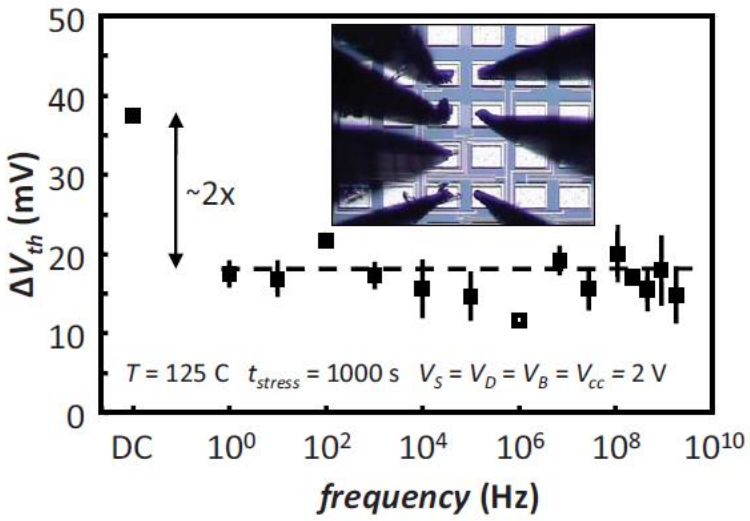


Figure 2.4 Threshold voltage shift is not dependence on the applied frequencies during AC NBTI testing and the DC stress shows ~2x more threshold voltage shift compared to AC NBTI. The inset is the measurement for AC NBTI (B. Kaczer, T. Grasser, J. Franco, 2011)

With regards to the digital circuit operation, the average length of time a signal being in the high state can vary between 0% and 100% over the entire cycle of the signal. From Figure 2.5 (B. Kaczer, T. Grasser, J. Franco, 2011), it can be observed that the reliance of BTI on the stress signal's duty factor (DF) showed weak dependence between DF of 10% to 90%. However, when the stress signals are of the outermost values of DF, there is a fast increase of threshold voltage shift. It is suggested that the magnitude of degradation was dependent on the DF particularly at the greater range of DF values. This greater range of DF values approaching to that of a DC stress but the frequency of the applied AC signal appeared to have no impact on the degradation.

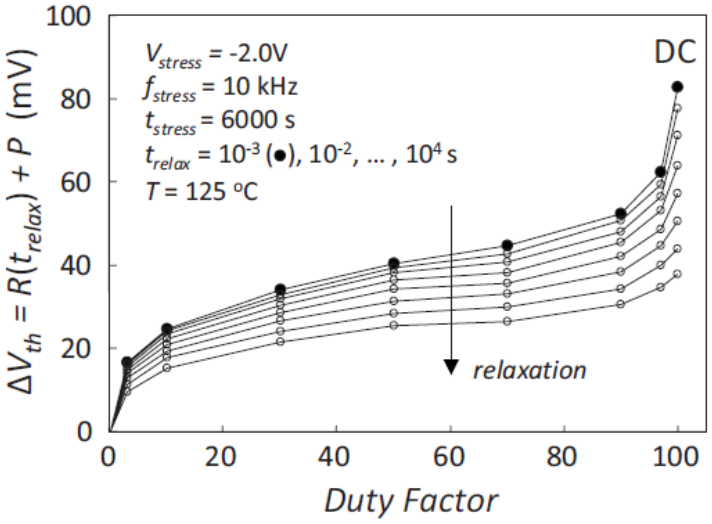


Figure 2.5 Total threshold voltage shift due to permanent and recoverable component at different relaxation times. From 10% to 90% the threshold voltage shift is observed to be weak dependence of DF but increase rapidly for outermost DF values. (B. Kaczer, T. Grasser, J. Franco, 2011)

The NBTI study based on AC condition is very much related to the recovery effect when the transistor is in the 'off' state. Thus, in-depth investigations of the recovery characteristics are very important to further understand the mechanism of degradation with the recovery issues. This recovery effect was ascribed to annealing of interface traps by free hydrogen in the gate dielectric in the perspective of the R-D model (M.A. Alam & Mahapatra, 2005; Chakravarthi et al., 2004). For device operating in AC condition, the recovery process during the 'off' state will eventually extend the device lifetime. However, for the characterization of device itself, when the stress is removed, the BTI degradation subsequently recovered very quickly within microseconds. Hence, this resulted in incorrect assessments of the degradation level.

With regards to the recovery issues that distorted the characterization of NBTI, several researchers developed techniques known as fast measurements to reduce the recovery effects. The fast measurements such as On-The-Fly, fast pulse Id-Vg and

ultrafast measurements were developed to minimize the recovery effects. Experimental techniques that can minimize the recovery effects and characterize the recovery found that NBTI cannot be explained solely by the interface state generation which were against the R-D model. Hence, the validity of this model was questioned as the recovery characteristics from the experimental observation could not be reproduced. In relation to these issues, NBTI populists like the pioneering authors of the R-D model developed a comprehensive theoretical framework in order to explain the vital and experimental signatures of NBTI based on the R-D model. The comprehensive theoretical framework confirmed the overall legitimacy of R-D theory from the perspective of DC and AC NBTI respectively. The authors developed the theoretical framework based on the universal and non-universal features of NBTI. The universal component can be consistently explained using the R-D model based on the interface defect dynamics while the non-universal component depend on the amount of oxide defect within the dielectric. To accurately explain the features of NBTI degradation, these two components are suggested to be decomposed hence the respective features will be explained based on their underlying theories. The next section will covers the non-hydrogen transport formalism of NBTI characteristics which is identified as contribution toward NBTI degradation and not only due to interface state generation.

2.4 Non-hydrogen Transport Formalism

The non-hydrogen transport formalism in this thesis provides the explanation of the recovery characteristics which cannot be explained through the RD model. There were several reports that showed that the RD model was incapable to explain the recovery characteristics (D S Ang et al., 2011; T. Grasser et al., 2009b; Huard, Denais, & Parthasarathy, 2006)(Tibor Grasser, Kaczer, et al., 2011). The experimental

works focusing mostly on the non-hydrogen transport model were carried out by two groups of prominent researchers who focused on dynamic NBTI (D S Ang et al., 2011; Boo et al., 2012; Boo & Ang, 2012; Gao, Ang, et al., 2011; Z. Q. Teo, Boo, Ang, & Leong, 2011; Zhi Qiang Teo et al., 2010) and the characterization of positive charges in the gate dielectric (S. W. M. Hatta et al., 2013, 2014; Ji et al., 2010; Jian F Zhang, Zhao, Chen, Groeseneken, & Degraeve, 2004; Ce Z. Zhao et al., 2008) respectively. Both experiments utilized the pulse current-voltage setup for measurement with a faster speed as compared to the conventional measurement using current-voltage. The concept of this pulse measurement approach was first developed by Kerber et al to study the large charge trapping effect occuring in high-k dielectric (Kerber et al., 2003). This pulse measurement approach enables the characterization of recovery experimental features which highlighted that the total degradation is contributed not only by the interface traps but also the pre-existing and the generated oxide defects. The key characteristics of every experimental result that become the NBTI signature by all the groups is explained in detail in the following sub-sections.

2.4.1 Two-Stage NBTI Model

The development of a two-stage NBTI model was initiated to point out that the degradation components consisted of recoverable and permanent components. The permanent component here is associated with the interface trap while trapped holes are usually responsible for the recoverable component (Huard & Denais, 2004; V. Huard, C. Parthasarathy, N. Rallet, C. Guerin, M. Mammase, D. Barge, 2007).

The two-stage model was developed based on a two stage process where the first stage consisted of the application of stress while holes can be trapped into near-interfacial oxygen vacancies through the multiphonon emission or multiphonon-field-

assisted tunneling (MPE/MPFAT) process. The MPE process was based on the invoked elastic tunneling process which featured temperature activation and larger time constants. The derivation of MPE is based on the assumption that electric fields which are neglected were not appropriate for the NBTI case (T. Grasser et al., 2009a). Hence, the MPFAT process is the extension of MPE of the large electric fields which was developed for the emission of particles from deep traps (T. Grasser et al., 2009a). In the second stage, the holes concentration that was increased enhanced the creation of poorly recoverable defects which are the P_b- centres in SiO_2 layers and k_N centres in oxynitrides.

The development of the two-stage model focuses on the properties of E'center which can act as a switching trap which has been modeled based on the Harry-Diamond-Laboratories (HDL) model (T. Grasser et al., 2009a). The E' center can be repeatedly charged and discharged where its energy-levels are within the silicon band gap (T. Grasser et al., 2009b). When this model implemented the E'centres to describe the hole trapping phenomenon, the oxide charge component played an important role in its contribution towards NBTI degradation (T. Grasser et al., 2009a). This is in agreement with the experimental work conducted by (D S Ang et al., 2011; Boo et al., 2012; Zhi Qiang Teo et al., 2010) where the hole trapping was not only the parasitic component and hence cannot be neglected when assessing the NBTI degradation. The HDL model of the E'center was then extended to couple between E' and Pb centres by introducing an E'/Pb H complex as illustrated in Figure 2.6 which forms the two-stage model (T. Grasser et al., 2009a).

Referring to Figure 2.6, Stage One is the oxygen vacancy where upon the application of stress, hole will be trapped that will positively charge E'center obtained

as shown in State Two. The assumption is made where there is available number of hydrogen passivated at silicon dangling bond at the interface and will be de-passivated upon the migration of the hydrogen to the dangling bonds which is formed at the E'center. To explain this, the extended HDL model for capturing the coupling between E' and P_b centres was realized by the introduction of the E'/Pb H complex. By introducing the E'/PbH complex, the migration of hydrogen can be modeled where the positively charged E'center will attract the hydrogen from the PbH hence the E'/Pb H complex is then moved to State 4. Thus, dangling bond and fixed positive charges are created.

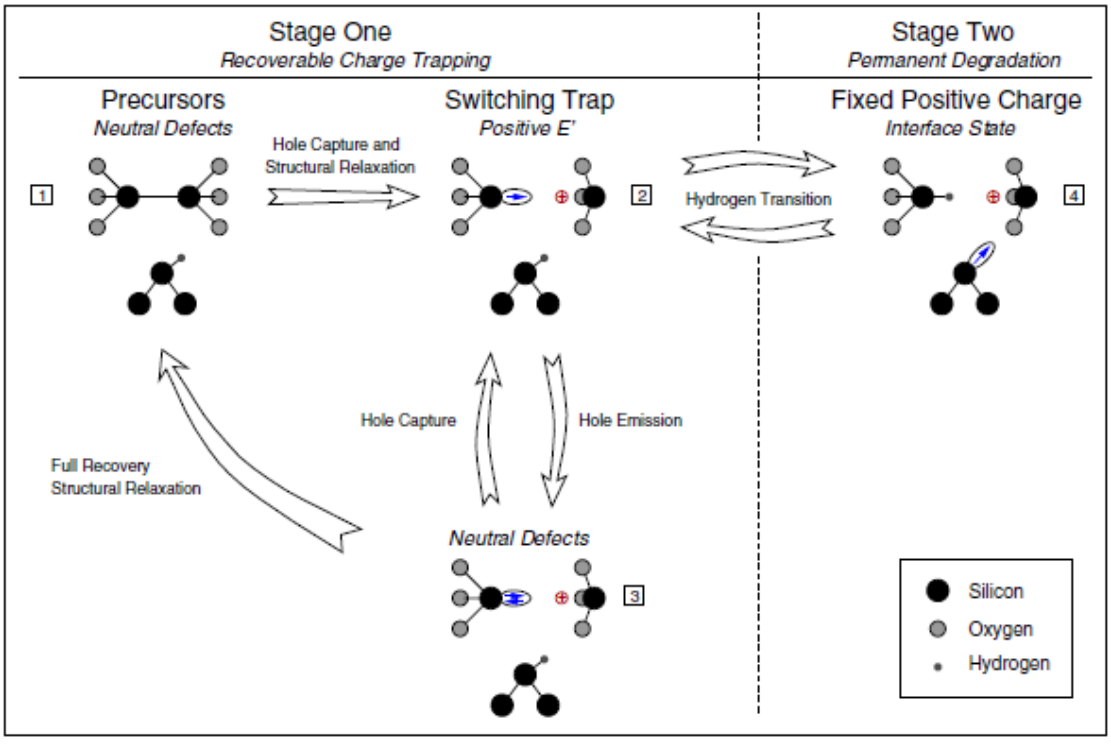


Figure 2.6 Two-stage model consist of extended HDL model to explain the switching oxide trap linked to the generation of a dangling bond at the interface (T. Grasser et al., 2009a)

During State 4, the generated dangling bond or interface trap is assumed to be positively charged above Ef and below the mid-gap. However, there is a contradictory assumption related to the interface trap occupancy between the developed model and the claims made by (A.E. Islam et al., 2007). The occupancy of interface trap reaches its equilibrium value in the nanosecond to millisecond regime when the Fermi level is below E_v when stress moves to mid-gap (A.E. Islam et al., 2007). This model hence assumed that the energy level of the interface trap will be distributed below the energy mid gap.

2.4.2 Dynamic NBTI Characteristics

The dynamic NBTI was experimentally shown to have non-hydrogen transport characteristics. This claim was made by (Zhi Qiang Teo et al., 2010) where the dynamic NBTI data do not support the key characteristics of the hydrogen transport formalism where the self-limiting recovery effect occurred. The self-limiting recovery, as observed in R-D model characteristics attributed that the number of interface traps recovered decreased as the number of repeated stress and recovery cycles increases. Hence, the threshold voltage shifted when the number of repeated stress and recovery cycles increase was reduced (D S Ang et al., 2011). Meanwhile, for the dynamic NBTI with non-hydrogen transport formalism, evidence showed the consistentency of threshold voltage shifted when the number of repeated stress and recovery cycles increases (D S Ang et al., 2011). These two observations are shown in Figure 2.7 (D S Ang et al., 2011).

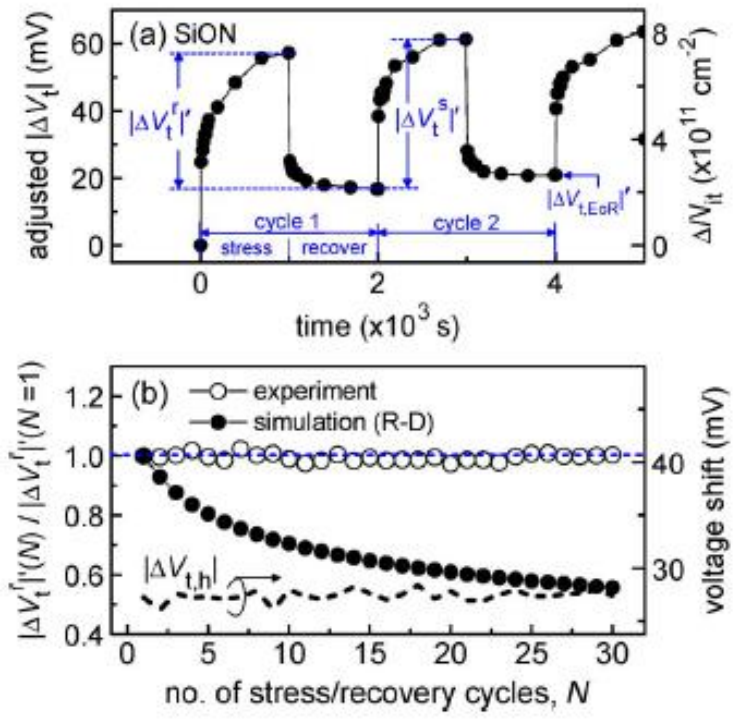


Figure 2.7 (a) Dynamic stress shows the evolution of threshold voltage shift with the definition of the $|\Delta V_t^r|$ and $|\Delta V_t^s|$ with the generation of interface trap (b) Dynamic stress gives the recoverable component is constant regardless of number of stress and recovery cycle while R-D model shows the recoverable component is reduced as number of stress and recovery cycle increased (D S Ang et al., 2011)

The theoretical explanation for this non-hydrogen transport formalism was attributed to the switching hole trap mechanism, which can be switched between the interface-state generation and relatively permanent deep-level hole trap. Based on the experimental data observed in (Zhi Qiang Teo et al., 2010), the switching hole trap behaviour under the dynamic NBTI stress is confirmed as the threshold voltage shift after stress, $|\Delta V_{t,r}|$ and after recovery, $|\Delta V_{t,s}|$ is approximately equal as depicted in Figure 2.8. This implied that upon the negative stress voltage applied to the gate, the hole traps are positively charged and was then discharged totally when the stress voltage was removed. A dynamic NBTI model is proposed based on the E'center

features which is suitable to be the candidate for the switching hole trap at the Si/SiO_2 interface. A two-stage NBTI model developed based on the properties of the E'centres is as discussed previously.

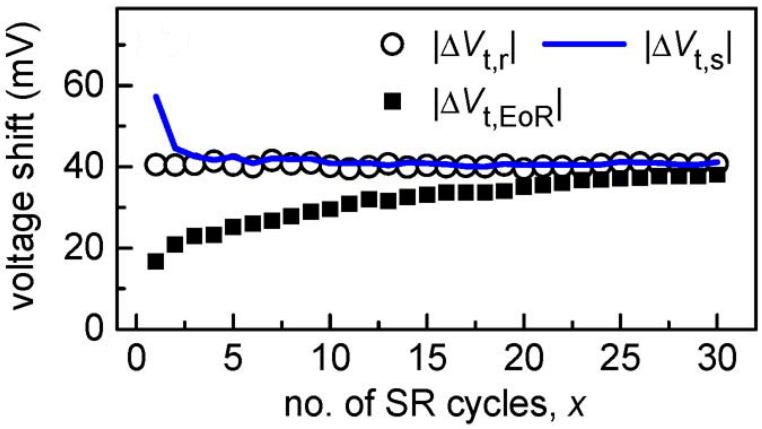


Figure 2.8 Comparison between $|\Delta V_{t,r}|$ and $|\Delta V_{t,s}|$ which gives a view on the characteristics of the switching oxide trap (D S Ang et al., 2011)

This dynamic NBTI with non-hydrogen transport formalism characteristics was obtained following the experimental method employed in the ultrafast measurement. The ultrafast switching measurements showed time exponent of $n \sim 0.1$ (D S Ang et al., 2011; Zhi Qiang Teo et al., 2010). An alternative mechanism proposes oxygen vacancy defects (E′ centers) that can act as hole-trapping sites in the gate dielectric (Warren, 1995) in which structural relaxation is reported to depend significantly on stress voltage and temperature (Boo et al., 2012; Boo & Ang, 2012). The resilience of the trapped-holes sites to the applied stress is manifested in the form of a recoverable component of dynamic NBTI observed during the recovery phase (Boo et al., 2012; Boo & Ang, 2012; Gao, Boo, et al., 2011). Oxygen vacancy defects are the major cause of trapped-hole sites in which structural relaxation can be marginal or large, depending on the stress conditions. Such defects have been extensively discussed in

(Gao, Ang, et al., 2011). Marginal and large structural relaxations redirect trapped-hole sites after removing stress. Trapped-hole sites can be annihilated under marginal structural relaxation or they can become permanent under large structural relaxation that transforms the recoverable component into a permanent component when stress introduces oxide network distortion (Gao, Ang, et al., 2011). The oxide network meanwhile may experience large distortions subsequent to the applied high stress condition.

2.4.3 Framework of Positive Charges

The framework of positive charges in gate dielectrics was first discovered by Zhang et al (Jian F Zhang et al., 2004) where the inconsistent behaviour originated from the existence of different types of positive charges in SiO_2. Two types of positive charges that significantly contributed to the NBTI degradation were previously identified. The first is the trapped hole that can be fully recovered to its precursor state while subsequent hole injection needed to be recharged. The second is the positive charge also known as recoverable where the hole injection was not needed as it can simply be positive recharged under a negative bias (Freitag, R. K., Brown, D. B., & Dozier, 1994; Trombetta, L. P., Feigl, F. J., & Zeto, 1991). The understanding of the second type of positive charges signatures is still poor as the formation of this type of positive charges are still confusing among the published literature. Several reports on the characterization of this positive charge referred this kind of positive charges as the slow states (Lai, S. K., & Young, 1981), border traps (Fleetwood, 2002), switching oxide traps (Lelis, A. J., & Oldham, 1994) and anomalous positive charges (Stahlbush, R. E., Cartier, E., & Buchanan, 1995; Young, D. R., Irene, E. A., DiMaria, D. J., De Keersmaecker, R. F., & Massoud, 1979).

The framework of positive charges which were published in (Jian F Zhang et al., 2004; Ce Z Zhao, Zhang, Groeseneken, & Degraeve, 2004; Ce Z. Zhao et al., 2008; Zhao, C. Z., & Zhang, 2005) highlighted that there are three different types of hole traps which are as-grown hole trapping (AHT), the cyclic positive charge (CPC) and the anti-neutralization positive charges (ANPC). The AHT is pre-existing traps which is available even before the stressing. The CPC is charges that can be recover upon the removal of the stress bias while ANPC is the charges that are hard to be neutralize. Each of the positive charges has its own signature (S. W. M. Hatta et al., 2013, 2014). The AHT is confirm to be originated from the pre-existing defect as it is insensitive to stress time and temperature. The CPC was found to be insensitive to stress temperature but sensitive to stress time. The ANPC was found to be sensitive to both stress temperature and stress time. The separation of these three types of positive charges was conducted by (Ce Z. Zhao et al., 2008). Figure 2.9 shows the procedure on how to separate these positive charges. The Substrate Hole Injection (SHI) was used to stress the p-MOSFET device in order to create the positive charges. Here, the neutralization process was carried out by adopting the Fowler Nordheim Injection (FNI). Subsequent to this procedure, the device was stressed and neutralized alternately with negative and positive bias with the oxide field, Eox ~ +-5 MV/cm and other terminals grounded.

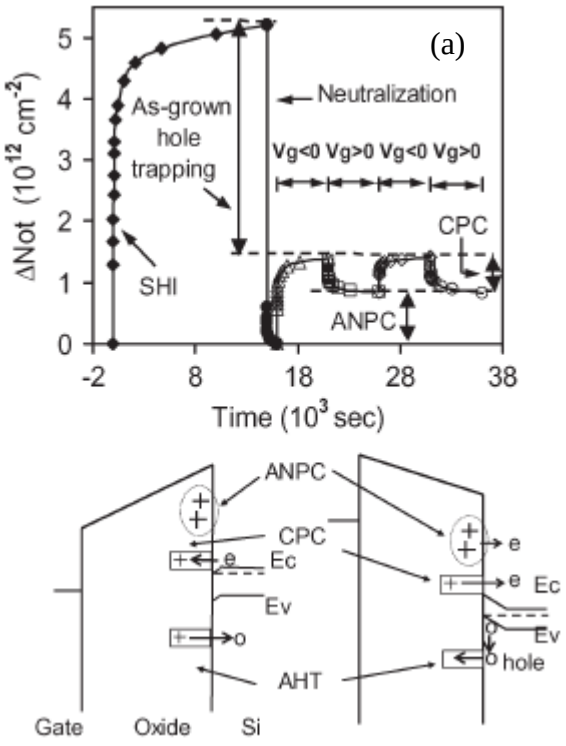


Figure 2.9 (a) Procedure for separation of three types of positive charges: as-grown hole trapping (AHT), cyclic positive charges (CPC) and anti neutralization positive charges (ANPC) by adopting SHI and FNI during stress and neutralization respectively (b) and (c) Energy levels of each types of the positive charges during neutralization and recharging respectively (Ce Z. Zhao et al., 2008)

2.5 Power Law Time Exponent, Type and Energy Distribution of Traps

Currently, the explanation on NBTI degradation mechanisms differs based on the experimental method by most known NBTI populists (M.A. Alam & Mahapatra, 2005; D.S. Ang et al., 2009; S. W. M. Hatta et al., 2013; Zhi Qiang Teo et al., 2010). Each of the mechanisms introduced different defects that contributed to the degradation. For the stress-measure-stress (SMS) experimental method, the degradation is due to the hydrogen transport mechanism (M.A. Alam & Mahapatra, 2005). This mechanism is based on atomic and molecular hydrogen where the time

exponent, n is ~ 0.25 and ~ 0.16 respectively. However, by using the SMS experimental method, the deep level hole trap (DLHT) effect gave time exponent, n of 0.3 when positively charged up (D.S. Ang et al., 2009). The ultrafast measurement emphasized previously produced time exponent of n ~ 0.1 and suggested due to the holes trapped at pre-existing oxide defects. The differences between time exponent, n based on hydrogen transport formalism (M.A. Alam & Mahapatra, 2005) and DLHT (D.S. Ang et al., 2009) which implemented the same experimental approach may be attributed due to the application of high positive stress bias. Hence, (D.S. Ang et al., 2009) can scan the DLHT located near and above the silicon conduction band edge. The analysis on experimental work in (M.A. Alam & Mahapatra, 2005) was mainly on the negative bias, therefore only the interface trap can be assessed. The framework of positive charges discussed in the previous subsection showed that there were three different types of hole traps consisting of as-grown hole trapping (AHT), the cyclic positive charge (CPC) and the anti-neutralization positive charges (ANPC). Recent works within the framework of positive charges to determine the threshold voltage shift due to AHT found that the time power exponent, n ~ 0.2 and is independent of stress gate voltage (S. W. M. Hatta, 2013). Thus, it can be concluded that the time exponent, n is very much related to the mechanism of NBTI. The following subsection will emphasize on the energy distribution of each mechanism.

2.5.1 The interface traps (N_{it})

The interface trap is believed to be electrically active throughout the energy band diagram (Schroder, 2007). They are acceptor-like in the upper half and donor-like in the lower half of the band gap. The polarities of the traps depend on the condition of the device as shown in Figure 2.10. For p-MOSFET, during flatband condition as shown in Figure 2.10 (a), donor-like traps are electrically neutral (‘0’) because the

electrons occupy the interface states below the energy mid-gap. Below the Fermi level and above mid-gap, the occupied acceptor-like traps were charged ('-'). Above the Fermi level, the unoccupied acceptor-like traps stay electrically neutral. During strong inversion condition in Figure 2.10 (b), the interface traps was positively charged ('+') due to the empty donor-like defect states hence producing negative threshold voltage shifts. The assessment of this interface trap based on discussion in (M.A. Alam & Mahapatra, 2005) highlights the hydrogen transport mechanism modeled after reaction-diffusion (R-D) model.

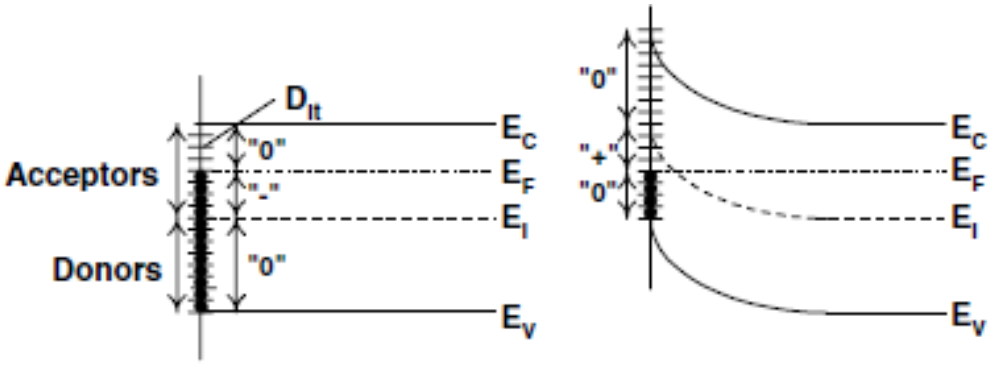


Figure 2.10 The occupancy of interface traps and resulting charge polarities on the band diagrams of p-MOSFET at (a) flatband condition (b) inversion condition (Schroder, 2007)

2.5.2 The deep level hole traps (DLHT)

The characterization work on DLHT made by group (D S Ang, Wang, Du, & Hu, 2008; D.S. Ang et al., 2009) provided new insights with evidence that the NBTI stress induce positive trap states are above mid-gap. The concept of positive trap states induced due to NBTI is shown in Figure 2.11. Upon the application of NBTI stress, Figure 2.11 (a) shows positive traps states are induced from E_v to above E_c within the wide energy distribution of the oxide bandgap. When the stress bias is removed,

narrow positive trap states relax naturally through the electronic charge exchange with the n-Si substrate while the deeper trap states with their energy levels near and above E_c are permanently positively charged as shown in Figure 2.11 (b). This is due to the tunneling electrons from the n-Si substrate not able to reach the trap states. When a positive bias is applied, the deep-level positive trap states are lowered below E_c as shown in Figure 2.11 (c) subsequently occurring a discharging process hence the threshold voltage shift is recovered.

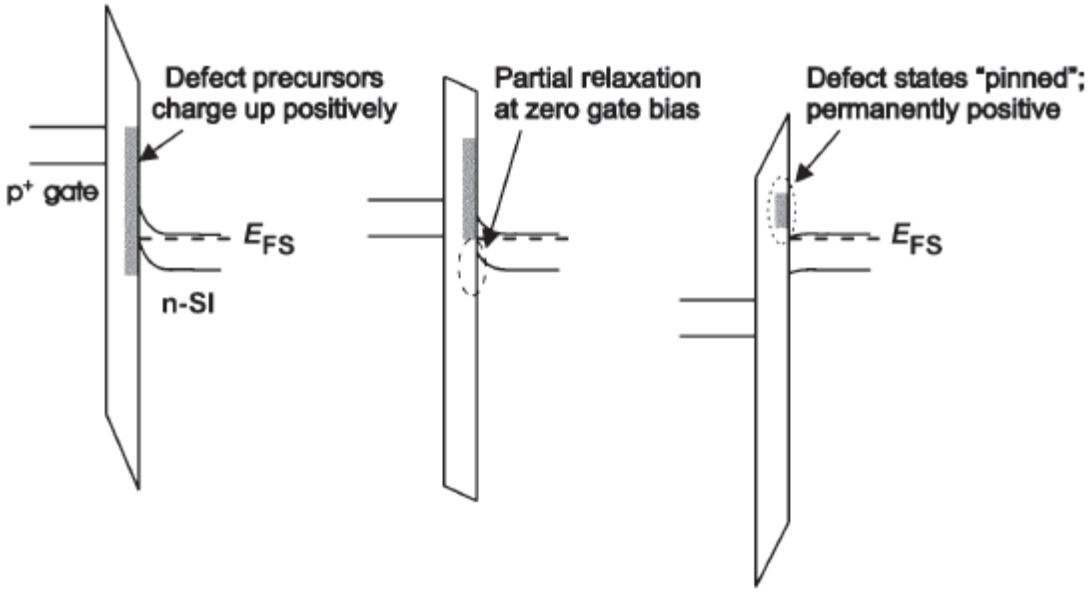


Figure 2.11 Energy band diagrams at different biasing condition for p-MOSFET (a) negative bias (b) zero bias and (c) positive bias (D S Ang et al., 2008)

2.5.3 As-grown hole trapping (AHT), cyclic positive charge (CPC) and anti-neutralization positive charges (ANPC)

Each of these positive charges has their own signatures as observed experimentally. In addition to that, they are also sensitive to energy level and vary significantly over the energy range (S. W. M. Hatta et al., 2013, 2014). The procedure

of extracting the energy distribution of positive charges in p-MOSFET with SiON dielectric was discovered by (S. W. M. Hatta et al., 2013) and illustrated in Figure 2.12.

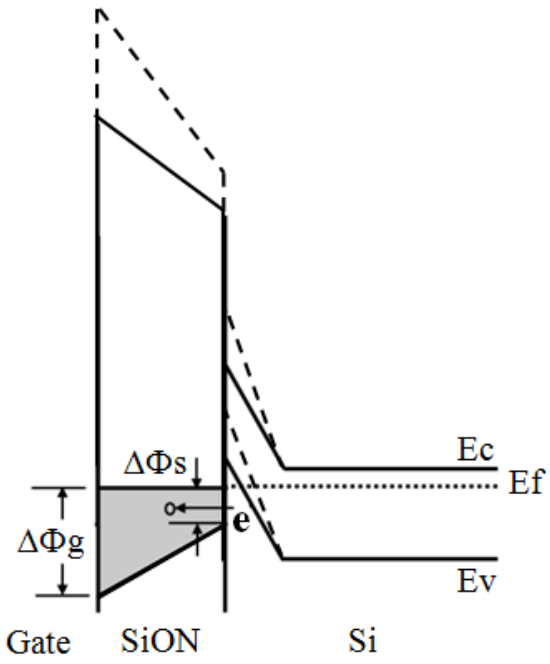


Figure 2.12 Schematic diagram to show the principle of extracting the energy distribution of positive charges. The $V_{discharge}$ is swept from negative stress level to positive, hence the Fermi level will move below E_v to above E_c (S. W. M. Hatta et al., 2013)

The probing of energy distribution procedures utilized the concepts of varying the $V_{discharge}$ over a sufficiently large range so that the E_f can be swept over a wide energy range at the interface as well as the region above E_c. When more positive $V_{discharge}$ was applied during each discharging step, the energy level of positive charges is dropped with respect to the substrate, thereby accommodating a new shaded region below E_f for discharging. The energy distribution extracted based on this principle is referred to as "effective" energy distribution, as the effective density of positive charges was used to induce the threshold voltage shift of $\Delta V_{th} = -qN_{eff}/C_{ox}$, where N_{eff} and C_{ox} is

the effective charge density and oxide capacitance respectively. From the probing procedure, the AHT, CPC and ANPC are located below, within and beyond the energy band gaps respectively as shown in Figure 2.13. It must be noted that during this probing process, the impact of interface trap was not taken into account as the contribution is very small.

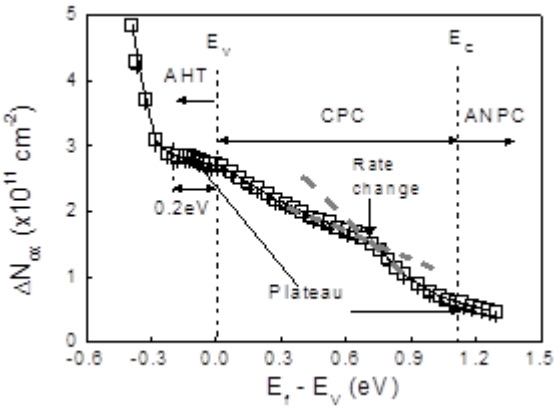


Figure 2.13 The energy distribution of positive charges. The AHT is distributed below Ev, CPC within the energy band gap while the ANPC above energy band gap (S. W. M. Hatta et al., 2013)

The positive charges below Ev originated from the AHT imposed experimental signature which are insensitive to stress time and temperature (S. W. M. Hatta et al., 2013). The positive charges above Ev are created from defects which consist of CPC and ANPC. The CPC distributed within the energy band gap has experimental signatures which are saturated at longer stress time and higher stress temperature (S. W. M. Hatta et al., 2013). Meanwhile, the ANPC is distributed above Ec did not saturate and was significantly more for higher temperature (J.F. Zhang, 2009; Jian F Zhang et al., 2004; Ce Z. Zhao et al., 2008).

2.6 NBTI Degradation in High-k based devices

Negative Bias Temperature Instability (NBTI) is a critical reliability issue for deca-nanometer MOSFETs which is further exacerbated with the introduction of high- *k* gate dielectrics. The integration of high-k gate dielectrics in future advanced CMOS devices remains a challenge as indicated by several studies on the existence of trapping centers in the 'bulk' HfO_2 and centers within the Si/dielectric interfacial layer (IL) which are causes of degradation in the device performance (Ryan et al., 2008). The existence of these trapping centers has been established by the electron spin resonance measurement (Ryan et al., 2007, 2008), and therefore it is important to understand the exact mechanism of the hole trap transformation process in each layer of the gate stack. It is broadly agreed that NBTI degradation mechanism involves hole captures in the high-*k* oxide E' centers and the generation of interface trap, N_{it}, under a negative bias gate voltage stress, leading to threshold voltage shift, ΔV_{th} (Gao, Boo, et al., 2011; Zhi Qiang Teo et al., 2010). This stress-induced ΔV_{th}, may include contributions from both the trap centers of HfO_2 and within the IL (Neugroschel et al., 2006). However, how the geometric properties of the HfO_2 metal gate stack PMOSFETs affect the kinetics of E' centers and generation of interface traps based has not been thoroughly investigated. The resulting findings could help device designers keep BTI-related degradations and gate leakage in check for future advanced devices.

Many published works related to the varied geometrical structure of High-k/metal gate stack found that there is a strong correlation between the physical thickness and NBTI degradation (S. F. W. M. Hatta et al., 2010; Neugroschel et al., 2006). However, the trend of the degradation with respect to the variation of physical

thickness was not uniformed that highly depends on the device technology as well as the stress conditions.

Figure 2.14 (a) - (g) shows published works on the geometrical effects on NBTI degradation. The interface trap density which contributed to NBTI degradation can also be reduced upon the optimization process of the High-k/metal gate stack's physical thickness (Bae et al., 2006; S. F. W. M. Hatta et al., 2010; M. A. Negara et al., 2007).

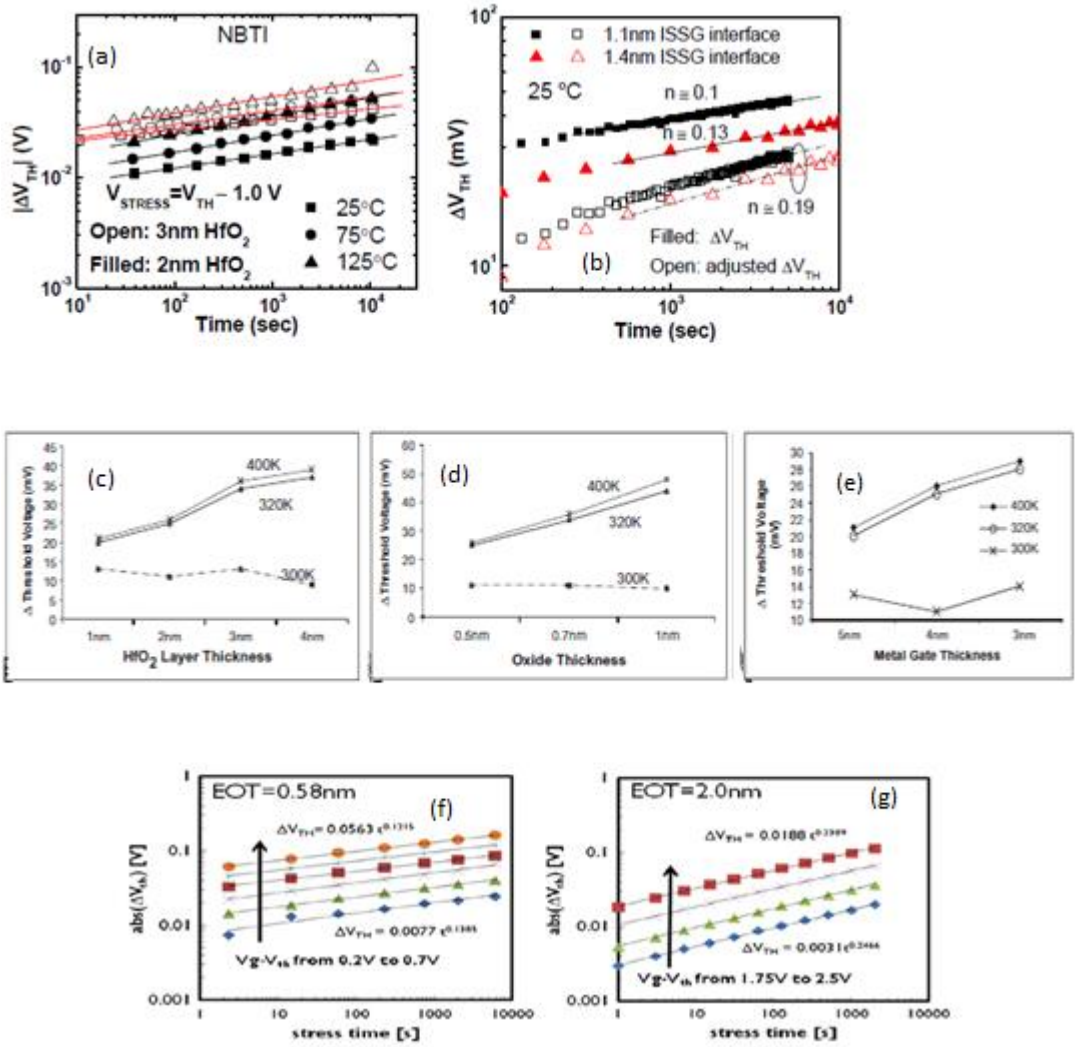


Figure 2.14 (a) - (g) Geometrical effect on NBTI degradation (Bae et al., 2006; S. F. W. M. Hatta et al., 2010; M. A. Negara et al., 2007)

2.6.1 E' center defects in SiO_2 Interface Layer

There has been outstanding progress made in the integration of HfO_2-based dielectrics in advanced deep-submicron MOSFET devices replacing conventional SiO_2 dielectrics. This was primarily motivated by the ability of high-*k* materials to yield bigger gate capacitance with less leakage current resulting in enhanced drivability and transistor performance in CMOS technology. However, high-k specific issues related to mobility degradation, compatibility with metal gate and threshold voltage instabilities still remained and need to be addressed. These issues are related to defects, traps and charges inside the high-k layers (Luigi Pantisano, L-A. Ragnarsson, M. Houssa, R. Degraeve, G. Groeseneken, T. Schram, 2006; Mitard, Leroux, Reimbold, Martin, & Ghibaudo, 2006).

The integration of HfO_2 in high performance MOS devices involves the atomic layer deposition (ALD) process to form a HfO_2 layer upon a thin SiO_2 interfacial layer (IL) on the silicon substrate (Ryan et al., 2007). This integration was overwhelmed by a host of reliability issues, particularly the negative bias temperature instability (NBTI) (Ryan et al., 2007, 2008). Recent studies using electron spin resonance (ESR) indicated that the high density of E' centers in interfacial SiO_2 layer of HfO_2-based MOS devices significantly contribute to reliability issues. These electrically active defect centers which are correlated with the quality and thickness of SiO_2 IL of the transistors exhibited the kinetics of charging and discharging behaviour which contributed to degradation performance (Luigi Pantisano, L-A. Ragnarsson, M. Houssa, R. Degraeve, G. Groeseneken, T. Schram, 2006). The density of E' centers in the layer largely depended on the processing temperature of SiO_2 (Ryan et al., 2007)(S. C. Song, C. S. Park, J. Price, C. Burham, R. Choi, H. C. Wen, K. Choi, H. H. Tseng, 2007). The oxygen transport between high-k and SiO_2 interface has been

investigated in a study of the effects of V_{fb} roll-off in scaled SiO_2 IL (S. C. Song, C. S. Park, J. Price, C. Burham, R. Choi, H. C. Wen, K. Choi, H. H. Tseng, 2007). It is found that oxygen-deficient silicon sites, V_O^+, were generated as the SiO_2 IL thickness increased, which then reduces the transistor's threshold voltage. Due to the high density of E' defects in the SiO_2 IL, it has been suggested that the IL is an oxygen-deficient silicon-rich dielectric and not a stoichiometric SiO_2 subjected to the processing details (Luigi Pantisano, L-A. Ragnarsson, M. Houssa, R. Degraeve, G. Groeseneken, T. Schram, 2006). The quality of the formed SiO_2 IL greatly affects the timing of transient charging instability which influences the pre-existing defects concentration (Luigi Pantisano, L-A. Ragnarsson, M. Houssa, R. Degraeve, G. Groeseneken, T. Schram, 2006). Recent NBTI studies involving dynamic NBTI stresses also suggested that the degradation mechanism is related to the oxygen vacancy defect (E' center) (Boo et al., 2012).

2.6.2 Dipole layer effect on High-k Devices

As the creation of interface trap and pre-existing defects in the dielectrics leads to a reliability performance, another important issue that needs to be highlighted is the dipole layer formed within the interface layer between HfO_2 and SiO_2 IL. The exact mechanism and origin of dipole layers are still being debated as well as whether it influences the flatband and threshold voltage shift (X. Wang et al., 2010). The creation of dipole layer is understood to be due to the areal density difference of oxygen atoms at high-k/SiO_2 interface as shown in Figure 2.15 (Tseng, 2010). From the energy band diagram shown in Figure 2.15, the effective work function (EWF) changed depending on the type of dipole. Therefore, in this study, the dipole interface model was incorporated to investigate the relationship of threshold voltage shift

phenomena with respect to NBTI stressing as the dipole surface density changed in scaled SiO_2 IL.

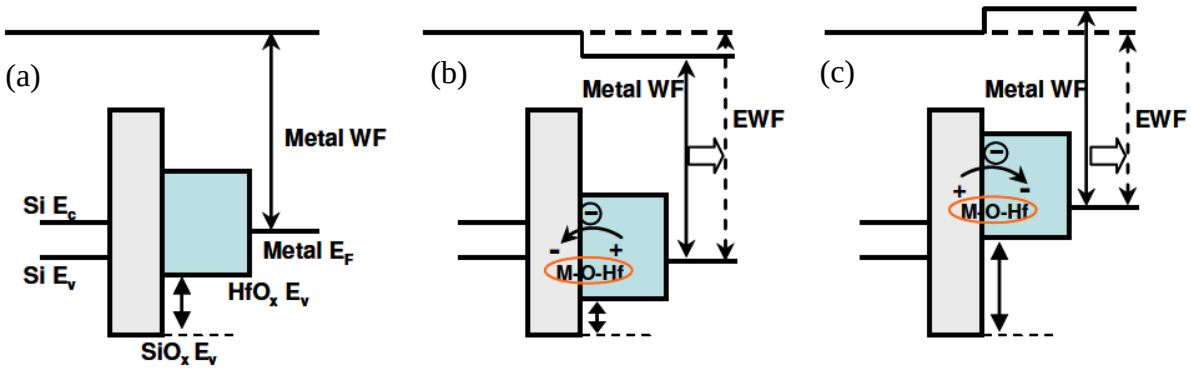


Figure 2.15 Band diagram illustrating the EWF change of metal gate depending on the type of dipole (a) without internal dipole (b) with negative type dipole (c) with positive type dipole (Tseng, 2010)

Published work in (Rasouli & Banerjee, 2010) found that the work-function variation can give a significant fluctuation impact in device reliability particularly in bias temperature instability. They showed that the work-function variation was the main source of variation in metal gate devices.

2.6.3 Work function of metal gate

Metal gate implementation consists of two choices which are single metal electrode and dual metal gate work function (Tseng, 2010). Single metal electrode for CMOS integration process has several advantages as compared to dual metal gate work function. The integration was more straightforward as well as less difficult in gate etching process optimization and control. However, for single gate metal electrode, the effective work function needs to be tuned in order to obtain proper n-type and p-type threshold voltage (Tseng, 2010). The dual metal gate electrode will have different work function for NMOS and PMOS which are 4.1 eV and 5.2 eV

respectively. The optimized work function is crucial to ensure that the short channel effect (SCE) can be reduced (Rechem, Latreche, & Gontrand, 2009). The effective work function can be tuned to desired values by several approaches like using different deposition technique that enables the single metal with dual work functions gates to be used in CMOS (Ana, 2011). In another study, the impact of modulating the effective work function if TiN by changing the metal gate thickness, post-deposition annealing (PDA), oxygen incorporation and also variation of nitrogen concentration (Han, Ma, Yang, & Wang, 2013) was addressed. All the modulation techniques showed significant impact to modulate the metal gate to be suitable for PMOS application. Dipole formation, as highlighted in the previous section can also tune the effective work function with the appropriate thin cap layer deposited on the high-k gate dielectric (Tseng, 2010). Several published work highlighted the effects of work function on the performance of the device. In (Rechem et al., 2009), no impact was observed on drain-induced barrier lowering (DIBL) and subthreshold slope (S) for device with channel length more than 10 nm. The increase work function gave an increase in the threshold voltage but decreased the leakage current.

2.7 Simulation Tools

2.7.1 Modeling Interface-defect Generation (MIG)

MIG simulator was developed by the reliability group from Purdue University (A. E. Islam, 2014). This simulator can be freely accessed from www.nanohub.org specifically used to study the effect of Negative Bias Temperature Instability (NBTI) in p-MOSFET devices. This simulator was developed based on the Reaction-Diffusion (R-D) model where the change in interface traps can be estimated and thus the threshold voltage shift can be observed depending on the stress conditions given (A. E. Islam, 2014). The mechanism of NBTI degradation based on R-D model is

based on the atomic and molecular hydrogen transport formalism where the generation of interface trap is stress driven (Y. Zhang et al., 2013). The theoretical explanation on the R-D model is explained in Section 2.3.

2.7.2 Sentaurus TCAD

In Sentaurus TCAD simulator tools, Sentaurus Device was used to simulate the electrical characteristics of semiconductor devices, as a reaction to external electrical, thermal or optical boundary conditions forced on the device. This software is capable to simulate the fabrication, operation and reliability of semiconductor devices ("Sentaurus TCAD Industry-Standard Process and Device Simulators," 2012). The simulation tools will enable the problem to become more computationally manageable where characterization of early reliability related problems associated with the particular of devices can be conducted at industrial simulations level (Bukhori, 2011; Kamsani, 2011; Liu, 2014). This is based on the numerical simulation of TCAD tools being solved based on the physics-based process modeling which can exactly model the semiconductor fabrication processes such as implantation, annealing, etching, doping and others. Subsequently, characterization of devices based on the I-V and C-V characteristics were produced using the Sentaurus Device tool computed using a finite element discretisation method to solve the semiconductor transport equations (Bukhori, 2011).

2.7.3 Simulation techniques for semiconductor device in Sentaurus TCAD

Semiconductor device simulation techniques are available based on the calculation involved in solving the fundamental physical model. Those techniques were used depending on the technology of the devices together with the computational related issues. In this section, each of the techniques involved in solving the semiconductor

physical computation will be highlighted. Each of the simulation methods is categorized based on the physical model. Six important categories of the physical models were identified in this work consisting of the carrier transport model, mobility models, generation-recombination models, electrostatic potential models, stress mechanical model and degradation model. Each of the categories is shown in detail in Figure 2.16.

The non-hydrogen transport formalism was studied using the Two-stage NBTI model calculated alongside the semiconductor device physical models which were required in this framework as identified.

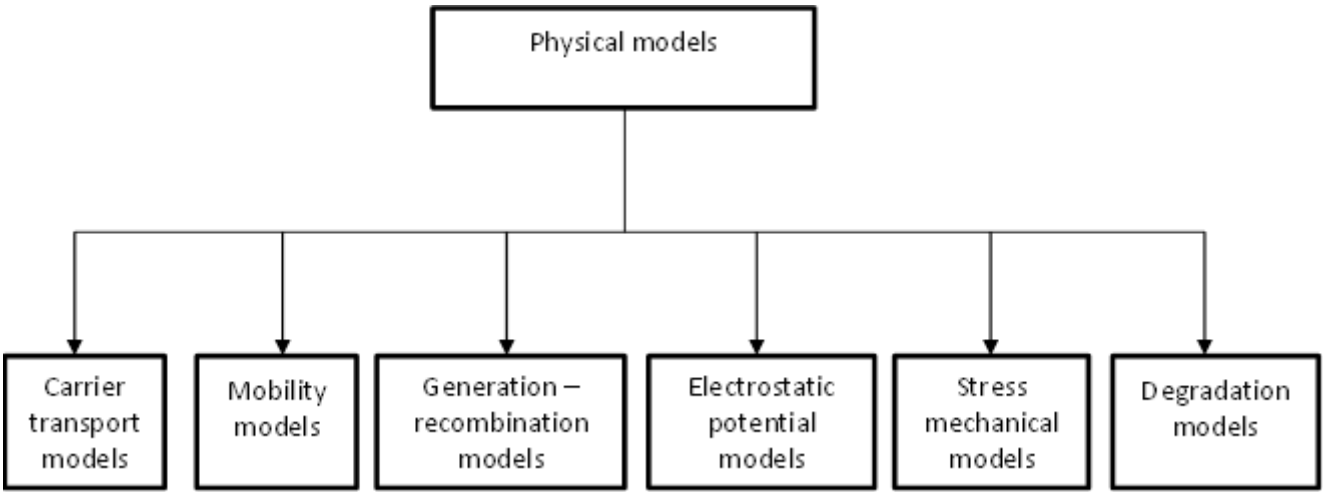


Figure 2.16 Categories of important physical models ("Sentaurus Device User Guide," 2013)

2.7.3.1 Carrier Transport Models (Carrier)

Sentaurus TCAD simulator supports five different transport models where each of them can be selected depending on the type of device under study and level of modeling precision required. The five different transport models are Drift-Diffusion,

Thermodynamic, Hydrodynamic, Quantum Transport and Monte Carlo as shown in Figure 2.17.

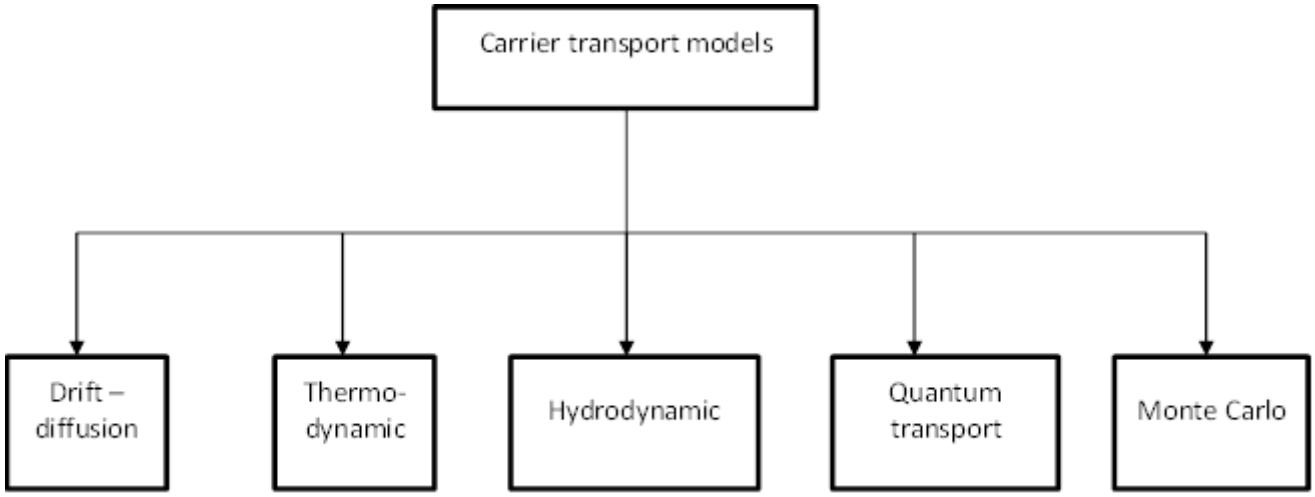


Figure 2.17 Carrier transport models ("Sentaurus Device User Guide," 2013)

All carrier transport models can be written in the form of continuity equation, which describe the charge conversation:

$$\nabla . J_n = qR_{net} + q\frac{\delta n}{\delta t} \quad (a) \qquad -\nabla . J_p = qR_{net} + q\frac{\delta p}{\delta t} \quad (b) \qquad (2.9)$$

Where:

R_{net} is the net recombination rate

J_n is the electron current density

J_p is the hole current density

n and p are the electron and hole density, respectively

The carrier transport models vary in the expression used to compute J_n and J_p. Brief explanation on each carrier transport model and selected model justified in this work are highlighted in this section.

(a) ***Drift-Diffusion Transport***

Drift-diffusion (DD) model is the simplest carrier transport model which solves the self-consistently coupled Poisson and carrier (electron or hole or both) continuity equation (Eq. 3.1) in the chosen device region with specified boundary conditions. The current densities for electrons and holes model are given by (2.10):

$$J_n = -nq\mu_n \nabla \varphi_n \qquad (2.10\ (a))$$

$$J_p = -pq\mu_p \nabla \varphi_p \qquad (2.10\ (b))$$

Where

μ_n and μ_p are the electron and hole mobilities

φ_n and φ_p are the electron and hole quasi-Fermi potentials

This model is the isothermal simulation and suitable to be used for low-power density devices with long active regions. Under low-drain bias, it is sufficient to use the DD model. Several studies have been conducted to investigate the suitability of this model for a particular device where most of them require modification to improve the accuracy of the simulation (T. Grasser, Kosina, & Selberherr, 2003).

(b) ***Thermodynamic Transport***

For the thermodynamic model, equation 2.10 (a) and (b) are extended to include the temperature gradient as a driving term:

$$J_n = -nq\mu_n(\nabla\varphi_n + P_n\nabla T) \quad \text{(2.11 (a))}$$

$$J_p = -pq\mu_p(\nabla\varphi_p + P_p\nabla T) \quad \text{(2.11 (b))}$$

Where P_n and P_p are the absolute thermoelectric powers and T is the lattice temperature.

Thermodynamic model will solve the lattice temperature equation in addition to the Poisson equation and carrier continuity equations. It is suitable for a simulation with high current levels where considerable self-heating can occur, such as for power devices, MOSFET with high gate or drain voltage and open bipolar transistors.

(c) ***Hydrodynamic Transport***

The hydrodynamic transport model solves the carrier temperature and heat flow equations in addition to the Poisson equation and carrier continuity equations. The current densities are defined as:

$$J_n = q\mu_n(n\nabla E_C + kT_n\nabla_n - nkT_n\nabla ln\gamma_n + \lambda_n f_n^{td} kn\nabla T_n - 1.5nkT_n\nabla lnm_n) \quad \text{(2.12 a)}$$

$$J_p = q\mu_p(p\nabla E_C + kT_p\nabla_p - pkT_p\nabla ln\gamma_p + \lambda_p f_p^{td} kp\nabla T_p - 1.5pkT_p\nabla lpm_p) \quad \text{(2.12 b)}$$

In the first term of equation 2.12 a and b, the contribution due to the spatial variations of electrostatic potential, electron affinity and the band gap were considered. The remaining terms considered the involvement due to the gradient of concentration, the carrier temperature gradients and the spatial variation of the effective masses m_n and m_p.

This model is suitable for deep-submicron MOSFETs below 0.18 um generation and as the energy, transport across the heterointerfaces taken into account during simulation, hence it is suitable to be used in heterostructure devices for partially depleted floating-body SOI MOSFETs. The velocity overshoot problem which was not considered in the DD simulation is taken into account in this model. This model also avoids the onset premature breakdown due to the local field assumption in the DD model. Another benefit of this model is where the energy, transport across the heterointerfaces is taken into account during simulation, hence it is suitable to be used for heterostructure devices.

(d) ***Quantum transport (Quantization model)***

When the MOSFET is scaled towards the nanometer regime, some of the features such as oxide thickness and channel width reached the quantum mechanical length scales. With regards to this, the wave nature of electrons or holes must be taken into account in calculating the device characteristics. This model was used in simulating nano scale devices such as fully depleted SOIs, double-gate SOIs and FinFET structures as well as ultra-thin oxide devices. The shrink of device dimension to the order of nanometers allowed the confinement and tunneling to play a significant role. The effect of quantum confinement due to band to band, source to drain and gate tunneling can lead to the shifts of threshold voltage and increased leakage. This impact was significantly observed in the performance of nanowire transistors as a possible device replacement for technology beyond the 22 nm technology node.

There are four quantization models implemented in Sentaurus which differed based on physical sophistication, numeric expenses and robustness. The four quantization models consists of the Van Dort model, 1D Schrodinger model, density gradient (DG)

model and modified local-density approximation (MLDA) model. These quantization models solved the quantum potential equations self-consistently with the Poisson equation and carrier continuity equations.

(e) ***Monte carlo***

Monte Carlo (MC) simulation techniques is a common category of computational algorithm used in recurrent random sampling to model a physical or mathematical system. Following the MC procedure, the microscopic physics of individual carrier motions was tracked resulting in a physical accuracy. The DD method, on the other hand, is based on the average properties of the charge transport system. It is therefore able to yield more accurate result when MC was adopted as compared to DD. However, the MC technique involved larger computational overhead. This required extended simulation times due to the presence of statistical noise which was larger in the sub-threshold regime. Hence it is not efficient as a simulation method as the number of carriers and scattering events are low in the sub-threshold regime.

2.7.3.2 Mobility Models

Sentaurus TCAD simulator used a modular approach to describe the carrier's mobility. A constant mobility model was used for undoped material where the mobility is a function of the lattice temperature. There are five different models used in this simulator, which consists of Doping-dependent Mobility Degradation, Mobility Degradation at interfaces, Thin-layer Mobility, Carrier-carrier Scattering, Philips Unified Mobility Model and High-Field Saturation as shown in Figure 2.18.

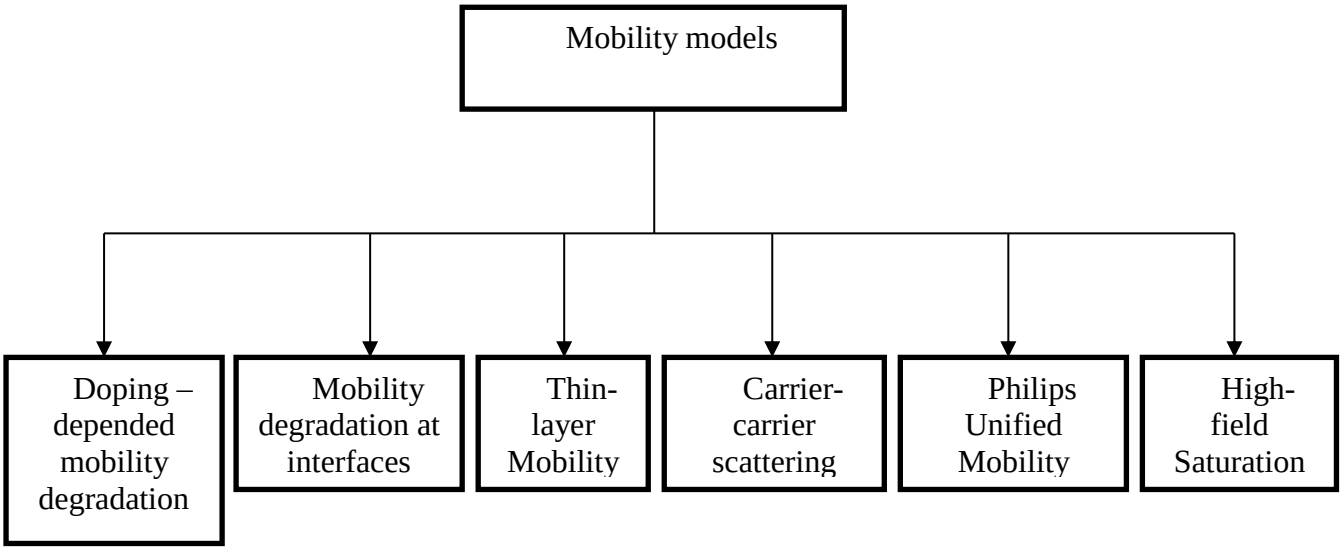


Figure 2.18 Mobility models ("Sentaurus Device User Guide," 2013)

The doping-dependent mobility degradation modeled the mobility degradation due to the scattering mechanisms because the carriers collided with the impurities. There are three different approaches in modeling the mobility degradation due to impurity scattering which are the Masseti, Aurora and University of Bologna models respectively. The mobility degradation at interfaces model describes the high transverse electric field that influences carriers to interact strongly with the semiconductor–insulator interface. The calculation of field perpendicular can be activated based on perpendicular to semiconductor-insulator interface or to current flow. Sentaurus provides four options for modeling the field perpendicular which are Enhanced Lombardi, Enhanced Lombardi with High-k Degradation, Inversion and Accumulation Layer Mobility and University of Bologna Surface Mobility.

Thin layer mobility can express the mobility of the carriers for devices with silicon layers that are only a few nanometers thick. The geometric quantization leads to a mobility that cannot be demonstrated by a normal field-dependent interface model as

it is influenced clearly by the layer's thickness. The effect of scattering of carrier-carrier was modeled using the Conwell-Weisskopf and Brooks-Herring model. To account for the effect of combination of majority and minority carrier bulk mobilities, Philips unified mobility model can be used. This model was capable of defining the temperature dependence mobility by taking into account the electron-hole scattering, screening of ionized impurities by charge carriers and clustering of impurities.

The carrier drift velocity was saturated and not proportional to the electric field during high electric fields. This is because the velocity saturates to a finite speed v_{sat}. To describe this effect, four models can be used namely, the Canali model, transferred electron model, basic model and Meinerzhagen-Engl model.

2.7.3.3 Generation – Recombination Models

Processes that exchange carriers between the conduction band and the valence band are called generation and recombination processes. The electrons and holes involved appear or disappear at the same location in each individual generation or recombination process. In this simulator, there are several generation and recombination models available such as the Shockley-Read-Hall Recombination (SRH) models, Surface SRH Recombination, Coupled Defect Level (CDL) Recombination, Auger Recombination, and the Band-to-Band Tunneling Models.

SRH was used to describe the recombination process through deep defect levels in the gap. The lifetimes for carriers were modeled based on doping-dependent, field-dependent and temperature-dependent. Due to strong electric field, the recombination lifetimes in regions of strong electric fields was reduced in the region of high electric fields. This led to the generation of electron-hole pair due to the defect-assisted tunneling process. Hence, two field-enhancement models can be used which are the

Schenk Trap-assisted Tunneling (TAT) model and Hurkx TAT model. Trap-assisted Auger (TAA) recombination model meanwhile is the modification of SRH recombination and Coupled Defect Level (CDL) model. For TAA, the lifetimes depended on carrier densities. The CDL is the steady state recombination rate for two coupled defect levels which generalizes the single-level SRH formula.

Another important generation and recombination model is the Band-to-Band Tunneling model. There are four band-to-band tunneling models which consist of the Schenk model, the Hurkx model, the simple Band-to-Band model and the nonlocal path model. Schenk model can describe the generation and recombination process due to the phonon-assisted band-to-band tunneling activity which occurs during high normal electric fields of MOS device. For Hurkx model, the tunneling carriers were modeled by an additional generation-recombination process. On the other hand, the simple Band-to-Band model predicts a nonzero generation rate at equilibrium.

2.7.3.4 Electrostatic Potential Model

Two types of charges available in semiconductor devices are mobile (electrons and holes) and immobile charges (ionized dopants or traps) which play significant roles. All the charges contribute to the electrostatic potential and their mechanism will be influenced by the electrostatic potential. Therefore, it is crucial to compute the electrostatic potential in every device simulation. When the device is in equilibrium, the electron and hole densities can be described by the constant quasi-Fermi potential. By introducing the electrostatic potential together with the relationship between quasi-Fermi potential and the electron and hole densities, the modest device simulation can be performed.

2.7.3.5 Mechanical Stress Effect Model

Sentaurus TCAD can model the mechanical stress effect in device simulation. One of the important technologies in advance device process is stress engineering technology. This technology can improve the performance of CMOS devices which can affect workfunction, band gap, effective mass, carrier mobility and leakage currents. The stress comes from many technological processes which under different process temperatures and material properties could alter the semiconductor microstructures. The mechanical distortion will change the band structure and also carrier mobility. The change in band structure was simulated based on the deformation potential theory while the change in carrier mobility was simulated based on stress-dependent mobility models.

The change in band structure can be described by the Deformation of Band Structure, the Strained Effective Masses and the Density-Of-States (DOS) and Multivalley Band Structure. For deformation of band structure, the strains are considered small with change in energy of each carrier sub-valley that is due to the deformation of lattice. This change is a linear function of the strain. The change in the energy band considers three band for electrons and two bands for holes. To separate the change of energy of each carrier for electrons and holes, a degenerate k.p theory can be used for electron bands while 6 x 6 k. p theory can be used for heavy-hole, light-hole and split-off bands. The k.p theory has been frequently used to model valence band of semiconductors and can be used to model the impact of strain on the conduction band. The degenerate k. p theory and 6 x 6 k. p theory are later be used to model the change of effective DOS mass for electrons and holes respectively for arbitrary strain in silicon.

The change of mobility due to stress was calculated in simulation based on several stress-dependent mobility models such as Stress-induced Electron Mobility Model, Intel Stress-induced Hole Mobility Model and Piezoresistance Mobility model. The mechanical stress in device structure resulted in anisotropic carrier mobility with essentials to be defined by a mobility tensor. The mobility of electron was changed because of the carrier redistribution between bands in silicon was an effect of lattice mismatch. On the other hand, the mobility of holes for strained PMOS was based on the occupancy of different part of the topmost valence band as suggested by INTEL ("Sentaurus Device User Guide," 2013).

2.7.3.6 Degradation Model

Sentaurus TCAD has three degradation models capable of simulating the time dependence of interface trap generation to predict the CMOS reliability. The models are trap degradation model, multistate configurations (MSC) - hydrogen transport degradation model and two-stage NBTI model.

The trap degradation model implemented in Sentaurus was based on the disorder-induced discrepancies among the Si-H activation energies at the passivated Si-SiO_2 interface believed to be the source of the sub-linear time reliance of the trap generation process. The time dependencies of trap generation ware explained based on the diffusion of hydrogen from the passivated Si-SiO_2 upon the application of stress. The discrepancies of the Si-H activation energies could also be due to the Si-H breaking on the electrical and chemical potential of hydrogen at the interface.

The MSC-Hydrogen transport degradation model can describe the charge-trapping, interactions between localized trapping centers and mobile carriers taking into account the interaction each process with mobile hydrogen. This model also

considered that the trapping centers could possibly have more than two internal states which rest on the structural relaxation and the existence of charges and hydrogen.

The two-stage NBTI degradation model describes the generation of positive oxide charges and interface traps in MOS structure under the influence of high negative bias at high stress temperature. The generation of positive oxide charges and interface traps led to the shift of threshold voltage and reduced the on-currents of PMOSFET. The two-stage NBTI model implemented in Sentaurus assumed that the degradation proceeded via a two-stage process consisting of generation of positively charge E'centers, the charging and discharging process of the positively charge E'centers and annealing process of positively charge E'centers to neutral oxygen vacancy precursors for the first stage and generation of poorly recoverable Pb centers for the second stage.

2.8 Summary

This chapter discussed the NBTI mechanism based on hydrogen and non-hydrogen transport formalism. Previous works have adopted the hydrogen transport formalism based on the R-D model while the non-hydrogen transport formalism could be possibly explained by the Two-stage NBTI model. The hydrogen transport formalism was explained based on the generation of the interface trap also known as a permanent component upon the application of stress. There were limited work that focused on the recoverable component within the context of hydrogen transport model in which the behavior would be different based on the underlying characteristics of R-D model.

With regards to the non-hydrogen transport formalism, unified defect characteristics have been identified which the mechanism of degradation relied on the pre-existing defect. The pre-existing defect can be known as oxygen vacancy or the

as-grown hole trap. With the application of stress bias, the hole was trapped in the pre-existing defect hence the generated defects created known as switching hole trap. This switching hole trap is also known as cyclic positive charges as it has energy distribution within the energy band gap. Hence, the importance of hole trapping effect in addition to the generation of interface traps should be taken into account in assessing the degradation of NBTI in p-MOSFET devices. As most of the previous work relied only on the interface trap contribution, the high-k device discussed in detail has shown several discrepancies in the degradation level with respects to the metal gate stack variation together with the high-k integration issues. Hence. the correlation between the hole trapping and interface trap generation should be evaluated carefully to provide meaningful information on the degradation level within the context of metal gate stack variation together with high-k integration issues.

To further carefully evaluate the NBTI degradation, the framework of positive charges which consist of the as-grown hole trap, cyclic positive charges and anti-neutralization positive charges, each of them have an energy distribution below, within and beyond energy band gap must be taken into account. As most of the experimental and modeling work only probed the charges below and within the energy band gap, there is a need to accurately model the NBTI degradation with charges that distributed beyond the energy band gap.

Prior to the NBTI characterization issues discussed here, the important issues highlighted in this thesis hence becomes the background of the project which is tabulated and presented in Table 2.1.

Table 2.1 Comparison of the NBTI mechanisms based on previous research works

NBTI Mechanism	Methodology	Static / Dynamic	Defect components			Reference
			Permanent	Recoverable	Precursor	
Hydrogen transport	Simulation based on R-D model	Static	Interface traps	X	Si-H	(Y. Zhang et al., 2013)(S. F. W. M. Hatta et al., 2010; Wan Muhamad Hatta et al., 2011)(Maiti, Mahato, Chakraborty, Maiti, & Sarkar, 2009)
Hydrogen transport	Simulation based on R-D model	Dynamic	Interface traps	X	Si-H	(D S Ang et al., 2011)

NBTI Mechanism	Methodology	Static / Dynamic	Defect components			Reference
			Permanent	Recoverable	Precursor	
Hydrogen transport	Conventional SMS experiment and Simulation based on R-D model	Static and dynamic	Interface traps	X	Si-H	(M. A. Alam, 2003; Chakravarthi et al., 2004)
Hydrogen and non-hydrogen transport	Conventional SMS experiment	Static and dynamic	Interface traps	Hole trapping/de-trapping	Si-H	(Huard & Denais, 2004)

NBTI Mechanism	Methodology	Static / Dynamic	Defect components			Reference
			Permanent	Recoverable	Precursor	
Hydrogen and non-hydrogen transport	OTF experiment and modeling based on R-D and hole trapping model	Static and dynamic	Interface traps	Hole trapping/de-trapping	Si-H	(Huard et al., 2006)
Hydrogen and non-hydrogen transport	OTF and UFM experiments R-D and elastic hole trapping/de-trapping model	Static	Interface traps	Hole trapping	Pre-existing defect	(Ahmad Ehteshamul Islam et al., 2007)

NBTI Mechanism	Methodology	Static / Dynamic	Defect components			Reference
			Permanent	Recoverable	Precursor	
Hydrogen and non-hydrogen transport	Theoretical framework based on R-D model and Shockley Read-Hall model	Dynamic	Interface traps	Hole trapping into generated oxide defect	Hole trapping into pre-existing oxide defect	(A. E. Islam, S. Mahapatra, S. Deora, V. D. Maheta, 2011)
Non-hydrogen transport	Two-stage NBTI with MPE mechanism using HDL model	Dynamic	Interface traps	E'center / Switching oxide trap	Oxygen vacancy precursors	(T. Grasser et al., 2009a, 2009b)

NBTI Mechanism	Methodology	Static / Dynamic	Defect components			Reference
			Permanent	Recoverable	Precursor	
Non-hydrogen transport	Two-stage NBTI model with MPE and MPFAT mechanism using HDL model	Dynamic	Interface traps	E'center / Switching oxide trap	Oxygen vacancy precursors	(T. Grasser et al., 2009a, 2009b)
Non-hydrogen transport	Two-stage NBTI model with quantization effect	Dynamic	Interface traps	E'center / Switching oxide trap	Oxygen vacancy precursors	(Goes, Grasser, Karner, & Kaczer, 2009)

NBTI Mechanism	Methodology	Static / Dynamic	Defect components			Reference
			Permanent	Recoverable	Precursor	
Non-hydrogen transport	SMS experiment with different hydrogen content devices	Dynamic	Interface traps	E'centers	Oxygen vacancy precursors	(Aichinger, Puchner, Nelhiebel, Grasser, & Hutter, 2010)
Non-hydrogen transport	DC Id-Vg, sub-threshold swing and CP methods	DC, Dynamic	Interface traps below Ei	Deep level positive traps near and above Ec	Trap precursor	(D S Ang et al., 2008; D.S. Ang & Wang, 2006; D.S. Ang et al., 2009)

NBTI Mechanism	Methodology	Static / Dynamic	Defect components			Reference
			Permanent	Recoverable	Precursor	
Non-hydrogen transport	Id-Vg fast pulse measurement	Dynamic	Interface traps	Switching hole trap	Oxygen vacancy precursor	(Boo et al., 2012; Boo & Ang, 2012; Du et al., 2009; Gao, Ang, et al., 2011; Gao, Boo, et al., 2011; Z. Q. Teo et al., 2009, 2011; Zhi Qiang Teo et al., 2010)

NBTI Mechanism	Methodology	Static / Dynamic	Defect components			Reference
			Permanent	Recoverable	Precursor	
Non-hydrogen transport	SHI & FNI	Dynamic	ANHT	CPC	AHT	(Jian F Zhang et al., 2004; Ce Z Zhao et al., 2004; Zhao, C. Z., & Zhang, 2005)
Non-hydrogen transport	Pulsed Id-Vg measurement and DC Id-Vg, SHI & FNI	DC, Dynamic	ANHT	CPC	AHT	(Ce Z. Zhao et al., 2008)
Non-hydrogen transport	Pulsed Id-Vg measurement	Dynamic	ANHT above Ev	CPC within energy band gap	AHT below Ev	(S. W. M. Hatta et al., 2013, 2014)

NBTI Mechanism	Methodology	Static / Dynamic	Defect components			Reference
			Permanent	Recoverable	Precursor	
Hydrogen transport model	RD model simulation on varied geometrical of high-k devices	Static	Interface traps	-	Si-H	(S. F. W. M. Hatta et al., 2010; Wan Muhamad Hatta et al., 2011)

CHAPTER 3: **METHODOLOGY**

3.1 Introduction

In this chapter, the simulation tools for developing simulation frameworks to characterize NBTI-induced defect components based on the perspective of hydrogen and non-hydrogen transport formalism are highlighted. The development of the simulation framework in the perspective of hydrogen transport formalism was implemented using the Modeling Interface-defect Generation (MIG) software. For the purpose of developing a simulation framework in the perspective of non-hydrogen transport formalism, the Synopsys' Sentaurus TCAD tool was used. The features and validation of the MIG simulation tool is highlighted as well as its limitations. Then, the simulation techniques employed in the Sentaurus TCAD tool for the purpose of NBTI study are discussed together with an explanation of the test bed devices selected for simulation. The simulation techniques engaged in this work were emphasized within the context of the requirement and suitability to the aims of this study. The overview of the overall methodology implemented in this research is highlighted in Figure 3.1.

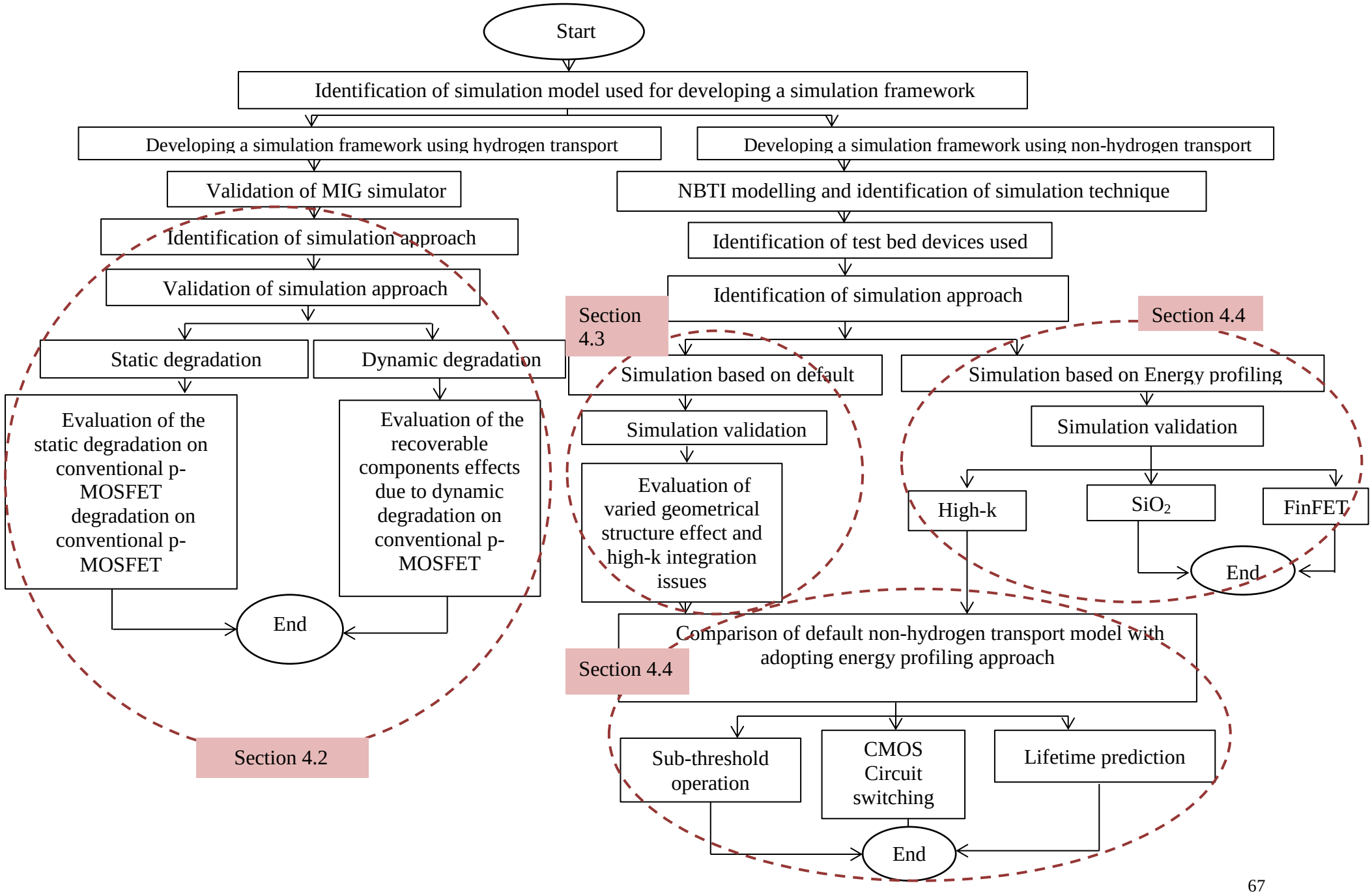


Figure 3.1 Schematic diagram of project flow chart used in this research

3.2 Modeling Interface-defect Generation (MIG) simulator

A key objective of the study based on hydrogen transport formalism is to demonstrate the threshold voltage shift under static and dynamic simulation approaches. These static and dynamic simulation approaches were based on the creation of interface traps due to the passivation of Si-H bond at the interface during NBTI stress. The static simulation approach was used as to verify the accuracy of this software upon implementation in this research work under different stress conditions and hydrogen species. The accuracy of the simulation result is then benchmarked against experimental work by ensuring the time exponent, n ~ 0.16 or 0.25 for molecular or atomic hydrogen respectively (M.A. Alam & Mahapatra, 2005). Upon validating the R-D model in the MIG simulator, the static simulation was used to understand the device processes dependence effects on NBTI degradation. The dynamic simulation approach is then used as to understand the recovery effects under the R-D model point of view. The evolution of recoverable component was demonstrated to study the recovery effects for dynamic simulation approach (D S Ang et al., 2011; Boo et al., 2012; Boo & Ang, 2012; Gao, Ang, et al., 2011; Gao, Boo, et al., 2011).

3.2.1 Features of MIG simulator

Two important features of MIG are the flexibility in inserting the desired PMOS parameter and specifying the NBTI model options. The PMOS parameter feature enables the user to set the parameter for device under test to be used in the simulation. The parameters that can be changed accordingly are the flatband voltage, Effective Oxide Thickness (EOT), substrate doping, poly doping and ambient temperature. In NBTI model options, the diffusion species types, simulation method, stress voltage and time duration, temperature dependence model parameter and forward dissociation

model parameter can be chosen for the simulation based on the specific requirement shown in Table 3.1.

Table 3.1 Model options as available in MIG tool (A. E. Islam, 2010, 2014)

Model	Options
Diffusion species types	Atomic hydrogen, molecular hydrogen
Simulation analysis	DC, AC, Pulse
Temperature dependence	Arrhenius Diffusion
Forward dissociation model	a. Purdue b. Exponential c. Power law

The diffusion species types that can be used are atomic hydrogen and molecular hydrogen, which results in a timely exponent of ~0.16 to 0.25. For the simulation method, options available include DC, AC and pulse simulation. In this work, the DC simulation analysis was used to investigate the static NBTI effect on different stress conditions while pulse simulation was used to investigate the recoverable component behavior. To ensure the validity of this simulation tool, a simulation validation framework was developed and discussed in the next section.

3.2.2 Validation of MIG simulation tool

The device used in this simulation validation is p-MOSFET with EOT 1 nm since NBTI degradation was found to be an important reliability concern for technology nodes with EOT less than 2nm (Brisbin & Chaparala, 2008; S. Mahapatra et al., 2005; Schroder, 2007). The substrate doping level n-type silicon was fixed to 3e-17cm^{-3} and

gate doping level p+ poly silicon type was fixed at 1e20cm^{-3} for the degenerated semiconductor. The forward dissociation model used in this simulation was based on the model developed by (S. Mahapatra et al., 2005) [1]. This forward dissociation model explains why NBTI degradation is field oxide dependent as shown in

$$K_f = AE_C \exp(B\, E_{ox}) \tag{3.1}$$

where E_C is Semiconductor surface electric field due to mobile carriers and E_{ox} is Oxide electric field. Arrhenius model,

$$D = D_0 \text{ x } \exp\,(E_A/kT) \tag{3.2}$$

explained that NBTI degradation is temperature dependent [1]. The diffusion prefactor, D_0 is 3 x 10^{-8} while the activation energy, E_A used in this simulation is 0.5 eV which both are default value in MIG. Based on literature, the E_A value is based on Arrhenius law which typically ~ 0.6 eV. This E_A value is determined from a range of temperature applied for accelerated test and safely extrapolated to operating conditions (Jacopo Franco, Kaczer, & Groeseneken, 2014).

To systematically validate the simulation work using MIG simulator, the simulation setting was used as shown in Table 3.2. The diffusion species used were the atomic hydrogen and molecular hydrogen based on the generation and recovery of interface trap as explained by the R-D model (S Mahapatra et al., 2013). The measurement delay specified in the table was based on the different experimental techniques where the measurement delay varies (Denais et al., 2004; Kumar et al., 2007; Souvik Mahapatra & Alam, 2008; Maheta et al., 2008; W. J. Liu, Z. Y. Liu, Daming Huang, C. C. Liao, L. F. Zhang, 2007; Yang & Liu, 2008). Stress temperatures and voltages applied within the range of NBTI experimental condition

as widely used in previous works (S. Mahapatra et al., 2005; Souvik Mahapatra & Alam, 2008; Z. Q. Teo et al., 2011).

Table 3.2 Simulation setting for validation based on different stress conditions

a) Effect of hydrogen species H and H_2

Parameter	Values
Measurement delay	0 s
Stress temperature	100^0C
Stress voltage	-1.25V

b) Effect of measurement delay

Parameter	Values
Hydrogen species	H_2
Stress temperature	100^0C
Stress voltage	-1.25V

c) Effect of stress temperature

Parameter	Values
Hydrogen species	H_2
Measurement delay	0 s
Stress voltage	-1.25V

d) Effect of stress voltage

Parameter	Values
Hydrogen species	H_2
Measurement delay	0 s
Stress temperature	100^0C

The threshold voltage shift resulting from the simulation conditions as shown in Table 3.2. The simulation results were validated based on the time exponent, n ~ 0.16 and n ~ 0.25 for molecular and atomic hydrogen respectively. The time exponent, n referred to the analytical solution of the R-D model which indicates the diffusing species (Chakravarthi et al., 2004). The neutral hydrogen atom was released upon the application of bias, represented by the relationship $SiH + h^+ \leftrightarrow Si^+ + H^0$. The molecular hydrogen formation is explained based on the neutral hydrogen, H^0 that is formed which can react with the SiH bond and form another dangling bond $SiH + H^0 + h^+ \leftrightarrow Si^+ + H_2{}^0$.

The resulting threshold voltage shift based on different hydrogen species is shown in Figure 3.2 (a). Time exponent, n ~ 0.16 and n ~ 0.25 are expected for molecular and atomic hydrogen species. The R-squared value was obtained to verify the goodness of fit for the power law extrapolation. The R-squared value obtained is within the range of 0.9 to 1 which confirm that the time exponent, n extrapolation fit almost the data. As variable delay time, stress temperatures and voltages were simulated using molecular hydrogen species, the n obtained was 0.171 which is approximately 0.16 as expected and hence confirmed that this simulator was capable of giving simulation result within the framework of hydrogen formalism demonstrated by the R-D model (Souvik Mahapatra & Alam, 2008). Closer observation on the values of the n in Figure 3.2 (b) – (c) indicated that the n increased for longer measurement delays (Rangan, Mielke, & Yeh, 2003) and at higher stress temperatures (S Mahapatra et al., 2013). The time exponent, n however, had independence of stress voltages which reflected the diffusion-limited phase as the hydrogen species correlated with the concentration gradient but did not correlate to the electric field.

Hence the time exponent was not affected with different stress voltages in this diffusion-limited phase (Souvik Mahapatra & Alam, 2008).

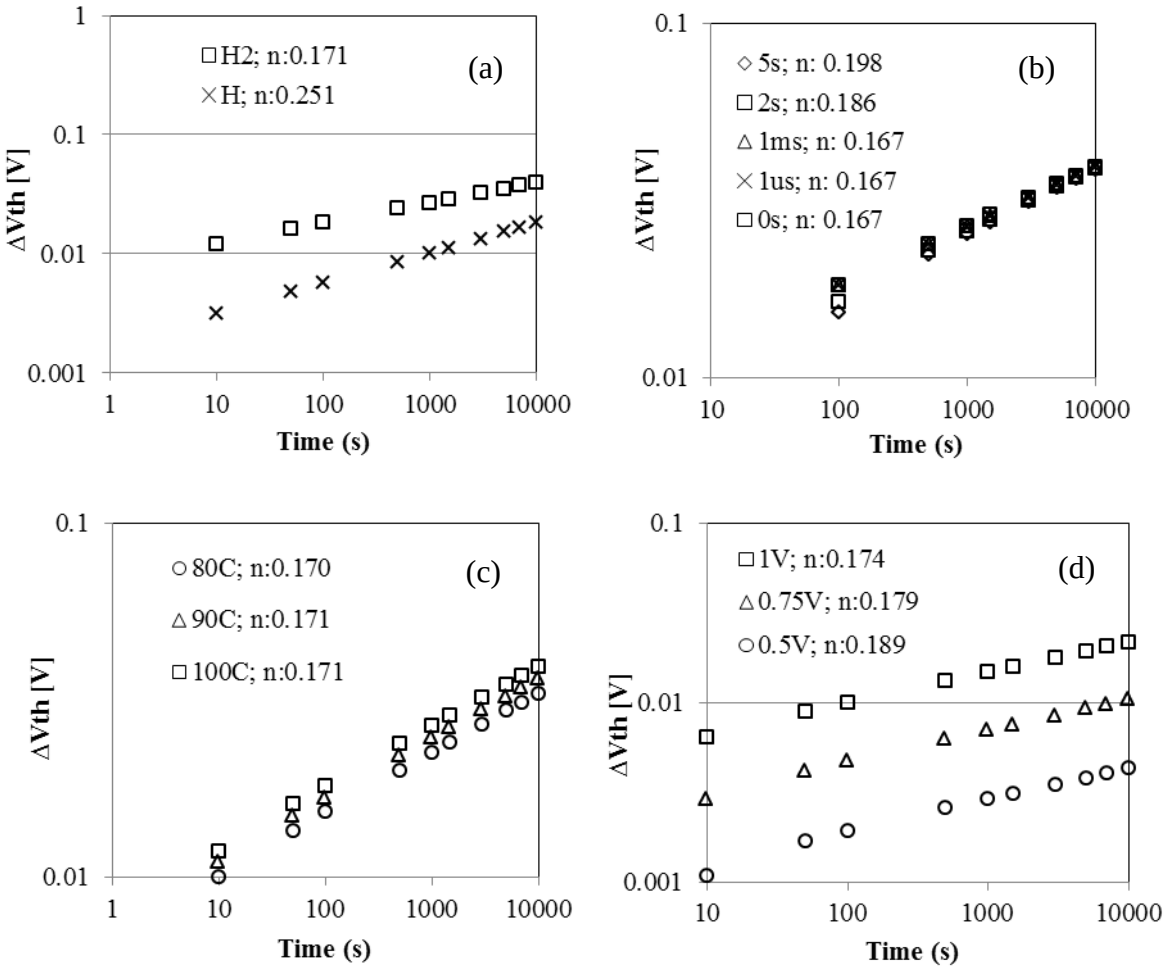


Figure 3.2 Resulting threshold voltage shift, ΔVth based on simulation settings for varying (a) hydrogen species, molecular hydrogen H_2 and atomic hydrogen, H (b) measurement delays (c) stress temperatures (d) stress voltages

3.2.3 Limitations of MIG Simulator

As discussed in the previous section, the aim of hydrogen transport formalism based study is to investigate the dependence of device process and evolution of recoverable component using static and dynamic simulation respectively. The process dependence only included the effects of varying effective oxide thickness (EOT)

which was based on the conventional SiO_2 dielectric. The calculation of NBTI degradation effect is based on the R-D model within the limited input parameters without the semiconductor physical device model. The behaviour of recoverable component extracted in the dynamic simulation approach can be related to oxygen vacancy defect and will be further elaborated in Chapter 4.

Undoubtedly, this method of characterizing the hydrogen transport formalism based on static and dynamic simulation approach presented a distinct level on degradation mechanism as observed recently in most NBTI populist where most experimental work were based on the fast measurement approach in order to reduce recovery effects (D S Ang et al., 2011; J.F. Zhang, 2009; Ce Z. Zhao et al., 2008). These works are however necessary to provide an insight on the specific study of recoverable component characteristics in determining the behaviour of the degradation mechanism within the framework of the R-D model. This is because the R-D model is still a valid approach which can accurately capture the NBTI degradation effect found in most experimental studies especially in conventional stress-measure-stress experimental setup (M.A. Alam & Mahapatra, 2005; S. Mahapatra et al., 2005). This was proven to the adopted static and dynamic method utilised in the MIG simulator which implements the R-D model mechanism and has been recognized as a suitable engineering approach among the NBTI populists. The results obtained from the MIG simulator can be well verified with experimental measurements, of which the experimental data was capable of replicating quantitative simulation data of the degradation together with the understanding on the relationship between the R-D model and hole trapping mechanism. The result of these static and dynamic simulation methods have since been published in reputable well-ranked journals (H. Hussin, N. Soin, Hussin, Soin, Karim, & Muhamad, 2012; H. Hussin, N.

Soin, M. F. Bukhori, 2014) and presented at important semiconductor electronic conferences (Hussin & Soin, 2011).

With regards to the research objective which is to develop an understanding on NBTI degradation within the framework of non-hydrogen transport formalism through a simulation based study, this MIG simulator cannot capture the degradation mechanism because of the pre-existing and generated oxide defect based on fast measurement experimental setups (D S Ang et al., 2011; J.F. Zhang, 2009; Ce Z. Zhao et al., 2008). Hence, the need to further understand the pre-existing and generated oxide defect responsible for NBTI degradation provided the motivation to implement a Two-Stage NBTI model in this research using different tools. This type of oxide defects are known also as non-hydrogen transport formalism which will be further investigated as part of this research work (Zhi Qiang Teo et al., 2010). As R-D model is the core of MIG implementation, this research was further enhanced through the NBTI degradation study using a Two-Stage NBTI model as implemented in the TCAD Sentaurus tool. By using Sentaurus TCAD tool, the semiconductor device simulation is based on the underlying physical methods and models as discussed in Section 2.7.3. The details on the method employed in the simulation for NBTI characterization of advanced semiconductor devices consist of high-k and FinFET devices will be highlighted in the next section.

3.3 Sentaurus TCAD simulator

The main objective in implementing this research work based on non-hydrogen transport formalism is to study the impacts of NBTI degradation based on the Two-stage NBTI model by analyzing the behavior of trapped charges consisting of pre-existing defects and generated oxide defects in an advanced CMOS fabrication

process. It is therefore necessary that the actual simulation technique engaged could appropriately resolve the stress conditions applied to the test bed devices used in this study in order to produce accurate simulation results. The adopted simulation technique should accurately represent the physical characteristics of advanced process of the test bed devices.

The next requisite here ascended out of the nature of traps known to be essential physical measures that can severely disturb the electrical performance of a device. The nature of these traps is that they can correspondingly turn to doping and contributing free carriers. This in turn can enhance the recombination process and lead to increased leakage. When these traps are charged, the number of total charges will increase, hence influencing the device electrical behavior. Since these properties are examined in this thesis for particular device designs rather than using the results to improve those designs, a specific simulation technique should be chosen so that it can accurately reflect the physics of both the oxide and the interface trap formation process. In addition to the trap formation process, the simulation technique should enable the trap distribution or occupation to be calculated and plotted. The carrier quasi-Fermi level location inside a material band gap was changed based on the trap energy distribution, doping and also bias conditions. It is therefore important to understand the trap distribution or occupation controlled by the trap energy distribution, doping and bias conditions. Hence, the trap spatial location within a specified material at which a trap distribution or occupation to be plotted must be determined.

To demonstrate the charge-trapping/de-trapping process in this research, the selected simulation technique should be able to accurately capture the important

physical effects within both the sub and super-threshold regime of the device operation. This is due to the trapping/de-trapping process of this study which can significantly shift the threshold voltage shift. Hence it is necessary for the simulation technique employed to accurately capture the important physical effects within. The simulation technique used which is precise and appropriate when applied to a certain mode of transistor operation may be imprecise in terms of capturing essential physical details when applied at dissimilar bias conditions because of the underlying assumptions of its physical model. Thus, the ability to accurately simulate the device in the sub and super-threshold regime is the third of the main requirements for selecting the simulation technique to be used in this work.

3.3.1 Modeling the NBTI effect

In this section, the general review on each of the simulation techniques available in the Sentaurus TCAD tool highlighted in Section 2.7.3 is concluded with a summary of their comparative precision and computational cost based on technology of test bed devices under study.

For the 32 nm technology high-k metal gate devices, both drift diffusion and hydrodynamic models were used in the simulation which solved the Poisson equation and carrier continuity equations for 2D simulation involved in high-k devices. The drift diffusion model was activated for the entire region, while the hydrodynamic model was only activated in the silicon region. The models were used selectively according to the region to ensure the convergence in the simulation is achieved. In addition to that, the hydrodynamic transport was restricted to only one type of carrier for a particular device. This helps to increase the simulation speed that guaranteed the accuracy. With regards to the 3D simulation which involved the FINFET structure,

the carrier transport model used is the drift diffusion while density gradient was used in the simulation which was self-consistently with the Poisson equation and carrier continuity equations.

The application of the hydrodynamic transport model can better capture the effects of carrier heating in the largely-varying electric fields inside a sub-micron device subjected to the extreme conditions of NBTI stresses as compared to the relatively simpler drift-diffusion simulation model. This yielded more physically-accurate simulation results as shown in Figure 3.3 which compares the degradation computed by the hydrodynamic transport model and drift-diffusion. It can be seen from the figure that the drift-diffusion model underestimated the NBTI-induced ΔVth by as much as 12% where this underestimation seems to be growing with extended stress time.

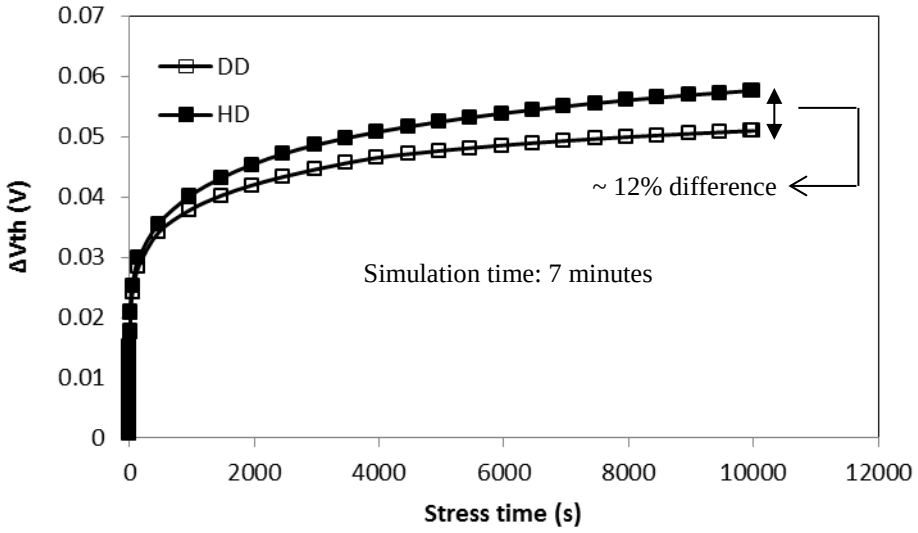


Figure 3.3 Comparison of NBTI-induced threshold voltage shift computed by hydrodynamic (HD) transport model and drift diffusion (DD) model. The DD model underestimates the degradation particularly at extended stress time.

The application of DD model was based on the derivation of simplifying the assumptions in the BTE. This simplification limits the validity of this model. It is hence important to ensure the validity of this model by empirically extended using the mobility models for the channel carriers with doping and electric dependencies (Shapiro, 1967). In ultra-small devices, the quantum correction was incorporated to model the quantum confinement effects (Tiersten, 1987). These refinements made the DD approximation valid only for devices which experienced slowly varying electric field based on the assumption that the carriers are able to respond instantly to variation in the field. Meanwhile, for short channel length devices, the lateral field varies rapidly as the carriers need a finite time and space to react to the field. Therefore, the carrier velocity overshoots the saturation velocity resulting in current increase. The carriers experienced ballistic transport which increases the driving current by 10% (Bude, 2000). To overcome this problem, the hydrodynamic model found to be capable of reaching the predefined value of vsat, 1×10^7 cm/s as compared to only DD model (Woo-Sung Choi, Fariborz Assaderaghi, Young-June Park, Hong-Shick Min, Chenming Hu, 1995) was included. Hydrodynamic model can account for the nonlocal transport effect influenced by the steep increase channel electric field near the source that contributed to the velocity difference near the source (Woo-Sung Choi, Fariborz Assaderaghi, Young-June Park, Hong-Shick Min, Chenming Hu, 1995). Another possible model to account for the ballistic transport phenomenon is the Monte Carlo model. As a comparison between rationality of DD model and Monte Carlo, the DD method can model transistor's on current of gate length down to 40 nm with less than 10% difference from the more precise and computationally costly Monte Carlo simulations (Granzner et al., 2006). To account for the quantization effect in 3D FinFET device simulation, the DD model was solved

self-consistently with density gradient (DG) quantum correction with auto-orientation ("Three-dimensional Simulation of 14/16 nm FinFETs with Round Fin Corners and Tapered Fin Shape," 2013). The simulated 3D FinFET has different crystal orientation for the top and side surfaces. These different crystal orientations have different quantization masses. As the quantum separation is a function of the quantization carrier mass, the auto-orientation basis was incorporated to deliberate orientation-dependent quantum correction. By considering the quantum effects for holes near silicon-oxide interfaces for PMOSFET, a hole quantization model based on Modified Local – Density Approximation (MLDA) was adapted to account for arbitrary bands (Ma, 2009). The combination of six-band k. p model and MLDA allowed the modeling of carrier confinement for holes in varied surface orientation and stress conditions. In the Sentaurus simulation process, the surface integration in k-space for inclusion of hole band DOS of the extended MLDA model is computationally costly. To prevent an increase in time consuming during and before simulation, Sentaurus computes the DOS only once and tabulates it for individually mesh point on a predefined energy mesh while numeric quadrature was used for computing total hole density.

Together with the hydrodynamic model, the DD model was extended with the mobility model to further validate the NBTI effect modeling. This work used Philips Unified Mobility, High-Field Saturation and E-normal (Enhanced Lombardi Model with High-k Degradation) while for 3D FinFET simulation, the Thin Layer Mobility model was included. The combination of low field mobility models is defined by the Matthiessen's Rule:

$$\frac{1}{\mu_{low}} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + \cdots \tag{3.3}$$

As the high-field saturation model was activated, the final mobility was computed in two steps where the first step is expressed in Eq. 3.5 and the final step will be computed as a function of a driving force F_{hs}:

$$\mu = f(\mu_{low}, F_{hfs}) \tag{3.4}$$

Philips Unified Mobility model unifies the description of the majority and minority carrier bulk mobilities. This model also describes the temperature dependence of the mobility, electron-hole scattering, screening of ionized impurities by charge carriers and clustering of impurities as well. During high electric fields, the carrier drift velocity is no longer proportional to the electric field, but the velocity saturates to a finite speed, v_{sat}. The Canali Model for the actual mobility model was chosen as it is suitable for all carrier transport models. The Canali Model is based on the Caughey-Thomas formula capable of modeling the carrier mobility during high electric fields. The Enhanced Lombardi Model with High-k Degradation is one of the model types in mobility degradation at interfaces. This model was adopted in this simulation as the test bed devices under test as the high-k based device. The mobility degradation at the interface is important in the channel region of MOSFET where the high transverse electric field forces carriers to interact strongly with the semiconductor-insulator interface. The carriers will be scattered due to the acoustic surface phonons and surface roughness. In high-k based devices, two possible contributors are remote Coulomb scattering (RCS) and remote phonon scattering (RPS). The mobility model further empirically extended for 3D FinFET device by incorporating the Thin Layer mobility model to ensure that the modulation of low field mobility due to the quantum-mechanical confinement effect is taken into account as the fin width become thinner than approximately 10 nm (Uchida, Koga, Ohba, Numata, & Takagi, 2001).

The difference of crystal orientation for top and side surfaces of FinFET need to be considered as the carriers are flowing in both surfaces during the on-state. Since the inversion layer mobility relied on the surface orientation, inversion and accumulation layer mobility (IALMob) was further included in the simulation to describe the 2D Coulomb scattering in the high channel doping region ("Three-dimensional Simulation of 14/16 nm FinFETs with Round Fin Corners and Tapered Fin Shape," 2013). The Coulomb interaction both in 2D and 3D simulation is perceived to be an important scattering mechanism due to the large occupancy of traps at high stress regime. During the high stress regime, traps state which is available will be filled. This caused a transformation of conduction charge in the inversion layer. Hence, the Coulomb scattering of mobile charges increased. The Coulomb interaction is depth dependent as mobile charges are more scattered in the inversion layer as compared to charges that are far from the interface (Maiti et al., 2009).

The generation and recombination simulation process adopted the SRH model by calculating the lifetime of the carriers based on doping-dependent model. The doping-dependent of the SRH lifetimes is based on Scharfetter relation where it accomplished the solubility of ultimate, acceptor-type defect which is powerfully interrelated to the doping density. The Hurkx band-to-band tunneling model was incorporated in addition to SRH based on the doping-dependent model in the 3D FinFET simulation. Hurkx band-to-band tunneling model described the leakage mechanism in FinFET structure as the structure tightens the gate control but the gate-induced drain leakage GIDL in the off-state increased ("Three-dimensional Simulation of 14/16 nm FinFETs with Round Fin Corners and Tapered Fin Shape," 2013).

The dipole interface model which defined the material interfaces between Hf-based and oxide dielectric was used to model the dipole layers of immobile charges that can occur hence producing a potential jump across the interface. In principle, in the bi-layer structure consisting of two dielectric materials with different conductivities, the charge trapping at the interface occurs as predicted in electromagnetic characteristics. The implementation of dipole model in Sentaurus TCAD tool is to account for the mobility degradation due to the charges at multiple arbitrary interfaces. The gate dielectric consisting of high-k HfO_2 layer and SiO_2 layer created dipole layer in between due to the areal difference of oxygen atoms at the interface. The creation of dipole layer led to the threshold voltage shift and channel mobility degradation (Kita & Toriumi, 2009). The dipole layer formation strongly depended on the applied voltage and other charges between the gate and substrate, including ionized donors and acceptors. Considering the existence of defects at the interface, inclusion of this dipole layer is important to determine the total contribution of defects generated during stress together with the influence of dipole layer in NBTI degradation.

The mechanical stress effect for 2D simulation on high-k based device used the deformation band structure model. This model was utilized by considering three bands for electrons applied to three two-fold bands in the conduction band and two bands for hole applied to heavy-hole and light-hole bands in the valence band. This model provided the change in energy of each carrier subvalley because the deformation of the lattice is a linear function of the strain. To describe the effect of mechanical stress which changes the carrier mobility due to the anisotropic carrier mobility, a mobility tensor is needed. Hence, the model which accounts for the mobility changes due to the carrier redistribution between bands in silicon was used. The relationship between the traps state available becomes filled with the mobility

degradation due to the Coulomb scattering effect and explained previously. Here, the contribution of strained effect based on Intel Stress-induced Hole Mobility Model was incorporated to model the trap occupation during stress and recovery of NBTI. The hole mobility change was calculated by considering the Boltzmann statistic and doping dependency was activated which assumed the charge neutrality between carrier and doping.

The formation of quantum well inside substrate led to the necessity to include quantum mechanical effect in the multi-layer high-k SiGe PMOSFET simulation (Hehenberger et al., 2011). Hence the calculation for subbands contribution is important to take into account the increase of hole concentration as the maxima of the subbands wavefunction move towards the interface when the recovery is switched to stress regime as demonstrated in (Hehenberger et al., 2011). This is because each subband calculates their transition rates which govern the occupation of the individual defects at certain stress or relaxation times. As compared to the simulation without the inclusion of this quantum mechanical effect, all holes were assumed to be energetically placed at the valence band edge of the substrate. In Sentaurus, the physics-based of six-band MLDA DOS was used for stress-induced inversion–layer mobility gain in 3D FinFET simulation. The accuracy for certain orientations was optimized in the carrier scattering model which accounts for intra and inter valley phonon scattering. The total hole mobility tensor can be applied for both bulk and inversion layers by accounting the six-band hole structure. This model can describe the contribution of subbands by computing the six-band MLDA DOS for each band and mobility ratio thus correcting the relaxed current density. This model works for both bulk and inversion layer and the activation of the model with doping-dependent

quasi-Fermi energy which can be applied to both the density and the inversion layer stress-induced mobility model.

The NBTI degradation is time-dependence and a complicated process as discussed in Chapter 2. In this work, a two-stage NBTI model to study the effect of NBTI in three different technology p-MOSFET devices was used. This model can describe the mechanism of NBTI degradation from both E'centers and interface trap kinetics point of view. The two-stage NBTI model was used to analyse the effect of NBTI on different geometrical structure which will be discussed in detail in the next section. The two-stage NBTI model will further be used to evaluate the effect on high-k integration issues on NBTI degradation. Previous studies based on these two cases were mainly on contribution of interface trap towards NBTI degradation (S. F. W. M. Hatta et al., 2010; S. W. M. Hatta, Abdul Hadi, & Soin, 2011). The implementation of simulation study based on energy profiling technique will be developed by adopting this two-stage NBTI model. The positive charges contributed consisting of precursor, positively charged E'centers and E'center/Pb H complex will be defined as as-grown hole trap (AHT), cyclic positive charges (CPC) and anti-neutralization positive charges (ANPC) with each energy profile similar to has been experimentally observed as published in (S. W. M. Hatta et al., 2013). The understanding of kinetic details of the degradation process using the new redefined energy levels for each two-stage NBTI component was developed and verified based on the trap concentration and trap density extracted under different stress conditions for a different test bed devices.

3.3.2 Test bed device

Three template devices from Sentaurus TCAD tool were considered in this study. The devices are advanced-process 32 nm high-k PMOS device, strained and without strained PMOS devices and the 3D p-channel FinFET device. Brief explanations on each of the test bed devices are highlighted in the following sub - section.

3.3.2.1 Advanced-process 32-nm high-k PMOS device

The testbed PMOSFET devices with high-*k*/SiO_2 gate stacks simulated in this study were based on the foundry-standard 32-nm CMOS process. The fabrication process incorporated shallow trench isolation, deposition of high-*k* dielectrics with metal gate, stress engineering using epi-SiGe pockets, silicidation, and dual-stress liner (S. F. W. M. Hatta et al., 2010; Yasutake et al., 2006). The device fabrication process flow in this simulation is presented in

Figure 3.4. This simulation process, which is based on the gate-first scheme, was adopted to overcome the process-related problems (such as ultra-shallow junction formation), suppress the leakage current, and improve the on-and-off state drain current. Incorporating the laser annealing process can help to suppress transient-enhanced diffusion.

To experimentally validate the testbed device, the electrical characteristics of IdVg obtained using this process flow was compared with experimental data in (Yasutake et al., 2006) and shown in Figure 3.5. The main performance characteristics based on this study are compared in Table 3.3. Given the information shown this table, it can be concluded that the process flow for the testbed devices used in this work was approximately within the range of the characteristics of the device fabricated by (Yasutake et al., 2006). The validation of testbed device method is similar to other

simulation work which confirms that the Id-Vg simulation results matched the experimental data (Bukhori, 2011). This is to ensure that the impact of NBTI degradation in this study is realistically assessed. The cross section with dimension of the simulated devices of based on high-k metal gates are shown in Figure 3.6 and Figure 3.7 which was used in the simulation framework implemented using Two-stage NBTI model and energy profiling technique respectively.

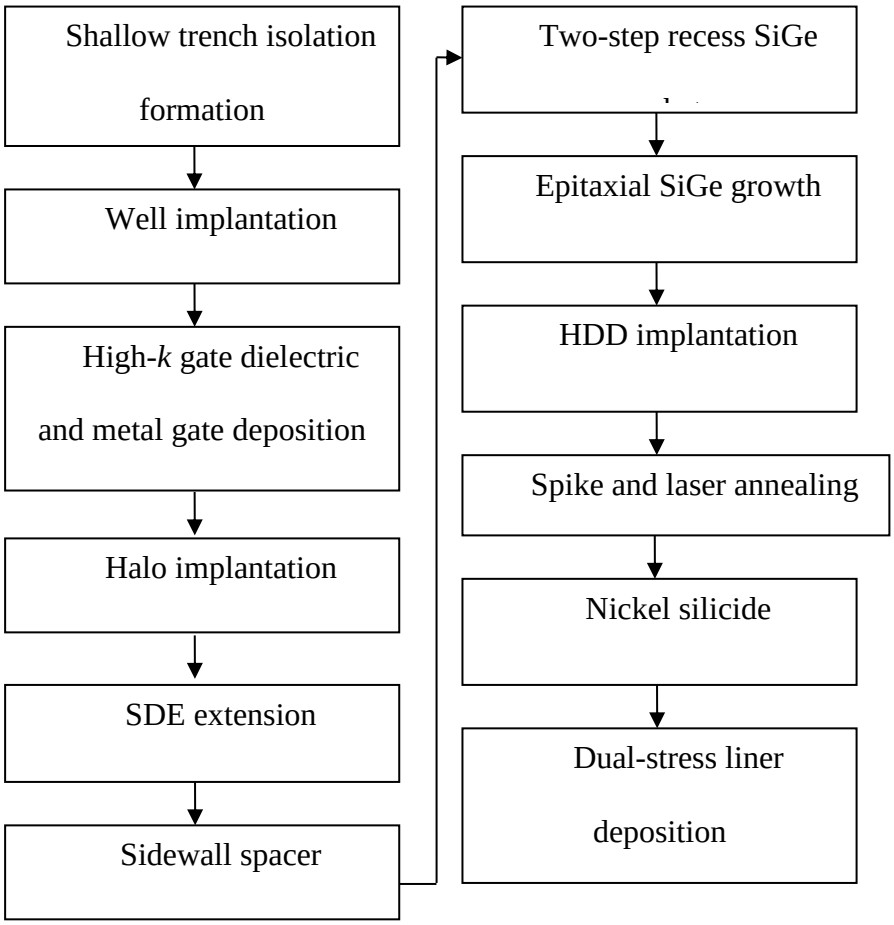


Figure 3.4 Process flow of the simulated advanced-process 32 nm high-*k* PMOS transistor ("Sentaurus Technology Template : 32-nm Gate-First Flow and CMOS Processing," 2011)

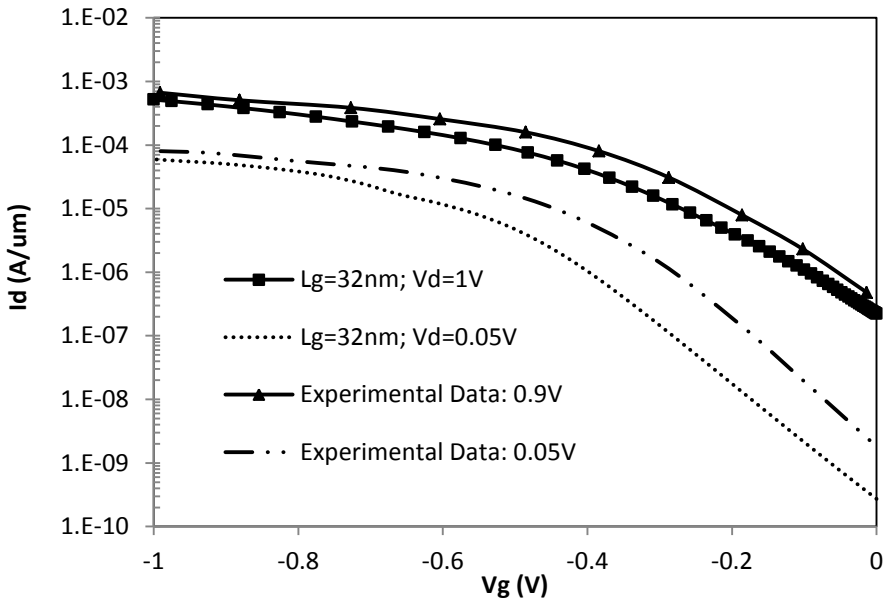


Figure 3.5 Comparison Id-Vg characteristics between simulation and experimental data in (Yasutake et al., 2006)

Table 3.3 Performance summary of simulated devices

	This work (Lg = 32 nm)	(Yasutake et al., 2006) (Lg = 24 nm)
Vdd (V)	1	0.9
Ion (A/um)	5.16×10^{-4}	5.25×10^{-4}
Ioff (A/um)	2.22×10^{-7}	3.70×10^{-7}

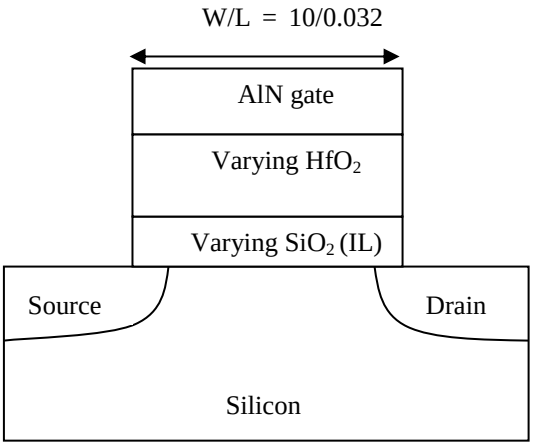


Figure 3.6 Cross section of test bed devices used for studying the effect of geometrical variation based on two-stage model (S. F. W. M. Hatta et al., 2010)

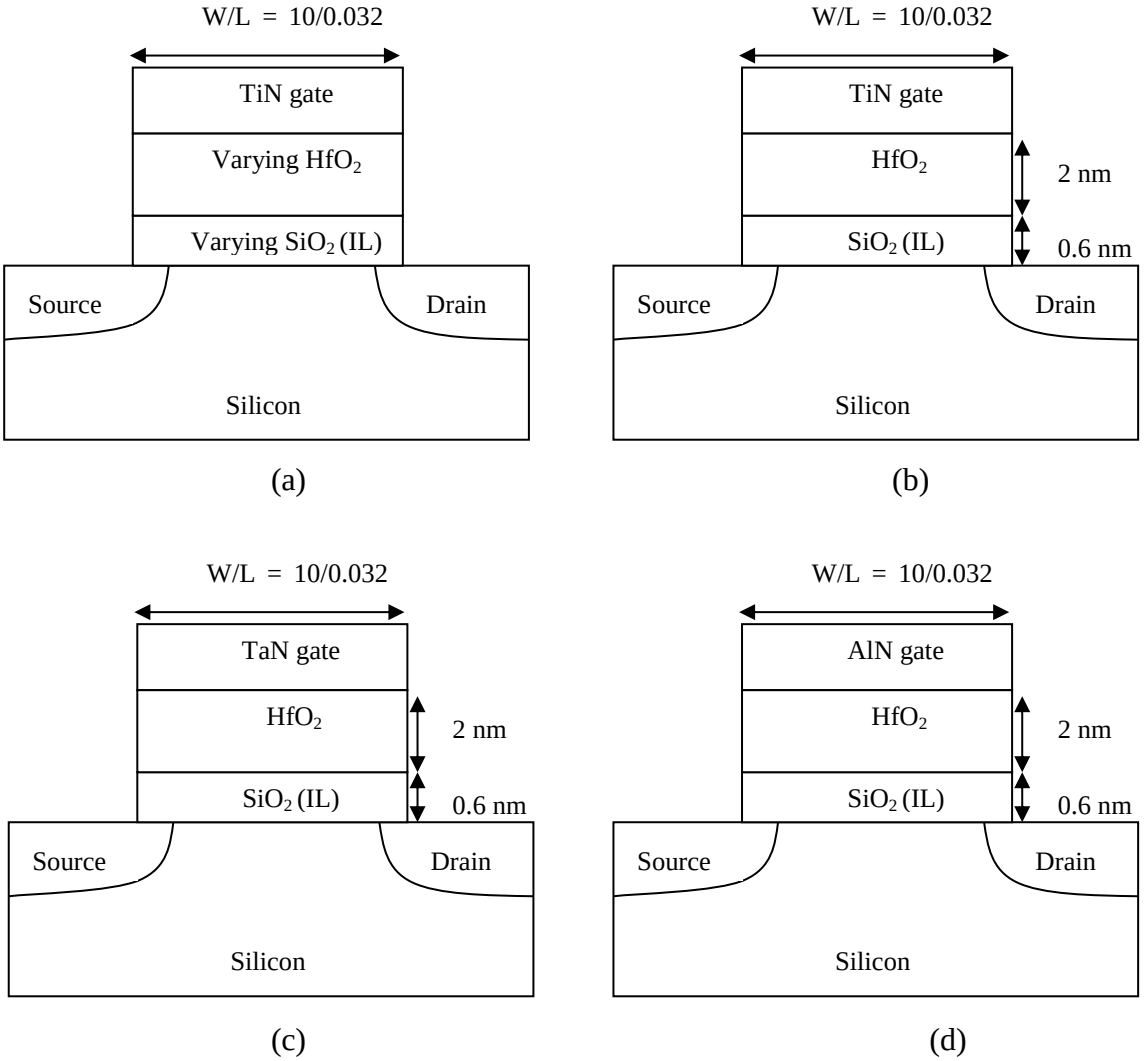


Figure 3.7 Cross section of test bed devices used for studying the effect of (a) geometrical variation and the effect of different metal gates (b) TiN (c) TaN (c) AlN using energy profiling technique (Bae et al., 2006; S. F. W. M. Hatta et al., 2010; S. W. M. Hatta et al., 2014; M. a. Negara et al., 2007; "Sentaurus Technology Template : 32-nm Gate-First Flow and CMOS Processing," 2011)

3.3.2.2 Strained SiGe channel and convetional p-MOSFET with SiO_2 dielectric

Using Sentaurus TCAD tools, the NBTI-induced threshold voltage shift (ΔV_{th}) and the corresponding generated defects which consist of positively charged E'centers and the E'/Pb H complex as well as their energy distribution density was investigated in this research. To ensure realistic assessment of NBTI degradation in a strained technology device, the test bed device from ("Simulations of Strained-Silicon CMOS Devices," 2007) was simulated by incorporating compressive strain into the channel exerted by the embedded SiGe pockets in the source and drain areas (Mistry et al., 2003; "Simulations of Strained-Silicon CMOS Devices," 2007). The simulation process flow is shown in Figure 3.8 (Mistry et al., 2003; "Simulations of Strained-Silicon CMOS Devices," 2007). The I_d-V_g characteristic of this simulated device is then benchmarked against that of a physically similar p-MOSFET fabricated with 50 nm gate length in (Mistry et al., 2003), as illustrated in Figure 3.9. A conventional, unstrained Si p-MOSFET with the same gate structure without the embedded SiGe pockets in ("Simulations of Strained-Silicon CMOS Devices," 2007) was also simulated for comparison. The cross section for embedded SiGe pockets p-MOSFET and conventional p-MOSFET are shown in Figure 3.10.

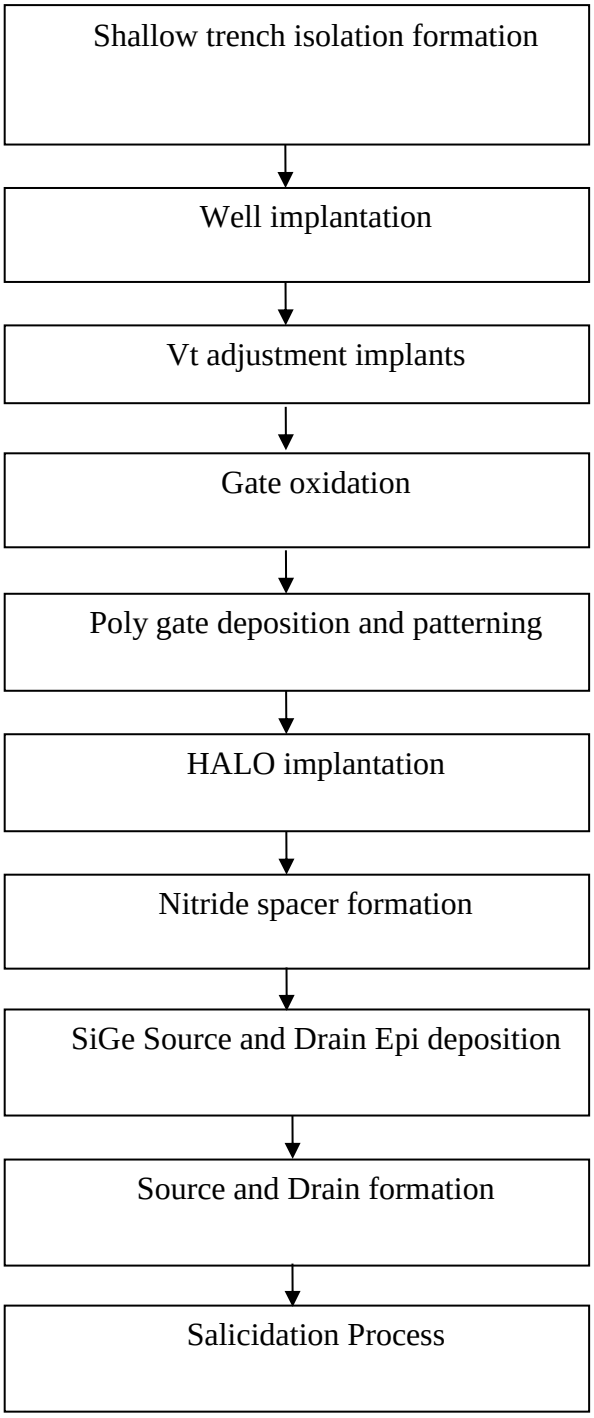


Figure 3.8 Process flow of simulated strained SiGe testbed device. For conventional p-MOSFET device, step for SiGe Source and Drain Epi deposition is omitted (Maiti et al., 2009; "Sentaurus Technology Template : CMOS Characterization," 2007, "Simulations of Strained-Silicon CMOS Devices," 2007)

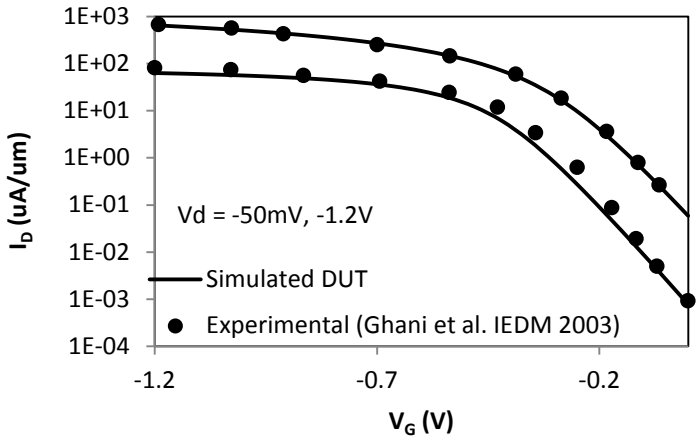


Figure 3.9 Comparison of I_d-V_g characteristics between simulation and experimentally measured characteristic of a physically real device ("Simulations of Strained-Silicon CMOS Devices," 2007)**,** (Mistry et al., 2003)

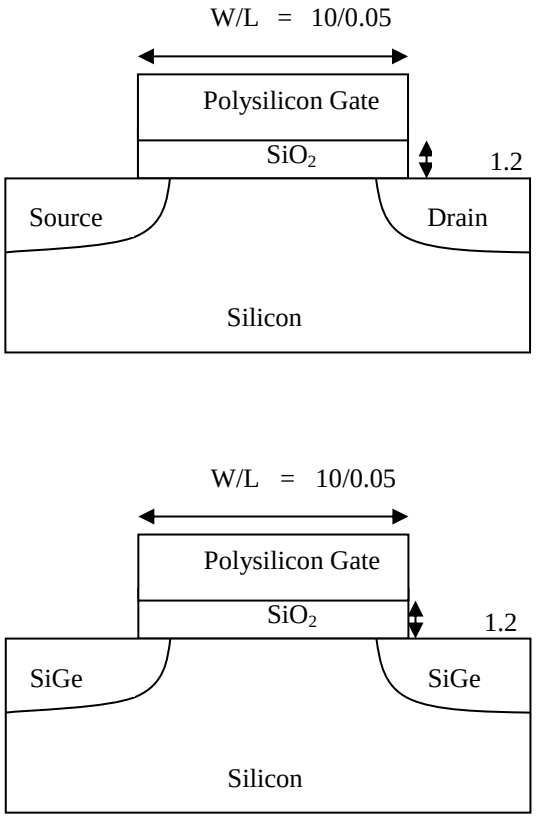


Figure 3.10 Cross section of conventional p-MOSFET and embedded SiGe channel p-MOSFET used in this simulation work ("Sentaurus Technology Template : CMOS Characterization," 2007, "Simulations of Strained-Silicon CMOS Devices," 2007)

3.3.2.3 FinFETs with Round Fin Corners and Tapered Fin Shape

The testbed PMOSFET FinFET devices simulated in this study are based on the 22 nm node FinFET technology available in Sentaurus TCAD tool ("Three-dimensional Simulation of 14/16 nm FinFETs with Round Fin Corners and Tapered Fin Shape," 2013). The simulation process flow for the 3D FinFET is shown in Figure 3.11 ("Three-dimensional Simulation of 14/16 nm FinFETs with Round Fin Corners and Tapered Fin Shape," 2013). This 3D FinFET was used to verify the suitability of the energy profile technique adopted for advanced design p-MOSFET. The fabrication process incorporated shallow trench isolation and deposition of high-*k* dielectrics which also featured in situ doped epitaxially grown SiGe raised source/drain for the purpose of reducing the Rext impact of the narrow fins further (Auth et al., 2012; "Three-dimensional Simulation of 14/16 nm FinFETs with Round Fin Corners and Tapered Fin Shape," 2013). This simulation process, which is based on gate-last scheme, was adopted for tuning the V_t by selecting an electrode material with the preferred work function. This is to ensure that the required work function was not affected by the high-temperature anneal which enabled the metal to migrate towards midgap work functions after the process. In this 3D FinFET simulation, the utilization of high-k first and metal gate last process will govern the amount of stress at the end of the process which in turn controls the FinFET performance ("Three-dimensional Simulation of 14/16 nm FinFETs with Round Fin Corners and Tapered Fin Shape," 2013). To ensure the advanced technology device adopted in this work matched the existing fabricated devices, this readily available design was used as it was verified that the simulated FinFET structure is similar to the TEM picture in (Auth et al., 2012).

A different fin width was adopted in this work as to study the effect on fin width variation on NBTI. The resultant threshold voltage for these simulated devices is -0.236 V to -0.282 V which are within the range of fabricated 22 nm FinFET technology in (Auth et al., 2012). The cross–section of simulated FinFET indicating the dimension of gate thickness, channel length and fin widths are shown in Figure 3.12.

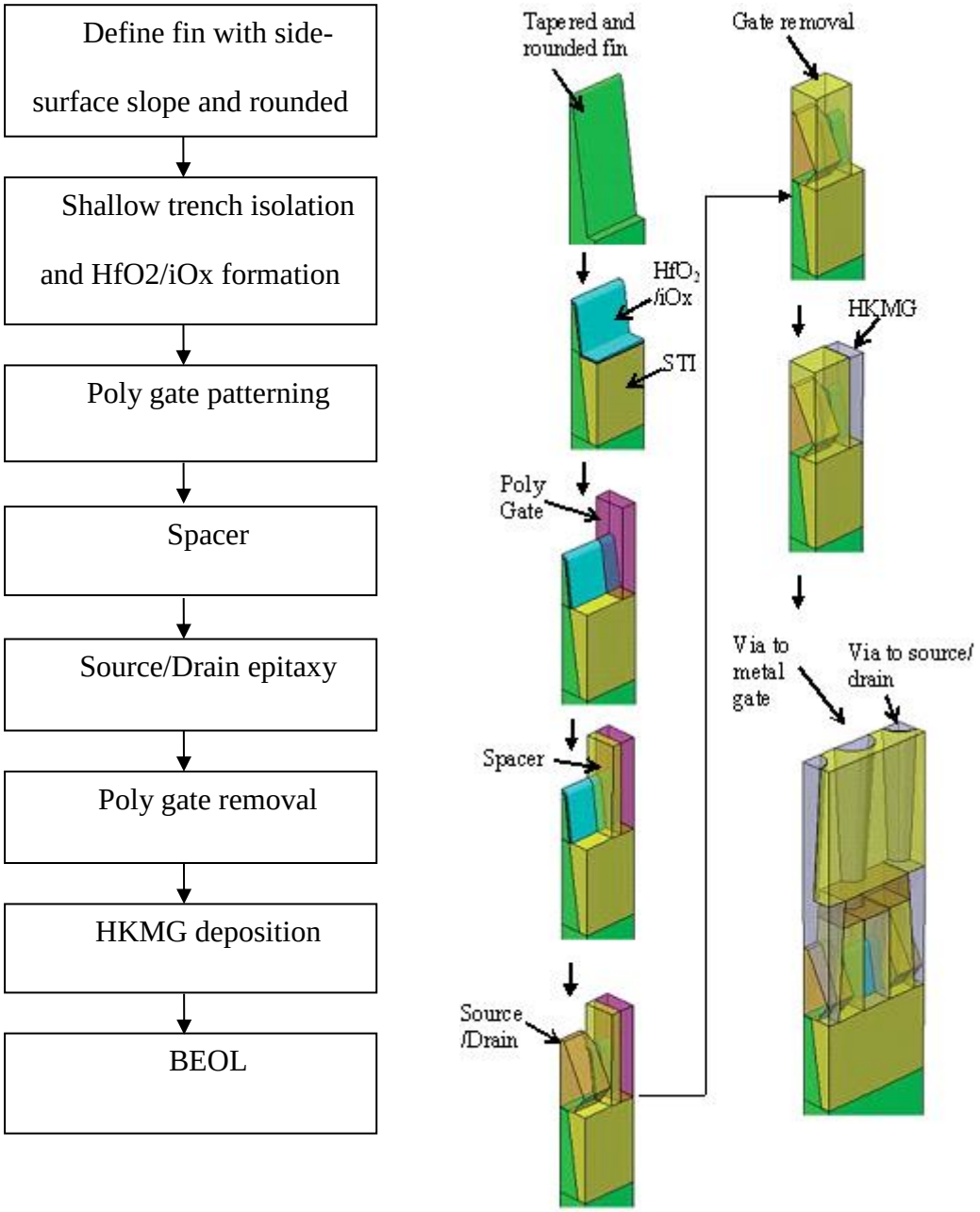
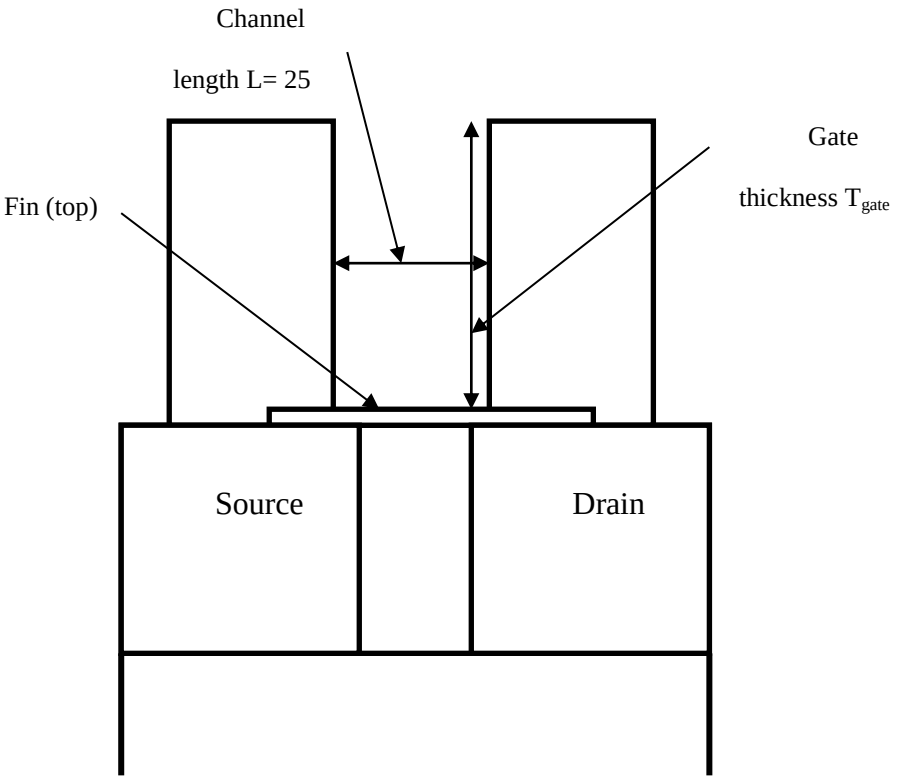
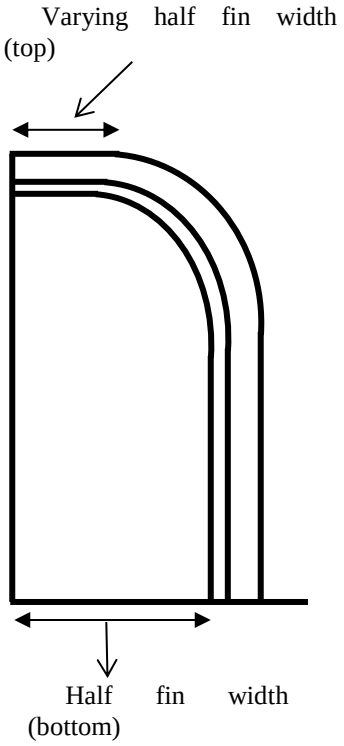


Figure 3.11 Process flow of the simulated 3D FinFET simulation ("Three-dimensional Simulation of 14/16 nm FinFETs with Round Fin Corners and Tapered Fin Shape," 2013)



(a)



(b)

Figure 3.12 (a) Diagram of dimension for simulated FinFET (b) The fin cross – section with varying top width

3.4 Summary

In this chapter, a simulation methodology adopted for NBTI characterization based on hydrogen and non-hydrogen transport formalism was discussed. The NBTI characterization simulation-based study was explained based on the implementation of using MIG simulator and Sentaurus TCAD simulator for hydrogen and non-hydrogen formalism respectively.

For the simulation based on hydrogen transport formalism, the feature of MIG was presented together with the simulation validation to ensure that the experimental features of NBTI based on hydrogen transport formalism were obtained using this simulator. The simulation was conducted under varied stress conditions using different diffusion species and measurement delay. The validation of the simulation results was based on the time exponent of atomic hydrogen and molecular hydrogen. Following this, the limitation of MIG simulator was discussed and the contributions of the simulation results in terms of static and dynamic simulation in this PhD thesis were subsequently highlighted.

For the framework of non-hydrogen transport formalism using the Sentaurus TCAD tool, the well-known methods employed for the simulation of the advanced design of modern semiconductor devices have been discussed. Among the available techniques, the drift-diffusion method with hydrodynamic model was chosen for 32 nm high-k devices while drift-diffusion method with Density Gradient quantum corrections was chosen for 3D FinFET devices.

Succeeding this, the framework of the Sentaurus simulator used in this study based on differences of device technology was described. Brief explanations of the simulation technique for each device were highlighted. Each of the carrier transport models were empirically extended to account for the mobility, generation and recombination process, electrostatic potential and mechanical stress to provide better physical accuracy and computational cost. Specific issues were addressed and discussed upon modeling the NBTI effects on 3D FinFET simulation to ensure physically-reliable results. Following this, the implementation of this framework using Sentaurus simulator for the scope of NBTI was also explained.

Finally, a description of the test bed devices used in the non-hydrogen transport formalism study was briefly discussed based on the device dimension, structure and fabrication process. The test bed devices were the realistic devices that could widely be used by others based on the obtained Id-Vg simulation demonstrating good agreement with experimentally measured Id-Vg characteristics for 32 nm high-k devices. For 3D FinFET simulation, the threshold voltage obtained from simulation was as predicted by the International Technology Roadmap Semiconductor (ITRS) projection and similarly observed with 22 nm fully depleted tri-gate transistor as fabricated by INTEL Corporation which was approximately -0.289 V. The 32 nm high-k based devices will be adopted for NBTI characterization using the Two-stage NBTI model and energy profiling technique while conventional silicon with and without SiGe and 3D FinFET devices will be adopted for the energy profiling technique.

CHAPTER 4: **RESULT AND DISCUSSION**

4.1 Introduction

This chapter presents the findings obtained from this work. The result and discussion will be divided into three parts. The first part will highlight the characterization of NBTI effects based on hydrogen transport formalism where the static and dynamic degradation were employed in this study. The second part is focused on the characterization based on default non-hydrogen transport formalism. The analysis will emphasize on the geometrical variation effects as well as the high-k integration issues on NBTI degradations. Meanwhile, the third part will present the refinement model of the default non-hydrogen transport model to correctly characterize the energy distribution of positive charges due to NBTI effects. Three different technologies of p-MOSFET consist of high-k based devices, unstrained and strained conventional SiO2 devices and FinFET devices were employed to demonstrate the applicability of the refined model. Lastly, the comparison between the default and refined non-hydrogen transport model are shown focusing on the sub-threshold operation, CMOS switching speed and lifetime prediction of high-k p-MOSFET device.

4.2 The Effect of NBTI Degradation Based on Hydrogen Transport Formalism

The study conducted in this section was based on static and dynamic simulation. The static simulation will analyse the resulting threshold voltage shift and identify the time in which the degradation reached 50 mV. This is to show that the optimized EOT for device under study was immune to NBTI effects. The important issue here is the recoverable component, denoted as *R* and thereafter, the characteristics. This has drawn significant interest because an accurate characterization of its transient

behaviour is very critical in modelling and assessing device and the system reliabilities accurately (Gao, Boo, et al., 2011). Previous studies have characterized the *R* dependence on duty factor and frequency in alternating current (AC) stress (B. Kaczer, T. Grasser, J. Franco, 2011; S. Mahapatra et al., 2011; Reisinger et al., 2009). However, only minimal information is available on the effects of recovery duration on the *R* over multiple cycles because most studies focused on repetitive stress and recovery cycles in a single run (D S Ang et al., 2011; Boo & Ang, 2012; Gao, Boo, et al., 2011; Z. Q. Teo et al., 2009). In present researches, the *R* of dynamic NBTI degradation was studied by using the modelling interface-defect generation (MIG) simulator (A. E. Islam, 2014; M.A. Alam & Mahapatra, 2005; Ahmad Ehteshamul Islam et al., 2007) and by applying a customized sequence of stress and relaxation pulses to the transistors. The *R* is characterized based on the applied stress voltage, temperature, duration, and *EOT*. On top of that, the characteristics from the perspectives of oxygen vacancy defect and hydrogen transport formalism is discussed.

4.2.1 Simulation Framework for Hydrogen Transport Formalism Based Study

For the hydrogen transport formalism based study, the simulation framework will be based on static and dynamic simulation. The static simulation approach will be explained in Section 4.2.1.1 while the dynamic simulation approach is explained in Section 4.2.1.2.

4.2.1.1 Static Simulation

The simulation process was performed by considering the stress voltage as static (DC) and the diffusing species as atomic hydrogen. Two p-MOSFETs with different EOTs of 5 nm and 1.1 nm respectively were employed. Stress voltages and temperature were changed systematically to analyze transistor characteristics. The

applied stress voltage was kept between -2 V and -3.5 V while the stress temperature was kept between 70^{o}C and 150^{o}C. The stress voltages and temperatures were used as within the range of NBTI experiment conducted by previous researchers (Gao, Ang, et al., 2011; S. W. M. Hatta et al., 2014) . The accuracy of the simulation was checked by keeping a harmony with the power law while a degradation slope of 0.25 was obtained due to the diffusion of atomic hydrogen (M. A. Alam, 2003; Chakravarthi et al., 2004; Kjell O. Jeppson and Christer M. Svensson, 2004; A. T. Krishnan et al., 2005).

4.2.1.2 Dynamic Simulation

The simulation of stress and relaxation sequence was developed to study the effects of dynamic NBTI using the pulse train simulation adopted in MIG. These pulses acted as stress voltage for a larger absolute voltage and also as a recovery voltage for a lower absolute voltage as shown in Figure 4.1. To investigate the dependence of threshold voltage degradation on stress and recovery time, the recovery time duration (t_r) varied for n = 500 s, 1000 s, 1500 s and 2000 s while the stress time (t_s) was fixed at 100 s in a multiple run and single run as shown in Figure 4.1 (b) and (c) respectively. Table 4.1 shows the stress and recovery time used in this simulation framework where the diffusion species in this simulation is molecular hydrogen. Two conventional structures of SiO_2 dielectric p-MOSFETs with different effective oxide thickness (EOT), 1.7 nm and 2.8 nm, were employed respectively [10]. The simulated p-MOSFETs had n-type substrate doping, $N_D = 3 \times 10^{17} cm^{-3}$, and p-type poly doping, $N_A = 3 \times 10^{20} cm^{-3}$.

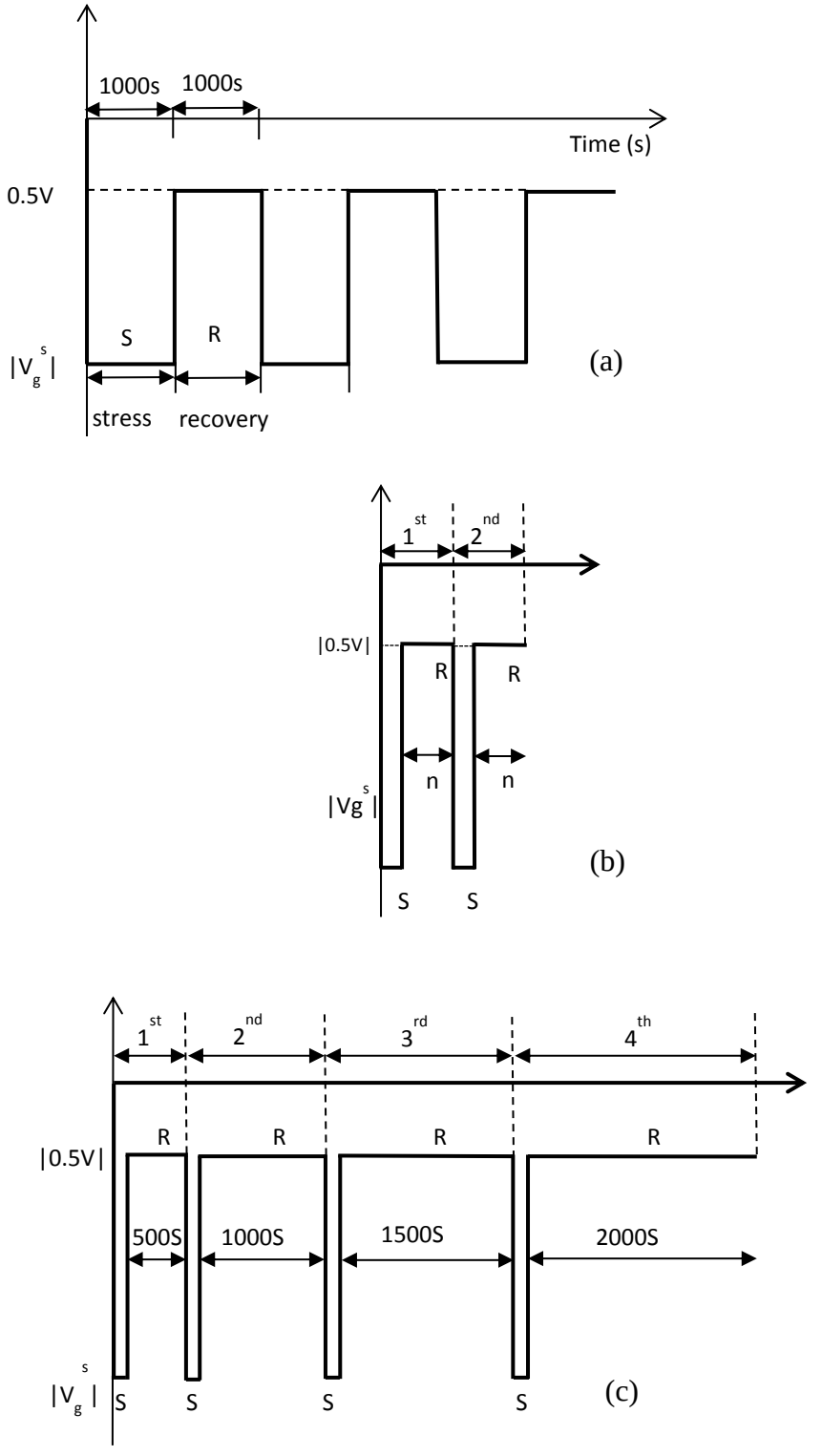


Figure 4.1 Schematic diagram of the gate voltage waveform for dynamic NBTI stress (S) and recovery (R) cycles (a) stress and recovery time fixed at 1000 s in single run (b) stress time fixed (100 s) while recovery time varied in multiple run (n = 500 s, 1000 s, 1500 s and 2000s) (c) stress time fixed (100 s) while recovery time varied in single run (1st cycle = 500 s, 2nd cycle = 1000 s, 3rd cycle = 1500 s and 4th cycle = 2000s)

Table 4.1 Simulation conditions based on the previous research works

Pulse	Stress time (t_r)	Recovery time (t_s)	Reference
(a)	1000 s	1000 s	(Gao, Boo, et al., 2011)(Gao, Ang, et al., 2011)
(b)	100 s	n = 500 s, 1000 s, 1500 s, 2000 s	(D S Ang et al., 2011)
(c)	100 s	n = 500 s, 1000 s, 1500 s, 2000 s	(D S Ang et al., 2011; Z. Q. Teo et al., 2009)

Stress voltages were varied accordingly to analyse the transistors characteristics. The applied stress voltages, V_S, were kept between -1.2 V and -2.52 V. These stress conditions were based on the experimental work conducted by (Gao, Boo, et al., 2011). The applied stress voltage was kept in that range so that the oxide electric field was maintained in the range of -6 to -9 MV/cm (Gao, Ang, et al., 2011). A suitable range of biasing condition was needed to avoid the process of the impact ionization problem (Boo et al., 2012). The recovery voltage, V_R, was fixed at 0.5 V chosen on the basis of the bipolar stress implementation in order to study the behaviour of recovery effects during a more positive gate bias stress (Maheta et al., 2008). The temperature applied was in the range of 100°C to 150°C based on the work conducted by (Gao, Ang, et al., 2011; Ryan et al., 2007; Yang & Liu, 2008) where significant NBTI degradation was observed and studied. The simulation condition was chosen to mimic the condition as discussed by (Ryan et al., 2008) [18] to explain the dynamic NBTI in the framework of R – D Model.

4.2.2 Validation for hydrogen transport formalism study

The validation of simulation using the MIG tool is based on the characterization of the device under different stress conditions. In this work, the stress conditions based on varied stress temperature and stress voltages. For a simulation using atomic hydrogen species, time exponent, n ~ 0.25 is expected for a wide range of stress conditions.

To examine the effect of temperature dependence on NBTI degradation, transistors with EOT 1.1 nm and EOT 5 nm were simulated at fixed stress gate voltage with different stress temperature. The simulation results are shown in Figure 4.2 (a) and (b). The slopes are in the range of 0.2 – 0.25, in agreement with (M. A. Alam, 2003; Chakravarthi et al., 2004; Kjell O. Jeppson and Christer M. Svensson, 2004; A. T. Krishnan et al., 2005). This behaviour also indicated that the diffusion species is atomic hydrogen. ΔN_{it} shows the temperature dependence where as temperature increases, ΔN_{it} will increase as well. This can be explained by (Khan & Hamdioui, 2010) based on the Arrhenius relation with diffusion rates affected by temperature variation, where the generation of ΔN_{it} was dependent on the number of broken Si-SiO_2 bonds. This mechanism was supported by (Souvik Mahapatra, Kumar, & Alam, 2004) where the ΔN_{it} creation dependent strongly on temperature.

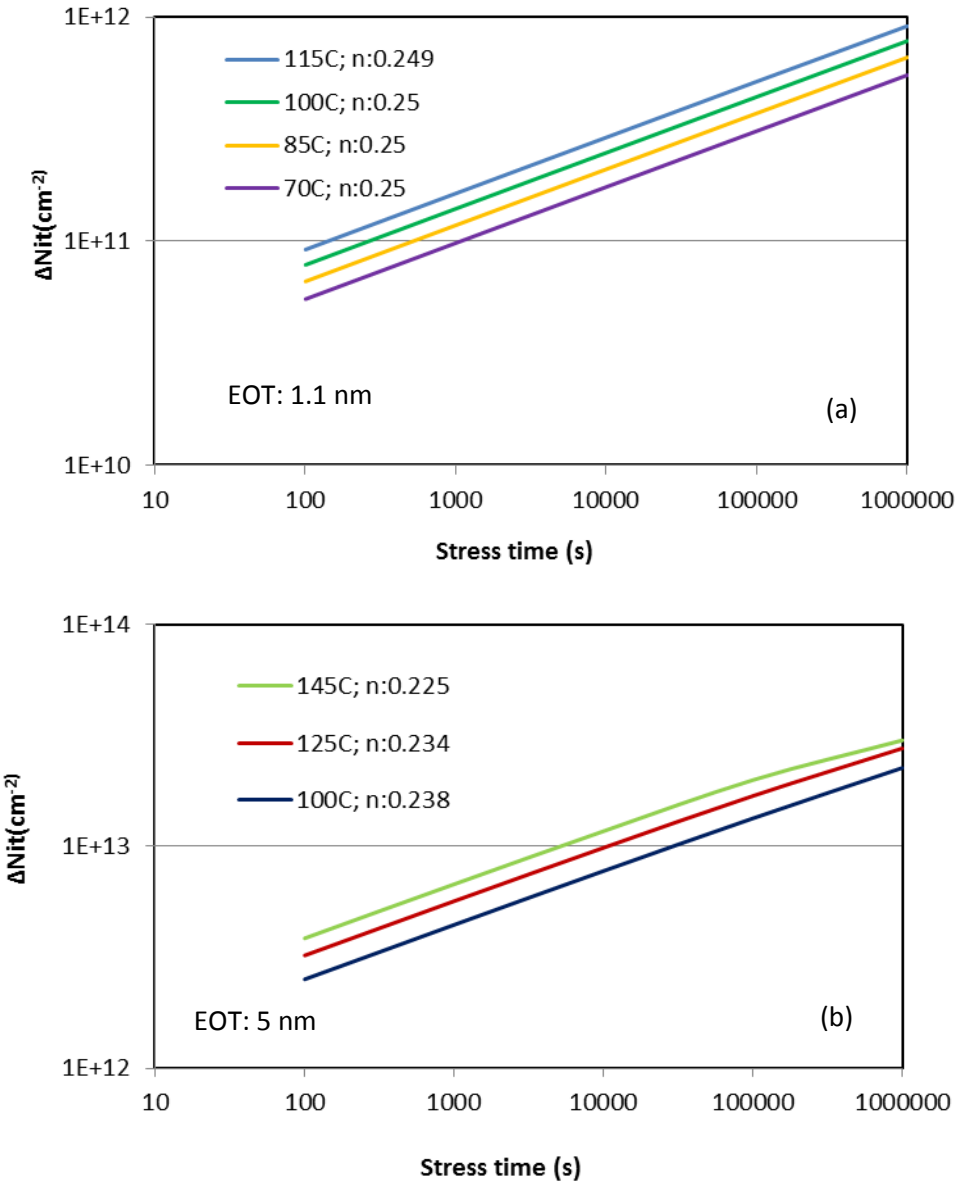


Figure 4.2 ΔN_{it} as a function of stress time for the fix stress voltage and various ranges of stress temperature (a) EOT = 1.1 nm (b) EOT = 5nm

Figure 4.3 (a) and (b) show the behaviour of two different p-MOSFETS with EOT 1.1 nm and EOT 5 nm respectively where the stress voltage was fixed and the temperature varied. Both transistors showed that ΔV_{th} increases when temperature increases, with a similar trend reported in (Schroder, 2007). The slope was found to

be 0.25, which again showed that NBTI is hydrogen species dependent. The thicker device showed higher degradation as compared to the thinner device. This may be due to the higher amount of defects in a thicker device (Ahmad Ehteshamul Islam et al., 2007) and based on the relationship between the drain current and oxide thickness (S. F. W. M. Hatta et al., 2010).

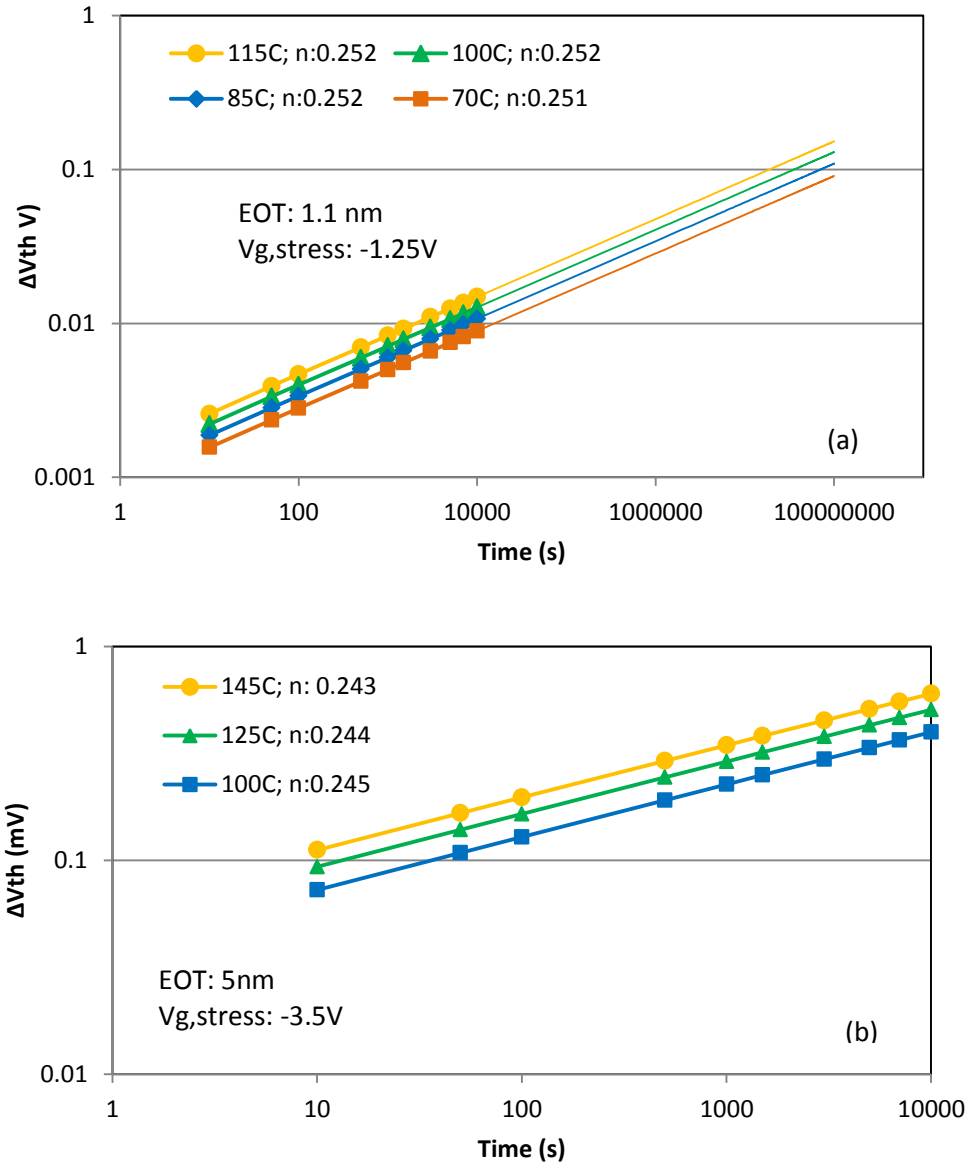


Figure 4.3 ΔV_{th} as a function of stress time for constant stress voltage and various ranges of stress temperature (a) EOT = 1.1nm (b) EOT = 5nm

Figure 4.4 (a) and (b) show the graphs for ΔV_{th} for EOT=1.1 nm and EOT=5 nm, at a constant temperature with different gate voltages. To show the dependence of generated interface trap on the stress gate voltage, the extracted interface concentration is plotted in

Figure 4.5 (a) and (b) for both EOTs. Higher stress voltage contributed to higher generation of interface trap. Time exponent, n ~ 0.25 obtained for the interface trap generation further confirms that the hydrogen species for the degradation is based on atomic hydrogen. There has been considerable debate regarding the voltage or field dependence of NBTI degradation and it was concluded that transistors with SiO_2 normally experience a field dependent process (Ahmad Ehteshamul Islam et al., 2007). It can also be concluded that the oxide field is an important factor in NBTI degradation. For both transistors, the interface trap concentration increases as the stress voltage increases which obey the power law, n ~ 0.25 due to the use of atomic hydrogen in the simulation. The resultant threshold voltage shift also increased as the stress voltage increases. This shows an elevated NBTI effect at higher stress voltage.

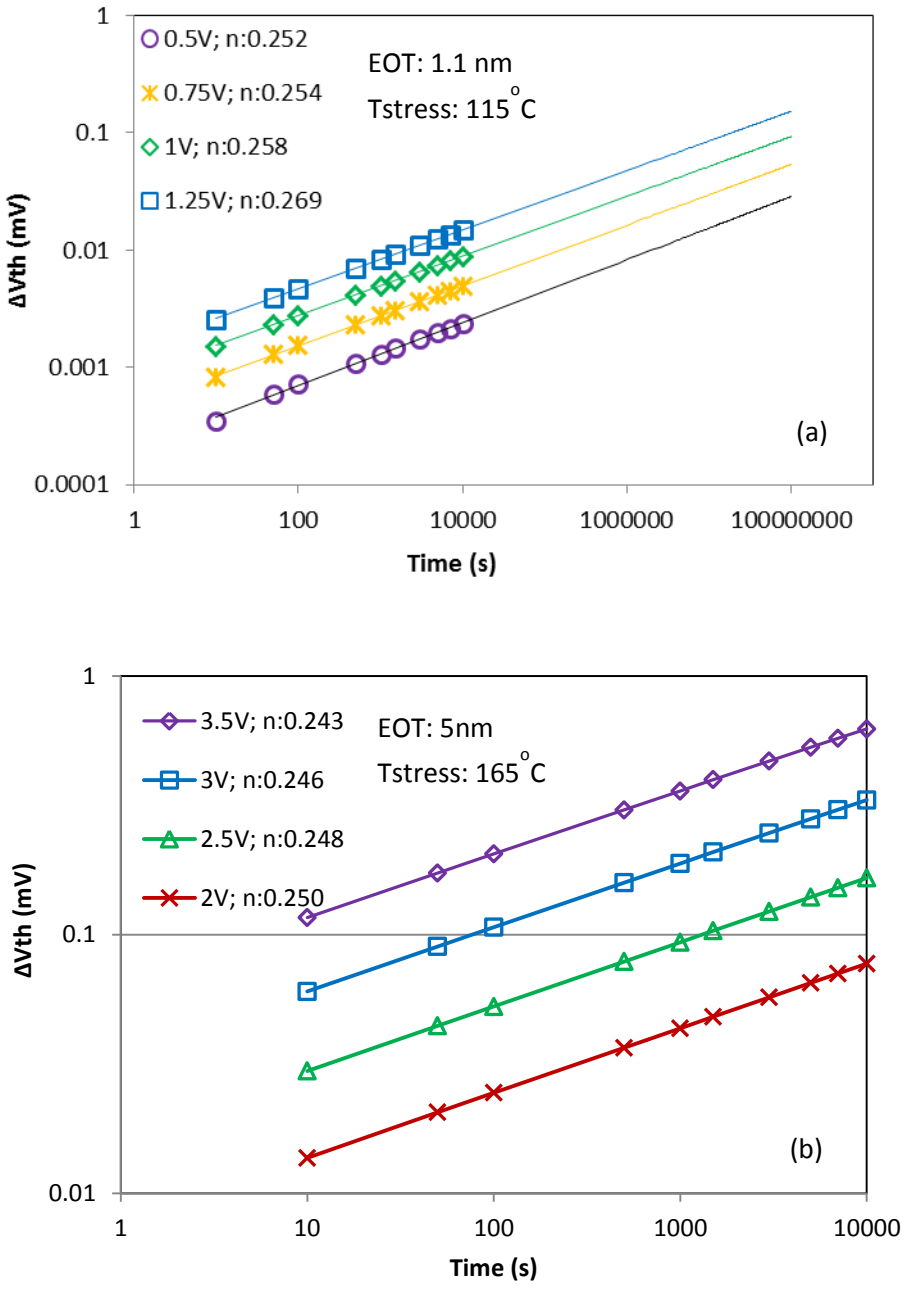
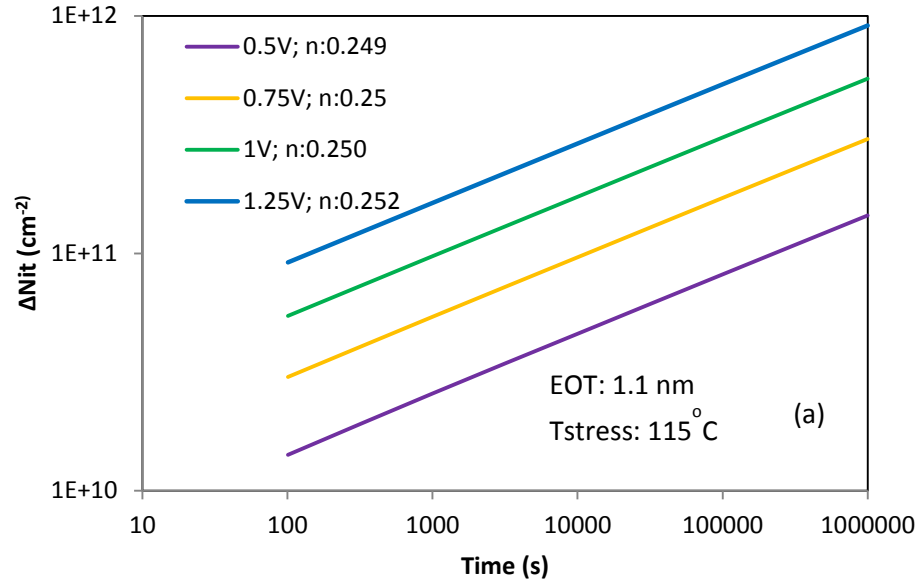


Figure 4.4ΔV_{th} as a function of stress time for constant stress temperature and various ranges of stress voltage (a) EOT = 1.1 nm (b) EOT = 5 nm



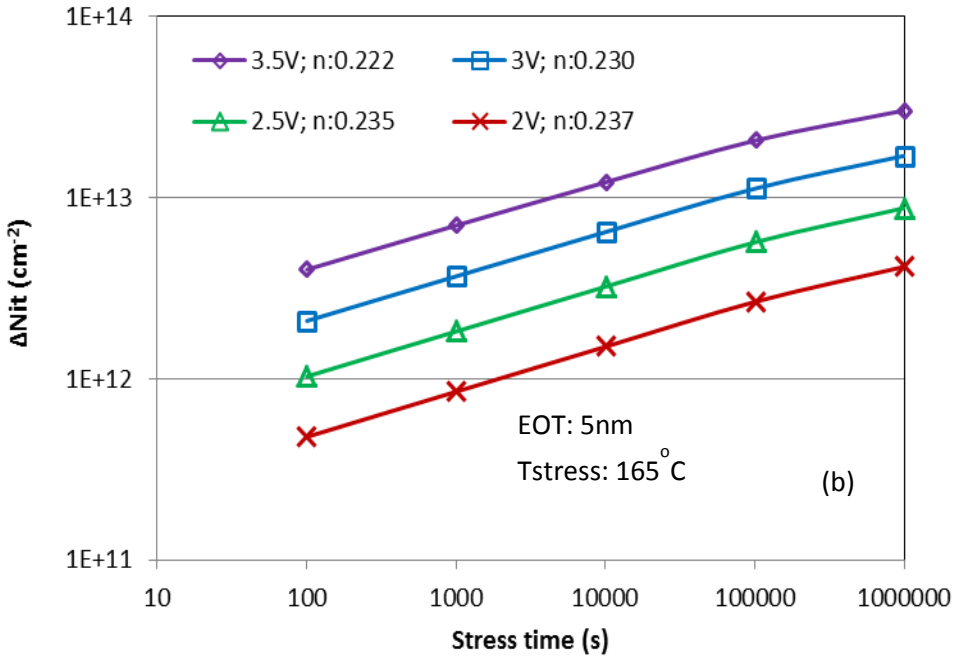
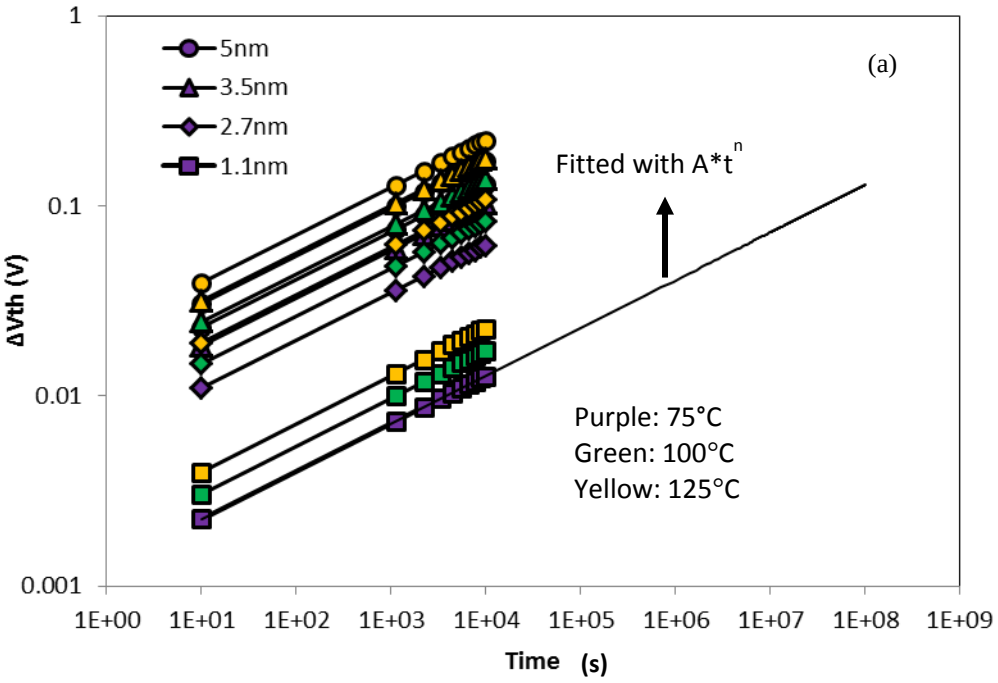


Figure 4.5 Interface trap concentration as a function of stress time for constant stress temperature and various ranges of stress voltage (a) EOT = 1.1 nm (b) EOT = 5 nm

4.2.3 Static Degradation Characteristics under Hydrogen Transport Formalism

Following the validation of the simulation framework based on hydrogen transport formalism in Section 4.2.2, the work was further conducted to study the degradation characteristic on different EOT. In this section, the effect of degradation on different EOT is investigated by keeping the same applied oxide electric field ~ 11 MV/cm for both EOT under different stress temperatures. The degradation was checked by extrapolating the resultant threshold voltage shift using the time exponent power law ($A*t^n$) as shown in Figure 4.6 (a). The time when the degradation reached 50 mV is then extracted and plotted in Figure 4.6 (b). From the results, the degradation is observed to be more suitable for a thicker EOT device. The possible explanation for this is because thicker oxides have more trapped charges since the de-trapping process in poly was difficult hence lesser empty states were available (Ahmad Ehteshamul Islam et al., 2007). All devices showed that the 50 mV threshold voltage shifts were observed earlier under higher stress temperature. For standard NBTI experimental stress temperature condition widely used in industries ~ 125°C, devices with EOT above 1.8 nm reaches 50 mV degradations earlier than 10 ks as shown in Figure 4.7 . Hence, it can be concluded that the devices with EOT thicker than 1.8 nm were less immune to NBTI effects.



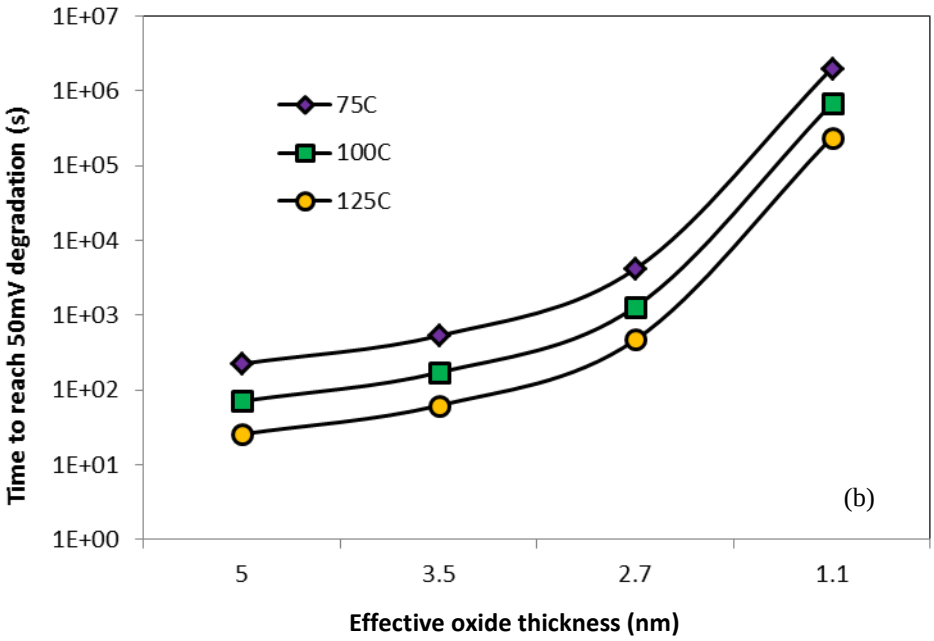


Figure 4.6 (a) Extrapolating the resultant threshold voltage shift using the time exponent power law ($A*t^n$) (b) The time when the degradation reached 50 mV is extracted

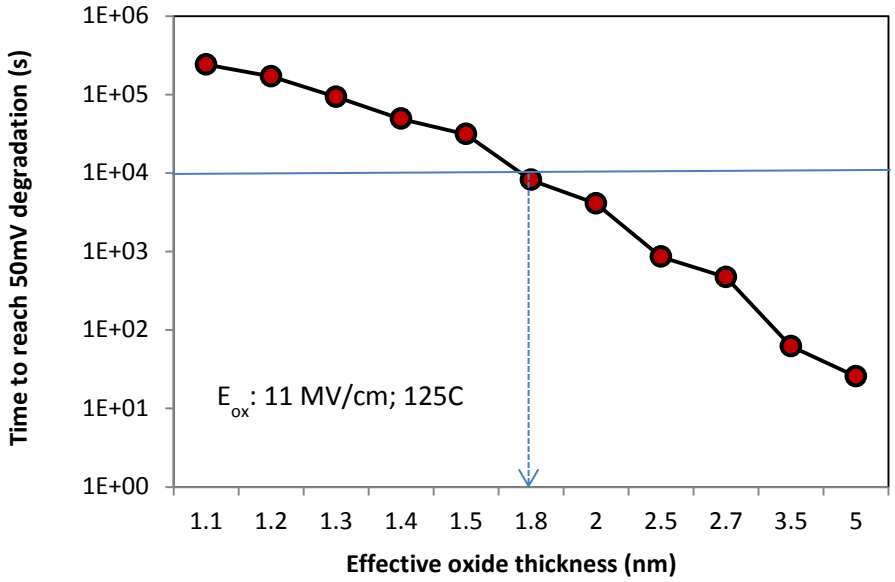


Figure 4.7 The samples for the conventional single layer SiO_2 device with an EOT larger than 1.8nm can reach the minimum of 50mV of degradation within the stress time of 10ks. This suggests that scaling is critical for this device in order to obtain lower NBTI effects

4.2.4 Recoverable Component Characteristics under Hydrogen Transport Formalism

In this part, the recoverable component will be characterized extensively to understand its behavior in dynamic condition which typically happens to the real device very much related to the condition in digital IC. The digital IC which operates in '1' and '0' represent the stress and recovery conditions.

4.2.4.1 Effect of stress voltage and temperature on the recoverable component of dynamic NBTI

Figure 4.8 shows the evolution of ΔVth resulting from the simulated stress and the relaxed cycles as shown in Figure 4.1 (a). Three stress and recovery cycles are

presented with four different applied stress voltages. It can be observed that the magnitudes of threshold voltage shift during both stress and recovery increase when the applied stress voltage is increased. Upon the application of stress bias, from the perspective of R-D model, the interface traps are generated at the Si/SiO_2 interface due to the de-passivation of Si-H bonds in the interface. Subsequent to the de-passivation process, the hydrogen species are released and diffuses away from the Si/SiO_2 interface thus degrading the performance of the device. Higher stress bias produces more interface traps, thus increasing the degradation (ie: threshold voltage shift).

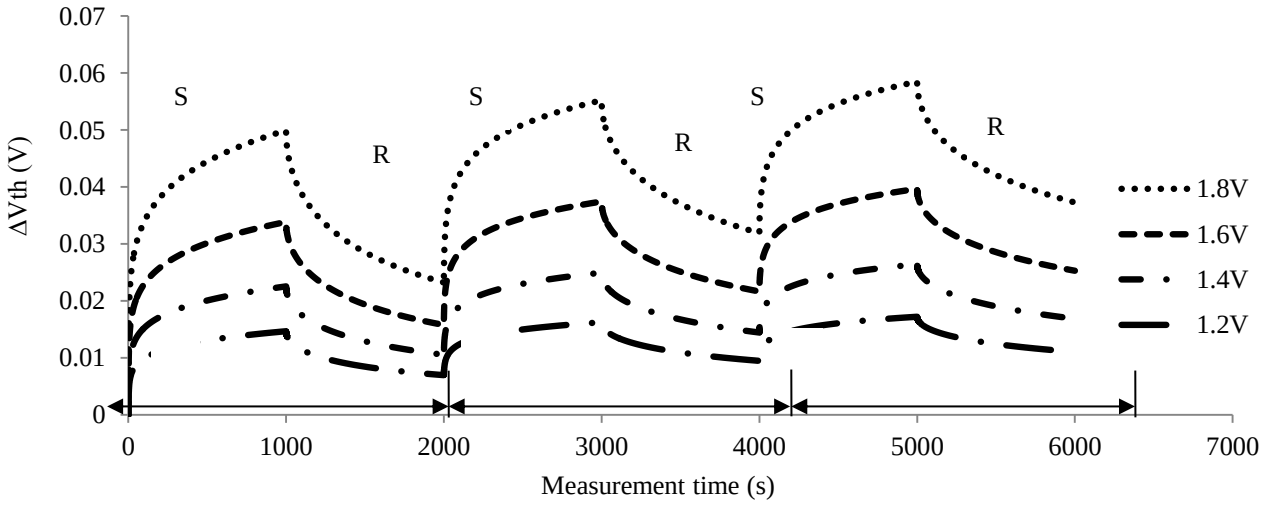


Figure 4.8 Evolution of threshold voltage shift under dynamic NBTI for EOT = 1.7 nm during stress (S) and recovery (R) cycles in single run

To further examine the characteristics of dynamic NBTI, the amount of threshold voltage shift recovery, R, over a number of cycles was analysed. Figure 4.9 shows the evolution of threshold voltage shift resulting from one complete cycle of stress and relax. The definition of the recoverable component, R, is as shown in the figure where the difference between the magnitudes of threshold voltage shift are at the end of

stress and at the end of recovery, that is, $R = |\Delta V_{th}|^{eos} - |\Delta V_{th}|^{eor}$ (Boo & Ang, 2012). In this effort, the magnitude of R decreases as the number of cycle increased, as shown in Figures Figure 4.10 (a) and (b). This result is consistent with the hole-trapping mechanism, where the trapped hole sites were transformed into a permanent component, thus increasing the $|\Delta V_{th}|^{eor}$ (Boo et al., 2012; Boo & Ang, 2012; Gao, Boo, et al., 2011). It can also be noted that R also increases when a higher stress voltage and temperature were applied. This can be explained by the increased hole trapping due to the higher applied stress, thus resulting in the increased magnitude of $|\Delta V_{th}|^{eos}$ (Boo et al., 2012; Boo & Ang, 2012). The existence of hole trapping mechanism supports the finding obtained in previous section where the threshold voltage shift was increased when the EOT increased (Ahmad Ehteshamul Islam et al., 2007).

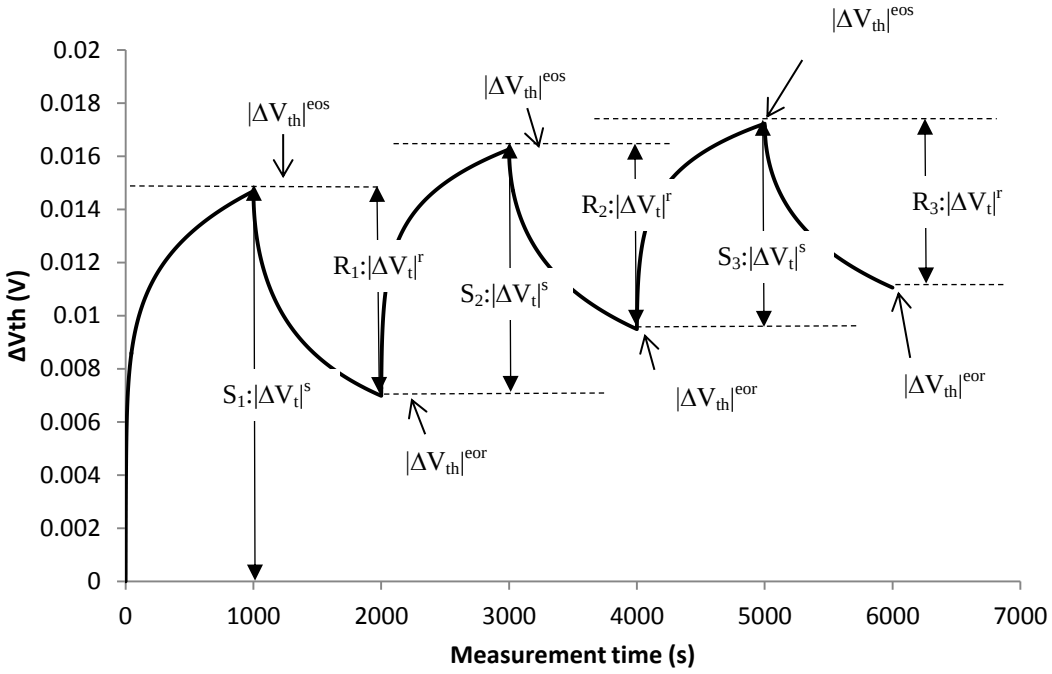


Figure 4.9 Evolution of |ΔVth| for single run and definition of stress component, (S_n) recoverable component, (R_n) in a typical dynamic NBTI cycle. n is the number of stress and recovery cycle. The S = $|\Delta V_t|^s$ is referring to the amount of threshold voltage different during stress cycle while R = $|\Delta V_t|^r$ referring to the amount of threshold voltage shift different during recovery cycle. The recoverable component, R is defined as R = $|\Delta V_{th}|^{eos}$ - $|\Delta V_{th}|^{eor}$

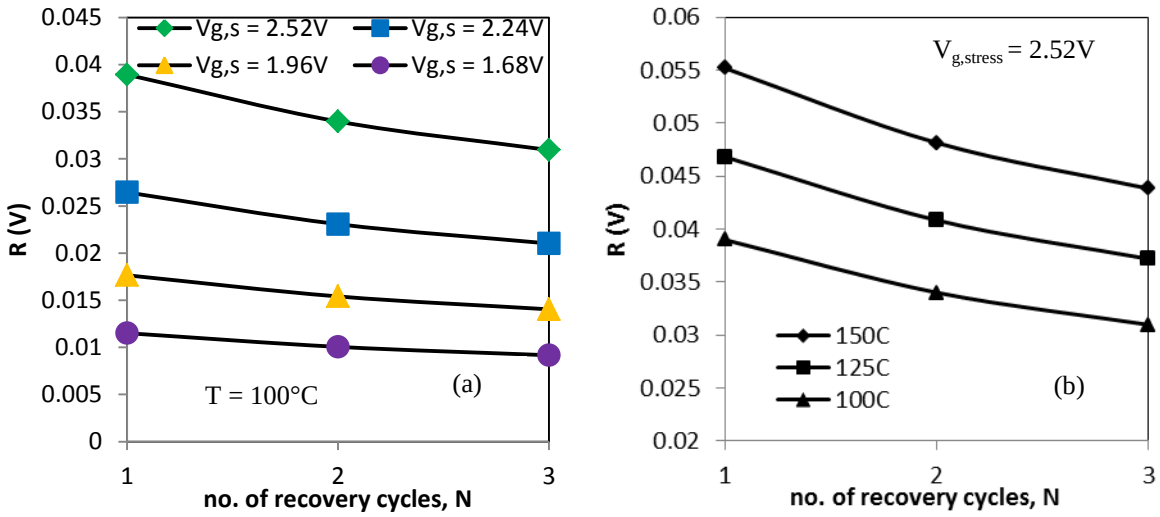


Figure 4.10 Recoverable components, R as a function of number of the dynamic NBTI cycles, N in a single run for (a) different gate voltages and (b) different stress temperature

4.2.4.2 Effect of stress and recovery Duration

(a) ***Multiple run***

Figure 4.11 shows the evolution of threshold voltage shift during stress and recovery cycles with fixed period of stress and varied period of recovery for multiple run for four different recovery time duration, tr, where (a) 2000 s, (b) 1500 s, (c) 1000 s and (d) 500 s. The simulation setup for a fixed duration of stress and the varied period of recovery were determined from (Gao, Ang, et al., 2011) and shown in Figure 4.1 (b). The applied oxide field was maintained at 9 MV/cm. From the figure, the biggest threshold voltage shift is almost similar for all periods of fixed stress and varied recovery.

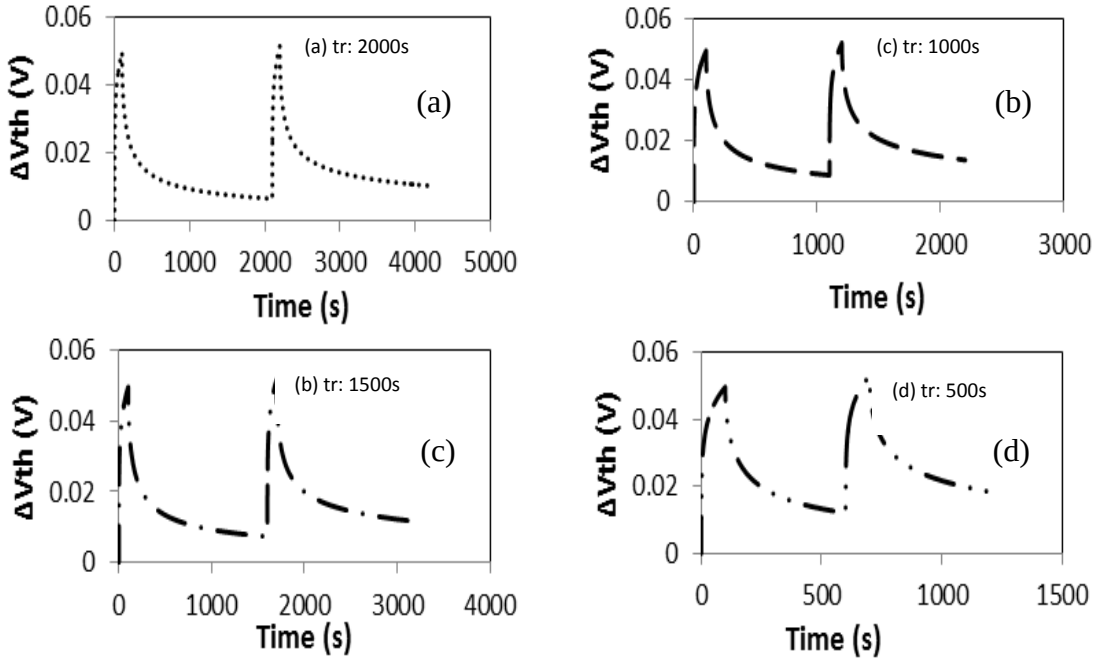


Figure 4.11 Evolution of threshold voltage shift with a variation of recovery cycle duration, tr, with fixed stress cycle time in multiple run based on fixed recovery voltage, V_R = 0.5V. (a) tr = 2000 s (b) tr =1500 s (c) tr =1000 s and (d) tr =500 s. The applied stress voltage is |2.5 V|.

To further comprehend the mechanism of dynamic NBTI, Figure 4.12 (a) and (b) summarizes the magnitudes of threshold voltage shift during stress, $|\Delta V_t|^s$, and recovery, $|\Delta V_t|^r$ cycles respectively. The $|\Delta V_t|^s$, and $|\Delta V_t|^r$ represents stress component, S, and recoverable component, R, respectively. The definition for both S and R components are illustrated in Figure 4.9. From Figure 4.12 (a), the threshold voltage shift ($|\Delta Vth|^s$) is almost similar for all stress cycles because the stress duration is fixed. The stress component, S for the second cycle for each device lessens as compared to the first cycle. This could be caused by some of the broken hydrogen species from the first cycle which have yet to relax thus contributing to more threshold voltage shift ($|\Delta Vt|^{eor}$) during the second recovery cycle (Gao, Ang, et al., 2011).

Figure 4.12 (b) shows the recoverable component, R, where the threshold voltage shift in recovery cycle, ($|\Delta Vth|^r$) increases over a recovery length time. This is because of more molecular hydrogen species that were able to diffuse back to the interface at a longer recovery time duration, therefore reducing the threshold voltage shift at the end of the recovery cycles, $|\Delta Vth|^{eor}$. This characteristic was similarly discussed in (D S Ang et al., 2011) where the recovery of interface trap was large due to the hydrogen being close to the Si/SiO_2 interface when the number of stress and recovery cycles was small thus reducing the $|\Delta Vth|^{eor}$. The smaller value of $|\Delta Vth|^{eor}$ for larger duration of recovery time exhibits the increment of recoverable component, R.

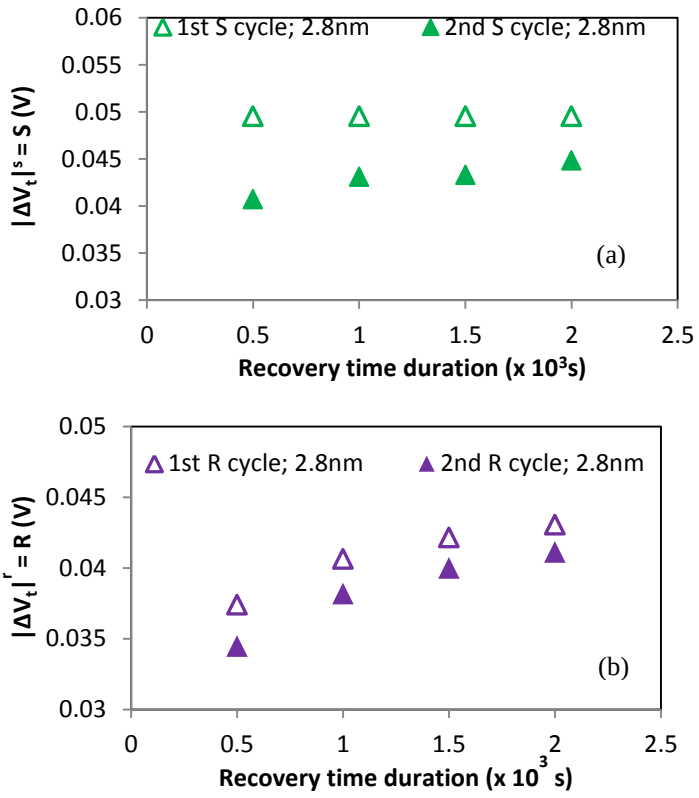


Figure 4.12 (a) Stress component, (S) as a function of stress time and (b) Recoverable component, (R) as a function of recovery time for multiple run. The S and R were extracted from Figure 5.

(b) ***Single run***

Figure 4.13 (a) and (b) shows the evolution of threshold voltage shift with a variation of recovery cycle duration, tr, in a single run with a fixed stress cycle duration with fixed recovery voltage, V_R = 0.5V and the extracted recoverable components, R, as a function of number of the dynamic NBTI cycles, N, respectively. The evolution of threshold voltage shift was obtained based on a simulation setup shown in Figure 4.1 (c). The extracted recoverable components, R, exhibited variation trend when increased from first cycle to second cycle. The recoverable components R however, reduced from the second cycle towards the fourth cycle. The smallest recoverable

component during the first cycle reflects the lowest $|\Delta Vth|^{eos}$ due to smaller number of interfaces trap concentration contributing to the threshold voltage shift. During the second cycle where the recovery time duration of the first stress cycle is the shortest, less hydrogen returns to the broken bonds due to the shorter time, thus increasing the $|\Delta Vth|^{eos}$ during the stress period for the second cycle. Towards the fourth cycle, the recovery time duration was increased while the increase of recoverable components, R, was expected by inferring that the hydrogen has more time to diffuse back to re-passivate the broken bonds. However, from the simulation results, the recoverable components, R, was reduced during the third cycle and further reduced during the fourth cycle. Similar recoverable component, R, behaviour was also found and discussed in (M.A. Alam & Mahapatra, 2005; D S Ang et al., 2011; S. Mahapatra et al., 2005). The reduction of the recoverable component was explained as, due to the mechanism of hydrogen species during the recovery cycle, the hydrogen still moved away from the Si/SiO_2 interface. Therefore, in each cycle, during the stress and recovery cycle, more hydrogen moved away from Si/SiO_2 interface thus reducing the number of re-passivation interface trap concentration in the subsequent cycle. As the number of interface trap that does not relax increases, the $|\Delta Vth|^{eor}$ increased thus exhibiting a less recoverable component. Based on the reduction of the recoverable component in the repeated stress and recovery cycles, the degradation mechanism can also be described due to the transformation of hole traps into a permanent form (Boo et al., 2012; Boo & Ang, 2012; Gao, Boo, et al., 2011).

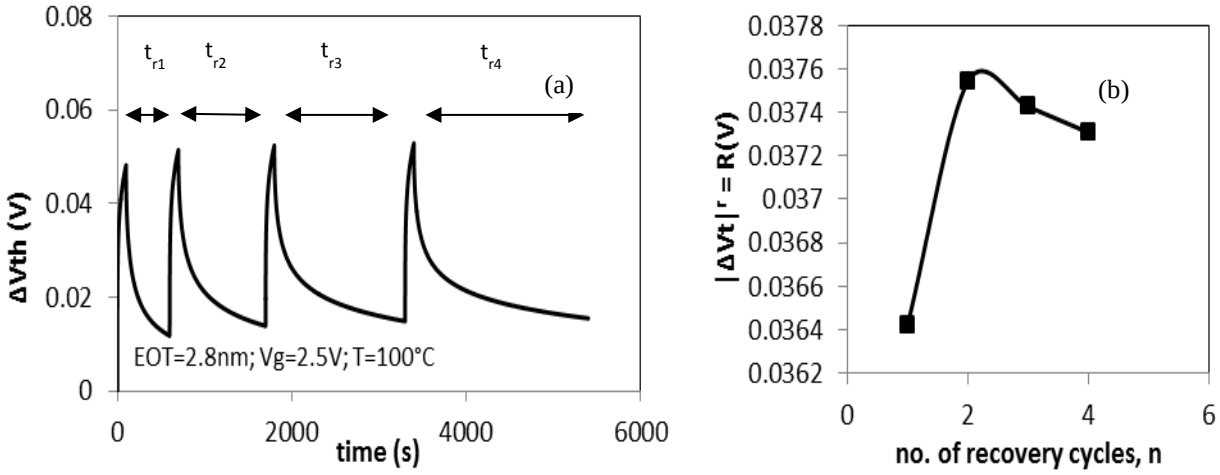


Figure 4.13 (a) Evolution of threshold voltage shift with a variation of recovery cycle duration, tr, in single run with fixed stress cycle duration based on fixed recovery voltage, V_R = 0.5V (b) Extracted recoverable components, R as a function of number of the dynamic NBTI cycles, N. The applied stress voltage is |2.52 V|.

4.2.4.3 Permanent component

Because the simulation is based on the R-D model, the resulting degradation was driven by a hydrogen transport mechanism where a gradually decreasing R component was observed when the number of stress cycle increased (Gao, Ang, et al., 2011; Gao, Boo, et al., 2011). This is also consistent with the self-limiting recovery perspective where the R is dependent on the number of stress cycles. The simulation results showed that the similar characteristics of R can be observed by both mechanisms of the hole trapping effect and hydrogen diffusion. These suggest that the underlying connection between the two different mechanisms is the interface trap concentration which represents the permanent component in both mechanisms (D S Ang et al., 2011, 2008).

4.2.4.4 Effect of effective oxide thickness (EOT) on recoverable component

To investigate the effect of EOT on recoverable component, R, a simulation setup as shown in Figure 4.1 (b) was used where multiple simulations were conducted based on varied recovery time duration. In this section, the fixed stress gate voltage, $V_{Gstress}$ = 2.52V for both EOT was used. This gave a higher electric oxide field for the thinner EOT. The recoverable component, R was found to be increased when the recovery time duration increased for both EOT as shown Figure 4.14 (a). A higher recoverable component, R was observed for a thinner EOT which indicated that a more permanent component contributed to the degradation (M. A. Alam, 2003). To further investigate the characteristics of the recoverable component, R, for a different EOT, Figure 4.14 (b) shows $|\Delta Vth|^{eos}$ and $|\Delta Vth|^{eor}$ as a function of recovery time duration. Higher $|\Delta Vth|^{eos}$ and $|\Delta Vth|^{eor}$ were observed for a thinner EOT. The $|\Delta Vth|^{eos}$ is almost constant for both EOTs due to a similar stress time duration. However, for the second cycle, an increment in $|\Delta Vth|^{eos}$ was observed for a smaller EOT. This could be explained as due to less hydrogen stored in SiO_2 for a thinner EOT as compared to a thicker EOT thus less hydrogen can re-passivate the interface trap during the first recovery cycle (D S Ang et al., 2011). Similar characteristics were also observed for the $|\Delta Vth|^{eor}$ where an increment in $|\Delta Vth|^{eor}$ for a thinner EOT in the second cycle implying that less hydrogen can contribute to re-passivating the interface trap thus a larger threshold voltage shift is observed for a thinner EOT. The $|\Delta Vth|^{eor}$ for both EOTs reduced as recovery time duration increased. This is more time was available for the hydrogen to diffuse back to the Si/SiO_2 interface thus re-passivating the interface trap and reducing the threshold voltage shift.

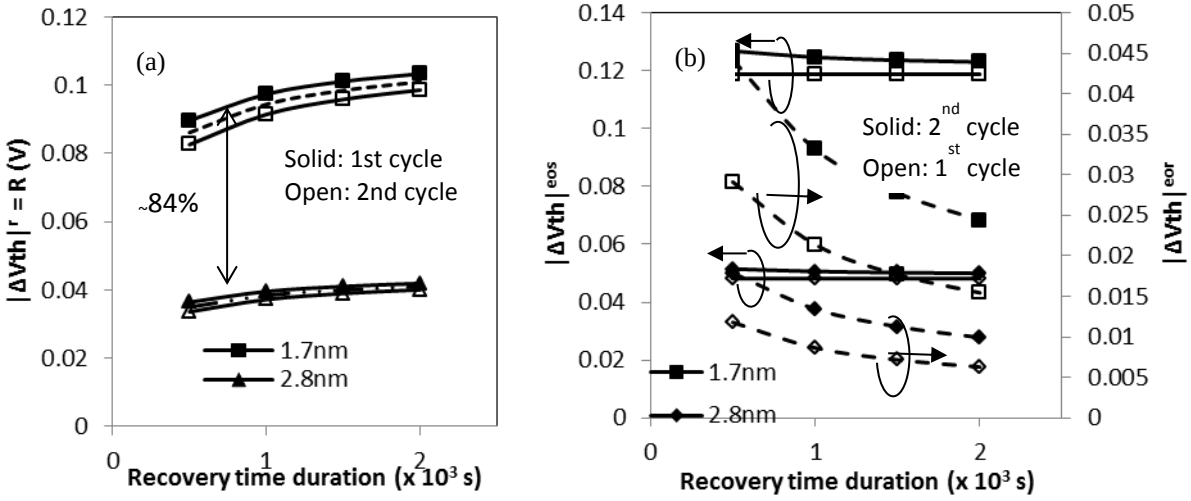


Figure 4.14 (a) Recoverable component, (R) as a function of recovery time duration based on multiple run (n = 500 s, 1000s, 1500 s and 2000 s) for EOT 1.7 nm and 2.8 nm (b) Characteristics of $|\Delta Vth|^{eos}$ and $|\Delta Vth|^{eor}$ as a function recovery time duration. The applied stress voltage is |2.52 V|.

4.3 The Effect of NBTI Degradation Based on Non-Hydrogen Transport Formalism

In the previous section, the degradation and recovery characteristics of NBTI features were studied based on the R-D model which considered the interface trap generation as the only contributor towards the degradation mechanism based on hydrogen transport formalism. Based on the single and multiple run simulation approach using pulse simulation method, the hole-trapping mechanism based on the recoverable component behavior could be distinguished. Further understanding on this recoverable component is essential in producing a robust theoretical framework for enlightening key characteristics of experimental features of NBTI. The recoverable component has been widely studied by prominent researchers in NBTI (D S Ang et al., 2011; Boo & Ang, 2012; Zhi Qiang Teo et al., 2010). The R-D model was contradicted by highlighting that the dynamic NBTI experiments were driven by non-hydrogen transport formalism (D S Ang et al., 2011; Z. Q. Teo et al., 2009; Zhi

Qiang Teo et al., 2010). Therefore, the two-stage NBTI model will be adopted in this chapter to understand the contribution of recoverable component known as positively charge E' centers or switching oxide trap while the permanent component is known as interface trap concentration or the Pb center. In this section, the two-stage model will be used to study the effect of NBTI degradation based on the gate stack variation of 32 nm high-k based devices and with regard to high-k process integration issues.

4.3.1 Simulation Framework for Non-Hydrogen Transport Formalism

To examine the effects of gate geometrics on NBTI, the physical layer thicknesses of the HfO_2, dielectric layer and the SiO_2 interface layer are varied based on an early study (S. F. W. M. Hatta et al., 2010). Each deposited stack layer is within the range of nominal thickness as shown in Figure 4.15 (S. F. W. M. Hatta et al., 2010; M. A. Negara et al., 2007). This study aims to account for the contribution of the hole trap to the NBTI degradation effect, whereas the earlier work only explained the interface trap generation in characterizing NBTI effects.

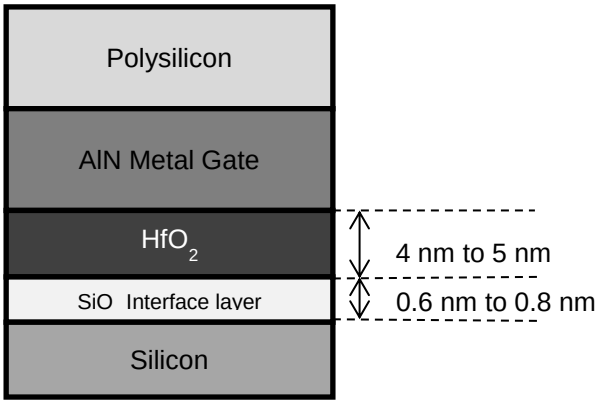


Figure 4.15 Gate stack cross-sectional profile of the testbed PMOSFET with variation in sub-layers

Based on the hydrodynamic transport model, the simulator self-consistently solves the holes and electrons current continuity equations coupled to Poisson's equations. To model the NBTI effects on the devices, the interface regions were defined in the device structure because the trap and charge densities were defined on the interfaces by using a Sentaurus mesh ("Suite, Sentaurus TCAD," 2011). The NBTI physical model is defined in the interface region between the silicon and oxide layers. The solutions of the device equations along with the two-stage NBTI model were used to extract threshold voltage degradation, hole trap density, and interface trap density ("Suite, Sentaurus TCAD," 2011). The stress temperatures range from 300 K to 400 K, which conform to the experimental settings of other NBTI studies (S. F. W. M. Hatta et al., 2010; Zhi Qiang Teo et al., 2010).

The threshold voltage degradation in this simulation was determined using the widely adopted on-the-fly (OTF) method (Huard et al., 2006; Souvik Mahapatra & Alam, 2008; Maheta et al., 2008; Yang & Liu, 2008). Application of pre-stress voltage was needed in this model to equilibrate the occupancy of different states and thus ensuring that all states were not empty at the early phase of stress period (Gupta et al., 2012). Time-zero delay in the OTF method introduced an artifact for the measured threshold voltage shift; thus, BTI power-law ($\Delta Vth = A.t^n$) was not observed during short stress (A.E. Islam et al., 2007). Therefore, the stress time was increased up to 1,000s to minimize the issue in this simulation.

4.3.2 Validation for non-hydrogen transport formalism study

The accuracy of the two-stage NBTI model used in this study was validated by observing the power-law time dependence of the resulting ΔVth. The observed power-law time dependence shown in Figure 4.16 (a) and (b) are subsequent to different

stress temperature and stress voltage respectively. A relatively small exponent of n ~0.1 was obtained and attributed to the hole trapping effect. This occurrence agrees with the ultrafast switching measurements in (Zhi Qiang Teo et al., 2010) which suggested that the dynamic NBTI was due to both the hole trapping/de-trapping event and interface state generation. To further examine the kinetics behind NBTI degradation effects, the hole trap density, S_2 and interface trap density, S_4 are plotted in Figure 4.16 (c) and (d), respectively.

The kinetics of the hole trap density, S_2 and interface trap density, S_4 observed for all the devices showed almost similar behavior. The density of the hole trap, S_2 is higher than that of the interface trap, S_4 during the early stressing period. However, as stress time increases, the hole trap density, S_2 tends to saturate while the interface trap density, S_4 continued to increase. The saturation in S_2 suggests that the positive charges are completely filled within the first 1ks and thus causing the saturation trend. This mechanism, which does not comply with the hydrogen-transport model, was also reported in other studies on dynamic NBTI (Gao, Boo, et al., 2011; Zhi Qiang Teo et al., 2010), thereby lending further credibility to the two-stage NBTI model used in this study. The graphs indicate that the hole traps were gradually transformed into a more permanent form, de-passivating the interface trap precursor as triggered by the hole captured at an E' center precursor (Gao, Boo, et al., 2011). This phenomenon has also been reported by other NBTI studies using the ultrafast measurement method (Gao, Boo, et al., 2011; Zhi Qiang Teo et al., 2010). The time evolution of distribution of interface trap density, S_4 and hole trap density, S_2 shows that the degradation kinetic is more noticeable in oxide bulk than in the interface region. The degradation kinetic observed is similar under a wide range of stress voltages and temperatures.

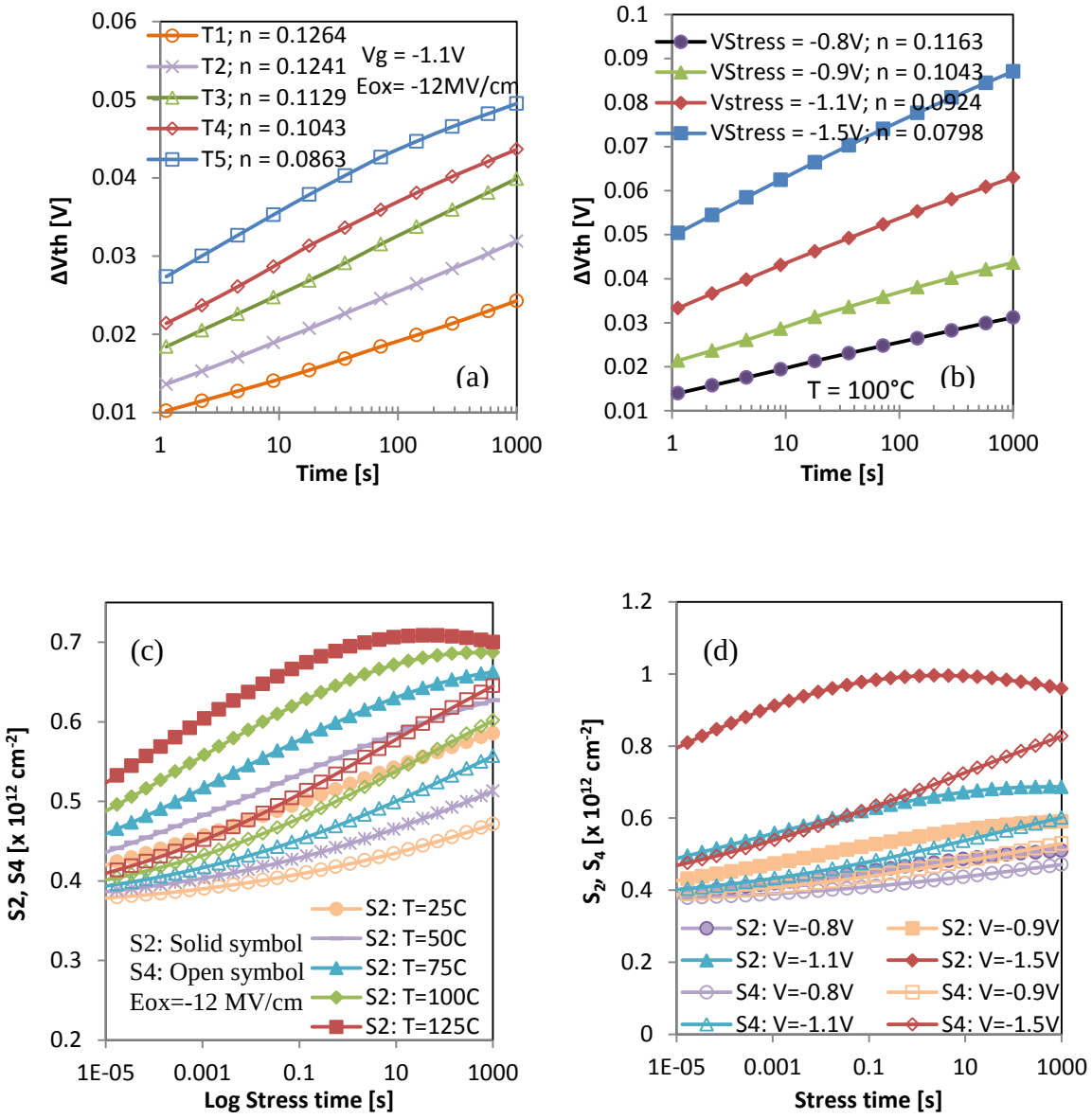


Figure 4.16 Threshold voltage shift as a function of stress time at (a) different stress temperatures and (b) different stress gate voltages. Hole trap density, S_2 and interface trap density, S_4 as a function of stress time at (c) different stress temperatures and (d) different stress gate voltages

4.3.3 The effects of gate stack variation on NBTI Degradation under Non-hydrogen Transport formalism

NBTI characterization based on non-hydrogen transport formalism will be explained in the next section. After thorough analysis based on the simulation setup using the R-D model, this scope of work will show the contribution of interface trap together with the hole trapping effect towards the NBTI degradation. The discussion will be based on the effects of gate stack geometrical variation in NBTI degradation upon validation the simulation framework for non-hydrogen transport formalism in Section 4.3.2.

4.3.3.1 Effects of gate stack sub-layer physical thickness on NBTI

This section presents the simulation results of the NBTI degradation subsequent to varying the physical thicknesses of the bulk HfO_2 and the SiO_2 IL layer. In Figure 4.17(a), the ΔV_{th} by varying the physical thickness of the HfO_2 layer was compared. A thicker HfO_2 dielectric layer at a higher stress temperature exhibited larger ΔVth. This observation is in accordance with the measurement reported in (Neugroschel et al., 2006), where a more pronounced ΔVth was observed because of more trapping centers in the thicker bulk of the HfO_2 dielectric layer. As shown in Figure 4.17(b), thicker SiO_2 IL results in less ΔV_{th}, which is also in agreement with (Neugroschel et al., 2006). The less ΔV_{th} observed in thicker SiO_2 IL can be attributed to smaller fast transient charging effect, which is similarly reported in other studies (S. Krishnan et al., 2012; Neugroschel et al., 2006). According to Ref. (J. H. Lee, Wu, Islam, Alam, & Oates, 2008), the thinner SiO_2 IL experienced higher gate oxide field thereby accelerating the NBTI degradation effect because of the subsequent increase of the diffusion rate of hydrogen species. In this study, the contribution of hole trap density to the degradation was computed. Thus, the higher gate oxide field accelerated the

hole trapping effect, which then increases the degradation rate. The contribution of the hole trap density, S_2 and interface trap density, S_4 to the degradation of scaled SiO_2 thickness will be described in the subsequent sections. From the simulation results, it can be suggested that the majority of the defects are located in the Hf-bulk layer due to the significant degradation it can cause at thicker bulk layer.

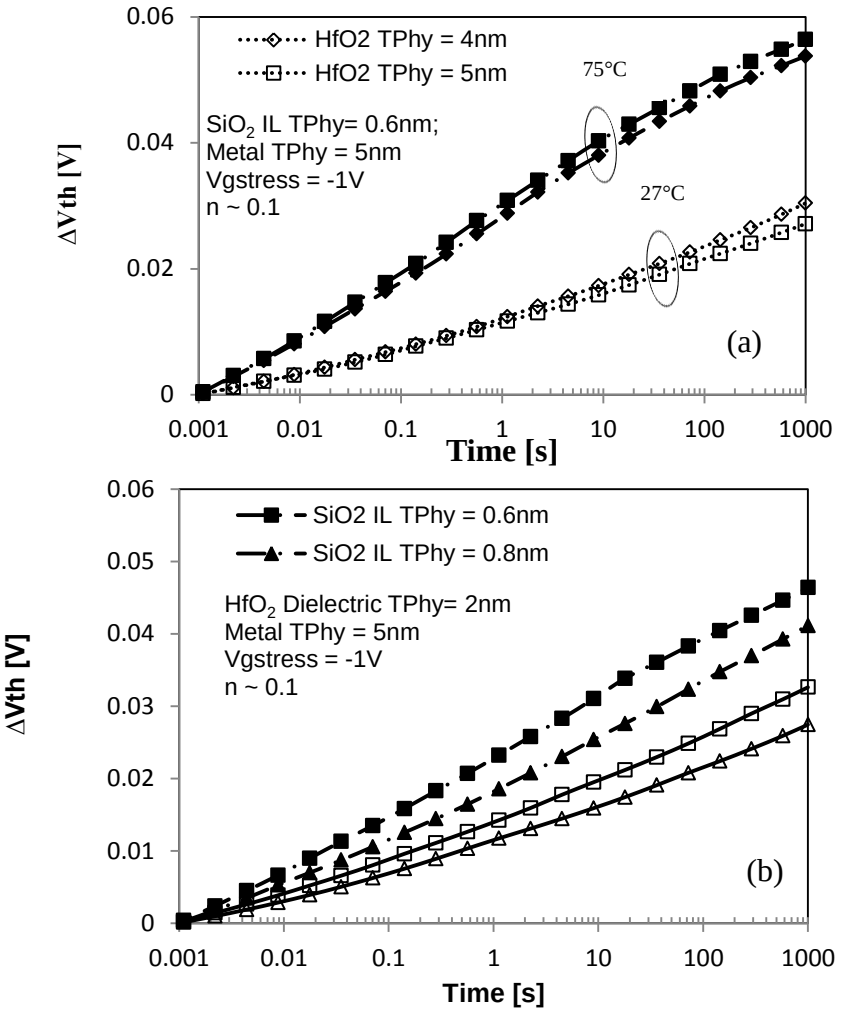


Figure 4.17 Power-law time dependence of simulated Δ*Vth* for variation of physical thickness (TPhy) for (a) HfO_2 layer and (b) SiO_2 IL

4.3.3.2 Effects of scaled SiO_2 interface layer thickness during stress and recovery cycle

This study was conducted by varying the stress and recovery condition of PMOSFETs with different SiO_2 IL thicknesses. The time evolution of threshold voltage shift was studied during the stress and relaxation phase as shown in Figure 4.18 (a) and (b), respectively. Higher degradation was observed in thinner SiO_2 IL as discussed previously. The relaxation phase dynamics followed the stress characteristics where thinner SiO_2 exhibits slower relaxation effects.

The dynamic behavior of stress and relax mechanisms are further explained by the time evolution of the hole trap density, S_2 and interface trap density, S_4 as shown in Figure 4.18 (c) and (d), respectively. The hole trap density, S_2 and interface trap density, S_4 were higher in the device with thinner SiO_2 IL. The higher hole trap density, S_2 in thinner IL device could be explained by the diffusion of oxygen from IL during the deposition process of HfO_2 on IL (Ryan et al., 2007). All of the fabrication process parameters used in the simulation were fixed except for the IL thickness which suggests that more oxygen was diffused in thinner IL; thus, higher density of E' defects is expected. This finding concurred with the ESR measurement study on electrically active IL defects in which E' center defects function as hole traps (Ryan et al., 2008). The defects can act as hole traps because of their locations which are close to the Si/dielectric interface and allowed the defects to play a role in the charge capture. These E' defects increased during stress bias upon the capturing of holes from the channel as explained by the switching hole trap mechanism. The de-passivation of the interface trap precursor triggered by the hole capturing process at the E' center increases as stress time increases. This phenomenon was observed in

most studies using the ultrafast measurement method (Gao, Boo, et al., 2011; Zhi Qiang Teo et al., 2010).

The stress time at which the hole trap density, S_2 was reduced for different thicknesses of SiO_2 IL constantly occurred after 10s stress duration. This occurrence implied that the hole traps took a more permanent form and do not depend on the SiO_2 IL thickness for a particular applied stress voltage and temperature. As indicated in Figure 4.18 (c), within the 1,000 s stress time, the hole trap density, S_2 is always higher than the interface trap density, S_4. It can then be deduced that during the period of stress, the defects were more significant in the oxide bulk than at the interface between the oxide and the substrates. However, in approaching the end of stress time, the positively charged E' centers were reduced significantly, whereas the interface traps continued to increase.

During the relaxation phase, interface trap density, S_4 was higher than the hole trap density, S_2 and both were reduced as the relaxation time increases. This behavior is in agreement with the experimental work in (Neugroschel, Bersuker, & Choi, 2007) based on the DCIV measurement where hole trap density, S_2 decreases during relaxation through a re-passivation process of interface traps. Higher interface trap density, S_4 during the relaxation process occurred when hydrogen leaves behind unpassivated dangling bond locked in the positively charged E' center defect which effectively delayed the recovery of the E' center defect (T. Grasser et al., 2009b; Tibor Grasser, et al., 2011). These defects are completely discharged when the stress bias is removed (Zhi Qiang Teo et al., 2010). However, the discharge process was highly dependent on time in which the relaxation phase dynamics was slower for

thicker SiO_2 IL. This dependence may be ascribed to slow charging kinetics of the defects in thicker SiO_2 IL, as highlighted previously.

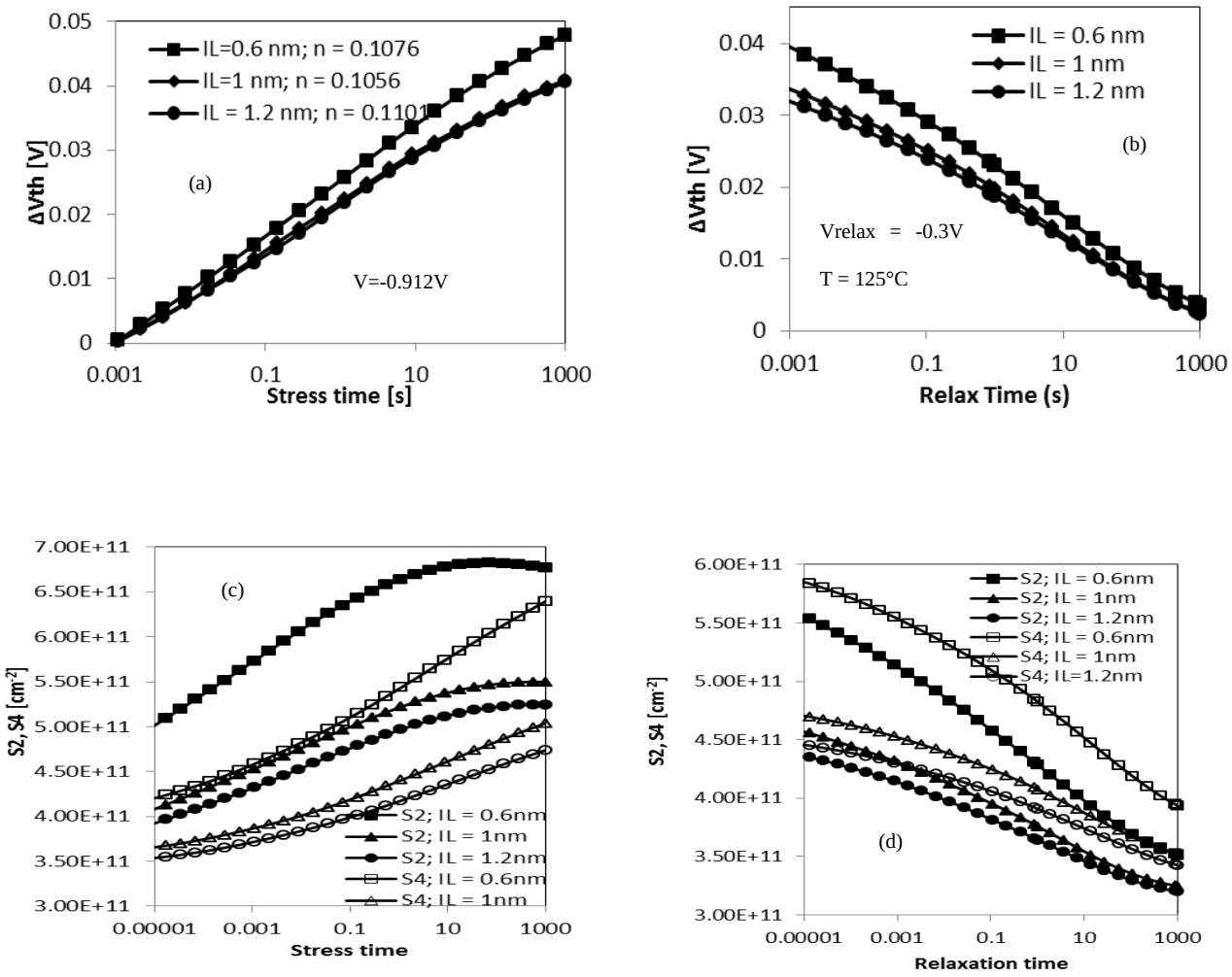


Figure 4.18 Threshold voltage shift for different SiO_2 IL thickness during the (a) stress phase and (b) relaxation phase as a function of stress and relaxation time, respectively. Time evolution of hole trap density, S_2 and interface trap density, S_4 for different SiO_2 IL thickness during the (c) stress phase and the (d) relaxation phase as a function of stress and relaxation time, respectively

4.3.3.3 Effects of gate stack sub-layer physical thickness on recoverable component

Figure 4.19 (a) shows the evolution of dynamic NBTI as a result of a simulated stress and relax cycle. The hole trap transformation can be further explored by analyzing the $|\Delta Vt|$ recovered per cycle, *R*, as determined in the figure, by following the work in (Boo & Ang, 2012). As shown in Fig. 7b, *R* is a function of stress temperature for devices with variation in HfO_2 dielectric layer and SiO_2 IL thicknesses. The relationship obtained between R and stress temperature, as illustrated in Figure 4.19(b), suggested that the hole transformation was thermally activated. This activation occurred because during higher stress temperature, the hole trapping effect increased, which is in agreement with (Boo & Ang, 2012). A closer observation indicated that more recoverable component can be observed in thinner SiO_2 and HfO_2.

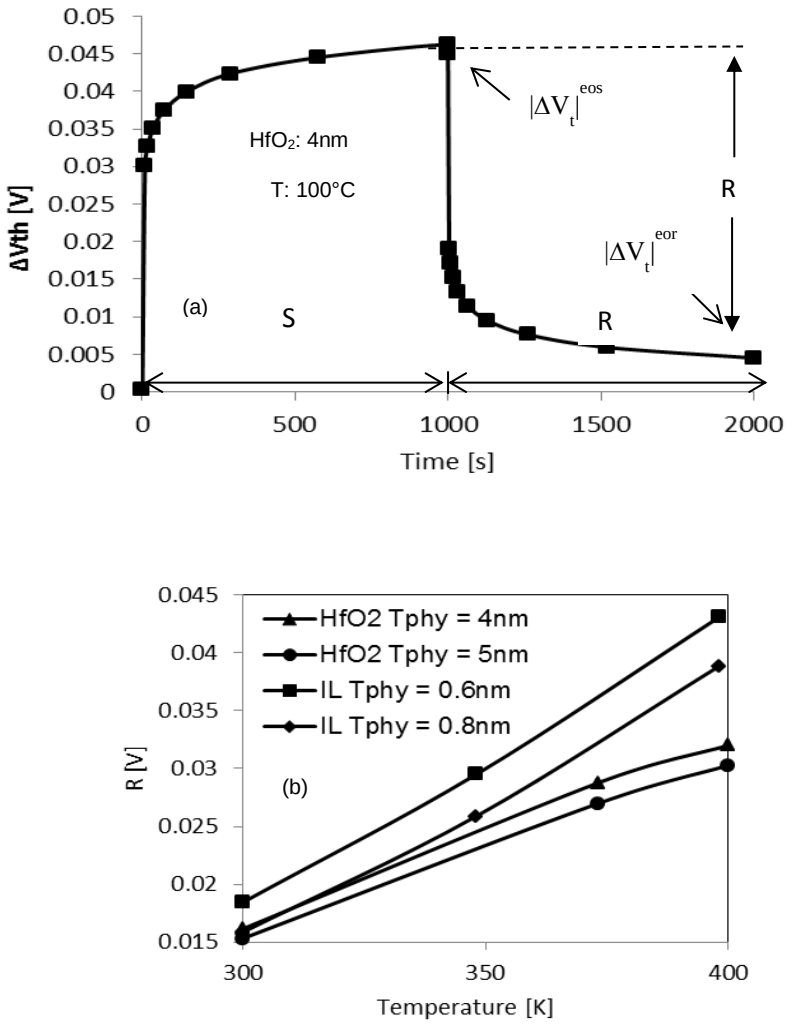


Figure 4.19 (a**) Evolution of** ΔVth **and definition of recovery component,** R **in a typical dynamic NBTI cycle and (**b**)** R **as a function of stress temperature**

4.3.4 High-k process integration issue with NBTI Degradation under Non-hydrogen Transport formalism

This section discusses the influence of related reliability issues in the gate insulator processing in high-*k* metal gate devices namely, the oxygen vacancy precursor and dipole charge. The effects of different densities of oxygen vacancy precursors and dipoles on the NBTI degradation are also explained. This study was conducted for PMOSFETs with varied thicknesses of dielectric layers.

4.3.4.1 Correlation of gate stack sublayer physical thickness and oxygen vacancy precursor concentration on NBTI

Figure 4.20 (a) and (b) illustrate the *Vth* shift kinetics according to the density of precursors. This study has been conducted on PMOSFET devices with varied thicknesses of the SiO_2 interface and HfO_2 layers. All devices in both figures show that the degradation occurred more in the case with high density of precursor. Higher degradation was observed during higher stress temperature for all devices. As stated, the oxygen vacancy precursor in the oxide can significantly generate the hole trap in the oxide upon the application of stress bias. Higher density of oxygen vacancy precursor led to more hole traps in the oxide, which enhances the degradation level.

Contrary to the enhanced degradation upon scaled SiO_2 interface layer thickness in the previous discussion, Figure 4.20 (a) shows a different result. The thicker SiO_2 interface layer has led to more degradation under higher applied stress voltage. This degradation could be attributed to the higher amount of hydrogen available in thicker SiO_2 interface layer (D S Ang et al., 2011). In the two-stage NBTI model, the positively charged E' center can attract the H from P_bH, thereby creating the dangling bond at the interface (T. Grasser et al., 2009a, 2009b). Higher stress voltage produced more positively charged E' centers and can therefore attract more H which subsequently created more dangling bonds at the interface. In Figure 4.20 (b), the increased trapping occurred at pre-existing defects in thicker high-k which was similar to what has been observed in the previous section. For the fixed SiO_2 interface layer, a similar number of H took part in the degradation mechanism for each device, which further proves that the occurrence of degradation increased in the trapping process in pre-existing defect. Thus, more positively charged E' centers were created for thicker HfO_2 dielectric upon the application of higher stress voltage. As indicated

in Figure 4.20 (b), severe NBTI degradation for device with 5 nm HfO_2 thicknesses occurs at higher stress voltage, such that this device experiences more than 10% *Vth* shift for the oxygen precursor of 5×10^{12} cm^{-2} at room temperature and higher. Devices with thinner HfO_2 in Figure 4.20 (a) exhibited less than 10% *Vth* shift for oxygen precursor of 5×10^{12} cm^{-2} at higher stress voltage application. It can then be concluded that the optimization of HfO_2 thickness was important to minimize the NBTI degradation effect. The density of the oxygen precursor should be approximately 1×10^{12} cm^{-2} or less for devices with HfO_2 thicknesses of 4 nm and 5 nm to ensure a *Vth* shift of not more than 10% during the specified stress duration. The severe degradation observed in high-*k* metal gate devices with thicker high-*k* dielectric implies that the defect mechanisms were more significant in the oxide bulk as compared to the interface between oxide and substrate.

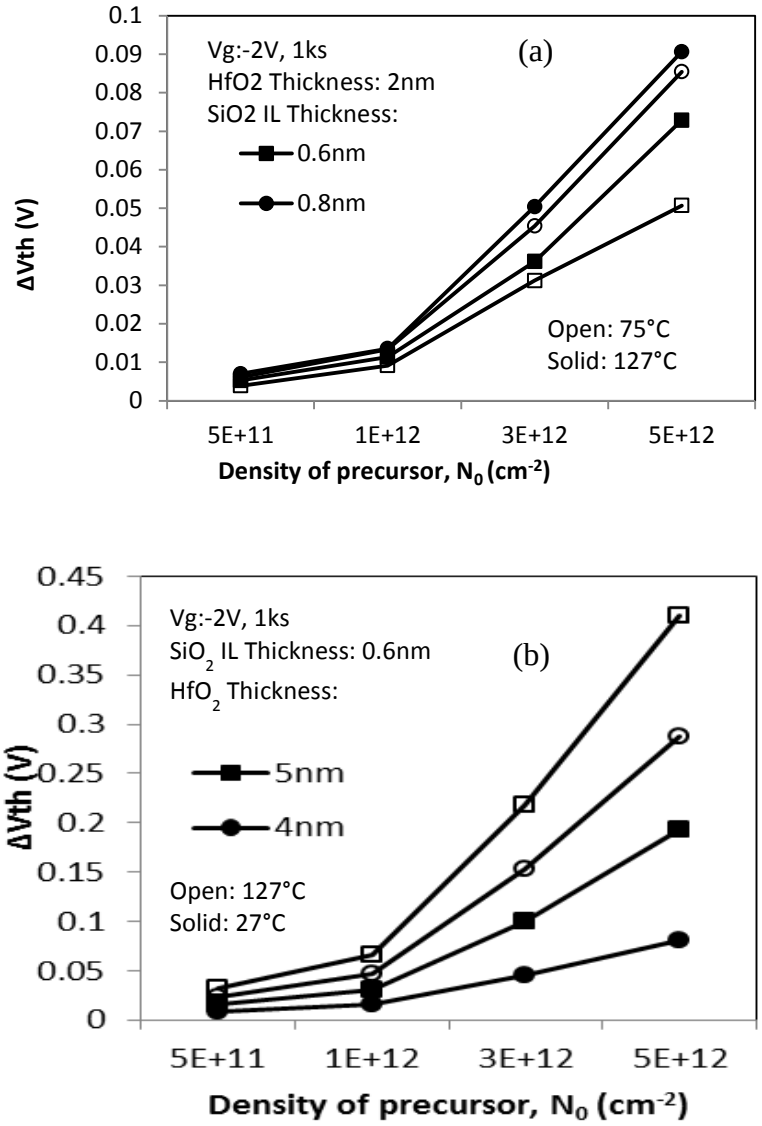


Figure 4.20 Evolution of threshold voltage shift based on different densities of precursor. (a**) Variation in thicknesses of SiO_2 with thickness of 2 nm HfO_2. (**b**) Variation in thicknesses of HfO_2 with thickness of 0.6 nm SiO_2 interface layer**

In Figure 4.21 (a) and (b), the hole and interface trap densities (S_2 and S_4) are shown as a function of density of the precursor for devices with thinner and thicker HfO_2 respectively under a different stress temperature. The first impression on the number of hole trap density, S_2 and interface trap density, S_4 in both graphs is that the defects increased as the density of oxygen vacancy precursor increases. However,

closer observation indicated that the dependence of the generated hole trap density, S_2 and interface trap density, S_4 on temperature contradicted with a different thickness of HfO_2. For devices with thinner HfO_2, the generated positively charged E' centers were insensitive to stress temperature. The hole trap density, S_2 was larger at room temperature and decreased as the stress temperature increased after 1,000s stress. As the thinner HfO_2 has less trapping in the bulk high-*k* layer (Neugroschel et al., 2006), the reduction in the generated hole trap density at higher stress temperature could be observed. This reduction is due to the transformation of the hole trap density, S_2 into the interface trap density, S_4 in accordance with constant voltage stress measurement in (Boo et al., 2012). As shown in this study, the interface trap density, S_4 is considered as a permanent oxide trap. This transformation process can happen during an adequately long duration of *dc* NBTI stress (Boo et al., 2012). The reduction of generated trapped holes at higher stress temperature implied that a more permanent oxide trap was created after the 1,000s stress in accordance with the experiment. The thermally activated transformation of the hole trap density, S_2 into the permanent oxide trap was observed as more interface trap density S_4 could be created at higher stress temperature.

In contrast, for devices with thicker HfO_2, the higher degradation was observed as discussed in the previous section. This degradation could be attributed to the higher generated hole trap upon application of bias resulting from fast transient charging effect (Neugroschel et al., 2006). Thus, the transformation of the permanent hole trap has an increased probability of occurrence. The generated interface trap density, S_2 at room temperature was considerably smaller than the generated interface trap density, S_4 at higher temperature.

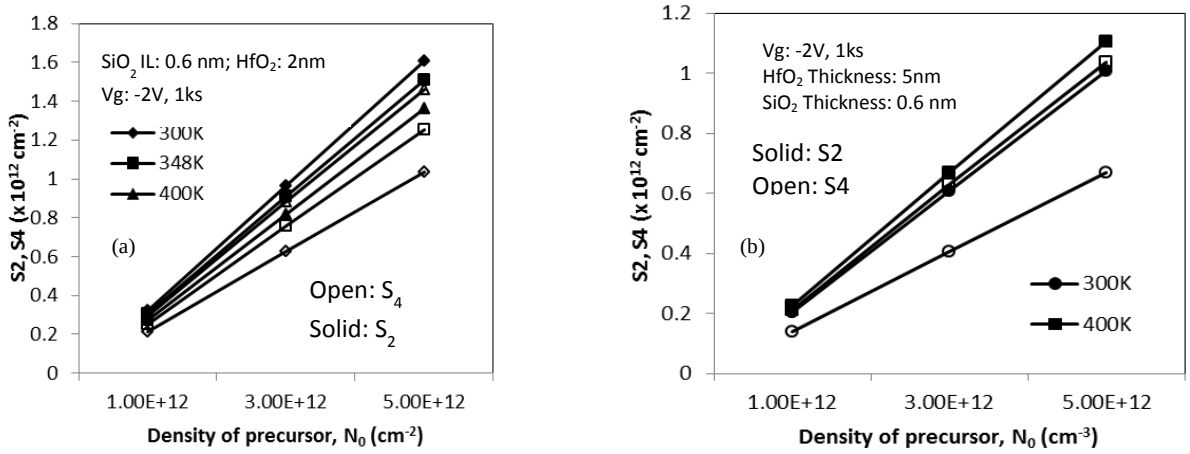


Figure 4.21 Hole trap density, S_2 and interface trap density, S_4 as a function of density of precursor under a different stress temperature for (a) thin HfO_2 and (b) thick HfO_2

Figure 4.22 (a) and (b) show the time evolution of hole and interface trap densities (S_2 and S_4) based on a different number of precursors for thin HfO_2 and thick HfO_2 layers respectively. A thinner HfO_2 layer shows that at high density of the precursor, the degradation was more prominent for interface traps than with those in bulk oxides as stress time increases. This degradation is because more interface trap density, S_4 than the hole trap density, S_2 was created. In contrast, for a thicker HfO_2 layer, the hole trap density, S_2 is greater than the interface trap density, S_4 within the specified stress time. Therefore, this greater density further confirms that a thicker HfO_2 layer contributed to increased degradation and the occurrence of the degradation was more prominent in the oxide bulk. Closer observation indicated that during the earlier stress time, the degradation kinetics occurred more often in the oxide bulk, as the hole trap density was more than the interface trap density. At shorter stress times, the number of precursors, which influences the degradation contributed more to the degradation of the thinner HfO_2 layer. This is attributed by the higher number of precursors, which increased the number of holes that can be trapped upon the application of stress bias. This increase in turn enhanced the creation of interface trap density, S_4 as explained by the two-stage model mechanism (T. Grasser et al.,

2009a, 2009b). In contrast, with regard to the thicker HfO_2 layer, the higher number of precursors led to a longer stress time needed for the interface trap density, S_4 to influence the degradation mechanism further. This appearance can be explained with regards to the influence of different thicknesses of HfO_2 layer deposited on a similar thickness of SiO_2 interface layer as discussed in (Bersuker et al., 2006). More oxygen vacancies were generated at the SiO_2/Si interface and in the bulk IL for thicker HfO_2, as observed in the experimental work. It can be concluded that for the thicker HfO_2 layer, more oxygen vacancies were available; thus, the higher defined number of precursors significantly influenced the degradation mechanism. As a result, greater hole trap density, S_2 than interface trap density, S_4 occurred throughout the specified stress time. This occurrence resulted in more degradation in the bulk oxide than in the interface region.

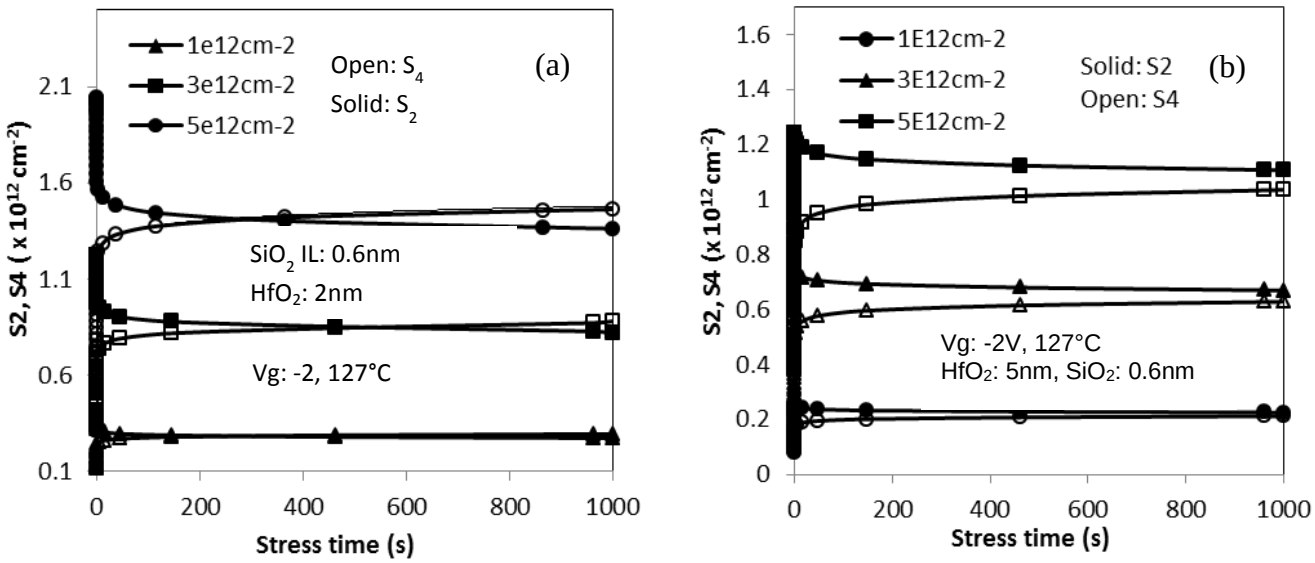


Figure 4.22 Time evolution for hole trap density, S_2 and interface trap density, S_4 for a different number of precursors. (a) Thin HfO_2 and (b) thick HfO_2

4.3.4.2 Correlation of scaled SiO_2 interface layer physical thickness and dipole layer on NBTI

This section highlights the relationship between dipole surface density and the NBTI degradation effect. The two-stage NBTI model is further used to explain the NBTI degradation effect with the influence of dipole surface density. For a similar stress bias condition, the higher dipole surface density influences the threshold voltage shift more than the lower dipole surface density as depicted in Figure 4.23 (a). Dipole charges formed between the SiO_2 IL and HfO_2 layers produced electrostatic potential that can influence the dynamic behavior of the hole and interface trap densities (S_2 and S_4), as indicated Figure 4.23 (b). The occurrence of the degradation mechanism was not influenced by the change in dipole surface density. The degradation was more significant in the oxide bulk than in the interface region. To investigate the effects of different dipole surface densities on varied SiO_2 IL thicknesses, the hole and interface trap densities are plotted after the 1,000s stress, as shown in Figure 4.23 (c). Higher density of the hole trap, S_2 was observed for higher dipole surface density in thinner SiO_2 IL. Similarly, the density of the interface trap, S_4 was also higher when the dipole surface density is higher.

For devices with thin and thick SiO_2 interface layers, more pronounced degradation was observed in the oxide bulk as the hole trap density, S_2 is higher when the dipole layer is smaller. Figure 4.23 (c) shows that for a larger dipole layer, the location of the degradation mechanism is different for devices with thin and thick SiO_2 interface layers. For thinner SiO_2 interface layers, the degradation mechanism occurred more in the interface, whereas for thicker SiO_2 interface layers, the degradation mechanism occurred slightly more in the oxide bulk.

One of the possible explanations for the relationship between the threshold voltage shift and the dipole layer effect could be the effect of the dipole on channel mobility. The channel mobility decreases with thinning SiO_2 IL because of remote scattering that occurred as a result of high-*k* phonon scattering and coulomb scattering caused by oxide charges in the high-*k* layer (Miyata, 2012). In principle, in the bi-layer structure consisting of two dielectric materials with different conductivities, the charge trapping at the interface occurred as predicted in electromagnetic characteristics. Considering the existence of defects at the interface, it is strongly believed that these defects play an important role in the charge trapping. Therefore, the effects of dipole layer formation between the high-*k* and SiO_2 layers should be considered in assessing the NBTI degradation effect. However, the dipole layer formation strongly depended on the applied voltage and other charges between the gate and substrate, including ionized donors and acceptors. Therefore, specific measurement should be developed to characterize the influence of the dipole layer on the NBTI degradation.

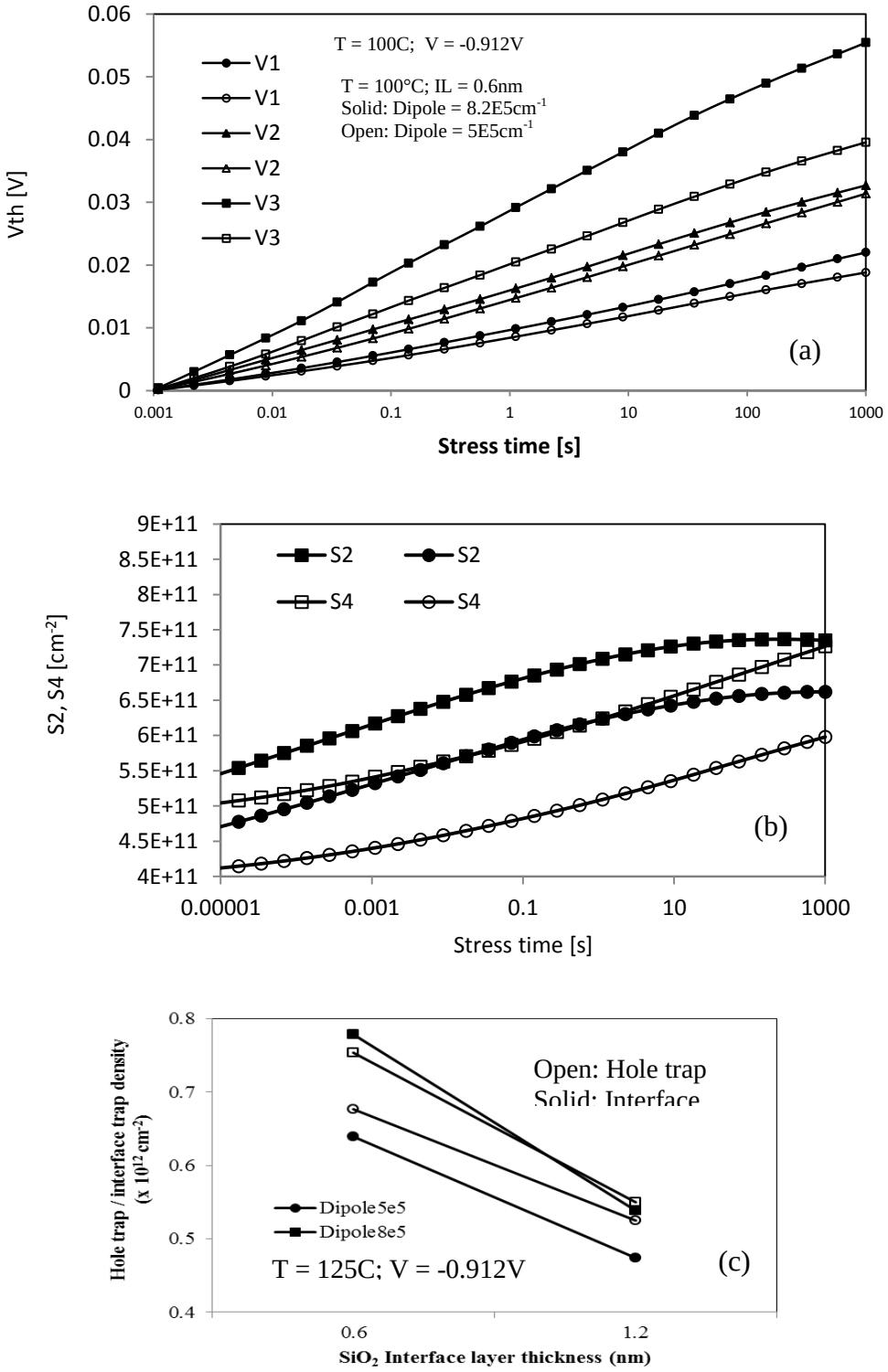


Figure 4.23 (a) **Threshold voltage shift (*V*1 < *V*2 < *V*3) and (b) time evolution of hole and interface trap densities because of the effect of different dipole surface densities. (c) Hole and interface trap densities in relation to different SiO_2 interface layer thickness for a different dipole layer**

4.4 Integration of Non-hydrogen Transport Formalism with Defects Based on Energy Profile Distribution

So far, this chapter has discussed the NBTI degradation effects based on the R-D model and the two-stage NBTI model for hydrogen and non-hydrogen transport formalism respectively. The NBTI based on R-D model was studied based on the interface trap contribution while the two-stage NBTI model was studied based on the contribution of positively charged E'centers and interface trap towards the degradation. The implementation of the two-stage NBTI model in the previous section was based on energy level of positively charged E'centers and interface trap below energy mid gap and 0.3 eV respectively.

In this section, the numerical simulation using Sentaurus TCAD was enhanced by developing the new simulation method in characterizing the NBTI degradation by implementing the energy profiling approach. The energy profiling approach is based on the probing of energy distribution of positive charges in the gate dielectric. The new simulation method will adopt the new defined energy level for each trap. Each of the energy level of the positive charges are defined accordingly (S. W. M. Hatta et al., 2013). Then, the NBTI degradation was studied based on this integrated new defined energy level for each traps. The energy probing simulation technique based on redefines energy level for each defect was then developed to accurately characterize the NBTI degradation on high-k based devices. The default energy level was simulated using the same device and stress condition for comparison. The validation of this redefined energy model was then compared against experimental data obtained by group (S. W. M. Hatta et al., 2013). The features of each charges contributed in the degradation was proven to be in agreement with the previous experimental works (S. W. M. Hatta et al., 2013, 2014; J.F. Zhang, 2009; Jian F Zhang et al., 2004; Ce Z.

Zhao et al., 2008). The continually growing advanced of sub-micron technology marks in the complex and varying structures of the high-k gate stacks. Therefore, several high-k based devices with varying EOT and different metal gate materials were demonstrated by applying the developed simulation technique to study the energy distribution of the different types of positive charges present in the Hf-based devices with different gate stacks.

Following this, the energy probing simulation technique developed in this chapter was applied to the single layered devices which consist of conventional SiO_2 dielectric device and conventional SiO_2 dielectric device with strained SiGe channel technology to further validate the applicability of this simulation technique across variant of device technology. The simulation result by applying this technique is shown in the 3D FinFET device as to demonstrate the applicability of this approach for advanced device design.

The accuracy of lifetime prediction for the devices was compared by applying default and integrated new energy level approaches. Besides that, the vulnerability of CMOS inverter to NBTI was investigated in a mixed-mode simulation. This is by considering that the stress conditions were executed on the p-MOSFET when $V_{in} = V_{low}$. The NBTI effect was limited in this study as the effect of degradation was analyzed due to positively charged generated defects based on this new approach. The shift of switching point of CMOS inverter based on default and integrated new energy levels was further analyzed to understand the limitation of the default energy level. Different precursor concentration to study the influence of pre-existing defects on the degradation level which ranging from 1 x 1 0^{12} cm^{-2} to 8 x 10^{12} cm^{-2} was then used.

The precursor known as oxygen vacancy defect acted as pre-existing defect (Gupta et al., 2012; Zhi Qiang Teo et al., 2010).

4.4.1 Simulation Framework Using Energy Profiling Technique

This sub-section will explain how the justification was made for defining the energy level of each traps and the technique developed to produce the energy distribution of the positive charges.

4.4.1.1 Profile energy distribution definition

The energy level of each traps were defined by referring to the energy distribution of positive charges as demonstrated in (S. W. M. Hatta et al., 2013). The Two-stage NBTI model consisting of precursor, E'centers and E'center/Pb H complex were adopted in the simulation (T. Grasser et al., 2009a; Gupta et al., 2012; "Suite, Sentaurus TCAD," 2011). The comparison of integrated new defined energy level in this work with literature is shown in Table 4.2.

NBTI simulation accuracy is validated by assessing the trap concentration upon application of wide range of stress biased, the resulting time exponent, trap density and the surface potential during stress and recovery phase. The device was stressed at 125°C K for 10 ks as had been demonstrated in most experimental work (S. W. M. Hatta et al., 2013).

Table 4.2 Defect charges and the energy levels

	Defect charges	Energy Levels	Literature	
			Defect charges	Ref.
Energy profiling approach	Precursor	Below Ev	AHT	(S. W. M. Hatta et al., 2013, 2014; J.F. Zhang, 2009; Jian F Zhang et al., 2004; Ce Z. Zhao et al., 2008)
			Precursor	(Goes et al., 2009; Gupta et al., 2012)
	E'center	Within bandgap	CPC	(S. W. M. Hatta et al., 2013, 2014; J.F. Zhang, 2009; Jian F Zhang et al., 2004; Ce Z. Zhao et al., 2008)
			Switching Oxide	(Zhi Qiang Teo et al., 2010)(T. Grasser et al., 2009a)
	E'center/ Pb H Complex	Beyond Ec	ANPC	(S. W. M. Hatta et al., 2013, 2014; J.F. Zhang, 2009; Jian F Zhang et al., 2004; Ce Z. Zhao et al., 2008)
			DLHT	(D.S. Ang & Wang, 2006; D.S. Ang et al., 2009)
Default ("Suite, Sentaurus TCAD," 2011)	Precursor	Below Ev	(Gupta et al., 2012; H. Hussin, N. Soin, M. F. Bukhori, 2014)	
	E'center	Ef – Ev = 0.3ev	(Gupta et al., 2012; H. Hussin, N. Soin, M. F. Bukhori, 2014; Schroder, 2007; "Suite, Sentaurus TCAD," 2011)	
	E'center/ Pb H Complex	Ef – Ev = 0.5ev	(Gupta et al., 2012; H. Hussin, N. Soin, M. F. Bukhori, 2014; Schroder, 2007; "Suite, Sentaurus TCAD," 2011)	

4.4.1.2 The simulation technique for energy distribution

First, the redefined energy level showed similar discharging characteristics as observed in experimental work (S. W. M. Hatta et al., 2013). A large variation of $V_{discharge}$ range enabled E_f to be swept from below valence band energy level, E_V to beyond the band gap above the conduction band energy level, E_C. The discharging time of 3000s under a given $V_{discharge}$ was used to ensure all the positive charges in dielectric below E_f are completely discharged (S. W. M. Hatta et al., 2013). The discharging characteristics based on default energy level is discussed and compared with the redefined energy level and illustrated in Figure 4.24 (a) and (b) respectively. The different discharging behaviour can be clearly seen in both figures. In Figure 4.24(a), the threshold voltage shift upon the discharging process is shown to be saturated with no further discharging effect after 3000s discharge time. On the other hand, the threshold voltage shift in Figure 4.24 (b) almost completely recover approaching 3000s discharge time for all different level of $V_{discharge}$. It can be explained here that the different behaviour was that in the redefine energy level, the E' center/Pb H complex is located above Ec. This contributed to permanent degradation known as ANPC observed in (S. W. M. Hatta et al., 2013). This positive charge that cannot be neutralized upon the application of positive bias is because of their energy level above Ec which makes it hard for the electron to reach them (S. W. M. Hatta et al., 2013). Unlike the default energy level where the P_b center is located below the energy mid-band gap where the behaviour is poorly recoverable, longer discharge time increased the potential of P_b center to recover which means full recovery was observed when approaching 3000s of the discharging time.

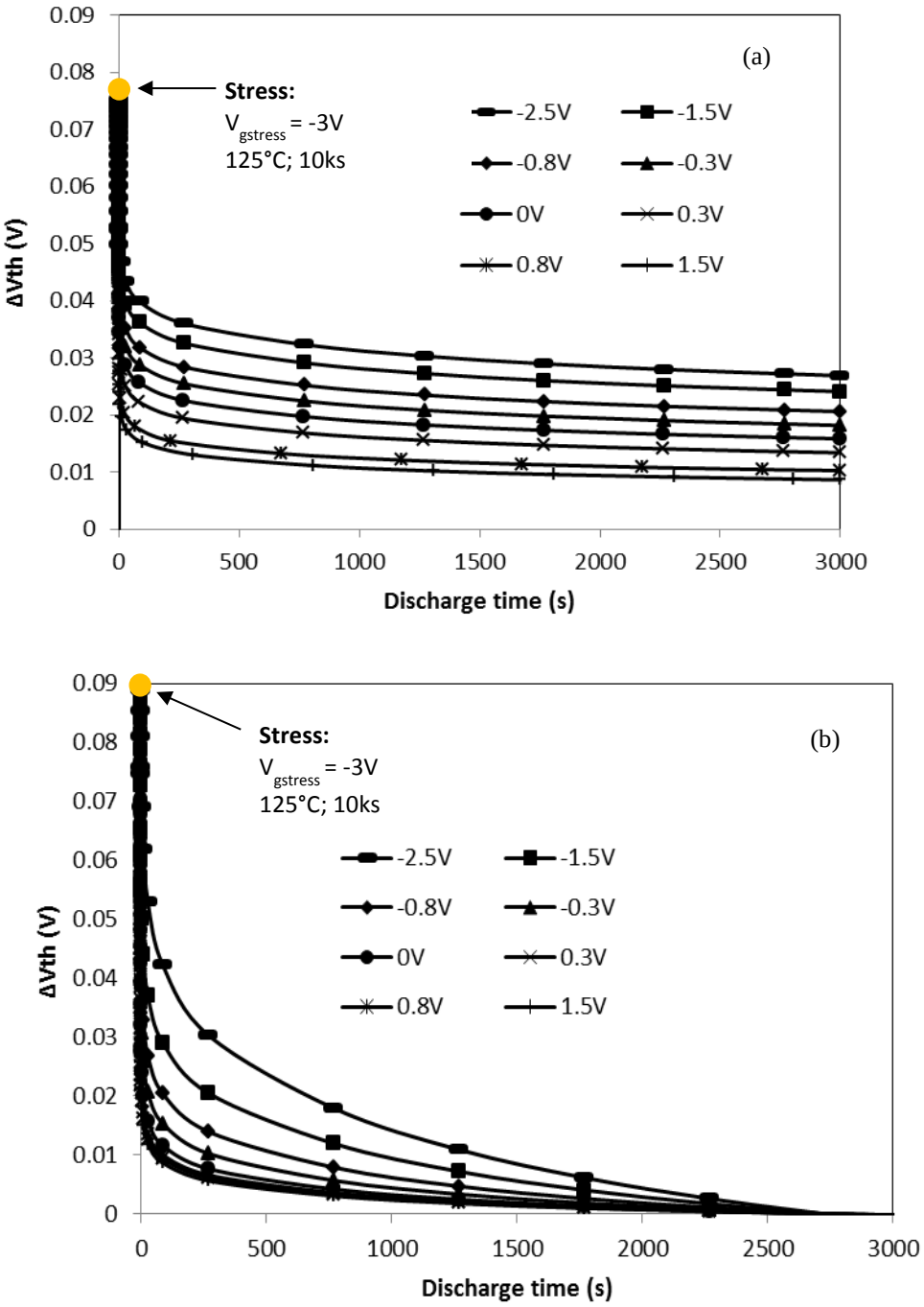
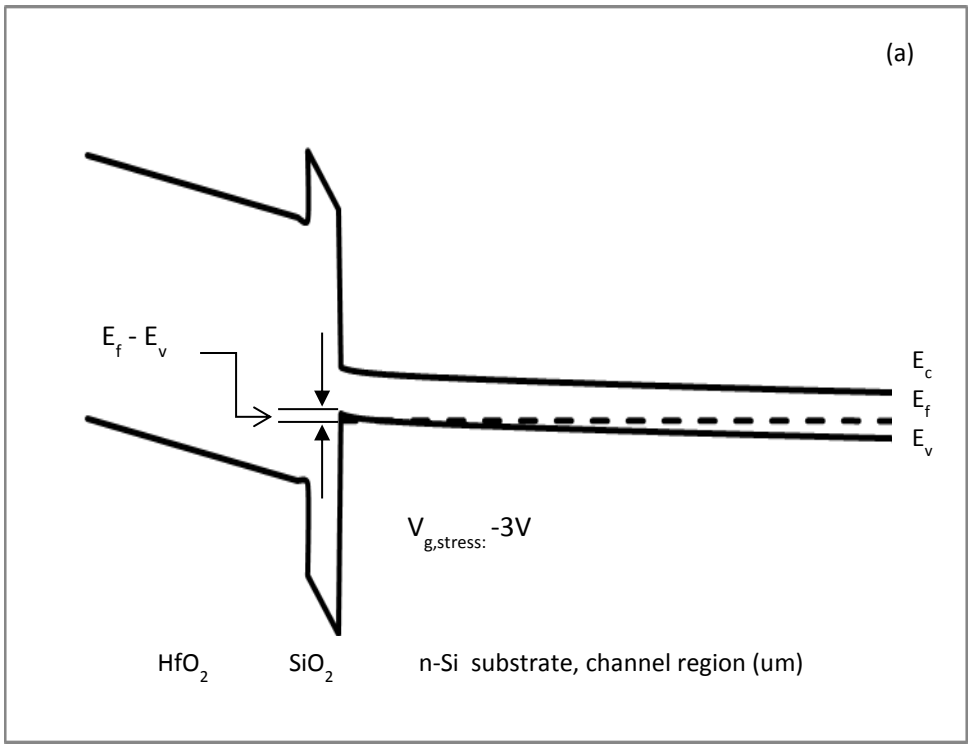
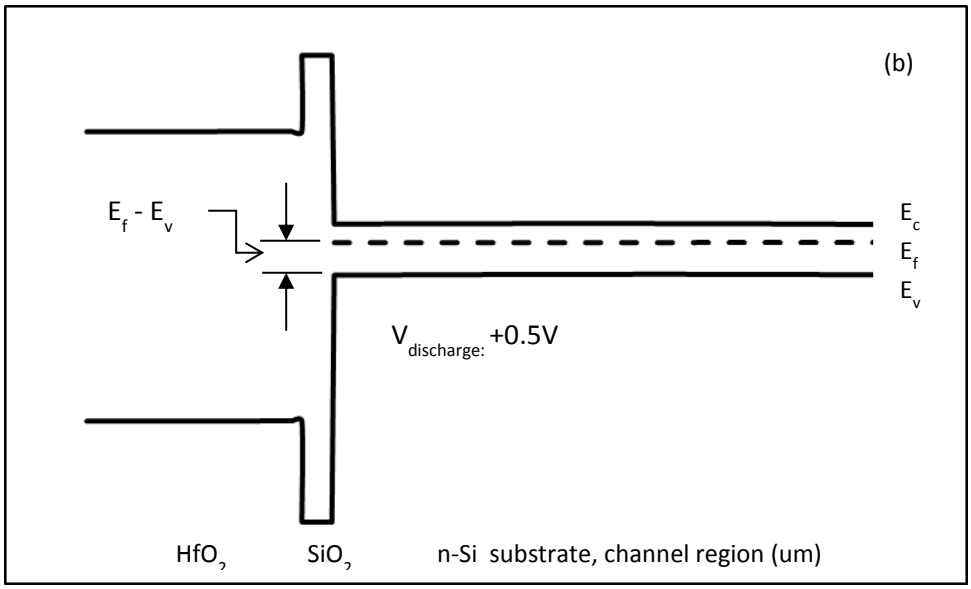


Figure 4.24 Typical discharging results under different Vdischarge (a) New redefine energy level (b) default energy level

Following this, the principle of extracting the energy distribution based on an energy band diagram obtained under different $V_{discharge}$ was highlighted.

Figure 4.25 (a), (b) and (c) show the energy band diagram under different $V_{discharge}$ to show that the E_f is swept from below E_v to above E_c as extracted from the device structure. At a given $V_{discharge}$, the E_f and E_v was extracted. The value of $E_f - E_v$ was then used to plot the total positive charges extracted from the simulation with respect to E_f - E_v as shown in Figure 4.26. Further details of the total positive charges will be provided to explain this.





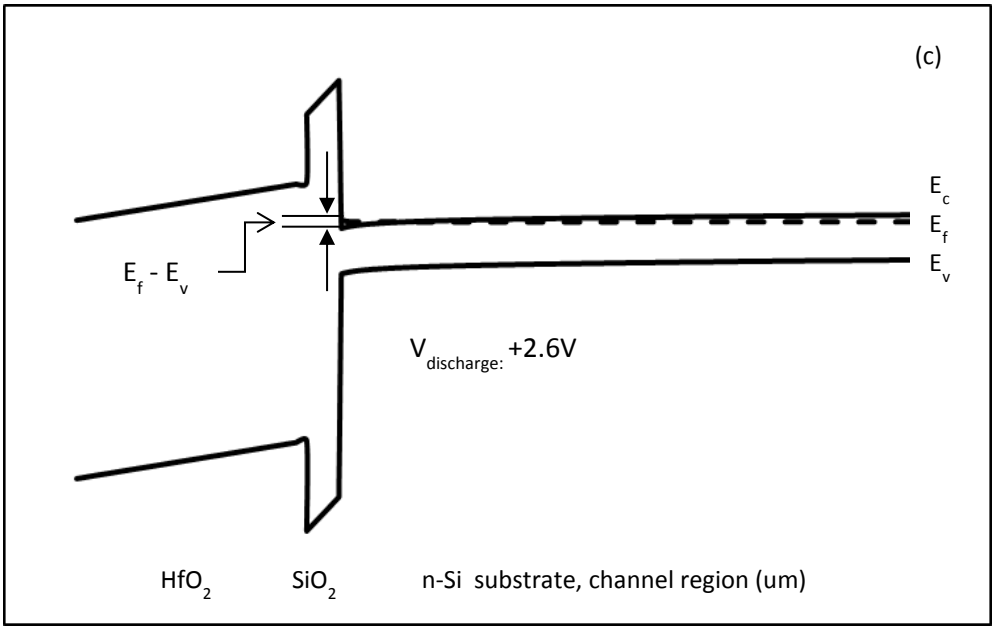


Figure 4.25 The energy band diagram to show the Ef is swept from below Ev to above Ec using different voltages (a) Ef - Ev < 0 with V_{stress} = -3 V, (b) Ef - Ev < 0 with $V_{discharge}$ = +0.5 V and (c) Ef - Ev > 0 with $V_{discharge}$ = +2.6 V

The total positive charges contributed in the degradation with respect to the $V_{discharge}$ and $E_f - E_v$ are shown in Figure 4.26 (a) and (b) respectively. It can be seen that the total concentration of positive charges for redefine energy level was higher than the default energy level. The percentage difference for total concentration of positive charges between the default and redefine energy level model is shown in Figure 4.26 (a).

As the simulation framework was based on the two-stage NBTI model, the total threshold voltage shift given by (T. Grasser et al., 2009a) is as the following:

$$\Delta V_{th}(t) = -\frac{\Delta Q_{ox}(t)+\Delta Q_{it}(t)}{C_{ox}} \quad (4.1)$$

Where the ΔQ_{ox} is the amount of positive charge stored in the E' center part of the complexes, the ΔQ_{it} is the amount of positive charge stored in the interface states.

The total positive charge, given in Figure 4.26 is the sum of total amount of ΔQ_{ox} and ΔQ_{it} which from here is referred to as effective charge density, N_{eff} as the distribution of each of the defects are defined according to their respective energy levels which has been thoroughly discussed previously. Following the definition by (T. Grasser et al., 2009a), the N_{ox} is the total number of oxide traps by all the defects not being in state 1 (the precursor state) is,

$$N_{ox}(t) = 1 - < f_1(t) > \quad (4.2)$$

Where the $<f_1(t)>$ is the probability defects in state 1. In this work, the precursor energy level is defined to be below E_v.

Hence, for the total threshold voltage shift in this work is,

$$\Delta V_{th} = -\frac{qN_{eff}}{C_{ox}} \quad (4.3)$$

Where the N_{eff} is the sum of positive charges with energy level below E_v, within and beyond the band-gap. The effective charge density, N_{eff} component will be known as AHT, CPC and ANPC by following the (S. W. M. Hatta et al., 2013, 2014). The validation of this proposition will be given in next section. This approach is validated against experimental data which highlighted that the positive charges in different energy regions originated from different defects (S. W. M. Hatta et al., 2013). By plotting the effective charge density, N_{eff} with respect to the different level of $V_{discharge}$ and E_f - E_v, the study on the energy profiling of positive charges can be further conducted.

The plot of total positive charges with respect to E_f –E_v as shown in Figure 4.26 (b) for redefine energy levels has almost similar behaviour as in (S. W. M. Hatta et al., 2013) but the default energy level was different. The default energy level where the interface trap was defined as below energy mid-gap, E_i has charge neutrality level acceptor-like above E_i and donor-like below E_i where the distribution of the interface trap was almost uniform in the band gap (Chang, Zhang, & Zhang, 2006; S. W. M. Hatta et al., 2013; J. F. Zhang, 1992). Thus, by introducing the new define energy levels for the component of effective charge density $N_{eff,}$ the contribution of each defect towards NBTI degradation was taken into account which was not previously observed (H. Hussin, N. Soin, M. F. Bukhori, 2014; H. Hussin, N. Soin, M. F. Bukhori, Y. Abdul Wahab, 2013; S. F. W. M. Hatta et al., 2010; Huard & Denais, 2004; V. Huard, C. Parthasarathy, N. Rallet, C. Guerin, M. Mammase, D. Barge, 2007; Wan Muhamad Hatta et al., 2011) . These early works only provided the information based on the recoverable and permanent component hence the threshold

voltage shift was only measured based on these two components. In addition to that, the permanent component was referred to the interface trap where the energy level is below the energy mid-gap.

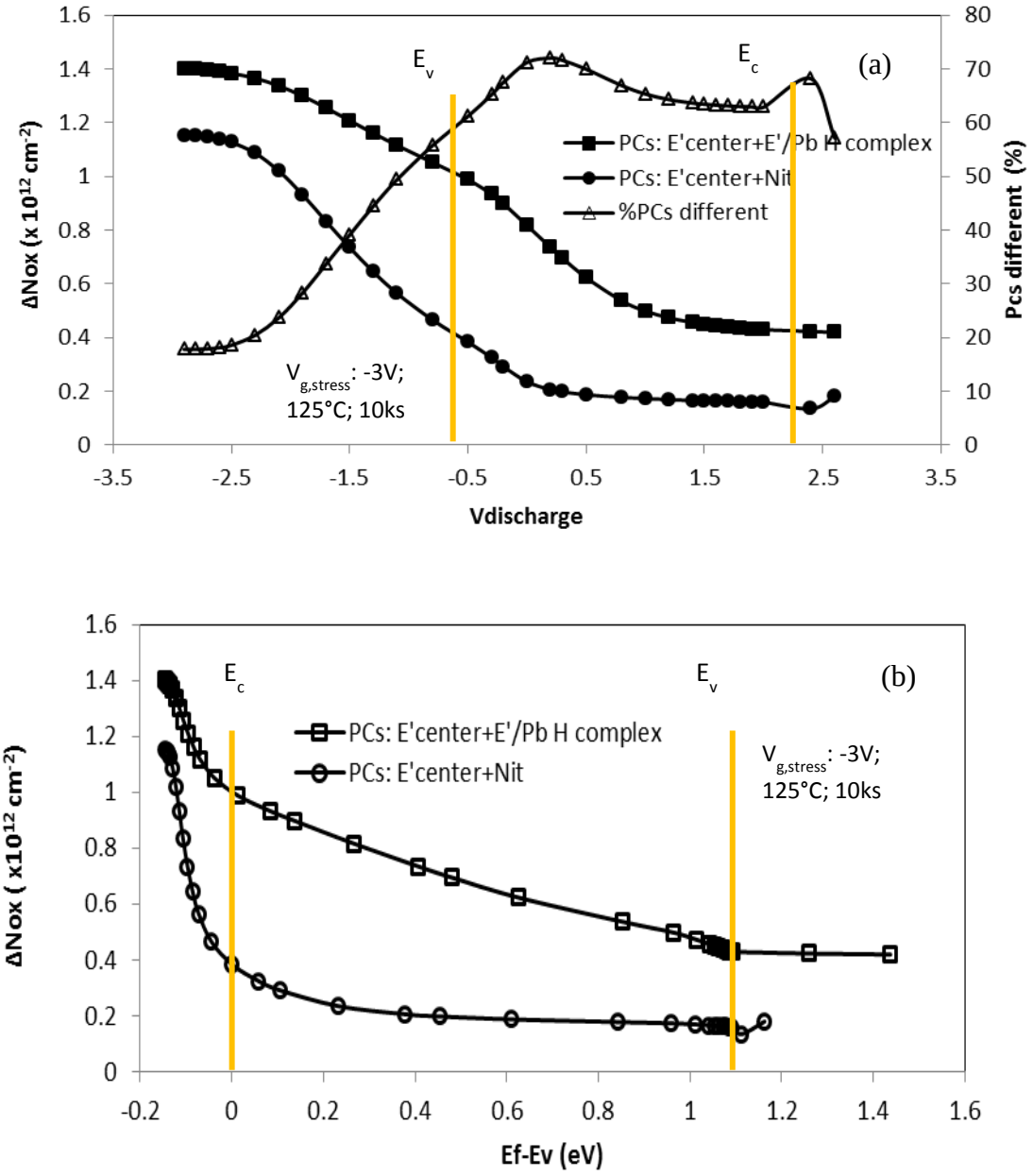


Figure 4.26 Total positive charges against (a) $V_{discharge}$ (b) E_f-E_v

Figure 4.27 shows the effective trap density as extracted from the simulation result. The plot for trapped carrier density versus energies was defined at the position of

SiO_2-Si substrate interface and probed near to the drain region. The resulting effective trap density was extracted for the case of default energy level and redefined energy level for high-k p-MOSFET as shown in Figure 4.27 (a) and (b) respectively.

The trap density for default energy level as shown in Figure 4.27 (a) was only distributed below Ei as the $E_f - E_v$ and defined to be 0.5 eV. Hence, it is further proven that the default energy level which only accounted for the interface trap and oxide trap with each energy levels defined below Ei reflected no contribution for positive charges located within and beyond the energy band-gap as observed in (S. W. M. Hatta et al., 2013, 2014). Another discrepancies on the default energy model is that the missing trap density for $E_f - E_v$ in range of 0 to -0.3 is observed. This is due to the energy level defined for the precursor is -0.3 to -0.5. Hence, $E_f - E_v$ between trap density between 0 to -0.3 are not accounted in the simulation. The proposed redefined energy level as shown in Figure 4.27 (b) provided the energy distribution of the trap density.

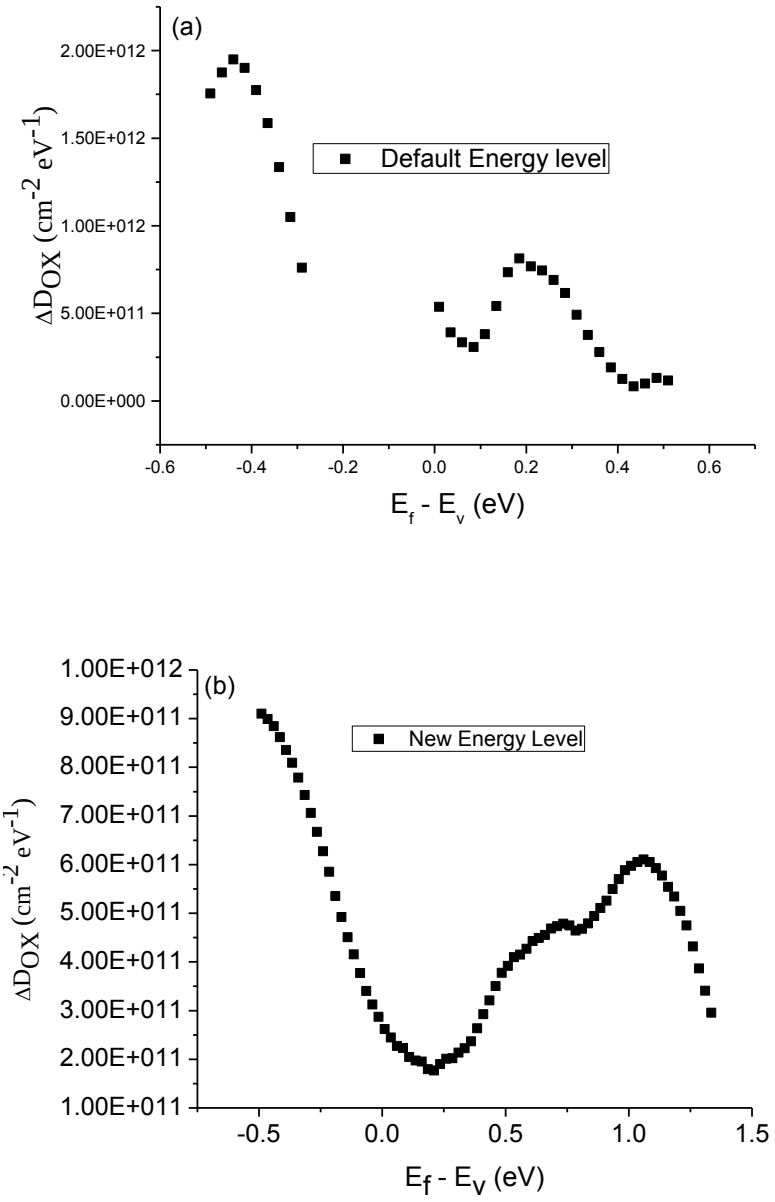


Figure 4.27 The resulting effective trap density is extracted from the case of (a) default energy level and (b) redefine energy level for higk-k p-MOSFET

4.4.2 Validation for Energy Profiling Approach

4.4.2.1 Different Types of PCs

For the redefine energy levels, the first impression of the plot in Figure 4.26 (a) and (b) indicated that the positive charges were sensitive to energy level and differed considerably over the energy range. Closer observations of the figures specified that the positive charges performed contrarily in different regions of $V_{discharge}$ and $E_f - E_v$. When E_f is below E_v where the $E_f - E_v < 0$, as shown in Figure 4.26 (b), the ΔN_{ox} initially dropped quickly hence contributing to a high trap density as shown in Figure 4.27(b). The significant high trap density below Ev in Figure 4.27 (b) suggested that large as-grown trap (AHT) existed in this device. The declining of ΔN_{ox}, however, slowed down abruptly around $E_f - E_v \sim -0.02$ eV, creating a plateau before reaching E_v, where the trap density becomes insignificant. This is in agreement with early works on HfO_2 based devices that suggested that the positive charges below E_v were AHTs and were easiest to discharge (S. W. M. Hatta, 2013). As compared to SiON dielectric devices, the created plateau is $E_f - E_v \sim -0.2$ eV (S. W. M. Hatta et al., 2013). The features of AHT resulting from this work will be further compared against experimental data in the next section.

When the $E_f - E_v > 0$ which was above Ev, the positive charges started to decrease again as shown in Figure 4.26 (b). However, the rate for the declining of positive charges above E_v was substantially lower than $E_f - E_v < -0.02$ eV. At a decreasing rate substantially slower as compared to below the E_v, significant peak near around Ev + 0.75 eV can be observed in Figure 4.27 (b) suggested CPC was energetically located within the band gap hence giving rise to the peak. This peak is almost similar to the observed peak in experimental work previously (Thomas Aichinger, Michael Nelhiebel, 2010)(S. W. M. Hatta et al., 2013).

Once above E_c, when the E_f reaches beyond E_c, the declining of positive charges become irrelevant which was almost constant hence resulting in a second plateau which can be observed in Figure 4.26 (b). Previous experimental works, (S. W. M. Hatta et al., 2013, 2014; J.F. Zhang, 2009; Jian F Zhang et al., 2004; Ce Z. Zhao et al., 2008) had suggested that the positive charges with energy levels above E_c were ANPC which were hard for the electrons to reach them and cannot be neutralized. For the existing model where the E'center/Pb H complex is defined below the energy mid gap, the positive charges were increased by means of the discharging process. This contradicted to the experimental data observed in (S. W. M. Hatta et al., 2013, 2014; J.F. Zhang, 2009; Jian F Zhang et al., 2004; Ce Z. Zhao et al., 2008) where the positive charges above E_c will slowly decrease or constant which means that they cannot be neutralized.

4.4.2.2 Effect of Stress Time

In Figure 4.28 (a) and (b), the first impression was that the positive charges increases as the stress time increased. Below the E_v, the positive charges became substantial and its energy trap density as shown in Figure 4.28 (c) which further confirms that the positive charges below E_v originated from the AHT. This was because the AHT essentially did not rise with stress time. On the other hand, the positive charges within and beyond the band gap increased as the stress time increases as shown in Figure 4.28 (a) to (c). The positive charges was confirmed to be CPC which was in agreement with (S. W. M. Hatta et al., 2013) because the CPC creation saturated after longer stress time (J.F. Zhang, 2009; Jian F Zhang et al., 2004; Ce Z. Zhao et al., 2008) as observed in Figure 4.28 (c).

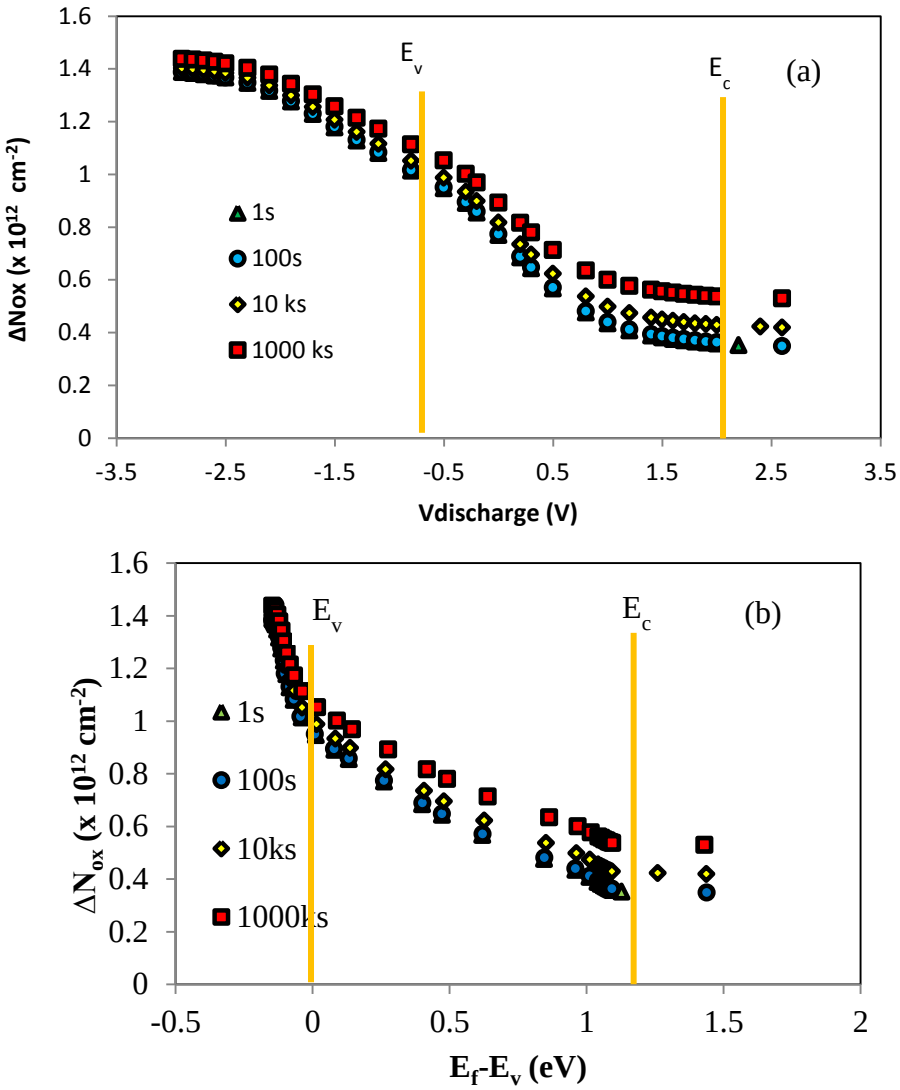


Figure 4.28 Effects of stress time on the trap energy distribution of positive charges. Device was stressed at -3 V at 125°C K for different stress time. The ΔN_{ox} was plotted against (a) $V_{discharge}$ (b) $E_f - E_v$ and the trap density in (c)

4.4.2.3 Effect of Stress Temperature

The results shown in Figure 4.29 (a), (b) and (c) are the positive charges effect with respect to $V_{discharge}$, $E_f - E_v$ and energy trap density respectively due to the different stress temperatures. The positive charges below E_v were insensitive to stress temperature hence further confirming that the positive charges below E_v originated from AHT as they were pre-existing defects (S. W. M. Hatta et al., 2013). The dependence of positive charges with respect to the variation of energy was further validated for positive charges within the energy band-gap region. After 10ks of stress time, the positive charges were insensitive to stress temperature as the stress time taken was sufficient for them to reach saturation even at room temperature. The feature of CPC which was insensitive to stress temperature is in agreement with previous experimental works (S. W. M. Hatta et al., 2013). A closer observation of positive charges above E_c indicated that the ANPC was substantially more for higher temperature with no saturation in agreement with previous works (S. W. M. Hatta et al., 2013; J.F. Zhang, 2009; Jian F Zhang et al., 2004; Ce Z. Zhao et al., 2008). The ANPC was confirmed to be a different type of defects since it was dependent on temperature and tend to increase for longer stress time as the creation was not saturated (S. W. M. Hatta et al., 2013).

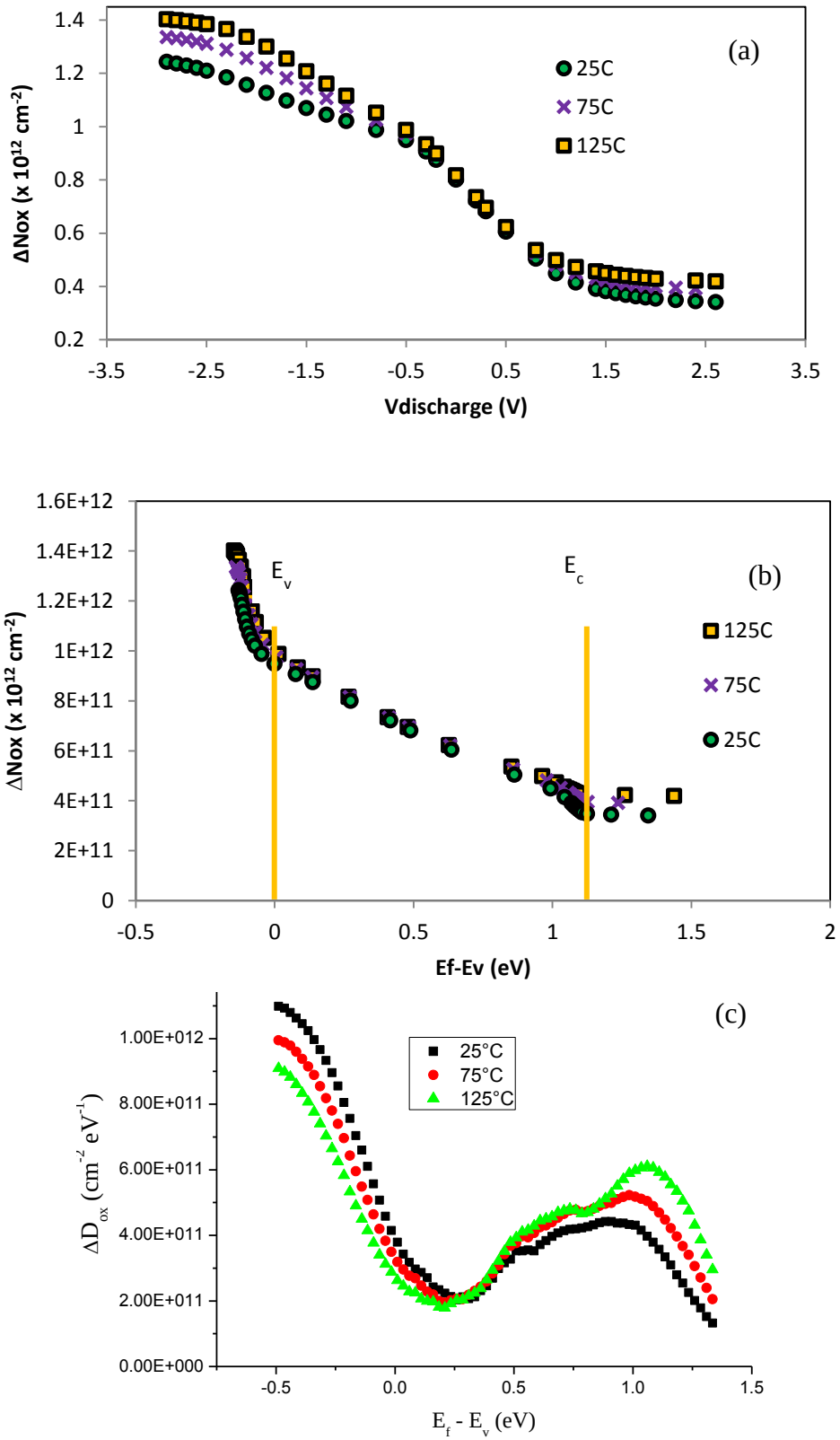


Figure 4.29 Effects of stress temperature on the trap energy distribution of positive charges. Device was stressed at -3 V at 125°C K for different stress time. The ΔN_{ox} was plotted against (a) $V_{discharge}$ (b) $E_f - E_v$ and the trap density in (c)

4.4.2.4 Comparison simulation with experimental data

To validate the simulation results based on the developed simulation technique for probing the energy distribution of positive charges, the simulation results with experimental data as in (S. W. M. Hatta et al., 2013) was compared. The comparison is made based on the trend between simulation and experimental data. Note that the testbed devices used in this work is different from devices in experimental data. This is due to the devices from experimental data is from a research group at Liverpool John Moores University. Hence, there are descrepancies between simulation and experimental results as we could not get all fabrication recipes of the transistors to be used in the simulation due to confidentiallity issues. The trend of the simulated results agreed with the experimental results although the magnitude was much smaller as depicted in Figure 4.30. It is shown that the numerical solution of the implemented two-stage NBTI model with a redefining energy level for each positive charges compared remarkably well with measured energy distribution of NBTI-induced PCs data. This was the first quantitative confirmation that the two-stage NBTI model with a redefines energy level of the PCs can capture the essential details of the energy distribution of the PCs, and therefore, would allow a microscopic study of the NBTI-induced PCs mechanism. All devices shown here were stressed at Eox ≈ -10MV/cm. Figure 4.31 shows the comparison of the Hf-stack simulated results as compared to the single layer SiON device. The magnitude of the trap density was more substantial in the Hf-stack device. This agreed with other works which reported that the Hf-stack devices had more defects and was prone to a higher NBTI effect as compared to single layered devices (S. W. M. Hatta, 2013).

Figure 4.30 shows a simulation trend which agrees with the experiment especially around the region below Ev. The trend followed very well even though the devices

were made up of different hf-based stacks. It can be observed that the ΔNox below E_v showed a sharp decrease as the device was discharged immediately after the stressing period. Figure 4.31 also shows a similar sharp reduction below the Ev when compared to the single layer SiON. The defect which plays a role below the E_v is suggested to be the as-grown hole traps (S. W. M. Hatta et al., 2013, 2014; J.F. Zhang, 2009; Jian F Zhang et al., 2004; Ce Z. Zhao et al., 2008).

The trend of the simulation results also agreed well with the experimental results within the band gap. The reduction continued even at a smaller reduction rate, that was not as steep as observed in below the E_v situations. This behaviour suggested the introduction of different type of defects. It has also been suggested that the generated CPC was the defect which plays a role within the bandgap (S. W. M. Hatta et al., 2013, 2014; J.F. Zhang, 2009; Jian F Zhang et al., 2004; Ce Z. Zhao et al., 2008).

There is a discrepancy of the data above E_c, which ANPC not agree very well with the experimental data. The simulated results showed that the trap density was not reduced to zero. It has been reported that the generated ANPC played a significant role in the region above E_c (S. W. M. Hatta et al., 2013, 2014; J.F. Zhang, 2009; Jian F Zhang et al., 2004; Ce Z. Zhao et al., 2008). The results suggested that the generated defects (ANPC) were higher in the case of the 0.85nm HfO_2/SiO_2 as compared to other experimental device which was eventually reduced to zero. This behavior was somehow different with the experimental data where the saturation of ANPC was observed. The saturation effect of ANPC was experimentally observed in early works (J.F. Zhang, 2009; Jian F Zhang et al., 2004; M. H. C. and J. F. Zhang, 2007) due to the fact that the occurrence of plateau was referred to the discharging process and was not significant anymore. It has been proposed that these positive charges were ANPC

as their energy levels were above E_c. Hence, the ANPC couldn't be reached by the electrons for neutralization process.

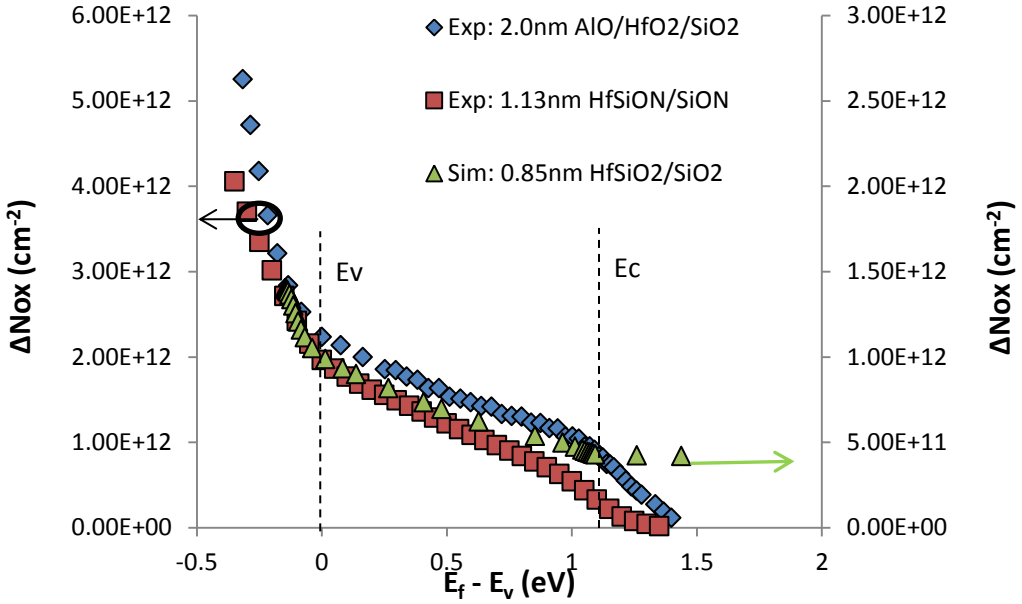


Figure 4.30 Simulation of HfSiO2/SiO2 compared with experimental data of Hf-based devices

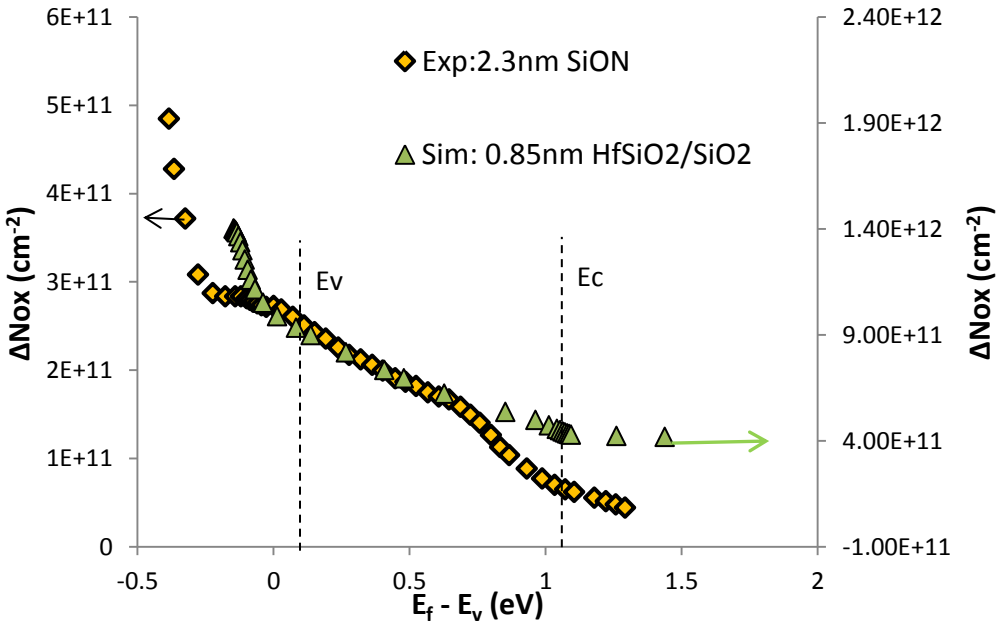


Figure 4.31 Simulation of HfSiO2/SiO2 compared with experimental data of single-layered device

The effective trap density, ΔD_{ox} is shown here for the different devices. Figure 4.32 shows a similar peak near E_c, which was believed to be due to the presence of Hf-based stack. Figure 4.33 shows a comparison of that with the single layered SiON, which can be seen that the peak near E_c was absent from the single layered device. Figure 4.33 shows that the decrease in the Dox below the E_v was much sharper for the single layered SiON. This may suggest that the as-grown hole traps discharges faster in the single layers SiON as compared to that in the Hf-gate stack devices. It can be speculated here that the defects may be easier to discharge in a single layer device where the trap is spatially distributed nearer to the bulk to which it is discharging to.

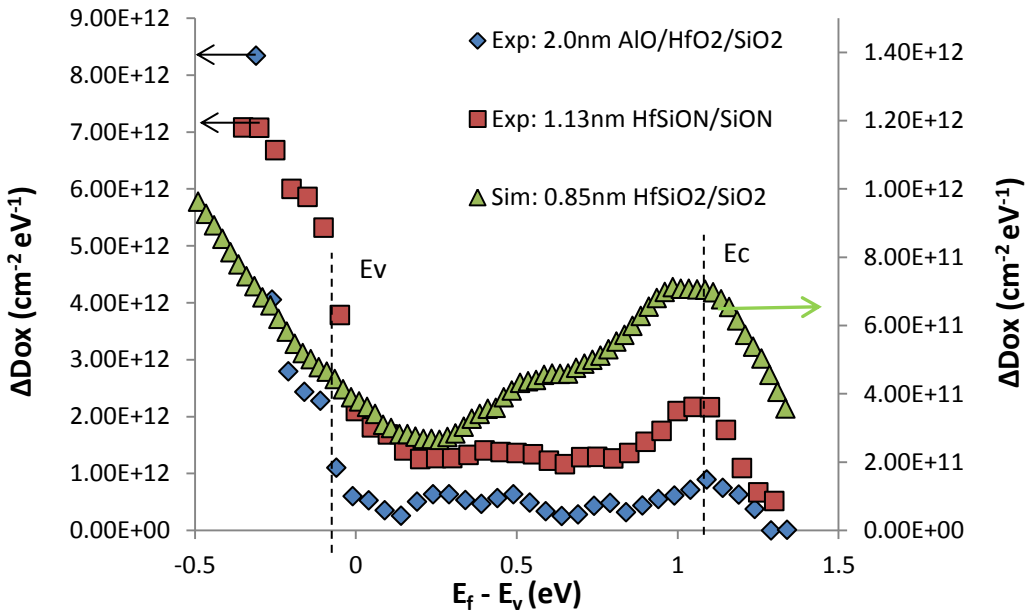


Figure 4.32 Comparison of effective trap density between simulated test bed device ($HfSiO_2/SiO_2$) with other experimental Hf-based devices

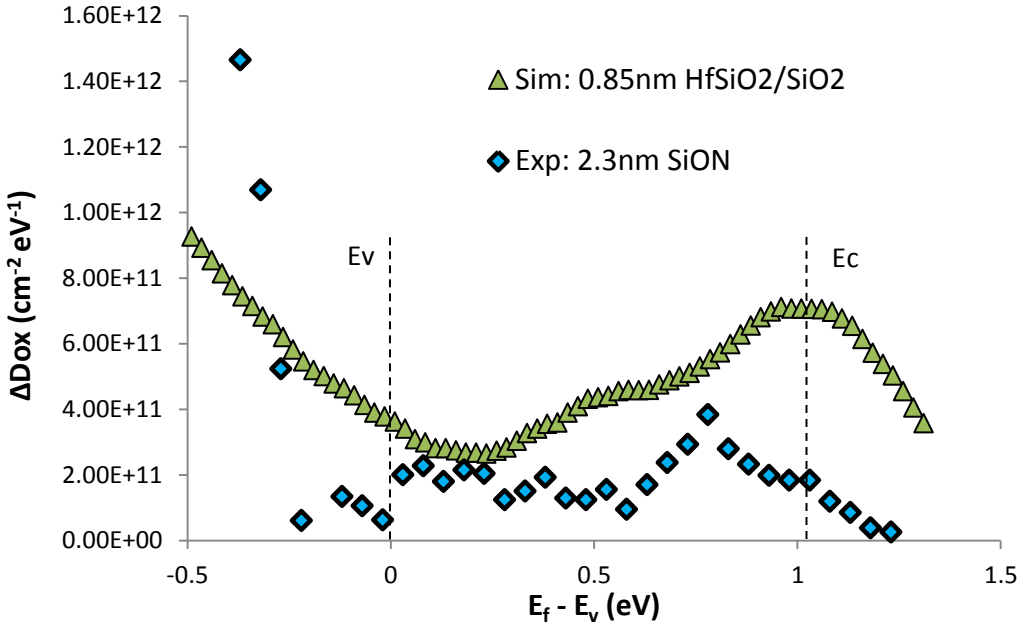


Figure 4.33 Comparison of effective trap density between simulated test bed device ($HfSiO_2/SiO_2$) with single-layered SiON device

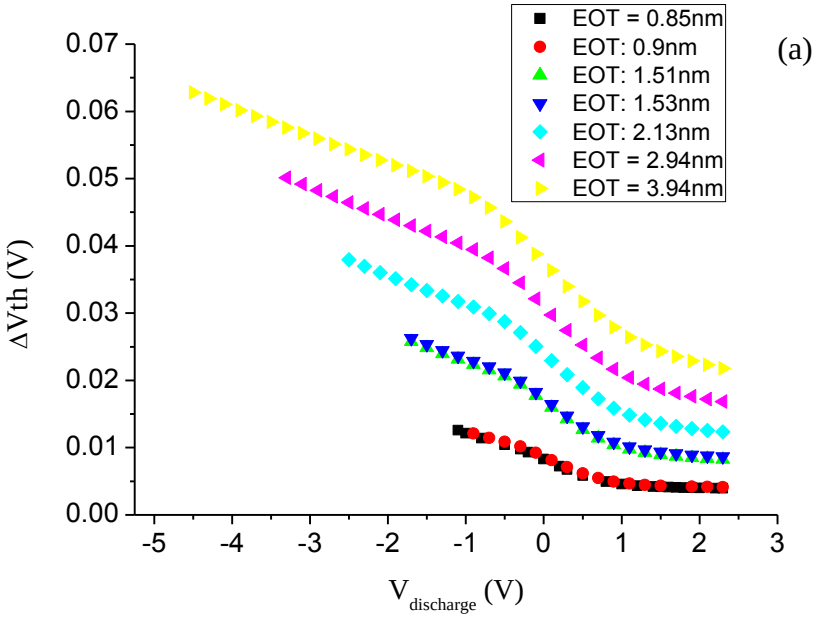
4.4.3 Application of the new simulation framework for different devices with high-k based

Upon validation of the new model of positive charges against the experimental data, the simulation technique for probing of energy distribution of positive charges using the profiling energy approach was implemented to study the energy distribution of positive charges in different effective oxide thickness (EOT) of high-k metal gate devices in this section. The energy distribution was then compared for different type of metal gate materials. In addition to that, the degradation characteristics for different structure of the high - k device based on the different stress conditions (gate bias, stress temperature and stress time) was also analyzed.

4.4.3.1 Energy distribution of positive charges in $TiN/HfO_2/SiO_2$ with varying EOT

The test bed device investigated in this sub-section is a $TiN\text{-}HfO_2\text{-}SiO_2$ device with varying effective oxide thickness (EOT). The range of EOT varied from 0.85 nm to 3.94 nm (S. W. M. Hatta et al., 2014). All devices have a width and length of 10 µm and 32 nm respectively. The devices were stressed at 12 MV/cm and the V_d applied for the measurement was -50 mV (Gao, Ang, et al., 2011; S. W. M. Hatta et al., 2013) while the stress time was set at 10 ks (S. W. M. Hatta et al., 2013, 2014) and the stress and discharge temperature was set at 125°C (S. W. M. Hatta et al., 2013).

Figure 4.34(a) presents the threshold voltage shift, ΔV_{th} that resulted from the discharging under different $V_{discharge}$. The ΔV_{th} was larger for thicker EOT as compared to thinner EOT throughout the $V_{discharge}$ applied. Further inspection on each of the EOT indicated that the thinner EOT generated the ANPC at smaller value of $V_{discharge}$ than thicker EOT. This observation was similar to the experimental work carried out by (S. W. M. Hatta et al., 2013, 2014) where the generation of ANPC was indicated by the saturation of threshold voltage shift. The values of respective ΔV_{th} due to the generated ANPC for each EOT are shown in Figure 4.34(b) which is the magnified view of (a).



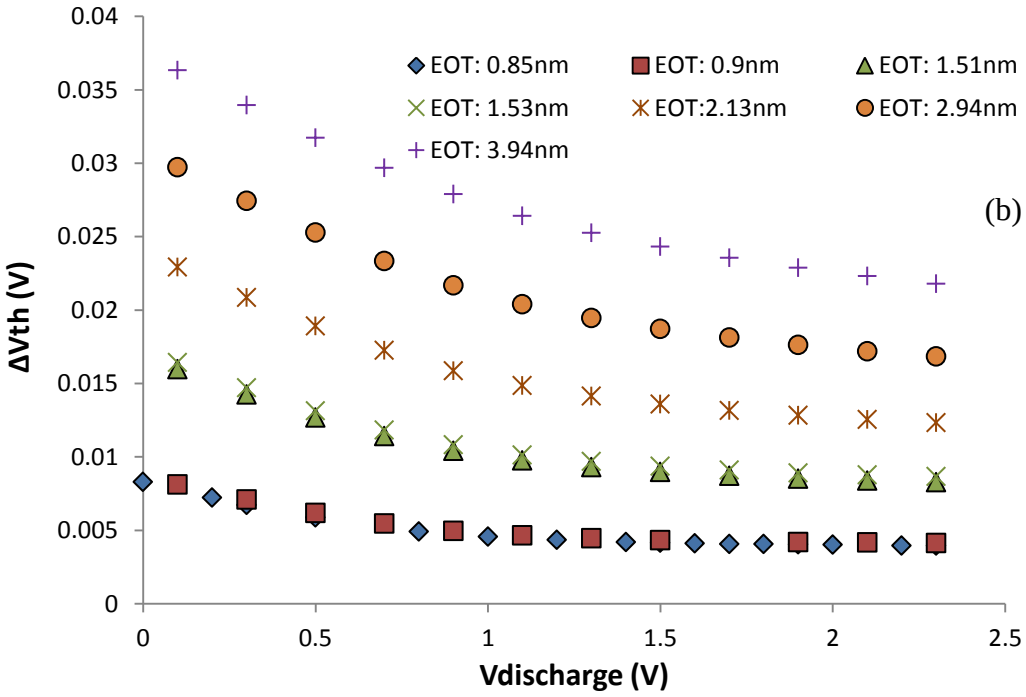


Figure 4.34 Threshold voltage shift for different EOT against $V_{discharge}$ for (a) entire $V_{discharges}$ applied (b) magnified view for $V_{discharge}$ within positive range

An examination of Figure 4.35 (a) and (b), indicated the profiles of the trap density against discharging voltages and surface potential respectively. Clear amount of trap density based on different EOT can be seen when plotted against the discharging voltages as compared to the surface potential. Based on the observation, the positive charges behaved qualitatively which was similar for all the EOTs. Below the E_v, for all the EOTs, the ΔN_{ox} will initially drop where as the $E_f - E_v$ increases, the ΔN_{ox} will also continuously drop for all EOTs. As observed in Figure 4.35 (a), the N_{ox} was clearly higher for thinner EOT but became smaller within and beyond the energy band gap. Below the Ev, the steep initial decline of the trap density ΔNox, became lesser when approaching Ef – Ev ~ 0 Ev similarly observed in (S. W. M. Hatta, 2013; S. W. M. Hatta et al., 2013, 2014). As discussed in (S. W. M. Hatta, 2013), the higher Nox below Ev did not reflect the number of hole traps for the thinner EOT below E_v for the case of SiON/Si. However, based on further observation on HfO2/SiO2 device in this work, the higher ΔNox below Ev reflected the number of hole traps for the thinner EOT. This was confirmed where the ΔD_{ox} was sensitive to the interface layer thickness below Ev as shown in Figure 4.36.

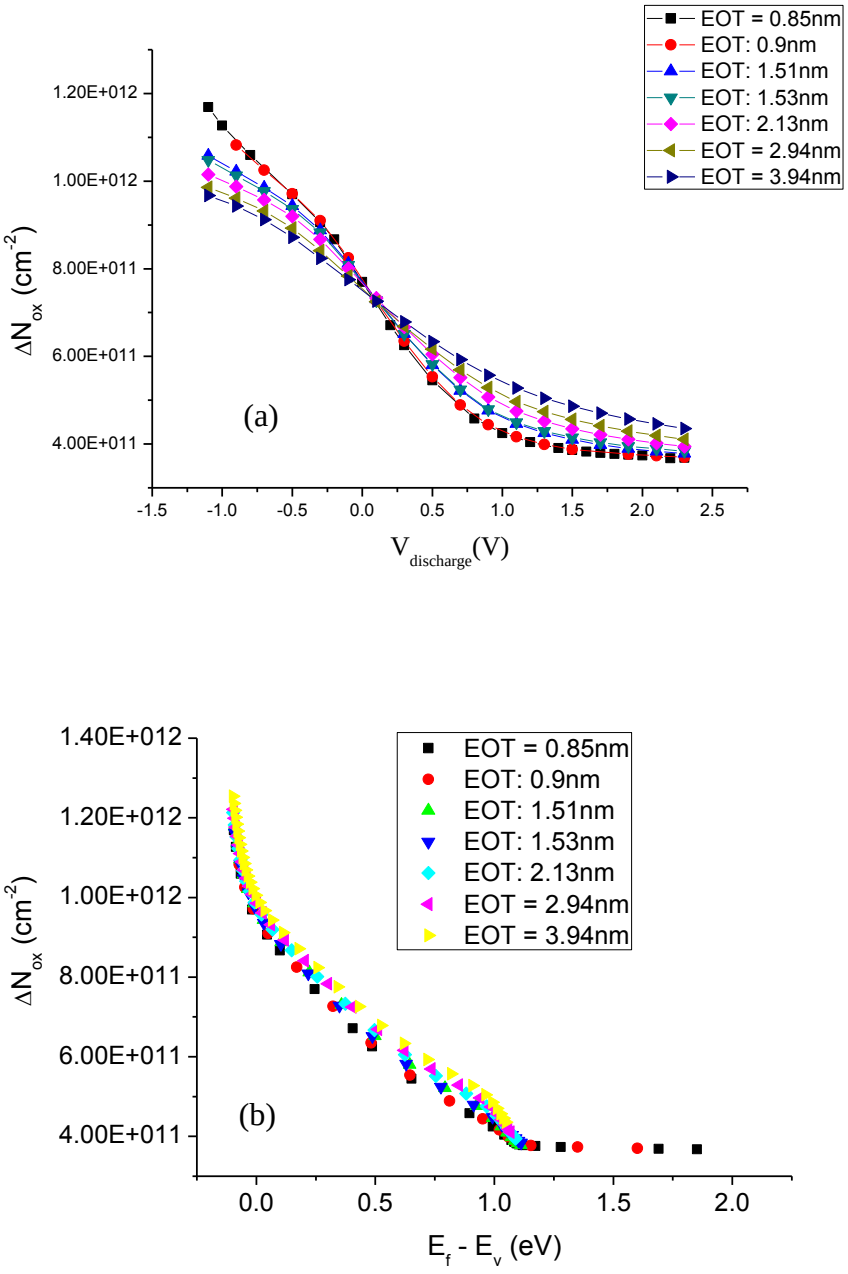


Figure 4.35 Resulting trap density against (a) $V_{discharge}$ (b) E_f-E_v

Closer inspection of Figure 4.36 based on the plot of D_{ox} indicated that the thinner EOT below Ev showed more traps as compared to thicker oxide. From the energy profiling technique conducted on this gate stack, four peaks were observed subsequent to the given stress as indicated by the circle in the figure. The higher peak which was

close to the Ec was observed that suggested the Hf related defect (S. W. M. Hatta, 2013; S. W. M. Hatta et al., 2014).

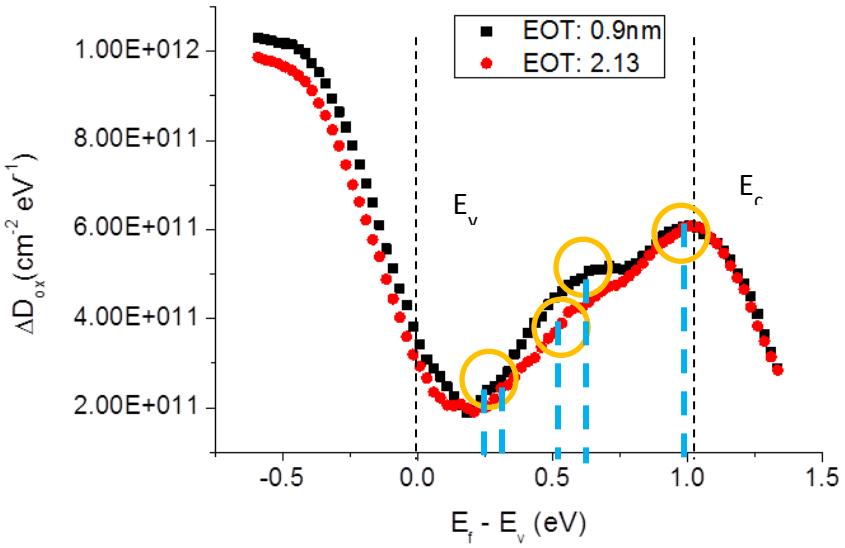


Figure 4.36 Resulting Dox against Ef – Ev for different EOT

The influence of different SiO_2 interfacial and HfO_2 layer thickness was compared as shown in Figure 4.37 (a) and (b) respectively. The trap energy density of different SiO_2 interfacial layer as shown in Figure 4.37 (a) gave different dependence for each region. Higher positive charges were observed below the E_v which proved that they originated from AHT. Two peaks were observed within the energy band gap which proved that the CPC exist hence contributing to the degradation. Since the two peaks were observed more for thinner SiO2 interfacial layer, it is then proven that the thinner SiO_2 interfacial layer produced more degradation. As a comparison, higher CPC was also observed for thinner SiON in (S. W. M. Hatta, 2013; S. W. M. Hatta et al., 2014). The two peaks of CPC appeared to be in both upper and lower half in agreement with high-k stacks used in (S. W. M. Hatta, 2013). The peak in the upper

half was higher than the peak in the lower half of the band gap. Above the E_c, the E'/Pb H complex which was confirmed to have originated from ANPC was permanently charged hence contributed to the permanent degradation. Just above the E_c, the E'/Pb H complex which, when permanently charged was more for thinner SiO_2 interfacial layer which further proved that thinner SiO_2 interfacial layer led to more degradation. On the other hand, the different thickness of HfO_2 layer with fixed SiO_2 interfacial layer provided almost similar trap energy density in all energy regions as shown in Figure 4.37 (b). Here, only a slightly higher trap energy density of thicker HfO_2 layer as compared to thinner HfO_2 layer was observed. Therefore, the reliability optimization based on gate geometrical structure should be focusing more on the thickness of SiO_2 interfacial layer as the degradation varied significantly in different thickness of SiO_2 interfacial layer.

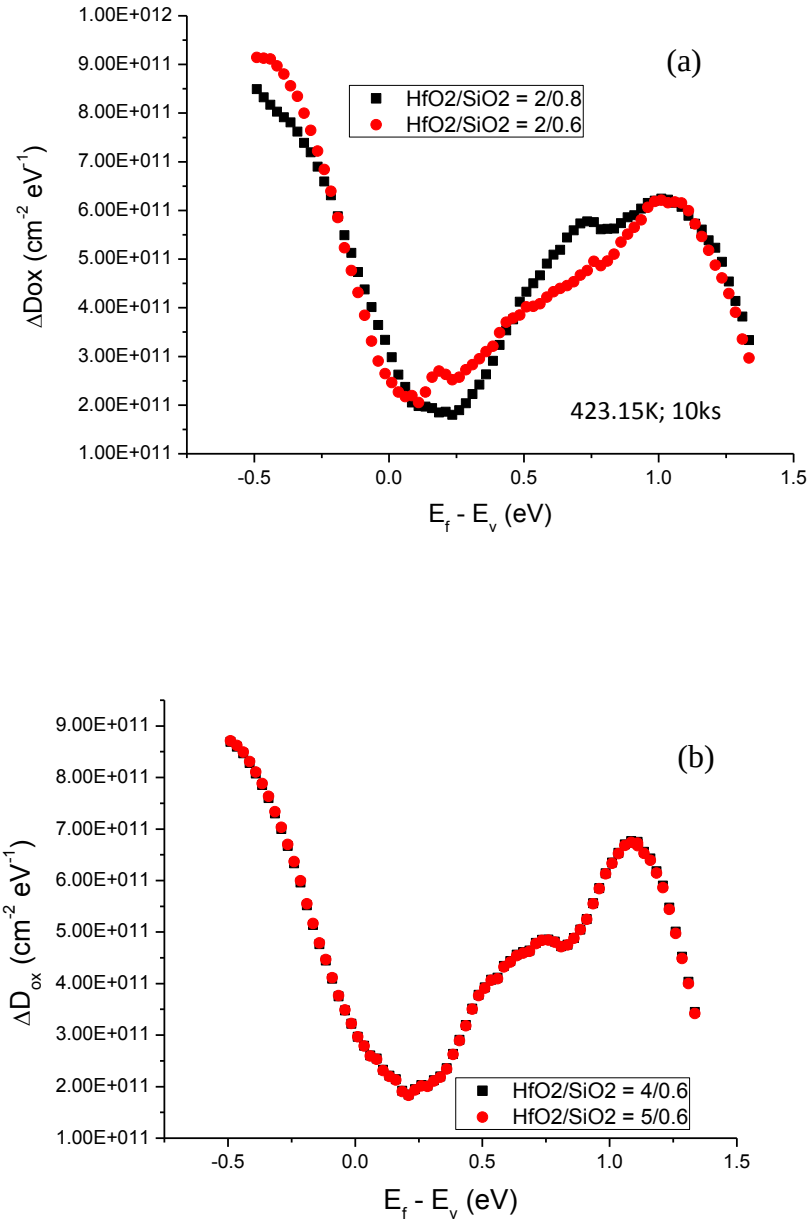


Figure 4.37 Comparison for different EOT (a) Vary SiO_2 thickness with fixed HfO_2 thickness (b) Vary HfO_2 thickness with fixed SiO_2 thickness

4.4.3.2 Comparison of energy distribution of positive charges in metal/HfO_2/SiO_2 with varying metal gate materials

In this subsection, the comparison of energy distribution between different metal gate materials of hf-based devices was performed. The thickness of SiO_2 and HfO_2 were 0.6 nm and 2 nm respectively. All the devices have the width and length of 10um and 32nm respectively. The stress simulation setup was similar as described previously where the Eox ~ 10 MV/cm and the temperature was 125 C. The traps were then discharged by applying more positive charges after the stress.

An inspection of Figure 4.38 (a) – (c) indicated that the PC behave qualitatively similar for all types of metal gate materials. The threshold voltage shift was shown to be decreased as the $V_{discharged}$ changed towards more positive value and constant approximately above the 1.5 V as depicted in Figure 4.38 (a). Figure 4.38 (b) and (c) show the trap density against the discharging process and surface potential respectively. A very small differences of threshold voltage shift and ΔN_{ox} between the different type of materials can be observed.

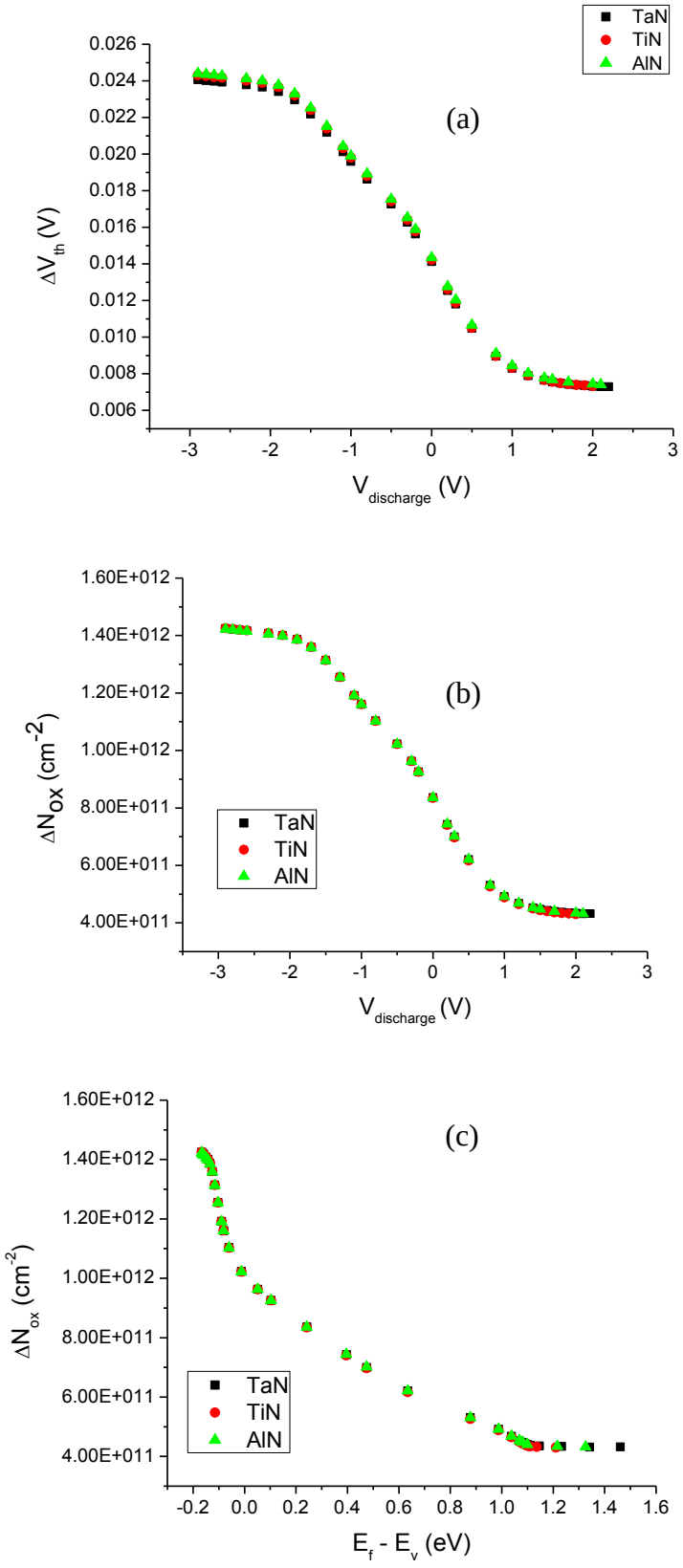


Figure 4.38 Energy profiling technique for different type of metal gate (a) Threshold voltage shift against $V_{discharge}$ (b) Trap density against Vdischarge (c) Trap density against E_f-E_v

To understand how the different types of metal gates can affect the energy profiling of the HfO_2/SiO_2 metal based devices, the trap energy density was plotted as shown in Figure 4.39 (a), (b) and (c) for AlN, TaN and TiN respectively for a different stress time. The trap energy density was plotted based on different stress temperature as depicted in Figure 4.40 (a), (b) and (c) for AlN, TaN and TiN respectively. The energy profiling of the different metal gates was similar to that which was observed previously for AHT which were below the E_v where the AHT was insensitive to stress time and stress temperature. The positively charges originating from the CPC was located within the energy band gap and both metal gate showed that the positive charge increased as stress time increased and saturate after a long stress time. Above E_c, the positive charge is shown to be a different defect which originated from ANPC as the generation of positive charge was sensitive to stress temperature. High stress temperature led to more positive charges. The generation here did not saturate which was similar to that observed and discussed previously. Closer observation on the effects of different stress time for a different type of materials showed that the highest peak which was located near E_c was different for AlN and TaN. As the stress time increased, the peak moved closer to E_c. As for the TiN, the highest peak was observed at E_c, regardless of the stress time. A detailed inspection of Figure 4.40 (a) – (c) indicated that the stress temperature above room temperature gave the highest peak to be located at E_c. The highest peak when stressed at room temperature is located below E_c. This behavior was similar to the different type of materials.

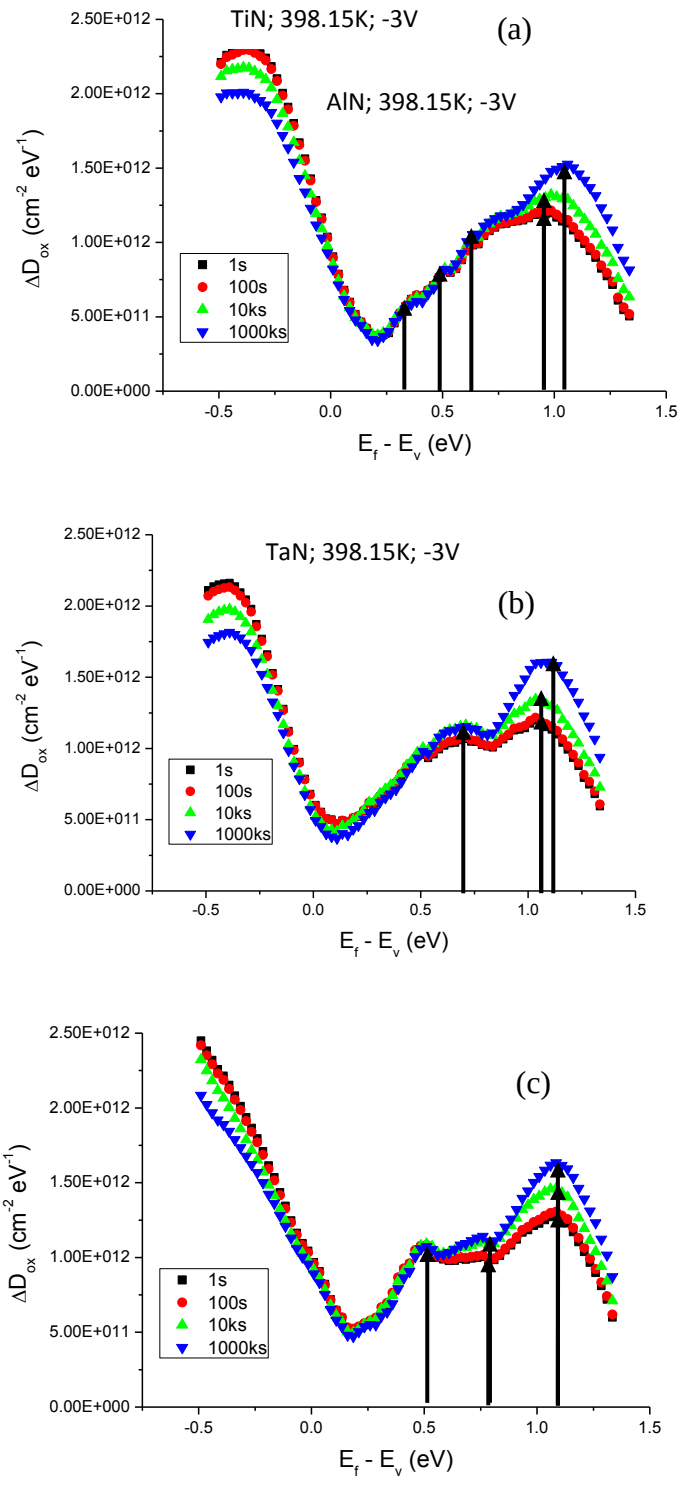


Figure 4.39 Energy density of positive charges at different stress time for (a) AlN (b) TaN (c) TiN

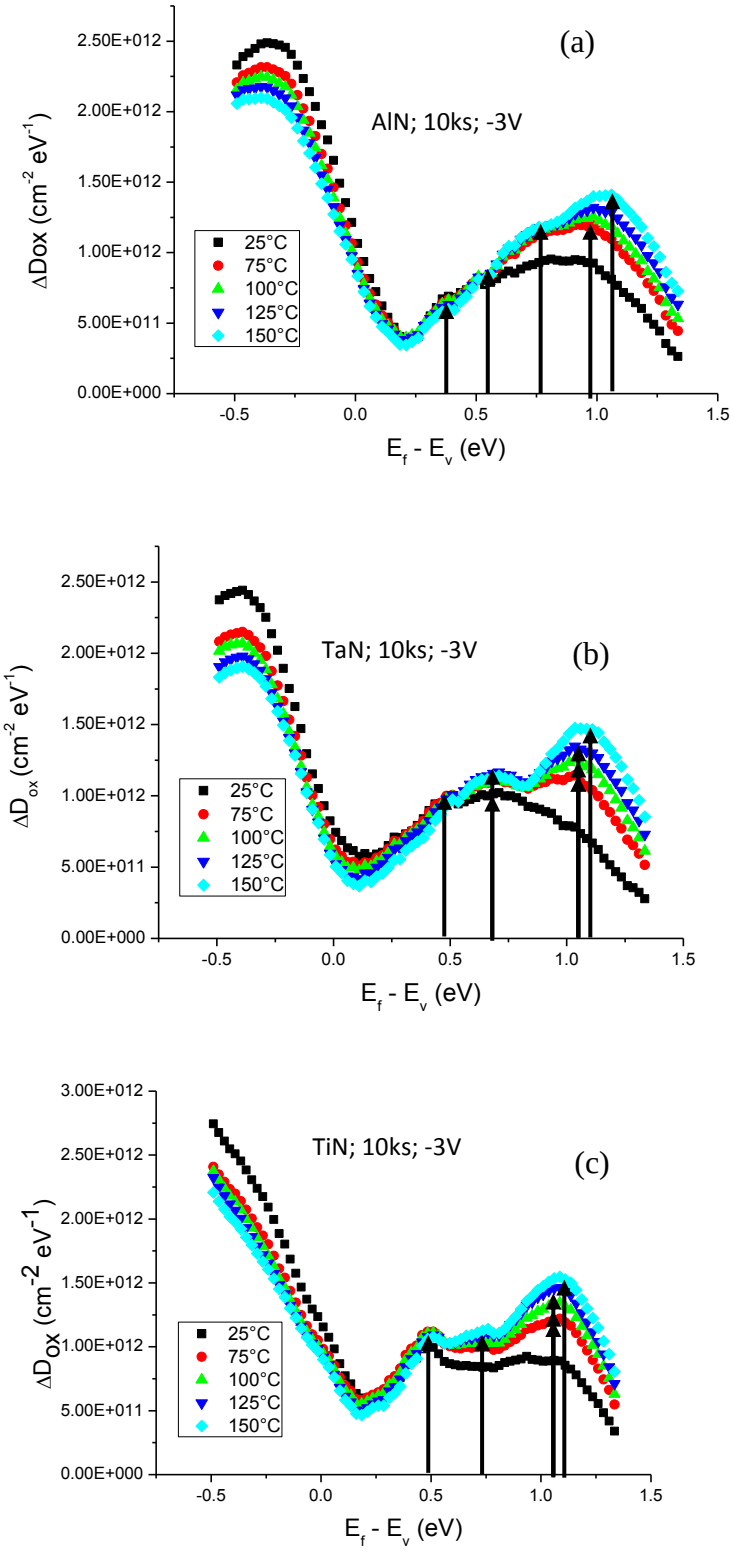


Figure 4.40 Energy density of positive charges at different stress temperature for (a) AlN (b) TaN (c) TiN

Comparison between different metal gate materials used in 32 nm high-k device process for energy profiling is illustrated in Figure 4.41. All the positive charges for different metal gates were sensitive to energy level and differed significantly over the energy range. The different metal gate materials are found to have observable effect on the location of the PCs density peak along the energy range, hence the type of metal gate material used is crucial for better resistance against NBTI. The positive charges below E_v have almost similar discharging effect for the three different metal gates. Near E_i, for positive charge which was within the energy band gap, there is only one peak observed below E_i where the gate material is AlN. At $E_f - E_i \sim 0.5$ eV, there were peaks for all three gate materials where the TiN was the highest followed by TaN and AlN respectively. Another group of peaks were observed for the different type of materials located near to $E_f - E_v \sim 0.75$ eV. The highest peak was observed for TiN metal gate located near to E_C. The highest peak for AlN and TaN were observed located near to $E_f - E_v \sim 1$ eV. Above E_c, the positive charge which originated from ANPC was shown to be permanent as the generation did not saturate for the three different metal gates. Hence, it was observed that the presence of different metal gates did not affect the non-saturation of ANPC generation.

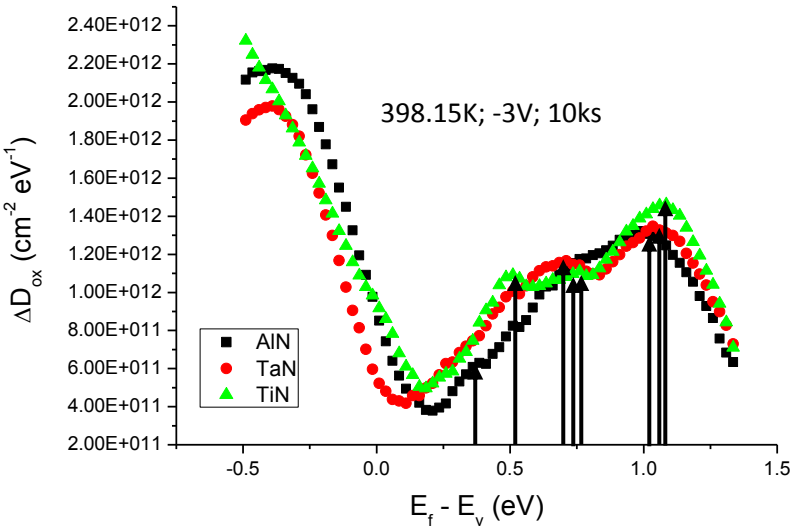


Figure 4.41 Energy density of positive charges for different type of metal gates

4.4.4 Application of new simulation framework on conventional SiO_2 dielectric p-MOSFET devices

The strained SiGe metal–oxide–semiconductor field-effect transistor (MOSFET) was one of the most promising means for further downscaling of MOSFETs so as to conform to the projections of Moore's Law. In particular, the introduction of uniaxial compressive strain into the channel by the embedded pockets of SiGe enhanced channel carrier mobility, thus increasing the drive current and boosting the performance of CMOS devices (Deora et al., 2011; Gomez, Hashemi, & Hoyt, 2009; C. H. Lee et al., 2007). Apart from the performance advantage, the negative effects brought about by the negative-bias temperature instability (NBTI) degradation were also reduced (Gomez et al., 2009; C. H. Lee et al., 2007).

However, most previous studies on the effect of NBTI on strained SiGe p-MOSFET have reported that degradation was based on the hydrogen transport

mechanism (Gomez et al., 2009; C. H. Lee et al., 2007; Maiti et al., 2009). In this section, clear results that indicate the instability in threshold voltage shift of p-MOSFET for strained SiGe and unstrained SiO_2 dielectric p-MOSFET devices, by implementing the energy profiling technique will be presented. Using the 2D numerical simulation tool Sentaurus TCAD, the NBTI degradation mechanism by adopting a new energy level for each defect was studied. After that, the characteristics of each defect through the energy profiling technique was analyzed.

The test bed devices used in this section was based on strained and unstrained SiO_2 p-MOSFET as explained in Section 3.3.2.2. The energy probing simulation technique conducted and stress simulation setup used was similar for the high-k based devices. The stress conditions can be different according to as stated in the graphs or highlighted in the discussion.

4.4.4.1 Energy distribution in strained SiO_2 p-MOSFET devices

The test bed device investigated in this subsection is the conventional strained SiO_2 p-MOSFET transistor with oxide thickness of 1.2 nm. This device has a width and length of 10 µm and 0.05 µm respectively. Figure 4.42 (a) – (c) and Figure 4.43 (a) – (c) presents the result obtained from the energy probing simulation technique after different stress temperature and time respectively.

The AHTs below E_v were the same for different stress temperature as indicated in Figure 4.42 (b). This implied that the AHT's pre-existing defects existed in the strained SiO_2 device. Within and beyond the energy band gap, the positive charges were shown to be temperature dependence. Contrary to high-k based devices, the CPC and ANPC were higher for smaller stress temperature. The reduction of ANPC at higher stress temperature has been observed in (Ce Z. Zhao et al., 2008). The

dependence of positive charges on stress temperature based on energy density is shown in Figure 4.42 (c) which shows that the CPC was insensitive to stress temperature while the ANPC was sensitive to stress temperature. The ANPC is significantly higher for bigger stress temperature. Hence, the signature of each defects was similar to the previous discussion. Based on Figure 4.43 (a) and (b), the distribution of ΔN_{ox} against $V_{discharge}$ and E_f - E_v was investigated. An inspection based on these two figures indicated that the ΔNox increased as the stress time increased. The ΔN_{ox} will initially drop as $E_f - E_v$ increased for all different stress time. Closer observation on Figure 4.43 (c) indicated that the energy density of positive charges below E_v was insensitive to stress time. The CPC within the energy band gap increased with stress time initially before saturating. This is similar to the experimentally observed in (S. W. M. Hatta et al., 2013; J.F. Zhang, 2009; Jian F Zhang et al., 2004; Ce Z. Zhao et al., 2008).

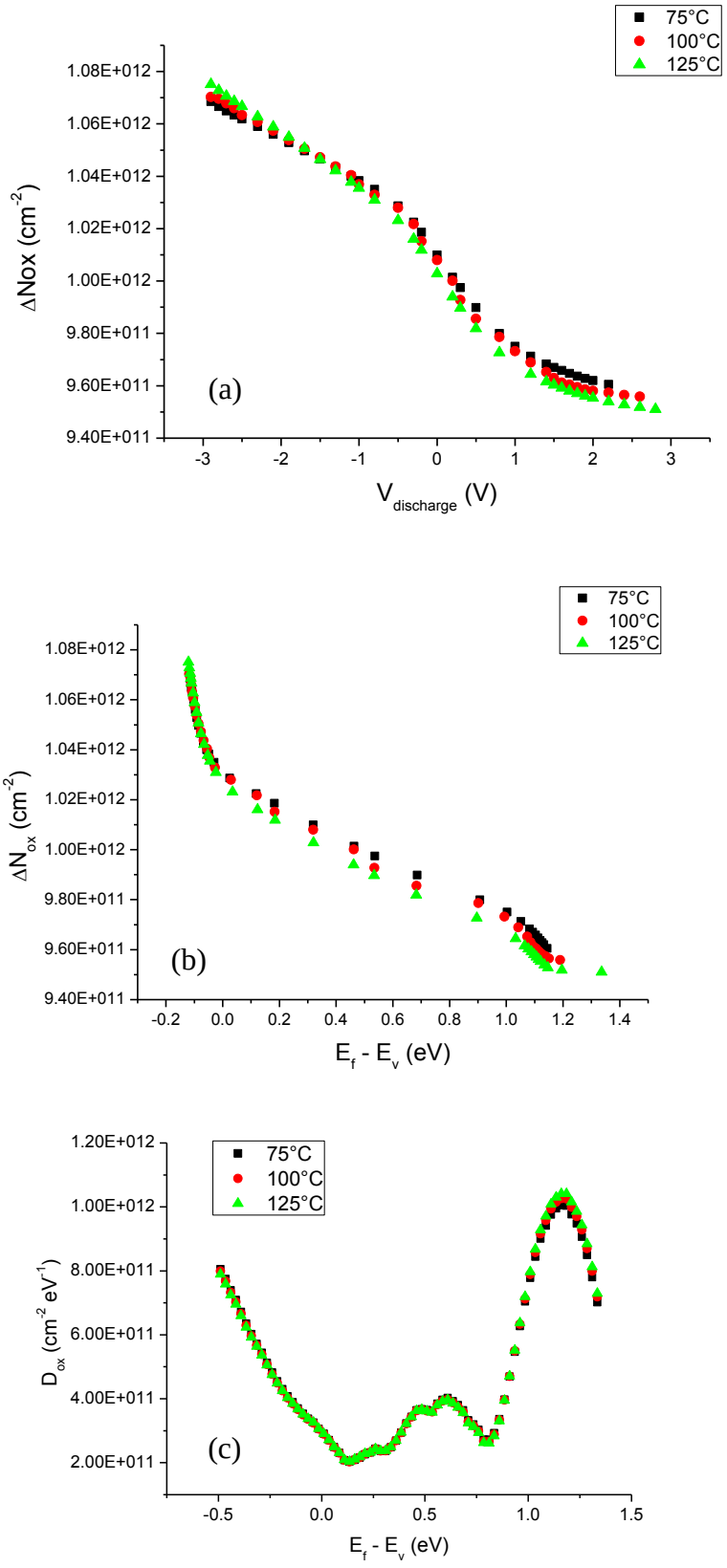


Figure 4.42 Energy profiling technique for strained SiO2 p-MOSFET for different stress temperature

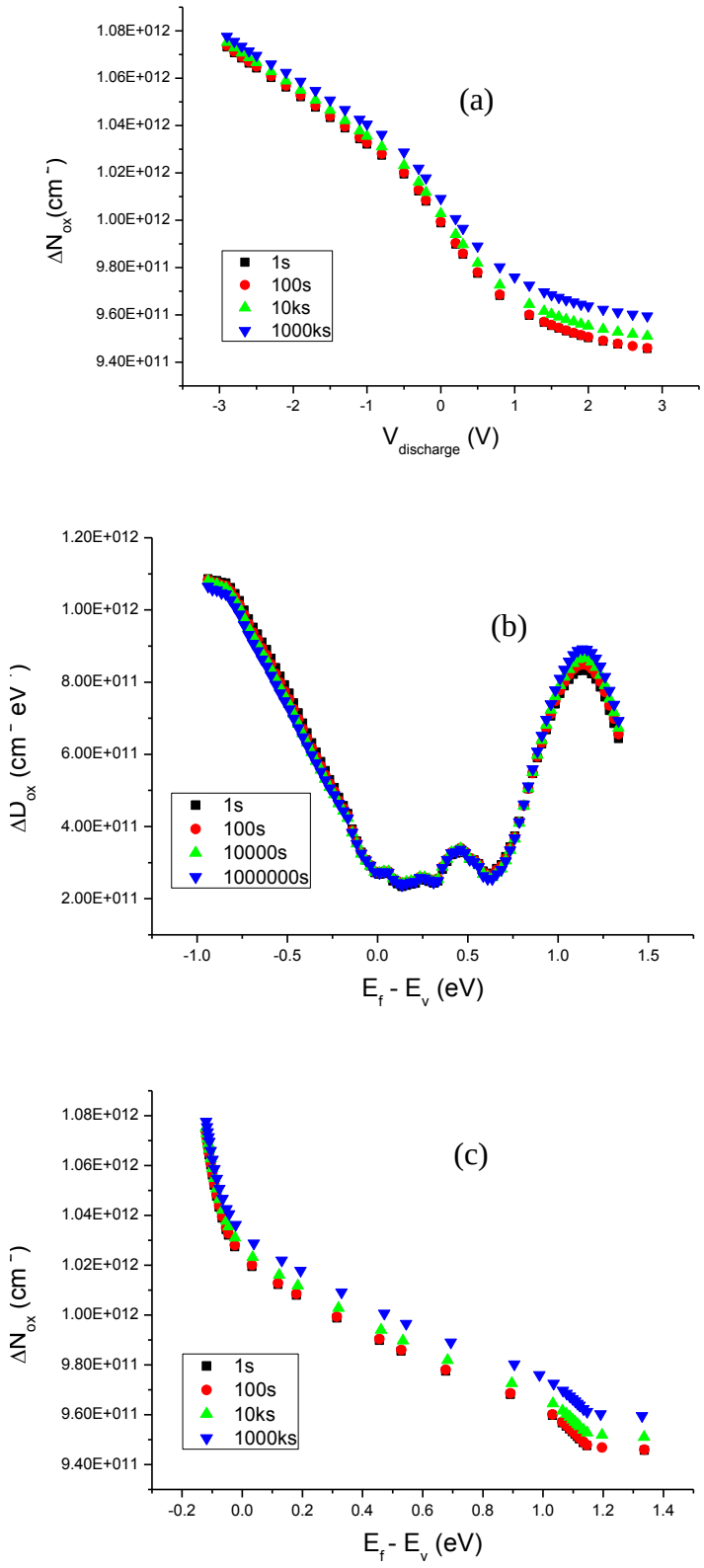


Figure 4.43 Energy profiling technique for strained SiO_2 p-MOSFET for different stress time

4.4.4.2 Energy distribution in unstrained SiO_2 p-MOSFET devices

The test bed device investigated in this subsection is the conventional unstrained SiO_2 p-MOSFET transistor with oxide thickness of 1.2 nm. The device has a width and length of 10 µm and 0.05 µm respectively. Figure 4.44 (a) – (c) and Figure 4.45 (a) – (c) presents the result obtained from the energy probing simulation technique after different stress temperature and time. An inspection on the conventional unstrained SiO_2 p-MOSFET device based on the plots showed similar defect's signature with the strained SiO_2 p-MOSFET as discussed in the previous subsection. The ΔN_{ox} against $V_{discharge}$ and E_f - E_v increased in lower stress temperature and higher for a high stress time. The AHT located below E_v was insensitive to stress temperature and time. Meanwhile, the CPC was insensitive to stress temperature and sensitive to stress time. It was confirmed that the ANPC for this device originated from different defect as it was sensitive to both stress temperature and time. A detail investigation for a comparison between both strained and unstrained SiO_2 p-MOSFET devices will be shown in the next subsection.

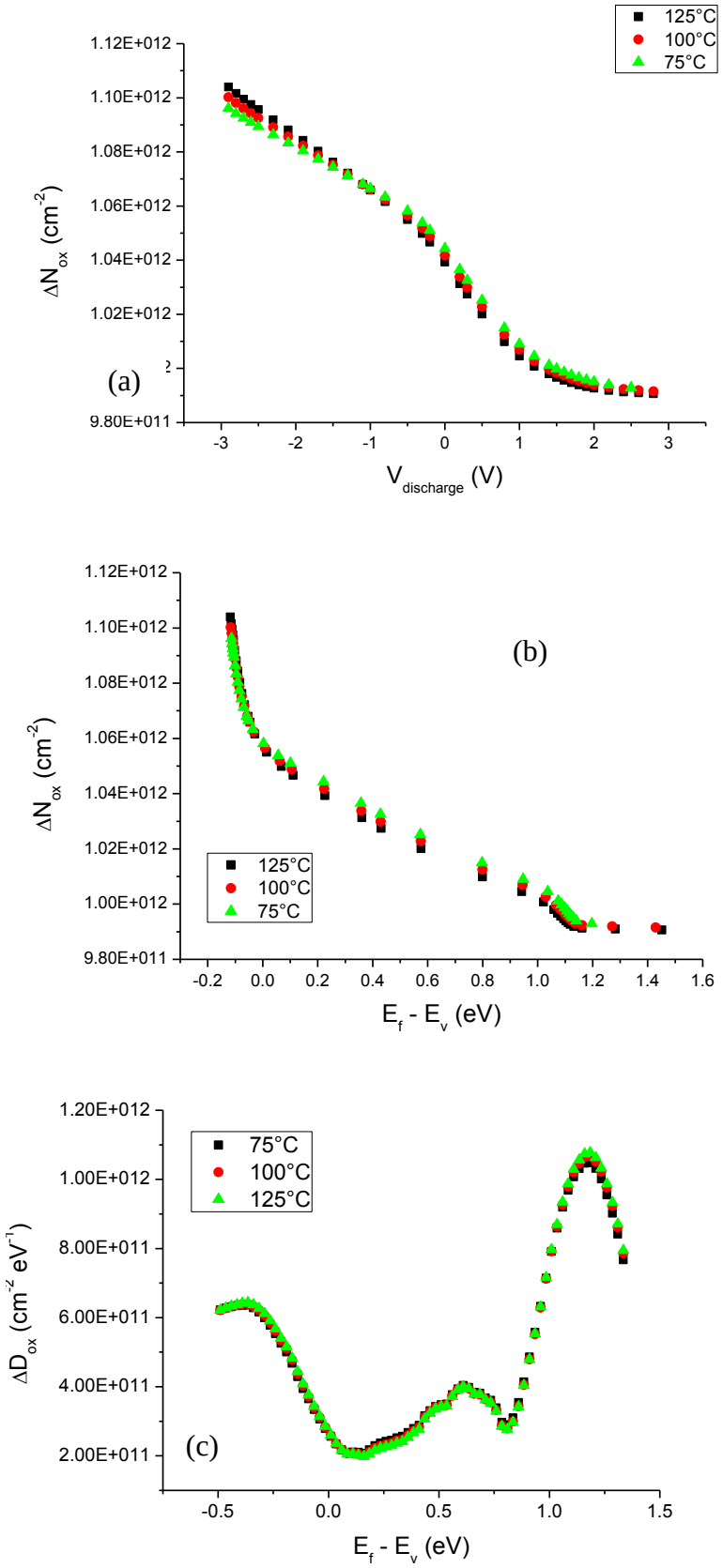


Figure 4.44 Energy profiling technique for unstrained SiO_2 p-MOSFET for different stress temperature

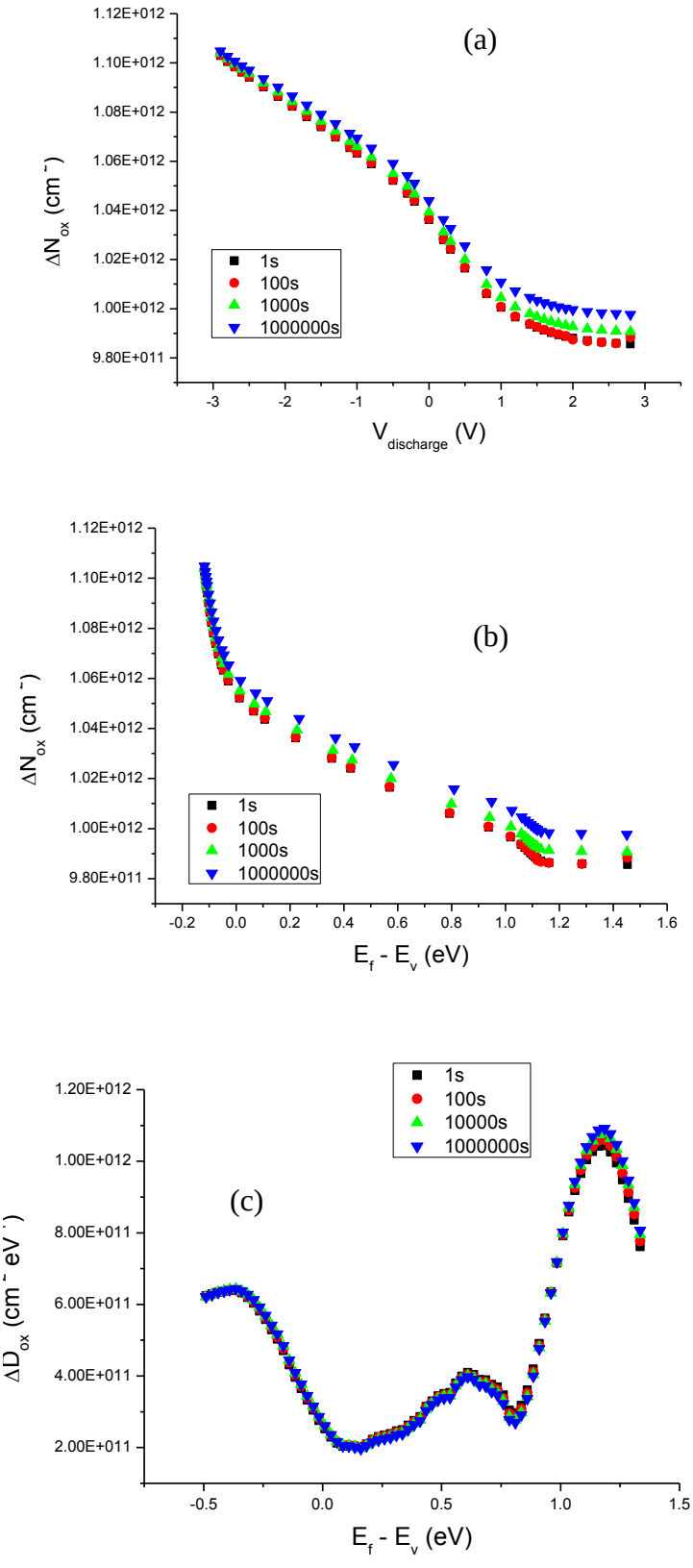


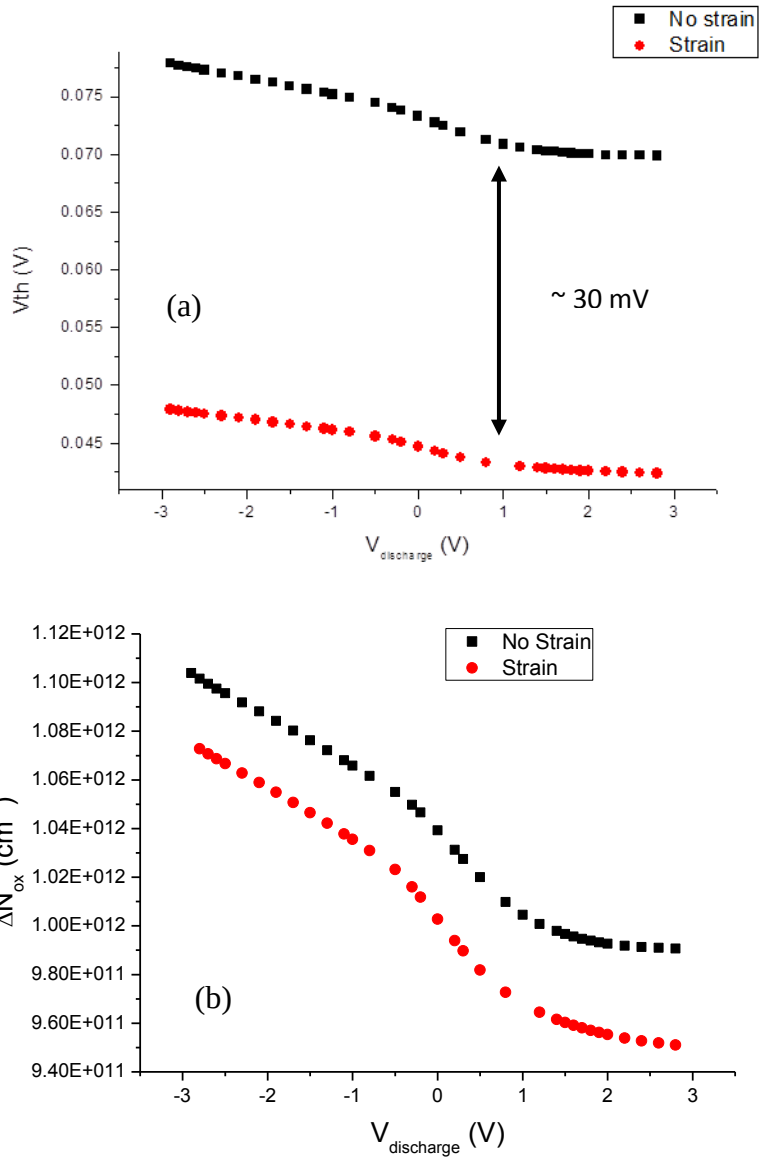
Figure 4.45 Energy profiling technique for unstrained SiO_2 p-MOSFET for different stress time

4.4.4.3 Comparison of the energy distribution in strained, unstrained SiO_2 and HfO_2- based p-MOSFET devices

In order to investigate how the energy distribution of the positive charges in the conventional SiO_2 with and without strained, Figure 4.46 (a) compares the threshold voltage while Figure 4.46 (b) to (d) compares the energy profiling of the conventional SiO_2 both with and without strained. The threshold voltage shift difference between the two devices be seen clearly with about 3 mV difference. Higher threshold voltage was observed for unstrained device. This result was in agreement with (C. H. Lee et al., 2007), wherein the degradation in conventional p-MOSFET was higher than in strained SiGe p-MOSFET. Higher degradation was observed due to the inversion holes' reaction with the Si-H bond, thus generating interface traps (S. Mahapatra et al., 2005). Different immunity toward degradation was attributed to the number of holes being lower in the SiO_2/Si interface of the strained SiGe p-MOSFET than that of the conventional p-MOSFET under the same stress conditions (C. H. Lee et al., 2007). The improved NBTI characteristic for strained SiGe p-MOSFET was attributed to the valence band offset, and thus, holes were mostly found in the SiGe channel (C. H. Lee et al., 2007). Reduction in degradation for strained SiGe p-MOSFET was also observed in (Deora et al., 2011) and was attributed to the increase in hole barrier height and the reduction in hole tunneling mass. Hence, tunneling current was reduced, thus further providing support that SiGe intrinsically improved NBTI.

The positive chargers plotted against $V_{discharge}$ and $E_f - E_v$ as shown in Figure 4.46(b) and (c) respectively confirmed that the degradation was more for unstrained device. The energy density plotted in Figure 4.46 (d) shows that there were two significant peaks observed, which was higher for unstrained device. The peaks were

located near to $E_f - E_v \sim 0.75$ eV and at E_c. Closer inspection on the energy density gave three peaks for the strained device located within the energy band gap located at $E_f - E_v \sim 0.25$ eV, $E_f - E_v \sim 0.45$ eV and $E_f - E_v \sim 0.65$ eV.



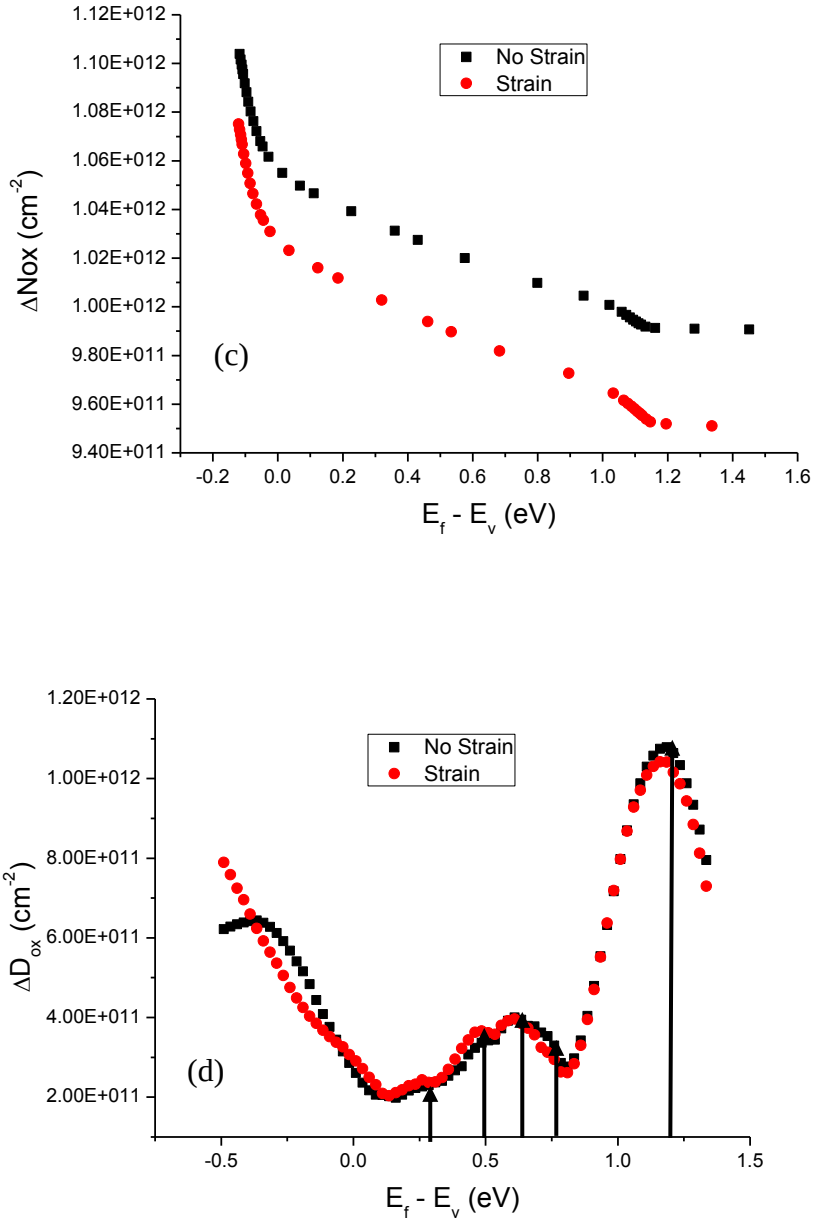


Figure 4.46 Comparison between strained and unstrained SiO_2 p-MOSFET devices (a) Threshold voltage shift against $V_{discharge}$ (b) Trap density of positive charges against $V_{discharge}$ (c) Trap density of positive charges against $E_f - E_v$ (d) Energy density of positive charges against $E_f - E_v$

To further examine how the energy distribution of positive charges in the conventional single-layered strained and unstrained SiO_2 varied from the high-k device, Figure 4.47 compares the energy profiling of the conventional single-layered strained and unstrained SiO_2 with that of HfO_2/SiO_2 device which was discussed previously. It was observed that all devices embraced considerable AHT designated from the significant peak below E_v. It can be seen that the amount of the AHT was the highest for Hf-based device indicate, that more pre-existing defect available in the device. Closer observation on the positive charges within the bandgap found one peak above the midgap and another clear peak close to E_c for the Hf-based device. Another observation worth mentioning here is that the CPC can be considerably higher in the Hf-based device as compared to SiO_2 dielectric device above the mid gap. Beyond the energy band gap however, the positive charges were higher for SiO_2 dielectric based devices indicating that the generation of ANPC was more for the SiO_2 dielectric devices as compared to HfO_2/SiO_2 based device.

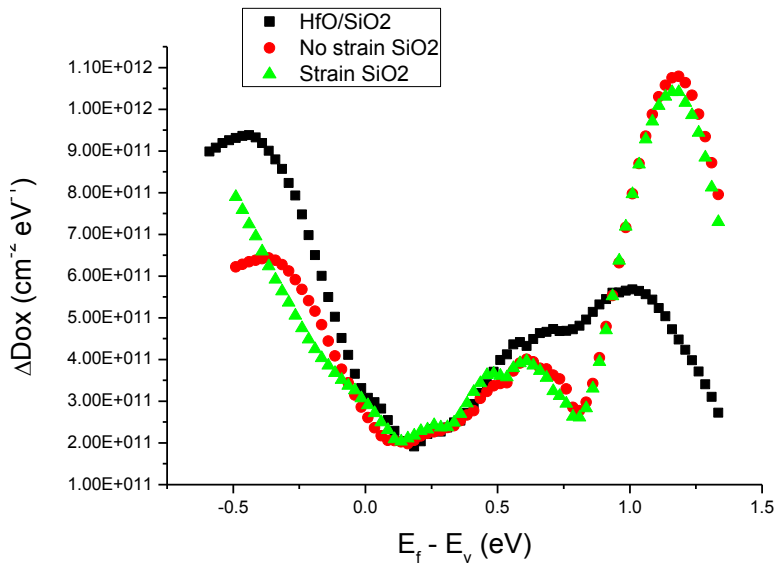


Figure 4.47 Energy density of positive charges against Ef-Ev for HfO_2-based device, unstrained SiO_2 and strained SiO_2 device

4.4.5 Application of new simulation framework of 3D FinFET simulation

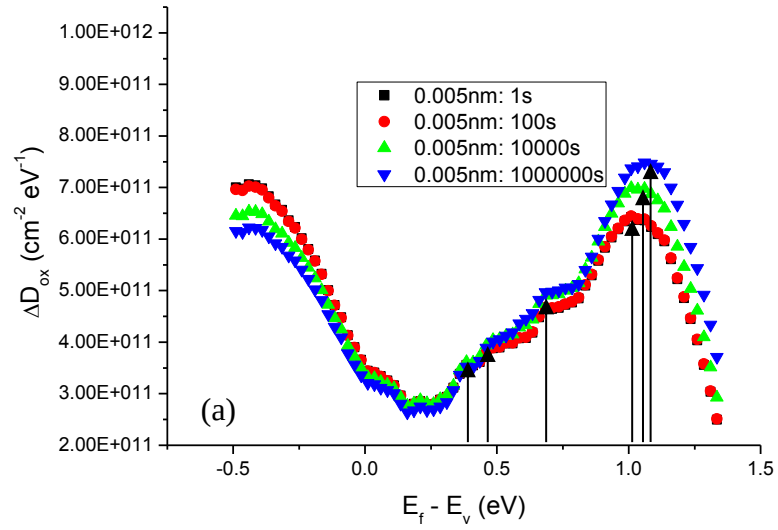
The fast scaling of the CMOS technology triggered the evolution from conventional planar MOSFETs of the FinFET design, particularly in the 22 nm and 14 nm technology nodes. FinFETs technologies ensured traditional scaling improvements as well as low power application and better area consumption. Transition from conventional planar MOSFETs to FinFET is seen as one of the best approaches to improve performance as CMOS scaling matures in the following decade. Recently, a better performance of FinFET was magnificently verified on a 22nm node FinFET technology as compared to planar MOSFETS [1]. The conducting channel which forms the body of the device was wrapped by thin silicon “fin” which was a unique characteristic of the FinFET. The effective channel length of the device was determined by the thickness of the fin which measured the source to drain. In adopting the FinFET, the challenges in modifying the transistor size is the discrete size of the fin where the transistor width is no longer a continuum. Discrete fin sizing conveys a new adjustable in design, providing designers with a new experience to improve the performance of the FinFET. Hence, to determine the best design, performance, and manufacturability compromises’ of the next node technologies (14nm and 16nm nodes), the 3D TCAD analysis of such FinFET are one of the best methods.

Therefore, this work will adopt the 3D TCAD simulation to simulate a 16 nm node FinFET technology where the energy density of FinFETs was studied. The device structure was generated via a 3D process simulation and the process step was explained in Section 3.3.2.3. To verify that the proposed new simulation method of characterizing the NBTI degradation by implementing the energy profiling approach was also applicable to advanced 3D FinFET device technology, the signature of each

positive charge will be evaluated based on the energy density plot. The evaluation process involved the effect of different stress times, stress temperatures and different size of FinFET widths.

4.4.5.1 Effect of Stress Time on Energy distribution of FinFET

Figure 4.48 (a) to (d) presents the energy density obtained subsequent to the stress applied to a different fin width of FinFET with variation in stress time. Different fin widths were used in this work consisting of 0.005 nm, 0.0075 nm, 0.01 nm and 0.0125 nm. The energy distribution for all of the FinFETs exhibited almost similar behavior as discussed in the Hf-based device. The positive charges were sensitive to the energy level and varied significantly over the energy range. Under closer observation, all the FinFET have positive charges below E_v, which originated from AHT as the positive charges insensitive with the stress time variation. Within the energy band gap, the positive charges increased as the stress time increases for FinFET with a fin width of 0.005 nm and 0.01 nm. The CPC within the band gap observed to be saturated after a long stress time, but for fin width 0.0075 nm and 0.0125 nm the CPC reduced above 10 ks. The ANPC located beyond the energy band gap significantly increased with the increasing of stress time. Another noteworthy observation here was that the CPC below the Ec significantly increased with the increasing of stress time for all the FinFETs. The effects of the location of the peak was because different temperature can significantly be observed for ANPC. For CPC, similar peak location was observed for different temperature. An interesting finding for the ANPC is that the peak moved to a higher energy lever when the stress time increased.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8.00E+011
7.00E+011
6.00E+011
5.00E+011
4.00E+011
3.00E+011
2.00E+011
ΔD_ox (cm^-2 eV^-1)
0.005nm: 1s
0.005nm: 100s
0.005nm: 10000s
0.005nm: 1000000s
(a)
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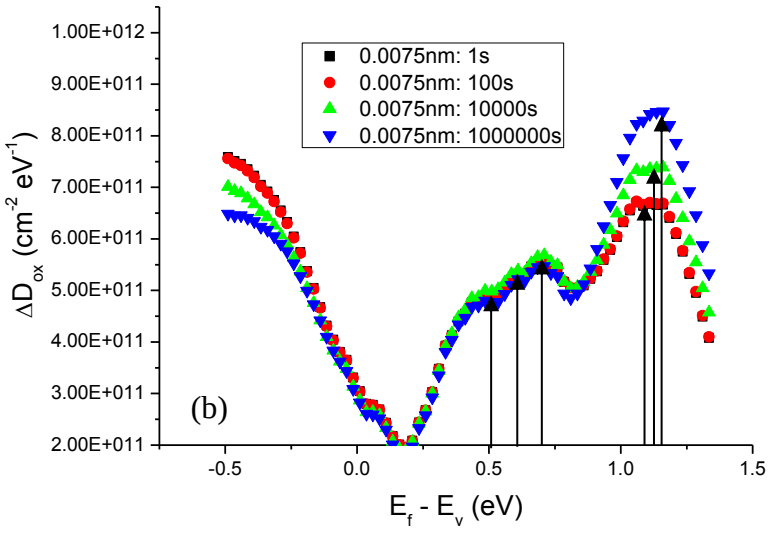
1.5
E_f - E_v (eV)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6.00E+011
5.00E+011
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3.00E+011
2.00E+011
ΔD_ox (cm^-2 eV^-1)
0.0075nm: 1s
0.0075nm: 100s
0.0075nm: 10000s
0.0075nm: 1000000s
(b)
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0.5
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1.5
E_f - E_v (eV)

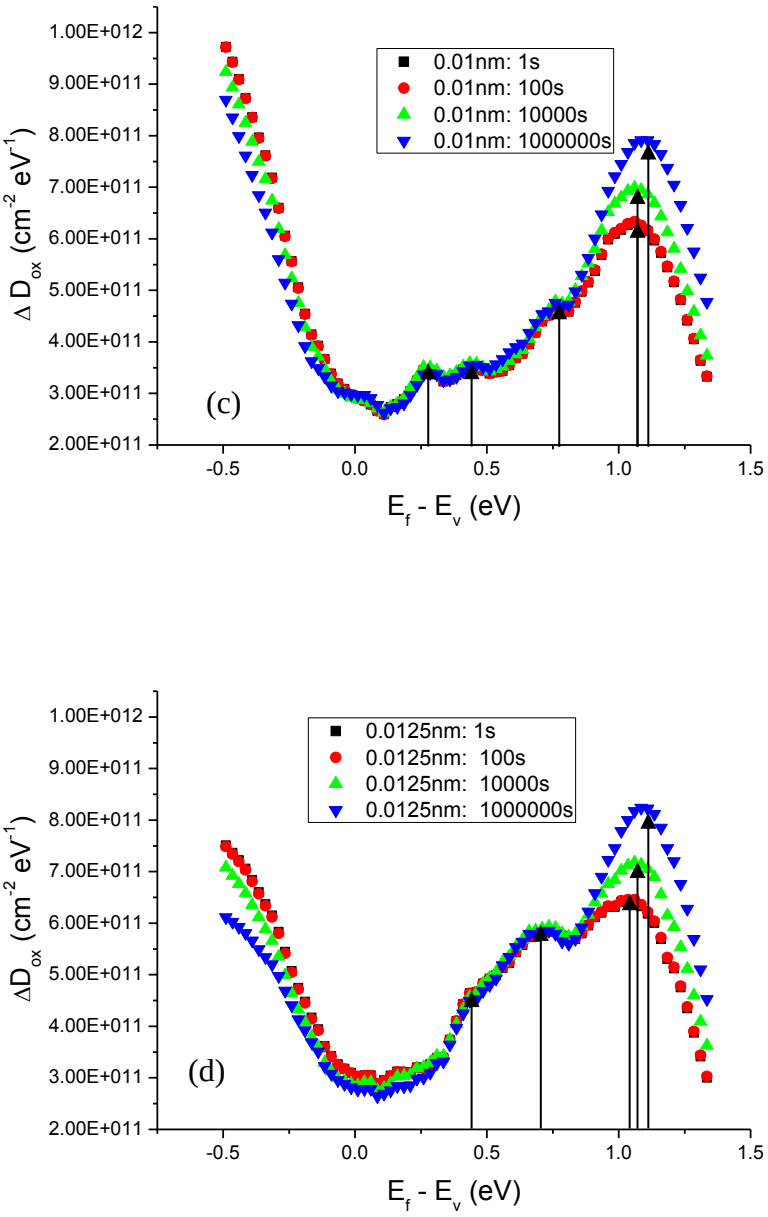
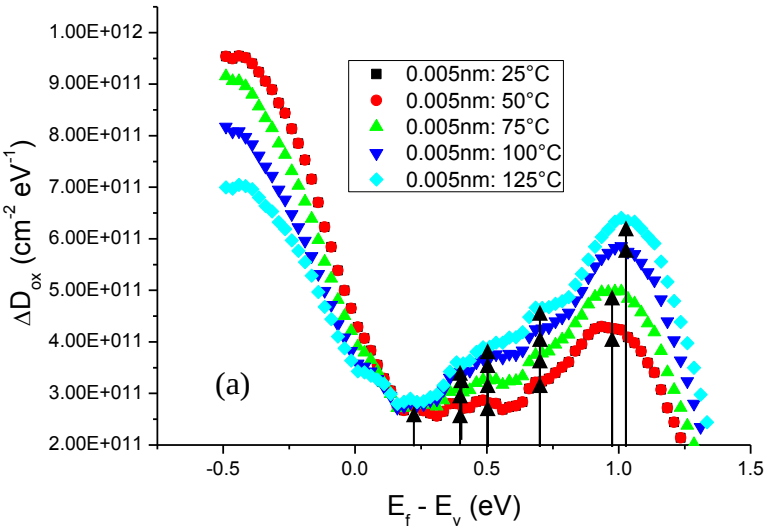


Figure 4.48 Energy profiling technique for different fin widths of p-finFET for different stress times (a) 0.005 nm (b) 0.0075 nm (c) 0.01 nm and (d) 0.0125 nm

4.4.5.2 Effect of Stress Temperature on Energy distribution of FinFET

The results reported in Figure 4.49 (a) to (d) were obtained by stresses at 10 ks with different stress temperature. As expected, below the E_v where the AHT is located was not stress temperature dependence which confirmed that there was available pre-existing defects in FinFET structure. Careful observation on positive charges within the band gap imposed that the CPC was sensitive to stress temperature for FinFET with a fin width of 0.005 nm and 0.0125 nm. However, for the fin width of 0e.0075 nm, the CPC increased as stress temperature increased below the $E_f - E_v = 0.75$ eV. Above $E_f - E_v = 0.75$ eV, the CPC was more when stressed at room temperature. Meanwhile, for the fin width of 0.01 nm, the CPC increased as stress temperature increased when stressed above room temperature. The generated CPC was the highest when stressed at room temperature. Another noteworthy observation is that the CPC was peaking at the same location for a different stress temperature. While the energy level of ANPC which was beyond the energy band gap shifted to a higher energy level, the stress time increased as well.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7.00E+011
6.00E+011
5.00E+011
4.00E+011
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2.00E+011
ΔD_ox (cm^-2 eV^-1)
0.005nm: 25°C
0.005nm: 50°C
0.005nm: 75°C
0.005nm: 100°C
0.005nm: 125°C
(a)
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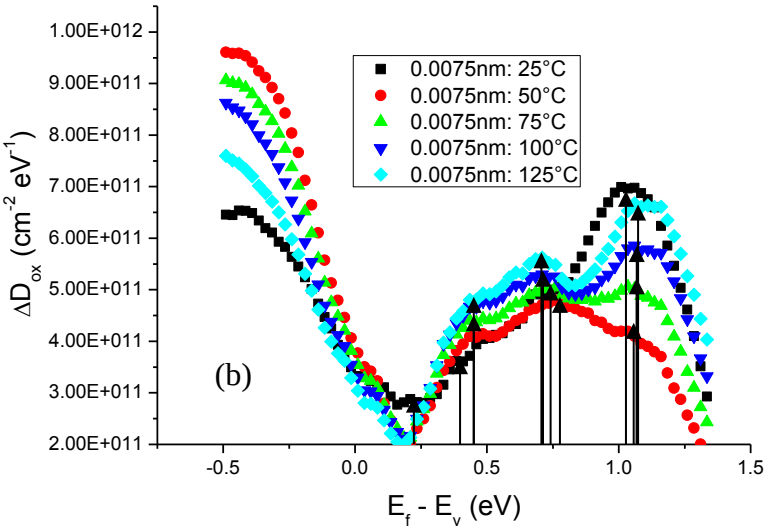
0.0
0.5
1.0
1.5
E_f - E_v (eV)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4.00E+011
3.00E+011
2.00E+011
ΔD_ox (cm^-2 eV^-1)
0.0075nm: 25°C
0.0075nm: 50°C
0.0075nm: 75°C
0.0075nm: 100°C
0.0075nm: 125°C
(b)
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1.0
1.5
E_f - E_v (eV)

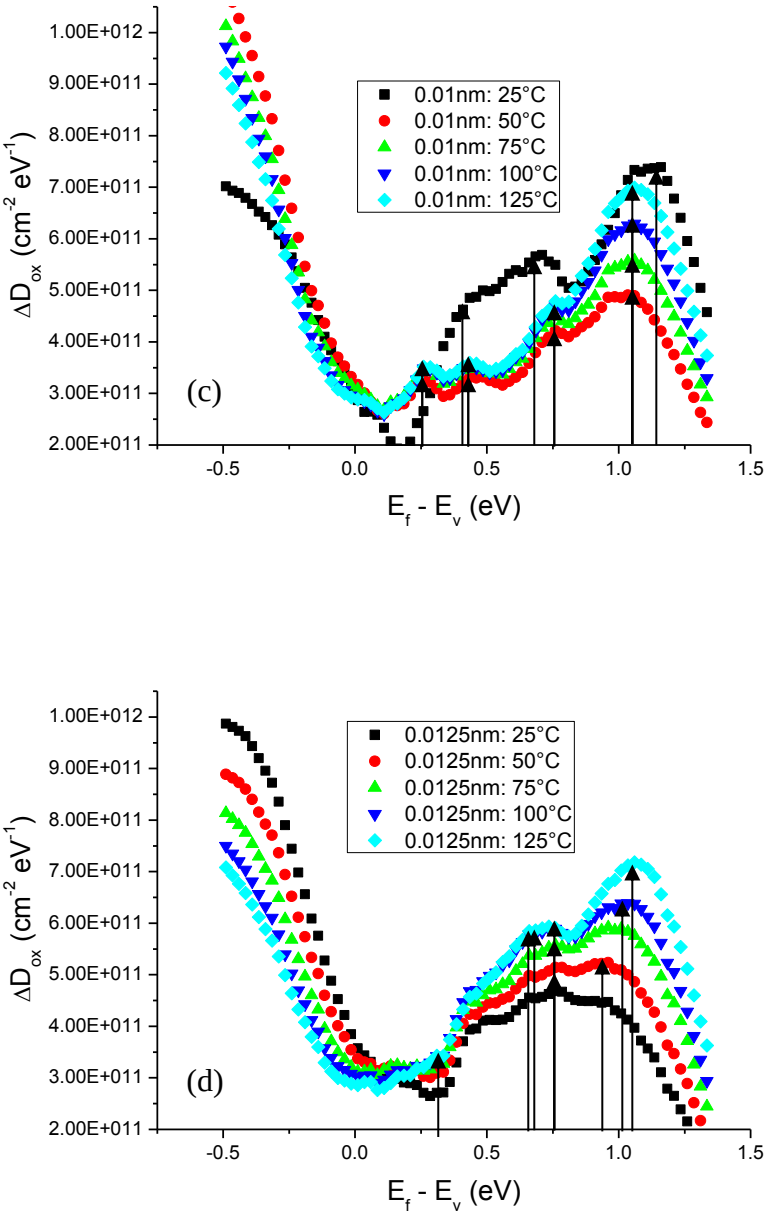


Figure 4.49 Energy profiling technique for different fin width of p-finFET for different stress temperatures (a) 0.005 nm (b) 0.0075 nm (c) 0.01 nm and (d) 0.0125 nm

4.4.5.3 Energy distribution in FinFET with different fin width and comparison with planar devices

In order to investigate the effects of fin width variation in the energy density of positive charges, all energy densities for each FinFETs were plotted and presented in Figure 4.50. The first impression here is that that there was no correlation between fin width variations with the energy density of the positive charges. However, the fin width is found to have observable effect on the location of the PC density peak along the energy range. Closer observation showed that the CPC within the energy band gap lowest for a fin width of 0.01 nm. Only the fin width of 0.0075 nm has ANPC peak which was located beyond the energy band gap. There was a similar highest peak observed for a fin width of 0.005 nm, 0.01 nm and 0.0125 nm which located near E_c. In addition to that, there were two other peaks by fin width 0.01 nm observed below energy midgap while one peak by fin widths 0.0075 nm and 0.0125 nm are observed above energy mid gap respectively. Since different fin width results in different peaks and their locations, optimizing the fin width was essential for minimizing NBTI of FinFET architecture. The immunity toward NBTI was found to be better for larger fin width (Chabukswar et al., 2010).

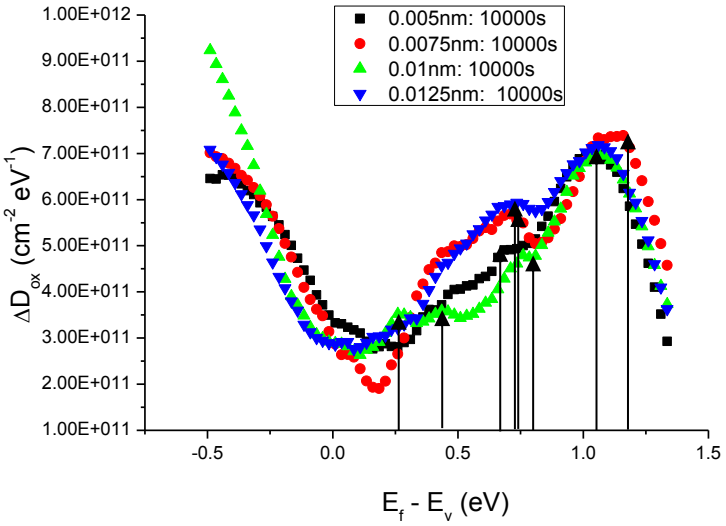


Figure 4.50 Comparison of energy density of positive charges for different fin width

The understanding on how the energy distribution of the positive charges in the FinFET varied from the planar p-MOSFET consist of Hf-based and conventional single-layered SiO_2 dielectric with and without strained devices was made by comparing the energy density of the FinFET with that of the Hf-based and conventional single-layered SiO_2 dielectric shown in Figure 4.51. It was detected that all the devices contained of considerable AHT specified from the significant peak below E_v. It can be noted here that the amount of the AHT was nearly twice in the high-k stack as compared to the FinFET and conventional SiO_2 dielectric. However, above E_v, the CPC was highest for FinFET. The energy distribution of positive charges between FinFET structure and planar Hf-based device was comparable where similar highest peak location was observed near E_c and one lower peak at $E_f – E_v = 0.7$ eV. Another remarkable observation was that the CPC can be considerably small in the conventional SiO_2 as compared to FinFET and planar hf-based device. The CPC

peak at $E_f - E_v$ = 1 eV was apparent in the FinFET and planar hf-based device, suggesting that it was Hf-related. Near E_c, only one peak was obvious in the conventional planar SiO_2 devices indicating the highest CPC in this sample. This can be explained based on the fabrication process which can fix the precursors of CPC where the generation of CPC was sensitive to hydrogen exposure during the fabrication (J.F. Zhang, 2009; C Z Zhao & Zhang, 2011). It is suggested that higher density of hydrogenous species exists in the sample with SiO_2 dielectric.

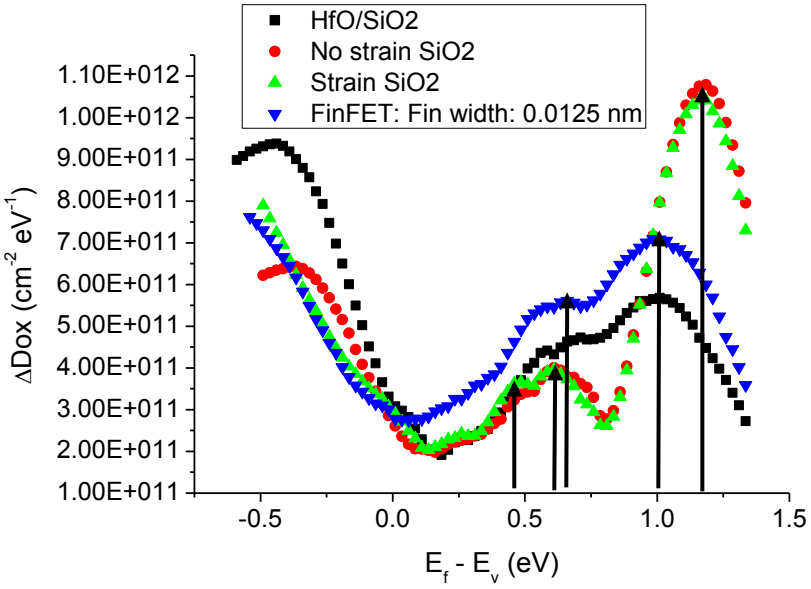


Figure 4.51 Comparison of energy density of positive charges for different technology of p-MOSFETdevices

4.4.6 Comparison between default and new define energy profiling of defect components on the NBTI degradation effects

4.4.6.1 Effects on Sub-threshold Operation

In ultra low-power applications, operations in a transistor's sub-threshold regime were critically important for meeting a system's stringent power requirements.

However, considering the aggressive downscaling of complementary metal-oxide-semiconductor (CMOS) transistors, stress-induced NBTI has emerged as a reliability threat even in low-power systems. As a result of scaled oxide thickness in sub-nanometre regime devices, the increased electric field further enhanced the NBTI degradation effects. Many studies that used circuit-level simulation used the R-D model to investigate the effects of NBTI degradation on a circuit's performance (W. Wang et al., 2010; Yuan, Yeh, Chen, & Hsu, 2011). However, as the oxide trapping/de-trapping effect mechanism affect device performance considerably (D S Ang et al., 2011; S. W. M. Hatta et al., 2013), a device-level analysis of the effect of NBTI, which involved both oxide and interface traps under sub-threshold operation regime, is necessary. From the device-level perspective, operation in sub-threshold regime for UT-EOT devices were contributed by the minority carrier and holes under the gate and diffuses due to the application of V_{DS}. However, different mechanisms occurred given the very thin EOT. Direct tunnelling of holes from substrate to bulk oxide will be trapped in the E'center defect precursor, which further degraded the device performance (Cho et al., 2012). The transistors that operated under sub-threshold operation were normally used as to meet the ultra low-power application requirement. In this section the effect of sub-threshold operation using default and new defined energy levels for each defect were compared. As observed in Figure 4.52 (a), the time exponent, n as a function of Vtho for new and default energy level varied significantly during the sub and super-threshold operations. The V_{tho} is the initial value of threshold voltage for the device. The default energy level showed that the time exponent, n was around 0.1. However, the super-threshold voltage gave a different n. The n for new define energy level can be varied up to 0.3 as observed in

most experimental works involving defects associated with DLHT or ANPC (S. W. M. Hatta, 2013) which shown to be distributed closer or above E_c.

The total positive charges contributed in the degradation for new and default energy level is shown in Figure 4.52 (b). Significant differences can be seen in the new define energy level based on the applied stress temperature. Higher temperature gave more total positive charges contributed towards the degradation during sub and super-threshold operation regime for the new defines energy level. However, the default energy level showed no temperature effects upon the generated total positive charges.

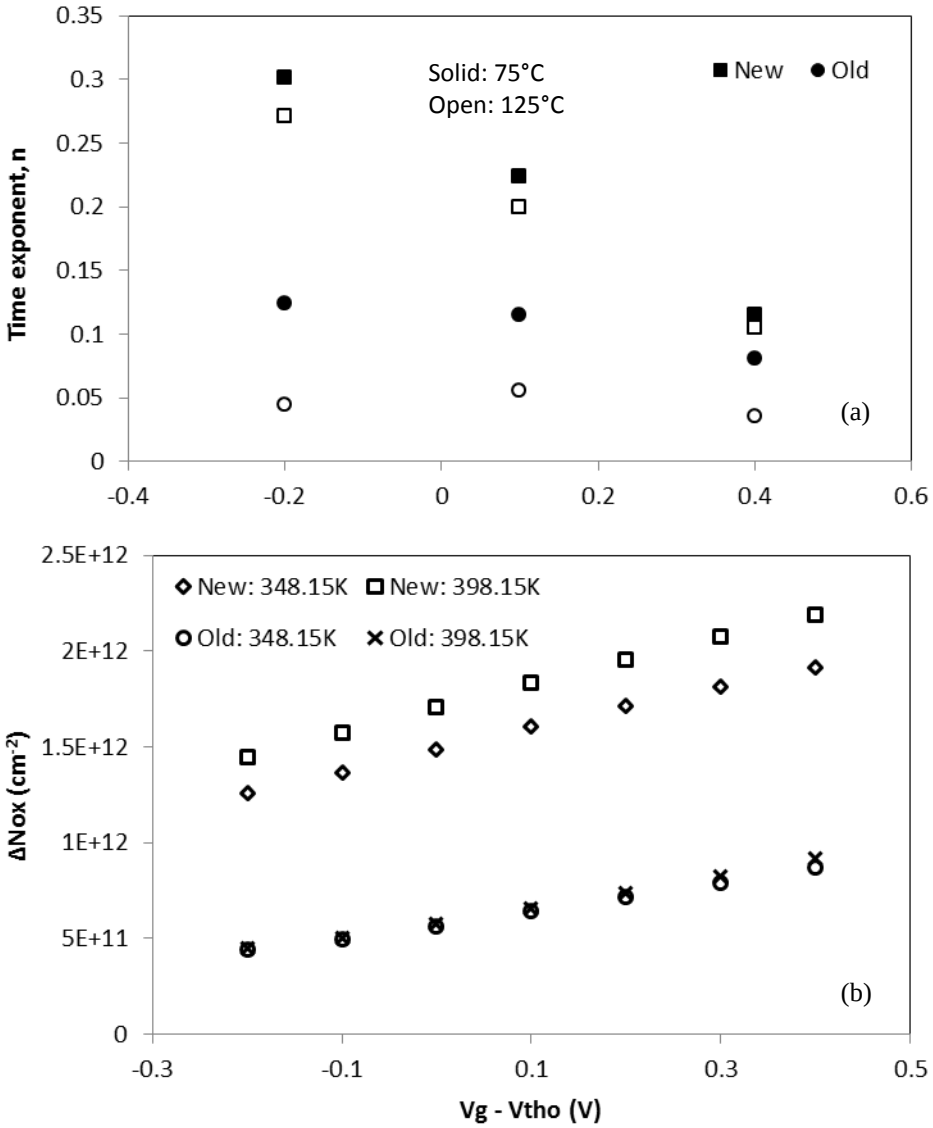
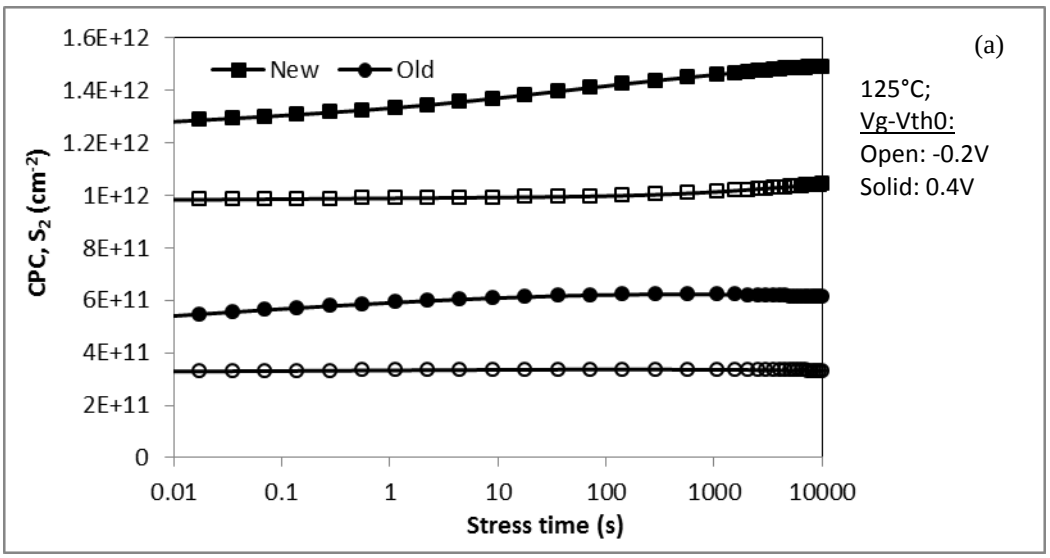


Figure 4.52 Plot for new define and default energy level under different stress temperature for (a) Time exponent versus $V_g - V_{tho}$ (b) Total positive charges concentration versus $V_g - V_{tho}$

The behavior of component of total positive charges which contributed in the degradation for different stress voltages as shown in Figure 4.53 (a) and (b) for E'centers and E'/Pb H complex concentration respectively was further probed. As observed in Figure 4.53 (a), the sub-threshold operation voltage shows that the generation of E'center concentration was almost saturated, but slightly increased,

approaching 10000s stress time while the super-threshold voltage shows the increasing of the E'centers generation when the stress time increased. In contrast, the E'centers concentration saturated and slightly reduced approaching 10000s stress time by using the default energy level. The generation of E'centers concentration using default energy level was smaller than using new define energy level for both sub and super-threshold voltage.

In Figure 4.53 (b), first impression on the concentration of generated ANPC increased as the stress time increased for both sub and super-threshold voltage. Closer observation indicated that the generated of ANPC during super-threshold operation regime increased throughout the stress duration for both default and new define energy level. In contrast, the generated ANPC during the sub-threshold operation regime only increased when the stress time was approaching above 1000s. Another closer observation indicated that the generated ANPC was shown to be higher for new define energy level as compared to default energy level similar to CPC concentration.



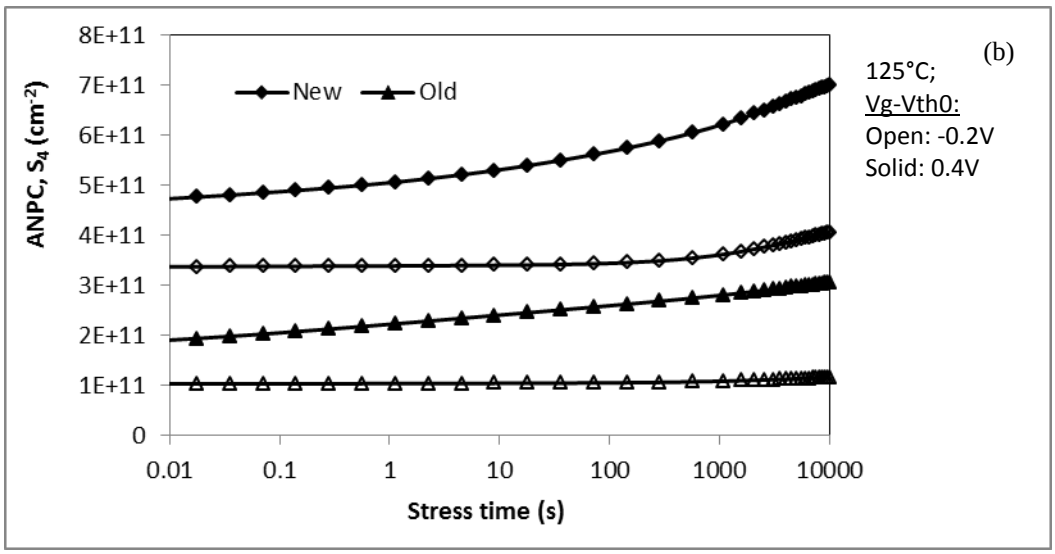
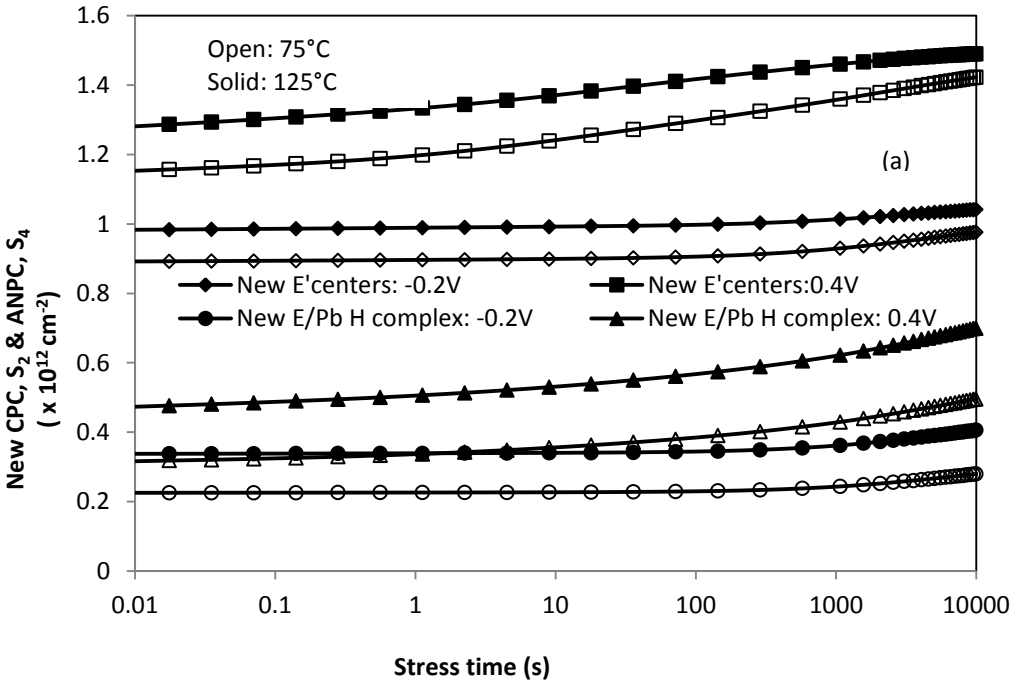


Figure 4.53 Component of positive concentration generated during NBTI stress for new define and default energy level consist of (a) CPC (b) ANPC

Figure 4.54 (a) and (b) show the CPC and ANPC complexes under different stress voltages and stress temperatures using new define and default energy level respectively. As shown in Figure 4.54 (a), the concentrations of generated CPC were higher than generated ANPC during the sub and super-threshold operation regime and

under higher stress temperature. This is in agreement with previous experimental works which highlighted that the generated of positive charges were thermally activated (Boo et al., 2012). Both components of positive charges were found to be temperature dependence. Therefore, the degradation during the sub-threshold operation regime was also thermally activated. This is not in agreement with (J. Franco et al., 2012) because the threshold voltage shift observed was not dependent on temperature during sub-threshold operation.

For comparison, the plot of default energy level presented in Figure 4.54 (b) gave different kinetics based on different stress temperatures for the sub and super-threshold operation regime. Above 1000s stress time duration, the CPC was higher for the lower stress temperature during the super-threshold voltage. In contrast, for sub-threshold operation, similar generated CPC concentration was observed for both stress temperatures. Upon approaching the 1000s, the generated CPC concentration started to reduce more for higher stress temperature hence during the 10000s stress duration, more generated E' centers concentration was observed during smaller stress temperature. However, the generated ANPC concentration for both sub and super-threshold is stress time and temperature dependence. As the stress time and stress temperature increased, the generated ANPC concentration too increased.



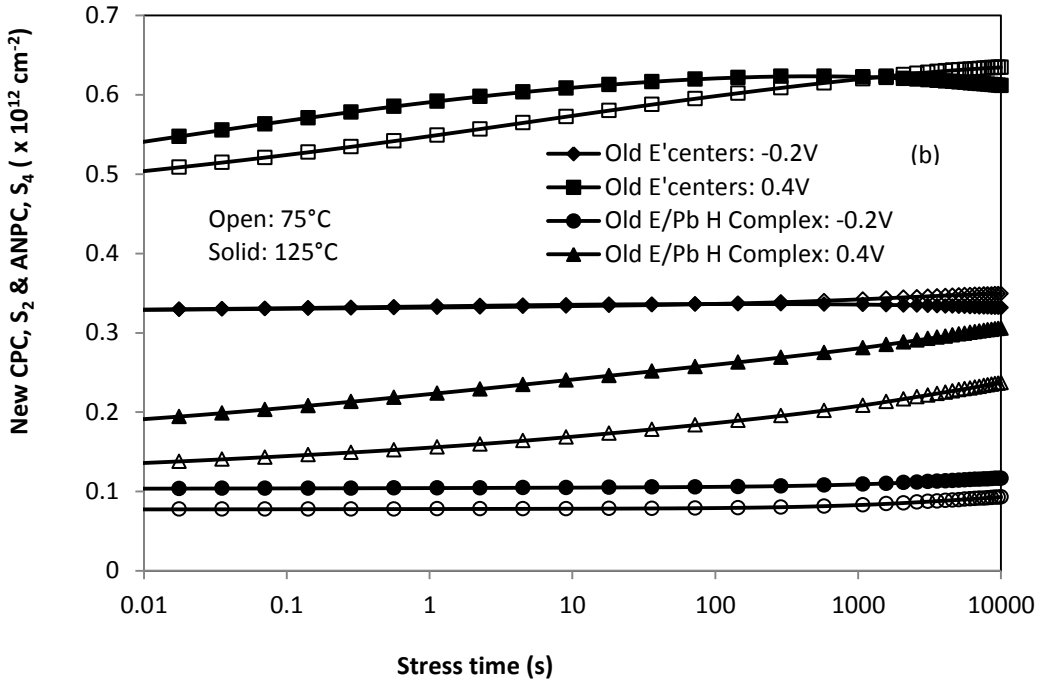


Figure 4.54 Plot of CPC and ANPC during sub and super-threshold voltage under different stress temperatures for (a) New define energy level (b) Old energy level

The lifetime of sub-threshold operation based on a hundred-year lifetime was estimated. The ΔV_{th} as a function of device lifetime which can be used in simulation study for circuit level degradation projection based on application-specific criterion (J. Franco et al., 2012) where it was readily understandable. Figure 4.55 (a) and (b) shows the level of device degradation in terms of ΔV_{th} as a function of device lifetime for new and default energy levels respectively for sub-threshold and super-threshold operation regime. The ΔV_{th} lines for each voltage were extrapolated to 10 and 100 years. The level of degradation in NBTI effect was assessed based on failure criterion is ΔV_t = 30mV (J. Franco et al., 2012). In the first impression for sub-threshold operation regime, based on the failure criterion target, the device can satisfy a hundred-year lifetime at sub-threshold operation voltage which was suitable for biomedical application which require extended device lifetime (J. Franco et al., 2012) for both new and old energy level. A closer observation as presented in Figure 4.55(c) shows that the threshold voltage shifted during the 10 and 100 years operation. For biomedical application devices, the sub-threshold operation regime which is for $V_g - V_{tho}$ = -0.2 V and up to $V_g - V_{tho}$ = 0.2 V meet the failure criterion target. The percentage different for threshold voltage shift extracted based on new define and default energy level is shown in the figure. There was significant difference on the prediction using default and new define energy level.

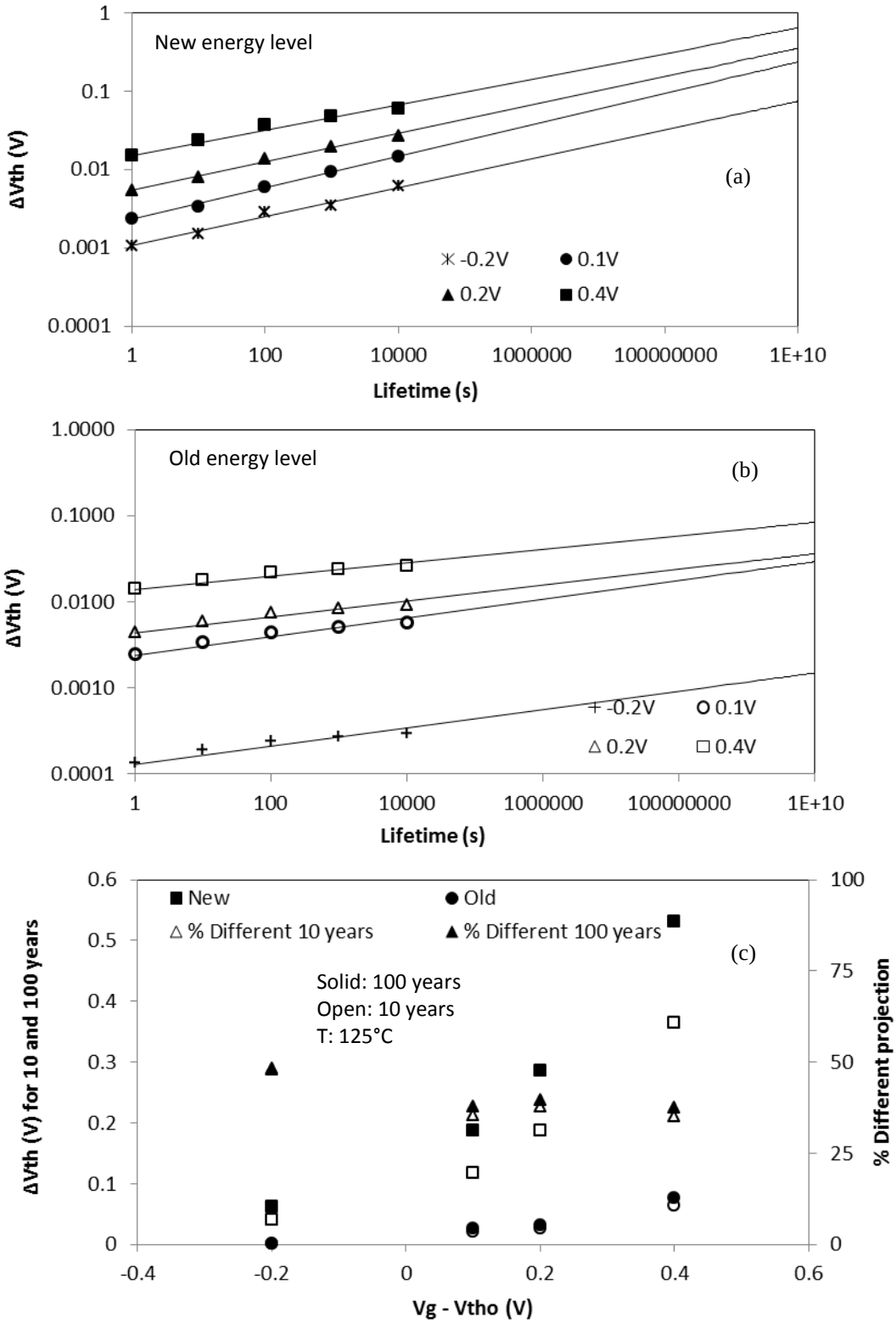


Figure 4.55 Power-law time dependence of extrapolated ΔV_{th} with respect to lifetime during sub and super-threshold operating regime for (a) New energy level (b) default energy level and (c) Estimation of ΔV_{th} after 10 and 100 years operation with the percentage different of estimation using new define and default energy level

4.4.6.2 Effect on CMOS Inverter performance

The integrated new defined energy level for each trap within the framework of two - stage NBTI model in mixed-mode simulation was implemented. In this work, the voltage transfer characteristic (VTC) of the CMOS inverter with default and new integrated energy level by varying the level of the precursor was analyzed and depicted in Figure 4.56 (a) to (c). In the CMOS inverter operation, when the V_{in} = V_{low}, the p-MOSFET was turned on to experience stress conditions. For the fresh inverter, the switching point was well aligned around $V_{dd}/2$.

However, as the NBTI stress has impact on the p-MOSFET during low input, the switching point of the output potential moved to a lower input voltage as shown in Figure 4.56(a) which was similarly observed in (Entner, 2007). The V_{out} was no longer $V_{dd}/2$. The VTC was magnified as depicted in Figure 4.56(b). It can be clearly seen that the increasing precursor led to a severe shift of switching point. The percentage of switching point shift from fresh inverter for default and integrated new energy level are 15% and 18% respectively at precursor of 2×10^{12} cm^{-2} as shown in Figure 4.56 (c).

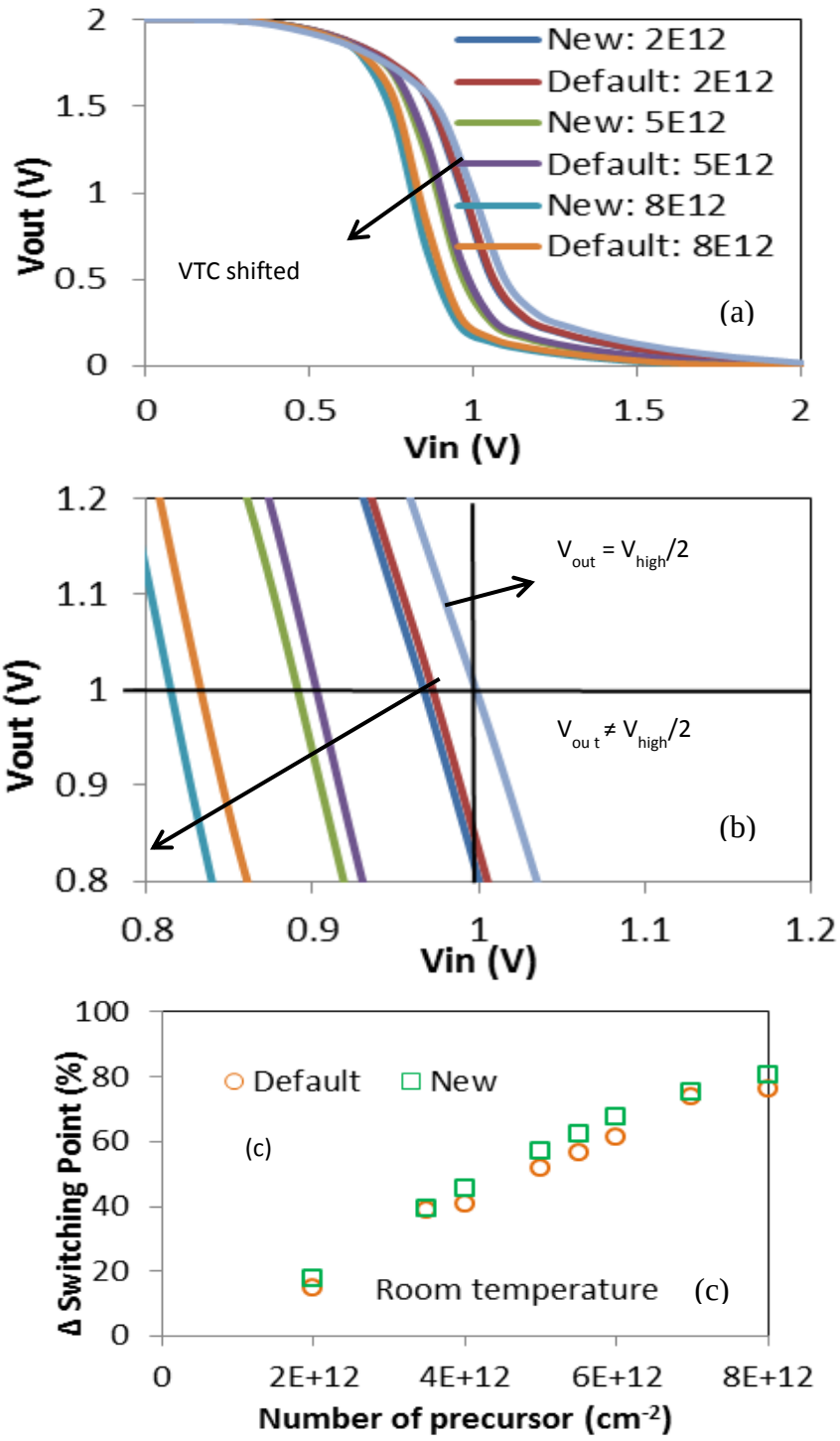


Figure 4.56 (a) VTC of CMOS inverter with and without degradation. (b) The shift of VTC is magnified, from (a). (c) Percentage of switching point shift

4.4.6.3 Lifetime Prediction

To further understand the limitation of the default energy level, the classical lifetime prediction by accelerating the test using a set of bias level higher than normally used in real operation based on the technology of the device (Kaczer et al., 2009) was implemented. For each of the bias levels, the stress time needed to reach a failure criterion of 0.1 V was extracted. The ensuing lifetimes were then extrapolated towards 10 year by fitting a power law to find its maximum operating voltage, $V_{gop,max}$. Figure 4.57 shows the extrapolated fitting a power law to the lifetime vs stress bias for default and integrated new energy level. Default energy level implied that the major contributor in the degradation is the hole trap. Hence, prediction using this model can lead to 57% error. Based on the same level of precursor, N_T = 2 x 10^{12} cm^{-2}, the maximum operating voltage for 10 year operation |Vgop,max|~ 1.2 V was obtained. This prediction was more accurate and similarly observed in (S. W. M. Hatta, 2013) for high-k based devices .

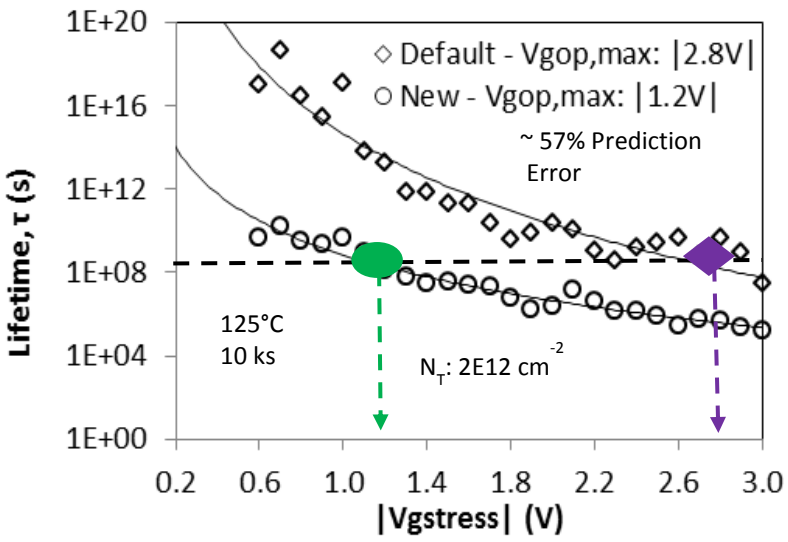


Figure 4.57 $V_{gop,max}$ evaluation for the 0.6 nm/1 nm HfO2/SiO2.

4.5 Conclusion

In this chapter, results based on the major contributions in this work were discussed. The discussion was made based on three main parts which consist of a study under hydrogen and non-hydrogen transport model and a study by using energy profiling approach.

The impact of static and dynamic characteristics of NBTI degradation on PMOSFET using MIG simulator has been investigated for hydrogen transport formalism study. A systematic simulation study was presented on the effects of static characteristic of NBTI degradation under different stress conditions and process variation in terms of EOT and substrate doping level variation. Based on this systematic simulation study, the threshold voltage change was observed. The change of threshold voltage was based on power-law where time exponent, n ~ 0.25 was observed subsequent to wide stress conditions with atomic hydrogen species.

On the other hand, the dynamic characteristics of NBTI degradation based on the systematic pulse simulation were developed to understand the behaviour of recoverable and permanent component. The *R* of dynamic NBTI by varying stress voltage, temperature, and duration were characterized. The effects of *EOT* were also investigated where a large *R* was found when high stress voltages and temperatures were applied. *R* was reduced as the number of stress cycles increased during a single run simulation based on varying recovery durations. In multiple runs wherein recovery durations varied in each run, the *R* was found to increase as recovery time increased. The *R* was larger in the *p*-MOSFET of a small *EOT* than in the *p*-MOSFET of a large *EOT*. These results suggested that the *R* of dynamic NBTI is consistent with

the classical R–D model and generalized R-D model with the hole-trapping effect mechanisms.

Under the non-hydrogen transport formalism based study, it was observed that the applied stress voltage and physical thickness of the dielectrics in the high-*k* metal gate stack in PMOSFETs exerts a certain influence on the degree of NBTI degradation. The degradation decreases for thicker SiO_2 IL under small stress voltage and increases under high stress voltage application. However, the degradation decreases for thinner HfO_2 and was not influenced by the stress voltage levels. The occurrence of the defect mechanism in the oxide bulk or interface region was also influenced by the stress conditions, physical thickness of the dielectrics, and number of precursor and dipole layer charges. The transformation of hole trapping into permanent trapped holes was thermally activated as proven by the recoverable component, *R* behavior. Optimizing the gate stack dielectric sub-layer physical thickness was essential to achieve a more reliable NBTI and high-*k* gate stack aging model.

From the new simulation framework based on energy profiling technique, new simulation evidence was uncovered indicating a limitation of default energy level where the hole trapping effect in pre-existing defect was the major contributor in the degradation mechanism. By adopting this integrated new energy level, the generated defects were taken into account as a major contributor in the degradation mechanism. This realistic model can be used by process engineer to improve the fabrication process by reducing the pre-existing defects which limit the lifetime of the devices.

In this study, the simulation technique for probing the energy distribution of positive charges was developed by adopting the numerical simulation method implemented by Sentaurus TCAD tools. By redefine the energy level of each of the positive charges, the AHT, CPC and ANPC can be probed over the entire energy range which confirmed to be in agreement with the experimental work by others. Energy profiling of different technology devices was comprehensively investigated and the distribution of positive charges generated subsequent to stress was reviewed. The devices that were investigated in this work included the high-k based devices, conventional dielectric SiO_2 with and without SiGe strained channel and FinFET.

All the different technology of devices showed high level of as-grown hole traps observed below Ev. The highest AHT observed was the planar high-k based devices. Above the Ev, which was within the energy band gap, the peaks were observed for all devices; however, their energy locations were not always the same. The planar Hf-based devices and FinFET have almost similar trend where more than one peak observed above the energy mid-gap. The highest peaks observed near E_c while the lower one apparent just above the mid-gap. The peak for FinFET was higher than that of planar Hf-based devices, suggesting that FinFET technology were much prone to NBTI. In contrast, for the conventional SiO_2 dielectric with and without strained technology, the peaks within the energy band gap were observed to be below and above energy mid-gap. The highest peaks were observed above Ec indicating the positive charges in SiO_2 dielectric devices are dominated ANPC. A similar trend was observed for both strained and unstrained devices. Another observation worth nothing here is that the highest peak located near E_c or above E_c regardless of technology will move to higher energy range as the stress time or temperature increased. This indicated that the CPC near E_c or the ANPC is depending on the stress conditions.

In order to understand the exact impact when the degradation was characterized based on default and new defines an energy level, three cases were investigated based on degradation during subthreshold operation, degradation of CMOS inverter and followed by the lifetime prediction of the device. During the sub-threshold operation, the time exponent, n observed for default and new define energy level was 0.1 and 0.3 respectively. The time exponent of 0.1 was referred to the pre-existing defect available in the device while the 0.3 was referred to the total defect contributed to the degradation consist of the CPC and ANPC which located near and above conduction energy level respectively. The degradation which characterized based on new define energy level found that the degradation was significant when stressed at higher temperature as compared to lower temperatures during the sub-threshold regime. However, the characterization using default energy level found that the degradation was not influenced by the stress temperature. More degradation was observed based on new define energy level where the concentrations of generated CPC were higher than generated ANPC during sub and super-threshold operation regime and under higher stress temperature.

The utilization of NBTI model based on default and new defines energy levels of CMOS inverter found that the degradation of the performance was higher when simulated based on new define an energy level NBTI model. The percentage of switching point shift from the fresh inverter for default and integrated new energy level were 15% and 18% respectively at precursor of $2 \times 10^{12} cm^{-2}$. For lifetime prediction assessment utilizing the default and new define energy level, the maximum operating voltage was 2.8 V and 1.2 V respectively. Therefore, there was a 57% error in the prediction when simulated using the default energy level.

CHAPTER 5: **CONCLUSION AND FUTURE WORKS**

5.1 Conclusion

Based on the simulation framework with hydrogen transport as the underlying mechanism, the interface trap generation and recoverable component characteristics were studied using the static and developed pulse simulation methods respectively. The results obtained from the systematic pulse simulation were analyzed using the threshold voltage shift. The recoverable component, R was extracted from the resultant dynamic threshold voltage shift which was consistent with the classical R–D model and the generalized R-D model with the inclusion of hole-trapping effect mechanisms. The characteristics of R suggested that the interface trap concentration is the underlying connection between the classical R–D model and generalized R-D model with the inclusion of hole-trapping effect mechanisms. The interface trap concentration represents the permanent component in both mechanisms. The proposed simulation approaches were able to indicate the behavior of R from the perspective of the R-D model.

Investigations on geometrical variation effect of high-k metal gate stacks due to NBTI using non-hydrogen transport formalism model concluded that the degradation was enhanced with thinner SiO_2 interfacial and thicker HfO_2 layer during lower stress voltage. However, as the stress bias increased, more degradation was observed in both thicker SiO_2 and HfO_2 layers. Due to more degradation observed for thicker HfO_2 layer devices regardless of stress voltage applied, the optimization in gate stack geometric process for better NBTI immunity can be focused by minimizing the thickness of HfO_2. With regards to the applied stress conditions in this work with higher density of precursor, further studies on the defect component associated with NBTI effects based on different HfO_2 thickness indicated that more degradation was

observed at the interface for thinner HfO_2 while more degradation was observed in the oxide bulk for the thicker HfO_2. On the other hand, the recoverable component, R was higher for both thinner SiO_2 interfacial and HfO_2 layers. Moreover, the R characteristics showed that the transformation of hole trapping into more permanent form is thermally activated. The influence of high-k integration issues on NBTI effects enhancement based on the non-hydrogen transport formalism shows that more threshold voltage shift was observed for higher dipole surface density. However, the generation of positively charged E'centers, S_2 and interface trap, S_4 was found to be higher in scaled SiO_2 interfacial layer regardless of the dipole layer concentrations.

Using the energy profiling approach, the defect components were shown to be sensitive to energy level and varied significantly over the energy range. This technique was applied to high-k based devices, strained and unstrained SiO_2 devices and FinFET devices. Different EOTs of the high-k based devices and fin width of FinFETs as well as strained technology gave different impacts on the energy distribution of charges. They also contribute to the different levels of degradation. Therefore, process optimization was essential for minimizing NBTI on the particular technology of devices. The comparison between default non-hydrogen transport model and energy profiling techniques on assessment of degradation for sub-threshold regime, mixed-mode simulation for CMOS inverter analysis as well as the lifetime prediction showed that the defect's energy level must be accurately defined in order to produce reliable projection of the developed devices in industry through the modeling and simulation of NBTI assessment.

5.2 Future work

Based on the work presented here, there are several aspects which can be extended through simulation-based studies on the hydrogen and non-hydrogen transport formalism.

Through the hydrogen transport formalism simulated using the MIG simulator, the pulse stress simulation setup developed in this work can be further used in understanding the correlation of the stress and recovery time within the context of R-D model through AC simulation setup. This is because most devices operated in integrated circuit experience alternating current. Recovery happens when the p-MOSFET is in the 'off' condition. Therefore, further work needs to be steered to investigate the recoverable component effect within the AC simulation setup.

The developments of the high-k based devices which introduced high pre-existing defects become significant issues that mitigate the NBTI problem which cause the performance and reliability of the devices to degrade faster. Hence, process optimization must be done by adopting a new propose, new define energy model to accurately characterize the device degradation. The exact gate stack thickness should be determined to produce longer lifetime of the devices. The characterization should also be implemented for multi-gate MOSFET and nano-wire MOSFETs. These two types of technologies were developed to reduce the drain-induced barrier lowering leakage current and increase the gate control. As for industry practice, development of those devices through virtual fabrication process was used to produce devices within particular specifications. Adopting the NBTI degradation model will provide added values to the device process parameters that can be optimized to increase the lifetime of the devices. The information regarding the defects properties can be extracted and

the understanding of the defects behaviour can be further developed. This is due to the very limited information available in literature to understand the defect properties of those devices within the context of defect's energy distribution.

Another possible extended work based on the energy probing technique utilizing new define energy level of defect charges is by taking into account the significant variation device-to-device specifically for nano-meter size p-MOSFETs. The simulation carried out in this work did not consider the device-to-device variation. After the fabrication process, the variations occurred normally consisted of the sources from gate line edge roughness, metal gate granulity, random dopant fluctuation, and gate work function fluctuation. Most works in literature highlighted the NBTI degradation from the perspective of hydrogen transport formalism. Hence, further work need to be carried out to include the variability effects on the energy distribution of the defect charges.

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S.Wan Muhamad Hatta, N.Soin, S.H.Abdul Rahman, H. Hussin and Y.Abdul Wahab, “Effects of the Fin Width Variation on the Performance of 16nm FinFETs with Round Fin Corners and Tapered Fin Shape”, International Conference on Semiconductor Electronics, Kuala Lumpur, 27 – 29 August 2014. (Oral presentation)

Y. Abdul Wahab, N. Soin, H. Hussin , ”Process-induced NBTI-imbalance of High-k/metal-gate deep-submicron CMOS”, International Conference on Semiconductor Electronics, Kuala Lumpur, 27 – 29 August 2014. (Oral presentation)

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H. Hussin, M. Muhamad, Y. A. Wahab, S. S. Shahabuddin, N. Soin and M. F. Bukhori, “A Study Using Two Stage NBTI Model for 32 nm High-k PMOSFET“,2013 IEEE International Conference on Electron Devices and Solid-State Circuits, The Hong Kong Polytechnic University, 3 – 5 June 2013. (Poster presentation)

H. Hussin and N. Soin, “Safe Operating Condition and Lifetime Estimation in p-MOSFET Device Due To Negative Bias Temperature Instability, IEEE Symposium on Industrial Electronics & Applications (ISIEA 2011), Langkawi, Malaysia, 25 – 28 September 2011. (Oral presentation)