# A FEEDFORWARD CONTROL FOR GRID-CONNECTED INVERTER UNDER UNBALANCED AND DISTORTED CONDITIONS

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## ABSTRACT

Grid-connected inverters utilizing renewable energy sources (e.g., photovoltaic, wind, fuel cell, etc.) are growing rapidly in recent years along with the constantly growing global demand for electricity. The utility is subjected to imbalance and distortion caused by unbalanced and nonlinear loads. Critical and random voltage disturbances could be established by time-varying loads like arc furnaces, the fluctuating output power of the wind and photovoltaic generation, voltage transients caused by line-start induction motors, and voltage transients associated with capacitor switching. These kind of voltage disturbances are stochastic in nature, with durations that differ from a small fraction of a cycle to some cycles. The two-level three-phase three-wire voltage-sourced inverter has become one of the main building blocks of renewable energy systems. In spite of weak grid condition; a grid-connected inverter must inject a synchronously regulated sinusoidal current to the utility grid with required low total harmonic distortion (THD) and high power factor. To overcome these challenges grid-connected inverters should provide unbalanced and distorted voltages. Hence, a new scalar implicit zero-sequence discontinuous pulse width modulation (IZDPWM) technique for three-phase three-wire two-level grid-connected voltage source inverters under the weak grid condition is presented. The proposed technique is the first scalar method that uses line-to-line voltages as reference signals. IZDPWM-based feedforward control strategy is proposed for current regulated grid-connected voltage source inverters under unbalanced and distorted condition. The feedforward control strategy is chosen because it can reject a large number of grid voltage harmonics simultaneously, while providing a clean sinusoidal current waveform to the grid. Regardless the grid topology, the compatible IZDPWM exactly copies the distorting harmonics of the grid voltage. Hence, a sinusoidal current is injected to the grid. IZDPWM-based closed loop controller minimizes low order harmonics in the grid current, and compensate for dc-link voltage ripple, deadtime delays, and

semiconductor device voltage drops. For straightforward and significant current control using PI, the three-phase ac current is transferred into the synchronous d–q rotating frame whereas the feedforward compensation of the grid voltage is implemented in abc frame. Appling IZDPWM-based controller; pure sinusoidal current is injected to the grid under balanced, unbalanced, and distorted conditions. Moreover, under weak grid condition in spite of phase voltages, line-to-line voltages are measured by two sensors only. Thus, overall system cost is reduced and reliability of control system is increased. IZDPWM-based feedforward control was extensively tested under balanced, unbalanced, and distorted conditions in both simulation and experimental testes. The compatibility IZDPWM with the line-to-line voltages feedforwarding leads to an adequate control performance with robustness against dynamic voltage disturbances. By applying the proposed IZDPWM-based feedforward control, high quality injected current with low THD (0.888 %) and high power factor (0.999) are obtained.

## ABSTRAK

Inverter disambungkan grid yang menggunakan sumber tenaga yang boleh diperbaharu (contohnya fotovoltaik, angin, sel bahanapi, dll) semakin pesat kebelakangan ini bersama-sama dengan permintaan global yang sentiasa berkembang untuk tenaga elektrik. Utiliti adalah tertakluk kepada keadaan tidak seimbang dan tidak sekata yang disebabkan oleh beban yang bersifat tidak linear. Gangguan teruk dan rawak voltan mungkin berlaku pada masa yang berbeza, seperti arka relau; generasi fotovoltaik, semasa transien turun-naik keluaran generasi kuasa angin dan fotovoltaik; transien voltan yang berkaitan dengan beban disambung selari, seperti motor aruhan line-start; dan menukar voltan transien disebabkan oleh kapasitor. Gangguan voltan yang bersifat stokastik ini berlaku, dengan jangka masa yang berbeza-beza dari sebahagian kecil daripada kitaran untuk beberapa kitaran. Inverter 2-aras voltan-bersumber tiga-wayar tiga-fasa telah menjadi salah satu komponen utama sistem tenaga boleh diperbaharui. Walaupun pada keadaan grid yang lemah; inverter bersambung dengan grid yang berkaitan mesti dimasukkan arus sinus serentak terkawal ke grid utiliti dengan kandungan THD rendah yang diperlukan dan faktor kuasa yang tinggi. Untuk mengatasi cabaran-cabaran inverters grid yang berkaitan perlu output voltan tidak seimbang dan tidak sekata. Tesis ini membentangkan teknik modulasi (IZDPWM) lebar scalar tersirat sifar-jujukan selanjar nadi baru bagi tiga fasa tiga dawai 2-aras disambungkan grid voltan sumber inverters di bawah keadaan lemah grid. Teknik yang dicadangkan adalah kaedah skalar pertama yang menggunakan talian ke talian voltan sebagai isyarat rujukan. Strategi kawalan berasaskan IZDPWM maklum awal adalah dicadangkan untuk inverters sumber voltan disambungkan grid terkawal semasa di bawah keadaan tidak seimbang dan tidak sekata. Strategi kawalan maklum awal ini dipilih kerana ia boleh menolak sejumlah besar grid voltan harmonik secara serentak, sambil menyediakan semasa bentuk gelombang sinus bersih ke grid. Tanpa mengira topologi grid, IZDPWM dapat melaras kandungan

harmonik tidak sekata voltan grid. Oleh yang demikian, arus sinus dimasukkan ke grid. Kawalan gelung tertutup yang berasaskan IZDPWM dapat merendahkan kandungan harmonik terendah dalam grid semasa, mengimbangi voltan sambungan DC, mengurangkan masa penukaran isyarat suis dan mengurangkan perbezaan voltan pada peranti semikonduktor. Untuk memudahkan kawalan menggunakan pelaras PI, pembolehubah tiga fasa semasa dipindahkan ke dalam bingkai berputar d–q manakala pembolehubah maklum awal grid voltan dilaksanakan dalam kerangka abc. Dengan menggunakan kawalan berasaskan IZDPWM arus sinus dimasukkan ke grid di bawah keadaan seimbang, tidak seimbang dan tidak sekata. Selain itu, di bawah keadaan grid lemah voltan fasa, voltan talian-ke- talian diukur oleh dua penderia sahaja. Oleh itu, keseluruhan kos dapat dikurangkan dan kebolehpercayaan sistem kawalan akan bertambah. Kawalan suap depan berasaskan IZDPWM telah banyak diuji dalam keadaan seimbang, tidak seimbang dan tidak sekata di dalam kedua-dua simulasi dan hasil eksperimen. Keserasian IZDPWM dengan voltan suap depan baris ke baris membawa kepada prestasi kawalan yang mencukupi dengan kelasakan terhadap gangguan voltan dinamik. Dengan menggunakan kawalan suap depan berdasarkan IZDPWM yang dicadangkan, THD yang rendah serta berkualiti tinggi disuntik ( 0,888 %) dan faktor kuasa yang tinggi ( 0.999 ) juga diperolehi .

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## LIST OF ABBREVIATIONS

| | |
|---|---|
| AC | Alternating Current |
| ASM | Average Switching Model |
| CMV | Common Mode Voltage |
| DC | Direct Current |
| DPWM | Discontinuous Pulse Width Modulation |
| DSP | Digital Signal Processor |
| DG | Distributed Generation |
| ECE | Energy Conversion Efficiency |
| FFT | Fast Fourier Transform |
| IGBT | Insulated Gate Bipolar Transistor |
| IZDPWM | Implicit Zero-sequence Discontinuous Pulse Width Modulation |
| MG | Modulator Ground |
| PI | Proportional Integral |
| PLL | Phase Locked Loop |
| PR | Proportional Resonant |
| PV | Photovoltaic |
| PWM | Pulse Width Modulation |
| SPWM | Sinusoidal PWM |
| SVPWM | Space Vector Pulse Width Modulation |
| THD | Total Harmonic Distortion |
| THIPWM | Third Harmonics Injection Pulse Width Modulation |
| UPS | Uninterruptable Power Supplies |
| VSI | Voltage Source Inverter |
| PCC | Point of Common Coupling |

## LIST OF SYMBOLS

| | |
|---|---|
| A | Ampere |
| C | Capacitor |
| MW | Mega Watt |
| $M_i$ | Modulation index |
| V | Volt |
| $T_{sw}$ | Period of the PWM modulation |
| % | Percent |
| θ | Grid voltage phase angle |
| $\omega_e$ | Grid Angular velocity |
| $f_{sam}$ | Sampling frequency |
| $f_{sw}$ | Switching frequency |

# CHAPTER 1: INTRODUCTION

## 1.1 Introduction

This chapter initially presents the background of the study. Then motivations and problem statement are described followed by objectives and significance contributions of this research in advancing the control method of grid-connected voltage source inverter under unbalanced and distorted conditions. The last section introduces the general organization of the thesis.

## 1.2 Renewable energy distributed generation

The penetration of renewable energy distributed generation (DG) systems in power grid are growing rapidly in recent years along with the constantly growing global demand for electricity (Bitar, Rajagopal, Khargonekar, Poolla, & Varaiya, 2012). A limiting factor is to conform to a number of code requirements aiming to maintain grid stability, to guarantee the safety, and transfer high quality of the electrical energy into the utility grid (Liserre, Teodorescu, & Blaabjerg, 2006c). Renewable energy sources are linked to the grid through power converters to transfer the produced dc power to the ac grid. The DG systems should be capable of presenting superior characteristics such as dynamic control of active and reactive power, stable operation within a range of voltage and frequency, voltage ride-through; reactive current injection during the faults, and engagement in stabilizing the grid (Liserre et al., 2006c; Peas Lopes, Moreira, & Madureira, 2006; Yun Wei & Ching-Nan, 2009; Zhe, Guerrero, & Blaabjerg, 2009). The application of high power electronic converters has been continuously advancing for generation, transmission, distribution, and delivery of electric power (Blaabjerg, Iov, Terekes, Teodorescu, & Ma, 2011). The main reasons are:

- Constant improvements in microelectronic technology empowered realization of advanced digital signal processing algorithms;

- Ongoing growth in energy demand led to close-to-the-limit using of the electric power utility facilities, calling for the employment of electronic power equipment for stability improvement;
- Further usage of green energy as a response to the global warming and environmental problems;
- Integration of large-scale renewable energy resources and storage systems in electric power grids.

Consequently, the application of renewable energy resources is increasingly being pursued as a supplement and an alternate to huge typical main power stations. The salient features of renewable energy sources are briefly introduced in the following subsections.

### 1.2.1 Photovoltaic power generators

The basic device of a Photovoltaic (PV) array is a cell made of doped silicon crystal in square or round shape. Solar cells are attached to make a module and modules are connected to form an array to produce electric power energy from the sunlight. The regularly reducing cost of PV modules results in significant cost reduction of the PV systems. However, larger sizes of photovoltaic generation units are limited. This is because the high cost of land, weak solar intensity in many areas around the world, and climate changes leading to unreliable sun exposure. Approximately, one acre of land would be needed to provide 150 kW of electricity (Lasseter, 2001). Small scale distributed PV panels (1-100 kW) yield cost effective solutions with higher reliability. Recently, under the green energy policies adopted by many countries, some interest in large scale PV farms appears. In general, the impact of photovoltaic generation profile on the system level, mainly voltage fluctuations and possible harmonic injection, is weak and it can be mitigated by injecting controlled reactive power through the PV inverter itself (Yun Tiam & Kirschen, 2007) or via nearby controlled reactive power sources. Therefore, the majority of PV studies are directed either towards the internal controls of the PV system

for better energy processing and precise power tracking (Weidong, Dunford, Palmer, & Capel, 2007) or towards the development of more exotic solar cell technology for greater efficiency and to lower the overall generation cost (Green, 2006). A PV generator is usually interfaced to the gird or load via a voltage source inverter (VSI) (Blaabjerg, Zhe, & Kjaer, 2004).

### 1.2.2 Wind power generators

Wind energy has been employed for many years in electrical energy generation. A wind turbine is made up of a rotor, turbine blades, generator, drive or coupling device, shaft, and the nacelle containing the gearbox and the generator drive (Johnson & Smithior, 1976). Current wind generators can produce clean electricity as individuals or as wind farms. Electricity capacity is limited by the amount of wind, so the wind plants should be installed in windy areas. It has expected the electrical efficiency of 20-40%, and the expected power sizes are in the range of 0.3 KW to 5 MW (Muljadi, Butterfield, Parsons, & Ellis, 2007; Petru & Thiringer, 2002). Modern power electronic converters are widely employed to fit the features of wind turbines with the grid interconnections requirements such as frequency, voltage, active and reactive power, and harmonics (Zhe et al., 2009). Wind farms have been found in areas with heavy wind profile. Large ratings such as 640 MW have been installed in Kriegers Flak 30 km south of Trelleborg (Andersson, Petersson, Agneholm, & Karlsson, 2007). Due to the large penetration of wind turbines and the chaotic nature of wind power generation, the impact of the wind generation on system performance is remarkable. Extensive research efforts are ongoing in addressing and mitigating the impact of wind turbines on system operation, stability, planning and reliability , power quality, and pricing (Billinton & Wangdee, 2007; Matevosyan & Soder, 2006).

### 1.2.3 Fuel cells

The fuel cell device is able to produce electric power and thermal energy through electrochemical processes (Ellis, von Spakovsky, & Nelson, 2001; Farooque & Maru, 2001). It could be considered as a battery supplying electric energy as long as its fuels are continued to supply. It generates clean power through the use of liquid fuels and gaseous. Fuel cells are able to use various hydrogen-rich fuels such as natural gas, gasoline, biogas or propane. They may perform in a wide range of temperatures and pressures that differ from atmospheric to hundreds of atmospheric pressure (Ellis et al., 2001). The capacity of fuel cells differs from 1kW to few MW for portable and stationary models, respectively. A fuel cell generator is usually interfaced to the grid or load via a voltage source inverter (Blaabjerg et al., 2004).

### 1.2.4 Energy storage systems

Employing energy storage devices in an electricity generation and supply system makes it possible for the decoupling of electricity production from demand (Lukic, Cao, Bansal, Rodriguez, & Emadi, 2008; Ribeiro, Johnson, Crow, Arsoy, & Liu, 2001). Basically, the electricity that can be generated on the occasion of either low demand low generation cost is shifted in time for release on the occasion of high demand high generation cost or when no other generation is available. Proper integration of renewable energy sources with storage systems enables for a larger market penetration and brings about major energy and emission savings. Current technologies enable efficient means of energy storage. Common among these are batteries, super-capacitors, flywheels, and super-conducting magnetic energy storage (Ribeiro et al., 2001). Energy storage devices have important roles, in DG systems, such as enabling fast load pick-up, enhancing the reliability, and flatting the generation profile in non-dispatchable sources (McDowall, 2001).

### 1.2.5 Hybrid systems

To improve the efficiency and generation characteristics, hybrid DG energy sources have been proposed (Ke, Xinbo, Mengxiong, & Min, 2009). DG systems depending on either solar or wind energy are difficult to rely on due to seasonal and diurnal variations of these sources. In (Daniel & Ammasaigounden, 2004) a hybrid system of a photovoltaic array and a wind-driven induction generator has been studied.

## 1.3 Grid-connected inverters under weak grid condition

DG systems are connected to the power grid that may experience any unbalanced or distorted voltage at the point of common coupling (PCC). The unbalanced and distorted conditions are typically attributed to nonlinear loads like diode rectifiers and adjustable-speed ac motor drives. The non-sinusoidal profile of the grid voltage waveform has adverse effects on the injected grid current. DG systems have to address this problem and ensure high-quality current injection to the utility in all grid conditions. L and LCL are the commonly used filters in order to suppress the current harmonics related to inverter switching frequency. Whereas both L and LCL low pass filters don't naturally attenuate the injected current's low-order harmonics attributed to the grid voltage disturbance. Therefore, the mitigation of the current disturbance under weak grid condition is a prominent aspect in control of the grid-connected inverters (Erika & Holmes, 2003). The adverse effects of the distorted grid voltage on the quality of the injected current are eliminated in different current regulators. The first introduced method uses multiple proportional resonant (PR) compensators in order to achieve infinite loop gain at targeted low-order harmonics frequency [26]. PR compensators effectively suppress the unwanted harmonics and eliminate the steady-state error. Nevertheless, excessive computation makes the controller costly. Moreover, PR controllers may not serve in compensating numerous harmonics and instability experienced in its implementation (Liserre et al., 2006c). Feedforward control is another alternative that tackles the power quality problems

in DG systems at random and non-periodic circumstances (Li, Ruan, Pan, & Wang, 2013). This reliable scheme may reject dynamic voltage disturbances in a wide range of low-frequency harmonics and provides a fast response.

## 1.4 Problem statement

Utility grid is subjected to unbalanced and distortion caused by unbalanced and nonlinear loads (Rodríguez et al., 2012; Xu, Tang, & Xie, 2013; Yaoqin, Jiqian, & Xiaowei, 2014). In unbalanced and distorted grid voltage condition, grid-connected inverters need to output unbalanced and distorted three-phase voltages in order to inject a balanced three-phase current into the grid (Xu, Xie, & Tang, 2014a, 2014b). Hence, the inverter has to exactly copy the distorting harmonics included in the waveform of the grid voltage. That can be realized by measuring distortion profile of the grid and online feedforwarding it to the PWM modulator (Abeyasekera, Johnson, Atkinson, & Armstrong, 2005; Li et al., 2013; Wang, Ruan, Liu, & Tse, 2010; Xu et al., 2014b). All the existing PWM modulators use phase voltages as reference signals. Therefore, feedforward scheme necessitates wye connection at the grid side; and three voltage sensors are required in order to measure the grid distorted phase voltages. However, in applications with a delta connection, feedforward control may not serve because phase voltages are not measurable. On the other hand, under unbalanced, distorted condition, online conversion of line-to-line values into phase values is crucial task.

## 1.5 Objectives

The aims of this thesis are as follows:

1. To introduce a new discontinuous pulse width modulation method that uses line-to-line voltages as reference signals;
2. To implement the proposed scheme under open-loop control strategy to obtain the steady state performance of the VSI system;

3. To develop a closed-loop control strategy for grid-connected operation under unbalanced distorted conditions;
4. To validate the proposed controllers through experimental verifications.

## 1.6 Thesis outline

This thesis is structured in 6 chapters; chapter one is an introduction to the project, containing short background, problem statement and the goals of the project. In chapter two the relevant literature on the grid-connected inverters topologies and control techniques under weak grid condition have been investigated. Chapter three focuses on the design of scalar implicit zero-sequence discontinuous pulse width modulation (IZDPWM) technique based on line-to-line voltages for two-level three-phase VSIs. The performance of the proposed modulation technique as an open loop controller is demonstrated and supported by simulation results. Chapter four presents IZDPWM-based feedforward control for a gird-connected inverter under weak grid condition. Chapter five deals with the experimental implementations of the proposed method. Chapter six includes concluding and directions for future work.

# CHAPTER 2: INVERTER-BASED DG INTERFACE

## 2.1 Introduction

Power converters, as an essential part of the integration of the distributed generation units, enables the flexible and efficient link of renewable energy sources to the main distribution power grid (Blaabjerg et al., 2011). Along with the improvement of economical and grid friendly converters, they are widely used in the grid-based systems. This chapter presents a survey on the inverters topology and control in DG systems.

## 2.2 DG interface topology

In addition to the electrical specifications, the selection of an appropriate structure for the inverter depends on various concerns including cables, electrolytic capacitors, lifetime, cost, and efficiency. Moreover, an inverter with the passive filter used in DG systems should fulfill a number of requirements that are given by nationwide and worldwide codes.

### 2.2.1 Inverter topology

In commercial grid-connected renewable energy systems, cost and energy conversion efficiency (ECE) of converters are the two major drivers to determine the payback period of the overall system (Ozkan & Hava, 2014). Considering the power level, single-phase and three-phase inverters are available in the market. Single-phase inverters cover low-range power 1-5 kW feeding low voltage distribution systems; whereas the three-phase inverters are utilized in a power range larger than 10 kW reaching MW levels. The output power of a single phase inverter is not a constant value, hence, to limit adverse effect of pulsating power higher amount of dc capacitors are needed. In balanced condition the output power of a three-phase inverter is a constant value, therefore, relatively small amount of dc capacitor is

required that enhance the system lifetime and reliability. Three-phase three-wire two-level voltage source inverter topology, which serves as the basis for nearly all three-phase inverters, is presented in Figure 2-1. In this topology, only six switches have been used. The output line voltage can be at two voltage levels, i.e. +$V_{dc}/2$ and -$V_{dc}/2$. However, a PWM strategy allows the output rms voltage to be readily controlled. Grid-connected inverter can be configured with or whithout transformer (Ozkan & Hava, 2014). Transformerless VSIs are available in power ratings 10 kW to several tens of kW, and they are generally connected to low voltage distribution systems directly (Kerekes, Liserre, Teodorescu, Klumpner, & Sumner, 2009). The leakage current problem is crucial in transformerless grid-connected PV inverters (Cavalcanti et al., 2010).

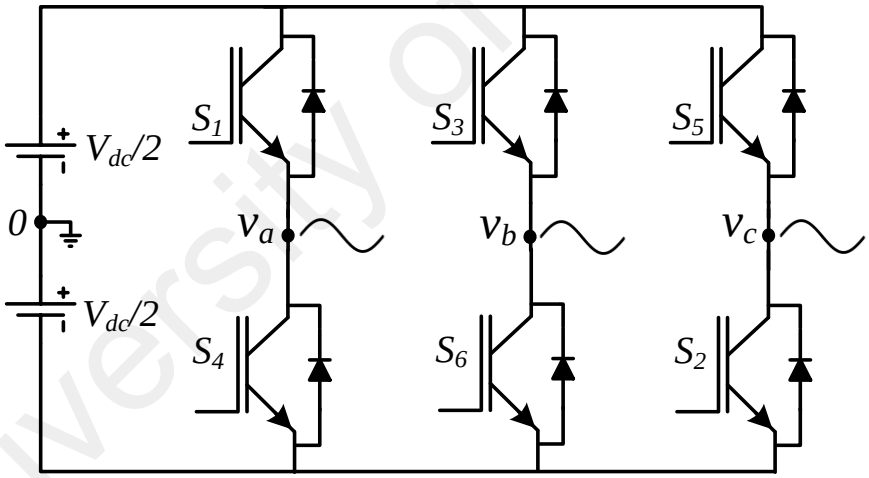



Figure 2-1: Three-phase three-wire two-level VSI.

Regarding safety issues, there are strict regulatory restrictions on ground leakage current in PV systems. Advanced scalar PWM methods with zero sequence voltage injection, for better dc voltage utilization and lower switching losses, in such a grounded system is avoided, as there is a path for zero sequence currents. Moreover, due to lack of a line frequency transformer, transformerless systems exhibit better ECE characteristics as compared to their

transformer based counterparts. However, the transformerless grid-connected inverter topology needs more complicated methods to maintain the dc current and leakage current under control. The inclusion of a transformer between the power system PCC and the inverter is necessary for some countries due to grid connection standards. Due to core and copper losses, the transformer may consume as high as 1-2 % of ECE. Furthermore, the inclusion of the transformer increases the cost, cooling, and real estate requirements. Despite these drawbacks, the transformer allows the connection to high voltage systems by voltage ratio changing, eases the grounding, reduces capacitive leakage current problems, and allows zero sequence voltage injection to increase the dc bus voltage utilization and to reduce switching losses of the inverter. However, without line frequency transformer also isolation can be achieve using a high-frequency transformer in dc-dc converter stage (Blaabjerg et al., 2004). It is desired to use the galvanic isolation transformer in the input high-frequency section rather than at the output line frequency because the line frequency transformer is heavy and costly. Another function of high-frequency dc-dc converter is boosting the inverter input voltage, to be able to produce required magnitude of the output ac voltage.

The multilevel inverter is suitable for high power applications (J. Rodriguez, Jih-Sheng, & Fang Zheng, 2002). A major advantage of this inverter is output voltage harmonic content reduction while maintaining lower switching frequency. While the inverter levels raise the output voltage total harmonic distortion (THD) reduces, and once the inverter levels reach infinity, the THD lowers to zero. The idea of multilevel inverters begins once the three-level inverter was presented by (Nabae, Takahashi, & Akagi, 1981). Multilevel inverters are usually classified in three common topologies; diode-clamped, flying capacitor and cascaded multilevel inverter. Figure 2-2 shows diode clamped three-phase three-level inverter topology. It consists of twelve controllable power semiconductor switches with freewheeling

diodes and six clamping diodes. The particular dc bus is divided by a couple of capacitors into three levels. MLI has a complicated network of switches compared to the conventional inverter. The high number of switches combinations leads to complexity in the control compared to the basic inverters (J. Rodriguez et al., 2002). Hence, MLIs with more devices are more expensive to implement and more prone to malfunction (Babaei & Hosseini, 2009).

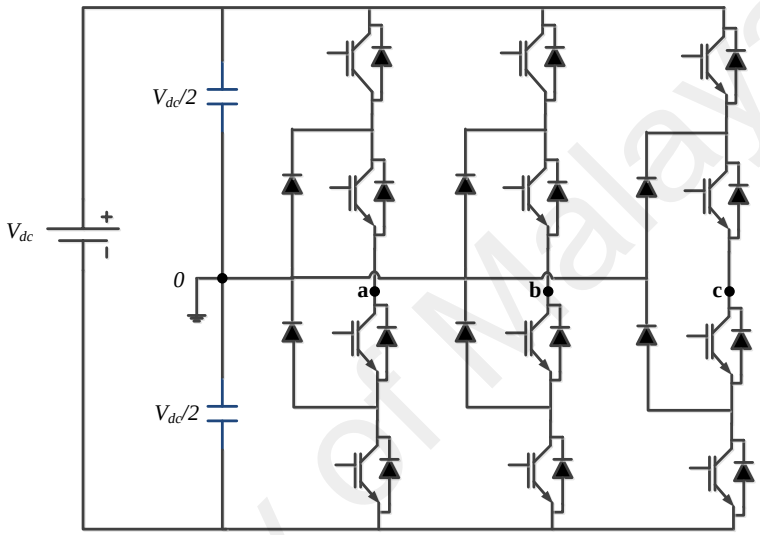



Figure 2-2: Three-phase three-level diode clamped inverter.

### 2.2.2 Filter topology

The particular function of the filters in VSI-based DG systems is twofold. In one hand dominant inductive behavior of the filter circuit is essential to ensure the appropriate operation of the voltage source inverter while is linked to the utility grid with uncontrolled voltage source specifications. On the other hand, VSI-based DG systems are switched at a carrier frequency that create voltage harmonics, hence, the filter should prevent associated current harmonics injecting into the utility which may disrupt some other vulnerable equipment (Min, Blaabjerg, Yongheng, & Weimin, 2013). The most common type of filter is a pure inductance L which serves as an impedance for absorbing the voltage variation to comply with the two aforementioned requirements. In applications about several kW power

level, such as the majority of common PV systems, the inverter switching frequency can be higher and even smaller value of inductors may fulfill the requirements. In applications about and over several hundreds of kW, such as the wind turbine systems, the inverter switching frequency usually is lower to reduce switching losses. Therefore, in high power converters employing a higher amount of reactors to suppress the injected current harmonics to meet the requirements become bulky and quite expensive (Rockhill, Liserre, Teodorescu, & Rodriguez, 2011). Furthermore, the inverter transient response can be poor. LCL filter is another alternative, which offers 60 dB per decade attenuation for the PWM switching harmonics. Using LCL filter, the possible minimum size of the filter elements can be obtained (Prodanovic & Green, 2003). This is also an important feature for small-scale inverters, such as photovoltaic inverters, to reduce the filter size and ease the packaging. However, due to the additional dynamics imposed by the LCL filter, the control complexity increases. In a system level, such as photovoltaic or wind parks, the important issue relates to the disturbances generated by a number of certain harmonics. Consequently, a chance is to apply a bank of tuned LC trap filters that have a benefit to prevent particular harmonics that could degrade the voltage quality. This kind of alternative is specially suitable for high power converters switching at hundreds of Hz, creating PWM harmonics at so lower frequency that it is hard to adopt a low pass filter such as the LCL filter. This type of filter makes a 60 dB/dec attenuation after the resonance frequency. (Jalili & Bernet, 2009). Therefore, the filter resonance frequency need to be significantly far from the inverter PWM switching frequency yet not so much that it does not challenge the current controller.

## 2.3 Inverter Control

Electric powered grids are generally complicated and dynamic systems troubled by multiple scenarios such as continual interconnection and disconnection of electric loads,

disturbances, and resonances due to the harmonic currents flowing from the grid lines, faults resulting from lightning strikes and mistakes in the functioning associated with electrical equipment (Wasynezuk, 1983; Zhe et al., 2009). Consequently, grid parameters are not regarded as constant magnitudes when a power converter is linked with the actual grid, nevertheless, they should be consistently administered in order to ensure that the grid state is suitable for the proper functioning of the power converter. In addition, if the power handled by means of this particular power converter cannot be ignored according to the rated power of the grid at the PCC, the grid parameters may be considerably impacted by the action associated with this type of power converter. For that reason, electrical power converters cannot be viewed as basic grid-connected apparatus simply because they maintain a great interactive connection with the grid which enables it to actively be involved in supporting the grid frequency and voltage, mostly when high levels of power are considered for that power converter (Vasquez, Mastromauro, Guerrero, & Liserre, 2009). This means, nevertheless, how the grid stability and also security ailments can be severely impacted in networks with expanded usage of electric power converters, seeing that could be the situation connected with dispersed renewable energy systems (Liserre et al., 2006c). Because of this, numerous global grid codes come in over the past several years as a way to manage behavior associated with solar and wind renewable energy systems in the both normal steady-state and irregular transient conditions, like grid faults problems (Tsili & Papathanassiou, 2009). These grid codes talk about the particular voltage and frequency restrictions inside of that the solar and wind generators really should keep on being linked with the particular grid whilst making sure dependable function. Consequently, in DG systems, power converter needs to properly monitor the grid parameters at the PCC to disconnect the converter once the parameters exceed the boundaries established through the grid requirements. Grid monitoring algorithms ought to identify the grid condition in a very fast and also to exact method as a way to satisfy

equally accuracy and also time reaction specifications required through the grid limitations (Tsili & Papathanassiou, 2009). In general an inverter-based DG system in addition to transferring the particular produced power to the network has an advanced control that allows capabilities such as dynamic management of active and reactive power, stable functioning inside a range of voltage and frequency, voltage ride-through fault condition, reactive current injection during faults, participation in grid controlling work like primary frequency control, and so forth. A broad literature review is presented in order to cover grid demands, current control, and voltage control methods.

### 2.3.1 Grid demands

As a result of raising the volume of distributed power generation systems linked to the grid, new and stricter codes regarding power quality, safe operating, and islanding protection are supplied. Consequently, the particular management involving with distributed generation systems need to be enhanced to fulfill the prerequisites regarding utility grid interconnection (Blaabjerg, Teodorescu, Liserre, & Timbus, 2006). A brief introduction into the most relevant control requirements of a DG system that stated in the grid codes follows.

#### 2.3.1.1 Grid synchronization

The most extended synchronization method in engineering applications, the phase locked loop (PLL) is usually a closed loop system where an interior oscillator is handled to adopt some output periodical signal (Karimi-Ghartemani & Iravani, 2004; P. Rodriguez et al., 2007). Presently, grid-tie power converters provide modern energy semiconductor products functioning with switched setting also at how much mega-converters, which in turn allow a top level of command. Presently, grid-tie power converters are established using modern power semiconductor products functioning in switching mode even at a mega power level,

which makes it possible for a superior control. Using advanced PLLs a synchronous control systems is applied to this kind of converters (P. Rodriguez et al., 2007). Single-phase grid-connected converters synchronization lies in precise detection of the characteristics of the grid voltage. Generally, the key involving characteristics for interfacing these type of inverter to the grid are the amplitude plus the phase angle of the fundamental component of the grid voltage. Grid synchronization approaches have a specific likeness for the harmonic recognition approaches employed in power systems and can categorize into two major groups are the frequency domain and the time domain detection techniques. The frequency domain detection approaches usually are depending on the discrete implementation of the Fourier analysis. The time-domain detection techniques use some type of adaptive loop that permits an interior oscillator to be able to track the fundamental component of the input signal. Three phase synchronization is not exactly same as the synchronization technique utilized in single phase systems, considering that in a three-phase system any of three phases do not perform autonomously but practice it within a coordinated mode, maintaining particular interactions with regard to phase angle and also phase sequence. As a result, a three-phase voltage needs to be recognized being a vector composed of three voltage elements. The vector and the revolving speed of a three-phase grid voltage maintain constant whenever balanced sinusoidal waveforms exist with the same amplitude, relative phase shift, and frequency. However, in practice, there are numerous nonidealities within power systems that result in some disturbances in the three-phase voltage vector. Any grid-connected power converter is particularly vulnerable to voltage disturbances due to the fact its control system might lose controllability on the power signals, that may lead to trip protection systems or may even damage the power converter under weak circumstances. In addition, an electric power converter can interact with the grid at the PCC to mitigate the adverse effect of the voltage disturbances. Hence, the particular voltage vector needs to be adequately detected by the

synchronization technique under weak gird condition (Karimi-Ghartemani & Iravani, 2004). In the unbalanced voltage condition, the positive and negative sequence parts should be detected by distinct diagnosis methods and handed to the control system to respond appropriately to this type of voltage disruption. Consequently, three-phase electric power converters grid synchronization requires the effective use of sophisticated recognition systems, especially meant to both equally reject high order voltage distortion harmonics and distinguish the sequence components of the voltage vector in a fast and precise manner (Gonzalez-Espin, Figueres, & Garcera, 2012). In particular, the real-time detection of the voltage vector positive and negative sequence components can be a crucial concern in the control of distributed generation and storage systems, flexible AC transmission systems (FACTS), and uninterruptible power supplies (UPS) (Teodorescu & Blaabjerg, 2004). In that applications, the positive and negative sequence voltage components are likely to be used for the converter synchronization, power calculation, and control variables transformation from the stationary frame into the synchronous rotating frame. For advanced synchronization of power converters under unbalanced and distorted grid circumstances the decoupled double synchronous reference frame PLL and the dual second order generalized integrator frequency locked loop are suitable solutions to be used (P. Rodriguez, Luna, Ciobotaru, Teodorescu, & Blaabjerg, 2006; P. Rodriguez et al., 2007).

#### 2.3.1.2 Power quality

DG system output power quality is a crucial factor. The power quality is primarily ruled through codes and requirements on frequency, voltage, and harmonics (Castilla, Miret, Camacho, Matas, & de Vicuna, 2013). Usually, regional rules made by the grid providers employ in many countries but significant efforts are made throughout the world to enforce a number of grid prerequisites which might be followed by various countries. Essentially the

most applicable global standards for the grid are developed by IEEE (Institute of Electrical and Electronics Engineers) in the United States, DKE (German Commission for Electrical, Electronic and Information Technologies of DIN and VDE) in Germany, as well as IEC (International Electrotechnical Commission) in Swiss. Deviation of a DG system from these requirements symbolizes out-of-bounds circumstances and may even need disconnection from the electric grid. Some of the important grid prerequisites which have an essential impact on the control and performance of a DG system are as follows.

**(a) DC current injection**

DG system control should prevent dc current injection since a certain amount of dc current results in power transformer saturation, overheat, and even system trip. In the case of using galvanic isolation transformer common current injection to the grid is very limited, however, in applications like transformerless photovoltaic systems, this problem need more attention. The allowable upper limit of the grid dc current identified by different standards are given in Table 2-1 ("IEC Standard 61727," 2002; Morari & Zafiriou, 1989; "VDE, DIN 0126-1-1," 2006).

Table 2-1: The upper limit of the grid injected DC current

| **IEEE 1574** | **IEC61727** | **VDE 0126-1-1** |
|---|---|---|
| $\boldsymbol{I_{dc}}$**<0.5**(%) **of the rated RMS current** | $I_{dc}$<1(%) Of the rated RMS current | $I_{dc}$<1(A) Maximum trip time 0.2 sec |

In IEEE 1574 and IEC 61727 standards, the dc component of the current should be determined applying Fast Fourier Transform (FFT) analysis and there is no maximum trip time. Moreover, the dc current should meet the limitation under 1/3, 2/3 and 3/3 of the nominal load current tests. According to VDE 0126-1-1, dc current is measured by a specific

current sensor and in the case of exceeding the threshold, disconnection is required in 0.2 seconds.

**(b) Current harmonics**

The DG systems output current should have limited distortion to avoid any damage to the sensitive equipment connected to the utility grid. The allowable upper limit of the grid current harmonics identified by IEEE 1547 and IEC 61727 standards are given in Table 2-2 ("IEC Standard 61727," 2002; "IEEE Guide for Conducting Distribution Impact Studies for Distributed Resource Interconnection," 2014).

Table 2-2: The upper limit of the grid current harmonics

| **Individual harmonic order(odd)*** | $h<11$ | $11\leq h<17$ | $17\leq h<23$ | $23\leq h<35$ | $h\leq 35$ | **Total Harmonic Distortion THD** |
|---|---|---|---|---|---|---|
| **%** | 4.0 | 2.0 | 1.5 | 0.6 | 0.3 | 5.0 |

*Even harmonics are limited to 25% of the odd harmonic limits.

**(c) Power factor**

According to IEC 61727 code, the PV grid-connected inverter should operate in a lagging power factor more than 0.9 at higher than 50% of nominal power ("IEC Standard 61727," 2002). IEEE 1574 as more general standard, has no requirement regarding the power factor and reactive power injection is allowed in distributed generation systems ("IEEE Guide for Conducting Distribution Impact Studies for Distributed Resource Interconnection," 2014). In VDE 0126-1-1 also there are no requirements for power factor ("VDE, DIN 0126-1-1," 2006).

#### 2.3.1.3 Islanding

A higher penetration of conventional and renewable energy technologies in distributed power generation systems (DPGSs) are changing the power system control. There is a fast evolution trend towards flexible grids that may consist remarkable amount of storage systems, able to work in island condition and could be connected through FACT systems (Bo, Xuesong, Jian, Caisheng, & Li, 2013; Peas Lopes et al., 2006). This kind of complicated DPGS units needs distinct requirements based on their power level and the level of integration with the utility power grid (Binyan, Xiaodai, & Bornemann, 2015). A possible island mode detection is a crucial task in DPGS control. In a low power DPGS such as PV systems, this function is defined as an ‘anti-islanding requirement to emphasize on the different action of grid operator that the DPGS unit should disconnect in the event that the main power grid should stop to energize the distribution line. High power DPGS such as wind plants, have totally different requirements and generally in the event that the main power grid should stop to energize the distribution line, instead of disconnection the DPGS unit maintain energizing the distribution line and contribute to the stability of the power system. The most recent grid standards require low voltage ride through capability, which means that DPGS units should remain connected during grid faults. Therefore, only low power DPGS units are involved in islanding detection. Nevertheless, the DPGS is changing toward smart micro grid (SMG) and the upcoming scenario may be required capability of stand-alone operation even in faults condition that the main power grid should stop to energize the distribution line. While generation control in grid-connected inverters is straightforward, significant complexities appear in the micro grid operation mode. A reliable operation of a micro grid system strongly relies on an effective control method of the generators. The main control target of micro grid system is to attain accurate power sharing whilst retaining close regulation of the frequency and voltage magnitude (Peas Lopes et al.,

2006). The mismatch between load and generation can collapse the micro-grid system (Mohamed & El-Saadany, 2008). Accordingly, a micro-grid collapse scenario probably takes place as a result of low damping of power sharing dynamics and limited overload capacity of an inverter unit, in terms of current and time. Unlike conventional rotary generators, inverter-based generators provide a very limited overload capability.

#### 2.3.1.4 Inverter stability

An inverter-based DG unit is a multi-input-multi-output nonlinear system with coupled dynamics. A wide range of dynamics can be observed in a VSI system, starting from the low-frequency power generation and sharing dynamics in the range of few Hz to the high-frequency dynamics of the ac-side filter at the range of few kHz. With the uncertain nature of a distribution network, there is a possibility for dynamic interactions between the inverter and the network dynamics. Of significant effect, the grid impedance can shift the resonance frequency of the ac side filter of the DG inverter (Jian, 2011). The presence of grid harmonics gives chances to harmonic excitation. Additionally, uncertainty in the interfacing impedance , that is a function of the grid impedance, affects the stability of the current control (Liserre et al., 2006c).

### 2.3.2 Current control

The inverter in DG systems should have a high-quality output current to assure that no adverse effects are caused to other electric devices connected to the grid. The regular practice is to agree to a maximum THD of 5% at rated inverter output (Castilla et al., 2013). Accordingly, the performance of the DG converter system generally relies on the current control technique that is the main element in the control structure of an inverter-based DG system (Blaabjerg et al., 2006; Blaabjerg et al., 2004). The principle goals of the current

controller are to give a moderately high bandwidth to guarantee exact current tracking; shorten the transient response; and force the voltage source inverter to identically function as a current source inverter. In addition, the current loop is responsible for the injected-current quality and over-current protection. Grid voltage harmonics, unbalance, transients and grid parameters directly affect the current controller performance and might impair the power quality, and even the stability of the inverter system. Recently the effects of supply harmonics on the control effectiveness of inverter-based DG have begun to be investigated (Erika & Holmes, 2003; Liserre, Teodorescu, & Blaabjerg, 2006a; Liserre et al., 2006c). Examinations in (Erika & Holmes, 2003) demonstrate that little distortion in the utility grid voltage remarkably increases the total harmonic distortion in the injected current and finally, the inverter can be unstable due to a possible interaction between grid voltage distortion and the inverter filter circuit. Therefore, suppressing the grid voltage distortions is one of the main features that should be implemented in the current controller in aVSI-based DG systems. The main methods for current regulation in a current-controlled VSI include either a variable or fixed switching frequency schemes are hysteresis control, stationary and synchronous frame proportional-integral (PI) control, and deadbeat predictive current control (Holtz, 1994; Kazmierkowski & Malesani, 1998). Hysteresis based current control methods have fast transient response, however, they suffer from phase distortion and steady-state errors up to twice the hysteresis band. In addition, they bring about uncertain inverter switching frequency that depends on the load parameters and hence the output current harmonics are variable. Despite the fact that a few schemes are developed to oblige the variations in switching frequency (Bong-Hwan, Tae-Woo, & Jang-Hyoun, 1998; Ching-Tsai & Ting-Yu, 1994), the incompatibility with digital implementation and extra complexity make this technique far from being pragmatic.

Current regulator with a PI control in the stationary-frame has a long history of utilization. In this method, the VSI currents are transformed into stationary reference frame using the $abc \rightarrow \alpha\beta$ module. However, control variables are sinusoidal that result in steady-state phase errors and sensitivity to system parameters. Moreover, *dq* control in synchronous rotating frame result in DC control variables that have a satisfactory behavior applying PI regulator (Erika & Holmes, 2003; Teodorescu & Blaabjerg, 2004). The compensation capability of PI controllers against low-order harmonics of the grid voltage disturbances is very poor, therefore, they are not suitable for control of the grid-connected inverters under weak grid condition.

Recently, multiple PR compensators have been proposed to achieve unlimited loop gain at predefined harmonic frequencies (Fukuda & Imamura, 2005; Liserre et al., 2006a, 2006c). In (Liserre et al., 2006a) multiple PR compensators with PI compensator are adopted in the synchronous *d-q* frame. Furthermore, multiple PR compensators are presented in the stationary frame (Liserre et al., 2006c). With the schemes mentioned above, the steady-state error of the injected grid current is eliminated, and the low-order injected grid current harmonics are suppressed effectively. Multiple PR compensators are minimized the steady-state error and effectively suppressed the low-order harmonics of the injected grid current. However, PR controller is designed to eliminate a limited number of harmonic frequencies and the controller tuning process is complex for a large number of harmonic cancellations and may lead to instability (Fukuda & Imamura, 2005). In (Twining & Holmes, 2002) multiple PR control disadvantages are investigated for grid current regulation in the stationary frame. The same drawbacks are considered in (Liserre, Teodorescu, & Blaabjerg, 2006b), where PR controller is implemented to mitigate grid current low order harmonics in the synchronous frame. Another hindrance of utilizing the PR compensators is the interaction

with inverter output filter and utility grid impedance parameters variations. Mismatching instability is faced in stationary or the synchronous reference frame when a variation in the grid impedance or inverter filter parameters shifts the bandwidth of the PR current controller to be lower than the system resonant frequencies (Liserre et al., 2006c).

Space vector pulse width modulation (SVPWM) based deadbeat (DB) controller is widely implemented for ac current regulation in various applications (Xu et al., 2013). In addition, the tracking ability of a high bandwidth current controller makes it feasible to be applied to regulate the current in the natural and stationary reference frames. Moreover, when combined with SVPWM technique, this control scheme provides high-quality current waveform with low current ripples. DB current control technique has theoretically potential to realize the fast transient response, precise current control, minimized steady-state error, and fully compatible with digital-control platforms. However, conventional DB predictive controller is developed based on the inverter filter and grid model and it shows large sensitivity to model and parameter mismatch (Mohamed & El-Saadany, 2007). In addition, DB current control technique is relatively complex to implement and its high computation burden results in remarkable control delays. These drawbacks increase the complexity and sensitiveness of the DB control technique (Qingrong & Liuchen, 2008). Hence, the realization of a high bandwidth current regulation scheme, in the presence of inherent system delays and plant uncertainties, is a challenging task. In the presence of grid harmonics and unbalance, there is no a priori knowledge of plant dynamics; i.e. a complete plant model is not known in advance. Feedforward control is another alternative that tackles the power quality problems in DG systems at random and non-periodic grid circumstances. Feed-forward control is the process controller which predicts the disturbances in the process and take corrective action to avoid or minimize it. This reliable scheme may reject dynamic voltage disturbances in a wide range

of low-frequency harmonics and provides a fast response. The feedforward control scheme for the L-type grid-tie inverters has been well established and widely used (Qingrong & Liuchen, 2008; Timbus, Liserre, Teodorescu, Rodriguez, & Blaabjerg, 2009; Wang et al., 2010). In (Qingrong & Liuchen, 2008) a predictive current controller based on SVPWM modulation technique for three-phase grid-connected voltage source inverters has been presented. This current regulator feedforward phase voltages to compensate grid voltage harmonic disturbance in synchronous *d–q* frame. In (Wang et al., 2010) the grid phase voltage full-feedforward function for a single-phase grid-tie inverter with LCL filter is determined using the inverter averaged switch model (ASM) and the grid current is effectively regulated under distorted condition. In (Li et al., 2013) a full-feedforward scheme of the grid phase voltages for three-phase LCL-type grid-connected inverters is introduced. Beside the LCL filter resonance hazard, full-feedforwarding is considered sophisticated; due to the existence of proportional, derivative, and second derivative parts (Jinming, Shaojun, & Ting, 2014). Furthermore, the extensively wide variation of the inductance value in different current levels makes LCL filter design complicated (Wu, Chang, Lin, Chang, & Chang, 2013). It is noteworthy that scalar DPWM-based feedforward controllers for the grid-connected inverters are not established. However, a straightforward current control strategy that guarantees high power quality current injection under weak grid condition, interfacing parameters variation and inverter system delays demands special attention.

### 2.3.3 Voltage control

Recently, advanced control techniques for inverter-based DG systems are developed to enhance the efficiency of distribution system, power quality, and voltage regulation at the PCC (Jinwei, Yun Wei, Blaabjerg, & Xiongfei, 2014; Jinwei, Yun Wei, & Munir, 2012; Marei, El-Saadany, & Salama, 2004). In order to minimize the adverse effect of distribution

system distortions many active and passive filtering methods have been proposed. However, setting up the filtration system is not beneficial and imply an extra cost. Alternatively, distribution system power quality enhancement using flexible control of grid-connected DG units is becoming an interesting topic (Gajanayake, Vilathgamuwa, Poh Chiang, Teodorescu, & Blaabjerg, 2009; Jinwei et al., 2012; Tzung-Lin & Po-Tai, 2007), where the ancillary harmonic compensation capability is integrated with the DG primary power generation function through modifying control references. This idea is especially attractive considering that the available power from backstage renewable energy resources is often lower than the power rating of DG interfacing converters. Moreover, the DG inverters are desired to operate with voltage control mode particularly considering the possible autonomous islanding operation in micro grid systems that it can provide direct voltage and frequency support for the loads (Vasquez, Guerrero, Luna, Rodriguez, & Teodorescu, 2009; Yun Wei & Ching-Nan, 2009). In general, this power devices control consist of two loops; the voltage regulator is developed based on the reactive reference current to control the load bus voltage, and the output current is regulated using an internal current control loop. Numerous control strategies have been proposed for the voltage control loop. PI regulators have been mostly employed to produce the reactive current component. Nevertheless, these types of linear controllers work against nonlinear error dynamics. Furthermore, there is difficulty in creating these kinds of controllers to manage the main harmonic voltage as well as to cancel high-frequency harmonic distortions. Because of zero frequency pole, PI controllers are not able to obtain quickly voltage regulation as well as are not able to reduce quickly voltage disturbances. In (Marei et al., 2004) a fuzzy-logic-based voltage controller is developed to control the DG system considering nonlinearity in the voltage control loop. To guarantee ideal regulation of the voltage at the PCC and offer an effective method for eliminating voltage disturbances, closed loop system should be contained the frequency spectrum of the disturbances to be

rejected. Consequently, the particular following error will not include these frequency modes. This specific requirements is fulfilled when the voltage controller can provide an internal model. Not a linear controller or a nonlinear controller may eliminate broad band of voltage disturbances except if an internal model for the voltage disturbances is presented (Morari & Zafiriou, 1989). For voltage regulation in case of periodic disturbances, the repetitive control method can be applied (Weiss, Qing-Chang, Green, & Jun, 2004). Nevertheless, only a few voltage disturbances are periodic by nature. On the other hand, the repetitive control is not easy to stabilize and cannot attain very fast response for all unknown disturbances. Furthermore, a fast current control loop with high-bandwidth is important permitting exact tracking of the highly dynamic reference trajectory generated by the voltage controller.

## 2.4 Summary

In this chapter, a literature survey with the focus on inverter-based DG system topology and control has been presented. In addition, the important specification of grid requirements in order to integration of renewable energy sources are introduced that may be having a major effect on the design and structure of the grid-tie inverters.

# CHAPTER 3: IZDPWM METHOD FOR TWO-LEVEL VOLTAGE SOURCE INVERTER

## 3.1 Introduction

DPWM methods improve the inverter efficiency at the expense of signal quality specifically at lower modulation indices (Hava, Kerkman, & Lipo, 1999; Yunxiang, Shafi, Knight, & McMahon, 2011). However with some modification on DPWM scheme; implicit zero-sequence discontinuous pulse width modulation (IZDPWM) method provides good output profile for three-phase three-wire two-level voltage source inverters is introduced (Shayestehfard, Mekhilef, & Mokhlis, 2015). IZDPWM may take place in any application where DPWM may exist. In DPWM strategy, phase values are necessary to determine appropriate zero-sequence. The zero-sequence signal is injected to the original references in order to attain the earlier mentioned merits. In contrast; the proposed IZDPWM directly uses line-to-line values and no zero-sequence is considered. Therefore, the proposed modulator is said to be implicited zero-sequence. This chapter briefly reviews carrier-based scalar PWM technique, advanced scalar PWM methods and investigates the prominent role of zero-sequence signal injection in improving the performance of VSIs. Then, IZDPWM method is presented and discussed in terms of operating principles and performance. Lastly, the simulation results are provided and discussed in detail to validate the proposed modulation scheme.

## 3.2 Scalar PWM method

Carrier-based scalar PWM techniques are getting involved in many VSI applications due to its simplicity comparing to other modulation methods such as selective harmonic elimination and space vector PWM (SVPWM) (Belkamel, Mekhilef, Masaoud, & Naeim,

2013; Hava & Cetin, 2011; Tan, Li, Wang, Cao, & Han, 2013). Figure 3-1 shows power circuit of two level VSI topology.

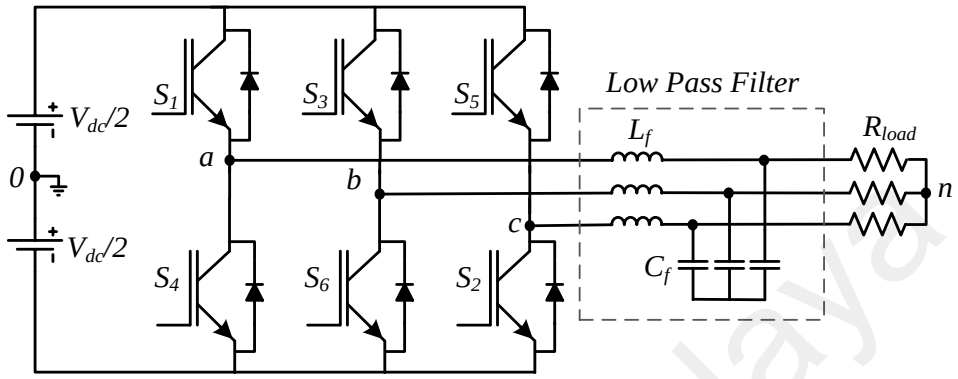



Figure 3-1: Schematic of VSI.

The main purpose of these topologies is to provide a three-phase voltage source, follow a given waveform on a continuous basis by properly driving power switches. Although most of the applications require sinusoidal voltage waveforms, arbitrary voltages are also required in some emerging applications such as active filters and voltage compensators. The carrier-based PWM technique is the most common method to achieve this outcome. The essential concept is that a low-frequency reference waveform (modulating signal) is compared against a high-frequency triangular waveform (carrier signal) and the comparator output is used to control the state of a switched phase leg. If the reference waveform is greater than the carrier waveform, the phase leg is switched to positive dc link. If the reference waveform is less than the carrier waveform, the phase leg is switched to negative dc link. The outcome is a stream of pulses switching between the upper and lower dc rails which have the target reference waveform as a fundamental component, but also incorporate a series of unwanted harmonics that centered around carrier frequency and its multiples. In sinusoidal PWM (SPWM) three $2\pi/3$ out-of-phase modulating signals are used as expressed in equations (3- 1) to (3- 3). Where $V_{1m-ph}$ is the peak value of fundamental component of the phase voltage.

$$v_{ma} = V_{1m-ph}\sin(\omega_e t) \quad (3\text{-}1)$$

$$v_{mb} = V_{1m-ph}\sin(\omega_e t - 2\pi/3) \quad (3\text{-}2)$$

$$v_{mc} = V_{1m-ph}\sin(\omega_e t + 2\pi/3) \quad (3\text{-}3)$$

The eight valid switch states are given in Table 3-1. The switches of any leg of the inverter cannot be switched ON simultaneously because this would result in a short circuit across the dc-link voltage supply. In order to avoid undefined states in the VSI, and thus undefined ac output line voltages, the switches of any leg of the inverter cannot be switched OFF simultaneously as this will result in voltages that will depend on the respective line current polarity. Of the eight valid states, two of them (7 and 8) produce zero ac line voltages. In this case, the line currents freewheel through either the upper or lower components. The remaining states produce non-zero ac output voltages.

Table 3-1: Switches states and output voltages of VSI

| States | Switch State | | | | | | $v_{ab}$ | $v_{bc}$ | $v_{ca}$ |
|---|---|---|---|---|---|---|---|---|---|
| | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | | | |
| 1 | ON | ON | OFF | OFF | OFF | ON | $V_{dc}$ | 0 | $-V_{dc}$ |
| 2 | ON | ON | ON | OFF | OFF | OFF | $-V_{dc}$ | $V_{dc}$ | $-V_{dc}$ |
| 3 | OFF | ON | ON | ON | OFF | OFF | $-V_{dc}$ | $V_{dc}$ | 0 |
| 4 | OFF | OFF | ON | ON | ON | OFF | $-V_{dc}$ | 0 | $V_{dc}$ |
| 5 | OFF | OFF | OFF | ON | ON | ON | 0 | $-V_{dc}$ | $V_{dc}$ |
| 6 | ON | OFF | OFF | OFF | ON | ON | $V_{dc}$ | $-V_{dc}$ | 0 |
| 7 | ON | OFF | ON | OFF | ON | OFF | 0 | 0 | 0 |
| 8 | OFF | ON | OFF | ON | OFF | ON | 0 | 0 | 0 |

In order to generate a given voltage waveform, the inverter moves from one state to another. Thus, the resulting output line voltages consist of discrete values of voltages that are $V_{dc}$, 0, and $-V_{dc}$. The two switching devices in each and every inverter leg change the states in complimentary manner. Equations (3- 4) to (3- 5) calculate the duty cycle of the switching devices. Accordingly, the appropriate gate signals are generated based on the references waveforms $v_{ma}$ , $v_{mb}$, and $v_{mc}$.

$$d_{S_x} = \frac{1}{2}\left(1 + \frac{v_{my}}{V_{dc}/_2}\right), \text{ for } (x, y) \in \{(1, a), (3, b), (5, c)\} \quad (3\text{- }4)$$

$$d_{S_z} = 1 - d_{s_x}, \qquad \text{for } (z, x) \in \{(2, 5), (4, 1), (6, 3)\} \quad (3\text{- }5)$$

Figure 3-2 shows VSI waveforms generated using SPWM modulator. It is noteworthy that the scalar PWM techniques introduced in the literature take the dc-link midpoint (*0*) into consideration in order to derive the switching signals. This midpoint is referred as modulator ground (MG) that has no effects on three-wire inverter power circuit. At $v_{ma}$=0 the calculated duty cycles for the switches $S_1$ and $S_4$ based on equations (3- 4) to (3- 5) are $d_{S_1} = d_{S_4} = 1/2$. Consequently terminal "a" is clamped to the positive ( $v_{ao} = V_{dc}/2$) and negative ( $v_{ao} = -V_{dc}/2$) dc-links for equal periods of $T_{sw}/2$. Where $T_{sw}$ is the period of triangular carrier signal. Therefore, an average value of zero volt ( $v_{ao}$ =0) is seen in the output of the inverter.

In order to use a single carrier signal to maintain synchronization and eliminate all even harmonics and triplen harmonics, frequency modulation index $f_c/f_e$ should be an odd integer multiple of three where $f_c$ *and* $f_e$ are carrier and modulating reference signals frequency, respectively. Thus, all inverter side phase voltages ( $v_{ao}$ , $v_{bo}$ , and $v_{co}$ ) are identical, but $120^\circ$ out-of-phase without even harmonics; moreover, triplen harmonics are identical in amplitude and phase in all phases. Thus, the output line-to-line voltage also will not contain triplen harmonics. The amplitude of the inverter output voltages is controlled by the modulation index $M_i$. The basic definition of $M_i$ is given in equation (3- 6), where $V_{1m-ph}$ and $V_{dc}/2$ are the peak values of the reference and triangular carrier signals, respectively.

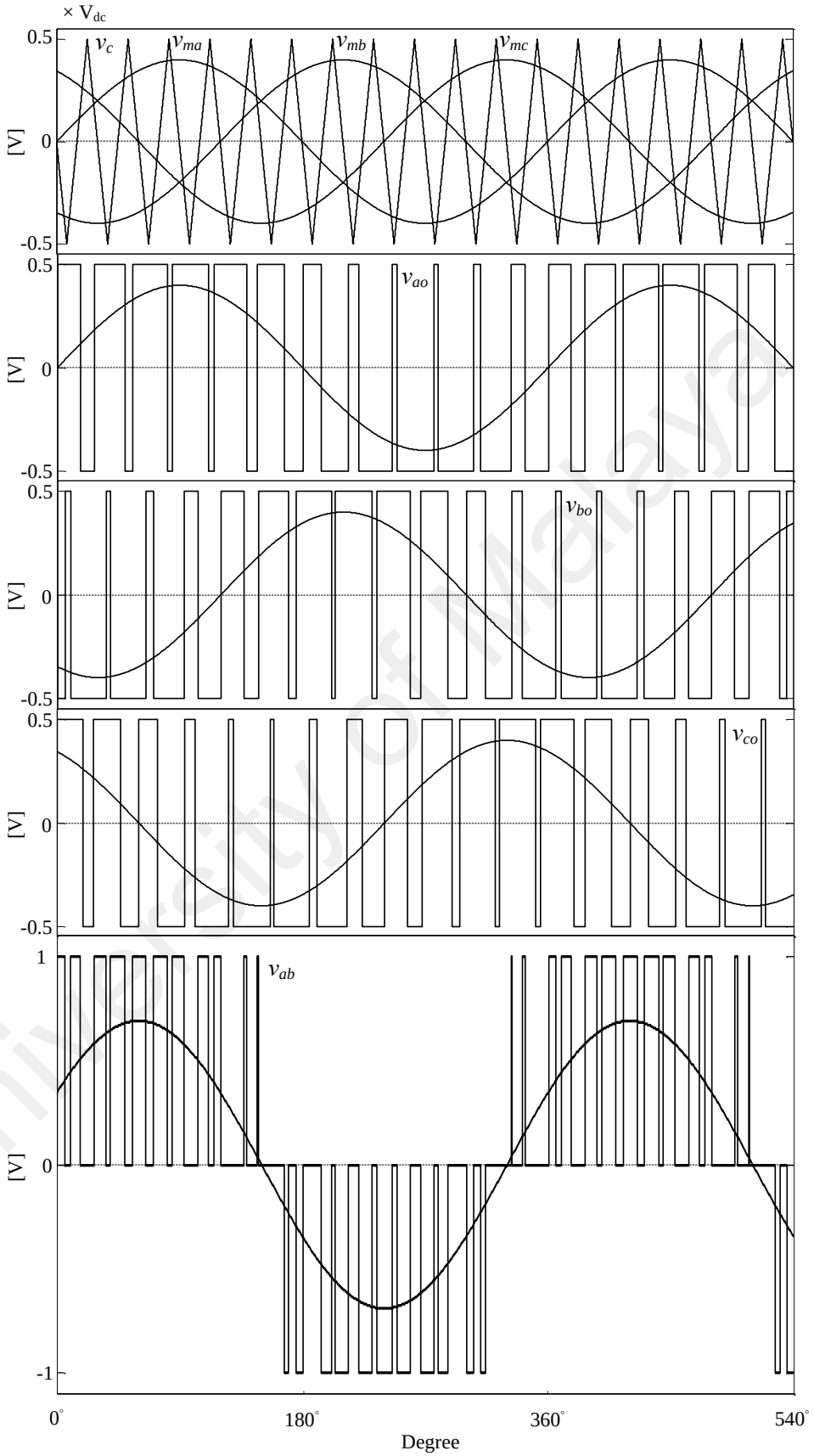



Figure 3-2: VSI waveforms generated using SPWM modulator.

$$M_i = \frac{V_{1m-ph}}{V_{dc}/2} \tag{3- 6}$$

For $0 \leq M_i \leq 1$, which is called the linear region of the modulating technique, the maximum amplitude of the fundamental phase voltage in the linear region is $V_{dc}/2$. In overmodulation region ($M_i > 1$) some intersections between the carrier and the modulating signal are missed, which leads to the generation of low-order harmonics but a higher fundamental ac output voltage is obtained. Unfortunately, the linearity between $M_i$ and $V_{1m-ph}$ achieved in the linear region does not hold in the overmodulation region and a saturation effect can be observed.

### 3.3 Advanced scalar PWM methods

For the purpose of improving the performance of SPWM scheme, advanced scalar PWM methods are employed based on zero-sequence injection principle (Hava & Cetin, 2011). The block diagram of an advanced scalar PWM approach is shown in Figure 3-3. Advanced scalar PWM modulators are two types; continuous and discontinuous. With continuous PWM, modulating signals do not go beyond the carrier signals, and as a result, modulating and carrier waves overlap in every carrier cycle. In DPWM methods, inverter terminals (a, b, c) are clamped to positive or negative dc-links for specific durations within the fundamental period. These discontinuous switching patterns considerably minimize switching losses and significantly improve the efficiency of the inverter (Hava, Kerkman, & Lipo, 1998; Kolar, Ertl, & Zach, 1991; The Dung, Hobraiche, Patin, Friedrich, & Vilain, 2011). Therefore, DPWM strategies are implemented in a variety of applications such as ac-drives (Un & Hava, 2009), active filters (Asiminoaei, Rodriguez, & Blaabjerg, 2008), matrix converters (Bradaschia, Cavalcanti, Neves, & de Souza, 2009), and high-power converters (Beig, Kanukollu, Al Hosani, & Dekka, 2014).

In advanced scalar PWM methods, the zero-sequence signal $v_0$ is injected into the sinusoidal reference signals $v_a$ , $v_b$, and $v_c$ (Hava & Cetin, 2011). The derived non-sinusoidal modulating signals $v_{ma}$, $v_{mb}$, and $v_{mc}$ are compared with the carrier signals to generate the appropriate switching signals. $v_{ma}$, $v_{mb}$, and $v_{mc}$ are expressed in equations (3- 7) to (3- 9).

$$v_{ma} = v_a + v_0 = V_{1m-ph}\sin(\omega_e t) + v_0 \quad (3\text{- }7)$$

$$v_{mb} = v_b + v_0 = V_{1m-ph}\sin(\omega_e t - 2\pi/3) + v_0 \quad (3\text{- }8)$$

$$v_{mc} = v_c + v_0 = V_{1m-ph}\sin(\omega_e t + 2\pi/3) + v_0 \quad (3\text{- }9)$$

In particular applications multicarrier waves ($v_{c1}$, $v_{c2}$, $v_{c3}$) are employed instead of the common triangular carrier (Kimball & Zawodniok, 2011; Un & Hava, 2009). Despite the non-sinusoidal modulating signals, only in the three-wire inverter, outputs are sinusoidal waveforms. The three-wire configuration depicted in Figure 3-4(a) helps to neutralize the injected zero-sequence signals. Therefore, no undesired zero-sequence current is conducted.

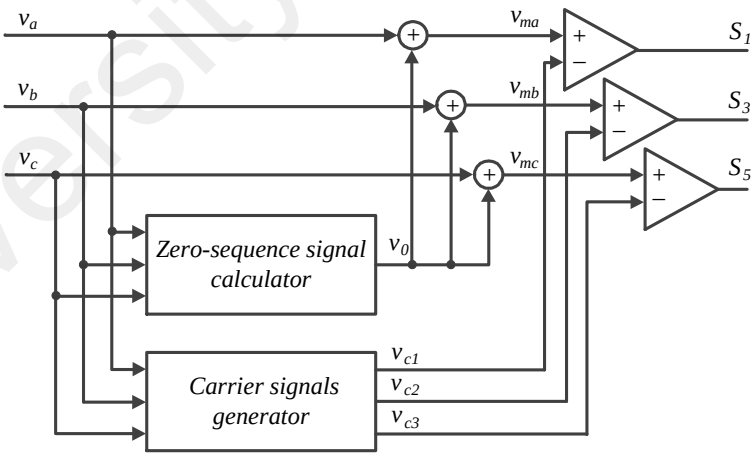



Figure 3-3: Block diagram of an advanced scalar PWM.

However, for four-wire load in Figure 3-4(b), the injection of zero-sequence signal creates a distorted phase voltages at the load side ($v_{an}$, $v_{bn}$, $v_{cn}$) and a specific current may flow through the fourth wire of the load. Hence, advanced scalar PWM methods are not applicable

to the four-wire inverters. Zero-sequence signals are selected and implemented in the way that enhances the performance of VSI in terms of output voltage control linearity range, switching loss, high-frequency common mode voltage (CMV), and the waveform quality (Kimball & Zawodniok, 2011).

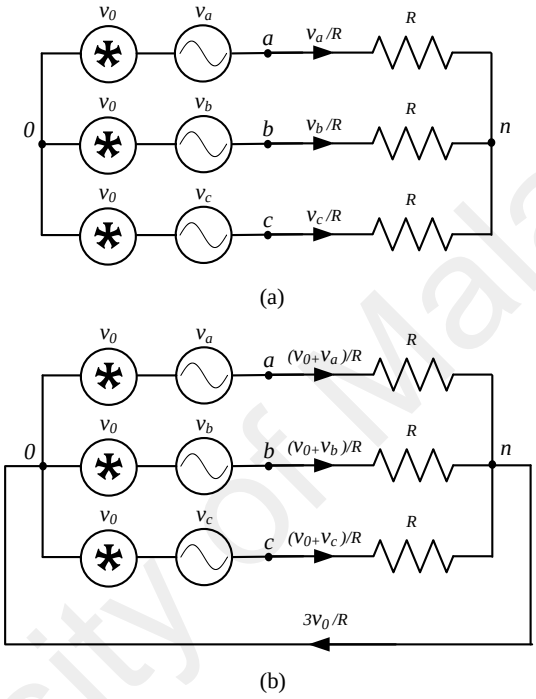



Figure 3-4: Zero-sequence current in (a) three-wire load and (b) four-wire load.

### 3.3.1 Increasing inverter output linearity range

It is well known that conventional SPWM shows nonlinear performance at $M_i$>1, since the magnitude of the modulating signal $|v_{ma}|$ is maintained higher than the magnitude of the carrier signal ($|v_{ma}|> V_{dc}/2$). To avoid the occurrence of over-modulation and make the modulating signals not to exceed the peak values of the carrier signals ($|v_{ma}|<V_{dc}/2$), a suitable zero-sequence signal need to be injected to the reference signals. The modified reference signals ensure the linear performance of the modulator at $1 < M_i$<1.15. In SPWM and based on equation (3- 6) at unity modulation index, the peak values of the phase and the

line-to-line voltages attained are $\mathrm{Vdc}/2$ and $\sqrt{3} * V_{dc}/2 \ = 0.87 * V_{dc}$ , respectively. In other words a sharp decline of 15.5% is observed in the inverter output voltage with regards to the maximum theoretical feasible limit $V_{dc}$ . However in some applications like motor drive output voltage of the inverter is a matter of concern. For $M_i$<1 where the magnitude of the modulating signal $|v_{ma}|$ is maintained lower than the magnitude of the carrier signal ($|v_{ma}|< \mathrm{Vdc}/2$) linear characteristics are observed in the inverter output phase voltages. The highlighted segments of the reference signals in Figure 3-5 represents the nonlinear regions (over modulation regions) where $M_i = \frac{1}{\sin 60^\circ} = 1.15$ . These arcuate segments form a periodic trajectory that repeat itself every 120°. And appears along the whole cycle of the fundamental component (6×60°=360°). In these un-switching intervals the switches remain in a single state continuously ON or OFF. Consequently, nonlinear performance is experienced with some undesired low order harmonic components at the output of the inverter. To avoid the occurrence of over-modulation and make the modulating signals not to exceed the peak values of the carrier signals ($|v_{ma}|<\mathrm{Vdc}/2$), a suitable zero-sequence signal need to be injected to the reference signals. The aforementioned periodic trajectory necessitates zero-sequence signal with similar period and opposite polarity. Hence, the third harmonic component is inherently included in all the zero-sequence signals. The modified reference signals ensure the linear performance of the modulator. Despite the injection of zero-sequence signals in three-wire topologies, the load side of the inverter gives sinusoidal like waveforms with enhanced magnitude. However, source side output phase voltages exactly copy the modified modulating signal in terms of shape and magnitude. For $M_i$>1.15, each and every segment highlighted in Figure 3-5 gets enlarged and exceeds 60°. And an over modulation phenomenon is experienced with more than a single phase simultaneously. In this case the injection of a common zero-sequence signal does not help to overcome the

over modulation problem. Accordingly the maximum expanded linearity range is restricted to $M_i \leq 1.15$. The third harmonic injection PWM (THIPWM) and the space vector PWM (SVPWM) are continuous scalar PWM methods that contribute all the ways in extending the output voltage linearity range. As shown in Figure 3-6 the zero-sequence of THIPWM is $v_0 = 1/6 \sin(3\omega_e t)$ (Houldsworth & Grant, 1984). And the minimum magnitude test is used to define the zero-sequence signals of SVPWM (Hava et al., 1999; van der Broeck, Skudelny, & Stanke, 1988).

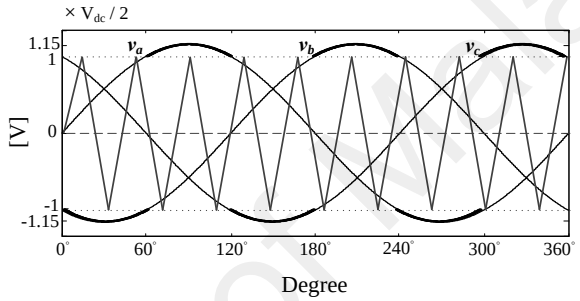



Figure 3-5: SPWM over modulation regions at $M_i$=1.15.

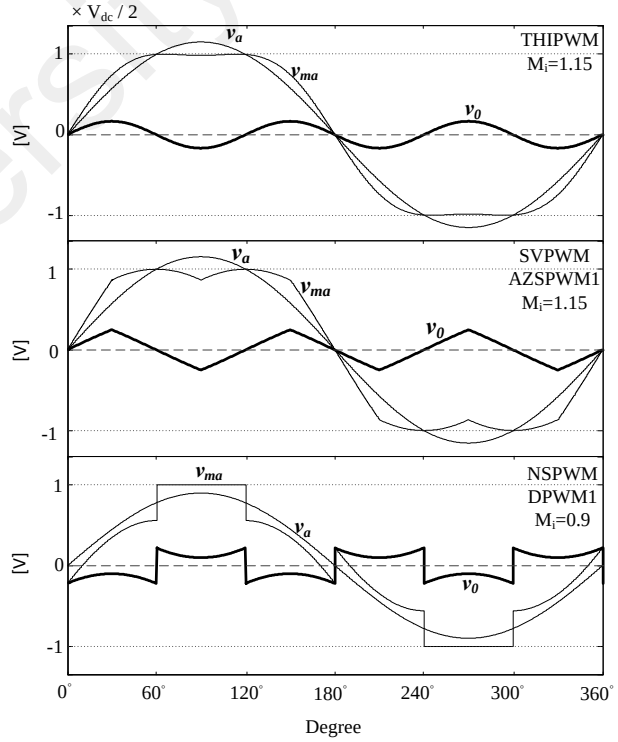



Figure 3-6: Zero-sequence signals and modulating waveforms for advanced scalar PWM methods.

### 3.3.2 Decreasing switching losses

Besides increasing the inverter output linearity range, the injection of zero-sequence signals in DPWM methods significantly improve the efficiency of VSI. The un-switching intervals introduced using DPWM techniques clamp one of the three inverter legs. That implies no switching for the corresponding clamped switching devices. As a result, switching losses are substantially reduced (Bradaschia et al., 2009; Hava et al., 1998; Yunxiang et al., 2011). Different DPWM strategies have been introduced in the literature with different clamping position within a fundamental period (Hava et al., 1998). For $2\pi/3$ of the fundamental period, DPWMMAX and DPWMMIN clamp each of the three legs of the inverter to positive and negative dc-link respectively. The unequal power losses among the switching devices of each inverter leg categorize the two methods under asymmetrical DPWM modulators. In order to ensure equal distribution of power losses among the switching devices, DPWM0, DPWM1, DPWM2, and DPWM3, clamp each leg to the positive and the negative dc-link for $\pi/3$. The zero-sequence signals of DPWM1 in Figure 3-6 are obtained by employing the maximum magnitude test. DPWM1 centers the non-switching periods for each phase leg symmetrically around the positive and negative peaks of its reference voltage. Such position is considered the most appropriate for resistive load due to the in phase condition of current and voltage. Moreover this method does not switch the inverter at maximum current resulting in minimum switching losses. In general, a leg's non-switching period can be feasibly placed where the corresponding reference signal is maximum or minimum among the three-phase set. Moreover, to effectively decrease power losses, the clamped regions of the modulating signals need to be selected according to load power factor. Therefore, the clamped regions are placed in such a way that the switch remains on in the vicinity of the load current peaks (Asiminoaei et al., 2008). Similar principles were

adopted in GDPWM introduced by (Hava et al., 1998; The Dung et al., 2011) and power losses were effectively reduced.

### 3.3.3 High-frequency common mode voltage reduction

The common mode voltage $v_{cm}$ of the three-phase three-wire wye-connected load defined in equation (3- 10) leads to undesired leakage current (Kimball & Zawodniok, 2011). The mitigation of CMV is getting more attention especially in motor drive and transformer-less photovoltaic applications (Un & Hava, 2009).

$$v_{cm} = v_{no} = \frac{v_{ao} + v_{bo} + v_{co}}{3} \tag{3- 10}$$

Scalar PWM methods employing common carrier wave synthesize discontinuous output phase voltages $v_{ao}$ , $v_{bo}$ , $v_{co}$ from the dc-links voltages $\pm V_{dc}/2$. Such inverter outputs make CMV always existing with non-zero magnitude. Clamping the three-phases simultaneously to the same dc-link makes magnitude of the common mode voltage $|v_{cm}| = V_{dc}/2$. However $v_{cm} = \pm V_{dc}/6$ is generated based on the other switching states (Un & Hava, 2009). In scalar PWM strategies, based on volt-second average principle the width of the active pulses are identified within the carrier cycle. The active pules may take different locations within the carrier cycle according the carrier waveform. Therefore the volt-second average is maintained all time for different position of the active pules. Recently PWM methods are developed based on interleaved multi carrier signals in order to limit common mode voltage $v_{cm}$ to $\pm V_{dc}/6$. Active Zero State PWM (AZSPWM1) and Near State PWM (NSPWM) (Un & Hava, 2009; Yen-Shin & Fu-San, 2004) are employed in order to reduce high frequency common mode voltage (see Figure 3-6).

### 3.3.4 Increasing waveform quality

Waveform quality of the VSI outputs that employed advanced scalar PWM modulators depend on many factors, such as switching frequency $f_s$, modulation index $M_i$, injected zero-sequence signal, carrier signal, and characteristics of the utilized filter (Hava et al., 1999; Holtz, 1994). The earlier mentioned THIPWM and SVPWM offer lower THD in comparison to the conventional SPWM (Blasko, 1997; Houldsworth & Grant, 1984; Keliang & Danwei, 2002; van der Broeck et al., 1988).

## 3.4 Principle and realization of the IZDPWM

The proposed IZDPWM uses line-to-line voltages ($v_{ab}$ , $v_{bc}$ , and $v_{ca}$) defined in equations (3- 11) to (3- 13) as reference signals.

$$v_{ab} = V_{1m-ll} \sin(\omega_e t) \quad (3\text{- }11)$$

$$v_{bc} = V_{1m-ll} \sin(\omega_e t - 2\pi/3) \quad (3\text{- }12)$$

$$v_{ca} = V_{1m-ll} \sin(\omega_e t + 2\pi/3) \quad (3\text{- }13)$$

Where $V_{1m-ll}$ is the peak value of the line-to-line voltage. The block diagram of the IZDPWM is depicted in Figure 3-7 . Similar to conventional scalar PWM methods, the proposed IZDPWM employs per-carrier cycle volt-second balance principle. In other words, IZDPWM adopts the statement in equation (3- 14), which is valid under balanced, unbalanced, and distorted conditions.

$$v_{ab} + v_{bc} + v_{ca} = 0 \quad (3\text{- }14)$$

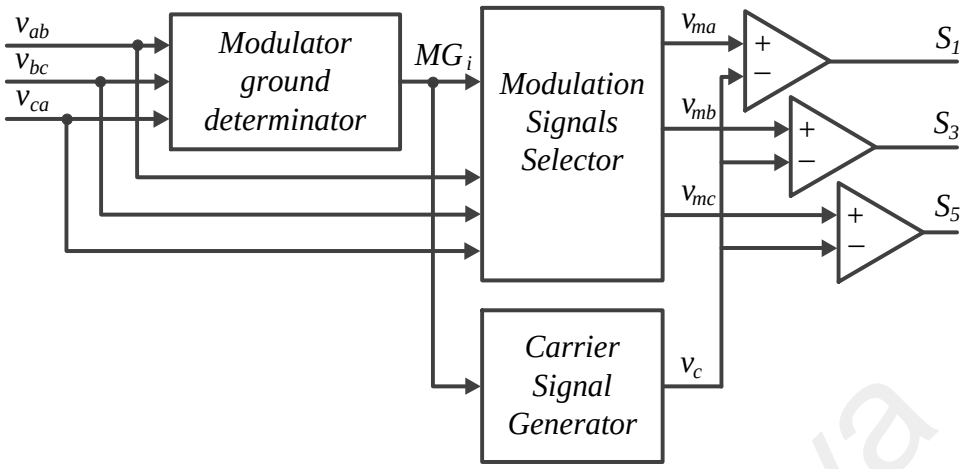



Figure 3-7: Block diagram of the IZDPWM.

According to equation (3- 14), defining two line-to-line voltages of the inverter output is sufficient to attain the third one. Assuming leg "b" is clamped to negative dc-link and considered as MG, two PWM generators are required to control leg "a" and leg "c" to create the desired line-to-line voltages $v_{ab}$ and $v_{cb}$ $(-v_{bc})$ respectively. Consequently the third voltage $v_{ca}$ readily provided based on equation (3- 14). DPWM methods that use the dc-link midpoint as MG, create two voltage levels $\pm V_{dc}/2$ in the inverter output. Taking the zero crossing areas into consideration, when $\nu_{ma}$=0 for instance, the duty cycle of the gate signals of $S_1$ and $S_4$ is $1/2$. Consequently, terminal "a" is clamped to the positive ($\nu_{a0}=V_{dc}/2$) and negative ($\nu_{a0}=-V_{dc}/2$) dc-links for equal periods of $T_{sw}/2$. Therefore, an average value of zero volt ($\nu_{an}=\nu_{a0}=0$) is seen in the output of the inverter. Considering the mentioned midpoint (*0*) in Figure 3-1, the value $V_{dc}/2$ with positive and negative polarity is achieved in the output of the inverter. Therefore, in DPWM methods the carrier and modulating signals are selected in a bipolar manner. However, the proposed modulation scheme uses the positive and negative dc-links alternately as MG whereas the modulating and carrier signals are determined in different ways.

### 3.4.1 Modulator grounds

The proposed IZDPWM may use the dc-links as MG. The positive and negative dc-links of the power circuit in Figure 3-1 are accessed in six different ways through six semiconductor switches $S_1$ to $S_6$. Therefore, the modulation technique considers six modulator grounds $MG_1$ to $MG_6$. For each clamping condition, the MG determinator in Figure 3-7, determines the corresponding modulating ground MG. The selected MG is adopted for a specific duration within the fundamental cycle. IZDPWM is a modified DPWM method that uses line-to-line voltages instead of phase voltages as references signals. Since the six modulator grounds might be flexibly used, different methods are derived based on the proposed IZDPWM. To validate the new technique, IZDPWM0, IZDPWM1, IZDPWM2, and IZDPWM3 are derived and designed to have similar non-switching intervals as DPWM0, DPWM1, DPWM2, and DPWM3, respectively. According to Figure 3-8 to Figure 3-11, the proposed methods are only different in clamping intervals and are shifted by 30°. In the balanced three-phase system, $\pi/6$ phase-shift between the phase voltages and the line-to-line voltages has to be considered in order to have similar clamping intervals. For instance, in IZDPWM0 the MG and the clamped area are defined based on the maximum absolute magnitude of the three line voltages. For $|v_{ab}|\geq|v_{bc}|$ and $|v_{ab}|\geq|v_{ca}|$, the terminal "a" is clamped to one of the dc-links. If $v_{ab}>0$, terminal "a" is clamped to the positive dc-link through $S_1$, which is referred to as $MG_1$. For $v_{ab}<0$, leg "a" is clamped to the negative dc-link. $MG_4$ refers to the state in which point "a" is clamped to the negative dc-link through $S_4$. As depicted in Figure 3-8, each $MG_i$ is maintained for $\pi/3$ of fundamental component. Accordingly, either $MG_3$ or $MG_6$ clamp leg "b" based on $v_{bc}$. However, $MG_5$ and $MG_2$ clamp leg "c" based on $v_{ca}$.

### 3.4.2 Modulating signals

IZDPWM is implemented based on six different modulator grounds $MG_1$ to $MG_6$. Table 3-2 defines the modulating signals $\nu_{ma}$ , $\nu_{mb}$, and $\nu_{mc}$ for each and every MG. The modulating signals are determined based on the line voltages $\pm\nu_{ab}$ , $\pm\nu_{bc}$, and $\pm\nu_{ca}$. As depicted in Figure 3-8, clamping one of inverter terminals to the positive dc-link requires the other two modulating signals to be of negative amplitudes and vice versa. The aforementioned principle has to be maintained to successfully execute the proposed method. For the sake of clarification, terminal "b" is considered. Clamping terminal "b" to negative dc-link $v_{mb}$=$-V_{dc}$brings $MG_6$ to use. With a specific switching pattern, terminals "a" and "c" may access any of the dc-links. In this case the line-to-line instant voltages, $v_{ab}$ and $v_{cb}$ may take any of the two values 0V and+$V_{dc}$. Accordingly, the modulating signals $v_{ma}$ and $v_{mc}$ are positive, whereas $v_{mb}$ is negative ($-V_{dc}$). However, $MG_3$ ($v_{mb}$= $V_{dc}$) ensures that $v_{ma}$ and $v_{mc}$ remain negative throughout its duration.

Table 3-2: Modulating signals of IZDPWM

| $MG_i$ | $MG_1$ ($S_1$:ON) | $MG_2$ ($S_2$:ON) | $MG_3$ ($S_3$:ON) | $MG_4$ ($S_4$:ON) | $MG_5$ ($S_5$:ON) | $MG_6$ ($S_6$:ON) |
|---|---|---|---|---|---|---|
| $v_{ma}$ | $V_{dc}$ | $-v_{ca}$ | $v_{ab}$ | $-V_{dc}$ | $-v_{ca}$ | $v_{ab}$ |
| $v_{mb}$ | $-v_{ab}$ | $v_{bc}$ | $V_{dc}$ | $-v_{ab}$ | $v_{bc}$ | $-V_{dc}$ |
| $v_{mc}$ | $v_{ca}$ | $-V_{dc}$ | $-v_{bc}$ | $v_{ca}$ | $V_{dc}$ | $-v_{bc}$ |

### 3.4.3 Carrier signals

In order to maintain the intersection among the carrier and the modulating signals as illustrated in Figure 3-8, the proposed IZDPWM avoids bipolar triangular carrier waves. Positive carrier signals are used for $MG_2$, $MG_4$, and $MG_6$. However, $MG_1$, $MG_3$, and $MG_5$

employ negative carrier signals. The carrier signal does not take positive and negative values within the same MG. In Figure 3-8, during $MG_6$ in IZDPWM0, $v_{mb}$ is clamped to the negative dc-link while $v_{ma}$ and $v_{mc}$ are unclamped with a positive amplitude. Around the zero crossing of modulating signal $v_{ma}$ ($v_{ab=0}$), the comparator outputs a square wave with a duty cycle of 100% low and 0% high. Consequently, the line "a" is clamped to negative dc-links for $T_{sw}$. Such condition results in desired average value of $v_{ab} = 0$. On the other hand, the carrier signal given in Figure 3-8 holds the switch $S_4$ on for the entire $T_{sw}$. Hence, the average value of $v_{ab} = 0$ per design is obtained.

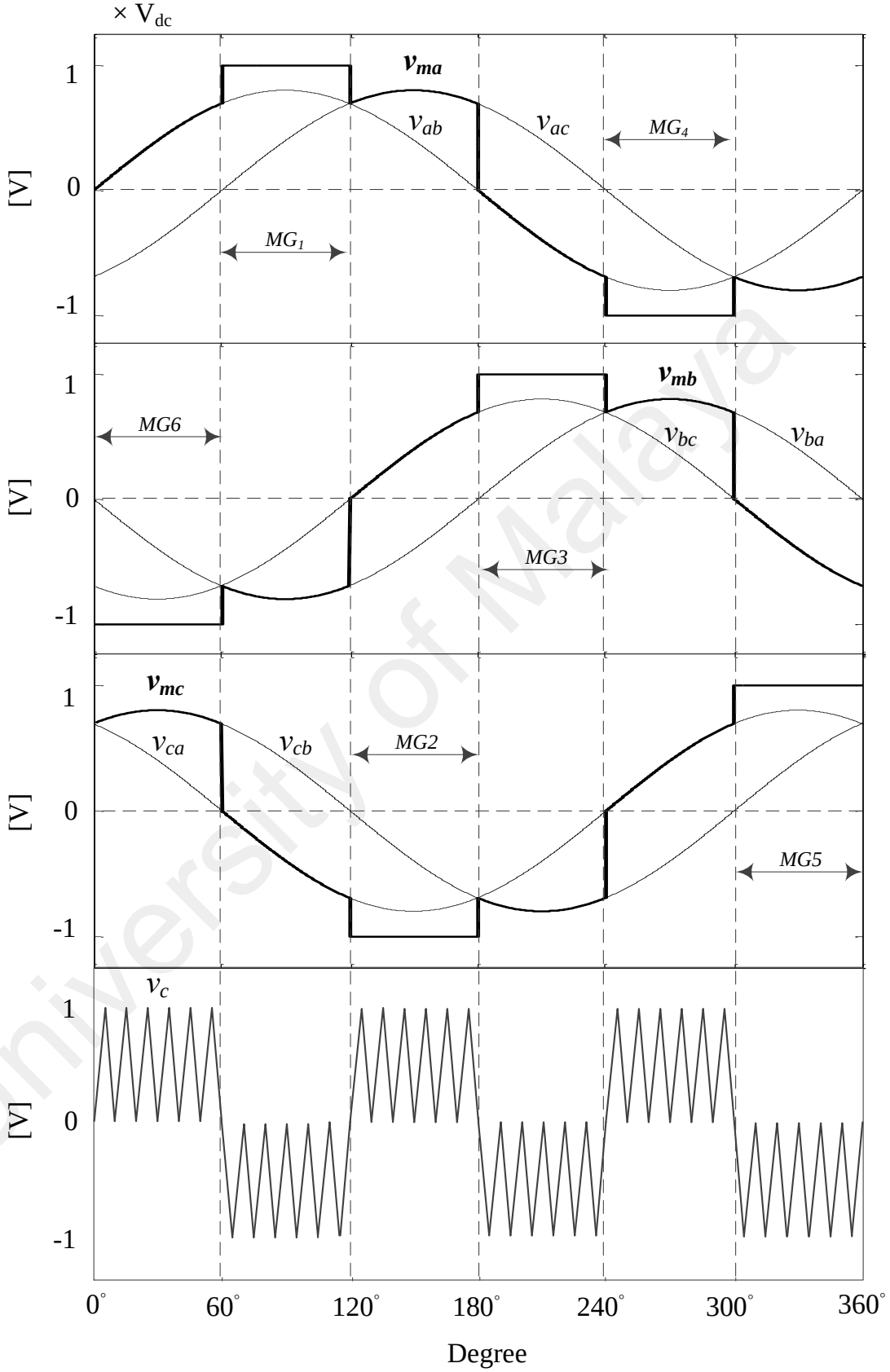



Figure 3-8: Modulating and carrier signals of IZDPWM0 at $M_i = 0.8$ .

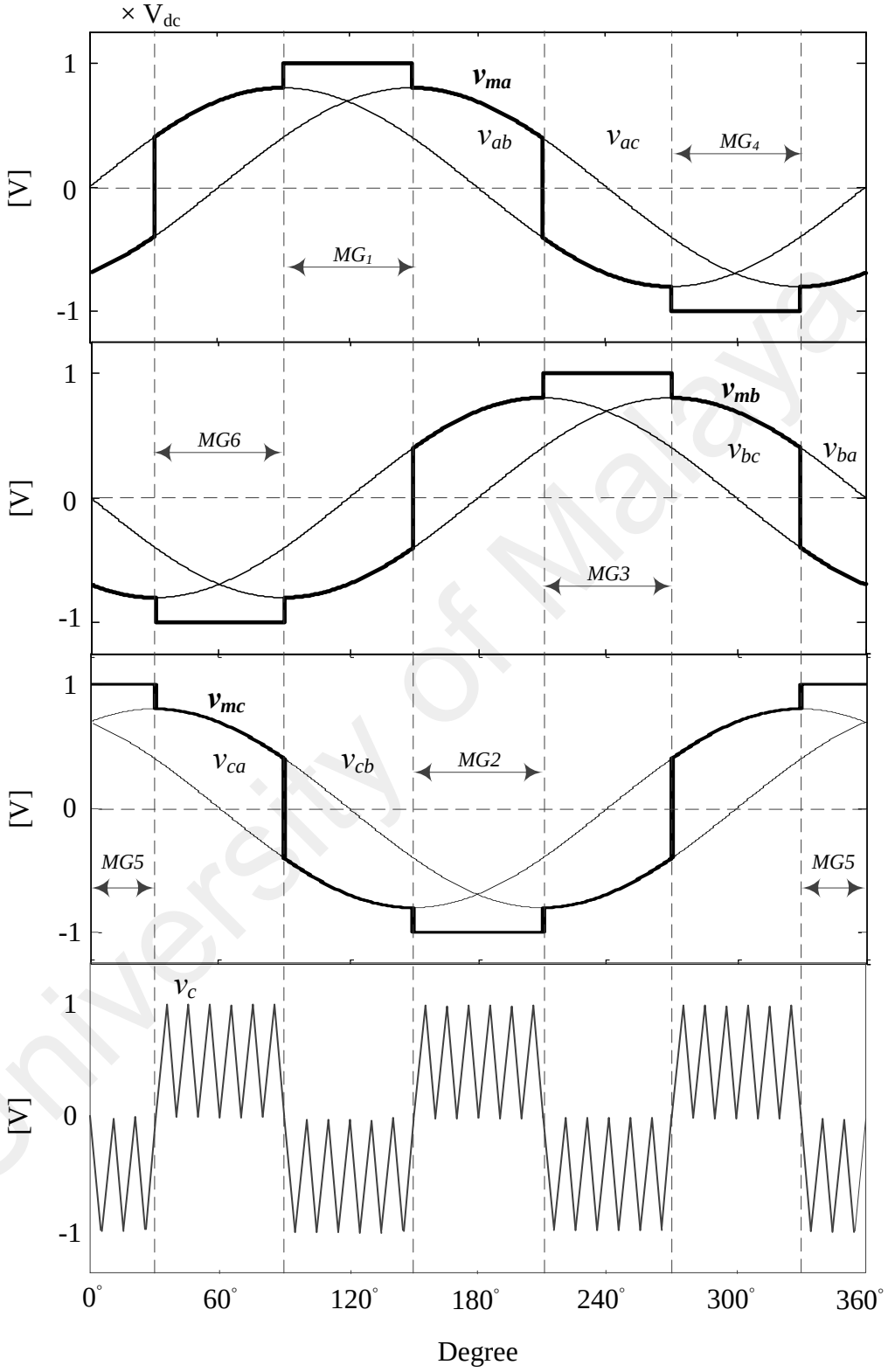



Figure 3-9: Modulating and carrier signals of IZDPWM1 at $M_i = 0.8$ .

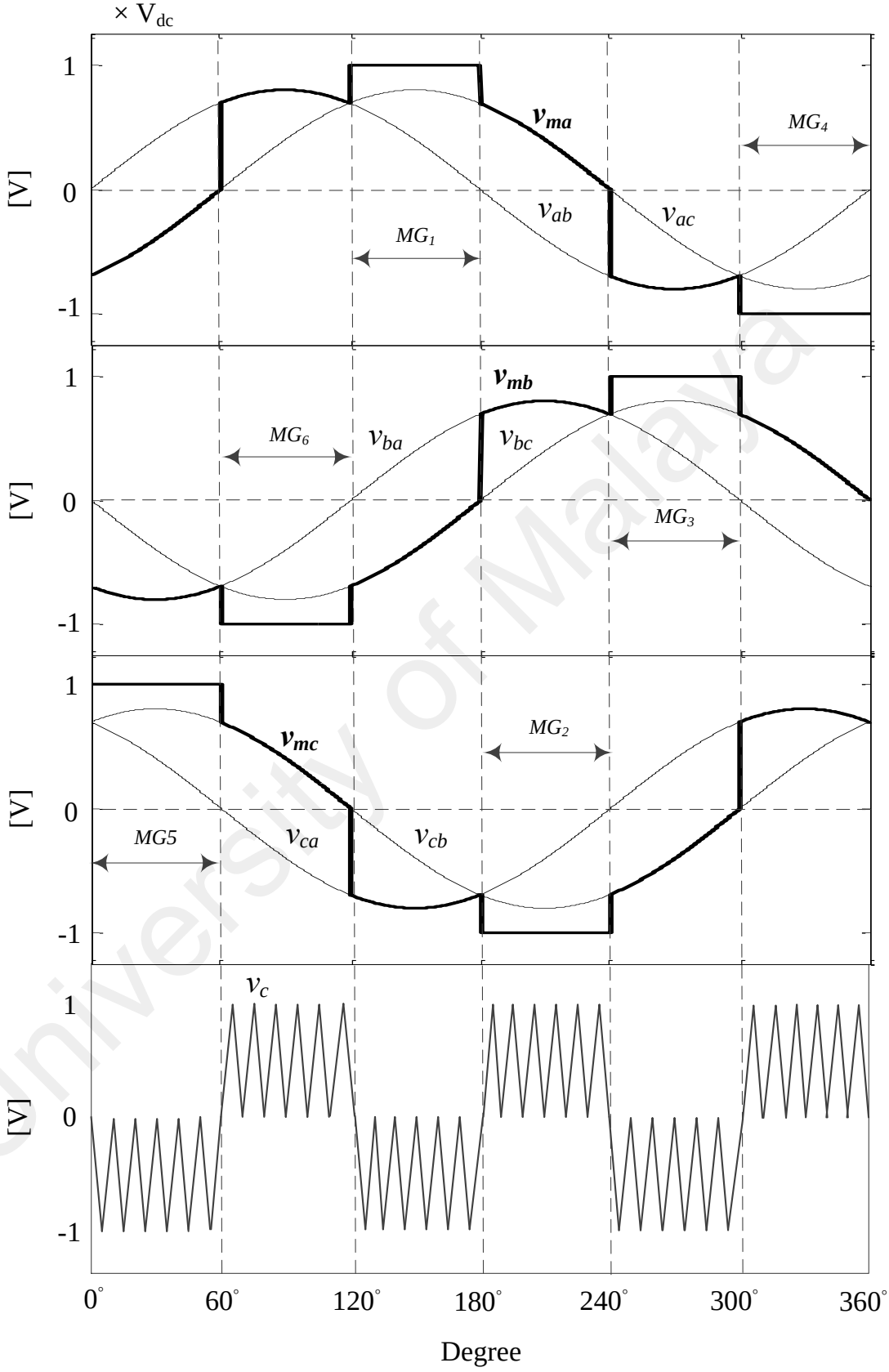



Figure 3-10: Modulating and carrier signals of IZDPWM2 at $M_i = 0.8$ .

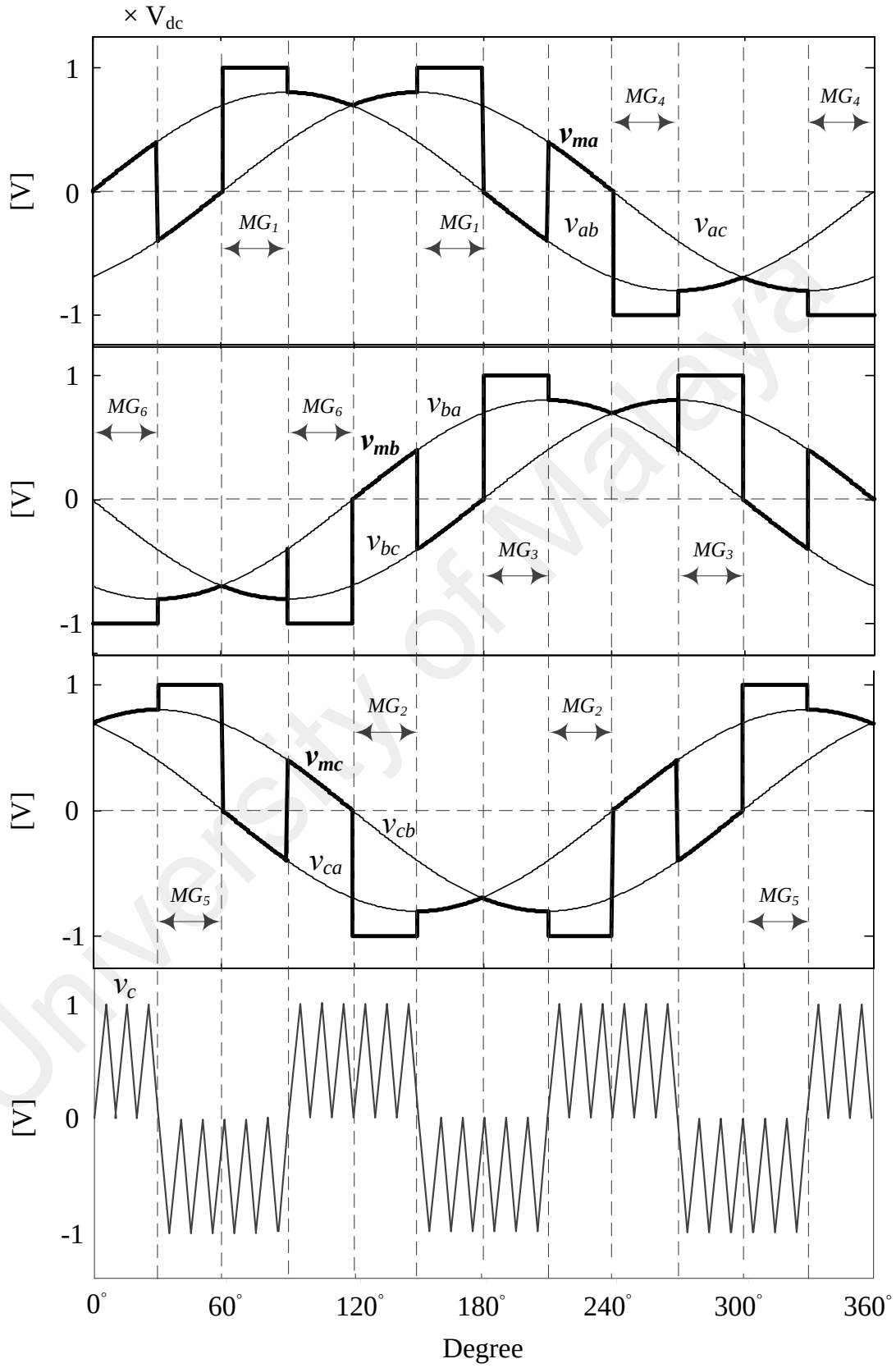



Figure 3-11: Modulating and carrier signals of IZDPWM3 at $M_i = 0.8$ .

### 3.4.4 Amplitude modulation index

Line-to-line voltages are taken as reference signals, therefore, the modulation index is expressed differently in formula (3- 15) that consider the line-to-line values and the amplitude of the carrier signals.

$$M_i = \frac{V_{1m-ll}}{V_{dc}} \quad (3\text{- }15)$$

where $V_{1m-ll}$ $(0 \leq V_{1m-ll} \leq V_{dc})$ is the peak value of the reference signal, and $V_{dc}$ is the peak value of the triangular carrier signal. The maximum output voltage $V_{1m-ll} = V_{dc}$is attained within the preferred linearity range $0 \leq M_i \leq 1$ instead of $0 \leq M_i \leq 1.15$ which is misleading range for practicing engineers.

## 3.5 Simulation results

### 3.5.1 Inverter output linearity range

To ensure the feasibility of the proposed modulation technique, IZDPWM was applied on a 2.4 kW three-phase, three-wire, two-level VSI, which is shown in Figure 3-1. The power circuit was simulated in MATLAB/Simulink power block set software. Table 3-3 shows the specifications of the inverter and the power electronics devices. Also switching frequency is kept constant $f_s$=9 kHz throughout the simulation test. The proposed algorithm was straightforward and simply implemented.

Table 3-3: Specifications of VSI

| | |
|---|---|
| DC Supply | 538 V |
| $L_f$ | 1.5 mH |
| $C_f$ | 10 uF |
| Resistive Load (Y) | 2.4 kW, 380V, 61.25Ω |

The phase voltage $v_{ao}$ and the line-to-line voltage $v_{ab}$, which are based on the implementation of IZDPWM0, are given in Figure 3-12. The modulation index provided in

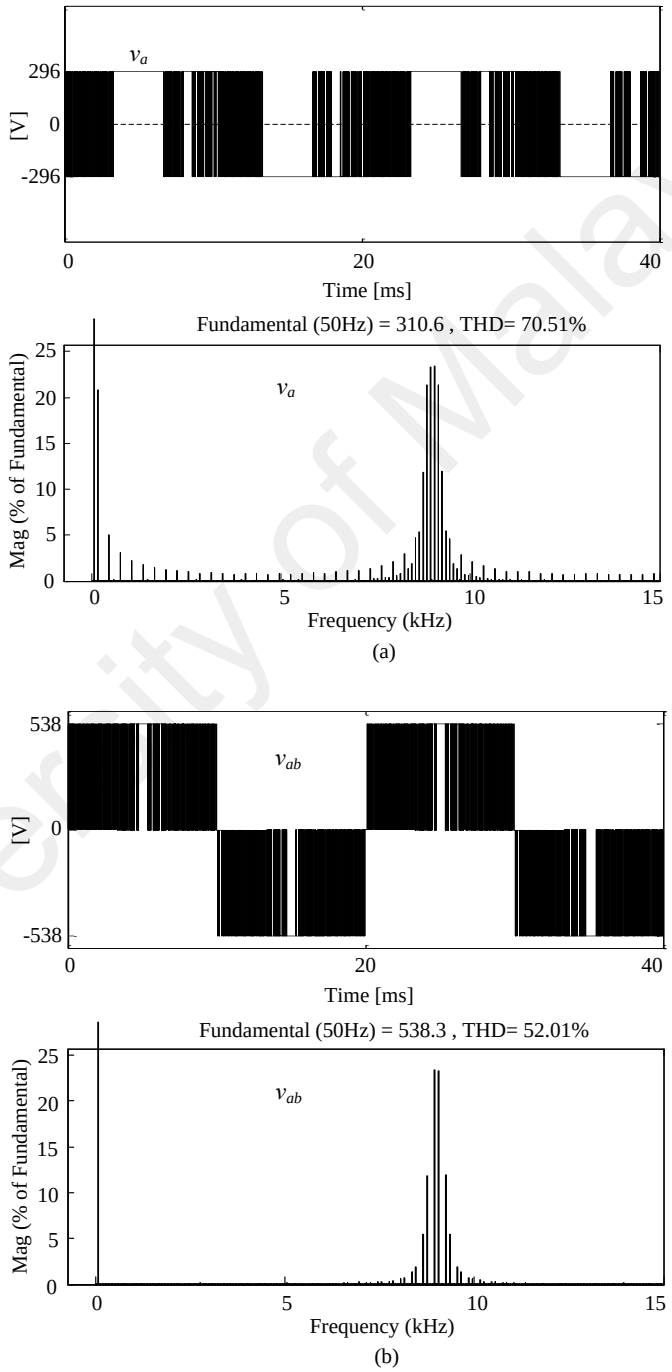



Figure 3-12: Inverter outputs based on IZDPWM0 at $M_i = 1$ (a) source side phase voltage $v_{ao}$ and FFT of $v_{ao}$ (b) line voltage $v_{ab}$ and FFT of $v_{ab}$.

equation (3-15) is considered in the simulation study. At $M_i = 1$ with an input voltage $V_{dc} = 538\,V$ the phase and line fundamental components reached 310.6 and 538.3 V, respectively. Figure 3-13 shows the line-to-line balanced voltages of the inverter load side. As can be seen simulation results clearly shows the linearity performance of the IZDPWM0. Figure 3-12 (a) demonstrates the frequency spectrum of $v_{ao}$. Some harmonics appear, such as the third harmonic component (64.6 V, 20.08% of the amplitude of fundamental component) and its odd multiples (9th, 15th, 21th…). The existence of those subcarrier harmonics in the phase voltage despite their absence in the reference signals indicates that the proposed modulation strategy is IZDPWM. These harmonic components were neutralized in the load side of the inverter. Furthermore, as shown in Figure 3-12 (b), three-wire topology confirms the elimination of third harmonic component and its odd multiples.

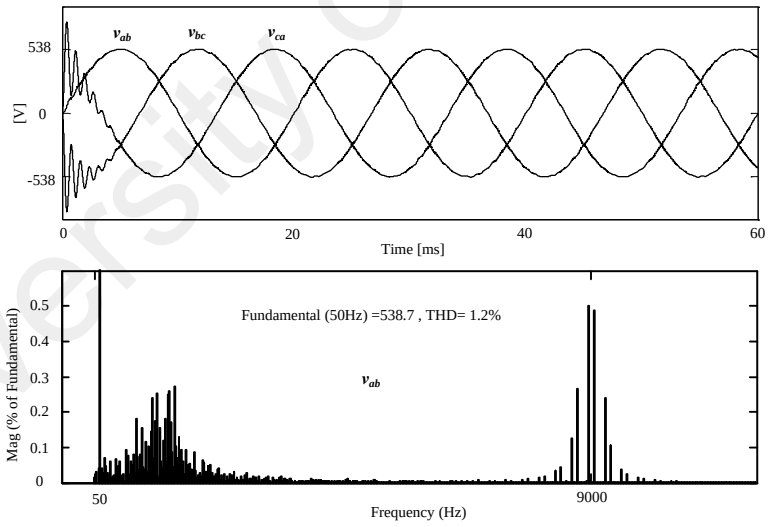



Figure 3-13: Inverter outputs and $v_{ab}$ frequency spectrum using IZDPWM0 under balanced condition at $M_i = 1$.

### 3.5.2 Inverter output signal quality

IZDPWM0, IZDPWM1, IZDPWM2, and IZDPWM3 were compared with DPWM0, DPWM1, DPWM2, and DPWM3, respectively, in terms of THD of $v_{ab}$ at $f_s$=9 kHz. As

depicted in Figure 3-14 applying IZDPWM shows an appreciable output compared with DPWM at different modulation indices.

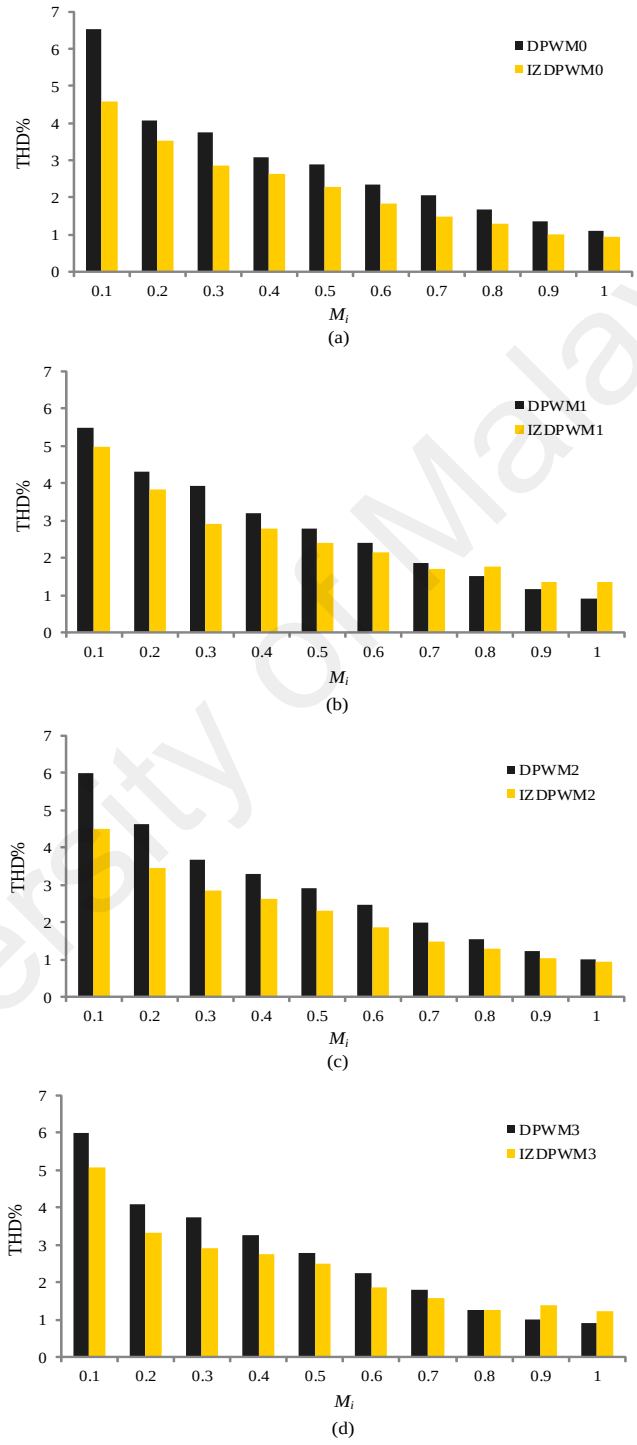



Figure 3-14: THD for DPWMx and IZDPWMx (a) x = 0 (b) x = 1 (c) x = 2 (d) x = 3.

However, slightly higher THD was calculated for IZDPWM1 and IZDPWM3 compared with that for DPWM1 and DPWM3 within the narrow range of 0.8 < $M_i$< 1. Basically, high signal qualities are achieved in high modulation indices and the THD is quite low in high modulation index for both IZDPWM and DPWM techniques. The result of THD in the proposed IZDPWM is attributed to the modulating and carrier signals that were employed. As shown in Figure 3-15, different switching patterns provide the same line-to-line value $v_{ab}$ at $M_i = 0.8$ and $f_s$=900 Hz.

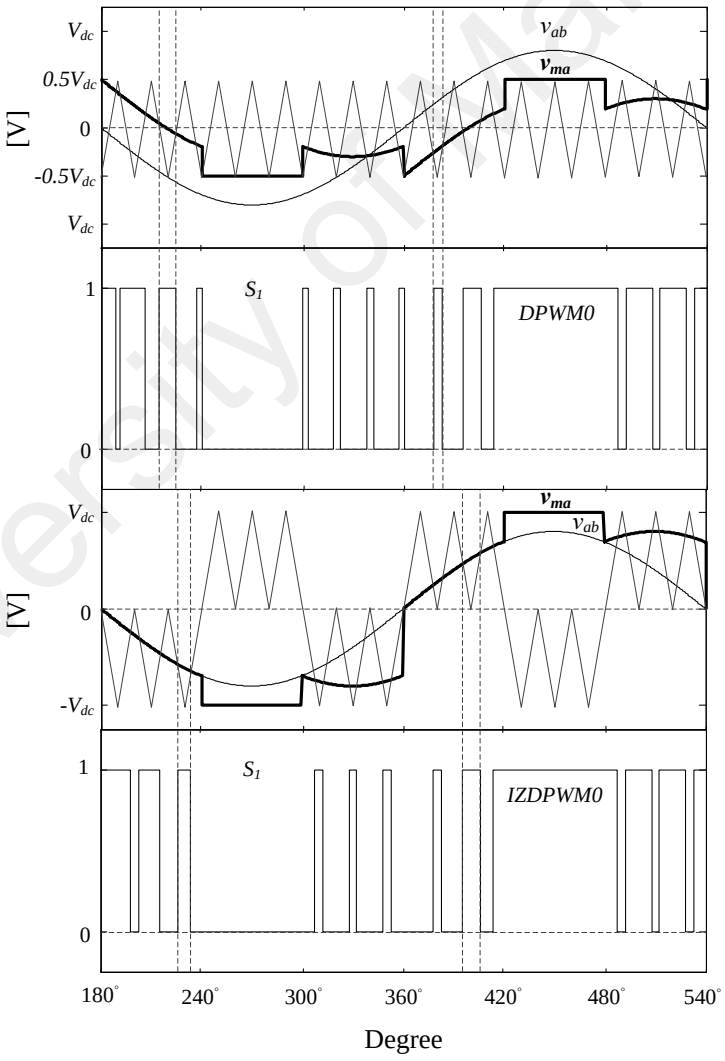



Figure 3-15: Switching patterns of $S_1$ based on DPWM0 and IZDPWM0 at $M_i = 0.8$.

The new proposed method is straightforward to implement with in-phase transfer between line voltages and the original references. However, the original reference signal of DPWM needs to be shifted by $-\pi/6$. The THD of $v_{ab}$ employed DPWM0 and IZDPWM0 is 128% and 115%, respectively.

### 3.5.3 Unbalanced and distorted conditions

As mentioned earlier, the principle of IZDPWM states that for a specific clamped modulating signal, the other two unclamped modulating signals need to be in the opposite polarity. This principle may not apply in generalized unbalanced and distorted conditions. However, IZDPWM0 is the best candidate for dealing with generic unbalanced and distorted conditions because it clamps the biggest reference signal in terms of magnitude. Moreover, IZDPWM0 does not strictly adopt the characteristics of the reference signals. In other words, IZDPWM0 offers better flexibility and robustness for dealing with generic unbalanced and distorted conditions. The unbalanced three-phase line voltage waveforms shown in Figure 3-16 are considered for testing IZDPWM0. The inverter was supplied with $V_{dc} = 310\,V$. For any two adjacent unbalanced line-to-line voltages, the phase shift is not maintained at $2\pi/3$. Clamping duration is proportional to line voltage amplitude. For instance, the lowest amplitude $\nu_{ab}$ leads to clamping leg A for the shortest duration. In other words, the modulating signal $\nu_{ma}$ is clamped for less than $2 * \pi/3$ durations. Despite the sufficiently unbalanced condition, IZDPWM0 manages to linearly copy the reference signals as given in Figure 3-17. To ensure the performance of IZDPWM0 under a distorted condition, the distorted line-to-line reference signals are considered as given in equations (3- 16) to (3-18). Based on the distorted reference signals of THD = 7.48% in Figure 3-18 (a), an output of

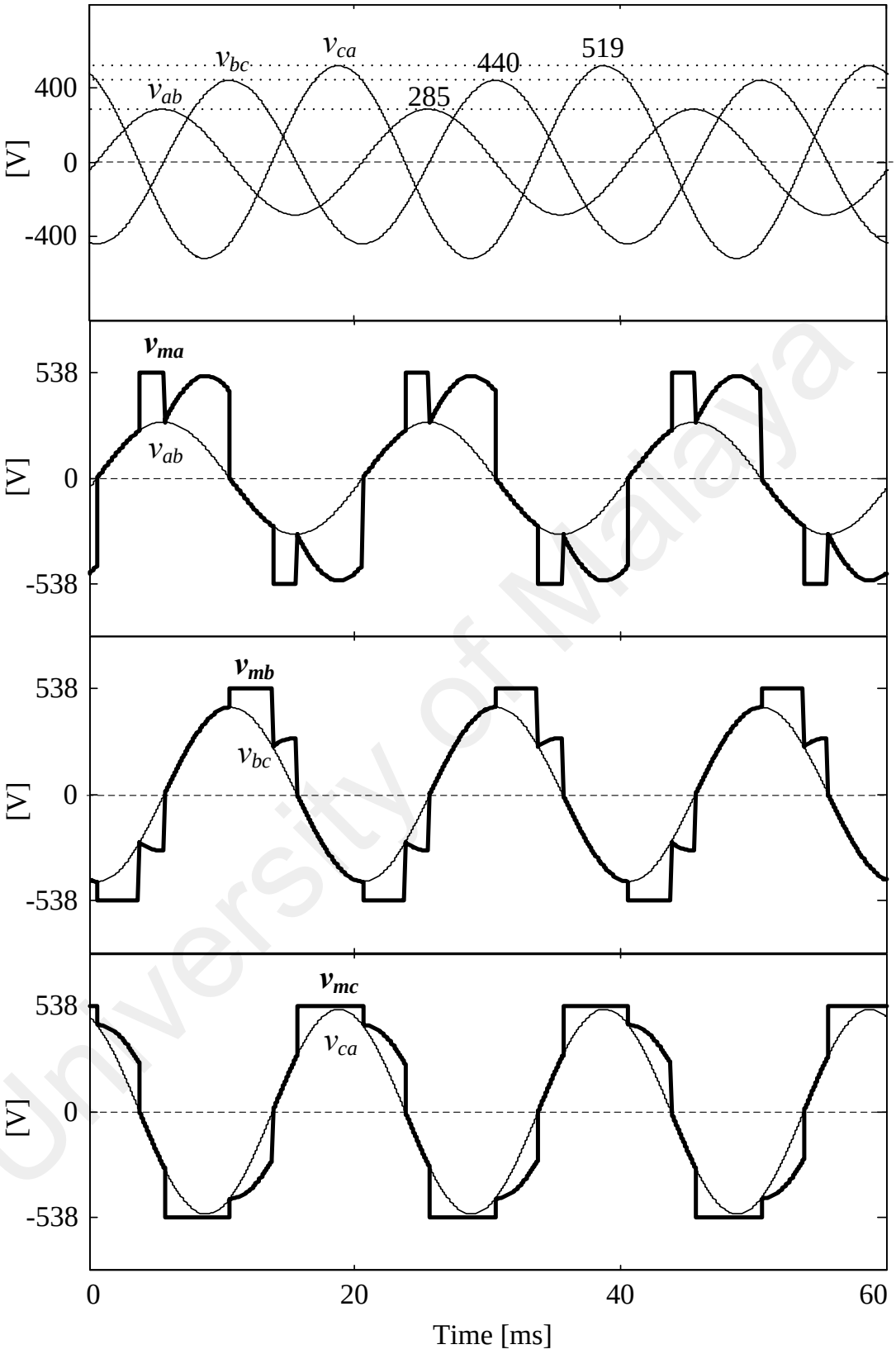



Figure 3-16: Reference and modulating signals of IZDPWM0 under unbalanced condition.

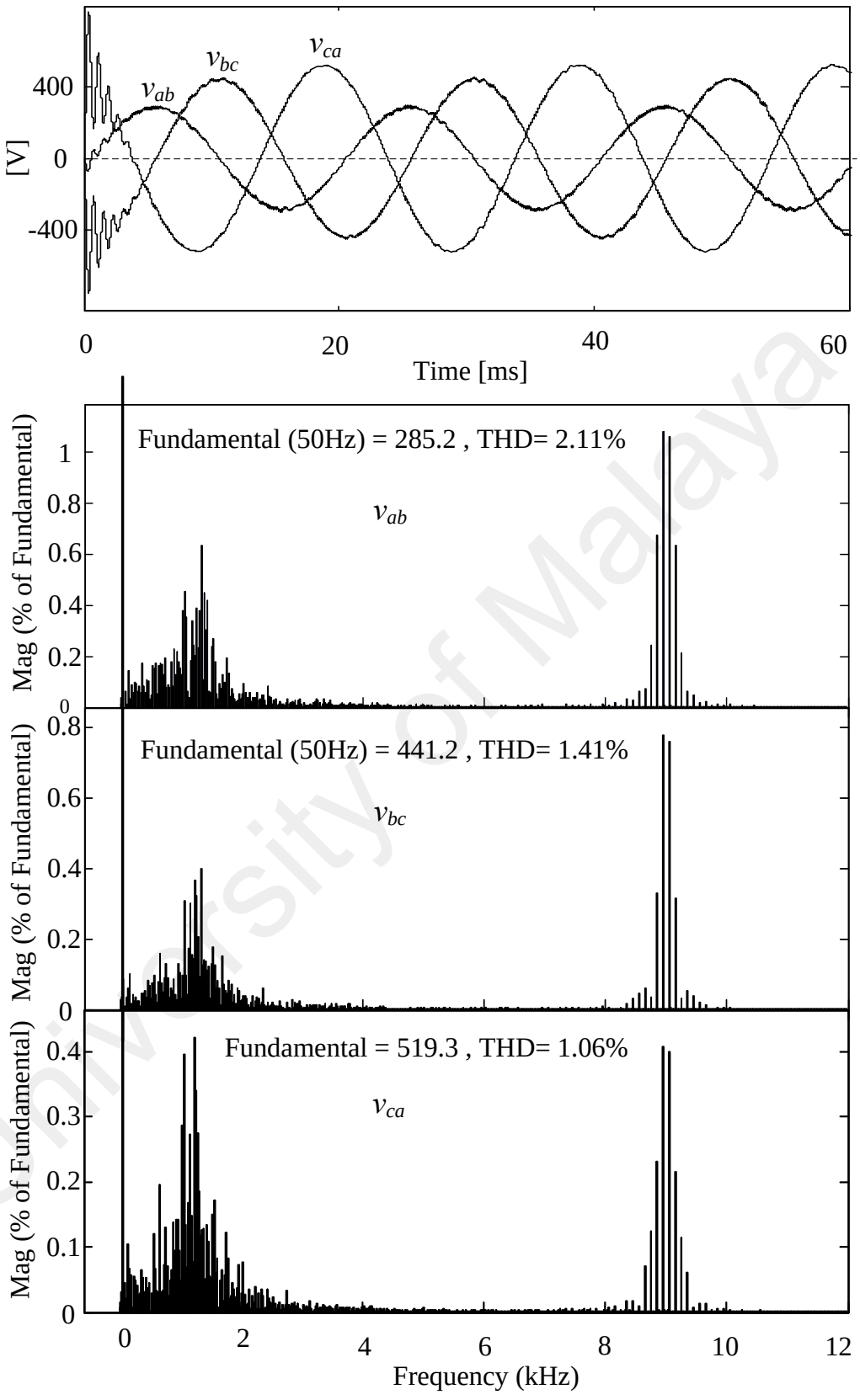



Figure 3-17: Inverter outputs and its frequency spectrum using IZDPWM0 under unbalanced condition.

THD = 8.17 % is attained, as depicted in Figure 3-18 (b). As can be seen, the harmonic components injected into the original reference signals appear exactly in inverter line voltages. Moreover, the shapes of the outputted waveforms are consistent with the distorted reference signals.

$$v_{ab} = 218\,[\sin(\omega_e t) + 0.06\sin(5\omega_e t + \pi/6) + 0.04\sin(7\omega_e t + \pi/6) + 0.02\sin(11\omega_e t + \pi/6)] \quad (3\text{-}16)$$

$$v_{bc} = 218\,[\sin(\omega_e t - 2\pi/3) + 0.06\sin\left(5\omega_e t - \frac{\pi}{2}\right) + 0.04\sin(7\omega_e t - \pi/2) + 0.02\sin(11\omega_e t - \pi/2)] \quad (3\text{-}17)$$

$$v_{ca} = 218\,[\sin\left(\omega_e t + \frac{2\pi}{3}\right) + 0.06\sin\left(5\omega_e t + \frac{\pi}{2}\right) + 0.04\sin\left(7\omega_e t + \frac{\pi}{2}\right) + 0.02\sin(11\omega_e t + \pi/2)] \quad (3\text{-}18)$$

For the purpose of validating IZDPWM0 for distorted and unbalanced condition line-to-line signals given in equations (3- 19) to (3- 21) are considered as reference signals. The unbalanced voltages include the different value of positive and negative-sequences. The positive-sequence is 80% of the rated grid voltage 538 V, with the phase of 0°. The negative-sequence is 20% of the rated grid voltage with the phase of -60°. The reference signals are distorted using 5th and 7th harmonics. The magnitudes of the harmonics with respect to the rated grid line voltage are 3.5% and 3% respectively. It worth to mention that most ac systems only contain odd harmonics in their Fourier series expansions while even harmonics are regarded negligible. The three-phase reference voltages are described as follows:

$$v_{bc} = 538\,[0.8\,sin(\omega_e t) + 0.2\,sin\left(\omega_e t - \frac{\pi}{3}\right) + 0.035\,sin(5\omega_e t) + 0.03\,sin(7\omega_e t)] \quad (3\text{-}19)$$

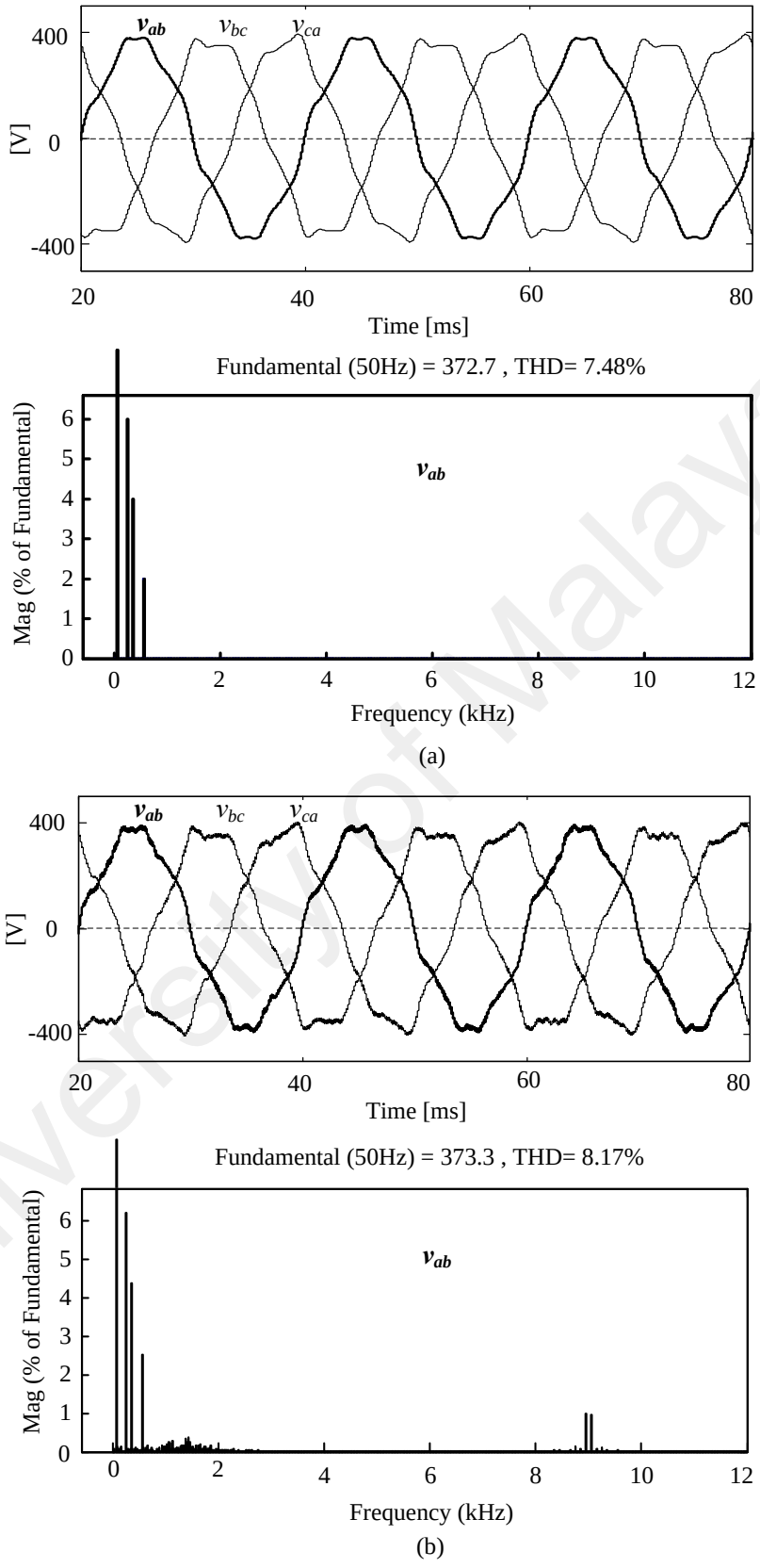



Figure 3-18: IZDPWM0 waveforms under distorted condition (a) original reference signals and its frequency spectrum (b) inverter outputs and its frequency spectrum.

$$v_{bc} = 538\,[0.8\,sin\left(\omega_e t - \frac{2\pi}{3}\right) + 0.2\,sin\left(\omega_e t + \frac{\pi}{3}\right) + 0.035\,sin\left(5\omega_e t + \frac{2\pi}{3}\right) + 0.03\,sin(7\omega_e t + \pi/3)] \quad (3\text{-}20)$$

$$v_{ca} = 538\,[0.8\,\sin\left(\omega_e t + \frac{2\pi}{3}\right) + 0.2\,\sin(\omega_e t - \pi) + 0.035\,\sin\left(5\omega_e t - \frac{2\pi}{3}\right) + 0.03\,\sin(7\omega_e t - \pi/3)] \quad (3\text{-}21)$$

Under balanced and undistorted condition that each inverter leg is clamped to either of dc-links for 60°; however the weak condition clamp legs ‘a’, ‘b’, and ‘c’ to the dc links for 71°, 38°, and 71° respectively as illustrated in Figure 3-19.

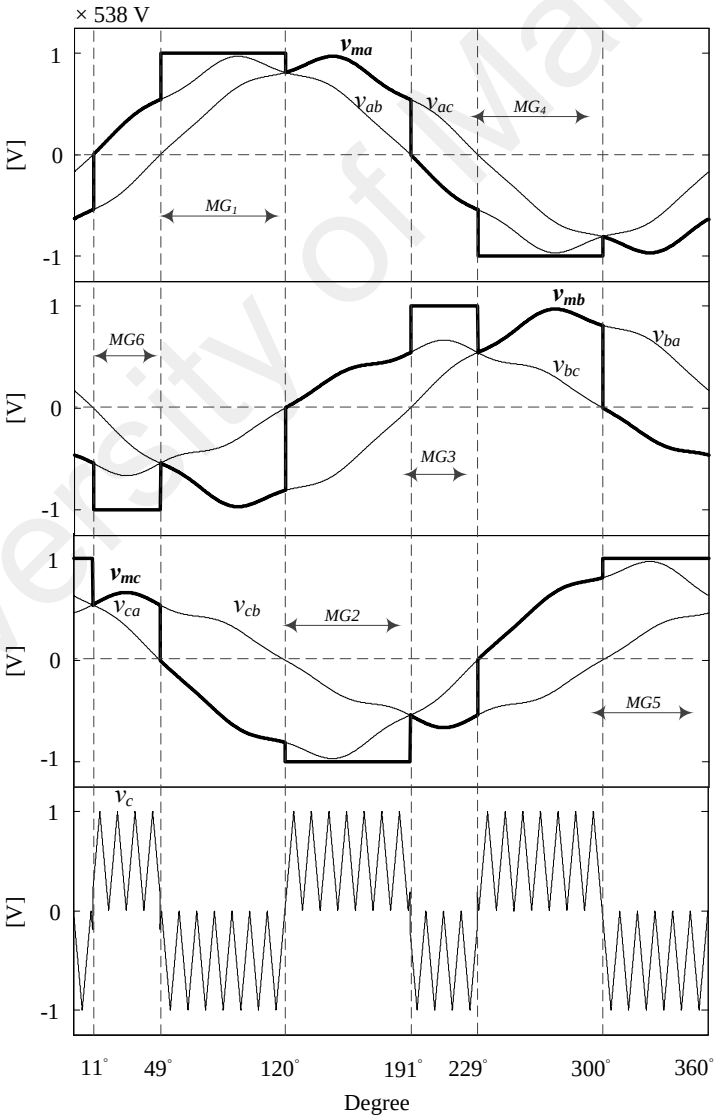



Figure 3-19: IZDPWM0 modulating signals under distorted and unbalanced condition.

According to the reference signals, the amplitude of the fundamental component and the THD of line voltages $v_{ab}$, $v_{bc}$ ,and $v_{ca}$ are 494V 5.36% , 323.7V 8.42%, and 493.7V 5.55% respectively. Simulation results are presented in Figure 3-20 that are significantly consistent with the given distorted and unbalanced reference signals.

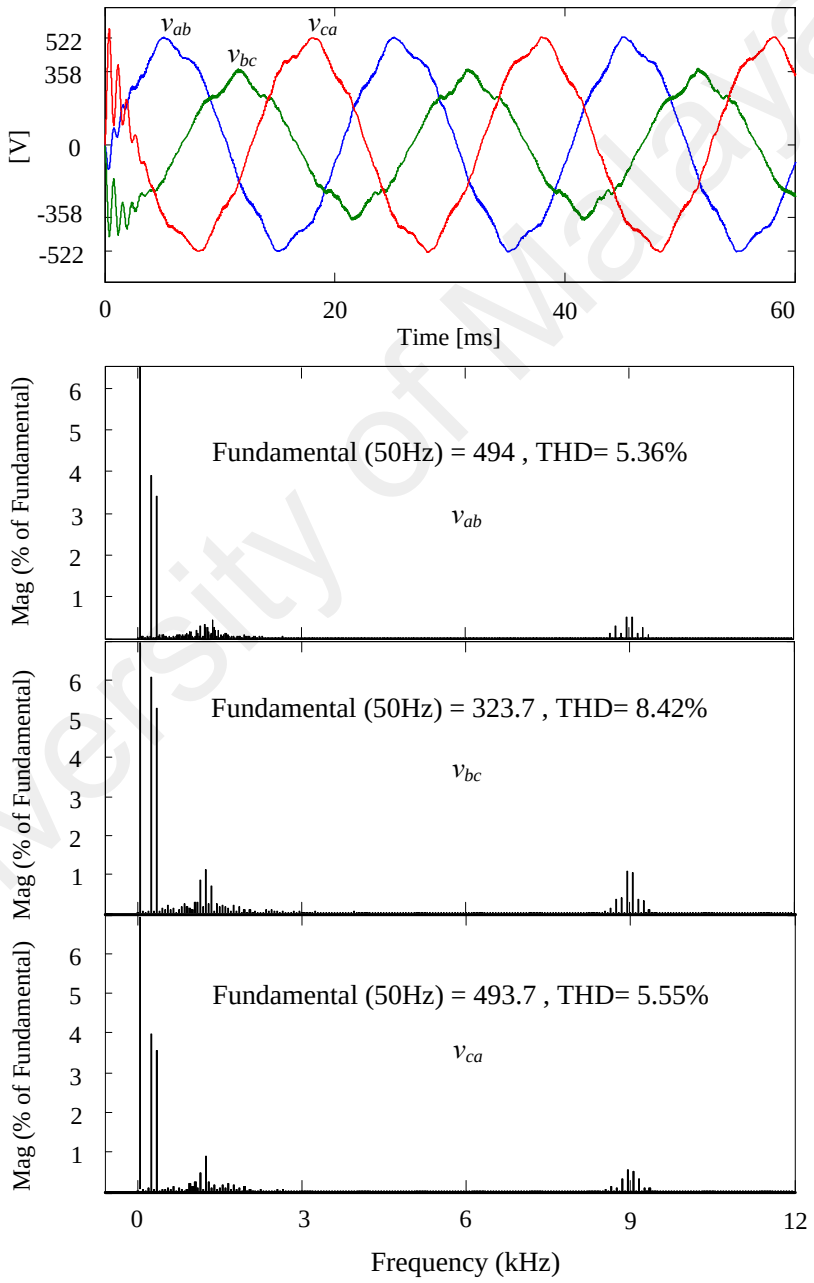



Figure 3-20: Simulated IZDPWM0 under unbalanced and distorted condition.

### 3.5.4 Switching frequency

In general, two types of semiconductor losses occur in the VSIs. Conduction loss is due to the voltage drop across the active semiconductor device when conducting current. The conduction loss is almost the same for two counterparts (DPWM, IZDPWM) because of similar clamping periods. The switching loss occurs at each current commutation of the device and is strongly related to the switching frequency $f_{sw}$. In addition, the signal quality depends on the switching frequency. To demonstrate the potential advantages of the proposed method, the inverter was modulated to produce an output signal of a specific quality (THD) by varying the switching frequency with the use of two different methods, namely, DPWM0 and IZDPWM0. As depicted in Figure 3-21 and Figure 3-22 the THD of the output of the inverter that used IZDPWM0 at 3.63 KHz is closest to the THD of the output of the inverter that used DPWM0 at 9 KHz. Switching losses are proportional to the switching frequency. Therefore, IZDPWM0 produced an appreciable output with reduced $f_{sw}$. Hence, using IZDPWM0 at lower switching frequency results in higher inverter efficiency.

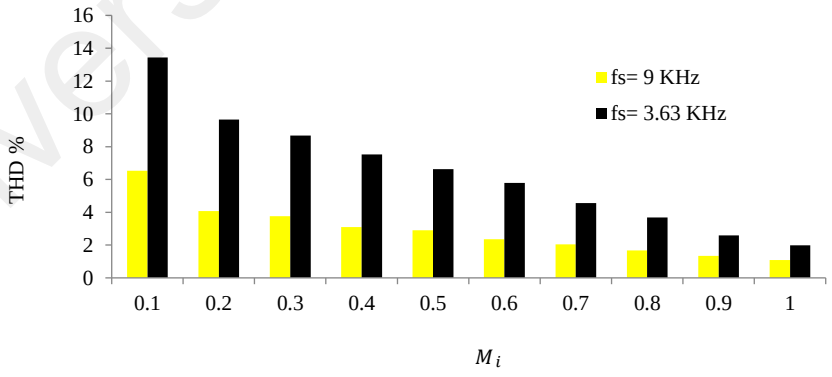



Figure 3-21: THD at different switching frequency for DPWM0.

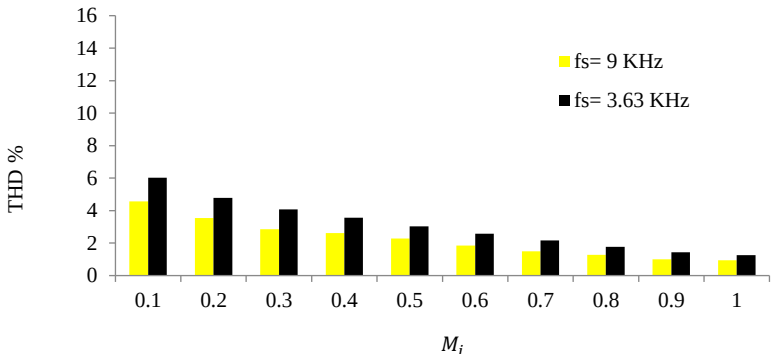



Figure 3-22: THD at different switching frequency for IZDPWM0.

## 3.6 Summary

A new scalar implicit zero-sequence discontinuous PWM (IZDPWM) for two-level, three-wire voltage source inverters was introduced. IZDPWM is the first scalar PWM method that directly uses line-to-line voltages as reference signals instead of phase voltages. Therefore by considering the line values, IZDPWM is implemented differently from all existing scalar PWM methods that take the phase values as reference signals. The injection of zero-sequence is necessitated in advanced scalar PWM methods for the sake of extending the inverter output voltage control linearity range, improving the waveform quality, decreasing the switching losses. The mentioned merits are realized in IZDPWM with no zero-sequence signals injected in the three reference line-to-line voltages. The proposed scheme was successfully implemented on three-phase, three-wire two-level voltage source inverter. Moreover, the proposed IZDPWM gave an appreciable output in balanced, unbalanced and distorted conditions which might be experienced in many applications. The well-known DPWM technique was considered to come up with fair comparison with the proposed IZDPWM in terms of signal quality, switching frequency, and linearity range. The subsequent chapter includes application of IZDPWM in closed loop control of grid-connected inverters under balanced, unbalanced and distorted condition.

# CHAPTER 4: IZDPWM-BASED FEEDFORWARD CONTROLLER FOR GRID-CONNECTED INVERTER

## 4.1 Introduction

In grid-connected inverters, feedforward controller accurately compensates a large number of harmonic components of the injected current. This fast and straightforward controller tackles the grid dynamic voltage disturbances without further harmonic analysis. In this chapter the feedforward controller using the proposed IZDPWM with in-phase transfer between inverter line-to-line voltages and the modulator original references is implemented regardless grid topology. Furthermore, the instant value of input dc voltage and reference current are considered in modulator in order to explore full advantages of IZDPWM. The performance of the proposed IZDPWM-based feedforward controller was validated through simulation tests on the grid-connected inverter with L-type filter for all grid circumstances.

## 4.2 DG inverter control under distorted grid voltage condition

The non-sinusoidal profile of the grid voltage waveform has adverse effects on the injected grid current. DG systems have to tackle this problem, and ensure high-quality current injected to the utility in all grid conditions. The grid-connected two-level inverter shown in Figure 4-1 is considered as platform to investigate the presented control method. The inverter low pass filter may not eliminate current harmonics under weak grid circumstances; since low-order harmonics of the injected current are not naturally attenuated. Increasing the bandwidth of the PI controller is one of the methods followed for rejecting more of low-order harmonics. In other words a lower grid current THD is attained at larger bandwidth; however system stability requirements ultimately determine the upper bandwidth limit of the PI controller (Abeyasekera et al., 2005; Erika & Holmes, 2003). Moreover, large system

bandwidth also decreases the noise immunity of the system. Therefore, controllers that further assist in mitigating the current disturbance under weak grid condition is a prominent aspect of the grid-connected inverter control. These alternative control systems have to realize improved tracking and increased rejection of external voltage disturbances without additional hardware costs.

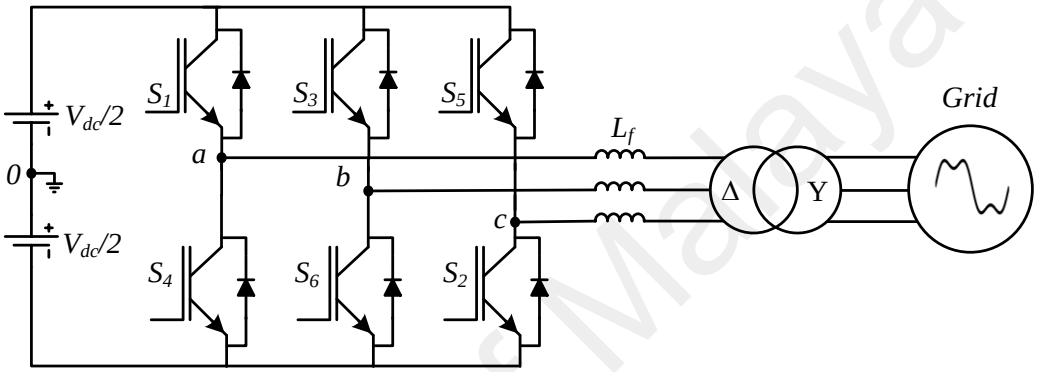



Figure 4-1: Schematic of a grid-connected two-level VSI.

The adverse effects of the distorted grid voltage on the quality of the injected current are eliminated in different current regulators. The multiple PR controllers are used to achieve infinite loop gain at targeted low-order harmonics frequency (Liserre et al., 2006b). PR compensators effectively suppress the unwanted harmonics and eliminate the steady-state error. Nevertheless, PR controllers may not serve in compensating numerous harmonics; and excessive computation makes the controller unstable and costly (Liserre et al., 2006c). In other words PR controllers are designed for preset harmonics and only periodic distortion harmonics can be eliminated. Feedforward control is another alternative that tackles the power quality problems in DG systems at random and non-periodic grid circumstances (Abeyasekera et al., 2005; Li et al., 2013; Qingrong & Liuchen, 2008; Wang et al., 2010). This reliable scheme may reject dynamic voltage disturbances in wide range of low frequency harmonics and provides fast response.

## 4.3 The proposed IZDPWM-based feedforward control scheme

The main objective of the control strategy for the grid-connected inverter is to control the current injected into the grid so that it follows the grid voltage in phase and its amplitude can be regulated as required. The inverter output current should have limited distortion to avoid any damage to the sensitive equipment connected to the utility grid ("IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems," 1993). The block diagram of the proposed IZDPWM-based feedforward controller is shown in Figure 4-2. The controller consists of a closed loop current control and an open loop voltage feedforward loop. The negative feedback current regulator compares the grid current with the grid current desired reference $i_{ref}$ and switches the VSI to track the set reference value. Meanwhile, the feedforward control method directly uses the grid voltage disturbances to stop undesired change in the inverter output current. A combination of both current control and voltage feedforward techniques is able to achieve superior performance. For synchronization, a PLL is used to detect the phase angle θ of the grid voltage. The grid current reference $i_{ref}$ is set based on the desired active and reactive power level. In order to inject active power only, the phase angle of the injected current is locked on the θ-30° due to 30° phase shift between phase and line-to-line voltages. A PI controller with high dc gain provided by the integral action properly regulates dc current with minimized steady state error. In contrast, it offers unsatisfactory performance in ac current control due to the limitation in the gain required for avoiding tracking error. Thus, the transformation of the three-phase ac current into the *dq* frame is a necessary step. As a consequence, the control variables are becoming dc signals that help to practice the full advantages of the PI controller (Abeyasekera et al., 2005; Erika & Holmes, 2003). It worth mentioning, the synchronous *dq* frame control is very convenient for the power flow control. The major constraint faced with linear closed loop ac current regulators in the synchronous *dq* rotating frame is the

proportional gain limitation in low-order harmonics of the injected current caused by the grid voltage harmonics. Therefore, the challenge mentioned above has been met in the presented work by incorporating voltage feedforward loop.

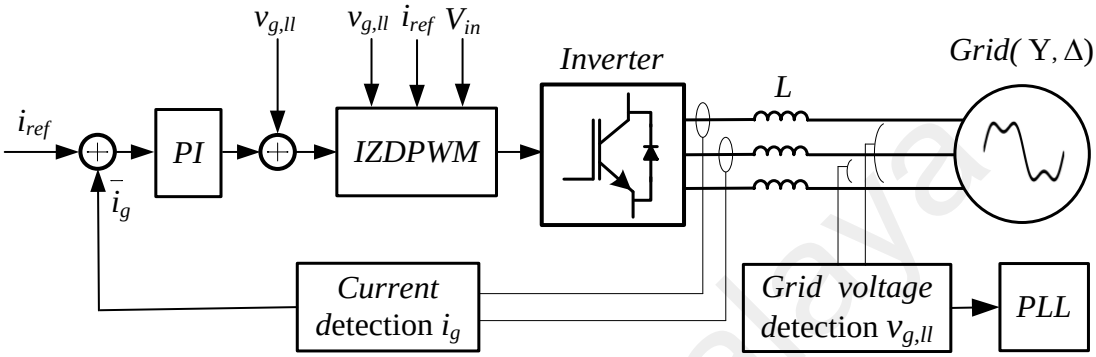



Figure 4-2: Block diagram of the IZDPWM-based feedforward controls for the grid-connected inverter.

### 4.3.1 Feedforward function

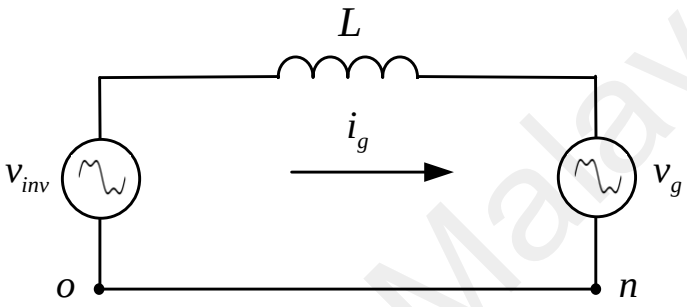
The VSI is switched at a significantly high frequency that has no effect on the control loop dynamics. Under the aforementioned assumption, the inverter system can be represented by linearized average switching model (ASM) (Shen, Xu, Cao, & Zhu, 2008). Using ASM, Figure 4-3(a) shows single-phase representation model of the grid-connected inverter. According to Kirchhoff voltage law (KVL), the relation for the current flowing through the grid $i_g$ is given by

$$i_g = (v_{inv} - v_g)/Ls \qquad (4\text{-}1)$$

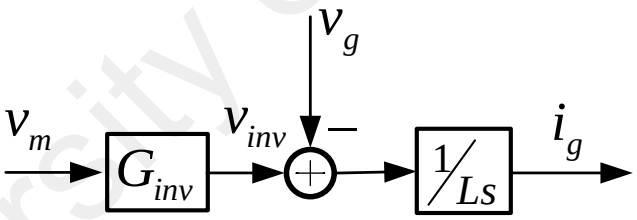
where $v_{inv}$ and $v_g$ are the inverter and grid voltages, respectively. Also, s denotes the Laplace operator. Figure 4-3(b) shows the model of the inverter, where $v_m$ is the modulating signal and the inverter power circuit is represented by the gain of $G_{inv}$ as follow:

$$G_{inv} = V_{in}/V_{tri} \tag{4- 2}$$

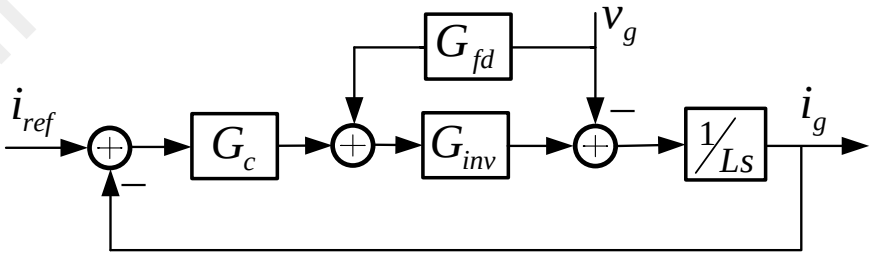
where $V_{in}$ is the input dc voltage and $V_{tri}$ is the amplitude of the carrier. Figure 4-3(c) shows the block diagram of the proposed control strategy, where $G_c$ and $G_{fd}$ is the transfer function of the current requlator and feedforward function, repectively.




(a)




(b)




(c)

Figure 4-3: Grid-connected inverter with *L* filter (a) Representation of single-phase circuit (b) Block diagram of the model (c) Block diagram of the proposed control strategy.

In Figure 4-3(c) relationship between the inputs and output can be expressed as follows:

$$i_g = \frac{G_c G_{inv}}{Ls + G_c G_{inv}} i_{ref} + \frac{G_{fd} G_{inv} - 1}{Ls + G_c G_{inv}} v_g \quad (4\text{- }3)$$

Obviously applying the appropriate feedforward function given in equation (4- 4), the effect of $v_g$ will be eliminated. Hence, voltage feedforward loop significantly can suppress the effect of grid voltage disturbances. As expressed in equation (4- 5), the steady-state error of $i_g$ is only caused by current reference tracking error. Furthermore, if the current requlator loop gain is large enough in magnitude, static tracking error will be substantially reduced.

$$G_{fd} = 1 / G_{inv} \quad (4\text{- }4)$$

$$i_g = \frac{G_c G_{inv} / Ls}{1 + G_c G_{inv} / Ls} i_{ref} \quad (4\text{- }5)$$

However, optimal implementation of the IZDPWM-based feedforward controller requires some modification on the IZDPWM modulator suggested in (Shayestehfard et al., 2015). These modifications are related to inverter gain $G_{inv}$ setting and clamped areas of the modulating signals. **Error! Reference source not found.** shows a flow diagram of the generalized IZDPWM implemented with feedforward controller. Where $v_{g,ll}$ is grid line-to-line voltages ($v_{ab}$, $v_{bc}$, $v_{ca}$).

### 4.3.2 Inverter gain

Considering equations (4- 2) and (4- 4), feedforward function $G_{fd}$ depends on the inverter gain while $G_{inv}$ is controlled by input dc voltage. A typical DG system may experience fluctuations in dc input voltage due to uncertainties in renewable energy sources. In the case

of a solar-inverter, for instance, the input voltage fluctuation occur due to varying irradiance level. Moreover, the unbalanced grid may lead to unstable dc input. Despite to unregulated input dc voltage, the open loop nature of feedforward control necessitates a reliable and stable inverter gain to efficiently reject the grid voltage disturbances. Thus, another feedforward loop that considers the input dc values is included in the implemented controller. As a result and based on equations (4- 2), the adopted IZDPWM illustrated in **Error! Reference source not found.** keeps the inverter gain unchanged at unity, in spite of variation of $V_{in}$. In fact, $G_{inv}=1$ is the maximum possible gain for the inverter that is the optimum value for both creating high quality inverter output signals and optimized dc input usage. It is worth to mention that DG systems always include the detector of input dc voltage for the purpose of protection and power managment

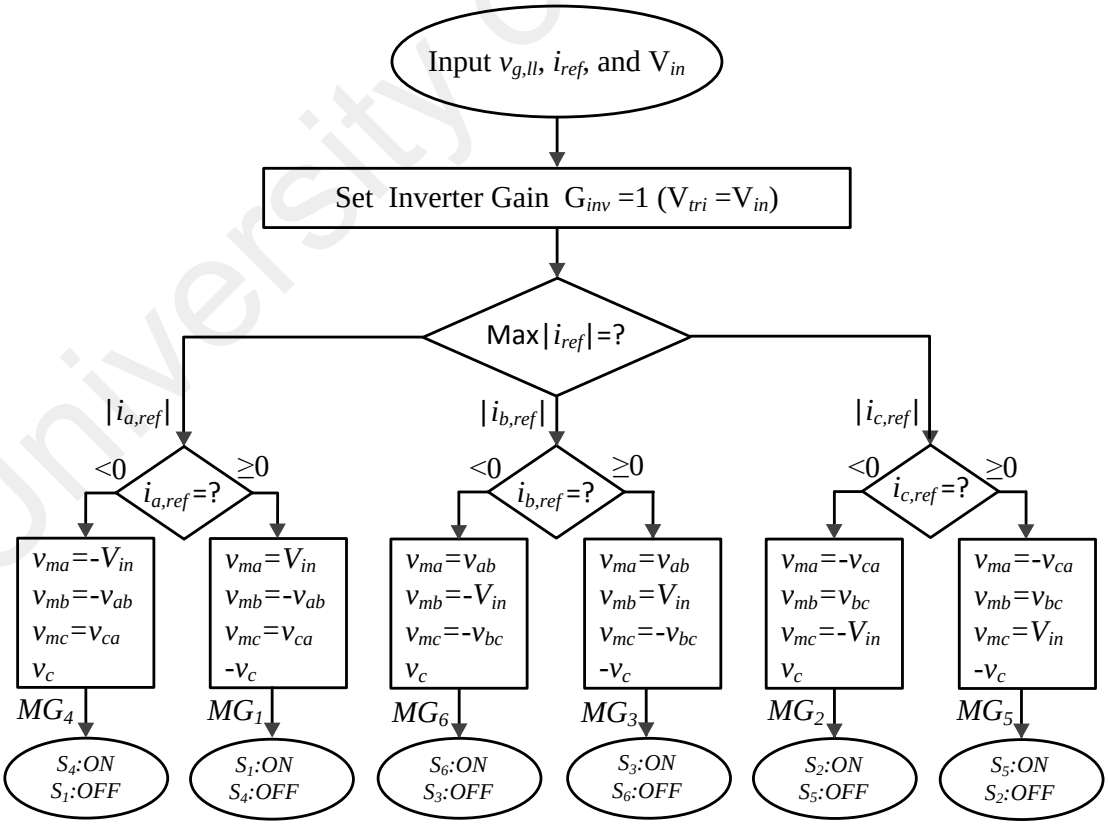



Figure 4-4: Flow diagram of the generalized IZDPWM.

like maximum power point tracking (MPPT), therefore, the required voltage sensor for dc voltage feedforward loop does not impose any extra cost.

### 4.3.3 Generalized IZDPWM modulator

IZDPWM0 was developed based on maximum absolute magnitude test that simply maintains its principle for balanced, unbalanced, and distorted reference profiles. Due to the foregoing merits, IZDPWM0 is adopted along with feedforward controller to effectively deal with the distorted grid condition. However, IZDPWM0 does not serve accordingly in closed loop grid connected inverter control since the clamped regions are decided based on the line-to-line voltage values that for sinusoidal reference signals, IZDPWM0 centers the non-switching periods for each phase leg symmetrically around the positive and negative peaks of its reference line-to-line voltage. Basically clamping around the peak voltage is not appropriate for active power injection because of the 30° phase shift between active current and line voltage. In other words, this method does not clamp the inverter leg at the maximum of the corresponding current. Consequently, power losses are not effectively decreased. Hence, in generalized IZDPWM, the clamped regions of the modulating signals are selected according to the current reference $i_{ref}$ (see **Error! Reference source not found.**). Therefore in the proposed method, the inverter legs are clamped at highest absolute grid current. Clamping the inverter legs based on the phase currents effectively reduces the switching losses (The Dung et al., 2011). The MGs are defined based on grid reference current $i_{ref}$. Whereas the modulating signals $\nu_{ma}$, $\nu_{mb}$, and $\nu_{mc}$ are derived based on the line-to-line values $\pm\nu_{ab}$ , $\pm\nu_{bc}$, and $\pm\nu_{ca}$ at each and every MG. Hence, a non-switching period of each leg can be feasibly placed where the corresponding reference signal is maximum or minimum among the three-phase set. Also, the phase shift between the injected current and grid voltage simply can be selected according to the desired power factor.

## 4.4 Filter design

The first order L filter has excellent performance in terms of voltage to current conversion and incorporate to effectively attenuate the switching frequency ripple and the even higher frequency harmonics. However, the inductance value has an upper and lower limits. The upper limit of filter inductance L is proportional to the tolerable voltage drop that is related to the available input dc source. The inverter is modulated to output the maximum voltage and rated current at unity power factor. Thus, the upper limit inductance is attained as follows

$$L_{max} = \frac{\sqrt{\frac{V_{dc}{}^2}{2} - V_{gll}{}^2}}{\sqrt{3}\omega_g I_g} \qquad (4\text{- }6)$$

where $V_{dc}/\sqrt{2}$ is the maximum possible inverter output line-to-line voltage, $V_{gll}$ is the grid line-to-line voltage, and $I_g$ is the grid current at full power condition (Jalili & Bernet, 2009). Assuming the simulated grid specifications of 130 V, 10.6 A, 50 Hz, and 2.4 kW as full power condition and corresponding input dc value of $V_{dc}$=220 V; the reactor value based on equation (4- 6) results in L < 14.8 mH. In one hand the filter size should be as low as possible, in order to decrease power losses and raise overall efficiency. In the other hand the lower inductance needs to meet the grid current quality standards. However, the filter reactor size is strongly related to the switching frequency. The higher switching frequency results in smaller inductor value. The simulation tests at $f_{sw}$=4.8 kHz gave appreciable output with filter inductance of 10 mH. The resistance of L filter is assumed to be negligible in comparison to the inductive reactance at the adopted switching frequency.

## 4.5 Simulation results

To evaluate the behaviour of the proposed IZDPWM-based feedforward method simulation tests were conducted. The simulated grid-connected two-level inverter is depicted in Figure 4-5. The system parameters are given in Table 4-1. The inverter PWM switching time set to the $T_{sw}$ =208.34 µs.

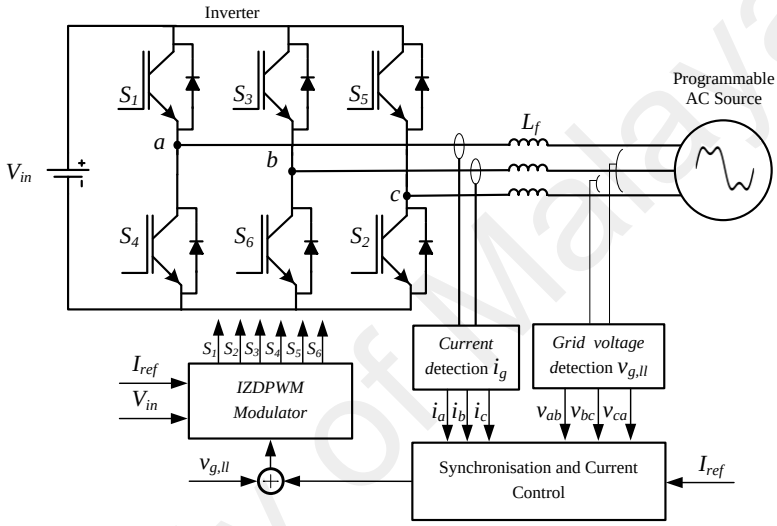



Figure 4-5: The simulated grid-connected inverter.

### 4.5.1 Sinusoidal grid voltage

Figure 4-6 provides the simulation results at full load (2.25 kW) under sinusoidal balanced grid voltage. The harmonics spectrum in Figure 4-7 indicates the attained THD of current $i_a = 10.02\ A$ is 1.46%. The phase shift between current $i_a$ and line-to-line voltage $v_{ab}$is 32°.

Table 4-1: Specifications of the gird-connected VSI

| | |
|---|---|
| DC Supply | 220 V |
| AC Supply | 130 V, 10 A, 50 Hz |
| Maximum power | 2.25 kW |
| $L$ | 10 mH |
| $f_{sw}$ | 4.8 kHZ |

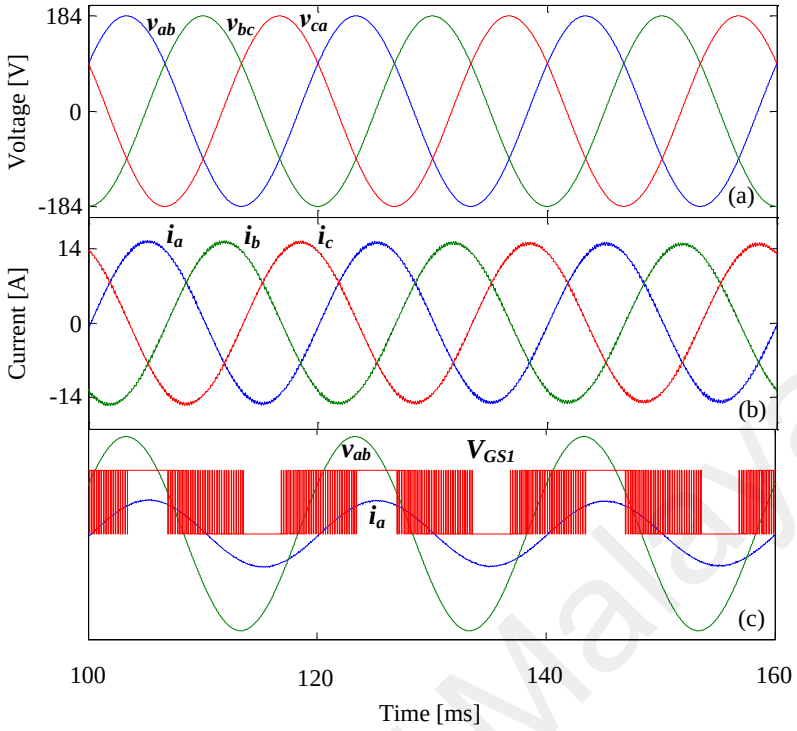



Figure 4-6: Simulation results under sinusoidal condition (a) grid voltage (b) grid current (c) $v_{ab}$, $i_a$and switching patterns of $S_1$.

Considering 30° phase shift between phase and line voltages the phase shift between injected current and grid phase voltage is only $\Phi$ =2° and the power factor of cos$\Phi$=0.994 was obtained. Therefore, the controller precisely regulated the active power to 2.25 kW and the reactive power to 0 kVA per desired. Furthermore, as Figure 4-6(c) shows the proposed method successfully clamps the switches of leg 'a' at the maximum of corresponding current. Accordingly, switch S1 is kept ON and OFF for 2*60° centred on the $i_a$ positive and negative peaks, respectively. It can be observed that the proposed IZDPWM-based method work quite well under balanced and sinusoidal grid voltage condition.

### 4.5.2 Unbalanced grid voltage

The proposed feedforward scheme for the three-phase L-type grid-connected inverter is investigated under unbalanced grid voltage condition. The grid voltage in such circumstance

is generated by considering both positive and negative-sequences. The unbalanced waveform is 80% of rated voltage in positive-sequence with 0° phase shift; whereas the other 20% of rated voltage is taken in negative-sequence with the phase of -60°. Thus, the three-phase grid voltages are as follows

$$v_{ab}=168 \sin(\omega t+19.1°) \quad (4\text{-}7)$$

$$v_{bc}=110 \sin(\omega t - 90°) \quad (4\text{-}8)$$

$$v_{ca}=168 \sin(\omega t + 160.9°) \quad (4\text{-}9)$$

Where $v_{bc}$ of 110 V magnitude maintains the same nominal phase shift, and the voltages $v_{ab}$ and $v_{ca}$ take a magnitude of 168 V with symmetrical phase deviation of 19.1°. Under unbalanced grid voltage condition, the grid voltage and current waveforms are depicted in Figure 4-8. The reference positive-sequence injected grid current is 10 A, and the negative-sequence current reference is 0 A. As can be seen despite remarkable unbalanced grid voltage the injected three phase current is balanced (9.93 A). And phase shift between current and positive-sequence of grid voltage are -31.5° ,-31.7° , and -31.2° respectively. Considering -30° phase shift among phase currents and line-to-line voltages, the PLL precisely synchronized the injected current with the positive-sequence of the grid voltage. Therefore, the proposed IZDPWM-based feedforward scheme successfully regulated the injected grid current under unbalanced grid voltage condition.

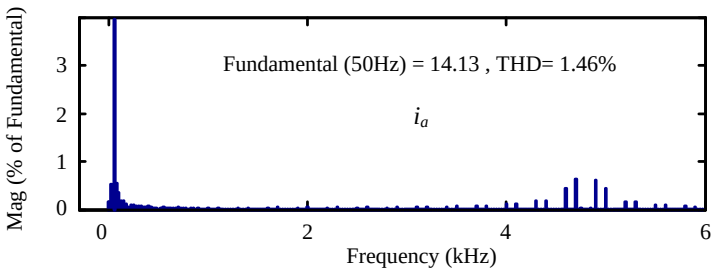



Figure 4-7: Frequency spectra of the injected grid current under sinusoidal grid voltage.

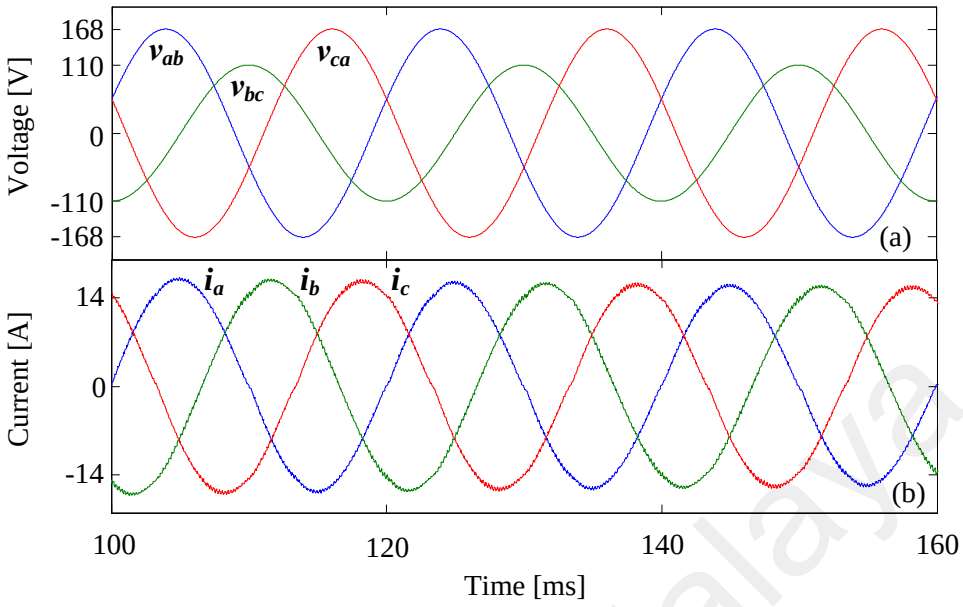



Figure 4-8: Simulation results under unbalanced condition (a) grid voltage (b) grid current.

### 4.5.3 Distorted grid voltage

In order to evaluate the performance of the proposed controller under distorted condition, the sinusoidal voltage waveforms that include its 5th, 7th, 11th, and 13th harmonics are considered. The magnitudes of the harmonics with respect to the fundamental component of the normal grid voltages 130 V are 3.5%, 3%, 1%, and 1%, respectively. In presence of the mentioned harmonics, the THD of the considered grid voltage is 4.82%. Thus, IEEE 519-1992 harmonic restriction standard is maintained ("IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems," 1993). For the purpose of understanding the feasibility of the presented controller under distorted circumstance, a further test that disregard the line-to-line values in the control loop is considered. The grid voltage and current waveforms are depicted in Figure 4-9.

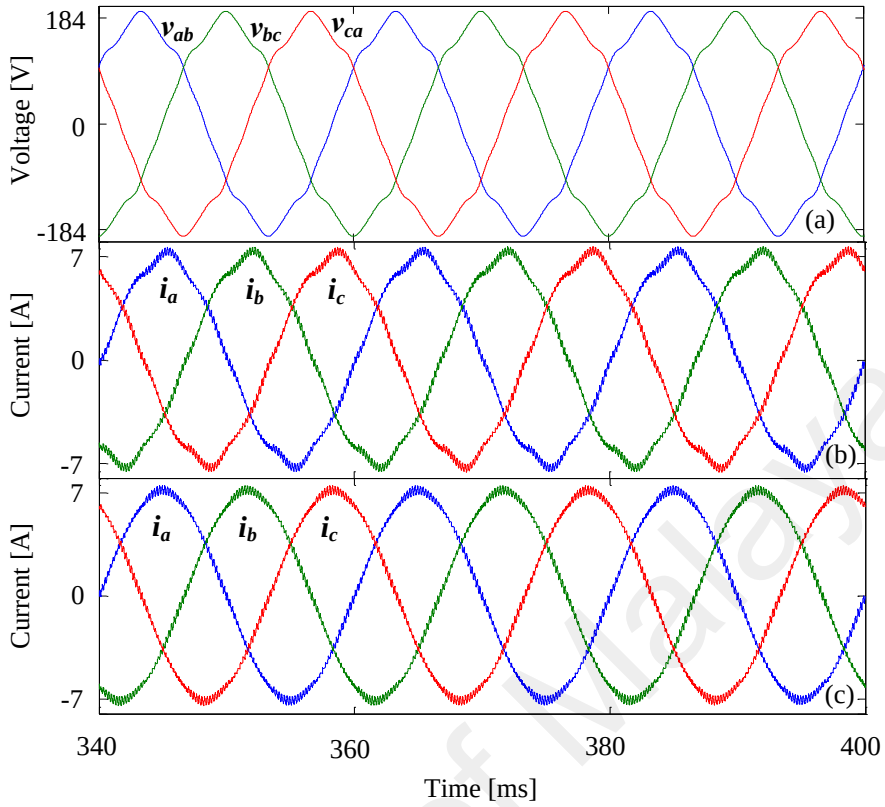



Figure 4-9: Simulation results under distorted condition (a) grid voltage (b) grid current without feedforward loop (c) grid current with feedforward loop.

Figure 4-10 illustrates that, feeding the line-to-line values to the control loop decreased the THD of the injected grid currents from 4.54 % to 2.81%. As shown in Figure 4-10 (b) without feedforwarding the grid voltage, low order harmonics of the magnitudes 2.17%, 2.87%, 0.44%, and 0.51% with respect to the fundamental component appeared in grid current. As depicted in Figure 4-10(c) using the voltage feedforward loop, the low order harmonics, of magnitudes 0.25%, 0.64%, 0.16%, and 0.21% respectively are attenuated in the injected grid current. These harmonics are calculated with respect to the peak value of the fundamental grid current 7.078 A. It can be seen from Figure 4-10 that feedforward loop has no impact on switching frequency harmonics attenuation. Thus, the proposed control scheme effectively suppresses current harmonics caused by the distorted grid voltage.

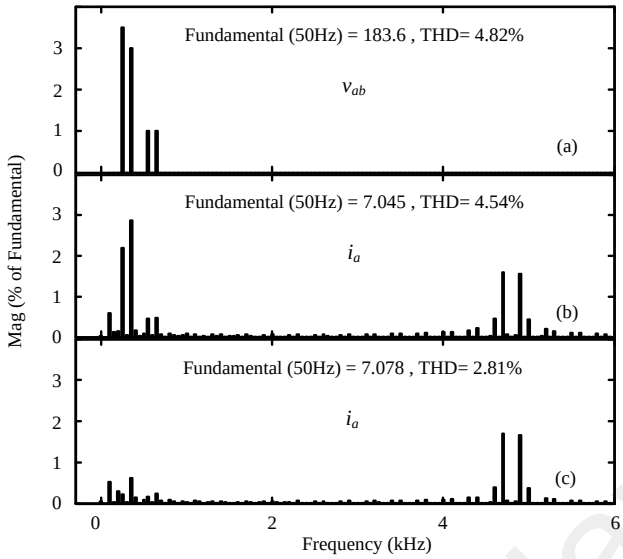



Figure 4-10: FFT of (a) distorted voltage $v_{ab}$ (b) current $i_a$ without feedforward loop (c) current $i_a$ with feedforward loop.

### 4.5.4 Transient response

In order to test the transient response of the current controller, the output current reference of the inverter was step changed from 10 A to 5 A under balanced sinusoidal grid voltage. A smooth transition performance of the inverter is demonstrated in Figure 4-11. The injected grid current follows exactly the reference current without any overshoot. The current regulator is capable of handling sudden changes in current with excellent transient performance.

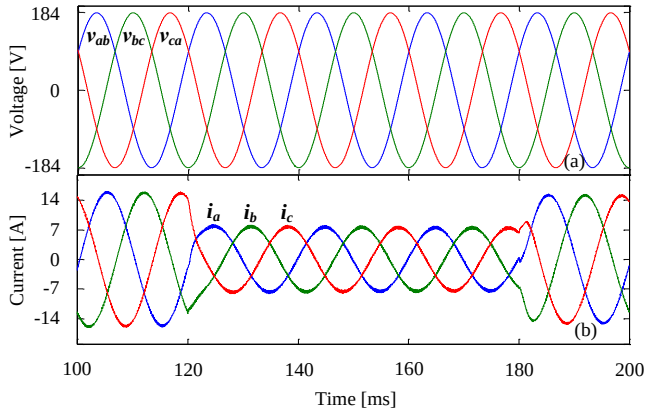



Figure 4-11: Simulation results under step changed current reference (a) grid voltage (b) grid current.

In Figure 4-12 (a), the three-phase grid voltages are stepped between 130 V and 106 V. As shown in Figure 4-12 (b) the amplitude of the injected grid currents is kept successfully unchanged with the proposed feedforward controller. . Hence the commanded reference current is accurately tracked during grid voltage transient changes. Thus, the excellent performance is provided by the proposed controller during step voltage transient.

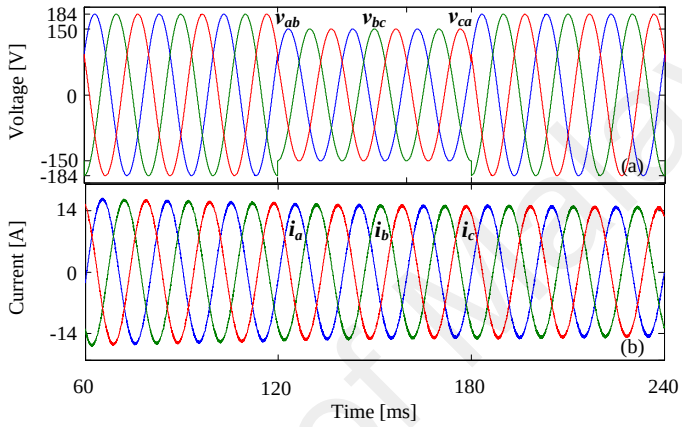



Figure 4-12: Simulation results under step changed voltage (a) grid voltage (b) grid current.

## 4.6 Summary

The IZDPWM-based feedforward controller for two level three-wire grid-connected VSIs is presented for the purpose of dealing with dynamic grid voltage disturbances. The inverter is modulated using IZDPWM that uses the line-to-line voltages as reference signals. Regardless grid topology, IZDPWM showed robustness in feedforward control of the grid-tie inverters. The proposed controller minimized low order harmonics in the grid current under weak grid condition and the current was precisely regulated. The presented control scheme was validated through simulation tests.

# CHAPTER 5: EXPERIMENTAL RESULTS AND DISCUSSIONS

## 5.1 Introduction

The obtained simulation results in chapter three and four need further verifications to better ensure the flexibility and high performance of the proposed controllers. Therefore prototypes of the inverters were developed to better confirm the compatibility of the proposed controllers on the standalone and grid-connected inverters. In following sections, the performance of the proposed IZDPWM modulator was experimentally examined. For standalone inverter, an open-loop control using IZDPWM modulator was adopted and successfully implemented. Moreover, the closed-loop IZDPWM-based feedforward controller for grid-connected inverter was implemented and desired sinusoidal currents are maintained in the grid under balanced, unbalanced, and distorted conditions.

## 5.2 The experimentation verification of the proposed IZDPWM modulator

To ensure the feasibility of the proposed modulation technique, IZDPWM was applied on a 2.4 kW three-phase, three-wire, two-level VSI. The platform used for standalone inverter is shown in Figure 5-1. The standalone inverter prototype was developed. Table 5-1 shows the specifications of the inverter and the power electronic devices. Also switching frequency is kept constant $f_s$ = 9 kHz throughout the test. Digital Signal Processor, DSP (TMS320F28335) was used to produce the switching signals for the inverter. The proposed algorithm was straightforward and simply implemented using mentioned controller, which involve a well-developed software programmable digital PWM unit (Hava & Cetin, 2011). Dead time was set to 0.2 μs for shoot-through protection. The carrier signal used in IZDPWM does not differ much from common bipolar triangular wave from the practical implementation point of view. The shifting or scaling on both carrier signal and modulating

signal has no impact on the intended switching pattern. Enhanced PWM (EPWM) module of the DSP provides unipolar carrier wave bounded to the range of 0 to 1. Therefore, both modulating signals of DPWM and IZDPWM have to be represented properly within the mentioned range.

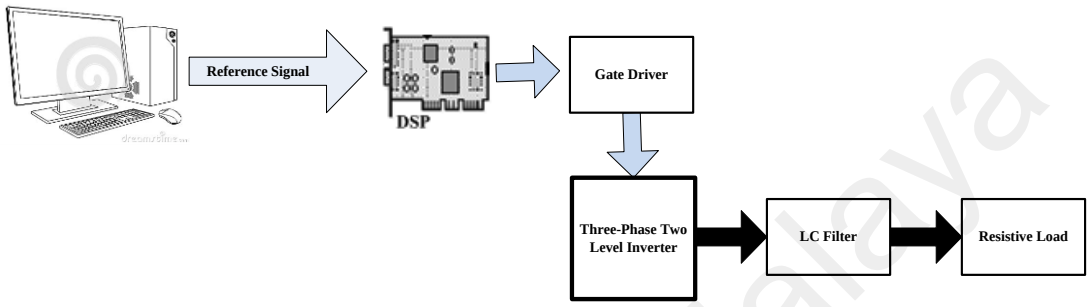



Figure 5-1: Platform for the standalone inverter.

Table 5-1: Specifications of standalone inverter prototype circuit

| | |
|---|---|
| DC Supply | TDK-Lambada 630 V, 5 A |
| IGBT | G4PH50UD 24 A, 1200 V |
| Controller | DSP, TMS320F28335 |
| $L_f$ | 1.5 mH |
| $C_f$ | 10 uF |
| Resistive Load (Y) | 2.4 kW, 380V, 61.25Ω |

### 5.2.1 Inverter output linearity range

The modulation index provided in equation (3- 15) is considered in the experimental studies. At $M_i = 1$ with an input voltage $V_{dc} = 538\,V$ the peak value of line-to-line voltage $v_{ab}$ reached up to 528.12 V. Figure 5-2 shows the line-to-line balanced voltages of the inverter load side. The linearity performance of IZDPWM0 is maintained, and it exhibited a negligible voltage drop in the power circuit at full load condition (2.4 kW). Experimental results clearly show the linearity performance of the IZDPWM0.


Figure 5-2: Standalone inverter balanced output voltages at $M_i = 1$.

### 5.2.2 Inverter output signal quality

The THD measured from the experimental setup is given in Figure 5-2. Appreciable signal quality with THD=0.242% was attained for $v_{ab}$ at $M_i$=1. As shown in Figure 3-14 (a), THD= 0.94% obtained from simulated work is not consistent with the experimentally found value. Such dissimilarity is attributed to the power analyzer's bandwidth limitation (0.0 Hz to 10.6 kHz), which prevents accurate measurement of high frequency components. The better result in terms of THD in the proposed IZDPWM is attributed to the modulating and carrier signals that were employed. As shown in Figure 5-3 different switching patterns provide the same line-to-line voltage $v_{ab}$ , which was depicted in Figure 3-15.

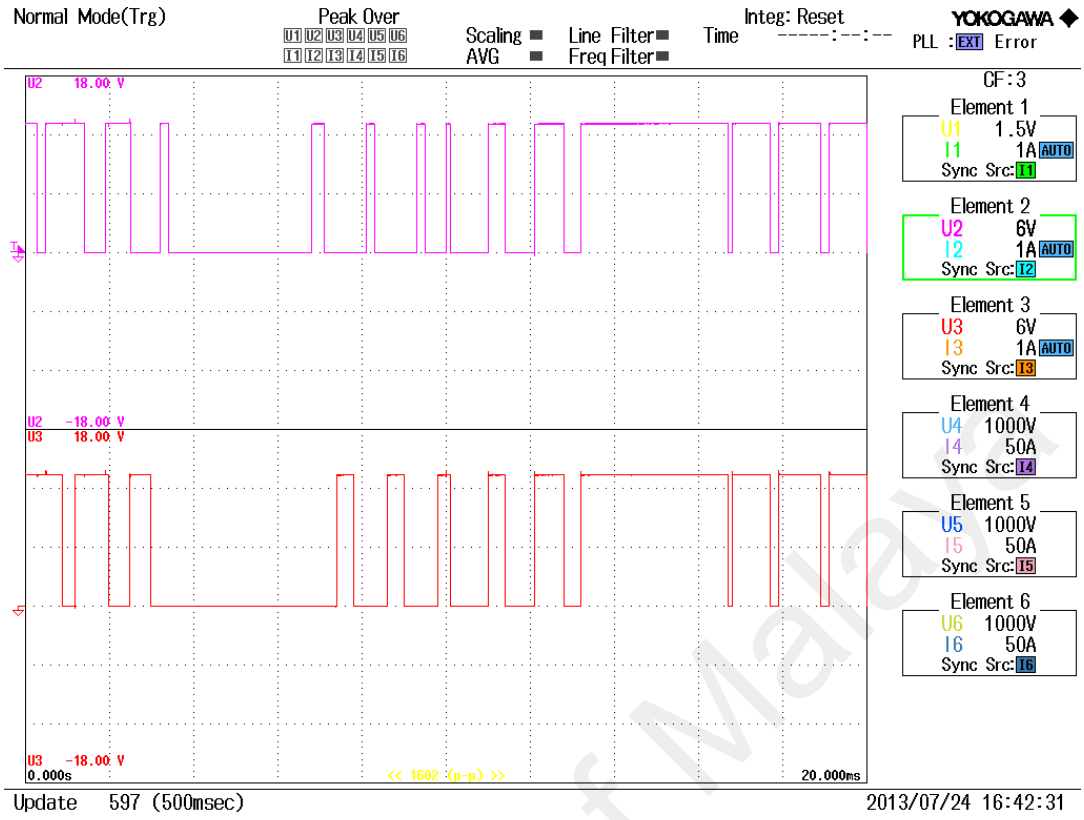



Figure 5-3: Switching patterns of $S_1$ based on DPWM0 and IZDPWM0 for same $v_{ab}$ .

### 5.2.3 Unbalanced and distorted conditions

The unbalanced three-phase line values ($v_{ab}$ , $v_{bc}$, $v_{ca}$) waveforms shown in Figure 3-16 are considered for testing IZDPWM0. The inverter was supplied with $V_{dc} = 310\ V$. Despite the sufficiently unbalanced condition, IZDPWM0 manages to linearly copy the reference signals as given in Figure 5-4. To experimentally test and ensure the performance of IZDPWM0 under a distorted condition, the distorted line-to-line reference signals are considered as given in equations (3- 16) to (3- 18) and depicted in Figure 3-18 (a). Based on the distorted reference signals of THD = 7.45% in Figure 3-18 (a), an output of THD = 7.953% is attained for $v_{ab}$ , as depicted in Figure 5-5. As shown in Figure 5-5, the harmonic components injected

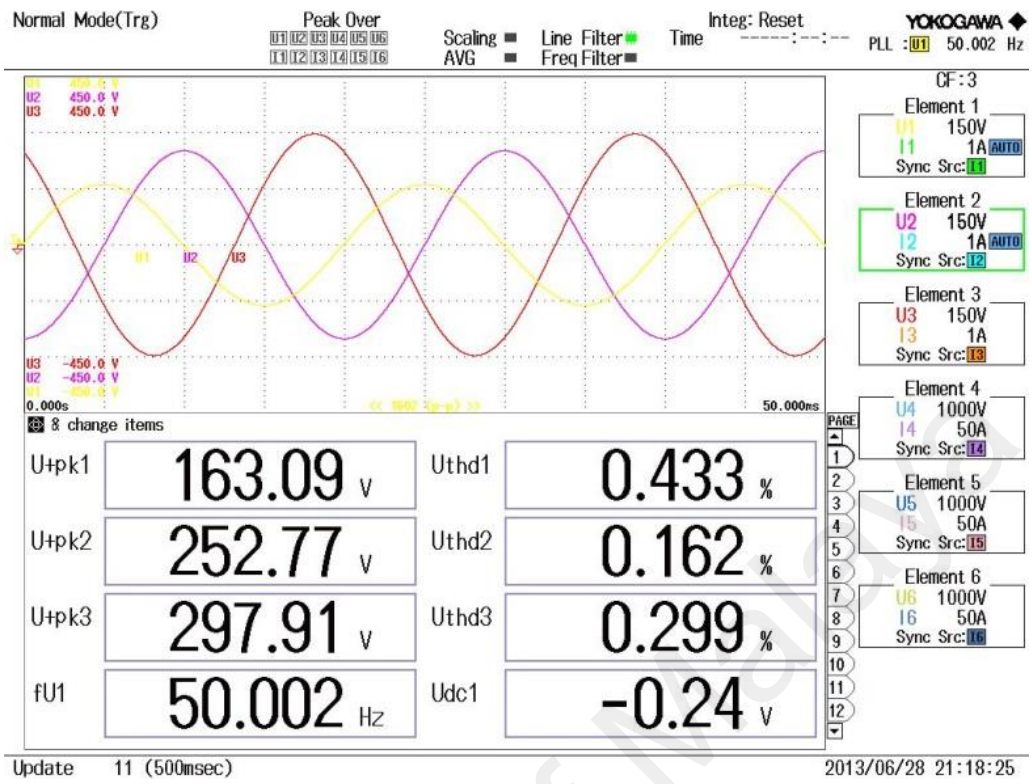



Figure 5-4: Standalone inverter unbalanced output voltages based on IZDPWM0 at $M_i = 1$.

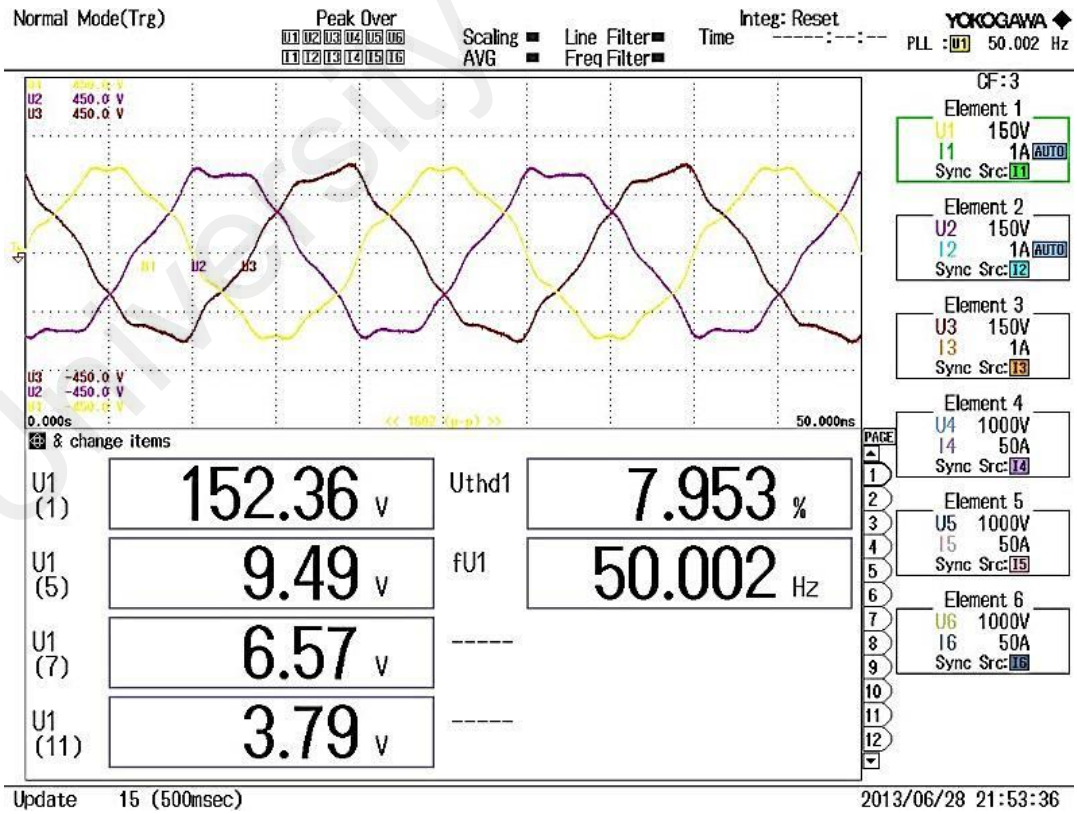



Figure 5-5: Standalone inverter distorted output voltages based on IZDPWM0 at $M_i = 1$.

into the original reference signals appear exactly in inverter line voltages. Moreover, the shapes of the outputted waveforms are consistent with the distorted reference signals depicted in Figure 3-18 (a).

### 5.2.4 Comparison of the proposed IZDPWM modulator with DPWM

DPWM and IZDPWM clamp the modulating signals to the dc-links, therefore it is possible to obtain a line-to-line output voltage that is 15% greater than that achieved when typical SPWM modulating signal is implemented. As predicted in Figure 5-2 neglecting voltage drop, the method switches the inverter to output an ac voltage of an amplitude equal to the dc supply. As a result the linearity range is significantly extended. Comparing to DPWM methods, IZDPWM improved the output profile of the inverter since it contributed in reducing the THD of output voltage specifically in the modulation range of $0 < Mi < 0.8$. Such improvement in the THD as illustrated in Figure 5-3 is attributed to the deployed modulating and carrier signals that results in different switching patterns. In Table 5-2 the proposed scalar modulator IZDPWM is compared with DPWM modulator in terms of methodology; the advantages and disadvantages are clearly addressed. In unbalanced and distorted condition both methods can be used to generate the desired output. However, in applications such as closed loop controlled grid-connected inverters, DPWM techniques may not serve in delta topology. In contrast IZDPWM can take place in either wye or delta configurations. Discontinuous switching patterns in DPWM and IZDPWM methods considerably minimize switching losses. Furthermore as depicted in Figure 3-22, IZDPWM method is more advantageous since it provides the outputs that meet the harmonic limits presented in the IEEE standards at lower switching frequency; that implies a lower power losses that leads to better efficiency.

Table 5-2: Comparison of the proposed IZDPWM with DPWM method

| Method | Methodology | Advantages | Disadvantages | Applications |
|---|---|---|---|---|
| DPWM | Appling volt-second principle using zero-sequence injection.<br>The midpoint of the dc-link is taken as modulator ground.<br>Take the phase voltages as reference signals. | Easy to implement.<br>The linearity range is increased. | The knowledge about the injected zero-sequence is a necessary.<br>Introduce higher THD at low modulation indices. | Limited to Y connected applications under balanced, unbalanced, and distorted conditions. |
| The proposed IZDPWM | Appling volt-second principle without injecting zero-sequence signal.<br>The modulator ground might be either of the dc-links (Positive and negative dc-link).<br>The line-to-line values are compared with the carrier signal. | Straightforward.<br>Lower THD is achieved.<br>The harmonic limits in the standards are met at lower switching frequency.<br>The linearity range is improved. | The method employ six different modulator grounds. | Promising technique for grid-connected applications under balanced, unbalanced, and distorted conditions.<br>IZDPWM is servable for both Y and Δ connected applications. |

## 5.3 The experimentation verification of IZDPWM-based feedforward controller

The performance of the two-level three-wire grid-connected inverter with IZDPWM-based feedforward control is experimentally verified. Hardware schematic and overall control structure of the grid-connected inverter is depicted in Figure 5-6 and the laboratory setup is depicted in Figure 5-7. The main parameters of this setup are given in Table 5-3. In order to evaluate the proposed controller a programmable ac source, Chroma 61511, is used for grid simulation under balanced unbalanced and distorted conditions. A resistive load is paralleled with the mentioned ac source since it is incapable of sinking the injected current. The inverter is controlled using dSPACE RTI1104 controller. A galvanic isolating transformer is employed for creating proper isolation between the dc power supply and the grid. Consequently, the inverter output is directly connected to the grid through the filter

inductance. It is always of interest to use a small filter in order to decrease power losses and increase overall efficiency. In the other hand the lower inductance needs to meet the grid current quality standards. However, the filter reactor size is strongly depends on the switching frequency. Switching the inverter at high frequency requires small inductance. In order to increase inverter switching frequency high-speed digital controller is needed for computation and sampling of feedback signals. A sampling frequency $f_{sam}$ = 9.6 kHz is considered to implement the advanced PLL under unbalanced and distorted grid condition. Since the delay of the proposed controller is relatively equal to the sampling period that sufficient to get all computations completed. The sampling period  is twice of the inverter swiching period for the purpose of minimizing the control delay(Qingrong & Liuchen, 2008).

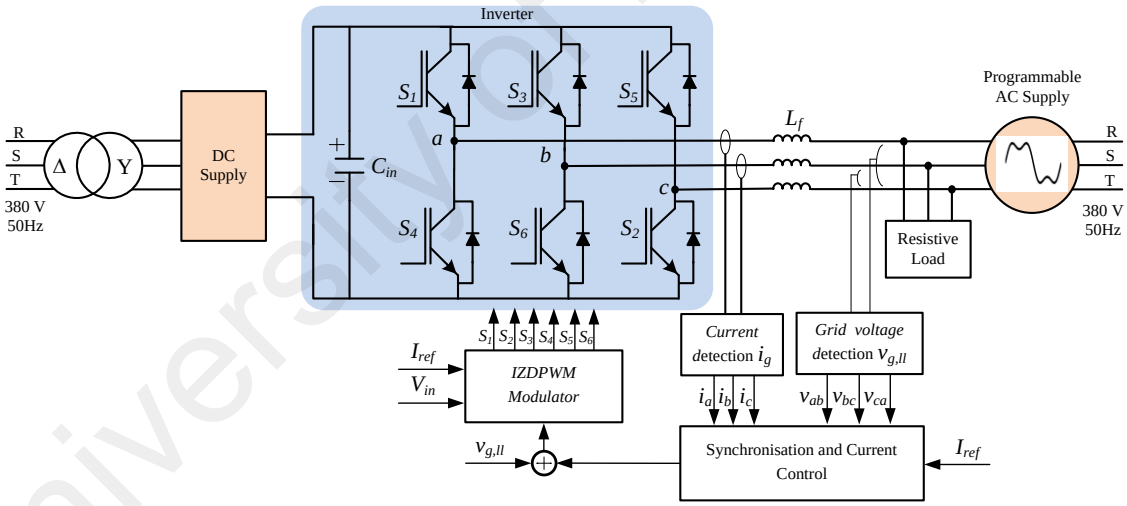



Figure 5-6: Hardware schematic and overall control structure of the grid-connected inverter.

An RC low-pass filter with the time constant of 1μs is used in the prototype to suppress the switching noise of the sampling circuits of the grid voltages. The mentioned RC low-pass filter resulted in small phase shift in the sampled grid voltage. Such phase shift does not have significant effect on the controller performance.

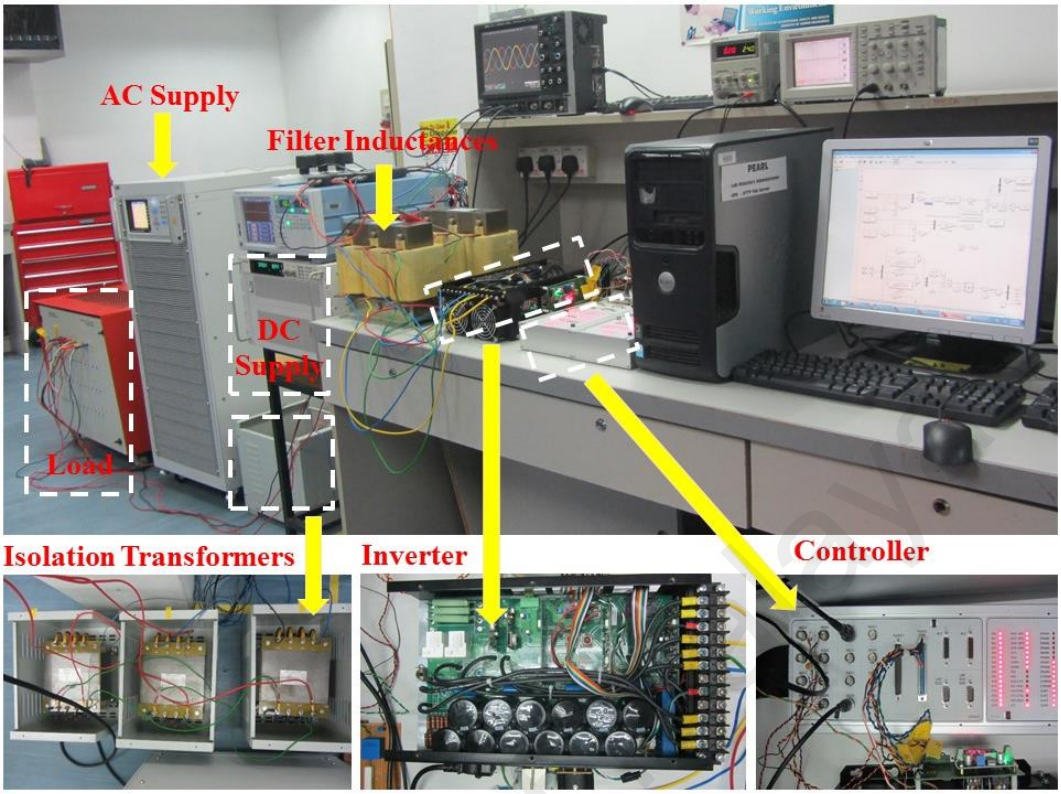



Figure 5-7: Grid-connected inverter experimental setup.

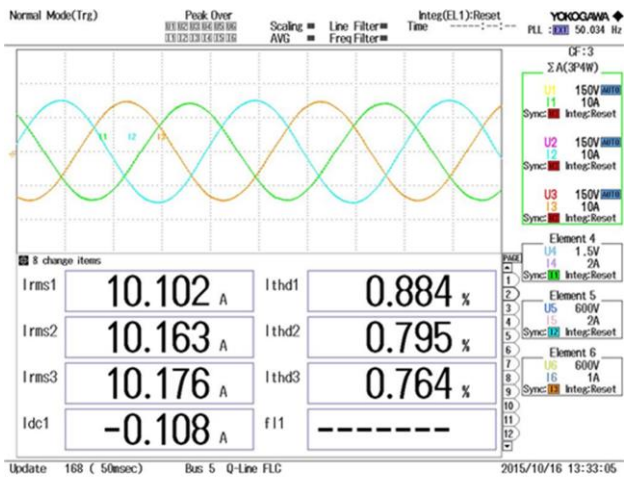
Table 5-3: Specifications of the gird-connected inverter prototype circuit

| | | |
|---|---|---|
| DC power supply | XANTREX 600 V, 20 A | |
| Isolation transformer | Δ/Y, 3*5 kVA, 380/220 V, 50Hz | |
| Programmable AC power source | Chroma 61511, 12 kVA | |
| Semikron inverter SKS 35F B6U+E1CIF+B6CI 21 V12 | IGBT | SK 60GB128 1200 V, 63 A |
| | DC-link capacitor | 2040 µF, 800 V |
| Controller | dSPACE RTI 1104 | |
| Hans von Mangoldt reactor | 10 mH, 380V, 25 A 50 Hz, 1.25 A 10 kHz | |
| Resistive load | 380 V, 50 Hz, 8 kW | |
| Sampling frequency | $f_{sam}$=9.6 kHz | |
| Switching frequency | $f_{sw}$=4.8 kHz | |

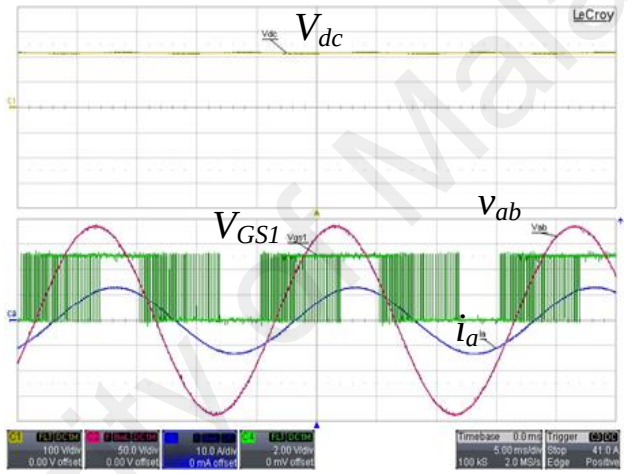
In translating the PI controller $G\ (s) = 20 + \frac{200}{s}$ to the *z*-domain, we put $s = (1 - z^{-1})/T_{sam}$ to obtain the backward difference equation for the PI controller gain.

### 5.3.1 Sinusoidal grid voltage

In sinusoidal and balanced grid voltage condition $I_{ref}$ was set to 10A at full power condition (2.25 kW). Figure 5-8 provides the experimental results under IZDPWM-based feedforward control. Figure 5-8 (a) depicts the injected current waveforms. The attained THD of injected current $i_a$ =10.102 A is 0.88%. Figure 5-8 (b) shows the input dc voltage, current of leg 'a', and switching patterns of $S_1$. The input dc voltage $V_{dc}$=220 is well regulated; and less than 2 V ripple measured. Such stiff dc performance is attributed to the 2040 µF capacitor paralleled with the high power dc source (12 kW). Moreover, the control strategy precisely regulates the active power to 2.25 kW and the reactive power to 0 kVA as desired. The measured phase shift between current $i_a$ and line-to-line voltage $v_{ab}$is 29.9° . Considering 30° phase shift between phase and line voltages the phase shift between injected current and grid phase voltage is $\Phi$ =0.1° and the power factor of cos$\Phi$=0.999 was obtained. As shown Figure 5-8 (b) the proposed method successfully clamps the switches of leg 'a' at maximum current. Accordingly, switch $S_1$ is kept ON and OFF for 2*60° centred on the $i_a$ positive and negative peaks, respectively. It can be observed that the proposed IZDPWM-based methods work quite well under balanced and sinusoidal grid voltage condition.




(a)



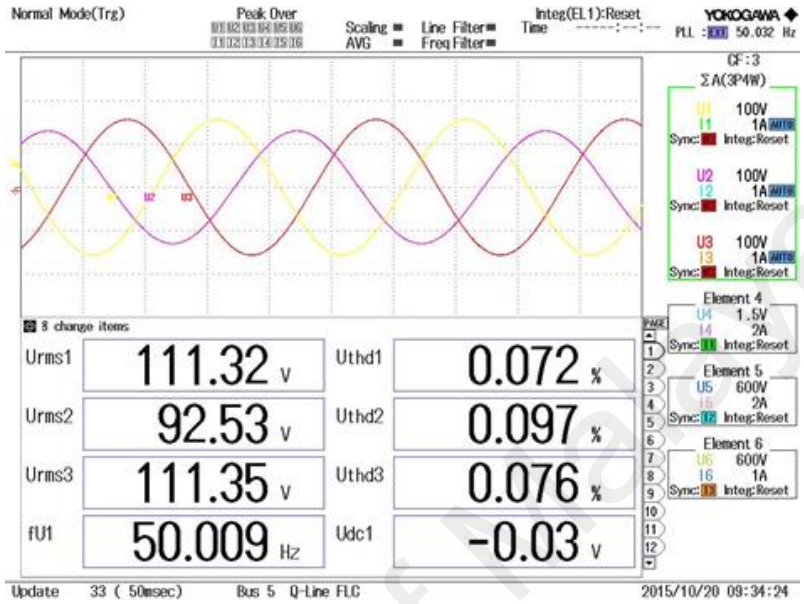

(b)

Figure 5-8: Experimental results under sinusoidal condition (a) grid current (b) Input dc voltage, $v_{ab}$, $i_a$and switching patterns of $S_1$.

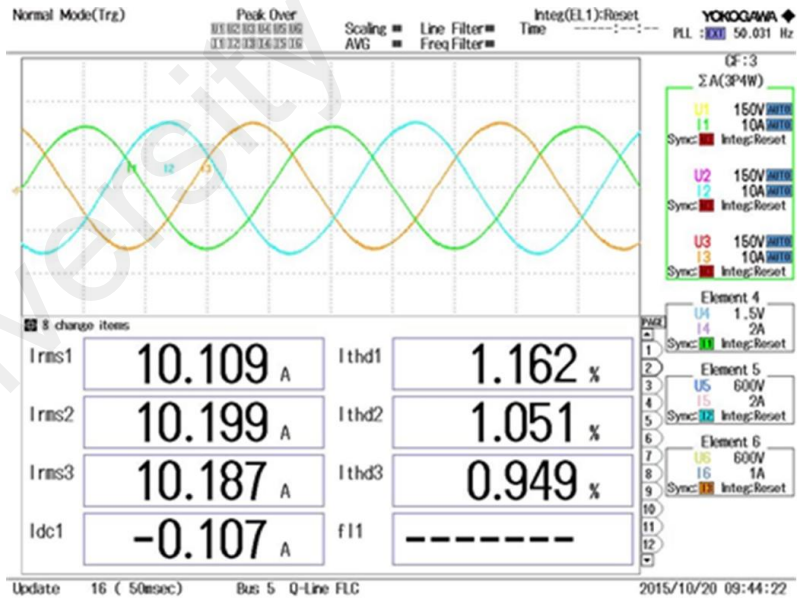
### 5.3.2 Unbalanced grid voltage

The proposed control scheme is investigated under unbalanced grid voltage condition. The grid voltage in such a circumstance is generated using both positive and negative- sequences. Thus, using the programmable ac source the three-phase grid voltages are derived based on the equations (4- 7) to (4- 9). The grid voltage and current waveforms are depicted in Figure 5-9. The reference positive-sequence injected grid current is 10.109 A, and the

negative-sequence current reference is 0 A. As depicted in Figure 5-9 despite remarkable unbalanced




(a)




(b)

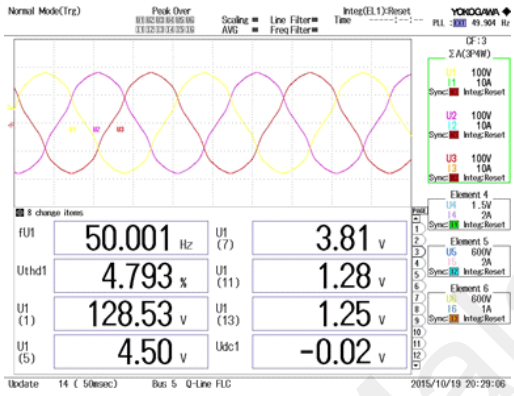
Figure 5-9: Experimental results under unbalanced condition (a) grid voltage (b) grid current.

grid voltage the injected three phase current is balanced and the measured phase shift between current and positive-sequence of grid voltage are -31.5° ,-31.3° , and -31.5° respectively. Considering -30° phase shift among phase currents and line-to-line voltages, the PLL precisely synchronized the injected current with the positive-sequence of the grid voltage. Therefore, the proposed IZDPWM-based feedforward scheme successfully regulated the injected grid current under unbalanced grid voltage condition.

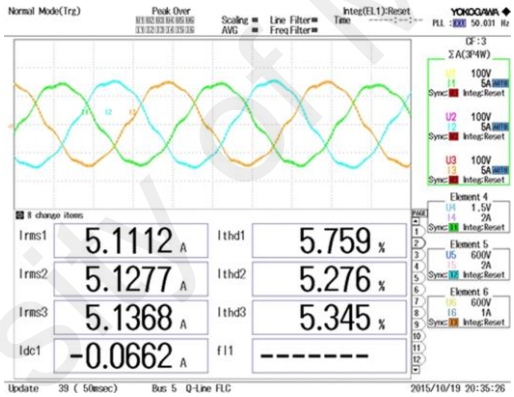
### 5.3.3 Distorted grid voltage

In order to demonstrate the performance of the proposed controller under distorted grid condition, experiments have been conducted with the consideration of grid line-to-line voltage feedforward control loop; and other tests disregard the mentioned loop (grid line-to-line voltage). The grid voltages were distorted by 5th, 7th, 11th, and 13th harmonics. These harmonics are 3.5%, 3%, 1%, and 1% of the fundamental component voltage (130) respectively. The presence of the mentioned harmonics makes the THD of the grid voltage 4.82%. Thus, IEEE 519-1992 harmonic restriction standard is fulfilled ("IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems," 1993). The grid voltage and current waveforms are depicted in Figure 5-10. Throughout the test under distorted grid voltage the desired inverter output current is set to $I_{ref}$ =5 A (1.125 kW). In Figure 5-10 (b) the current and voltage waveforms are taken when the feedforward loop is disregarded in controller. The THD of the injected current goes beyond the THD standard limit 5%. As depicted in Figure 5-10(c) feeding the line-to-line values to the control loop decreased the THD of the grid current $i_a$ from 5.76 % to 3.08 %. Moreover, low order harmonics of magnitudes 2.24%, 2.96%, 0.45%, and 0.52% with respect to the fundamental component appeared in grid current $i_a$ due the absence of the grid voltage loop in proposed current controller. The proposed scheme effectively suppresses current

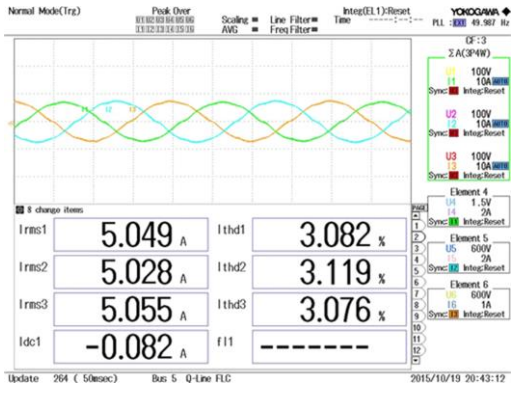
distortion caused by the grid voltage low order harmonics since the low order current harmonics, of magnitudes 0.25%, 0.62%, 0.15%, and 0.22% respectively are attenuated. Hence the effectiveness of the presented feedforward control is clearly addressed.




(a)




(b)




(c)

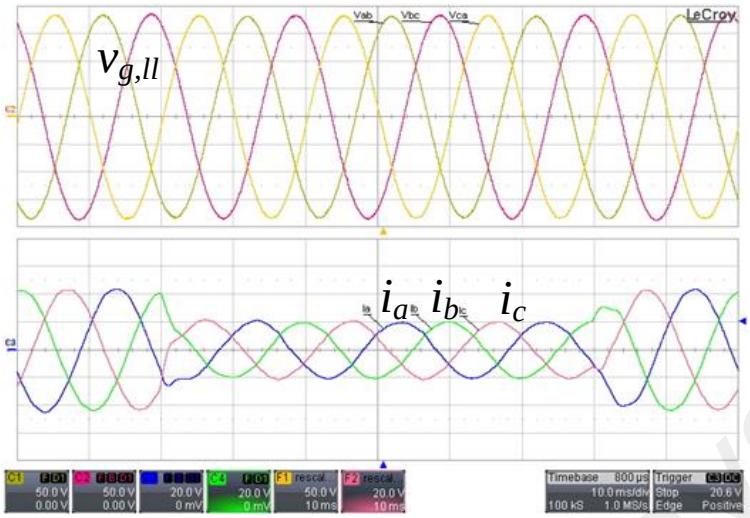
Figure 5-10: Experimental results under distorted condition (a) grid voltage (b) grid current without feedforward loop (c) grid current with feedforward loop.

### 5.3.4 Transient response

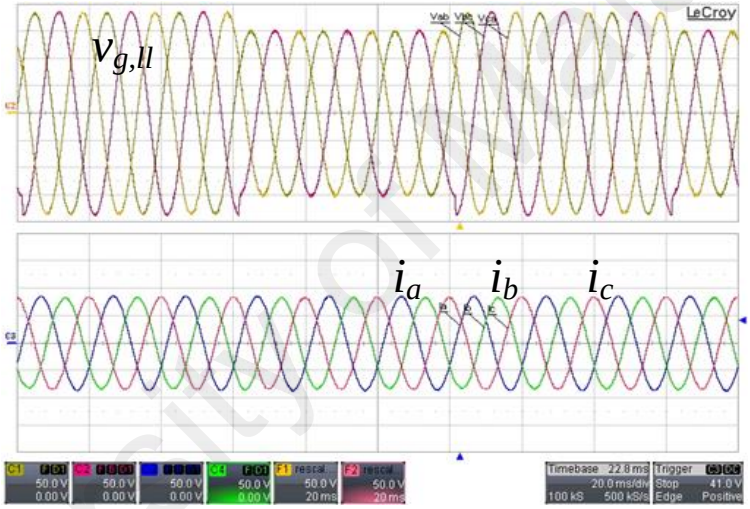
In order to test the dynamic response of the current controller, the output current reference of the inverter was step changed from 10 A to 5 A. The dynamic test was done under balanced sinusoidal grid condition. A smooth transition performance of the inverter current is demonstrated in Figure 5-11(a). The injected grid current follows exactly the reference current without any overshoot. The current regulator is capable of handling sudden changes in current with excellent transient performance. In Figure 5-11(b) the three-phase grid line-to-line voltages are stepped between 130 V and 106 V while the grid current reference kept constant with the value of 10 A. As can be seen the injected grid currents is kept unchanged. Hence the commanded reference current is accurately tracked during grid voltage transient changes. Thus, the excellent performance is provided by the proposed controller during step voltage transient.

### 5.3.5 Comparison of the simulation results with experimental results

In Table 5-4 the simulation results are compared with experimental results under sinusoidal, unbalanced, and distorted grid condition. As can be seen the experimental results correspond precisely to the results attained from the simulation in all the grid conditions. It worth mentioning that simulation results were achieved based on ideal switches with no dead time whereas in experimental tests dead time automatically was set in range of 1.8 μs to 4.5 μs by the Semikron inverter for shoot-through protection. Considering the inverter low swithing frequency $T_{sw}$=208 μs nonzero dead time causes subtle differences among the results. As shown in Figure 5-11, Figure 4-11, and Figure 4-12, the experimental results of transient responses are consistent with the simulation results.




(a)




(b)

Figure 5-11: Experimental results under step changed of (a) grid current (b) grid voltage.

Table 5-4: IZDPWM-based feedforward control simulation and experimental results

| Grid Voltage Condition | The injected current $i_a$ | | | | | |
|---|---|---|---|---|---|---|
| | Amplitude (A) | | THD (%) | | Phase Shift ($\Phi$°) | |
| | Simulation | Experimental | Simulation | Experimental | Simulation | Experimental |
| Sinusoidal | 14.13 | 14.28 | 1.46 | 0.884 | 0.1 | 0.1 |
| Unbalanced | 14.04 | 14.29 | 1.47 | 1.162 | 0.5 | 0.2 |
| Distorted | 7.078 | 7.14 | 2.81 | 3.082 | 0.0 | 0.1 |

## 5.4 Comparison of the grid-connected inverter current control methods

In Table 5-5 a comprehensive comparison on the grid-connected inverter current control methods under weak grid condition are provided. The advantages and disadvantages of the proposed IZDPWM-based feedforward controller, multiple PR (Fukuda & Imamura, 2005; Liserre et al., 2006a, 2006c), PWM-based feedforward (Li et al., 2013; Wang et al., 2010), and predictive current controllers (Mohamed & El-Saadany, 2007; Qingrong & Liuchen, 2008) are clearly addressed.

Table 5-5: Grid-connected inverters current control methods under weak grid condition

| Controller | Inverter Modulator | Advantages | Disadvantages |
|---|---|---|---|
| Multiple PR | PWM | Easy to implement.<br>Preset low-order grid voltage harmonics are suppressed effectively. | Possible instability in wide band of distortion cancellations.<br>Difficult tuning process.<br>Three voltage sensors are required. |
| Grid phase voltage feedforward controller | PWM | Straightforward.<br>Easy tuning process.<br>Reject dynamic voltage disturbances in wide range of low frequency harmonics. | Three voltage sensors are required.<br>Applicable only in wye topology. |
| Predictive current controller | SVPWM | High quality current control and fast dynamic response. | Much more complicate implementation.<br>Advanced controller is required to decrease control delay due to high computation.<br>High sensitivity to system parameters.<br>Three voltage sensors are required. |
| The proposed grid line-to-line voltage feedforward controller | IZDPWM | Easy to implement.<br>Improved inverter efficiency with 33% less switching losses.<br>Reject even non periodic voltage disturbances.<br>Just two voltage sensors are required.<br>Applicable in wye and delta topology. | Implementation of an advanced PLL under unbalanced and distorted grid voltage condition increases the control delay. |

## 5.5 Summary

The experimental testing results of the presented IZDPWM modulation technique and IZDPWM-based feedforward control have been presented. Besides the provided simulation results, as open-loop modulator IZDPWM was successfully implemented and stable output is noted. The implemented IZDPWM-based feedforward controller force the grid currents to follow the references under balanced, unbalanced, and distorted conditions. Hence outstanding current regulation was guaranteed in a wide range of grid conditions and fast dynamic response was achieved during voltage and current step changes. Appling IZDPWM, the switching losses are decreased, and better efficiency was obtained. The current controller performance was evaluated by the output current THD and power factor. Transient response of the proposed current controller is verified and good stability and fast transient response are achieved. Since the line-to-line voltages were considered in the implemented modulator, the measurement of distorted grid voltages needs only two sensors. Hence, high reliability control is achieved with decreased overall system cost. The experimental results have clearly shown the compatibility of IZDPWM in two-level three-phase inverter control.

# CHAPTER 6: CONCLUSION AND RECOMMENDATIONS

This chapter contains the conclusions and the possible future works for the thesis.

## 6.1 Conclusion

In this thesis, the problem of grid-connected inverter control under weak grid condition was introduced. A complete survey of the inverter-based DG system topology and control were performed. The research includes a complete description of the proposed modulator, computer simulation, and laboratory measurement verification. DG inverters are connected to the power grid that may experience any unbalanced or distorted voltage at the point of common coupling. The non-sinusoidal profile of the grid voltage waveform has adverse effects on the injected current. The controller of the grid-connected inverters have to tackle this problem and ensure high-quality current in weak grid conditions. The low pass filters do not serve well against the grid voltage low-order harmonics and they are not naturally attenuated. Therefore, a controller that further assist in mitigating the injected current harmonics under weak grid condition is a prominent aspect of the inverter control. Feedforward controller tackles even the non-periodic grid voltage disturbances without further harmonic analysis. However, the implementation of feedforward controller based on typical scalar PWM method impose some disadvantages. First, output linearity range is limited; and the input dc source is not used in optimized manner. Second, feedforward loop in weak grid condition necessitates three sensors for phase voltage measurement. Third, feedforward control is not applicable in delta topology due to the inaccessible phase voltages. In other words under weak grid condition, online conversion of line-to-line values into phase values is a crucial task. In the other hand scalar DPWM based controllers for the grid-

connected inverters are not established. It is remarkable advantageous to apply DPWM method which reduces the switching losses and increases the utilization of dc supply compared with conventional continuous SPWM scheme. DPWM methods can be realized using the SVPWM approach by eliminating one from the redundant zero vectors in the switching state sequence, however, scalar DPWM method is quite straightforward to implement than SVPWM-based discontinuous technique. These problems are the main motivation for the work in this thesis.

In all, development of a new scalar implicit zero-sequence discontinuous PWM for two-level, three-wire voltage source inverters is the crucial contribution of this study. IZDPWM is the first scalar PWM method that directly uses line-to-line voltages as reference signals instead of phase voltages. Therefore by considering the line values, IZDPWM is implemented differently from all existing scalar PWM methods that take the phase values as reference signals. The injection of zero-sequence is necessitated in advanced scalar PWM methods for the sake of extending the inverter output voltage control linearity range, improving the waveform quality, decreasing the switching losses. The mentioned merits are realized in IZDPWM with no zero-sequence signals injected in the reference line-to-line voltages. Consequently, IZDPWM-based feedforward controller for two level three-wire grid-connected VSIs is presented for the purpose of dealing with dynamic grid voltage disturbances.

Regardless grid topology, the proposed controller was successfully implemented on three-phase, three-wire two-level grid-connected voltage source inverter. Moreover, the proposed scheme gave an appreciable output in balanced, unbalanced and distorted conditions which might be experienced in many applications. The presented control scheme was validated through simulation and experimental tests. The proposed IZDPWM-based

feedforward control under full power condition (2.25 kW) results in high quality injected current with low THD (0.888 %) and high power factor (0.999). Since the line-to-line voltages were considered in the implemented modulator, the measurement of distorted grid voltages needs only two sensors. Hence, high reliability control is achieved with decreased overall system cost.

## 6.2 Future work and Recommendations

Although the developed control methods meet the study objectives, several issues require further investigation. The suggested future works with some recommendations are summarized in the following points.

- The proposed topology involve dc power supply, therefore, there is the possibility to replace the dc power supply with renewable energy devices such as photovoltaic or fuel-cell.
- Despite the appreciable simulation and experimental results attained using IZDPWM-based current regulators for L type grid-connected inverters, it is more attractive to develop similar controller for LCL type inverters.
- Both open-loop and closed-loop controller were successfully applied on the grid-connected VSIs. And high flexibility of the proposed modulator is demonstrated through the achieved simulation and experimental results. Thus the feasibility of the modulator was accurately noted. The aforesaid merits are sufficient to promote the proposed modulator to take part in other applications such as active power filters.

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## LIST OF PUBLICATIONS

### ISI Journals

A. Shayestehfard, S. Mekhilef, H. Mokhlis, " Modified Scalar DPWM Method for Two-level Three-wire Voltage Source Inverters under Unbalanced and Distorted Conditions," IET Power Electronics, vol. 6, pp. 1696-1706, 2013.

A. Shayestehfard, S. Mekhilef, H. B. Mokhlis, H. Belkamel,"IZDPWM-Based Feedforward Controller for Grid-Connected Inverters under Unbalanced and Distorted Condition," Accepted in IEEE Transaction on Industrial Electronics.

### Conferences

A. Shayestehfard, H. Belkamel, S. Mekhilef, H. B. Mokhlis, M. Nakaoka, and K. Ogura, "Feedforward of grid line-to-line voltages for grid-connected inverter under the weak grid condition," in *9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, 2015, pp. 150-156.