INTEGRAL-DERIVATIVE (I-D) AND MODULATION-INDEX-CURVE PREDICTION CONTROL TECHNIQUES FOR THREE-PHASE AC-DC BUCK-TYPE CONVERTER WITH SIMPLIFIED VOLTAGE-BASED SPWM

AZRITA BINTI ALIAS

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ABSTRACT

This thesis presents the design of a three-phase AC-DC buck-type converter with bidirectional capability using simplified voltage-based sinusoidal pulse-width-modulation (SPWM) switching technique. With its four diodes connected to the switch enable bidirectional power flow in each switch. The proposed topology is an extension of the conventional 6-switch three-phase AC-DC buck-type converter whereas the proposed switching technique is a simplification of conventional modified SPWM technique. It uses one reference signals (0-60° sine wave) and one type carrier signal, instead of two reference signals and two types of carrier signals to generate PWM signals. The proposed circuit configuration produces sinusoidal AC current with low THD at near unity power factor using simplified voltage-based SPWM. Voltage feedback control allows high dynamic performance of the DC output voltage in the step-changing of reference and disturbance. Two digital feedback voltage controls, Integral-Derivative (I-D) and modulation-index-curve prediction techniques, are suggested to equalize the output voltage to the reference voltage with high dynamic performance and simpler implementation. The algorithm of the modulation-index-curve prediction technique is obtained through I-D control model by determining closed-loop dominant poles. By assuming zero system loss, a small steady-state error is still present (absent in the I-D controller). Modulation-index-curve-prediction technique is still advantageous because it reduces dependence on feedback-sensor reading and simplifies the I-D algorithms. The converter's validity, PWM switching strategy, and feedback control strategy have been verified by simulation using MATLAB/Simulink. The hardware prototype has been implemented in a TMS320F28335 Digital Signal Processor (DSP) and the results are validated.

ABSTRAK

Tesis ini menerangkan reka bentuk penukar rendah tiga fasa AU-AT dwiarah menggunakan teknik pensuisan ubahsuai pemodulatan lebar denyut sinusoidal (PLDS) berasaskan voltan. Dengan empat diodnya yang disambungkan pada suis membolehkan pengaliran kuasa dwihala dalam setiap suis. Topologi penukar yang diusulkan ini merupakan unjuran daripada penukar AC-DC tiga fasa enam suis di mana teknik pensuisannya dipermudahkan daripada teknik konvensional PLDS terubahsuai. Teknik yang dimaksudkan menjana isyarat PWM dengan menggunakan satu isyarat rujukan (gelombang sin 0-60°) dan satu jenis isyarat pembawa sebagai ganti dua isyarat rujukan dan dua jenis isyarat pembawa berbanding strategi sebelumnya yang menggunakan dua isyarat rujukan dan dua jenis isyarat pembawa bagi menghasilkan isyarat PLD. Konfigurasi litar yang dicadangkan menghasilkan arus sinusoidal AU dengan THD yang rendah pada faktor kuasa uniti menggunakan ubahsuai PLDS berasaskan voltan. Pengawalan suap balik voltan meninggikan prestasi dinamik voltan keluaran DC meskipun terdapat pertukaran langkah isyarat rujukan dan isyarat gangguan. Dua pengawal digital suapbalik, pengawal Kamiran-Derivatif (K-D) dan teknik ramalan lengkung indeks modulasi, dicadangkan bagi menyetarakan voltan keluaran dengan voltan rujukan dengan prestasi dinamik yang tinggi dan juga menggunakan implementasi yang lebih mudah. Algoritma ramalan lengkung indeks modulasi diperolehi melalui model pengawal K-D menggunakan kedudukan kutub-kutub dominan gelung tutup. Dengan anggapan tiada kehilangan dalam sistem, ia menyebabkan sedikit ralat keadaan mantap wujud (tiada dalam pengawal K-D). Teknik ramalan lengkung modulasi indeks mempunyai kelebihan kerana ia mengurangkan kebergantungan pada pengesan voltan suapbalik dan meringkaskan algoritma pengawal K-D. Keberkesanan penukar, teknik pensuisan PLD dan strategi kawalan suapbalik

disahkah melalui simulasi menggunakan MATLAB/SIMULINK. Perkakasan prototaip telah direalisasi dalam Pemproses Isyarat Digital (PID) TMS320F28335 dan keputusannya disahkan.

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LIST OF SYMBOLS AND ABBREVIATIONS

Symbols

B	manipulated signal
C_d	output filter capacitor at DC side
C_f	input filter capacitor at AC side
c	constant value
D	disturbance signal
E	error signal
e_{ss}	steady-state error
f_1	fundamental frequency
f_s	switching frequency
$G_p(s)$	plant's transfer function
$G_{C1}(s)$	controller's transfer function (outer loop)
$G_{C2}(s)$	controller's transfer function (inner loop)
G_{YR}	closed-loop transfer functions subjected to the reference input
G_{YD}	closed-loop transfer functions subjected to the disturbance input
I_a	phase A AC current
I_b	phase B AC current
I_c	phase C AC current
I_L	inductor current at DC side
I_{load}	load current at DC side
I_m	maximum/peak current
K_I	integral gain
K_P	proportional gain
K_D	derivative gain
K_1	coefficient values

K_2	coefficient values
K_3	coefficient values
k	the discrete-time index (k= 1, 2, 3….).
L	inductance
L_d	output filter inductor at DC side
L_f	input filter inductor at AC side
M	modulation index
$n1$	number of sample
n_3	number of sinewave sample at 120°
Op-k	the *k*th output of the (*p*-1)th layer
P	maximum value of the sinewave signal
PRD	maximum value of counter
p	pole
R	resistance
R	reference signal
S1-S7	switch of power converter
T	switching period
T_s	settling time
T_r	rise time
$1/T_D$	zero's location of I-D controller
t	time in seconds
t_{on}	switching transition from low to high
t_{off}	switching frequency from high to low
U_1	the output signal of the controller $G_{C1}(s)$
U_2	the output signal of $G_{C2}(s)$
V_{DC}	direct current voltage

V_{in}	input voltage
V_m	maximum voltage/peak voltage
V_{ref}	reference voltage
V_o	output DC voltage
$V_{L\text{-}N}$	line-to-neutral voltage
V_B	bridge voltage
V_a	phase voltage A line-to-neutral voltage
V_b	phase voltage B line-to-neutral voltage
V_c	phase voltage C line-to-neutral voltage
V_{ab}	line-to-line voltage (between phases A and B)
V_{cb}	line-to-line voltage (between phases C and B)
$w_{p,i,k}$	the weight of the *k*th input of the (*p*-1)th layer
Y	output signal
z	zero
ZRO	minimum value of counter
ϕ	displacement factor
ξ	damping ratio
ω_n	natural frequency
$\theta_{p,i}$	the bias
Δt	the change in sampling time
ΔV_{ref}	step-size of reference voltage
$\sigma 1$	location of the dominant pole
$\sigma 2$	location of the dominant pole
%OS	Overshoot percentage

Abbreviations

AC	Alternating current
ADC	analog-to-digital converter
ASD	adjustable speed drive
BJT	bipolar junction transistor
BLDC	brushless direct current
CPU	computer personal unit
CSR	current source rectifier
DC	direct current
DCM	discontinuous current mode
DIP	dual-in-line-package
DSP	digital signal processor
DPC	direct power control
EMI	electromagnetic interference
ESR	equivalent series resistance
ePWM	enhanced pulse-width-modulation
FLC	fuzzy logic controller
FPGA	field-programmable gate array
GPIO	general pin input/output
GTO	gate turn-off
HVDC	high voltage direct current
I-D	integral-derivative
IGBT	insulated gate bipolar transistor
LC	inductance-capacitance
MOSFET	metal oxide semiconductor field effect transistor

MSPWM	modified sinusoidal pulse-width-modulation
NLC	nonlinear-carrier
NN	neural network
OS	overshoot
PCC	predictive-current-control
PFC	power factor correction
PI	proportional-integral
PD	proportional-derivative
PID	proportional-integral-derivative
PLL	phase-locked loop
PWM	pulse-width-modulation
RC	resistance-capacitance
rms	root mean square
SISO	single-input-single-output
SMC	sliding mode control
SPWM	sinusoidal pulse-width-modulation
SVM	space vector modulation
THD	total harmonic distortion
UPS	uninterruptible power supplies
VSC	voltage source converter
VSS	variable structure system
XNOR	exclusive NOR
ZCD	zero-crossing detector

CHAPTER 1

INTRODUCTION

1.1 Background

Metal oxide semiconductor field effect transistors (MOSFET), insulated gate bipolar transistor IGBT, and gate turn-off GTO have been used to replace conventional diode rectifiers in switch-mode three-phase AC-DC rectifier configurations to overcome problems such as non-sinusoidal wave of the ac mains supply, low power factor, and uncontrollable DC voltage. A buck-type switch-mode three-phase rectifier enables step-down voltage conversion. Used in power supplies of telecommunication systems and process technologies, its recent topology incorporated a boost-type output stage to enhance power conversion (Ortiz-Lopez, Leyva-Ramos, Carbajal-Gurtierrez, & Morales-Saldana, 2008; Raihan & Rahim, 2013; Yang, Liang, & Chen, 2008). Some buck-type rectifiers (i.e., current source rectifier) can be classified as bidirectional converters. They can regenerate power in two directions: AC-DC and DC-AC. The concept of reversible direction of power flow of one polarity can be realized only by adding an anti-parallel switch to the diodes (Green, Taha, Rahim, & Williams, 1997; Kolar & Friedli, 2013), or through bidirectional diodes (four diodes), which achieve bidirectional flow (Yang, Liang, & Chen, 2006). Bidirectional-type converters are suitably used in adjustable speed drives (ASDs)) (J. Rodríguez, Morán, Pontt, Osorio, & Kouro, 2003; Zargari et al., 2001) and battery charging of uninterruptible power supplies (UPSs) (Green et al., 1997).

Various modulation switching techniques such as pulse-width-modulation (PWM), predictive control, hysteresis, and space vector have been designed for switch-mode buck-type three-phase rectifier to obtain an almost sinusoidal AC input current and near-unity input power factor. The techniques usually use a high switching frequency to reduce ripple current and minimize filter size. Microprocessors (i.e., DSP) and FPGA allow the use of a high sampling rate in digitally-controlled power converters. The use of DSP has been investigated to control power converter's switching power supply (Daigavane, Suryawanshi, & Khan, 2007; Ellabban, Mierlo, & Lataire, 2011; Malinowski, Jasin, & Kazmierkowski, 2004; Mansor & Rahim, 2011; Zhang, Feng, Liu, & Wu, 2004, 2006). Switching control mostly requires current-feedback (current sensors and ADC) when generating pulses, to improve the waveshape and power factor of the ac input current. The use of current sensors can be avoided if an appropriate modulation strategy is adopted (A. Alesina & Venturini, 1989; Alberto Alesina & Venturini, 1981; Holmes & Lipo, 1992; Milanovic & Dobaj, 2000). Among the advantages of no current sensor is shorter A/D conversion time and shorter overall calculation time (Hwu, Chen, & Yau, 2012; Raihan & Rahim, 2010). Three-phase AC-DC power converter configurations with various switching techniques that improve power quality have been reviewed by J. R. Rodríguez et al. (2005) and Singh et al. (2004).

A modified sinusoidal PWM (SPWM) switching scheme is one of the current sensorless techniques that have been used in three-phase AC-DC rectifiers. Green et al. (1997), Omar & Rahim (2003), Rahim et al. (2010) and Raihan & Rahim (2013) used it in unidirectional AC-DC three-phase buck converter of 3-switch 12-diode configuration. It functions as excellently when integrated with Flyback (Omar & Rahim, 2003) and Sepic (Raihan & Rahim, 2013, 2010) converters. The studies prove that modified SPWM produces high-quality AC-current waveform, near-unity power factor, and system stability. They also show that DC output voltage can be controlled by modulation gain.

Without a voltage feedback control strategy, however, large starting current and voltage (during transient) could result from large step-changes to the reference voltage, owing to the DC-side LC filter. In practice, significant voltage drop is caused when the modulation gain changes by theoretical calculation. The drop is likely caused by load changes due to losses in non-ideal converter elements, insulated-gate bipolar transistors (IGBT), and diodes (Milanovic & Slibar, 2011).

One common example of voltage feedback controller is Proportional-Integral (PI). PI controller exhibits excellent small-signal transient response (i.e., a disturbance that varies in close proximity to the operating point), but is unsuitable in systems subjected to large-signal disturbances and uncertainties. The other most popular voltage control is proportional-integral-derivative (PID) controller. PID is implemented in many industrial applications (power converters, motor control, hybrid electric vehicle, etc.) for its well-known simplicity and robustness. A satisfactory performance can be achieved in many linear or nonlinear systems by proper tuning of PID controller's parameters/gains (proportional gain (K_P), integral gain (K_I) and derivative gain (K_D)).

In practice, a basic PID control system produces a set-point-kick phenomenon especially when the reference input is a step function (Rashid, 2004). Modified PID such as PI-D or I-D is preferred to avoid the phenomenon; the derivative action is placed in a minor loop around the plant instead of in the forward path. Such controllers are categorized as single-degree-of-freedom PID control; they cannot respond to more than one requirement. A two-degrees-of-freedom configuration responds to two independent requirements (disturbance input and reference input). A formulation of PID control is recently investigated for PID control in DC-DC converter to improve dynamic performance in transient response. A formula for PID control based on capacitor current in geometric terms has been proposed in Kapat & Krein (2012). Saggini, Mattavelli, Ghioni, & Redaelli (2008) explored a digital PID control based on mixed-signal

voltage-mode control in a DC-DC converter. These techniques improve conventional PID control's transient performance.

1.2 Problem Statement

Theoretically, conventional modified SPWM technique uses a look-up table of sixty degree (60°) sine wave as reference signal and two types of carriers. It is more complicated to implement than the standard SPWM technique, especially in DSP. A new modulation strategy of modified SPWM is needed to construct PWM in DSP via the PWM module provided. The choice of a DSP is due to its fast sampling of tasks, capability to solve mathematical algorithm in digital control tasks (via c-coding), and easy handling of floating numbers. The board is well designed, equipped with modules such as ADC, enhanced PWM (ePWM), and GPIO. The ePWM module is able to generate complex pulsewidth signals with minimal CPU intervention; it clocks synchronously to enable single-system operation (suitable for 3-phase systems). A three-phase AC-DC buck converter with bidirectional capability is proposed to test the PWM switching design.

Modified SPWM resolves issues of obtaining almost sinusoidal AC input current, near-unity input power factor, low THD, and a controllable DC voltage in three-phase AC-DC buck-type converter. The switching technique does not address issues of system disturbance. Such issues can be addressed by suitable voltage feedback control. PI and PID controllers are popular techniques to address these issues. However, both of these controllers have their own drawbacks such as PI is not able to produce the desired transient response for a large step changes in reference/load while PID produces a set kick phenomenon (for the step input of reference) in practice. Therefore a modified PID

technique is required and investigated to address issues of step changing (small and large step changing) issues in reference and load.

1.3 Objective

The research's aim is to design a new voltage feedback control and implement it in a three-phase AC-DC buck-type converter with bidirectional power flow, to achieve sinusoidal input current with low THD and unity power factor input current, and regulated and controllable DC voltage via modified PWM technique. The voltage feedback control should be able to solve the dynamic response in step-changing issues of reference and disturbance during AC-DC operation. The objectives are:

1) To develop a simpler modified SPWM technique on a new approach.
2) To implement the proposed simplified voltage-based SPWM in a proposed three-phase AC-DC buck-type converter with bidirectional power flow capability.
3) To develop new voltage feedback controller (during AC-DC operation) to address issues of step-changing of reference or disturbance. This work concentrates on the design procedures, the effects of the control parameters, and evaluating the control performance.

The methodologies of the work are:

1) Design of the modified SPWM technique with a new approach and proof of its similarity to the original technique.

2) Proposal of a three-phase AC-DC buck converter that incorporates bidirectional power flow to reduce the number of switches and the complexity of designing PWM switching patterns.
3) Simulation of the new simplified voltage-based SPWM technique in the proposed three-phase AC-DC buck converter during AC-DC and DC-AC power flow.
4) Design of new, simple technique in implementing digital voltage controller to resolve disturbance issues and offer good dynamic responses.
5) Implementation of a hardware prototype of the proposed three-phase buck-type converter with bidirectional power flow.

1.4 Structure of Thesis

This thesis is organized into seven chapters, with its remainder organized as such:

Chapter 2 presents a review of literatures on various topologies of AC-DC converters and their classification. The modulation and control techniques are also discussed in terms of their operational principle and PWM switching. General reviews of past works on feedback control techniques used in AC-DC buck converters are also presented.

Chapter 3 discusses the circuit configuration of the proposed bidirectional AC-DC buck converter, and the converter's operating principle and switching technique during AC-DC and DC-AC operations. The proposed modifications to SPWM and verification of their feasibility via mathematical analysis and simulation are also discussed, including the method of implementing the proposed simplified-modified SPWM in a DSP microprocessor.

Chapter 4 presents the design and analysis of the proposed feedback control algorithm in a linear system during AC-DC operation. Two control algorithms are presented and discussed: I-D control and modulation-index-curve prediction technique. The controller's design procedure (such as gain tuning) is described and the dynamic performances of the control algorithms are analyzed by using MATLAB/Simulink for transient cases of step-changed input and step-changed disturbance.

Chapter 5 presents the simulation results using MATLAB/Simulink of the proposed bidirectional AC-DC buck converter circuit configuration and the simplified-modified SPWM switching technique, during the AC-DC and DC-AC operations. The effectiveness of the proposed feedback control algorithms during AC-DC operation is evaluated for its DC voltage/currents transient and steady-state responses, the harmonic distortion in the AC currents, and the power factor, from step-changes in the references and loads.

Chapter 6 presents the laboratory setup, the test results of the proposed circuit configuration, and the verifying simplified-modified SPWM switching technique on open-loop system. The results of the closed-loop system are presented and evaluated to prove the effectiveness of the proposed control algorithms, which was developed in a TMS320F28335 DSP.

Chapter 7 concludes with a summary, a listing of contributions, and recommendations for possible future work.

CHAPTER 2

AC-DC CONVERTERS AND SWITCHING CONTROL TECHNIQUES: OVERVIEW

2.1 Introduction

Power converter is used to process and control the electric energy by supplying voltage and current sources, in a form that is suited for user's loads. Basically the devices consist of non-linear elements, mainly electronic semiconductor switches i.e. diode, IGBTs, and MOSFETs; and linear reactive elements i.e. capacitors, inductances and mutual inductances or transformers. These reactive components are used for intermediate energy storage but also for voltage and current filtering. The conversion process includes converting electric energy between alternating current (AC) and direct current (DC); changing the amplitude of voltage, current or frequency; or also the combination of those.

A converter that converts the AC from the main supply to a DC is known as an AC-DC converter or rectifier. The converter generally contains a rectifier bridge and regulating devices to rectify the AC current of the input line and produce one or more regulated DC voltages. The applications of AC-DC converter is established in the systems such as telecommunication's power supplies, adjustable-speeds drive (ASD), uninterruptible power supplies (UPS), high voltage direct current (HVDC), interfacing

and battery energy storage in solar photovoltaic (PVs), and electric vehicle's battery charging (Singh et al., 2004).

The use of diodes and thyristors in the conventional AC-DC converter causes poor power quality, such as low power factor and high total harmonic distortion (THD) at input AC mains, fluctuate rippled at DC output and hence produces poor efficiency of the system. Various works report the switch modes configuration for AC-DC converters that use as a replacement of the conventional diodes rectifiers.

This chapter presents the configurations of AC-DC converters that can be classified based on the type of AC source which is single-phase and three-phase. Three-phase type can be categorized as buck, boost, buck-boost and multilevel converters. The discussion then more focuses on three-phase AC-DC buck-type converter and its principle of operation. Various techniques of switching and modulation control of AC-DC switch-mode converters are also discussed in order to achieve unity power factor and lower total harmonic distortion (THD) at line current. The system feedback control techniques are also reviewed to highlight the advantages and limitations. A comparison between an existing and the proposed of three-phase AC-DC converters are also provided.

2.2 AC-DC Converters

As it has been observed for recent decades, an increasing part of the generated electric energy is converted through rectifiers, before it is used at the final load. The AC-DC converters are non-linear in nature and, consequently, generate harmonic currents in to the ac line power. The high harmonic content of the line current, resulting

low power factor of the load and cause a number of problems in the power distribution system like:

- Voltage distortion and electromagnetic interface (EMI) affecting other users of the power system.
- Increase volt ampere ratings of the power system equipment (generators, transformers, transmission lines, etc.).

Therefore, governments and international organizations have introduced new standards (in the USA: IEEE 519 and in Europe: IEC 61000-3), which limit the harmonic content of the current drown from the power line by the rectifiers.

A great number of new switch-mode AC-DC topologies that comply with solid-state self-commutating devices such as MOSFETs, IGBTs, GTOs, etc. are widely used nowadays as a replacement of conventional diode rectifier to obtain nearly sinusoidal input current, regulation of input power factor to unity, low harmonic distortion of line current (THD below 5%), and stabilization of DC-link voltage (or current). The configurations and the methods of operation can be divided into two: single-phase and three-phase.

2.3 Single-Phase AC-DC Converters

Single-phase AC-DC converters are widely used for power supplies for domestic equipment, electric vehicles battery charging applications, interfacing storage batteries for uninterruptible power supplies and supplying energy from photovoltaic systems to the grid. The function of the converters is to achieve a nearly unity power factor by drawing a sinusoidal current that is in phase with the source voltage, thus eliminating the reactive power and the harmonic interference with other equipment operating off the same source.

Basically, single-phase AC-DC converter consists of a diode bridge plus a step-down chopper (Xu, Ruan, & Yan, 2001) or step-up chopper (Huber, Jovanovic, & Lee, 2001; Yoshida, Shiizuka, Miyashita, & Ohniwa, 2000) or both of step-down and step-up chopper (Qiao & Smedley, 2001) depends on the application. The configurations also known as single-phase buck type, boost type, and buck-boost AC-DC converters as shown in Figure 2.1.

The introducing of multilevel type AC-DC converters are beneficial for high-voltage and high-power applications (Cruz & Barbi, 2001; Bor-ren Lin & Lu, 2000). The concept of multilevel converters may reduce the switching frequency of the devices and also avoid a low-frequency transformer (Singh, Singh, Chandra, Al-haddad, & Pandey, 2003). Singh, Singh, & Chandra (2011) performed a comprehensive study on the single-phase AC-DC power factor corrected converters with-high frequency isolation for benefits of practice, application and design engineering field.

Investigation on the concept of AC-DC-DC has been done by Bor-ren Lin & Huang (2005) where they proposed a single-phase AC-DC-AC converter with capacitor clamped topology to achieve a power factor correction in the AC-DC converter and to generate a sinusoidal voltage in the DC-AC inverter. A three-level three-leg AC–DC–AC converter for single-phase applications has been investigated by Freitas, Jacobina, Roberto, & Oliveira (2010) using PWM technique. The converter result in lower losses and costs compared to two-level converters, furthermore the voltage stress on the power switches and harmonic distortion on the input and output voltages are reduced.

The new concept of single stage converters instead of two stages (a boost converter plus H-bridge AC-DC converter) using two controllers to actively control input power factor and the intermediate DC bus voltage; and to control output voltage, has been proposed by Das, Pahlevaninezhad, & Moschopoulos (2013). An active single-phase AC-DC converter using combination of H-Bridge and decoupling circuit has been

investigated by Su, Pan, Long, Sun, & Yang (2014) to enhance power-decoupling performance. The energy-storage inductor method and multiresonant controller with feed-forward control are used to increase the ability of current tracking.

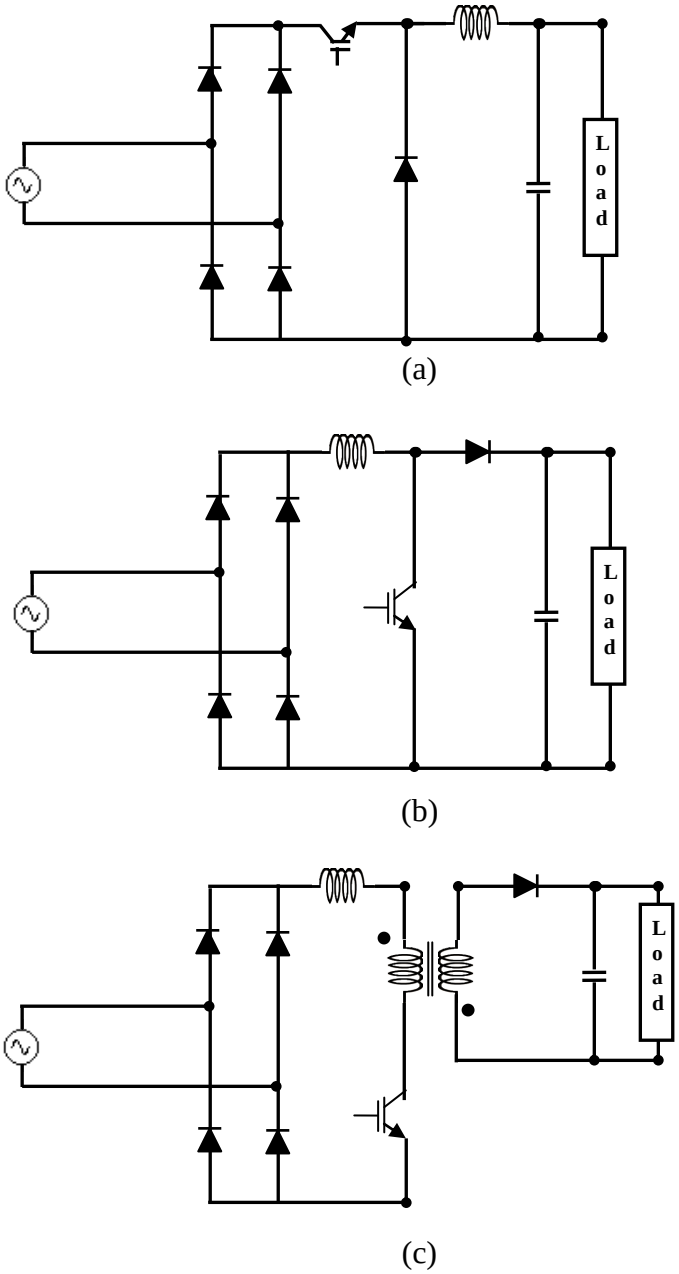


Figure 2.1: Single-phase (a) buck, (b) boost, and (c) Flyback AC-DC converters

2.4 Three-Phase AC-DC Converters

Three-phase AC-DC converter are extensively used in battery charging in automotive applications (Heme & Ave, 2001; Soeiro, Friedli, & Kolar, 2012), DC motor speed control for various applications (Senini & Wolfs, 2000; Singh, Garg, & Bhuvaneswari, 2007), power supply for telecommunication systems (Kalpana, Bhuvaneswari, Singh, Singh, & Gairola, 2013) and for high power application in industry (Wallace, Bendre, Nord, & Venkataramanan, 2002). Same as single-phase system, the main objective of the converter is to achieve a nearly unity power factor with a sinusoidal current, low THD and a controllable DC voltage.

Three-phase AC-DC converter system can be categorized as a passive system, hybrid system and active system (Kolar & Friedli, 2013). Passive system is a conventional ac-dc converter such as single-diode bridge and multipulse rectifier where it used passive elements (inductance and capacitance) at AC and DC sides. The drawbacks of this converter are; low power quality and bulky size of filter. To overcome these problems, hybrid system and active system are investigated. Hybrid system includes system of electronic reactance based rectifier, combination of diode rectifier and DC/DC converter and third harmonic injection, while active system uses a direct three-phase system approach either impresses input current (current-source) or input voltage (voltage source).

The classification of switch-mode three-phase AC-DC converters on the basis of converter circuit configurations can be divided into four main categories, buck-type (Stupar, Friedli, Minib, & Kolar, 2012), boost-type (T. Lee, 2003), buck-boost-type (Pires & Silva, 2005; D. Wijeratne & Moschopoulos, 2013; D. S. Wijeratne & Moschopoulos, 2014) and multilevel-type (Bai, Zhang, & Chen, 2008; Marcelo Lobo Heldwein, Mussa, & Barbi, 2010; B Lin, Lee, & Yang, 2003) as shown in Figure 2.2.

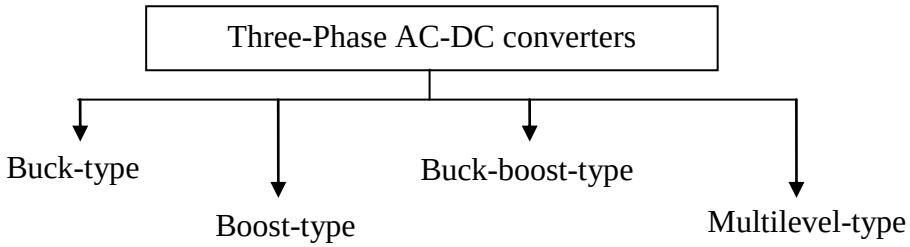


Figure 2.2: Classification of three-phase AC-DC converters

Three-phase boost-type AC –DC converter is well established and widely used in power conversion systems that require output voltage greater than input voltage. Large numbers of circuit configurations of these converters such as using single-switch (Jang & Jovanovi, 1998; J. Lee et al., 2001; Zou, Yao, Ye, & Ruan, 2012), two-switch (Naik, Rastogi, & Mohan, 1992), three-switch (Kolar, Drofenik, & Zach, 1999; Sabzehgar & Moallem, 2013), four switch (G. Kim & Lipo, 1996) and six-switch (Ma, Xu, & Li, 2012; Ooi, Dixon, Kulkarni, & Nishimoto, 1988; Wan, Huang, & Tse, 2013) are reported to provide unity power factor with lower THD at AC lines, and to obtain constant regulated DC output voltage with excellent dynamic response under any condition that involve in variations of AC voltage and DC load.

Zou et al. (2012) proposes a three-phase single-switch boost-type AC-DC converter that operates in discontinuous current mode (DCM) by implementing a variable duty cycle control circuit for switching. The converter is suitable for low-to-medium power conversions and it has special features such as constant frequency operation with simple analogue control, low cost implementation, zero-current turn-on for the switch and no need a reverse recovery in diode.

Three-phase boost-type AC –DC converters with six-switches using outer voltage and inner current loop are commonly used to regulate DC voltage with unity input power factor. However, the control techniques show greatly attainment of ideal

power grid case and linear operation. Wan et al. (2013) studies the behaviour and instability in the converter when it is connected to a nonideal power grid and nonlinear operation (with the presence of other interacting loads). An irreversible divergence phenomenon in a three-phase VSC connected to a power grid with an interacting load is analysed using large-signal analysis to identify the physical origin of the phenomenon and also to locate the boundary of the instability.

Three-phase single-stage buck–boost-type AC-DC converter proposed by Pires & Silva (2005) has the following benefits such as; the converters requires only four power switches (eg. the conventional converter uses at least six power switches) and improves the converter efficiency due to only one reverse-blocking power semiconductor conducts at any time. The proposed three-phase buck-boost AC-DC converter employs a vector-based sliding-mode control method to track fast and robust suitable sinusoidal reference in phase with the input source voltage; and an external proportional-integral (PI) controller for output voltage regulation of the converter.

Three-phase AC-DC quasi-resonant buck-boost converter using two switches suitable for a wide range of output DC voltages and power levels applications is proposed by D. Wijeratne & Moschopoulos (2013). D. S. Wijeratne & Moschopoulos (2014) also propose a simple, low-cost, reduced-switch, three-phase AC–DC buck–boost-type converter. The two-switch buck–boost-type converter has a significantly reduced peak switch voltage stresses compared to a single-switch buck–boost-type converter as implemented in Borges & Barbi (2011).

Cuk- or sepic-converters also can be considered under buck-boost-type of AC-DC converters (Zane & Maksimovic, 1996). Because of its complex circuit realization, hence these converters were not described in more detail. However Bist & Singh (2014) successful applied PFC cuk converter in BLDC motor drive.

Interest in multilevel-type three-phase AC-DC converter is shown due to its benefit in high power application. However, the main drawback of this type of converter is the large number of power switches used in the circuits (eg. the conventional three-phase neutral point clamped rectifier use twelve power switches). B Lin et al. (2003) reduce number of switches by adopting a control scheme which consists of hysteresis current controller, neutral point compensator, PI controller and phase-locked loop (PLL) circuit to draw the balanced and sinusoidal line currents with unity power factor, to control the DC output voltage to be constant, and to balance the neutral point voltage. However, the method requires a complex control circuit implementation.

A simpler control scheme that uses more power switch (18 power switch) is proposed by Bai et al. (2008). It comprises three modules of current-source with carrier phase-shifted sinusoidal pulse-width modulation (SPWM); has some advantages such as a simpler control of power factor, equivalent higher switching frequency at AC side even with lower switching frequency and eliminates low harmonics (eg. 6^{th} harmonics, etc.) in DC output voltage. So the converter will be a good potential AC-DC converter especially for higher power applications.

2.5 Three-Phase AC-DC Buck Converter

Three-phase AC-DC buck converter provides output voltage lower than input voltage. In practice the buck-type configuration solves the requirement for medium power with high input such as telecommunication power supply (M.L. Heldwein, Nussbaumer, & Kolar, 2010; Nussbaumer, Baumann, & Kolar, 2007), battery charging systems (Heme & Ave, 2001) and uninterruptable power supply (UPS) systems (Jeltsema, Scherpen, & Klaassens, 2001). The classification of switch-mode three phase

AC-DC buck-type converters on the basis of circuit configurations can be divided into two main categories: unidirectional and bidirectional.

Unidirectional AC–DC power buck-type converters are typically implemented either in single-stage or two-stage as a replacement for the conventional diode bridge or thyristors. This type of converter allows only one direction of power flow, AC side to DC side. Several unidirectional of typical three-phase AC-DC buck-type converter's configurations are shown in Figure 2.3. Figures 2.3(a-b) are two-stage converter, used a combination of conventional diode bridge and a DC-DC buck converter using a switch (Pouliquen, Buchheit, & Lethelliez, 1994) and two switches (Nishida, 1996). Figures 2.3 (c-d) are known as single-stage converters or active AC-DC converters that involving the use of three (Nussbaumer et al., 2007) and six switches (Bai, Ma, Xu, & Wu, 2014; M. Baumann, Drofenik, & Kolar, 2000; Martha Baumann & Kolar, 2001). A buck-type configuration needs a path for inductor reverse current (at DC side). A diode is placed at DC side to provide the freewheeling path (refer Figure 2.3).

Milanovic & Slibar (2011) and Raihan & Rahim (2013) remove the freewheeling diode by designing an appropriate switching control that can provide the freewheeling path using Field Programmable Gate Array (FPGA). A lot of modification and improvement on circuit configuration and switching control design are investigated to suit design or application requirement. The objective of these modifications are to simplify the circuit configuration and switching control design, to reduce harmonics currents at input AC mains, to lower the number of switches, and etc.

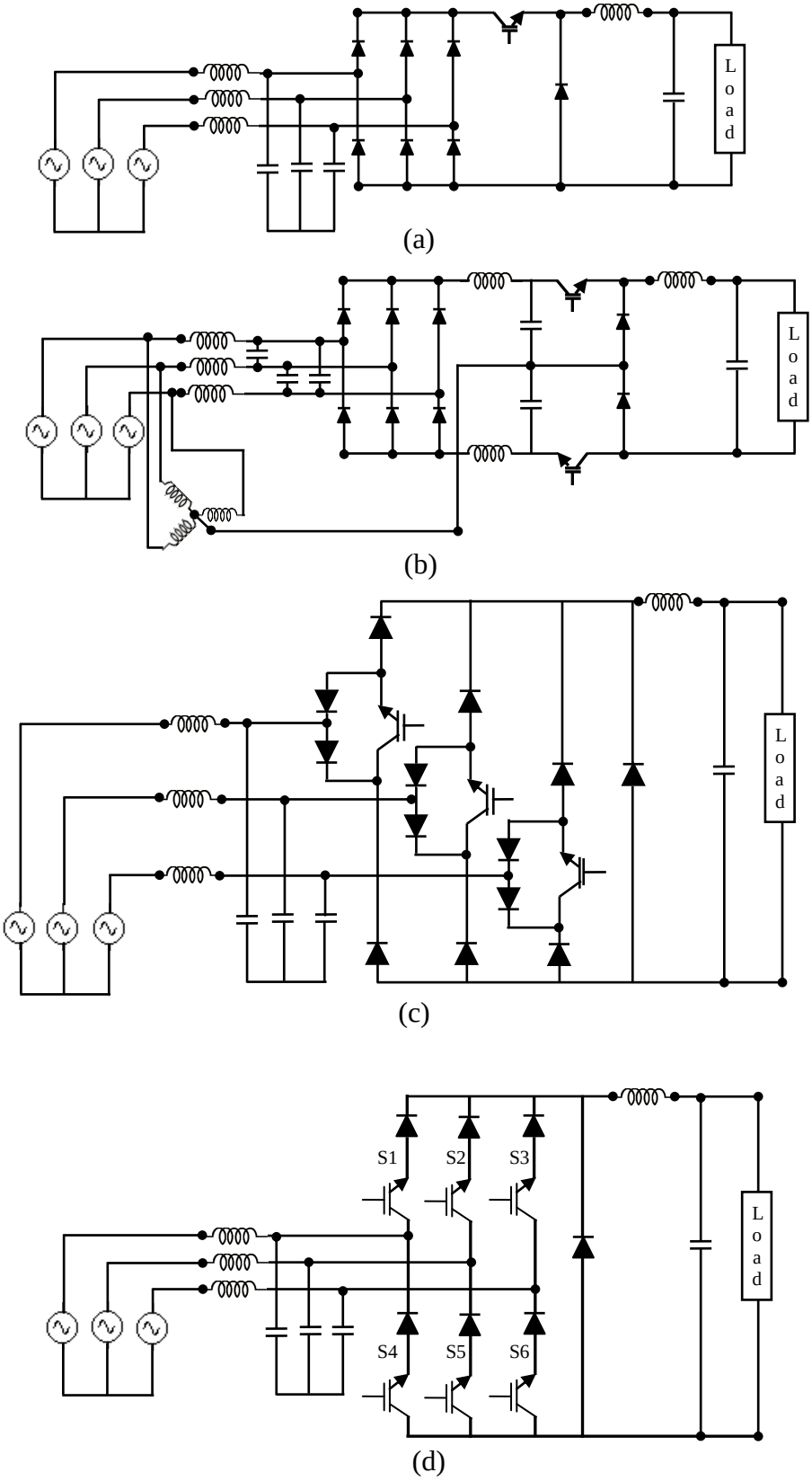


Figure 2.3: (a) Single-switch, (b) Two-switch, (c) Three-switch, and (d) Six-switch buck-type converters

The bidirectional topologies provide two modes of power flow, AC to DC or DC to AC sides. Such circuit configuration (refer Figure 2.4), that can function as both AC-DC and DC-AC converters, have been reported, namely, GTO-based bidirectional buck converter (Hill & Luo, 1987; Ueda, Hombu, & Ueda, 1987), IGBT-based bidirectional buck converter that using six-switches (D. Lee & Kim, 1996; Yang et al., 2006) and four pole bidirectional buck converter (Chudoung & Sangwongwanich, 2007). IGBT-based bidirectional buck converter that using six-switches is also known as a Current Source Inverter (CSI) or Current Source Converter (CSC) when the power flow from DC to AC side. (Bai et al., 2014) used this CSC configuration for grid-connected to solve the problem of resonance damping and harmonic suppression. A common ASD circuit configuration with two six-switch converters, that function as AC-DC and DC-AC (as shown in Figure 2.5) is developed to generate high-quality AC current waveforms in term of reducing harmonics while keeping a constant DC voltage with nearly unity power factor displacement. The extensively researches have been done using this configuration for wind applications system (J. Dai, Xu, & Wu, 2007; Tan, Dai, & Wu, 2011).

However some of the circuit configuration is able to deliver energy back from the DC side to the AC power supply, which means the converter can reverse the energy flow during the operation. This converter is known as a regenerative AC-DC converter and examples for these applications are found in machine drives such locomotives, downhill conveyors, cranes, etc. (J. R. Rodríguez et al., 2005). The concept of reversible power flow direction of one polarity can be realized only by adding an anti-parallel switch to the diodes (Green et al., 1997; J. R. Rodríguez et al., 2005), or through bidirectional diodes (four diodes), which achieve bidirectional flow (Yang et al., 2006). The regenerative bidirectional-type converters are suitably used in adjustable speed drives (ASDs) (Gubia, Sanchis, Lopez, Ursua, & Marroyo, 2008; Klumpner & Blaabjerg, 2004),

especially in a controlled braking system and in battery charging of uninterruptible power supplies (UPSs).

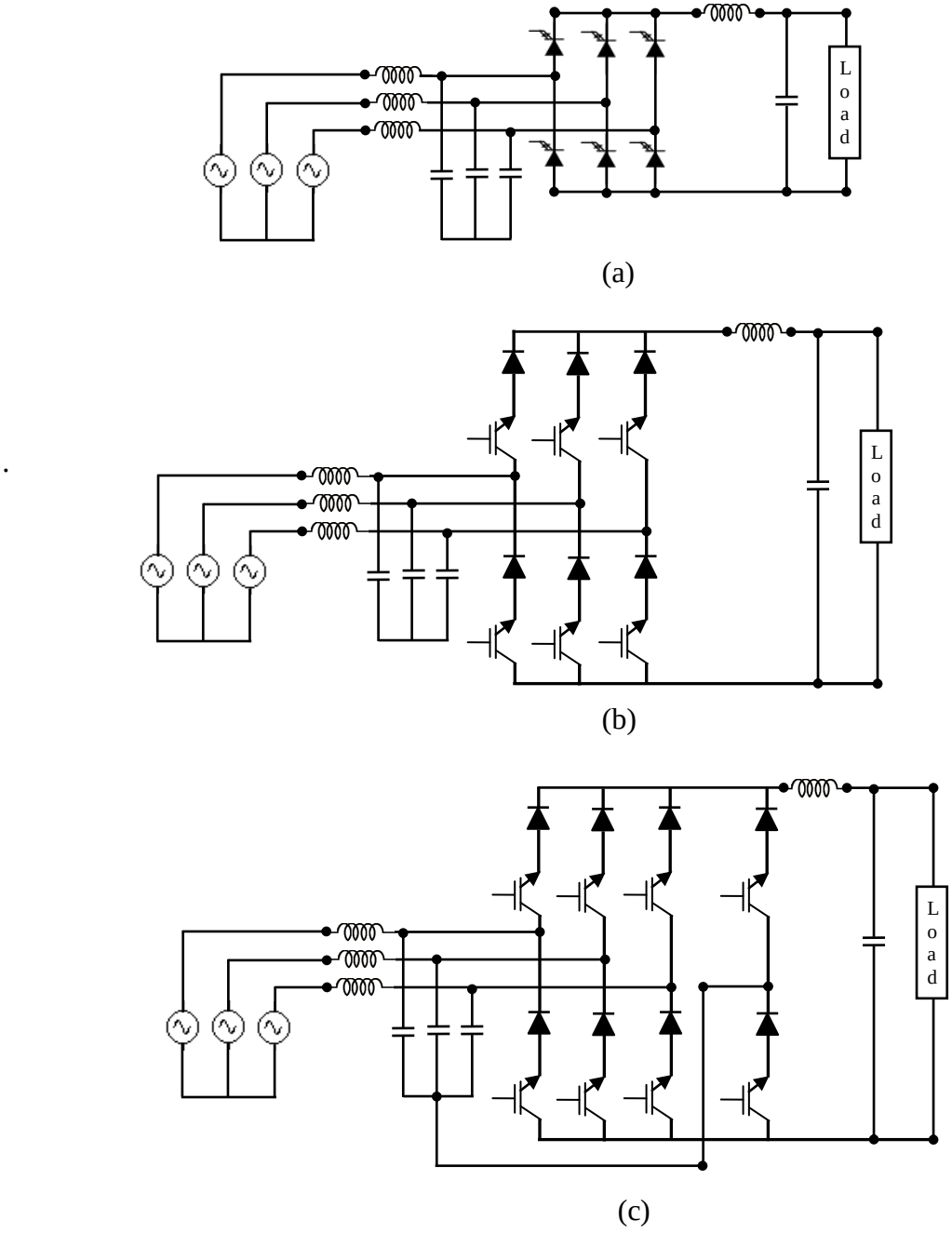


Figure 2.4: (a) GTO-based bidirectional buck converter (b) IGBT-based bidirectional buck-type converter (c) Four-pole bidirectional buck converter

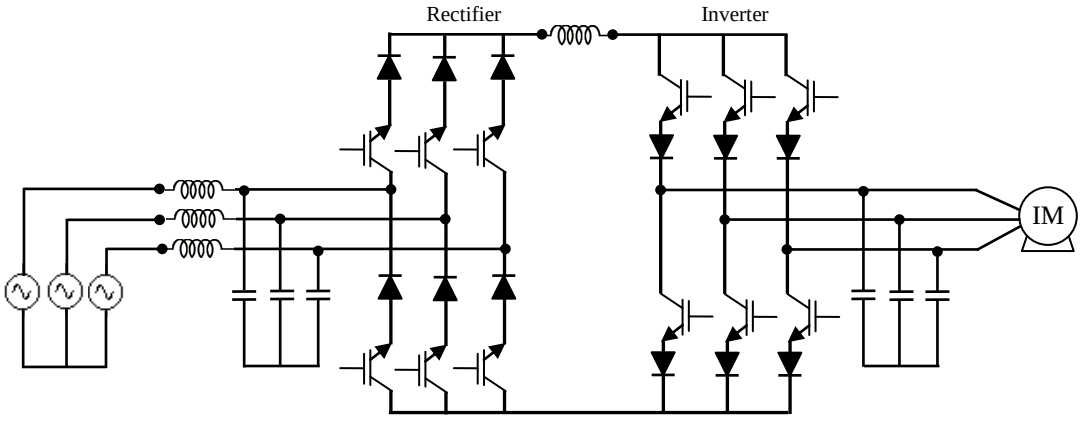


Figure 2.5: ASD based on a current source rectifier (CSR)

2.6 Three-Phase Six-Switch Buck-Type AC-DC Converter

Three-phase six-switch buck-type AC-DC converter (refer Figure 2.3(d)) with PWM strategy can produce identical normalized electrical variables for which equivalent gating patterns have been found by the modulating techniques. Normally this configuration needs a filter (LC filter) at AC side and DC side to accomplish the regulated DC voltage with sinusoidal input current at AC mains supply. Figure 2.6 shows a general block of overall three-phase six-switch buck-type AC-DC converter's system, containing input and output filters, modulating technique and control strategy.

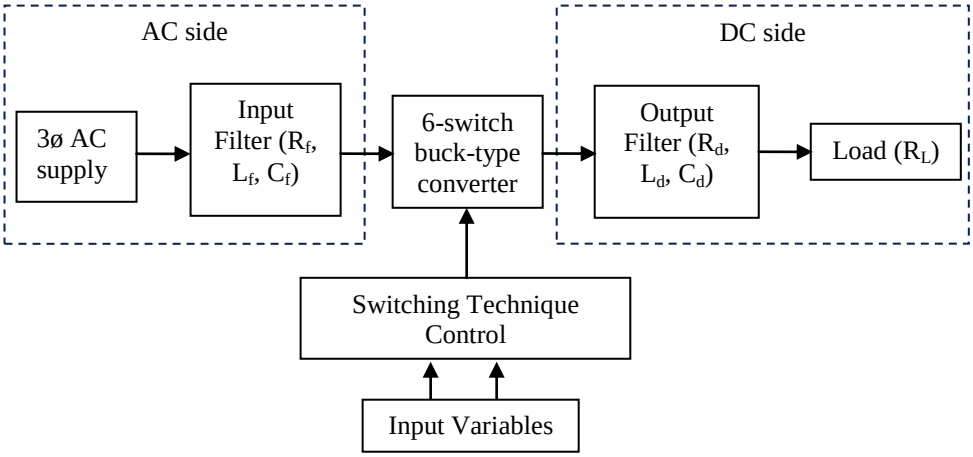


Figure 2.6: Three-phase six-switch buck-type AC-DC system

The main objective of three-phase six-switch buck-type AC-DC converter is to produce an adjustable regulated DC current from the AC main supply. The converter has been extensively developed to provide high-quality waveforms which are described as nearly sinusoidal ac input current, regulation of input power factor to unity and low harmonic distortion of line current, as a replacement of the conventional diodes/thyristors rectifiers. The filter's size and cost also can be reduced compared to the conventional.

Two common constraints that must always be met in order to properly operate the three-phase six-switch buck-type AC-DC topology. First, the AC side must not be short circuited due to its mostly capacitive. The second constraint is the DC bus cannot be opened because of the current-source type. Therefore, it summarized that one top switch and one bottom switch must be closed at all time (Jos´e R. Espinoza & Joos, 1997) for a three phase six-switch buck-type AC-DC converter circuit operation. From these constraints imply that nine switch states must be followed, as shown in Table 2.1.

Table 2.1: Switch states for a three-phase six-switch buck-type AC-DC converter

Switch						**State**	$\mathbf{I_a}$	$\mathbf{I_b}$	$\mathbf{I_c}$
Top			**Bottom**						
S1	**S2**	**S3**	**S4**	**S5**	**S6**				
1	0	0	0	0	1	1	I_L	0	$-I_L$
0	1	0	0	0	1	2	0	I_L	$-I_L$
0	1	0	1	0	0	3	$-I_L$	I_L	0
0	0	1	1	0	0	4	$-I_L$	0	I_L
0	0	1	0	1	0	5	0	$-I_L$	I_L
1	0	0	0	1	0	6	I_L	$-I_L$	0
1	0	0	1	0	0	7	0	0	0
0	1	0	0	1	0	8	0	0	0
0	0	1	0	0	1	9	0	0	0

The constraints are reduced the states in three-phase six-switch buck-type AC-DC converter, where states 7–9 (Table 2.1) produce zero AC line currents, with no energy supplied to the DC load. In this case, the DC current freewheels through the combination of up and bottom switches at the same leg, which is either the switches S1 and S4, S2 and S5 and S3 and S6. The other solution recommended to provide an alternative path output current is by adding a freewheeling diode across the DC-link as shown in Figure 2.7 (J.Conde-Enriquez, J.S.Benitez-Read, Duran-Gomez, & Pacheco-Sotelo, 1999). In the absence of this diode, the transition from a standby mode to an energy provision mode must be very exact to maintain a continuous path to the current of the output inductor. Normally this path can be maintained constantly by employing overlapping of turning-on and turning-off switches.

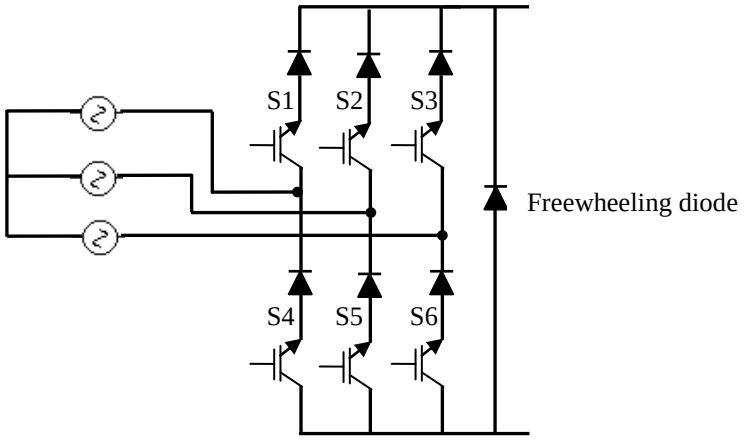


Figure 2.7: The conventional 6-switch 6-diode with freewheeling diode at DC side

The conventional 6-switch 6-diode is simplified to 3-switch 12-diode as shown in Figure 2.3(c), which has less driver-device. The advantage of this modification making it has less switch states as shown in Table 2.2. This simplified topology with different control approaches is proposed in (Malesani & Tenti, 1987; Nussbaumer, Heldwein, Gong, Round, & Kolar, 2008; Nussbaumer, Heldwein, & Kolar, 2006) with different control approaches for online implementation. However the three-switch configuration requires double diodes compared to six-switches.

Table 2.2: Switch states for a modified switch states for a three-phase six-switch buck-type AC-DC converter.

Switch			**State**	$\mathbf{I_a}$	$\mathbf{I_b}$	$\mathbf{I_c}$
S1	**S2**	**S3**				
1	1	0	1	$I_L/-I_L$	$I_L/-I_L$	0
0	1	1	2	0	$I_L/-I_L$	$I_L/-I_L$
1	0	1	3	$I_L/-I_L$	0	$I_L/-I_L$
1	0	0	4	0	0	0
0	1	0	5	0	0	0
0	0	1	6	0	0	0

2.7 Switching Technique Design for AC-DC Converter

Switch-mode three-phase AC-DC converters require specific control switching technique design either in open-loop or closed-loop operations. The objectives of these control switching techniques for power factor correction (PFC) of AC-DC power converters are: to control the active and reactive AC current component, and also to regulate DC output. The most common techniques will be discussed: hysteresis current control, pulse-width modulation (PWM), ramp comparison control and predictive current control.

2.7.1 Hysteresis current control

The basic switching pattern of hysteresis current control technique is defined by comparing the current's error with the fixed hysteresis band. The technique can be easily implemented in analog circuit and it is known for its very good dynamic performance, fast transients, no DC offset and simplest implementation. The main drawbacks of this method include the inconstant switching frequency, lack of communication between phases for three-phase system, very dependent on sensors that will increase the current error, the propensity to lock into high-frequency switching cycles, and the current error that is not strictly limited (Holtz, 1994). This switching strategy is popular in low/medium power due to its high switching losses at high switching frequency.

Due to the drawbacks of the conventional hysteresis current control, modifications on the strategy are introduced, including:

i. The space-vector-based hysteresis: the technique is a combination of hysteresis current control and the space vector modulation strategy and suitable for three-phase system (Bor-ren Lin, Wu, & Shiue, 1997). The technique greatly improves the switching numbers of the system and simplify the hardware circuit implementation.

ii. Double-band hysteresis current control: the technique achieve a fast response and implement a double-band hysteresis current control in stationary reference frame to reduce the switching frequency and current error (B. Kim, Oh, & Lees, 2004).

iii. The variable hysteresis band control: the technique is implemented to achieve a constant switching frequency and the hysteresis band is controlled as variations of the AC-DC converter input voltage and output DC link voltage at any operating conditions (Liu & Maswood, 2006).

2.7.2 Nonlinear-Carrier Control

Nonlinear-carrier (NLC) control is a technique for power factor correction (PFC) and applied in AC-DC boost-type converter. The control technique is proposed for reducing the structure complexity circuit realization in the average current mode controller (Bazinet & Connor, 1994). (Maksimovic & Erickson, 1996) proposed NLC for boost rectifier and also then extended the application of NLC control for high-power-factor rectifier based on flyback, cuk or sepic converter (Zane & Maksimovic, 1998). A general block diagram of the NLC controller for generating a switching pattern in the rectifier application is shown in Figure 2.8. The input voltage-sensing, error

amplifier in the current-shaping loop and the multiplier or divider circuitry in the voltage feedback loop are eliminated (Zane & Maksimovic, 1996).

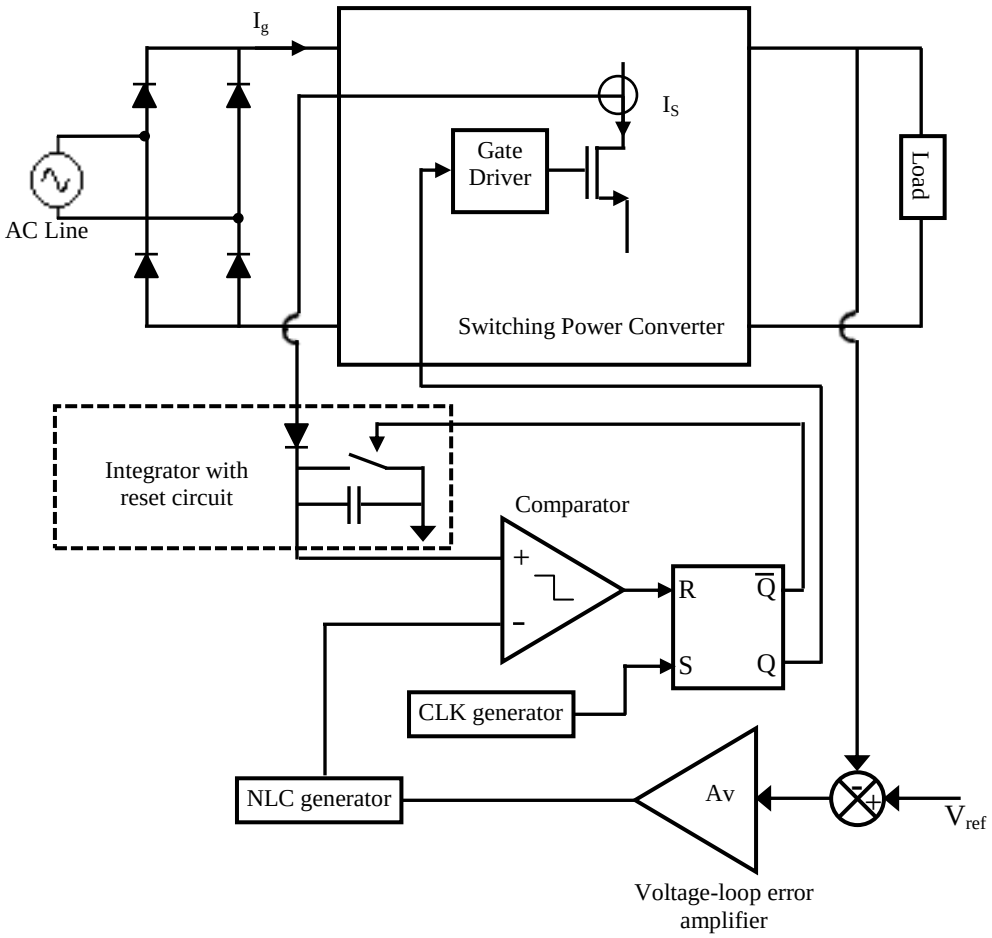


Figure 2.8: A block diagram of the NLC controller for rectifier

A modified version of NLC control for boost rectifier has been proposed in K. I. Hwu (2006) where a feedforward control technique is additionally applied to generate the nonlinear carrier by using a double integrator. The improved NLC reduce the total harmonic distortion of the line current and increase the corresponding power factor of the system. Chiang, Liu, & Chen (2013) implement NLC for a single-phase PFC boost converter with variable slope ramp on field-programmable gate-array (FPGA). The complexity of the analog-controlled integrated circuit is replaced by implementing

FPGA-based for generate the nonlinear carrier. With this modification, the wide output range for PFC rectifier system is achieved using a simple implementation compared to analog circuitry.

In conclusion, the NLC control has several advantages, such as a simpler implementation by removing the input voltage-sensing circuit, an error amplifier in the current shaping loop, or other external control component; nearly-unity power factor; and low harmonic distortion. However this NLC is only suitable for single-phase boost-type AC-DC converters.

2.7.3 Predictive Current Control

Predictive current control (PCC) is an instantaneous-current control method that is widely used in power electronics applications (Nussbaumer et al., 2008). The technique applies the concept of one-sampling-ahead-preview (Nishida, Miyashita, Haneyoshi, Tomita, & Maeda, 1997), generally to predict the track of current vector or current error vector and then generate the switching pattern for the next sampling interval. The switching technique is usually implemented by a microprocessor or digital signal processors (DSP). Field programmable gate array (FPGA), which popular for its advantages of parallel instructions operation and input-output capabilities, has also been used recently in developing the prediction algorithm to control the switching for AC-DC converter (Perez, Vasquez, Rodriguez, & Pontt, 2009). (Jeong & Song, 2007) proposed an improved algorithm for PCC to make control system faster by introducing an online correction of load parameters.

Comparative study between NLC and PCC in Orabi, Haron, & El-Aroudi (2007) shows that predictive current control is less sensitive for unstable condition than NLC control, but the implementation of PCC is more complicated. The integration of

prediction switching modulator and NLC control is verified by Chattopadhyay, Ramanarayanan, & Jayashankar (2003) to give a high power factor with low total harmonic distortion for boost-type AC-DC converter.

Recent publications combine predictive control technique with direct power control (DPC) (Bouafia & Krim, 2010; Mesbah, Masoum, & Islam, 2011) for three-phase AC-DC converter. The proposed predictive direct power control was greatly improved in both transient and steady-state performance compared with conventional DPC using the switching table.

The predictive current method greatly improved in dynamic and steady-state responses; and the capability to handle complex control objectives. The implementation is simpler (software) and robustness of system also can be achieved. However, the excellent performance of the system directly dependent on the accuracy of system parameters and operating conditions (Chaves, Margato, Silva, Pinto, & Santana, 2011; Jeong & Song, 2007).

2.7.4 Pulse-Width Modulation (PWM)

Pulse-width modulation (PWM) is among the most recognized techniques of converting AC to DC (Singh et al., 2004). The scheme diminishes low-order harmonics and eliminates high-order harmonics through passive filtering. Various PWM techniques have been evaluated by Nussbaumer et al. (2006) according to application. Among several modulating techniques to generating a PWM, carrier-based PWM is the simplest. It involves comparing the reference signal with the carrier signal. Other PWM modulating techniques that have been implemented include selective harmonic elimination (Enjeti, Ziogas, & Lindsay, 1990; José R Espinoza, Joós, Guzmán, Morán, & Burgos, 2001; Karshenas, Kojori, & Dewan, 1995; Sharon & Fuchs, 2000) and

space-vector modulation (Malinowski et al., 2004; Salo & Tuusa, 2000). Selective harmonic elimination uses low switching frequency and allows elimination of specific harmonics, but the technique produces higher THD and needs a complex algorithm to solve. Space vector is a digital modulating technique; it generates PWM AC line currents that averagely equal the given reference currents, through proper selection of the switch states and calculation of each sampling period. The states and time periods are selected through space vector transformation (Kwon & Min, 1993).

The relationship between space vector modulation and non-sinusoidal carrier-based PWM in three-phase systems have been analyzed by Zhou & Wang (2002). They found a common platform to both PWM techniques, allowing transformation from non-sinusoidal carrier-based PWM to space-vector modulation. The analysis was independent of the load type, and indicated that in both modulation techniques the maximum possible modulation signal is $2/\sqrt{3}$ the linear modulator range.

The pulse pattern of PWM technique for AC-DC power converter is frequently generated via offline implementation. The drawbacks of offline PWM modulators include slow dynamic response and transient DC offset. To overcome these drawbacks, Jos´e R. Espinoza & Joos (1997) proposed an online analog carrier-based PWM modulator; it lowers switching frequency and reduces current-harmonic distortion.

Common carrier-based PWM techniques in AC-DC converters are sinusoidal-pulse-width modulation (SPWM) and modified sinusoidal-pulse-width modulation (MSPWM). The extensive use of carrier-based PWM in AC-DC converters is due to its wide range of applications, uncomplicated control implementation, and easy implementation in analog circuits or digital systems.

2.7.4.1 Sinusoidal-Pulse-Width Modulation (SPWM)

The PWM gating signals are generated by comparing the sinusoidal reference signal with the higher-frequency carrier signal. Figure 2.9 illustrates a sinusoidal reference signal of 50Hz frequency, a carrier signal of 1kHz frequency, and the pulse pattern generated by SPWM. The principle of SPWM is that the output (pulse) is high when the sinusoidal signal has a magnitude higher than the carrier signal's, otherwise, it is low. The carrier signal is usually a triangular or sawtooth signal and has a fixed frequency (Boost & Ziogas, 1988). The sinusoidal reference signal, known also as the control signal, has a fundamental frequency (which is the same as that of the mains supply). Therefore, the output of the modulating signals can be varied by changing the amplitude of the control signal. The modulation index M can be obtained from Equation (2.1):

$$\text{Modulation Index} \quad M = \frac{Vm}{Vc} \tag{2.1}$$

where Vm is the peak amplitude of the sinusoidal reference signal and Vc the peak amplitude of the carrier signal.

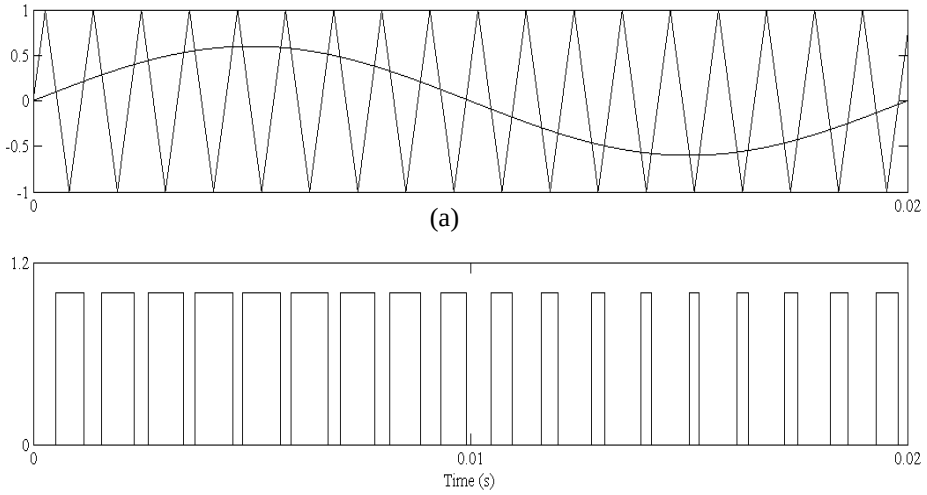


Figure 2.9: (a) The 50Hz sinusoidal reference signal and the 1kHz carrier signal; (b) The SPWM-generated pulse pattern

SPWM techniques have been successfully applied to various three-phase power converters such as multilevel-type converter (GhuoPan & Peng, 2007), AC-DC matrix converter (Zhaoyang, Kun, Minli, & Weiyang, 2008), five-level cascaded H-Bridge (Jayaram, Pramod, & Das, 2012), etc. Dai, Lujara, & Ooi (1992) used SPWM scheme to obtain a stand-alone, unity-power–factor, current-regulated AC-DC converter because its switching harmonics are more predictable and a high-quality current waveform can be obtained at a low switching frequency.

2.7.4.2 Modified Sinusoidal-Pulse-Width Modulation (MSPWM)

Modified sinusoidal-pulse-width modulation (MSPWM) gating signals are generated by dividing a sine waveform (considered a reference signal) into six equal sections with a fundamental frequency (Boost & Ziogas, 1988; Pouliquen et al., 1994). Generation of a modified SPWM is as illustrated in Figure 2.10. The reference signal to the 0° to 60° and 120° to 180° sine waveforms are compared with two types of carrier signals (M-shaped and W-shaped) (Green et al., 1997), to generate the modulated PWM patterns. The output (pulse) of the MSPWM is high when the reference signal has a magnitude higher than the carrier signal's; otherwise, it is low.

The PWM patterns at the 60°-120° section are obtained by "folding" the pulses of the 0°-60° and 120°-180° sections (Boost & Ziogas, 1988); the PWM patterns are high pulse whenever the modulated patterns of the 0°-60° and 120°-180° sections are high (as illustrated by Figure 2.11). Some research assumed the signal pattern at this section to be a high pulse because it is nearer to the peak of the sine wave, which indicates no significant change to the pulse width with variations to sinewave amplitude (Alias, Rahim, & Hussain, 2013; Raihan & Rahim, 2010). The technique is popular in three-phase AC-DC buck-type converters.

MSPWM technique provides a substantially higher AC/DC gain than does SPWM technique (Boost & Ziogas, 1988). The hardware implementation of an MSPWM modulator, however, is more complex than that of SPWM.

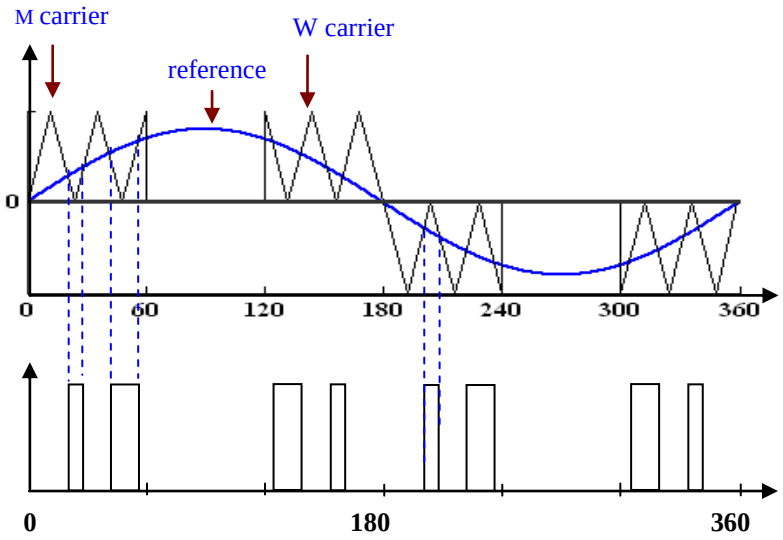


Figure 2.10: Illustrating generation of MSPWM pulse pattern

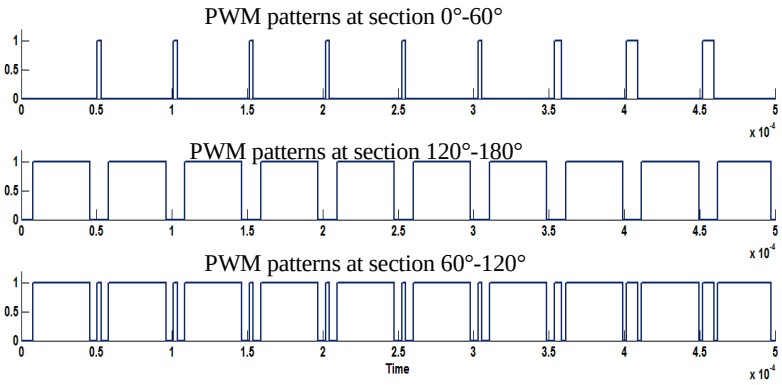


Figure 2.11: Generating pulse patterns at the 60°-120° section

2.8 Feedback Control Techniques for PWM Strategy

Feedback control is usually required in the PWM strategy of an AC-DC power converter to control the power factor correction (PFC) and regulate the output DC voltage. Its basic characteristics in PWM strategy are as follows; PFC control strategy is obtained by adjusting the lagging and leading power factors of the reference to unity displacement power factor; the output DC voltage is regulated by adjusting the modulation index M.

Feedback control techniques for PWM AC-DC converters can be classified into two categories, namely model-based and non-model-based as shown in Figure 2.12. Model-based controllers are well-established and widely used in industry. The technique requires a precise mathematical model and its design procedure is systematically structured. The control performance is predictable and can be analyzed using analytical tools such as root locus, Bode plot, and Nyquist. Examples of model-based controllers are Proportional-Integral (PI), Proportional-Integral-Derivative (PID), and Sliding Mode Control (SMC).

Non-model-based controllers do not require a mathematical model thus has grown popular and more accepted by industry. Their drawbacks include the lack of a standard design procedure, unpredictable performances, and difficult optimization. Fuzzy Logic and Neural Network are common examples of non-model-based controllers.

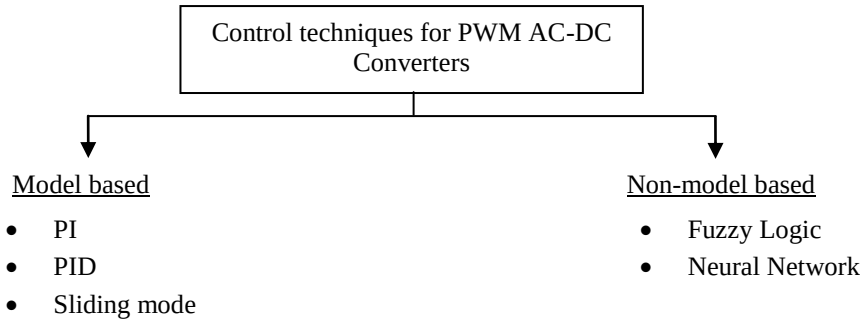


Figure 2.12: Classification of feedback control techniques

2.8.1 Proportional-Integral Controller

Proportional-Integral (PI) is implemented in AC-DC power converter applications (Blasko & Kaura, 1997; Cichowlas & Kamierkowski, 2002; Guo, Lin, & Zheng, 2005) to regulate the output voltage/current and eliminate the steady-state error for its well-known simplicity and ease of implementation. PI is usually configured in cascade with the plant (see Figure 2.13), implemented in either analog or discrete. It requires two gains (proportional (K_P) and integral (K_I)), and needs proper tuning to obtain the required output. Poor tuning produces an unsatisfactory output response. PI is able to produce the desired transient response when the changes in disturbance or reference are small (because the change is still close to the design operating system), but not so with large changes. A derivative term is then needed to improve the transient response.

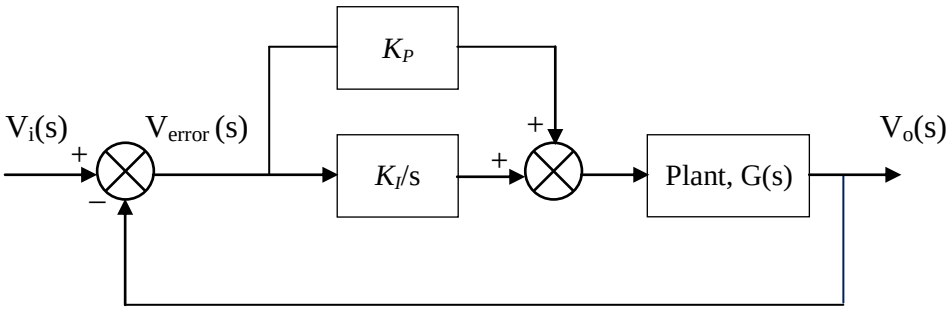


Figure 2.13: PI controller

Proportional-Derivative (PD) improves transient response through fast settling time and small overshoot. The configuration of a PD controller and a plant is as shown in Figure 2.14. Having two gains (proportional (K_P) and derivative (K_D)), it needs proper tuning to obtain the desired output. PD controllers have two major drawbacks: an active circuit is required to perform the derivative term, and the differentiation process is noisy (in high frequencies they produce unwanted signals or saturate the amplifiers).

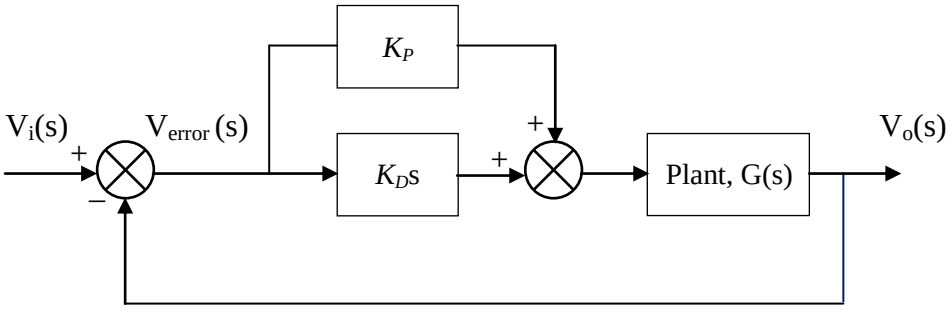


Figure 2.14: PD controller

2.8.2 Proportional-Integral-Derivative Controller

Proportional-Integral-Derivative (PID) overcomes the limits of PI and PD controllers. A combination of proportional, integral, and derivative terms, it is implemented in many industrial applications for its well-known simplicity and robustness: in, power converters, motor control, hybrid electric vehicle, etc. (Armstrong, Neevel, & Kusik, 2001; Huang & Han, 2002; Soebagia, Yoshida, Murai, & Lipo, 1996). Satisfactory performance can be achieved in many linear or nonlinear systems by proper tuning of the PID controller parameters/gains, i.e., proportional gain (K_P), integral gain (K_I), and derivative gain (K_D) (Dorf & Bishop, 2005; Nise, 2008).

A common PID configuration is the cascaded configuration shown by Figure 2.14. This type of controller is very popular owing to its simple design procedure and easy implementation (either analog or digital).

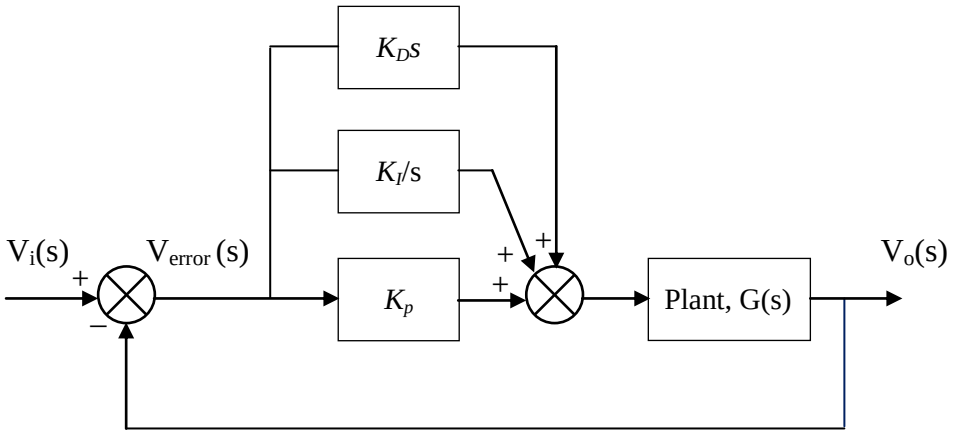


Figure 2.15: Cascaded PID controller

A PID controller has the following transfer function (Dorf & Bishop, 2005):

$$G_{PID} = K_P + \frac{K_I}{s} + K_D s \tag{2.2}$$

Rearranging Equation 2.2,

$$G_{PID} = \frac{K_D(s^2 + as + b)}{s} = \frac{K_D(s + z_1)(s + z_2)}{s} \tag{2.3}$$

where $a = K_P/K_D$ and $b = K_I/K_D$. Equation (2.2) shows the PID controller having one pole at the origin and two zeros (the location is valid for as long as the closed loop poles located in the left-hand-side of the *s*-plane).

Optimum performance of the PID controller depends on good tuning of its K_P, K_I, and K_D. Several tuning methods have been designed, such as Ziegler-Nichols (Meshram & Kanojiya, 2012; Yadaiah & Malladi, 2013), and pole-placement (Bae, Yang, Lee, & Cho, 2007; Yousefi, Emami, Eshtehardiha, & Poudeh, 2008).

Ziegler-Nichols First Method tuning table (Table 2.2) is referred to for easy obtaining of PI, PD, and PID controller gains. The table was obtained through the response curve shown by Figure 2.16. This tuning method is simple but less popular because it limits the controller's usability and does not optimize the controller's performance.

Table 2.3: Ziegler-Nichols First Method tuning table (Meshram & Kanojiya, 2012)

Controller Type	K_P	T_I	K_D
P	T/L	-	-
PI	0.9T/L	L/0.3	-
PID	1.2T/L	2L	0.5L

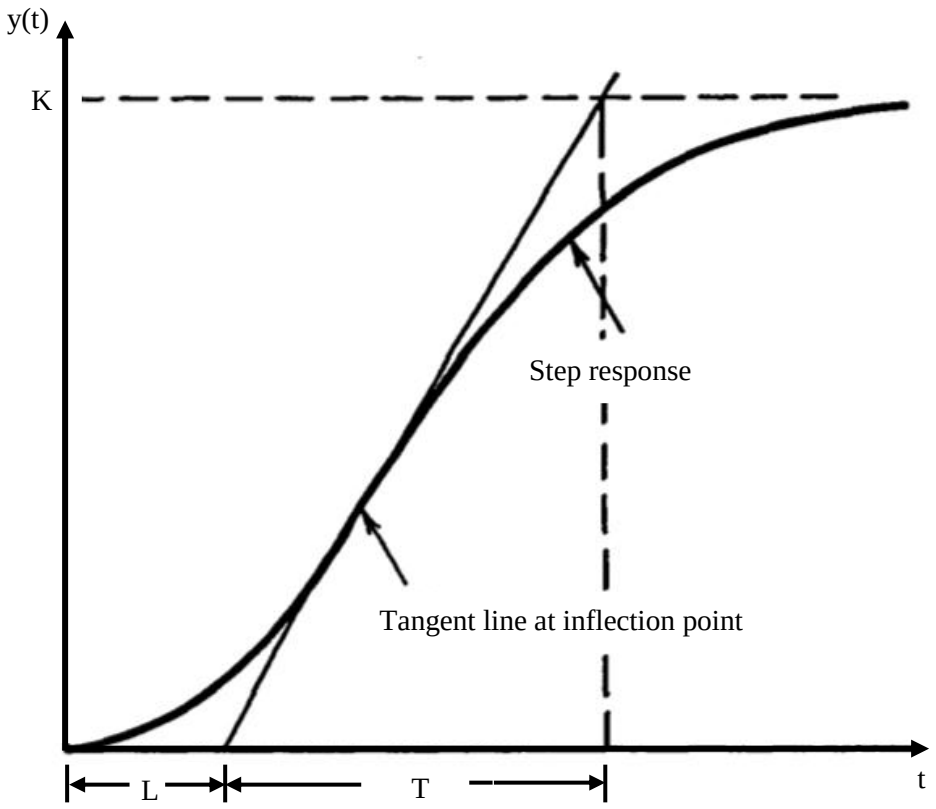


Figure 2.16: The response curve of Ziegler-Nichols method

Pole-placement method is useful in low-order systems (i.e., first-order and second-order systems). The PID controller's gains are obtained by determining the location of the closed-loop poles (Yousefi et al., 2008). This method has a drawback in handling higher order systems but it can still be used if the dominant second-order pair of the closed-loop poles is five times farther than the other system poles. Its basic concept is to find the PID controller's gains on the specified natural frequency ω_n and damping ratio ξ.

In practice, a cascade PID controller produces a set-point kick phenomenon especially when the reference input is a step function. Modified PID such as PI-D, PD-I, or I-D is preferred to avoid the set-point kick phenomenon.

2.9 Conclusion

This chapter reviews switch-mode AC-DC converters. There are two types of switch-mode three-phase AC-DC buck converters: unidirectional and bidirectional. Their switching and modulation techniques depend on application. Especially in three-phase AC-DC buck-type systems, modified SPWM is the technique to be explored. Feedback control techniques ensure good dynamic response, and a review of them here shows that the modified PID controllers (such as PI-D, PD-I and I-D) are the best possible because they solve the plant input saturation of cascaded derivative action in conventional PID controllers. PID design procedure is systematically structured, its control performance predictable, and its analysis possible through the techniques of Bode plot, root locus, or state-space.

CHAPTER 3

THREE-PHASE AC-DC BUCK-TYPE CONVERTER: PROPOSED CONFIGURATION AND SWITCHING TECHNIQUE

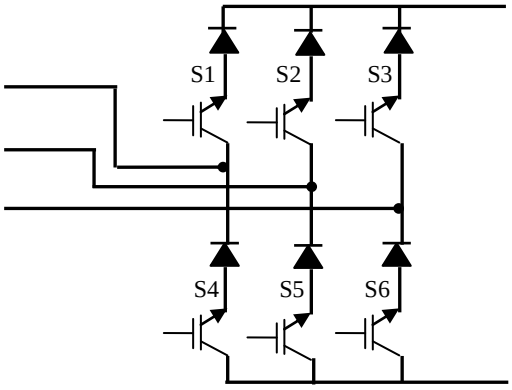
3.1 Introduction

This chapter describes the design and AC-DC/DC-AC operating principles of the proposed bidirectional three-phase buck-type converter. A conventional six-switch three-phase AC-DC buck converter is extended by incorporating four diodes in each switch to achieve bidirectional power flow. The overall circuit configuration comprises inductance and capacitance (LC) input and output filters, six switches, twenty-four diodes and a freewheeling diode/switch. The resonant frequency of the input filter is designed to be much lower than the PWM switching frequency to prevent circuit attenuation. Other related existing circuit configurations for AC-DC buck-type converters are presented as comparison.

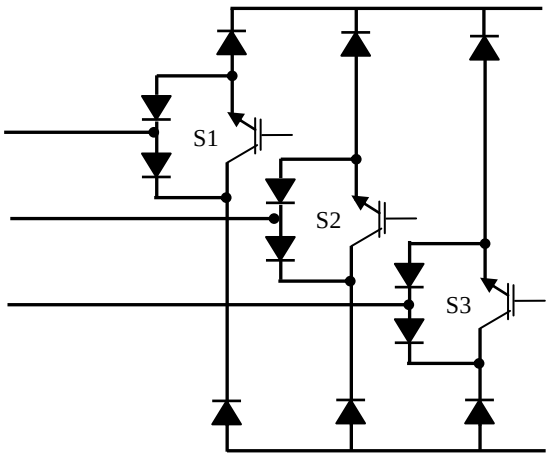
Modified SPWM is the modulation strategy to obtain a near unity power factor, low THD AC currents, and controllable DC output in the proposed converter. The technique uses a look-up table of 60° sinewave as the reference signal and two types of carriers, namely “M” and “W” carriers. A modified SPWM simplification proposed allows it to operate with only one carrier signal, instead of two carrier signals, easing the DSP construction of the gating signals. The proposed simplified voltage-based SPWM will be subjected to a mathematical analysis, a MATLAB simulation, and a DSP implementation, for its verification.

3.2 Three-Phase AC-DC Buck-Type Converters: Proposed Circuit Configuration

Two common configurations of PWM three-phase buck-type AC-DC converters to improve AC mains power quality and DC output are shown in Figure 3.1. Figures 3.1 (a) and (b) respectively shows a conventional 6-switch 6-diode converter (Alias et al., 2013; Green et al., 1997; Milanovic & Slibar, 2011) and a 3-switch 12-diode converter (Nussbaumer et al., 2008, 2006; Omar & Rahim, 2003; Raihan & Rahim, 2010) (which has fewer driver-devices and a simpler PWM switching pattern). These configurations are classified as unidirectional.



(a)



(b)

Figure 3.1: Unidirectional AC-DC buck-type converters: (a) 6-switch 6-diode (b) 3-switch 12-diode

Configurations with bidirectional power flow capability have been studied (Green et al., 1997; J. Rodríguez et al., 2003; Yang et al., 2006; Zargari et al., 2001). The one proposed in this work is shown in Figure 3.2. It modifies a conventional unidirectional 6-switch 6-diode AC-DC buck converter with the incorporation of four diodes in each switch, which realizes bidirectional power flow. It uses 6 switches (S1, S2, S3, S4, S5, and S6), 24 diodes, and a freewheeling diode/switch. S1-S3 are the upper switches and S4-S6 the lower switches. Inductance and capacitance (LC) filters are placed on the AC and DC sides. The circuit configurations for the AC-DC and DC-AC power flows are respectively shown by Figures 3.3 and 3.4.

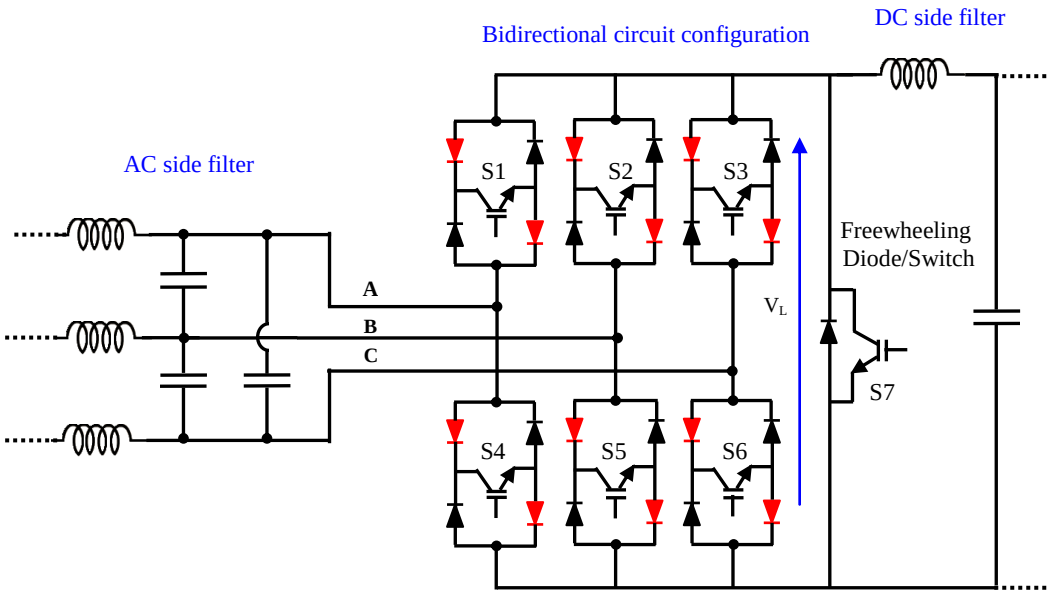


Figure 3.2: The proposed AC-DC buck-type converter with bidirectional capability using six switches plus one switch and diode for freewheeling

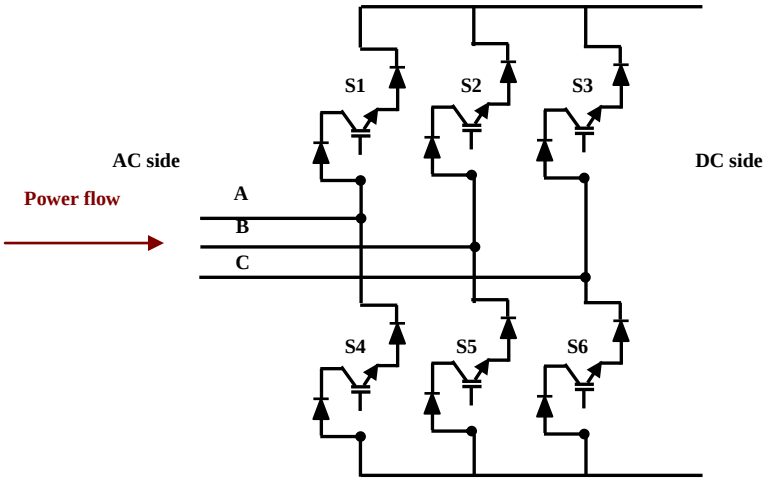


Figure 3.3: The circuit configuration for AC-DC power flow

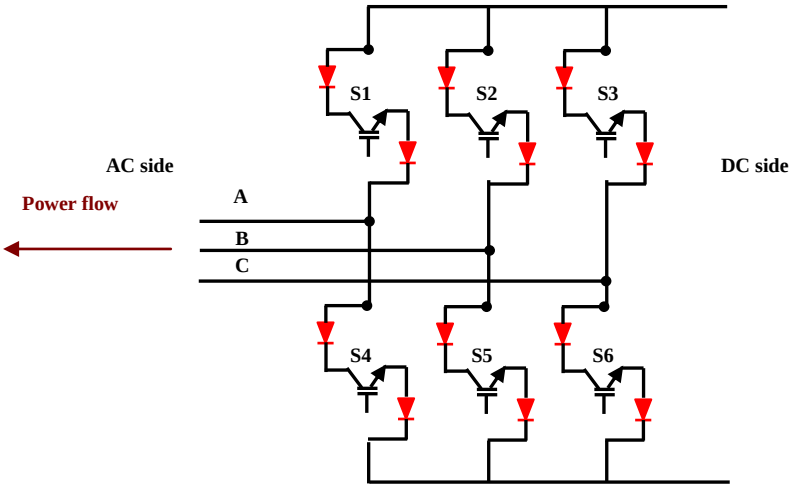


Figure 3.4: The circuit configuration for DC-AC power flow

Table 3.1 compares the proposed AC-DC system with a conventional anti-parallel system and other related AC-DC buck converters (Green et al., 1997; Milanovic & Slibar, 2011; Yang et al., 2006).

Table 3.1: Comparing AC-DC buck-type converters

No.	Features	Conventional anti-parallel	The proposed ac-dc buck-rectifier	(Green et al., 1997)	(Yang et al., 2006)	(Milanovic & Slibar, 2011)
1	Providing bidirectional power flow?	Yes	Yes	Yes	Yes	No
2	Total no. of switches	12 (6 for ac-dc and 6 for dc-ac)	6 (the same are used for ac-dc and dc-ac)	9 (3 for ac-dc and 6 switch for dc-ac)	6 (the same are used for ac-dc and dc-ac)	6
3	No. of diodes	12	24	12	24	6
4	Switching technique	PWM	MSPWM with 1 ref. signal	MSPWM with 2 ref. signals	PWM	IDF PWM
5	Pattern of PWM for ac-dc and dc-ac power flow same or different?	Different	Same	Different	Different	NA
6	Simulation/Hardware	NA	Both	Both	Simulation	Both
7	Employed Feedback control	NA	Yes	Yes	No	No
8	PWM algorithm controller	NA	DSP-TMS320 F28335	FPGA and a microcontroller	NA	FPGA and micro-controller
9	Freewheeling during AC-DC power flow	NA	Diode at dc side	Switching technique using the upper and lower switch of each leg	Diode at dc side	Switching technique using the upper and lower switch of each leg
10	Freewheeling during DC-AC power flow	NA	Switch at dc side	Switching technique using the upper and the lower switch of each leg	Switching technique using the upper and the lower switch of each leg	NA

3.2.1 Operational Principle of the Proposed Three-Phase Buck-Type Converter

The operation of the proposed converter in AC-DC and DC-AC power flows comprises six states (States I, II, III, IV, V, and VI) according to the three-phase supply-voltage waveforms (refer to Figure 3.5). Each state involves three modes of operation: Modes 1, 2, and 3. Modes 1 and 2 are effected by giving to the appropriate switches the modulation patterns of T_a and T_b simultaneously. The modulation pattern of T_a and T_b are produced by comparing the reference signal of 0°- 60° and 120°-180° sine waveforms are compared with two types of carrier signal, M shape and W shape respectively. Three switches activate during Modes 1 and 2; one is "On" while the other two are modulated into T_a and T_b. There will be a situation where both modulating patterns T_a and T_b are "off". Mode 3 is then needed, to provide a path for freewheeling current to flow in the DC side during this situation. The path is created through a freewheeling diode for AC-DC power flow. In DC-AC power flow, S7 is modulated as T_f (the pulses forming upon zero-state, during which neither T_a nor T_b is off simultaneously) to create a freewheeling path. The switch S7 is off (T_{OFF}) during AC-DC power flow because the freewheeling path is created by a diode that connected parallel with S7. The commutating states of the converter switching period T in both the AC-DC and DC-AC operations are the same for S1-S6, as summarized in Table 3.2. The change in mode between the rectifier and the inverter is allowed only when I_L is zero (the charge will be removed from the capacitor) under a condition whereby all switching are on.

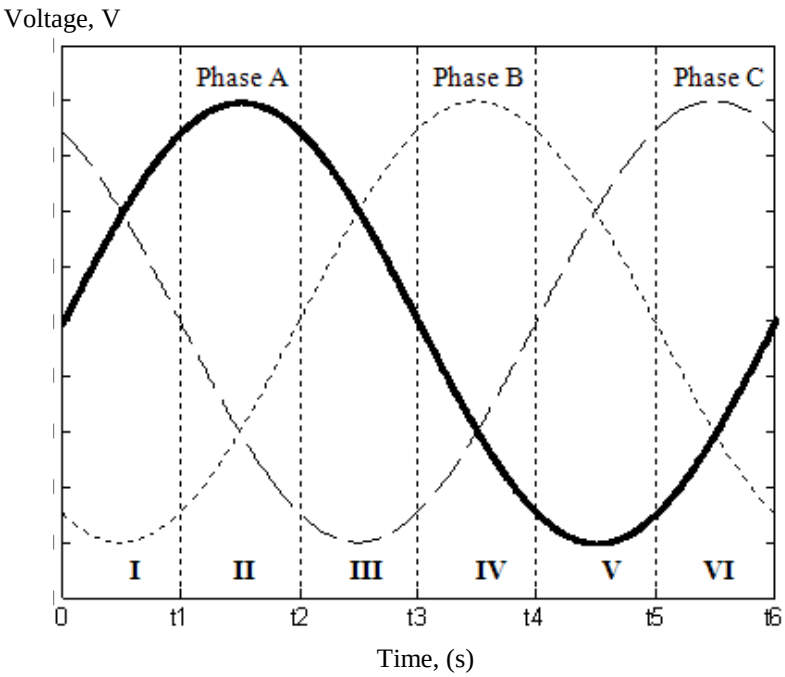


Figure 3.5: Three-phase supply-voltage waveforms divided into six equal states of the 360° mains cycle

Table 3.2: Switching-states of the proposed bidirectional converter during AC-DC and DC-AC power flows

State	AC-DC/DC-AC Power Flow						AC-DC Power Flow	DC-AC Power Flow
	S1	S2	S3	S4	S5	S6	S7	S7
I	T_a	T_{OFF}	T_b	T_{OFF}	T_{ON}	T_{OFF}	T_{OFF}	T_f
II	T_{ON}	T_{OFF}	T_{OFF}	T_{OFF}	T_b	T_a	T_{OFF}	T_f
III	T_b	T_a	T_{OFF}	T_{OFF}	T_{OFF}	T_{ON}	T_{OFF}	T_f
IV	T_{OFF}	T_{ON}	T_{OFF}	T_a	T_{OFF}	T_b	T_{OFF}	T_f
V	T_{OFF}	T_b	T_a	T_{ON}	T_{OFF}	T_{OFF}	T_{OFF}	T_f
VI	T_{OFF}	T_{OFF}	T_{ON}	T_b	T_a	T_{OFF}	T_{OFF}	T_f

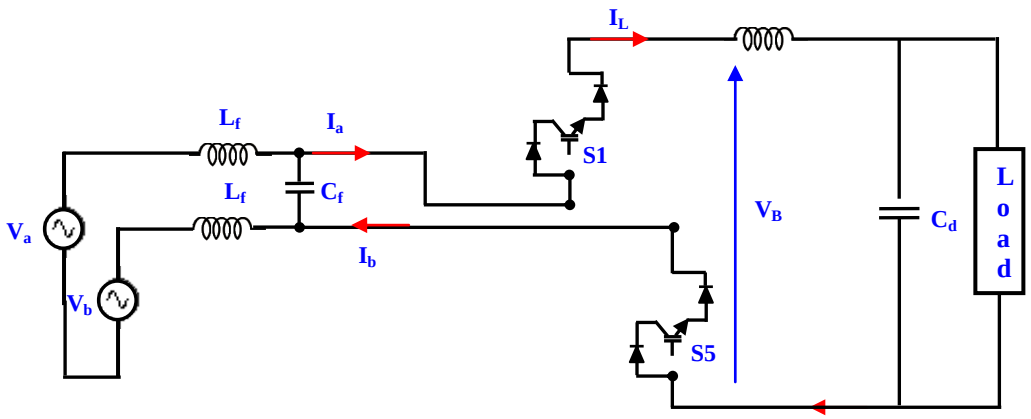
Figures 3.6(a)-(c) are the circuit configurations for AC-DC power flow during Modes 1, 2, and 3 in State I when three-phase input voltages V_a, V_b, and V_c are applied.

The equations of AC currents flow (I_a, I_b, and I_c) and bridge voltage (V_B) during State 1 are determined as follows:

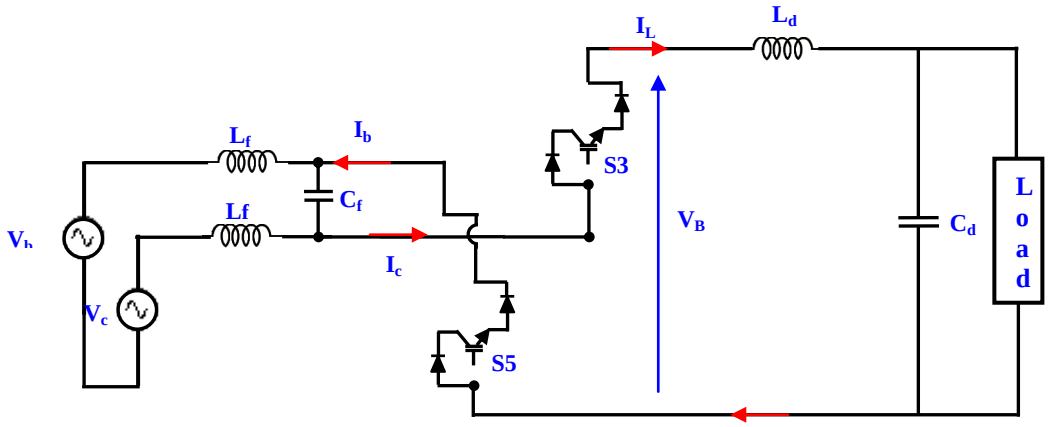
Mode 1:	$I_a = I_L \times M \times T_a$	$I_b = -I_a$	$I_c = 0$	$V_B = V_{ab}$	(3.1)
Mode 2:	$I_a = 0$	$I_b = -I_c$	$I_c = I_L \times M \times T_b$	$V_B = V_{cb}$	(3.2)
Mode 3:	$I_a = 0$	$I_b = 0$	$I_c = 0$	$V_B = 0$	(3.3)

where M is the modulation index, and I_L the inductor (L_d) current on the DC side.

The circuit configurations for DC-AC power flow during Modes 1, 2, and 3 in State I when the DC supply is applied are as shown in Figures 3.7(a)-(c).



(a)



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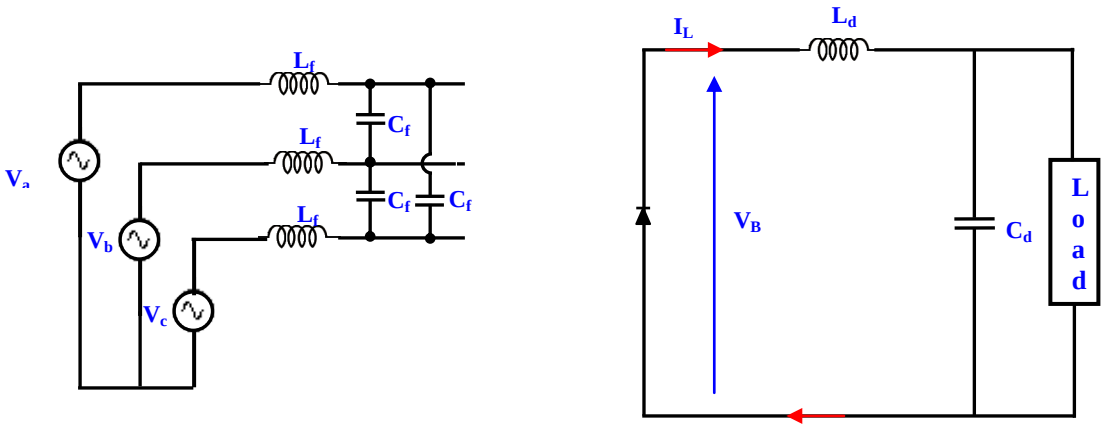
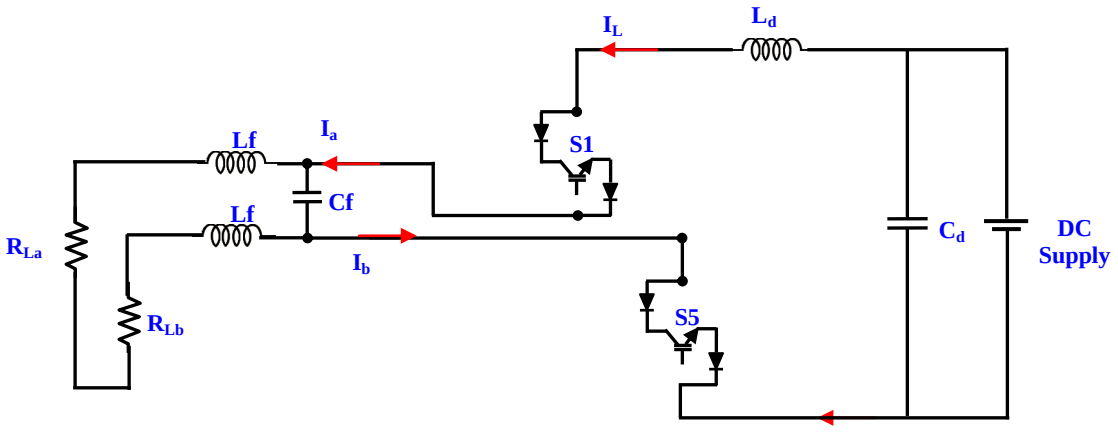
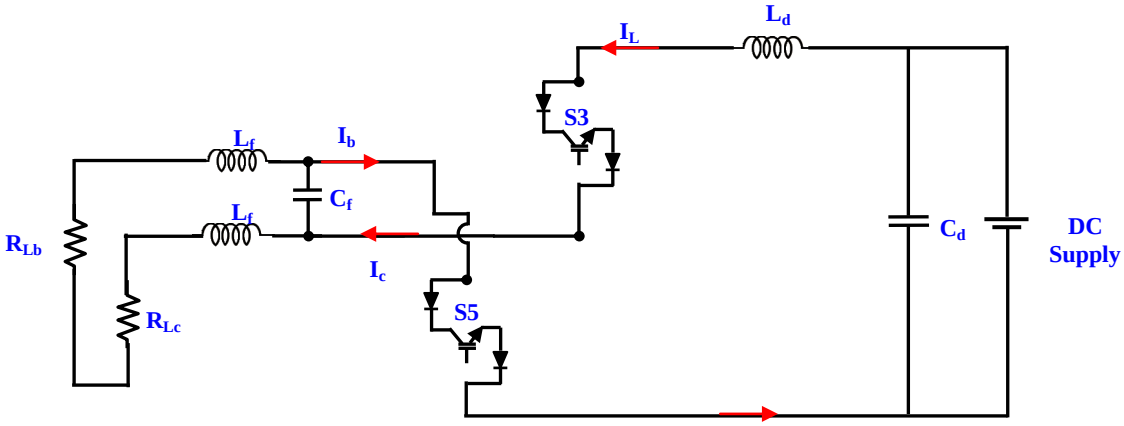


(c)

Figure 3.6: The circuit operation of AC-DC power flow in (a) Mode 1, (b) Mode 2, and (c) Mode 3, during State I.



(a)



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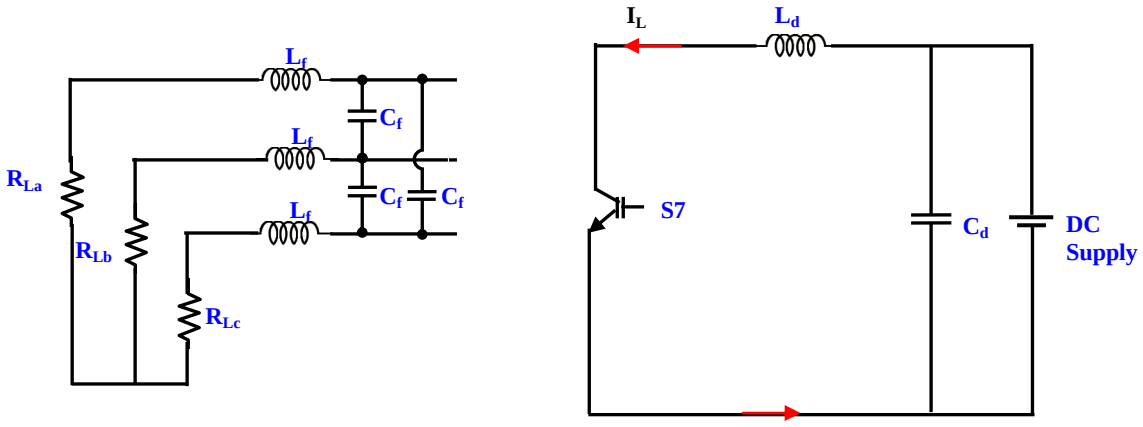


(c)

Figure 3.7: The circuit operation of DC-AC power flow in (a) Mode 1, (b) Mode 2, and (c) Mode 3, during State I.

3.2.2 Mathematical Analysis of AC-DC Buck-Type Power Converter

The mathematical analysis should prove the theory behind the relationship between the bridge voltage (V_B) and the modulation index (M). The input phase voltage and the current waveforms can be expressed in terms of phasors, as follows:

$$V_a = V_m \angle -90° \qquad I_a = I_m \angle (\phi - 90°) \tag{3.4}$$

$$V_b = V_m \angle (-\frac{2\pi}{3} - 90°) \qquad I_b = I_m \angle (-\frac{2\pi}{3} + \phi - 90°) \tag{3.5}$$

$$V_c = V_m \angle (\frac{2\pi}{3} - 90°) \qquad I_c = I_m \angle (\frac{2\pi}{3} + \phi - 90°) \tag{3.6}$$

where V_m is the peak voltage, I_m the peak current, and ϕ the angle between the phase voltage and current or the displacement factor. Through Equations (3.4-3.6), the line-to-line voltage at Section I can be expressed as:

$$V_{ab} = V_m \angle (-90°) - V_m \angle (-\frac{2\pi}{3} - 90°) = \sqrt{3} V_m \angle -60° \tag{3.7}$$

$$V_{cb} = V_m \angle (\frac{2\pi}{3} - 90°) - V_m \angle (-\frac{2\pi}{3} - 90°) = \sqrt{3} V_m \angle 0° \tag{3.8}$$

Averaging the bridge voltage V_B over a switching period T,

$$V_{B(average)} = \frac{V_{ab} T_a + V_{cb} T_b}{T} \tag{3.9}$$

Substituting Equations (3.4-3.9) into Equation (3.10) yields:

$$V_{B(average)} = \frac{3}{2} V_m M \cos\phi \tag{3.10}$$

If the power factor is considered unity,

$$V_{B(average)} = \frac{3}{2} V_m M \tag{3.11}$$

Equation (3.11) shows the bridge voltage (V_B) increased linearly with increased M, proving that the DC output voltage can be controlled through M.

3.3 Theory behind Modified SPWM

Theoretically, modified SPWM gating signals are generated by dividing a sinewaveform (considered the reference signal) into six equal sections (Green et al., 1997) as shown in Figure 3.8. The reference signals of 0° to 60° and 120° to 180° sinewaveforms are compared with two types of carrier signals (M shaped and W shaped) to generate modulated PWM patterns. If the reference signal is greater than the carrier signal, the pulse is "ON", else the pulse is "OFF". The reference signal 90° to 120° (nearer the peak of the sinewave and which indicates no significant change to the pulse width against variations to the sinewave amplitude) is assumed to generate an "ON" pulse.

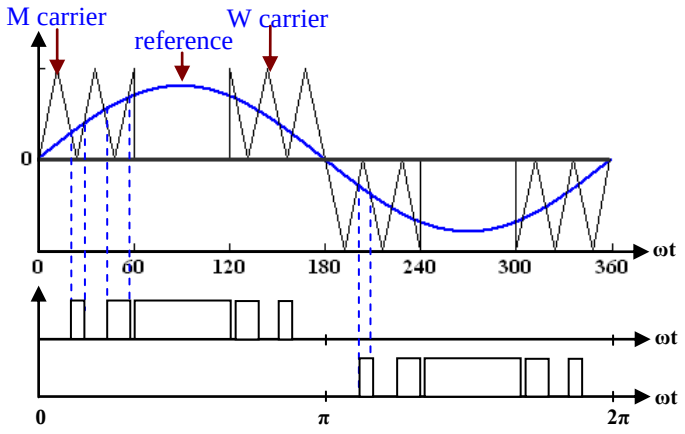


Figure 3.8: Generating the modified SPWM signal

Figure 3.9 shows the three-phase voltage waveforms (the reference signals) of 50Hz and their six equal states (I-VI). Each state shows a similar pattern, so analysis will

focus on State I only. The reference signals A, B, and C respectively represent the input phase voltages V_a, V_b, and V_c. The modulated PWM patterns, namely T_a and T_b, are produced by comparing the reference signals (A and C) with the triangular carrier signals ("M" and "W"), as discussed in [6-8]. The mathematical equation of the modulation patterns T_a and T_b between 0° and 60° are given by:

$$T_a = T \times M \times \sin(\omega t + \varphi) \tag{3.12}$$

$$T_b = T \times M \times \sin(\omega t + \varphi + \frac{2\pi}{3}) \tag{3.13}$$

where T is a switching period of the triangular carrier signal and M the modulation index (0<M<1).

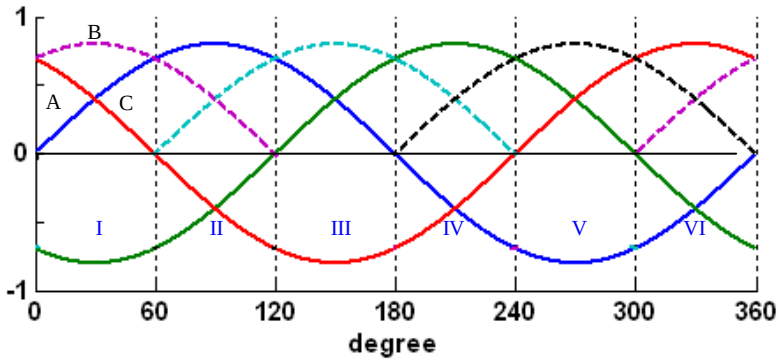


Figure 3.9: The six-states of the three-phase supply waveforms showing identical patterns

3.4 Simplified Voltage-Based SPWM

A simplified voltage-based SPWM is proposed to generate the gating signals. It uses only one carrier signal, instead of two carrier signals, simplifying construction of the gating signals in the practical implementation.

Theoretically, the modulated PWM patterns (T_a and T_b) are produced by comparing the reference signals (A and C) with the triangular carrier signals ("M" and "W"). T_b is modulated by mirroring the positive and negative sides. The C reference (section I) and the "W" carrier signal are inverted to be on the negative side (as shown in Figure 3.10), creating an "M" shaped carrier signal. The comparison process is a reverse, i.e., the pulse is "ON" if the reference signal is bigger than the carrier signal, producing similar pulses as in the original method. The simplified concept is proven digitally by a mathematical approch. The lookup table of C reference signal is sampled based on the following:

$$C_n = round(P \times \sin(2 \times \pi \times f_1(n_3 + n - 1)/(2 \times f_s))) \quad (3.14)$$

where P is the maximum value of the sinewave signal that equals the peak value of the carrier signal, f_1 the fundamental frequency, f_s the switching frequency, n=1 the number of sample, and n_3 the number of sinewave sample at 120°. For example, P=303, f_1=50Hz, f_s=19.8 kHz, and n_3=264 if the complete sinewave sample is 792. From (3.14), $C_{1,2}$ are 262 and 261. Applying the mirror concept and making the value positive, the new look up table of C reference signal is

$$C_{n(new)} = -C_n + P \quad (3.15)$$

The new values of $C_{1,2(new)}$ are 41 and 42. Referring to Figure 3.11 (a-b), Table 3.3 shows the values of t_{on} and t_{off} pulses on the theoretical and the proposed methods. The mathematical calculation proves that modifying the comparing process to generate PWM T_b produces pulses that have the same pattern as the original. The modification of the PWM T_b is important to enable generation of the modified SPWM in the DSP through the PWM module, as changing the counter every 1/6 of a 50Hz sine-wave cycle is difficult.

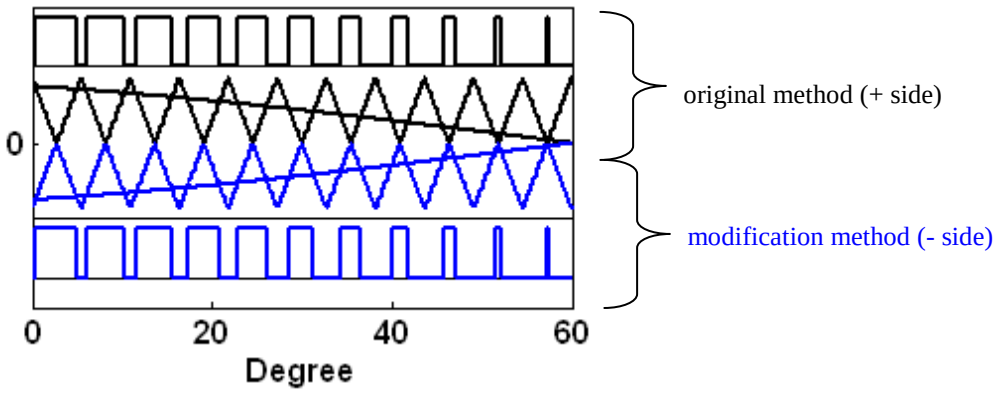
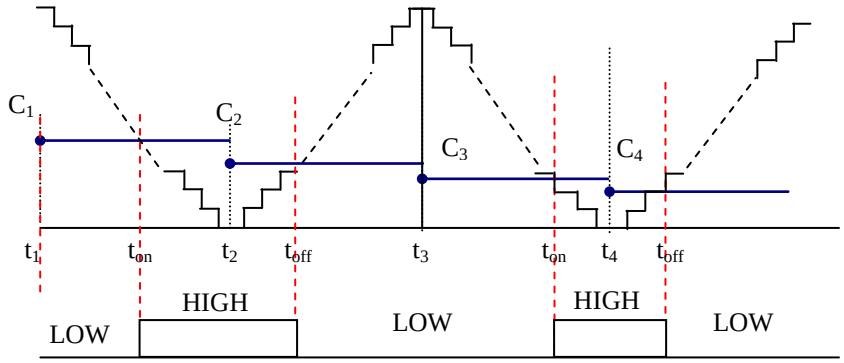
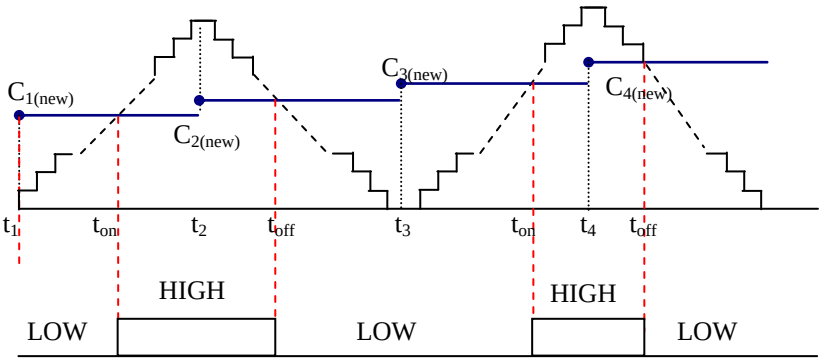


Figure 3.10: Illustrating PWM T_b through the mirror concept (the reference signal is compared with the 'M' carrier signal instead of with the 'W' carrier signal)



(a)



(b)

Figure 3.11: Turn on and off times; (a) the original method, with W type carrier (down-up carrier/counter), (b) the proposed method, with M type carrier (up-down carrier/counter)

Table 3.3: The values of t_{on} and t_{off} pulses

Theoretical Method	Proposed Modification Method
$t_{on} = t_1 - \Delta t_1$ where, $t_1 = t_0 + 1/(2xf_s)$ and $\Delta t_1 = C_1 \times 1/(2xf_s \times 303)$ Therefore, t_{on} = 3.3367ms $t_{off} = t_1 + \Delta t_2$ where, $t_1 = t_0 + 1/(2xf_s)$ and $\Delta t_2 = C_2 \times 1/(2xf_s \times 303)$ Therefore, t_{off} = 3.3804ms	$t_{on} = t_0 + \Delta t_1$ where, t_1 =3.3333ms and $\Delta t_1 = C_{1(new)} \times 1/(2xf_{s\,x} 303)$ Therefore, t_{on} = 3.3367ms $t_{off} = t_2 - \Delta t_2$ where, $t_2 = t_1 + 1/(2xf_s)$ and $\Delta t_2 = C_{2(new)} \times 1/(2xf_s \times 303)$ Therefore, t_{off} = 3.3804ms

3.5 Simplified Voltage-Based SPWM Switching Design in Simulation

The simplified voltage-based SPWM was developed on MATLAB/Simulink. With 19.8kHz switching frequency, 396 triangular carriers (M type) are required to produce a 50Hz main frequency. The 0°-60° reference signal and the altered 120°-180° sinewaveforms (respectively known as Ref A and Ref B) are offline-generated and stored in look-up tables. Ref A and Ref B are compared with the "M" shape carrier to generate the PWM patterns of T_a and T_b, respectively as shown in Figures 3.12 and 3.13.

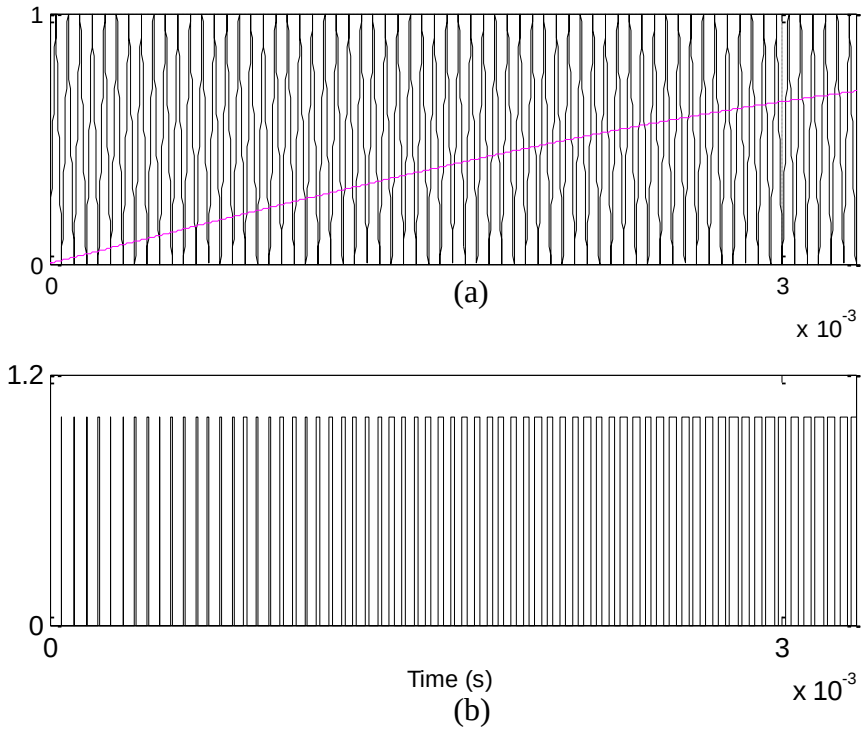


Figure 3.12: (a) Ref A and triangle (“M” type) signals, and
(b) The modulation patterns of T_a

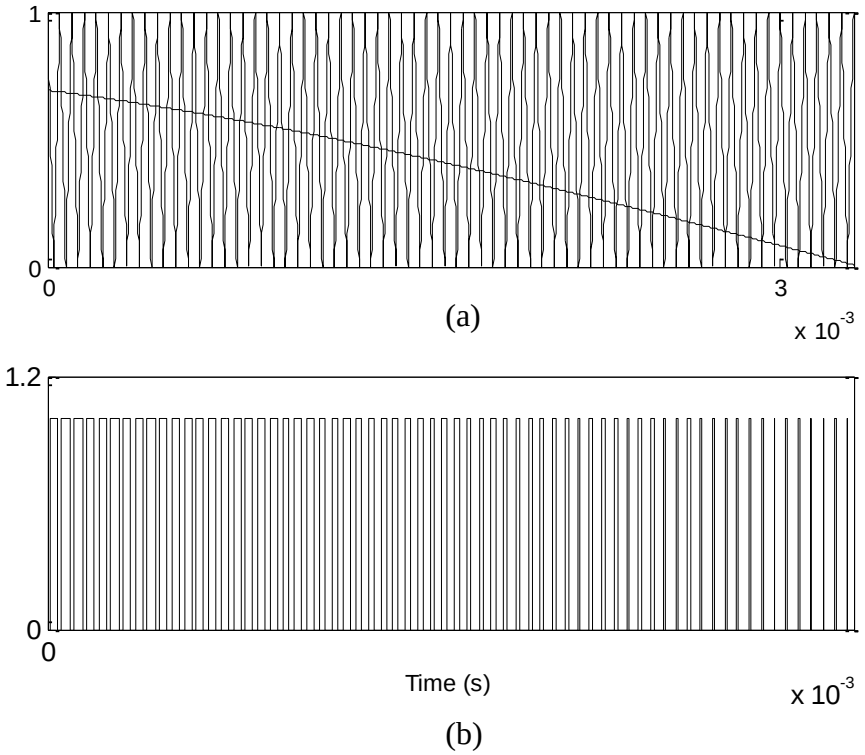


Figure 3.13: (a) Ref B and triangle (“M” type) signals, and
(b) The modulation patterns of T_b

The difference in switching patterns during AC-DC and DC-AC operations can be seen in the construction of the freewheeling path on the DC side. The freewheeling path is needed for the inductor current on the DC side to freewheel when the modulating modulation pattern of T_a and T_b is at zero ("OFF"). In the AC-DC operation, the path is created by adding a freewheeling diode but during the DC-AC operation the path is formed by PWM switching pattern of T_f, which is "ON" when both T_a and T_b are "OFF", as shown in Figure 3.14. In Simulink, T_f is created by using an XNOR gate where T_a pulses and T_b pulses are inputs.

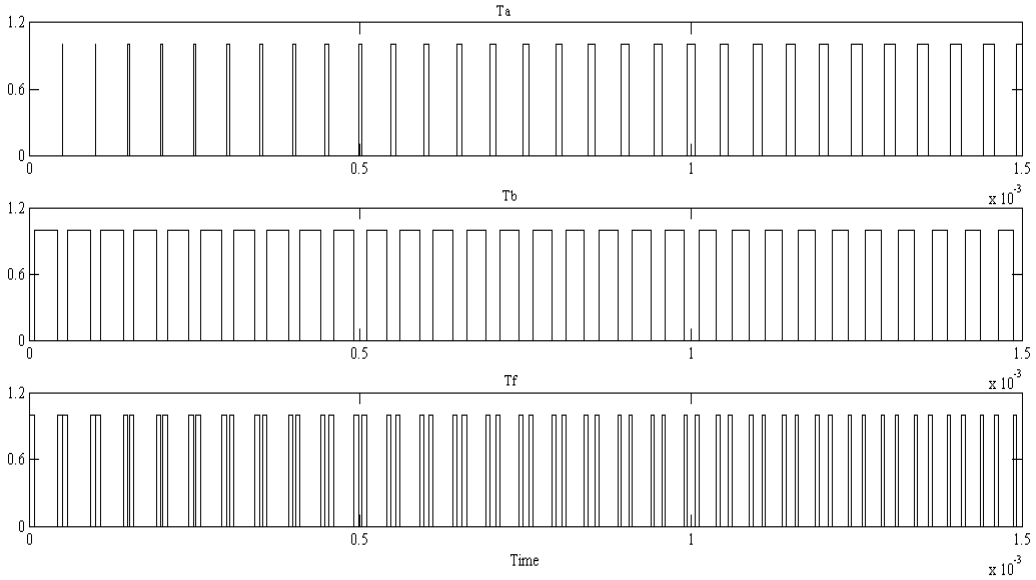


Figure 3.14: PWM patterns of T_a, T_b and T_f.

The process of generating simplified voltage-based SPWM for three-phase buck-type converter during AC-DC and DC-AC operations are summarized in flowcharts (Figures 3.15 and 3.16). The modulation index (M) can be controlled between 0 and 1 by multiplying the value with the sine-wave look-up tables of reference signals.

Figures 3.17 is the MATLAB/SIMULINK subsystem's block PWM A, B, and C respectively to generate PWM T_a, T_b, and "ON" pulse for AC-DC operation. During DC-AC power flow, a subsystem's block Tf is added to create PWM T_f as shown in Figure 3.17. Block OR is then used to combine PWM A, B, and C to generate a 50Hz

switching pattern for each switch (S1 to S6) in the converter. Six states of reference (due to six switching states) are stored in the look-up tables (block repeating table) for comparing between the references and the carrier signals to generate PWM T_a as shown in Figure 3.18; Figure 3.19 shows subsystem block Tf that generates T_f.

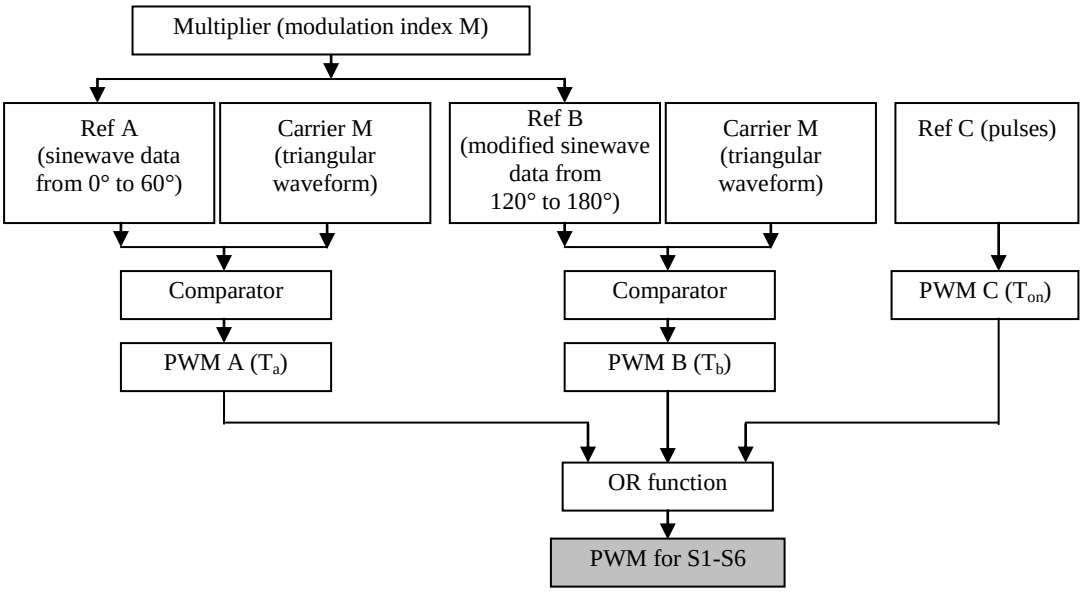


Figure 3.15: The generation process of simplified voltage-based SPWM during AC-DC operation

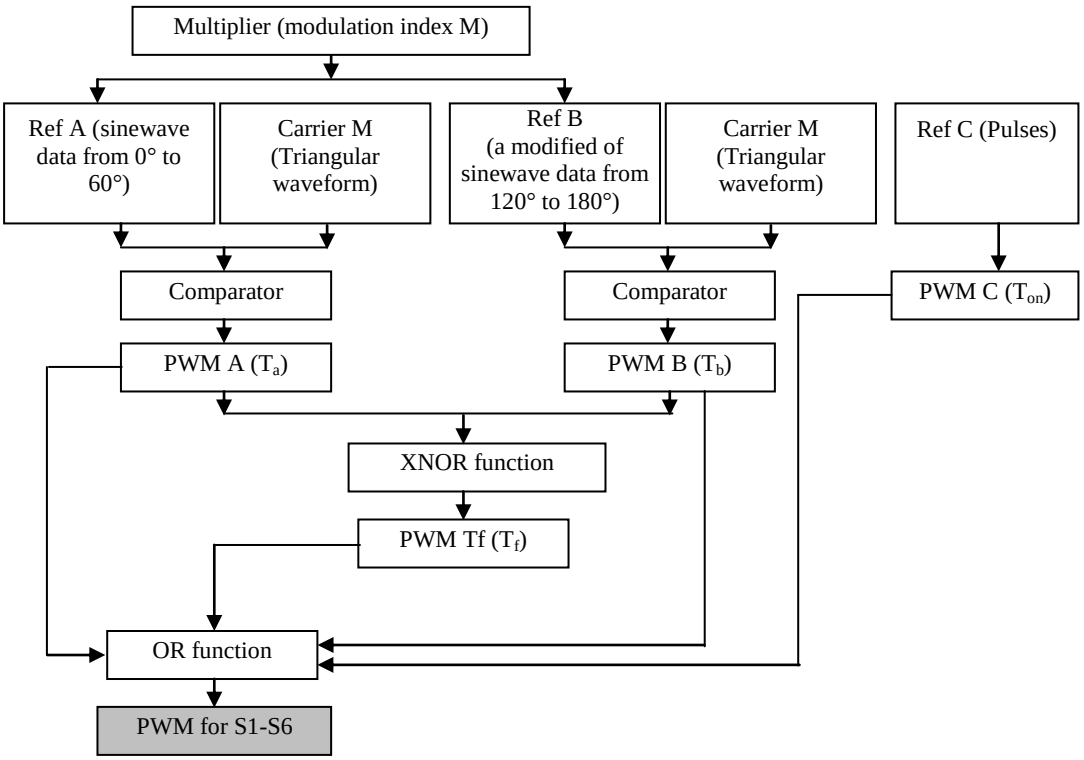


Figure 3.16: The generation process of simplified voltage-based SPWM during DC-AC operation

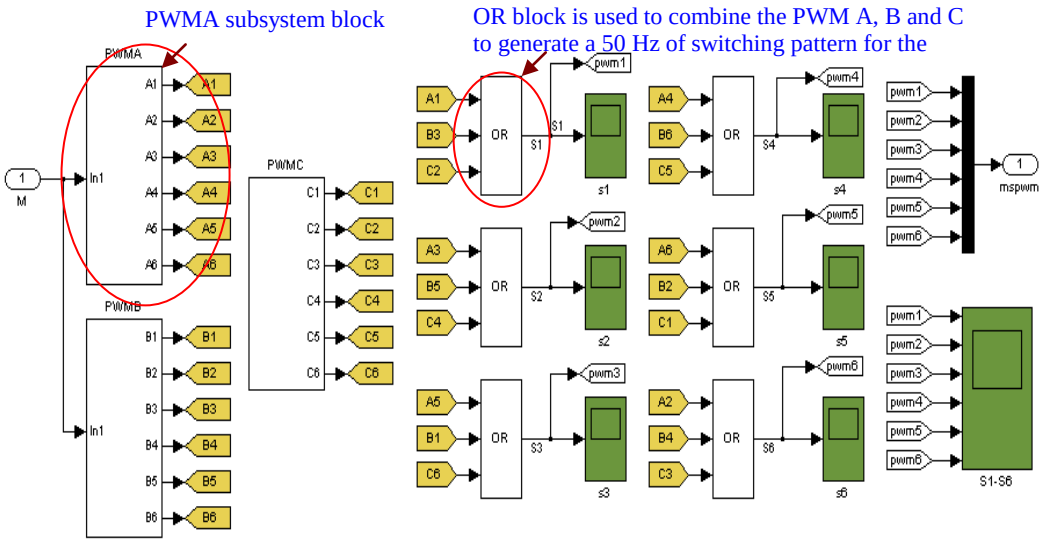


Figure 3.17: Simulink block diagram of the simplified voltage-based SPWM switching during AC-DC operation

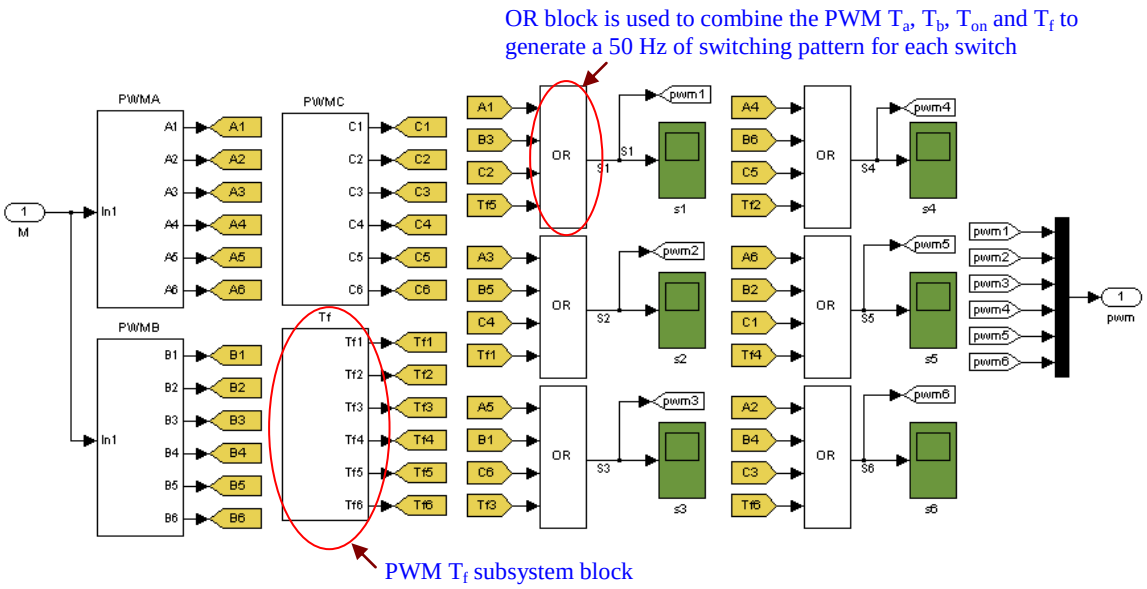


Figure 3.18: Simulink block diagram of the simplified voltage-based SPWM switching during DC-AC operation

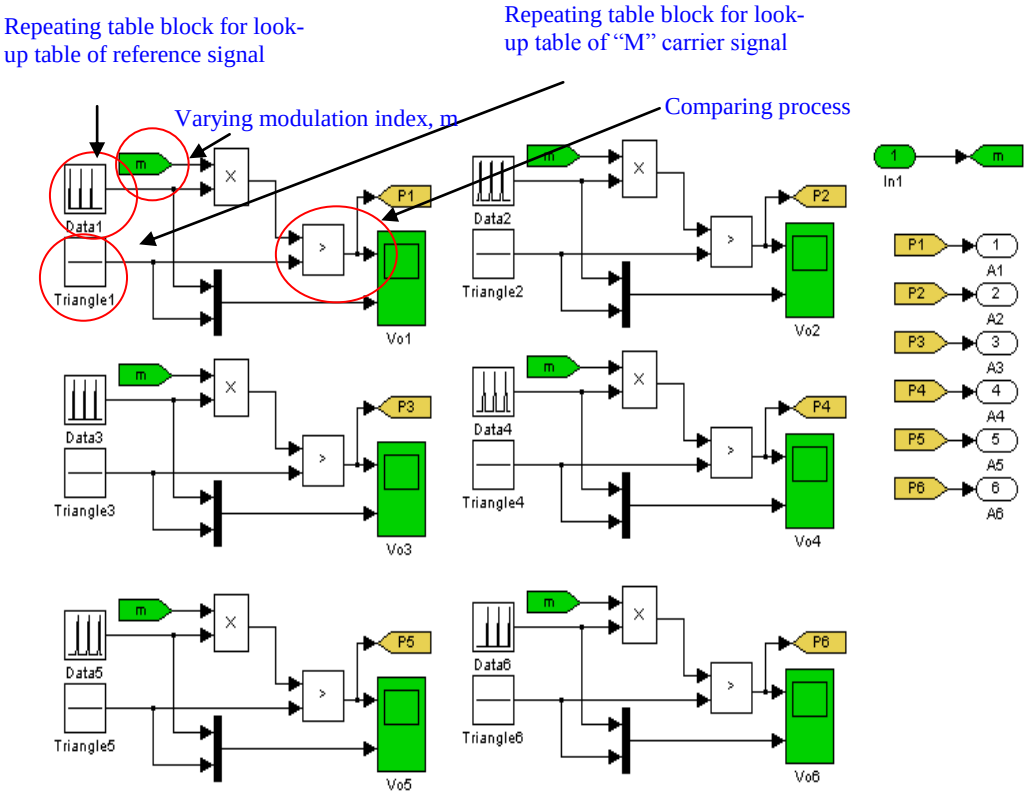


Figure 3.19: The comparison generating PWM A on Simulink

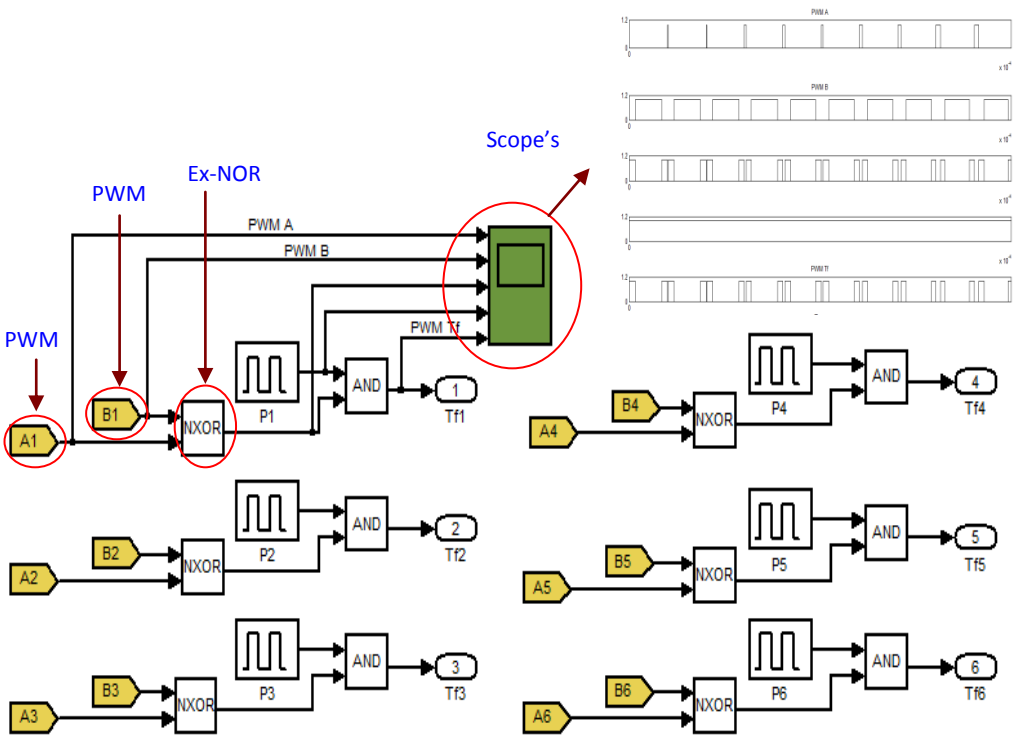
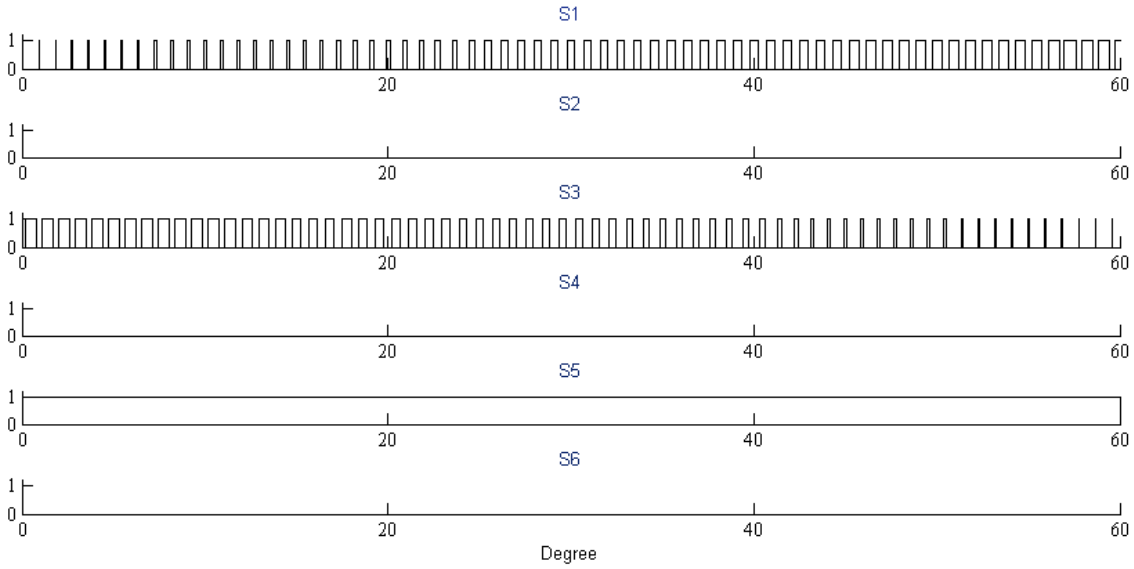
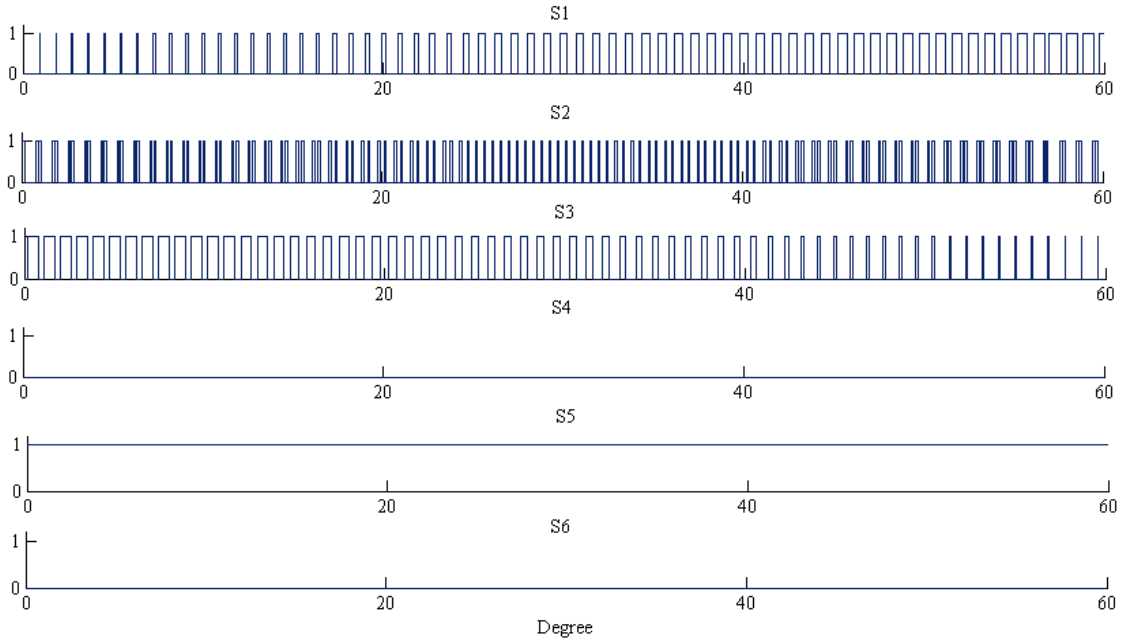


Figure 3.20: Generating the PWM T_f on Simulink

Figures 3.20 (a) and (b) respectively show the pattern of PWM switching appropriate to the switches during AC-DC and DC-AC operations based on the operating principle of the three-phase power converters (Table 3.2) for switching State I (0^{o}-60° sinusoidal signal).



(a)



(b)

Figure 3.21: The PWM pattern (at State I/0°-60°) to appropriate switches (S1-S6) during (a) AC-DC operation, and (b) DC-AC operation

3.6 Simplified Voltage-Based SPWM Switching Design in DSP

The development of microprocessors (DSP and FPGA) allows implementation of high switching frequencies, whose advantage is ripple-free current and a smaller filter on the power converter. Both microprocessors have their own advantages. FPGAs are highly flexible circuits and allow parallel processing. They are thus suitable for designing of the modified SPWM, as proven by Green et al. (1997), Omar & Rahim, (2003) and Raihan & Rahim (2010).

DSP TMS320F28335 was chosen in this work for its fast processing of sampling tasks, its capability to solve mathematical algorithm in developing digital control tasks (through c-coding), and its easy handling of the floating numbers. The board is well designed, equipped with modules such as ADC (Analog to Digital Conversion), enhanced PWM (ePWM), and GPIO. The ePWM module is able to generate complex pulsewidth signals with minimal CPU intervention and was clocked synchronously to enable single-system operation (suitable for 3-phase systems). Reference data is sent to the module, and then PWM is generated. The carrier signal (triangle waveform) is performed by setting either up/down (W type) or down/up (M type) counters. Therefore, a modification of the theoretical technique is required, by the use of two carrier signals to modify the SPWM patterns through the ePWM module of the DSP.

The DSP is equipped with six ePWM modules capable of generating twelve complex pulse-width waveforms with minimal CPU intervention. It is very flexible to use. In this work, three ePWM sub-modules (ePWM1, ePWM2, and ePWM3) controlled the six switches required for the proposed bidirectional topology, and one ePWM sub-module (ePWM4) controlled the freewheeling switch for the DC-AC operation. A look-up-table consisting of 132 sampling data (on 39.6kHz sampling frequency), in turn comprising 1/6 of a 50Hz sinewave signal, was stored in the main source code of the DSP as the reference data of T_a and T_b. The DSP's sampling frequency f_s was 19.8kHz (the

same as the switching frequency), and the sampling time T_s was about 0.0505ms. There were 396 up/down counter per cycle of 50Hz sinewave. An asymmetrical PWM sampling technique used ensured update of the reference data every 0.0253ms (during ZERO and PRD) through module interrupt. The use of asymmetrical technique is important to allow modulation of T_f through the ePWM module.

A GPIO module varied the modulation gain ($0<M<1$). M is multiplied with the reference data of the look-up-table to generate the PWM pulse. For PWM synchronization with the 50Hz AC-voltage line, a simple zero-crossing-detector circuit was connected as the DSP's digital input in the GPIO module. Figure 3.22 is a block diagram of the proposed simplified voltage-based SPWM generator in the DSP. the DSP's clock frequency was defined as 120MHz and reduced to 12MHz through a high-speed peripheral clock prescaler, to generate a 19.8kHz switching/carrier frequency of up/down counter.

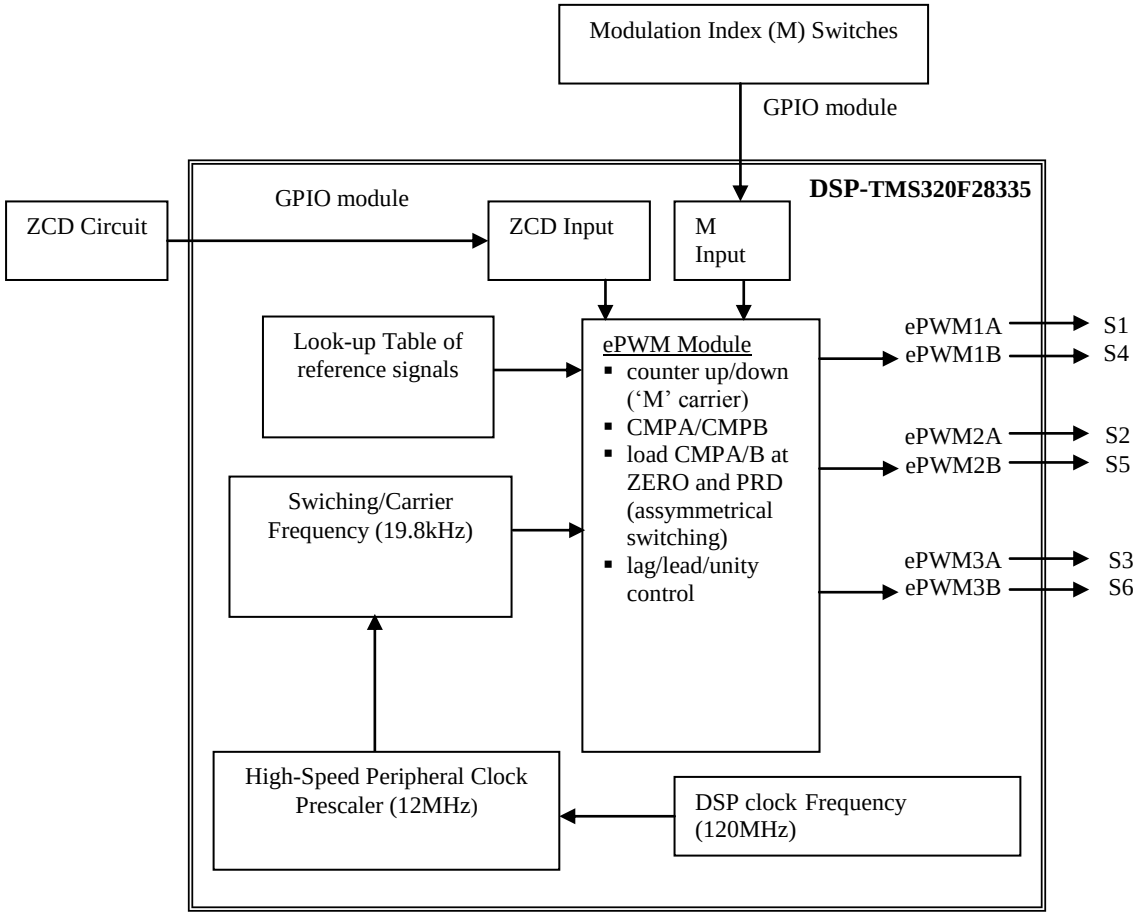


Figure 3.22: Implementation of the simplified voltage-based SPWM developed in DSP

3.6.1 Generating the Look-up Table of the reference signal

The 0 to 60° sinusoidal waveform reference signal was generated on MATLAB and stored as a look-up table to generate the modulated PWM T_a, T_b, and T_f. Asymmetrical switching technique was used so the data updates during zero state (e.g., t_1 and t_3) and maximum state (e.g., t_2 and t_4) of the carrier/counter; see Figure 3.23.

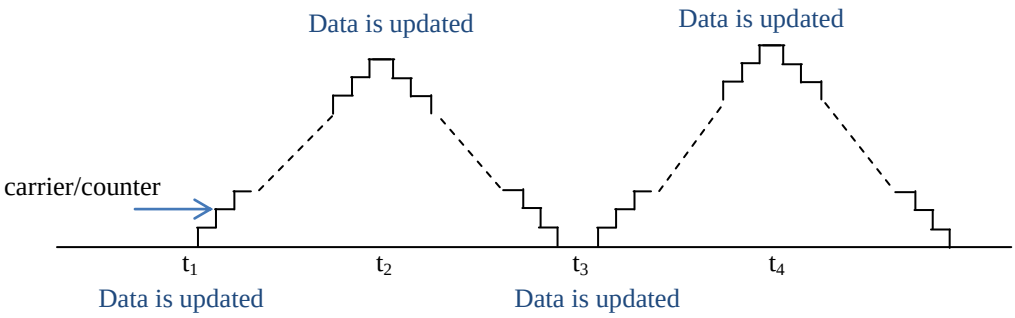


Figure 3.23: Illustration of the asymmetrical switching technique

The maximum state of carrier/counter equals the reference signal's 0 to 60° sinusoidal amplitude. The switching technique was asymmetrical and the counter/carrier frequency was 19.8kHz; 132 look-up table data of the 0 to 60° sinusoidal waveform were thus stored as reference data in the main source code of the DSP (see Figure 3.24). The data of the reference signal (with 50Hz fundamental frequency) can be obtained through (3.16).

$$\text{Data}(n) = A \times \sin(2 \times \pi \times 50 \times t \times n) \tag{3.16}$$

Where, A= amplitude, n = 1, 2, 3, …, 132 and t = 1/(19.8 kHz x 2).

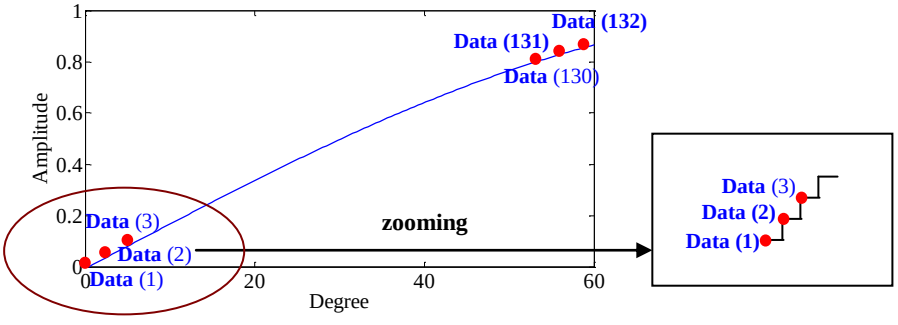


Figure 3.24: The reference signal comprising 132 data

3.6.2 Generating the Simplified Voltage-Based SPWM for the Switches S1-S6

The PWM patterns of simplified voltage-based SPWM (T_a, T_b, T_{on}, T_{off}, and T_f) for switches S1-S6 were similar over a 50Hz cycle. They differ only in their sequence of the six-state switching patterns, in both the AC-DC and DC-AC operations, as shown by Table 3.2. Because of the similarity, the PWM pattern generation in the DSP will be explained for switch S1 only.

Figure 3.25 is the process flowchart for generating the simplified voltage-based SPWM through asymmetrical switching technique for a cycle of 50Hz mains. ZRO and PRD respectively occur when the carrier/counter signal value is zero and maximum (A). The cycle of 50Hz signal consists of 792 reference data, which will be updated during ZRO and PRD as such: PWM1A (i), where i = 0, 1, 2,..., 791. There will be six states of switching pattern (j = 1, 2, 3,…, 6) consisting of 132 data (k = 0 : 132); these will generate the PWM gating signal through the ePWM1A sub-module for S1. The comparator ePWM1A generates a pulse on the condition below:

If PWM1A data > carrier/counter, the pulse is high

The process is repeated after i = 791, and the values of i, j, and k are reset to i = 0, k = 0 and j = 1 for as long as the DSP is running.

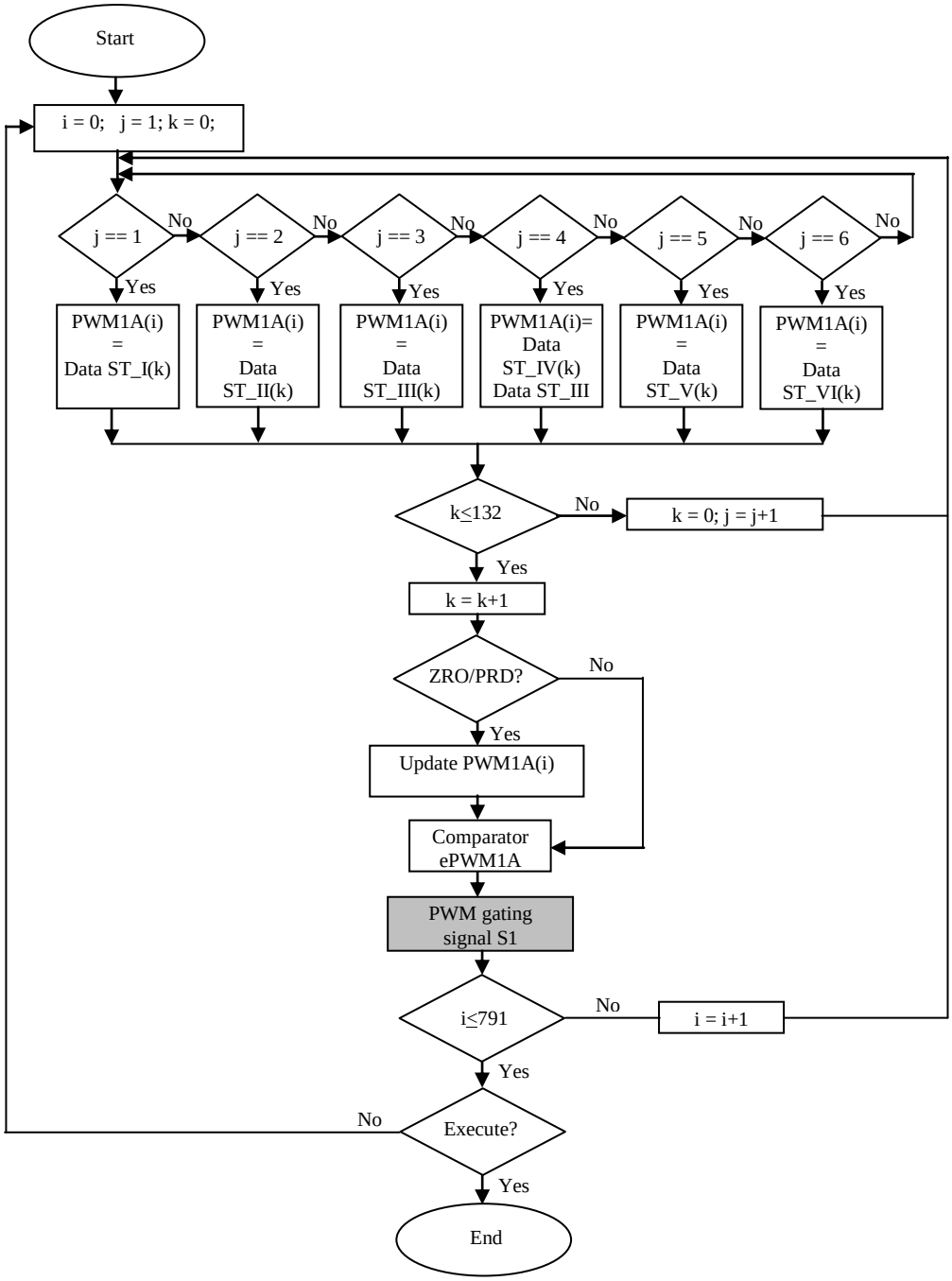


Figure 3.25: The process of generating the simplified voltage-based SPWM signals for S1 through asymmetrical switching technique

Table 3.4 summarizes the values of the reference data (PWM1A) obtained for State I through to State VI: Data ST_I(k), Data ST_II(k), Data ST_III(k), Data ST_IV(k), Data ST_V(k) and Data ST_VI. Data (k) is the look-up-table data, and A is the topmost counter/carrier. Because the clock frequency of the ePWM module is

12MHz, the topmost counter should be 303 to obtain a 19.8kHz switching frequency (counter frequency).

The processes generating the gating signals for the rest of the switches (S2-S6) are similar except for the values of the reference data (they will be referred to as PWM2A for S2, PWM3A for S3, PWM1B for S4, PWM 2B for S5, and so on) and of the ePWM sub-module comparator as shown in Table 3.4.

Table 3.4: The values of the reference data obtained at States I-VI and of the sub-module ePWM, for S1-S6

Upper Switch			
	S1	**S2**	**S3**
Data ST_I (k) =	Data (k)	0	A- Data (132 - k)
Data ST_II (k) =	A	0	0
Data ST_III (k) =	A- Data (132 - k)	Data (k)	0
Data ST_IV (k) =	0	A	0
Data ST_V (k) =	0	A- Data (132 - k)	Data (k)
Data ST_VI (k)=	0	0	A
Sub-Module ePWM	ePWM1A	ePWM2A	ePWM3A
Lower Switch			
	S4	**S5**	**S6**
Data ST_I (k) =	0	A	0
Data ST_II (k) =	0	A- Data (132 - k)	Data (k)
Data ST_III (k) =	0	0	A
Data ST_IV (k) =	Data (k)	0	A- Data (132 - k)
Data ST_V (k) =	A	0	0
Data ST_VI (k)=	A- Data (132 - k)	Data (k)	0
Sub-Module ePWM	ePWM1B	ePWM2B	ePWM3B

Figure 3.26 shows the results of the generated simplified voltage-based SPWM waveforms for half the 50Hz sine-wave cycle via the TMS320F28335 DSP, for switches S1-S4. The modulation index M (from 0 to 1) can be controlled by multiplying with the look-up-table of the reference data. The width of the pulse varies as the modulation index for the PWM patterns of T_a and T_b, as shown respectively by Figures 3.27 (a) and (b).

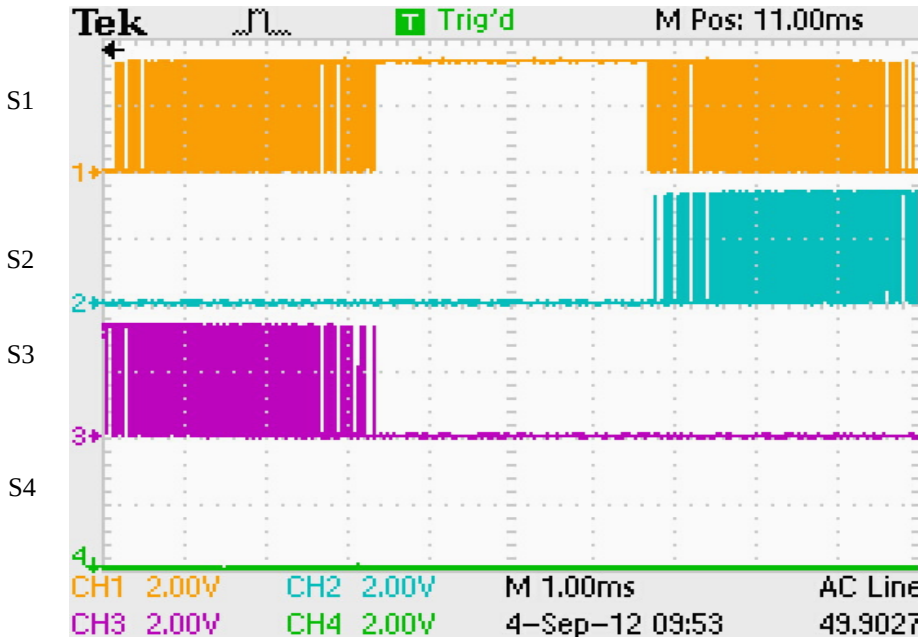
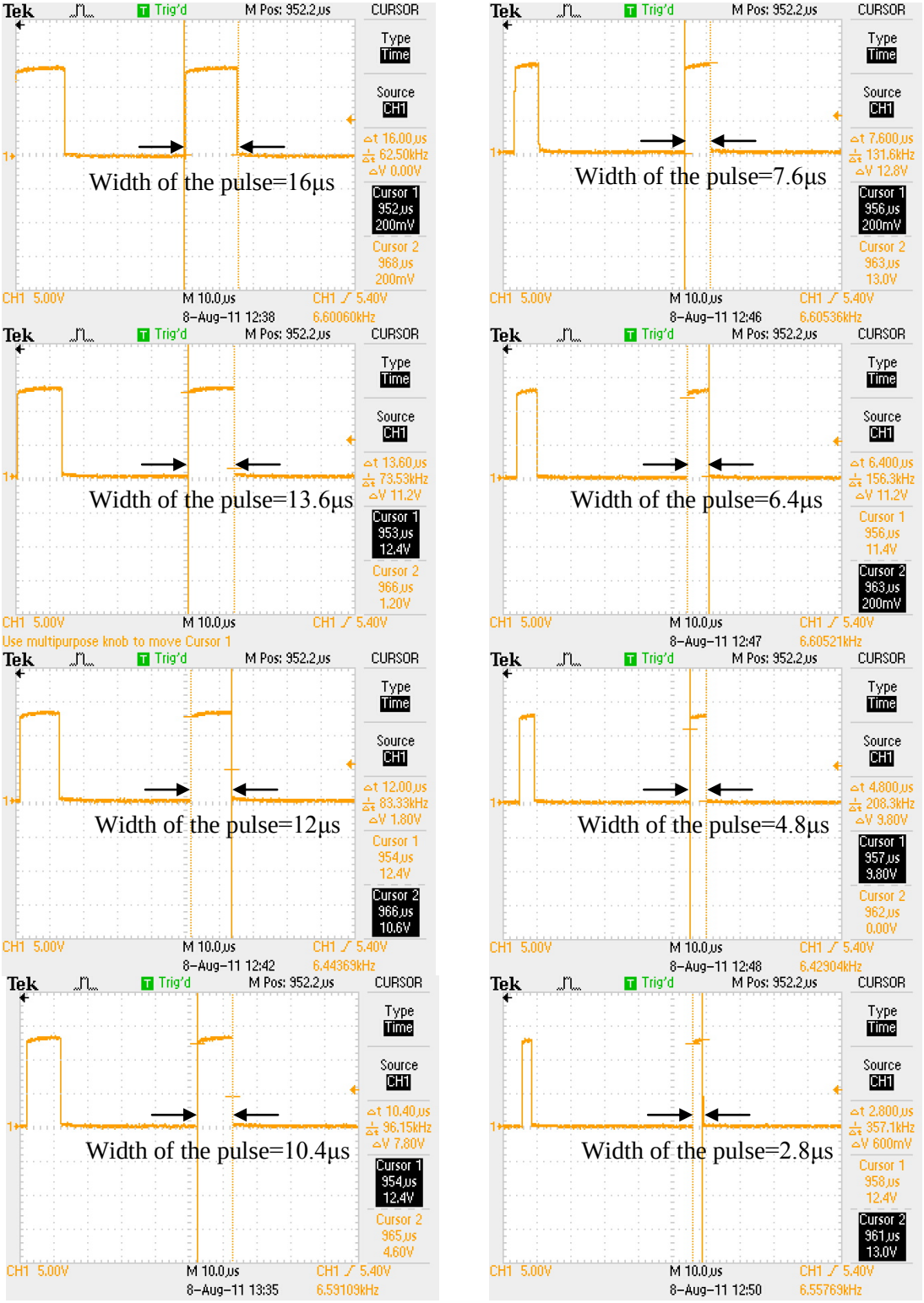


Figure 3.26: The DSP-based simplified voltage-based SPWM for S1-S4 (180° cycle)



(a) (b)

Figure 3.27: The PWM patterns of (a) T_a and (b) T_b, against variations of M

3.6.3 Generating the Simplified Voltage-Based SPWM for the Switch S7

The switch S7 is needed to create a path for the inductor current on the DC side to freewheel when T_a and T_b are not modulating (i.e., zero modulation or "OFF") during DC-AC operation. This path is formed by generating a PWM switching pattern of T_f for S7. In the DSP, T_f is created through an available sub-module such as ePWM4A. Because of the asymmetrical switching technique applied, ZRO and PRD will each occur when the carrier/counter signal value is respectively zero and maximum (A). Two reference data will be updated during ZRO and PRD, namely PWM4A and PWM4B. The pulse is created on the conditions listed in Table 3.5.

Figure 3.28 demonstrates the generation of the T_f pulse. The process flowchart for generating the DSP-based simplified voltage-based SPWM for S7 is as shown in Figure 3.29. The cycle of 50Hz signal consists of 792 reference data. Two data sets will be updated during ZRO and PRD, namely PWM4A (i) and PWM4B (i), where i = 0, 1, 2,..., 791. Data (k) is the look-up-table data, and A is the topmost counter/carrier. The comparator ePWM4A generates the pulses on the conditions listed in Table 3.5. The process is repeated until i equals 791, then the values of i, j, and k are reset to i = 0, k = 1, and j = 1 for as long as the DSP is running.

Table 3.5: The conditions for generating PWM T_f

During UP counter (ZRO)	**During DOWN counter (PRD)**
If PWM4A data > carrier/counter, the pulse will be high, OR If PWM4B data>carrier/counter, the generated pulse is low.	If PWM4B data > carrier/counter, the pulse will be high, OR If PWM4A data>carrier/counter, the generated pulse is low.

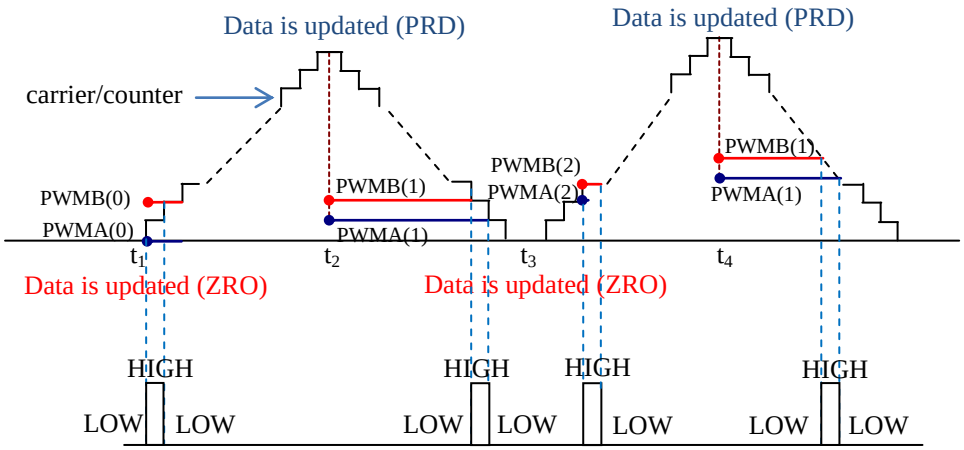


Figure 3.28: Generating the T_f pulses

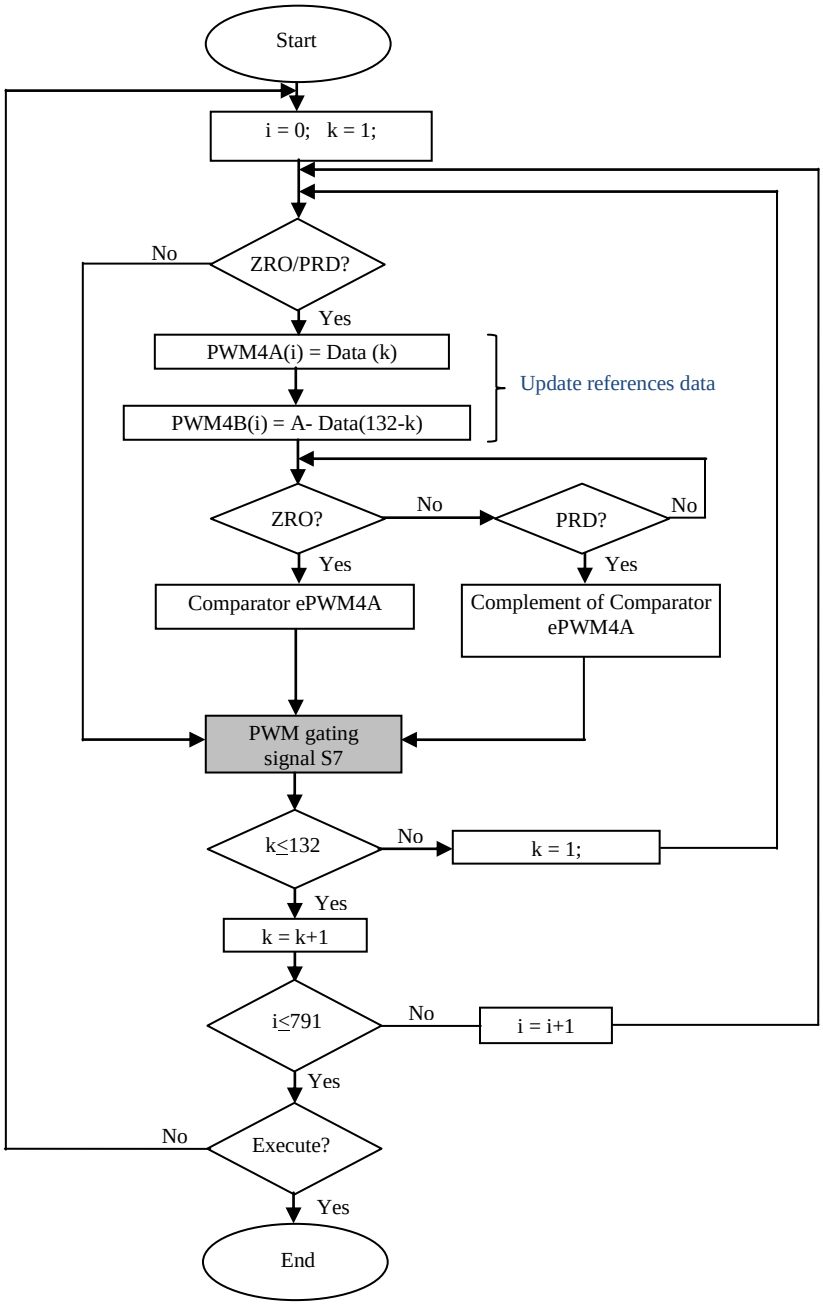


Figure 3.29: The process of generating simplified voltage-based SPWM signals for S7 through asymmetrical switching technique

Figure 3.30 shows the PWM T_a, T_b and T_f waveforms generated by the TMS320F28335 DSP for switch S7. Zooming shows the PWM T_f (bottom) to be "on" when both the PWM T_a (upper) and the PWM T_b (middle) were "off" (zero-modulation state).

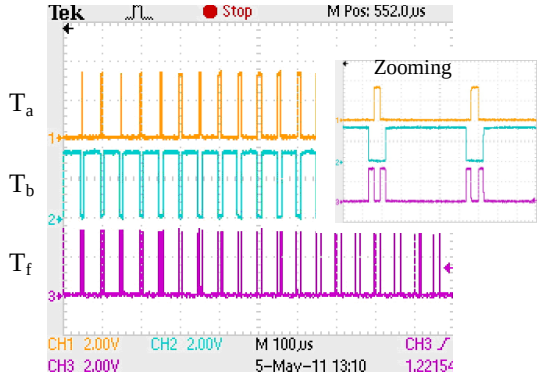


Figure 3.30: The DSP-based simplified voltage-based SPWM for PWM T_a, T_b, and T_f

3.7 Summary

The operational principle of proposed three-phase AC-DC buck-type converter with bidirectional capability have been presented, also the design of the proposed simplified voltage-based SPWM as the switching control for the three-phase AC-DC buck-type converter, which was developed through simulation and validated. The switching control algorithm has been implemented in TMS320F28335 DSP.

CHAPTER 4

FEEDBACK CONTROL DESIGN FOR THREE-PHASE AC-DC BUCK-TYPE POWER CONVERTER

4.1 Introduction

This chapter explains the design and illustrates the importance of the feedback control of the proposed AC-DC buck-type converter. The main objective of the feedback control system is to obtain good voltage response (especially the dynamic response). A mathematical model of the AC-DC buck-type converter system is attained and used as the plant in the design and analysis of the voltage feedback control. The widely-used voltage controls are modeled on conventional cascaded proportional-integral-derivative (PID) and proportional-integral (PI). Cascade derivative action in a forward path in PID control, however, will saturate the plant input. Also, PI control alone does not greatly improve transient response, particularly when the disturbance is large. Modified PID is therefore introduced to avoid set-point-kick phenomena such as PI-D (Proportional-Integral Derivative) and I-D (Integral Derivative).

This work proposes I-D control for AC-DC buck-type converter. A minor loop around the plant contains the derivative (D) compensator, whereas an outer loop (the forward path) contains an integral (I) compensator. This type of I-D controller is categorized as single-degree-of-freedom which is unable to satisfy more than one requirement on output response. More analysis of system performance can be done with more requirements on output responses. A two-degrees-of-freedom configuration is thus

introduced to satisfy two independent requirements (i.e., the response to the disturbance/reference inputs). The control scheme, through the I-D controller, improves the dynamic performance of the transient response.

In designing the proposed controller and the gain tuning, classical transfer function method is used because it allows the specification of a closed-loop zero location, unlike state-space method. This is a disadvantage of state-space method, because zero location affects transient response. A state-space design may also be very sensitive to parameter changes.

A modulation index prediction curve of the closed-loop-pole position (obtained by I-D control model) is also proposed. This improved control algorithm (modulation-index-curve prediction technique) simplifies implementation, reduces the sensor reading dependency (that may contains noises) and minimizes the digital-computation burden on the DSP. The proposed controllers are discrete model developed in MATLAB/Simulink to assist code-writing in C-program for its DSP implementation.

4.2 The Importance of Feedback Control

Simplified-plus-modified SPWM is the switching technique applied to the three-phase AC-DC buck-type converter. It greatly improves the sinusoidal shape of the AC current and the quality of the power factor. The drawbacks of this switching technique in a three-phase AC-DC buck-type converter are the huge (due to the DC filter value) starting current and voltage (transient response) needed upon large step changes to the reference voltage input. There is also significant drop in voltage when the load changes with non-ideal converter elements (most significantly through the ohms resistance of the filter inductors). All these problems can be solved by voltage feedback control.

4.3 The Mathematical Model of the System

A mathematical model, that is used to solve the control problem, can be presented in state space or transfer function. Transfer function is a convenient form for analysis of transient/frequency response, especially in systems that are single-input single-output, linear, and time invariant. The plant's transfer function (G_p) is the ratio of the output voltage to the input voltage (V_o/V_{in}). If the system's transfer function is known, the output or response to various forms of input can be studied.

The derivation of the transfer function is based on the DC-side second-order RLC circuit. The DC bridge voltage (V_B) of the proposed converter is considered the DC power supply (see Figure 4.1). The plant is assumed to be a linear and time-invariant system, $G_p(s)$.

$$G_p(s) = \frac{V_o(s)}{V_i(s)} = \frac{1}{L_d C_d s^2 + R_d C_d s + 1} \tag{4.1}$$

The uncompensated system's step response and root locus are as shown in Figures 4.2 and 4.3 respectively, for L_d=6mH, R_d=0.5Ω, and C_d=220μF. Its open-loop step response was simulated with the open-loop poles located at -41.67 + j869.39, 870.39 $rads^{-1}$ natural frequency, and 0.0479 damping ratio. A very small damping ratio means oscillation and a huge percentage of overshoot in the output voltage of the uncompensated system. A controller is thus needed to change the location of the closed-loop dominant poles so good transient response and zero steady-state error can be achieved.

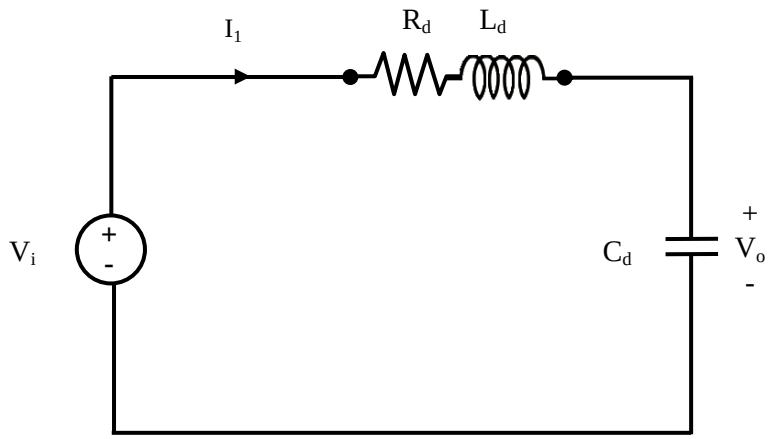


Figure 4.1: The equivalent plant circuit

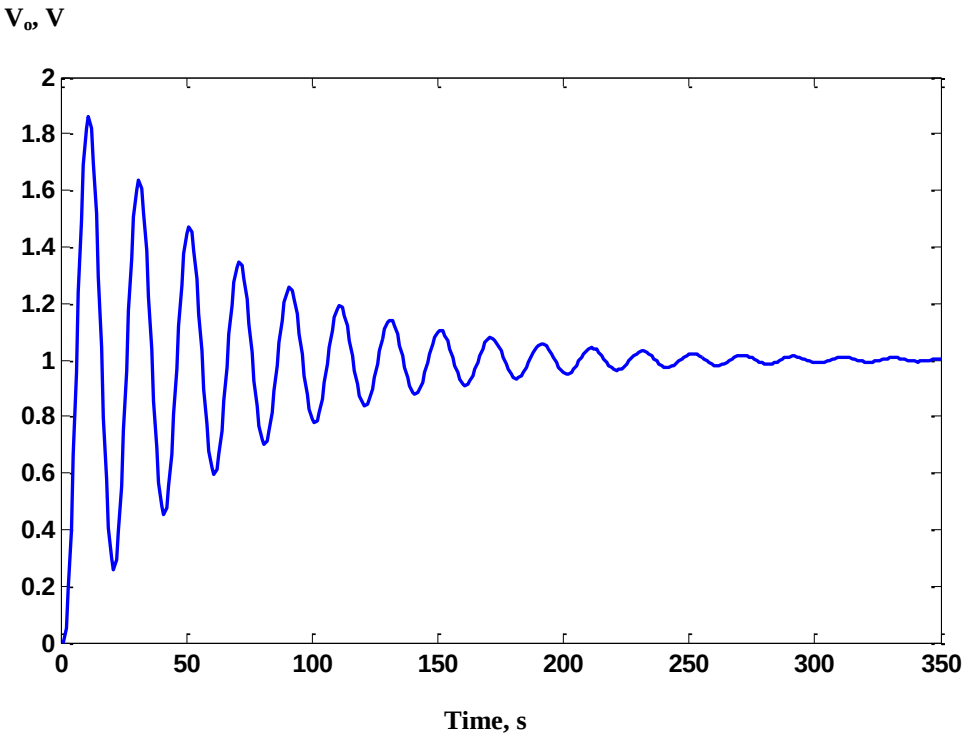


Figure 4.2: The output V_o step response

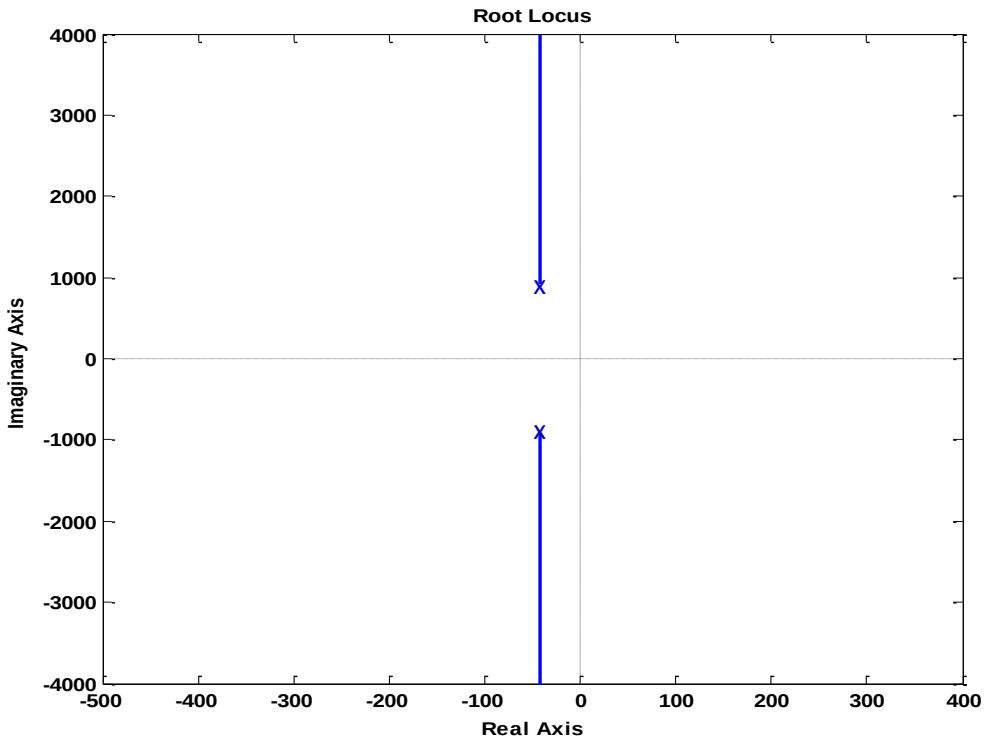


Figure 4.3: The root locus of the uncompensated system

4.4 Integral-Derivative (I-D) Control

The proposed I-D control (as in Figure 4.4) can be categorized as having a single degree of freedom. It has a derivative compensator $G_{C2}(s)$ in a minor loop around the plant and a proportional integral compensator $G_{C1}(s)$ in an outer loop (the forward path). The minor-loop feedback controller is a more suitable implementation than the conventional cascade PID is particularly when there are step changes to the reference input.

This I-D controller uses the single-input-single-output (SISO) concept. Its input and output respectively are the desired/reference (R) and compensated output voltage (Y). The error signal E is a difference between signals R and Y, and will be corrected by the integral action of G_{C1}. The output signal G_{C1} will be a reference signal U_1 for controller

G_{C2}. The manipulated signal U is fed to plant G_p. G_{C1} is an integral controller and G_{C2} a derivative term with a roll-off pole. Their transfer functions are:

$$G_{C1} = \frac{K_I}{s} \tag{4.2}$$

$$G_{C2} = \frac{K_D s}{T_D + s} \tag{4.3}$$

Single-degree-of-freedom control method meets no more than one requirement of the response (i.e., responds to only the reference input). A two-degrees-of-freedom configuration is introduced to analyse the system's performance of two independent requirements such as response to reference input (R) or response to disturbance input (D) as shown in Figure 4.5.

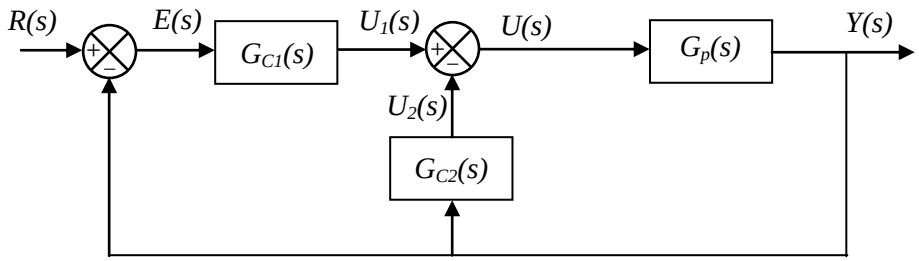


Figure 4.4: The proposed single-degree-freedom I-D control for the AC-DC buck-type converter

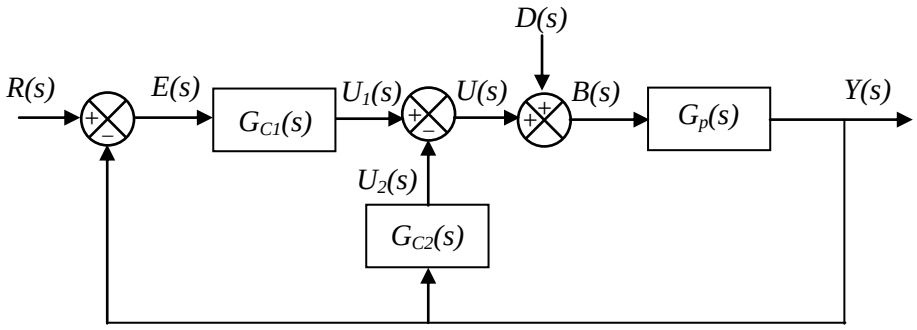


Figure 4.5: The proposed two-degrees-freedom I-D control for the AC-DC buck-type converter

The scheme of two-degrees-freedom voltage control contains a disturbance input D that is summed with the error signal U, a difference between signals U_1 (the output signal of the controller $G_{C1}(s)$) and U_2 (the output signal of $G_{C2}(s)$). The manipulated signal B is then fed to the plant (G_p).

The closed-loop transfer functions subjected to the reference input R and the disturbance input D are obtained independently, whereas $Y(s)/R(s)$ and $Y(s)/D(s)$ are derived when $D(s) = 0$ and $R(s) = 0$, respectively;

$$G_{YR}(s) = \frac{Y(s)}{R(s)} = \frac{G_{C1}G_P}{1 + (G_{C1} + G_{C2})G_P} \tag{4.4}$$

$$G_{YD}(s) = \frac{Y(s)}{D(s)} = \frac{G_p}{1 + (G_{C1} + G_{C2})G_p} \tag{4.5}$$

The advantage of the proposed I-D control is that only the integral gain K_I needs to be tuned to control the system transient response, on damping ratios 0 to 1 (also suitable values of T_D and K_D). Also, unlike other controllers (e.g., current controller, sliding mode controller, and fuzzy controller), it uses only one DC-voltage sensor to achieve a zero-steady-state-error output voltage with high dynamic response against step changes to the reference (R) and the disturbance (D).

4.4.1 Gains Tuning of the I-D Controller

Root-locus technique suits SISO-type controllers, hence was used here in designing the gain values of K_I, K_D, and T_D. It forces the root locus to pass through the desired closed-loop poles on the s-plane so the response meets system performance specifications. The basic characteristic of the transient response of a closed-loop system closely relates to the location of the dominant closed-loop pole, therefore the

designer/engineer should know how the closed-loop poles move on the *s*-plane (the root-locus) as the loop gain varies. The desired response specification can be met through an appropriate/suitable gain value. The gain-value tuning procedure, with the closed-loop transfer functions subjected to the reference input *R*, is as follows:

1. Find the equivalent closed-loop transfer function (based on Figure 4.4),

$$\frac{E(T_D s+1)}{As^4+Bs^3+Cs^2+Ds+E} \tag{4.6}$$

   With $A= T_D L_d C_d$, $B= (T_D R_d C_d+L_d C_d)$, $C= (T_D+R_d C_d+K_D)$, $D=1+K_I T_D$, and $E=K_I$.
2. Choose a value for T_D, where $-1/T_D$ is a location of zero and must be far to the left of the *s*-plane so the influence of zero on the system can be ignored. The value of 0.0003 was chosen for T_D.
3. K_D was selected to be about 10 times T_D to avoid the manipulated variable becoming an impulse function when a step-change is applied to the plant. The manipulated variable thus becomes a sharp pulse function. K_D was fine-tuned through a study of the root locus shape. In this design, K_D was 0.002.
4. K_I is the system loop gain. This variable does not change the root locus shape. In the beginning, K_I was assumed to be 1.

Figures 4.6 and 4.7 show the root locus (with its closed-loop poles) and the output response of the closed-loop transfer functions subjected to the reference input (G_{YR}), with T_D=0.0003, K_D=0.002 for these variations to K_I=50, 100, 200, 500. The smaller K_I is, the slower the response. The bigger K_I is, the faster the response, producing a bigger overshoot in transient response. The system is stable for as long as $0<K_I<2434$. The larger the K_I value, the closer to the right of the *s*-plane does the dominant poles reach, thus increasing oscillations in the transient response.

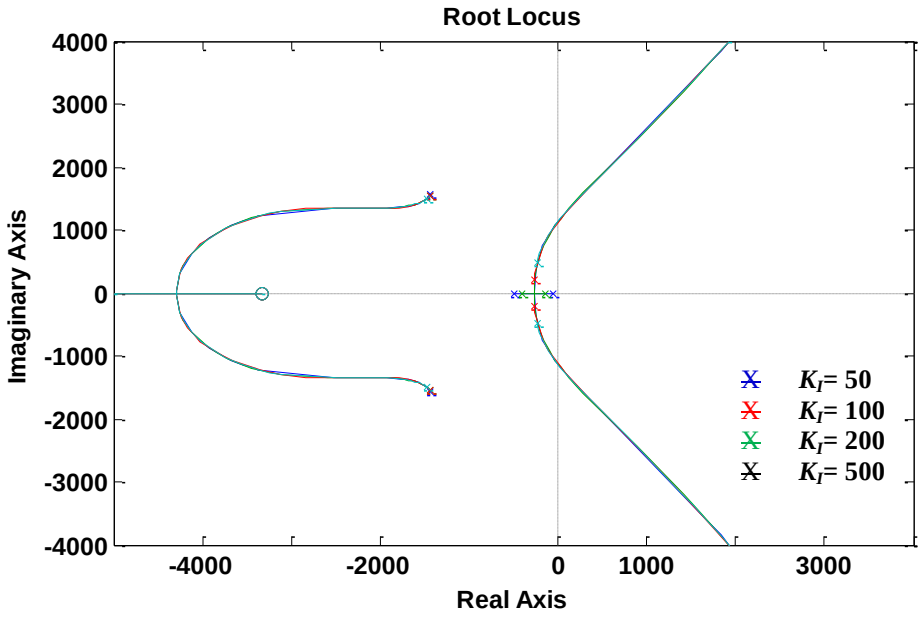


Figure 4.6: The closed-loop system (G_{YR}) root loci against values of K_I

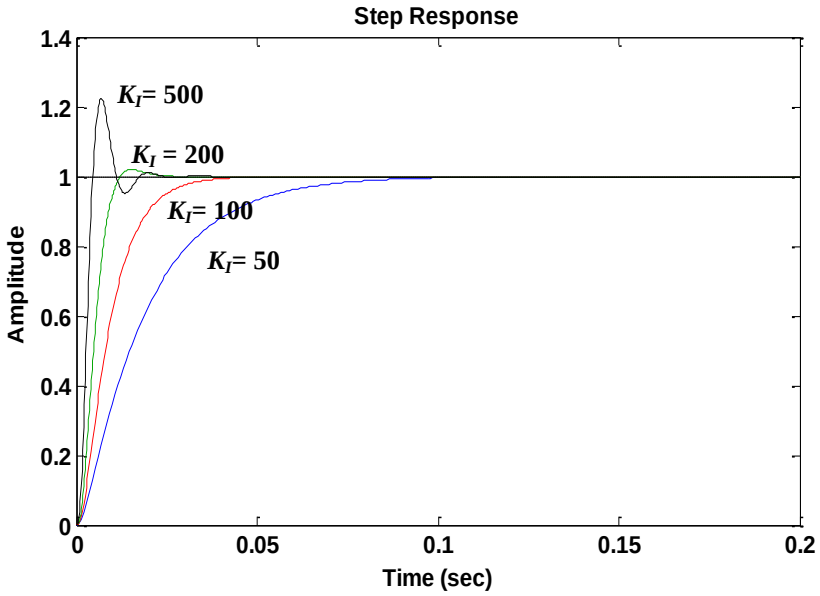


Figure 4.7: The closed-loop system (G_{YR}) step response to values of K_I

The root loci (with their closed-loop poles) and the output response of the closed-loop transfer functions subjected to the disturbance input (G_{YD}) are respectively plotted

in Figures 4.8 and 4.9, with the same gain values for T_D and K_D against variations of K_I in meeting both the reference and disturbance inputs. The root loci plot shows that the closed-loop system of G_{YD} increases the number of zero (placed at origin). The steady-state error in the step disturbance input can thus be eliminated. The response verifies that the proposed I-D controller is able to eliminate the step disturbance input for K_I between 50 and 500. The larger the K_I value, the faster the system reaches zero steady-state error but also the more oscillations in the transient response.

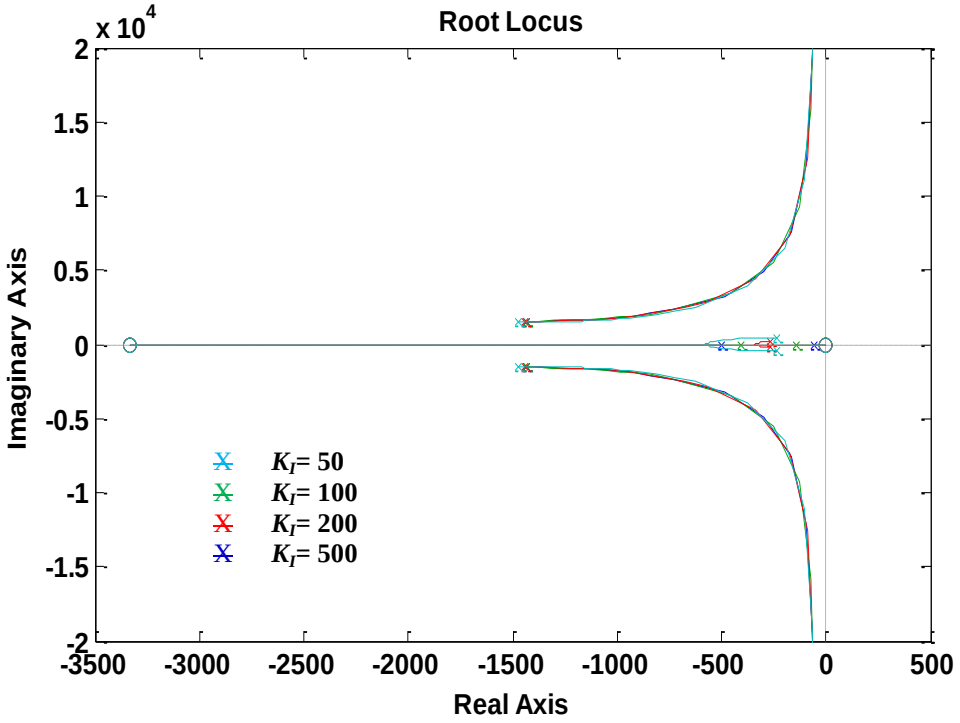


Figure 4.8: The closed-loop system (G_{YD}) root loci against values of K_I

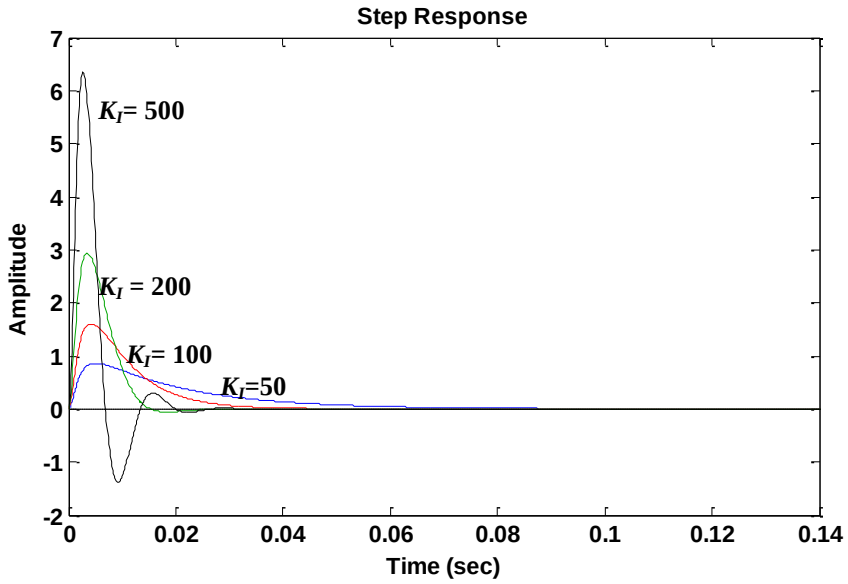


Figure 4.9: Response to the unit-step disturbance input against values of K_I

4.4.2 Discrete Model

For microprocessor implementation, the control system algorithm is more conveniently modelled in discrete form than in transfer function form. The discrete model was developed on MATLAB/Simulink, and verified by DSP programming.

The algorithm is expressed in discrete-time domain through the basic concept of integral. The integral term is considered discrete via the following trapezoid approximation:

$$\int_{\tau}^{t} e(\tau)d\tau \cong \sum \frac{\Delta t}{2}[e(t_i) + e(t_{i-1})] \tag{4.7}$$

The time relationship is $t_i = \Delta t*k$, with Δt the sampling time, and k the discrete-time index (k= 1, 2, 3….). In digital, Equation (4.7) is computed as a continuous summation:

$$u(k) = u(k-1) + \frac{\Delta t}{2}[e(k) + e(k-1)] \tag{4.8}$$

Figure 4.10 is a block diagram for the integral in discrete domain, drawn on MATLAB/Simulink as per Equation (4.8).

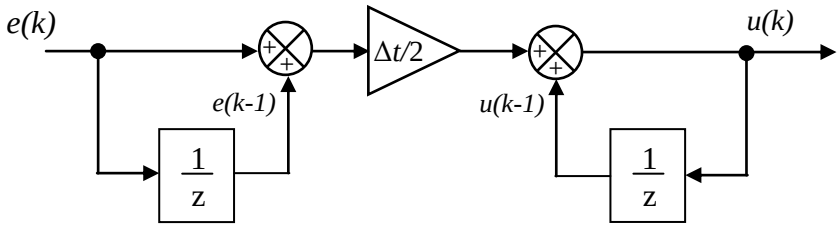


Figure 4.10: Implementing integral action in discrete domain

The block diagrams of Figures 4.11 and 4.12 respectively shows the plant G_p and the proposed I-D controls (outer-loop G_{C1} and minor-loop G_{C2}), modelled in time domain.

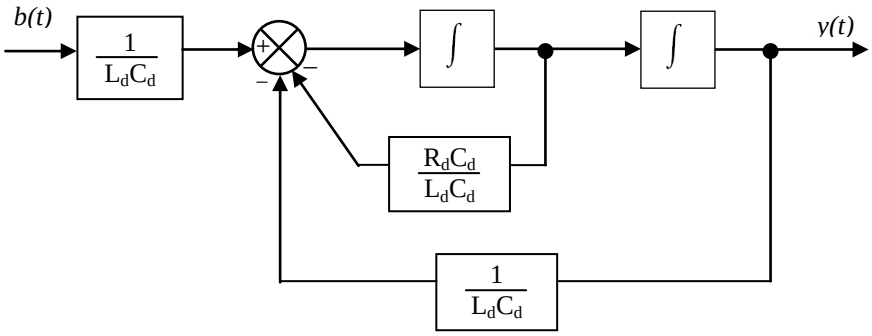


Figure 4.11: The plant, in time-domain

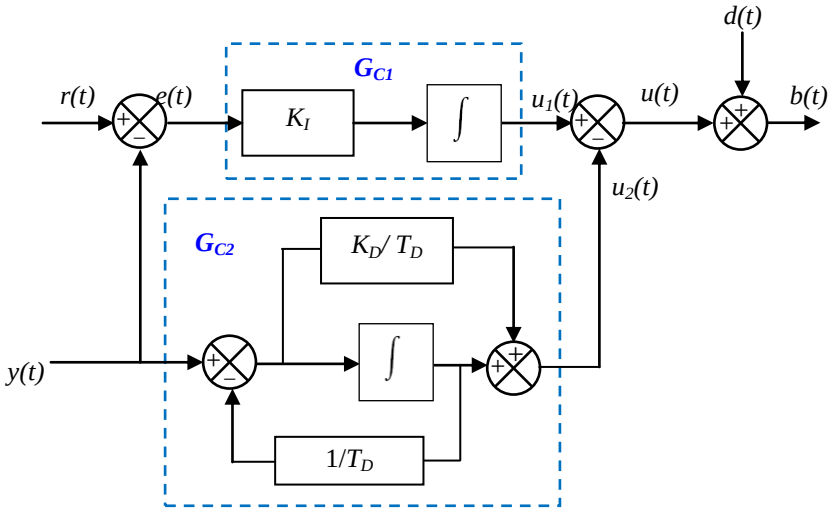


Figure 4.12: The control, in time-domain

Figures 4.13 and 4.14 respectively show the time-domain plant and control replaced by discrete-domain equivalents through the application of basic integral concept of discrete-time domain (Figure 4.10).

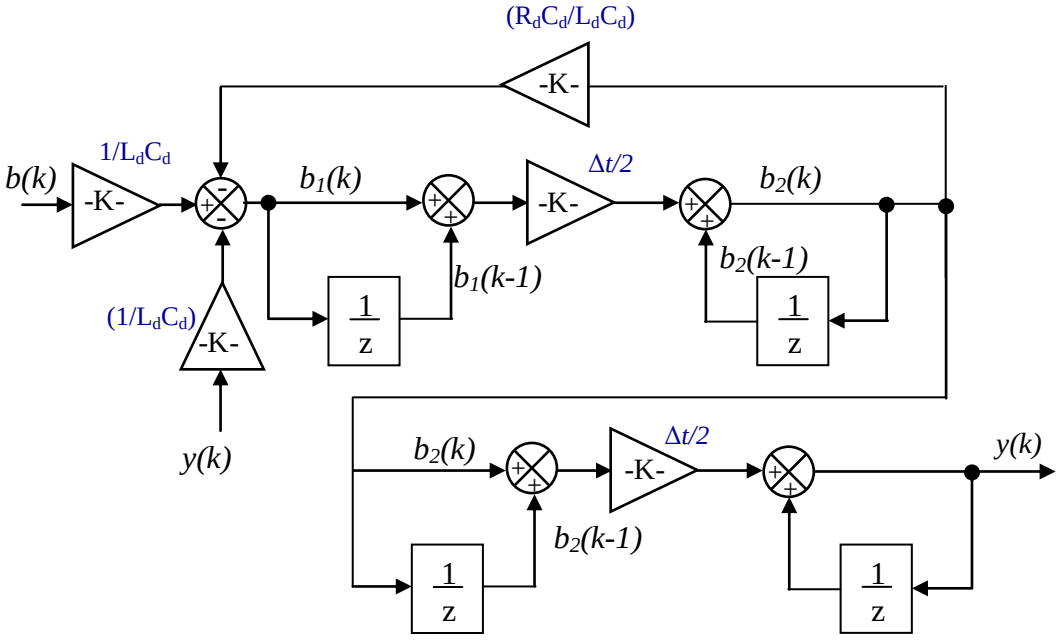


Figure 4.13: The equivalent plant, in discrete-domain

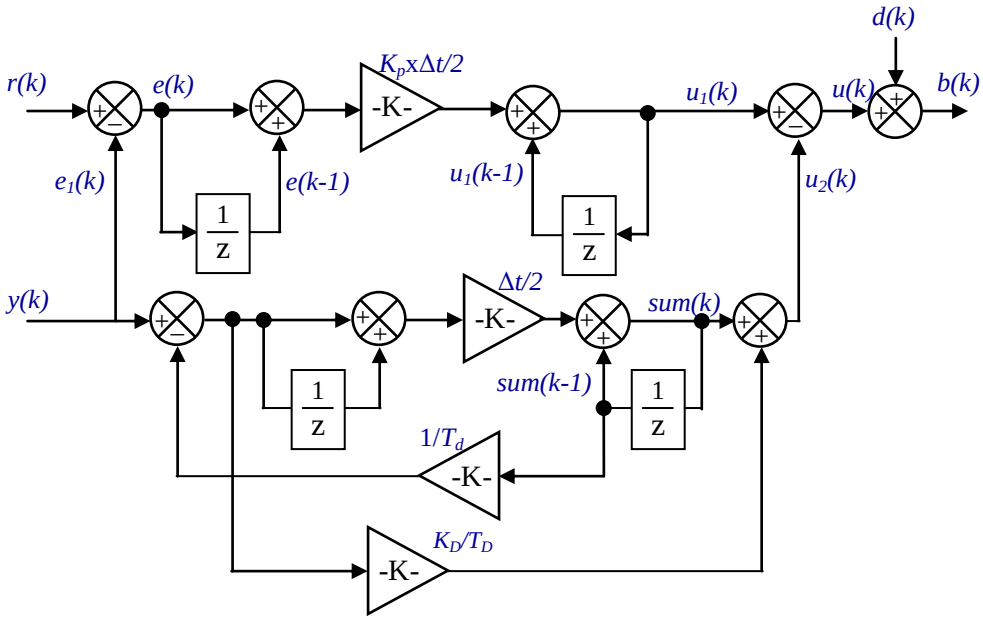


Figure 4.14: The equivalent I-D control, in discrete-domain

From Figure 4.13, the output algorithm of the plant $G_p(k)$ in discrete domain is:

$$y(k) = y(k-1) + \left([b_2(k) + b_2(k-1)] \times \frac{\Delta t}{2} \right) \tag{4.9}$$

Where,

$$b_2(k) = b_2(k-1) + \left([b_1(k) + b_1(k-1)] \times \frac{\Delta t}{2} \right) \tag{4.10}$$

and

$$b_1(k) = b(k) \times \frac{1}{L_d C_d} - \left([b_2(k) \frac{R_d C_d}{L_d C_d} + y(k) \frac{1}{L_d C_d} \right) \tag{4.11}$$

The algorithm of I-D control system on two-degrees-freedom (as shown in Figure 4.14) can be determined from a continuous summation of $u_1(k)$ and $u_2(k)$ computed in digital (with the time relationship $t_i = \Delta t*k$):

$$u_1(k) = u_1(k-1) + K_I \times \frac{\Delta t}{2}[e(k) + e(k-1)] \tag{4.12}$$

$$u_2(k) = sum(k-1) + \frac{\Delta t}{2}[e_1(k) + e_1(k-1)] + \frac{K_D}{T_D} * e_1(k-1) \tag{4.13}$$

Then $b(k)$ and $u(k)$ are calculated as:

$$b(k) = u(k) + d(k) \tag{4.14}$$

$$u(k) = u_1(k) - u_2(k) \tag{4.15}$$

The other related equations are computed as follows:

$$e(k) = r(k) - y(k) \tag{4.16}$$

$$e_1(k) = y(k) - \frac{1}{T_d} \times sum(k-1) \tag{4.17}$$

$$sum(k) = sum(k-1) + \frac{\Delta t}{2}[e_1(k) + e_1(k-1)] \tag{4.18}$$

With $y(k)$ the measured output (from the plant, G_p), $r(k)$ the reference input, and $d(k)$ the disturbance input, in discrete domains.

4.5 Simulation of the I-D Control Algorithm in Discrete Model

The discrete algorithm of the I-D controller system, obtained from Equations (4.9) and (4.18), were developed on MATLAB/Simulink for verification. Figure 4.15 is the MATLAB/Simulink block diagram of the closed-loop system on discrete model/algorithm. The system simulation was developed similarly with the DSP

implementation. The output *y(k)* was compared with a triangle to generate the PWM. The generated PWM of *y(k)* was then filtered by a series resistor-capacitor (RC) for monitoring of the output response *y*.

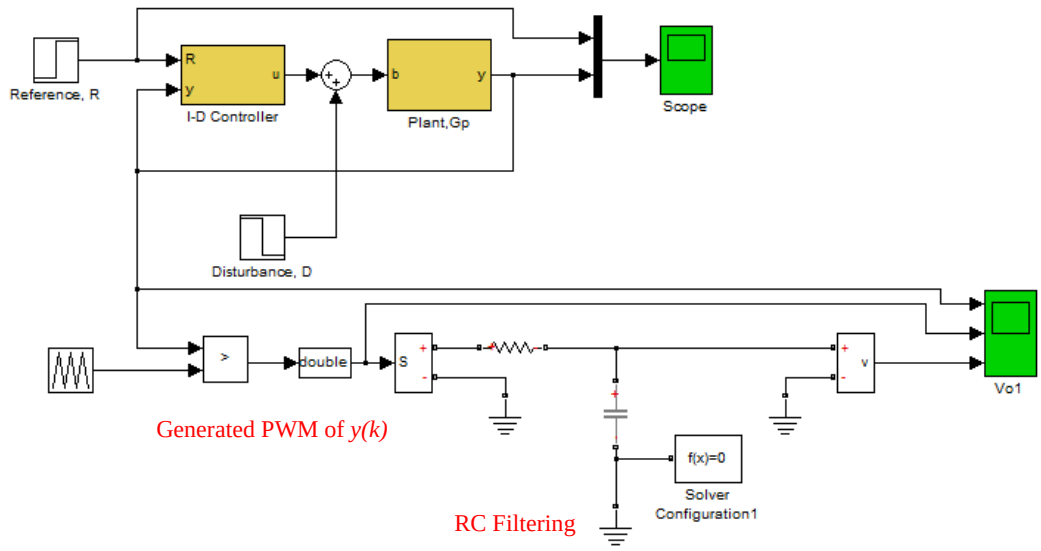


Figure 4.15: MATLAB/Simulink block diagram of the closed-loop system

Tests on the proposed control algorithm were done for three cases (Cases I, II, and III) and with three values of integral gain K_I:

- Case I: Step-up (from 0.5 to 1.0) and step-down the reference *R* (from 1.0 to 0.5) for K_I = 50, 100, and 500, and disturbance D=0.
- Case II: Step-up (from 0 to 0.2) and step-down the disturbance *D* (from 0.2 to 0) for K_I = 50, 100 and 500, with reference being 0.7.
- Case III: Step-up (from 0.5 to 0.9) and step-down the disturbance *D* (from 0 to −0.2) for K_I=100.

The tests used derivative controller gain T_D=0.0003 and K_D=0.002. Figures 4.16, 4.17, and 4.18 show the simulation results (*y(k)* after filtering), respectively for Cases I, II and III.

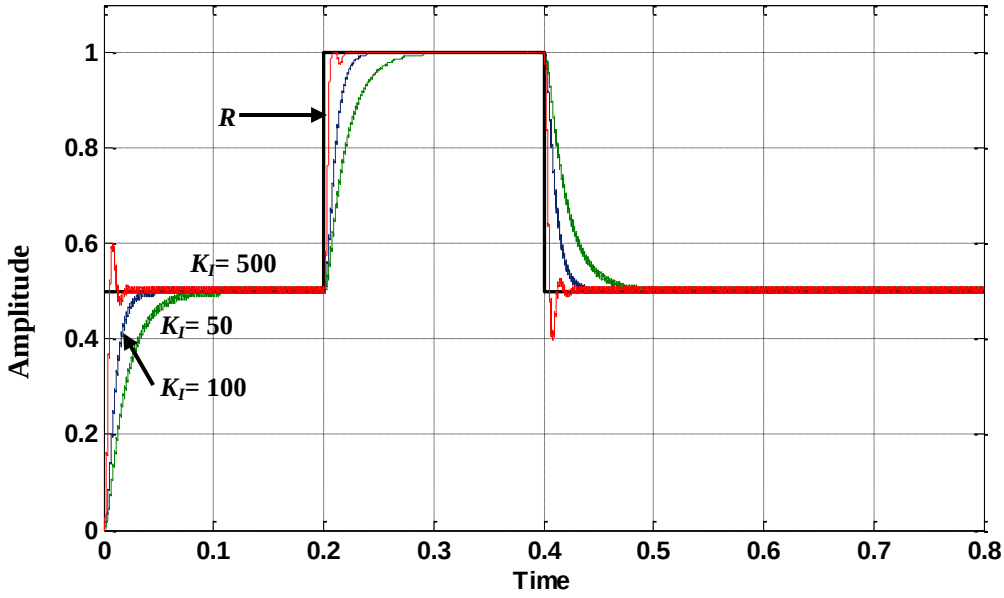


Figure 4.16: Case I for K_I= 50, 100 and 500 (D = 0)

Referring to Cases I and II in Figures 4.16 and 4.17, the gains K_I = 50, 100, and 500 were able to follow the reference, with zero steady-state error but with difference in transient response. In practice, tuning of a suitable K_I may be preferred, to reduce the current stress on the semiconductors during transients (Green et al., 1997). A fast and lightly damped system gives a fast step response but also a large-amplitude capacitor-charging current. The best integral gain is thus K_I=100 because it produces faster response and zero oscillation. Figure 4.18 (Case III) demonstrates the results of the output response (*y(k)*), the generated PWM of *y(k)*, and the output response (*y(k)*) after RC filtering.

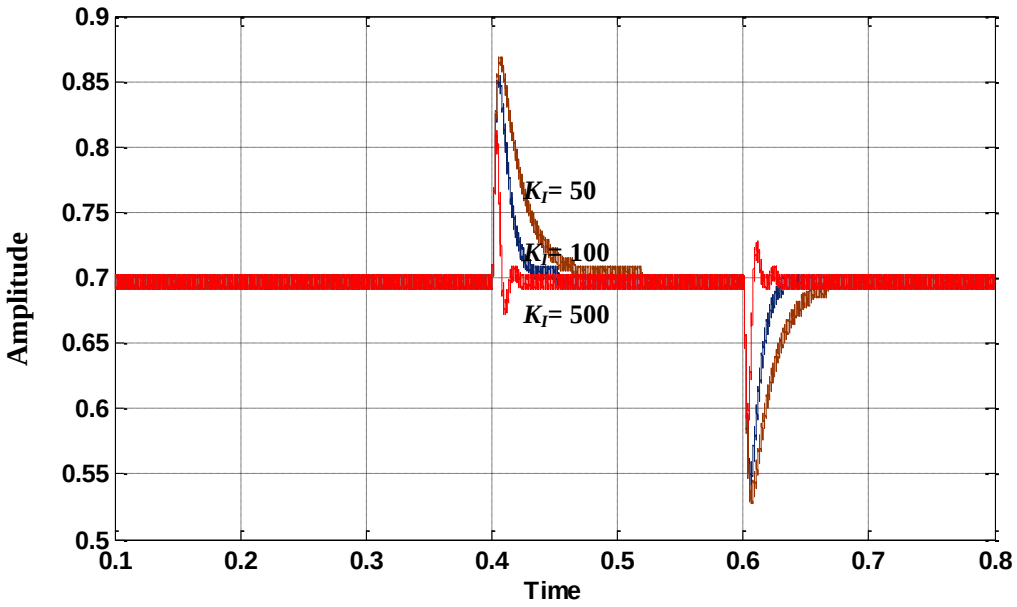


Figure 4.17: Case II for K_I = 50, 100, and 500 (R=0.7)

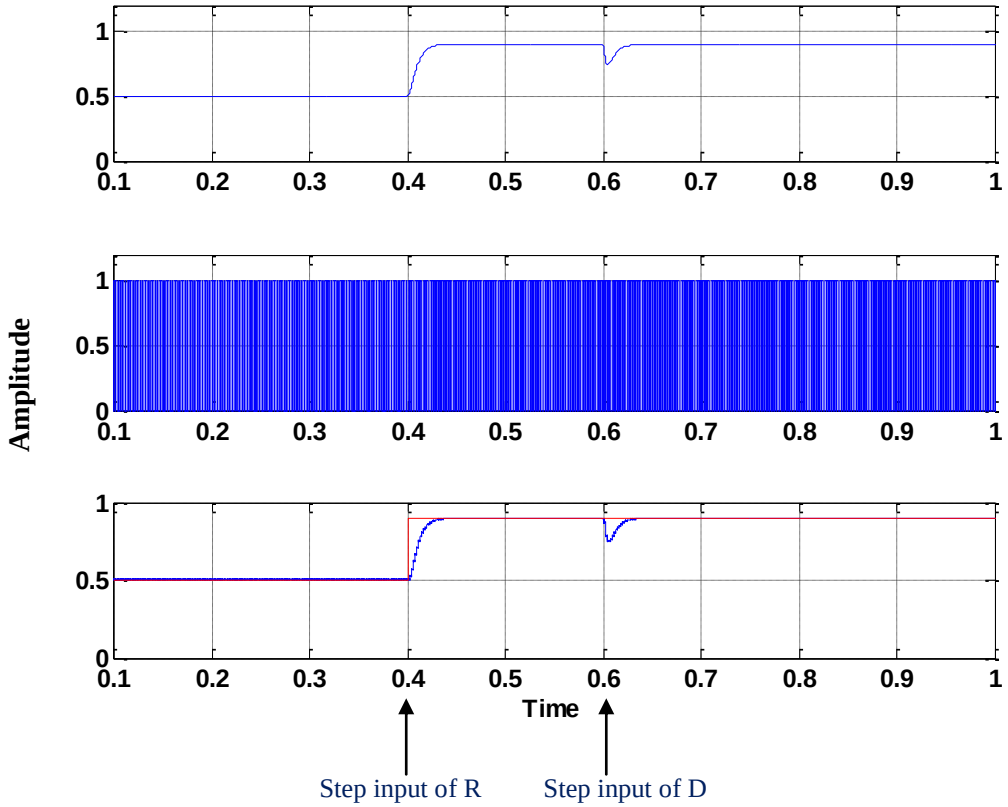


Figure 4.18: Results of Case III: (a) the output response *y(k)*, (b) the generated PWM of *y(k)* and, (c) the output response *y(k)* after RC filtering

4.6 DSP Verification of the Control Algorithm

The discrete algorithm of the I-D controller system, obtained from Equations (4.9) and (4.18), was written in DSP source code (c-language) for verification. Figure 4.19 is the flowchart of the DSP control algorithm verification process. A complete cycle consists of 1200 data (k = 1, 2, 3, …, 1200), and the data processed by the algorithm was updated every 1ms. The generated output of *y(k)* was sent to the ePWM module to generate the PWM. The ePWM output pin was connected to the RC filter before the signal was monitored on oscilloscope. The process was repeated after *k*=1200, and the value of *k* reset while the DSP was still running.

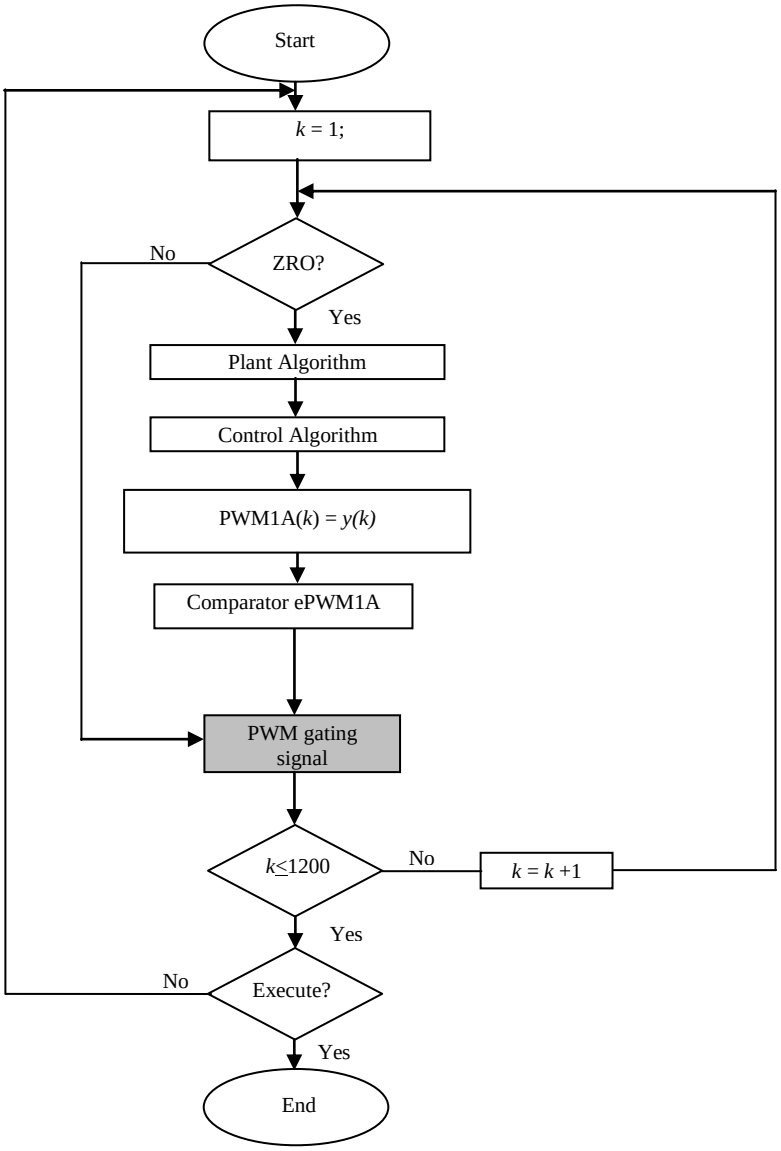
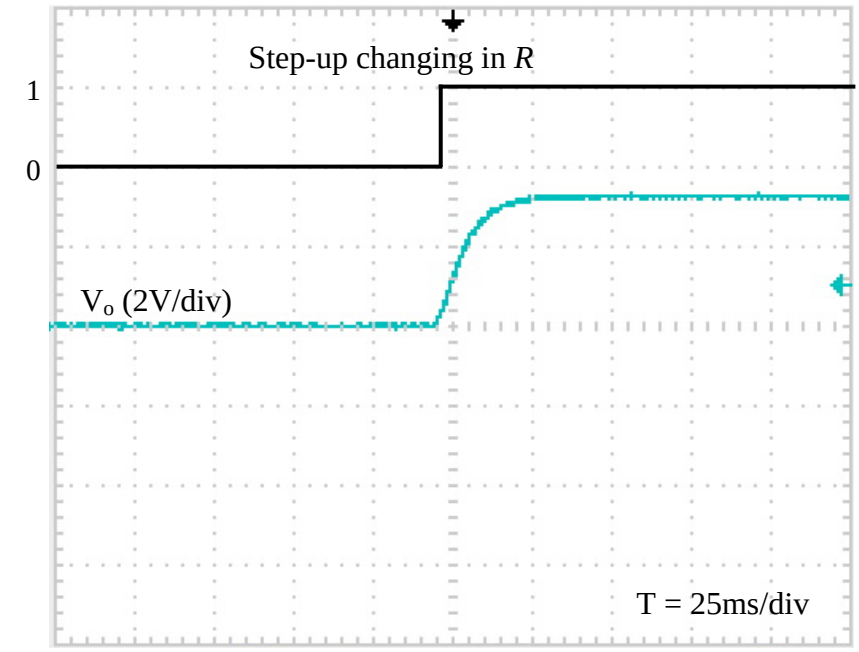
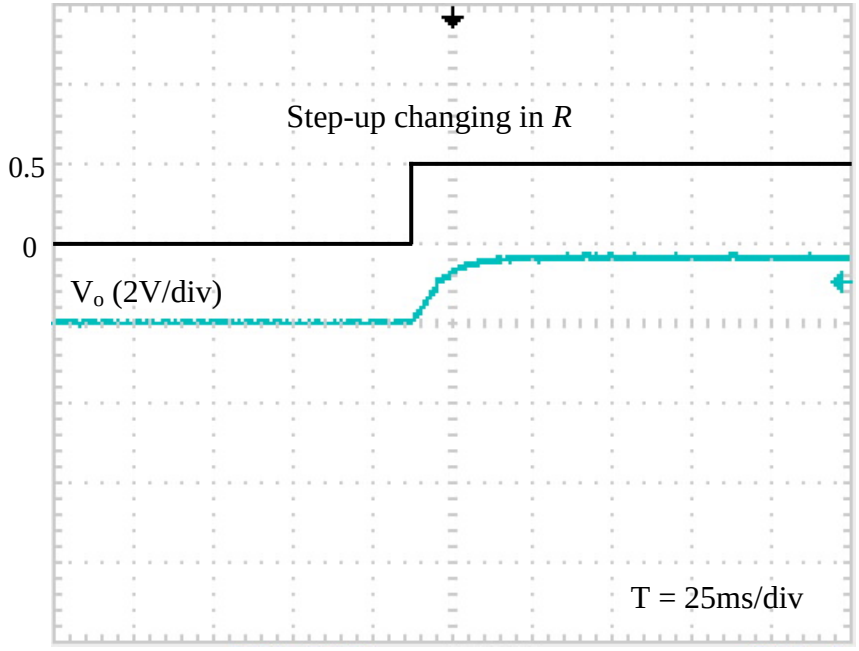


Figure 4.19: The flowchart of the DSP verification of the control algorithm

DSP control algorithms verified by stepping up and stepping down the reference *R* and the disturbance *D*. The verification tests used integral gain K_I=100, and derivative controller gain T_D=0.0003, with K_D=0.002. Figures 4.20-4.21 show the results of stepping up and stepping down the reference *R*. The output responses show the control algorithm producing good responses and able to follow the reference *R* input in both the step-up and step-down tests. In the case of step-change the disturbance *D*, the control algorithm is also able to eliminate the disturbance *D*, as Figure 4.22 shows.

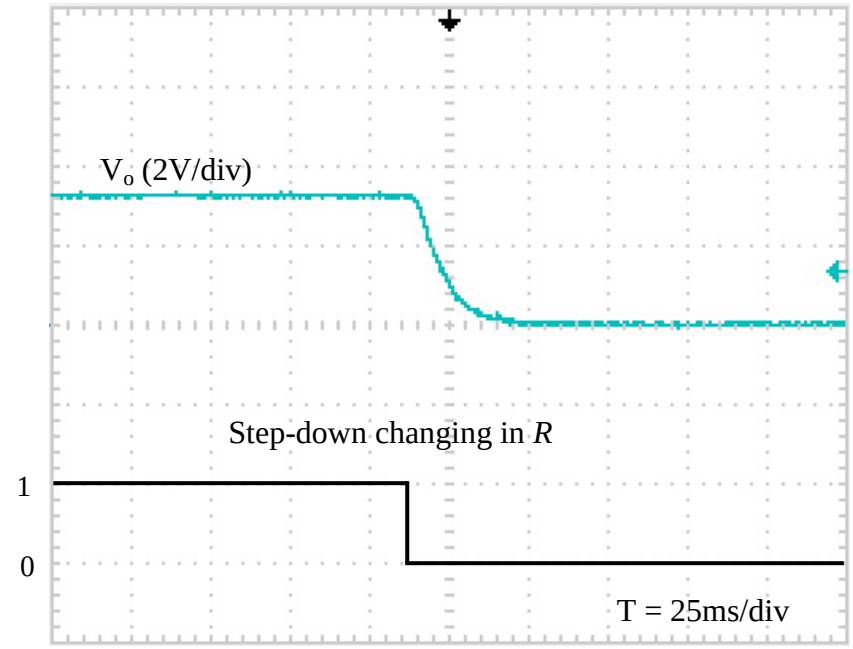


(a)

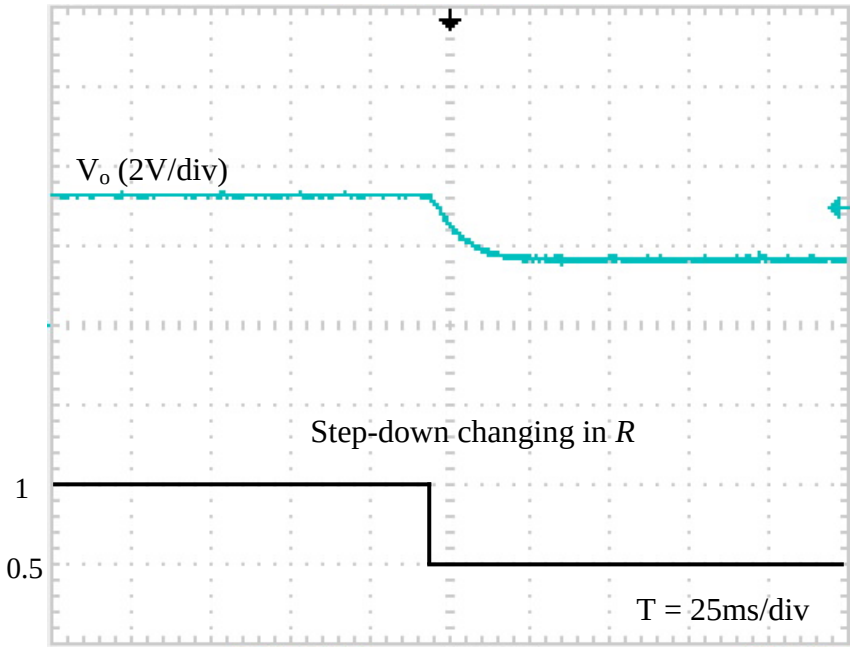


(b)

Figure 4.20: Verifying the DSP control algorithm by stepping up the reference *R*, (a) from 0 to 1 (b) from 0 to 0.5

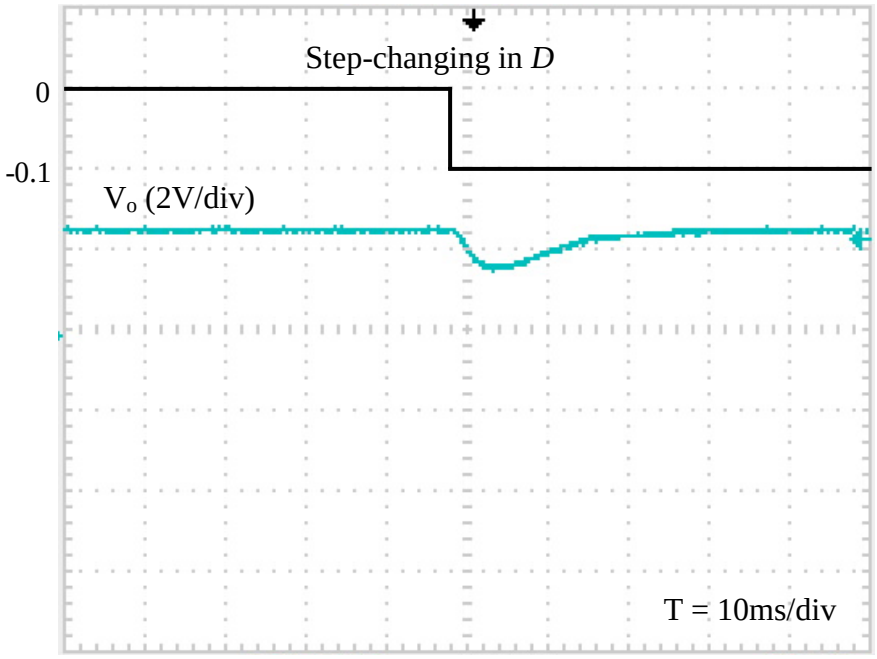


(a)

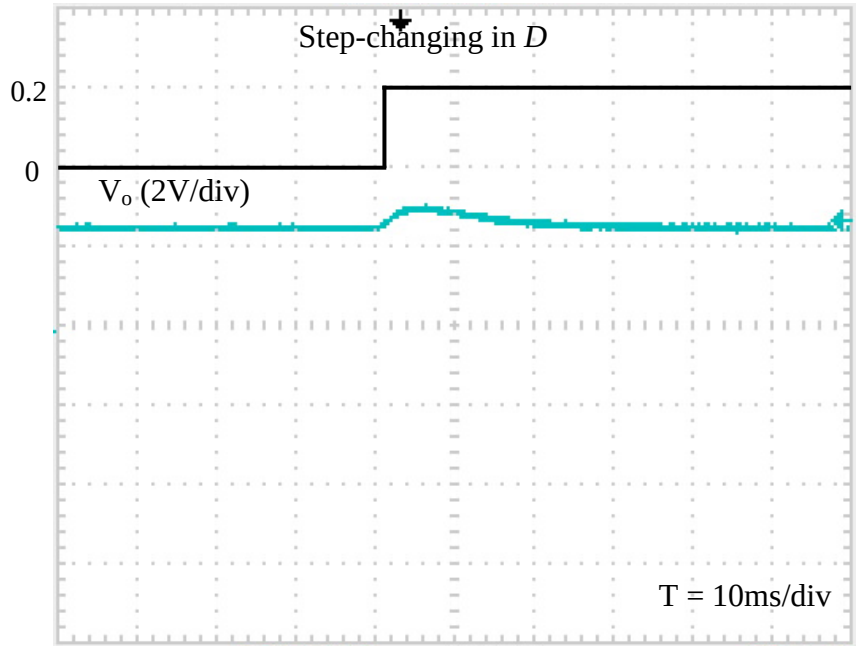


(b)

Figure 4.21: Verifying the DSP control algorithm by stepping down the reference *R*, (a) from 1 to 0 (b) from 1 to 0.5



(a)

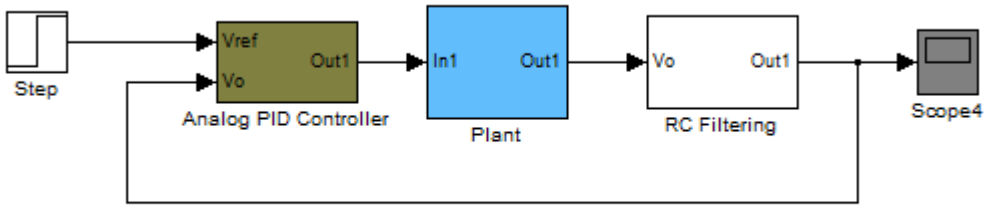


(b)

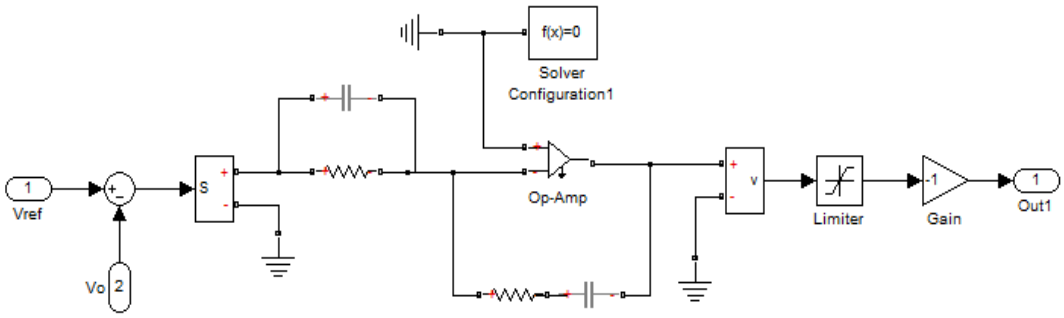
Figure 4.22: Verifying the DSP control algorithm by stepping change the disturbance *D* (a) from 0 to -0.1 (b) from 0 to 0.2

4.7 Comparing the Cascaded PID and the I-D controllers

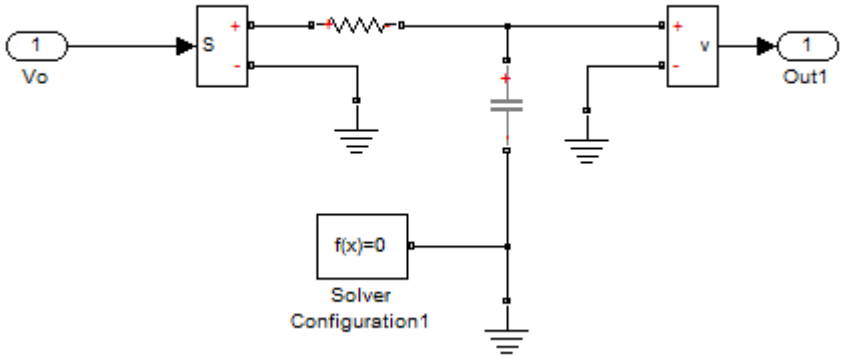
A conventional cascaded PID has been comparatively studied against the proposed I-D controller. Figure 4.23(a) shows a system of PID controller that implemented in active circuit realization (analog implementation) in MATLAB/Simulink.



(a)



(b)



(c)

Figure 4.23: (a) A system with cascaded PID controller, (b) Analog PID controller, (c) A series resistor-capacitor (RC)

The analog PID controller needs additional circuits such as anti-wind-up control (limiter) to solve the saturation problem and a series resistor-capacitor (RC) at system's output for filtering as shown in Figure 4.24(b) and 4.24(c), respectively. However these additional circuits degrade the performance of the controller (analog PID controller).

Both controller techniques (PID and proposed I-D) were tested to the same converter parameters and in AC-DC power flow. The PID used the gains K_P = 6.461, K_I = 372.2 and K_D = 2.278x10^{-3}, whereas the I-D controller used K_I = 130, T_D = 0.0003, K_D = 0.002. All the gains values were designed to achieve settling time, T_s less than 0.04s. The cascaded PID has two zeros plus a pole at origin (number of zero greater than pole), so that it was difficult to implement the cascaded PID (especially the derivative term) into practical or computer algorithm. The closed-loop transfer function, $T_{PID}(s)$ of compensated system (with a PID controller) is

$$T_{PID}(s) = \frac{1726\ s^2 + 4.895\times10^6\ s + 2.82\times10^8}{s^3 + 1809\ s^2 + 5.625\times10^6\ s + 2.82\times10^8} \tag{4.19}$$

Figure 4.24 shows the step responses of the cascaded PID ($T_{PID}(s)$) and I-D controllers in a linear system. The I-D controller gave better output response compared to the cascaded PID controller in term of lower percentage overshoot and faster settling time.

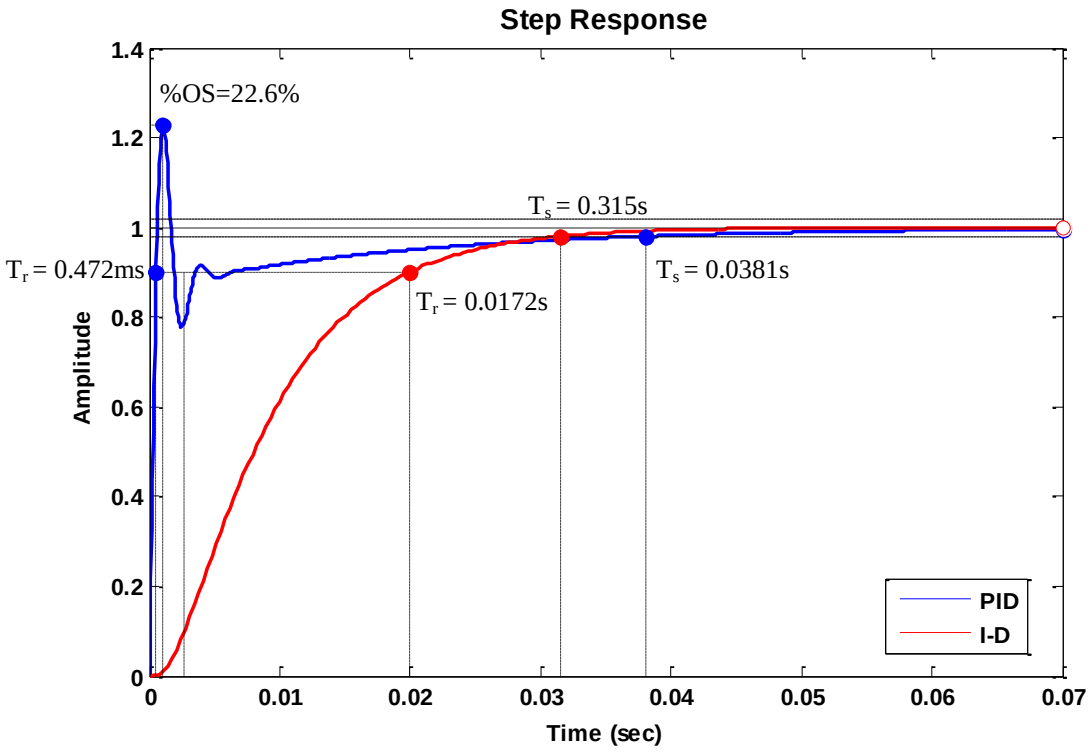


Figure 4.24: Step response of PID and I-D controllers

Figure 4.25 shows the output response of I-D controller, analog PID controller with and without RC filtering, where reference value is 1. The I-D controller gave better output response compared to the analog PID controller in term of lower percentage overshoot, zero steady-state error, faster settling time and rise time.

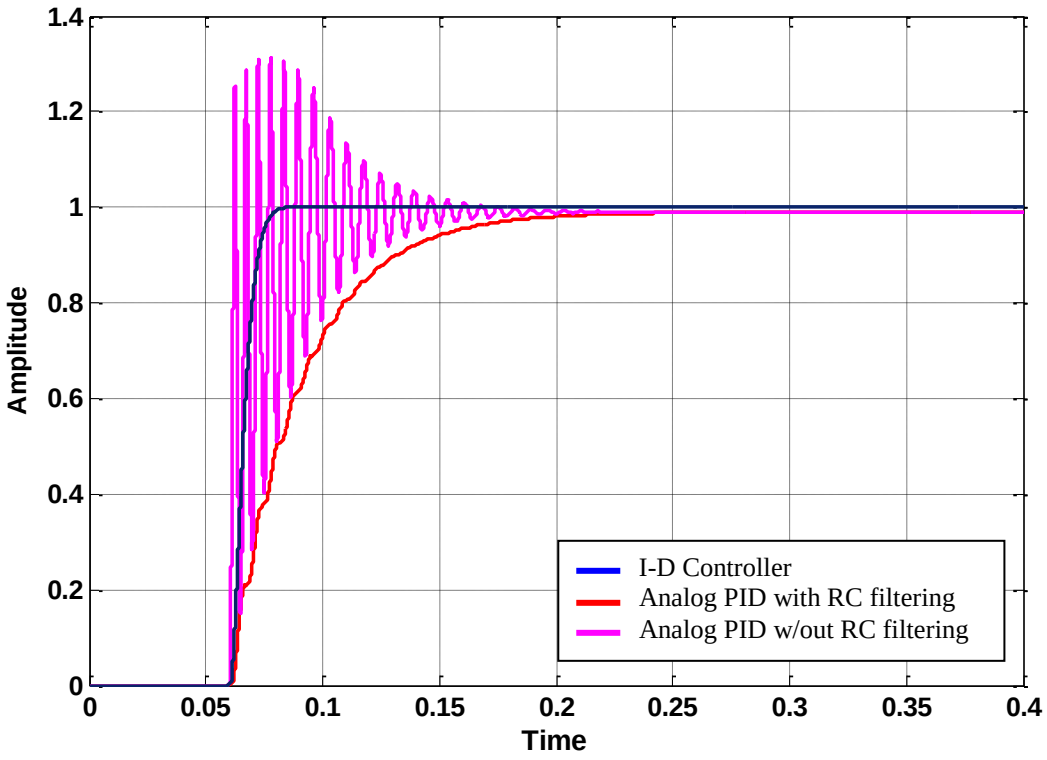


Figure 4.25: The output responses of output response of the I-D controller, analog PID controller with and without RC filtering.

4.8 Predicting the Modulation Index Curve through Placement of the Dominant Closed-Loop Poles

The linear relationship between the bridge voltage (V_B) and the modulation index (M), as derived in Chapter 3 (Section 3.2.2), is:

$$V_B = \frac{3}{2} V_m \mathrm{M} \tag{4.20}$$

The bridge voltage V_B is considered an output voltage to the plant (G_p), allowing Equation (4.20) to be written as:

$$V_o = \frac{3}{2} V_m \mathrm{M} \tag{4.21}$$

From Equation (4.21), the discrete-domain modulation index M(k) can be computed as:

$$\mathrm{M}(k) = \frac{\left(y_r(k) + y_d(k)\right)}{1.5 \times V_m} = \frac{y(k)}{1.5 \times V_m} \tag{4.22}$$

Where $y_r(k)$ and $y_d(k)$ are the output responses, respectively subjected to the reference input and disturbance input, in discrete domain. Equation (4.22) expresses M(k) as being linear to the total of output response $y(k)$ of the closed-loop system. The control action of the modulation index curve M(k) can therefore be predicted and simplified through an investigation of the closed-loop output response $y(k)$.

The basic characteristic of the output response of a closed-loop system usually relates closely to the location of the dominant closed-loop poles. The dominant poles dominate the output response since their contribution takes a longer time/locus path than those of the other poles. Predicting the M curve of the I-D controller using placement of the dominant closed-loop poles can be a new control technique approach (namely as modulation-index-curve-prediction), used as the control action of M(t). The process of determining this prediction M curve is easier by analyzing the system separately (i.e. system subjected to the reference input and system subjected to disturbance input).

4.8.1 Predicting the Curve of a System Subjected to a Reference Input

The closed loop of the transfer function (I-D controller), $T_r(s)$ is determined by Equation (4.2). Substituting the values of L_d = 6mH, R_d = 0.5Ω, C_d = 220μF, K_I = 100, T_D = 0.0003, and K_D = 0.002 into the equation, the closed-loop transfer function of the proposed system, subjected to the reference input, is,

$$T_r(s) = \frac{Y(s)}{R(s)} = \frac{2.273 \times 10^4 \; s + 7.576 \times 10^7}{0.0003\, s^4 + 1.025\, s^3 + 1826\, s^2 + 7.803 \times 10^5 s + 7.576 \times 10^7} \tag{4.23}$$

Therefore, the location of the closed-loop zero and poles are as follows:

Zero : z1= -3.3333 x 10^3

Poles : p1 = - 407.9, p2 = -138.8, and p3, p4 = -1435 $\pm$ j1549.5

p1 and p2 are the dominant poles because of their location (the closest to the imaginary axis). Figure 4.26 shows the system output response T_r(s). The curve of the response is similar to that of the overdamped system, which has a pole at the origin (from the unit step input) and two real poles (known also as dominant poles, from the system). The input pole at the origin generates the constant forced response and each of the dominant poles on the real axis generates an exponential natural response whose exponential frequency equals the location of the poles.

The general output response $c(t)$ of the overdamped system can be written as

$$c(t) = K_1 + K_2 e^{-\sigma 1 t} + K_3 e^{-\sigma 2 t} \tag{4.24}$$

where K_1, K_2, and K_3 are the coefficient values, and σ1, σ2 the locations of the dominant poles.

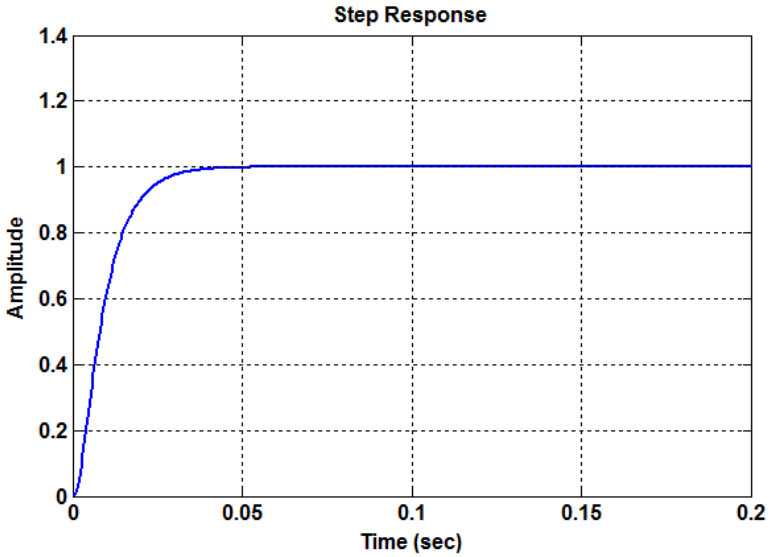


Figure 4.26: The step-reference output response T_r

The values of K_1, K_2, and K_3 of Equation (4.24) can be solved if the locations of the dominant poles (σ_1, σ_2) are known (through Partial Fraction Expansion Method). Substituting the dominant poles p2 and p3 into Equation (4.24) gives:

$$y_r(t) = 1 + 0.5158e^{-407.9t} - 1.5158e^{-138.8t} \tag{4.25}$$

Figure 4.27 shows the output response of $y_r(t)$. Both the responses (refer to Figures 4.24 and 4.25) show that Equation (4.25) can be used as the prediction curve of the modulation index (M) for systems subjected to the reference input.

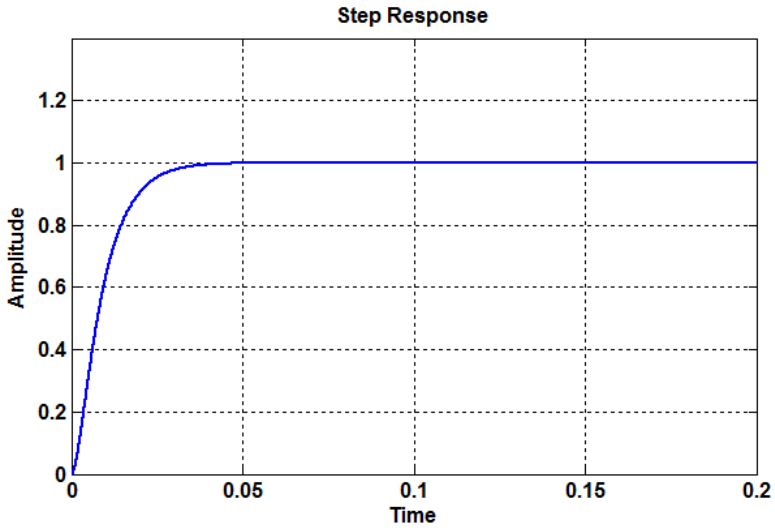


Figure 4.27: The output response of $y_r(t)$

4.8.2 Predicting the M Curve of a System Subjected to a Disturbance Input

In the system subjected to a disturbance input (i.e., a load change), the controlling action of M depends on the curve of the output response to the disturbance input. The closed-loop transfer function of the proposed system subjected to a disturbance input is

$$T_d(s) = \frac{2.273\times10^4\ s^2 + 7.576\times10^7\ s}{0.03\ s^4 + 102.5\ s^3 + 1.826\times10^5\ s^2 + 7.803\times10^7\ s + 7.576\times10^9} \tag{4.26}$$

The location of the closed-loop zeros and poles are as follows;

Zeros : z1 = 0, z2= -3.3333 x 10^3

Poles : p1 = - 407.9, p2 = -138.8, and p3, p4 = -1435 $\pm$ j1549.5

A zero at origin is added to the system receiving a disturbance input, and a comparison is made with the system receiving a reference input. The zero affects the residue or amplitude of the output response (Nise, 2008), but the natural response (i.e., exponential, damped sinusoid) is dominated by the dominant poles of p1 and p2. The

prediction curve of the modulation index M for the system receiving the disturbance input can be produced through determination of the output response $y_d(t)$ and use of the zero and the dominant poles.

The output response $y_d(t)$ can be written as

$$y_d(t) = K_1 e^{-\sigma 1 t} + K_2 e^{-\sigma 2 t} \tag{4.27}$$

where K_1 and K_2 are the coefficient values, and σ1, σ2 the location of the dominant poles.

By using the location of the dominant poles and the zero at origin, and then solving by Laplace partial method, the prediction curve of the modulation index M for the system receiving the disturbance input is

$$y_d(t) = 2.1083(e^{-138.8t} - e^{-407.9t}) \tag{4.28}$$

Figure 4.28 shows both the output response of the closed-loop system (T_d) and the proposed prediction (y_d) using I-D controller. Both the responses are almost similar, i.e., the proposed M-curve-prediction control approach is also applicable to a system subjected to the disturbance input.

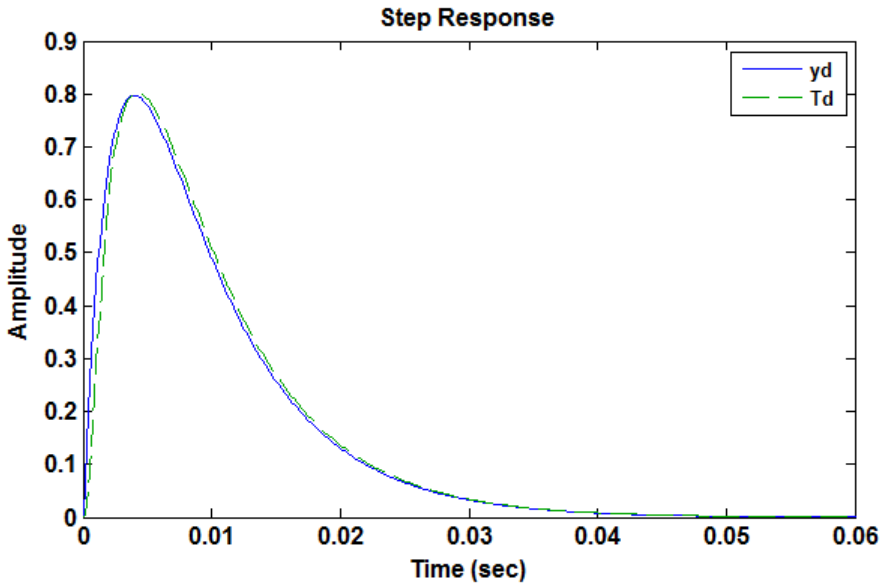


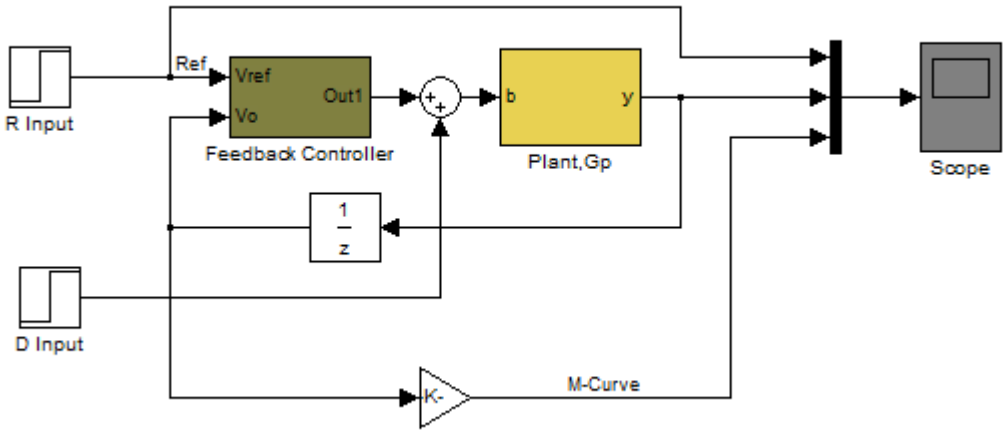
Figure 4.28: The output response T_d of the closed-loop system and the prediction control y_d

4.9 Implementing the Proposed Modulation-Index-Curve Prediction Technique

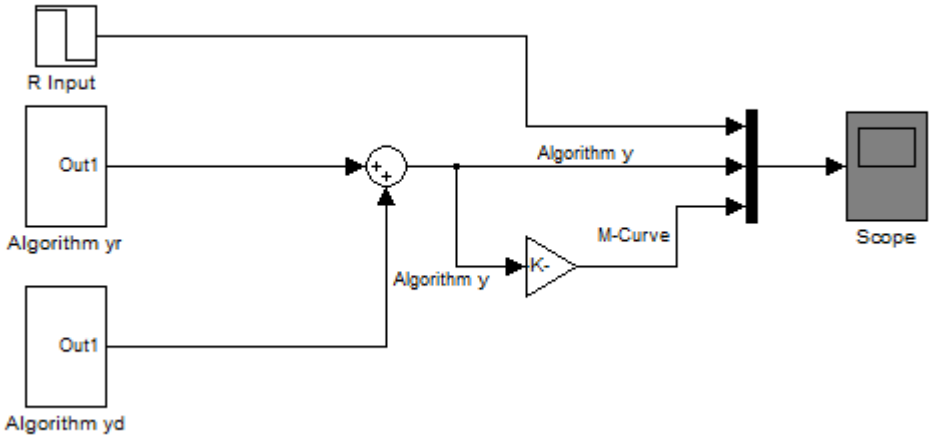
The algorithm of modulation-index-curve prediction is determined by combining equation (4.25) and (4.28), yielding

$$y(t) = y_r(t) + y_d(t) \tag{4.29}$$

Figure 4.29(a) and (b) is a block diagram showing implementation of the I-D control technique and the proposed M-prediction curve systems in MATLAB/Simulink, respectively. M-curve is obtained using the Equation (4.21) and Equation (4.22) for the I-D control technique and the proposed M-prediction curve, respectively. Algorithm yr, yd and y are obtained from the Equations (4.25), (4.28) and (4.29).



(a)



(b)

Figure 4.29: The closed-loop systems of (a) I-D control and (b) the proposed M prediction curve technique, drawn on MATLAB/Simulink

The reference, output responses and the modulation index curve for both control systems are shown in Figures 4.30 and 4.31 respectively, for tests on step-up and step-down in the reference and disturbance inputs. The similarity in both output responses prove that the proposed M curve prediction can be used as the new feedback control technique. The new technique has simpler algorithm and more autonomous, i.e., its physical implementation does not depend too much on the feedback-sensor information.

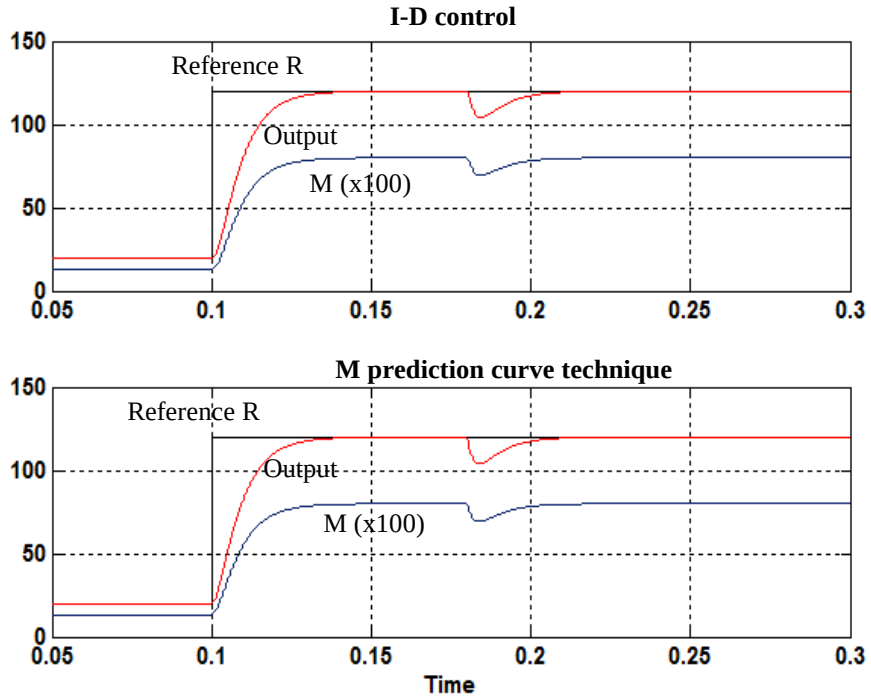


Figure 4.30: Step-up in the reference (20 to 120V) at 0.1s and disturbance (0 to -20) at 0.18s inputs

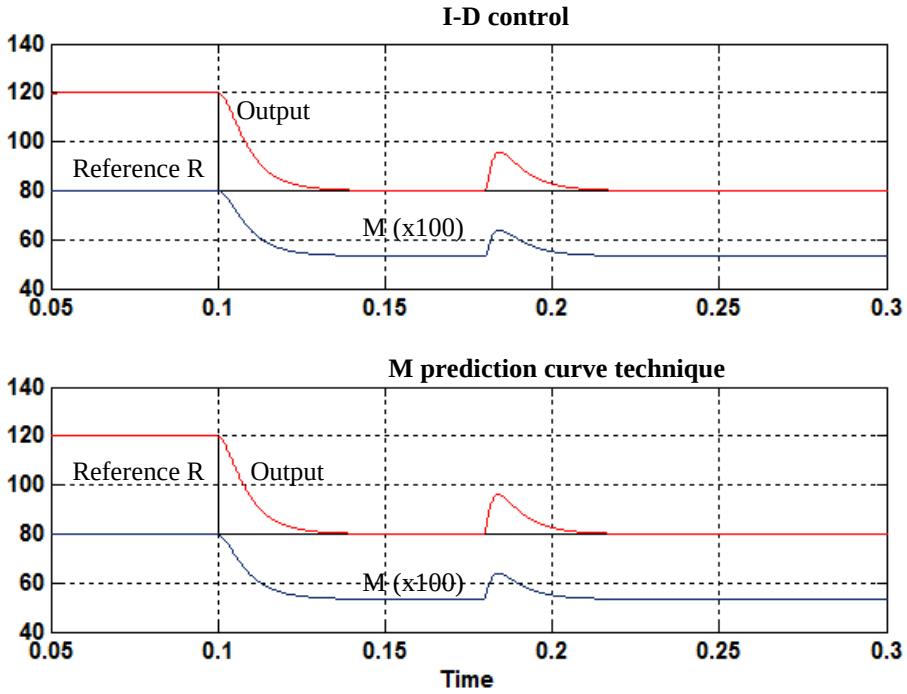


Figure 4.31: Step-down in the reference (120 to 80V) at 0.1s and disturbance (0 to +20) at 0.18s inputs

4.10 Summary

Chapter 4 presents the design and implementation of the proposed feedback controller in a linear system. The I-D controller proposed is a two-degrees-of-freedom model that achieves the desired dynamic response to changes in the reference and disturbance inputs. An improved voltage feedback control was introduced, through the design of a prediction modulation index curve based on placement of the closed-loop poles (the I-D control). The improved control (modulation-index-curve prediction technique) simplifies implementation and minimizes the digital computational burden on the DSP. Its effectiveness was verified on MATLAB/Simulink, and its mathematical model implemented in a TMS320F28335 DSP. The simulation and experiment results of the three-phase AC-DC buck-type with simplified-plus-modified SPWM technique and the proposed feedback controller will be presented in Chapters 5 and 6.

CHAPTER 5

SIMULATION RESULTS

5.1 Introduction

This chapter discusses the simulation results of the proposed three-phase AC-DC buck-type converter (with bidirectional capability) in open-loop system, closed-loop system and the dynamic performance of bidirectional system. MATLAB/Simulink was chosen to produce the results of voltages, current, modulation index and total harmonic distortion (THD) for further analysis.

The open-loop system was used to verify the operation of the proposed bidirectional three-phase AC-DC buck-type converter and its proposed simplified-plus-modified SPWM during AC-DC and DC-AC operations. The comparison between the proposed modulation techniques and the standard modulation technique under the same conditions are also discussed. The closed-loop system was simulated to validate the capability and effectiveness of the proposed feedback control, I-D control, and modulation-index-curve prediction based-on the placement of closed-loop poles, in compensating start-up current/voltage and achieving zero steady-state error for AC-DC operation. The tests included step-changing the reference voltage input and step-changing the load (various loads, i.e., their resistance and inductance). The controller gain values were analyzed for their transient performance. To accomplish the closed-loop analysis, a comparison is also provided between conventional PID controller and the proposed I-D controller. Hence, the simulation of bidirectional operation was done

to demonstrate its capability in providing energy back from DC to AC voltage sources; and vice versa.

5.2 System Parameters and MATLAB/Simulink Circuit

The bidirectional three-phase AC-DC buck-type converter circuit configuration with the simplified-plus-modified SPWM design was simulated on MATLAB/Simulink. It was configured with LC input and output filters, six IGBTs and 24 diodes, and for freewheeling conduction, one diode and one IGBT. To prevent circuit attenuation, the input filter resonant frequency was designed to be much lower than the switching frequency. The influence of the input filters (L_f and C_f) can be ignored if an appropriate input filter design is used (Milanovic & Dobaj, 2000; Milanovic & Slibar, 2011). Table 5.1 lists the parameters of the power converter used in the simulations for AC-DC and DC-AC operations.

Table 5.1: Parameters of the power converter in the MATLAB/Simulink simulation

Parameter	AC-DC	DC-AC
Switching frequency, f_s	19.8kHz	19.8kHz
Input filter, L_f-R_f, C_f	1mH-0.5Ω, 1μF	1mH-0.5Ω, 1μF
Output filter, L_d-R_d, C_d	6mH-0.5Ω, 220μF	6mH-0.5Ω, 220μF
Main voltage frequency, f	50Hz	50Hz
Line-Neutral AC voltage, V_m	100 V_p	NA
DC voltage source, V_{dc}	NA	120V

Note: R_f and R_d are considered equivalent series resistance (ESR) of the inductor filter.

The open-loop schematic circuit of the proposed system and its proposed PWM control were developed on Simulink, for AC-DC and DC-AC operations (respectively, Figures 5.1 and 5.2); the details of the PWM gating signals of each switch has been

discussed in Chapter 3. The solver of the discrete variable step was used to perform digital simulation. The simulation sampling time chosen was 0.8418μs because the reference data in the look-up table was sampled every 8.418μs in the MATLAB script file (*.m) for 2376 data, to suit the system's switching frequency of 19.8kHz for the 50Hz mains supply. Figure 5.3 is a block diagram of the bidirectional power converter which uses 6 switches and 24 diodes, and for freewheeling, 1 switch and 1 diode.

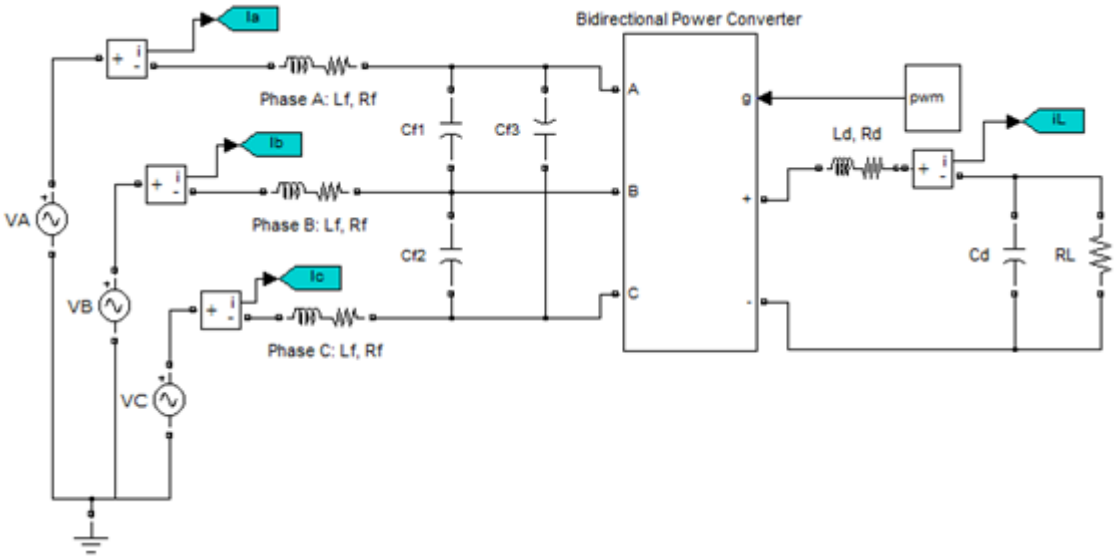


Figure 5.1: The AC-DC circuit configuration, drawn on MATLAB/Simulink

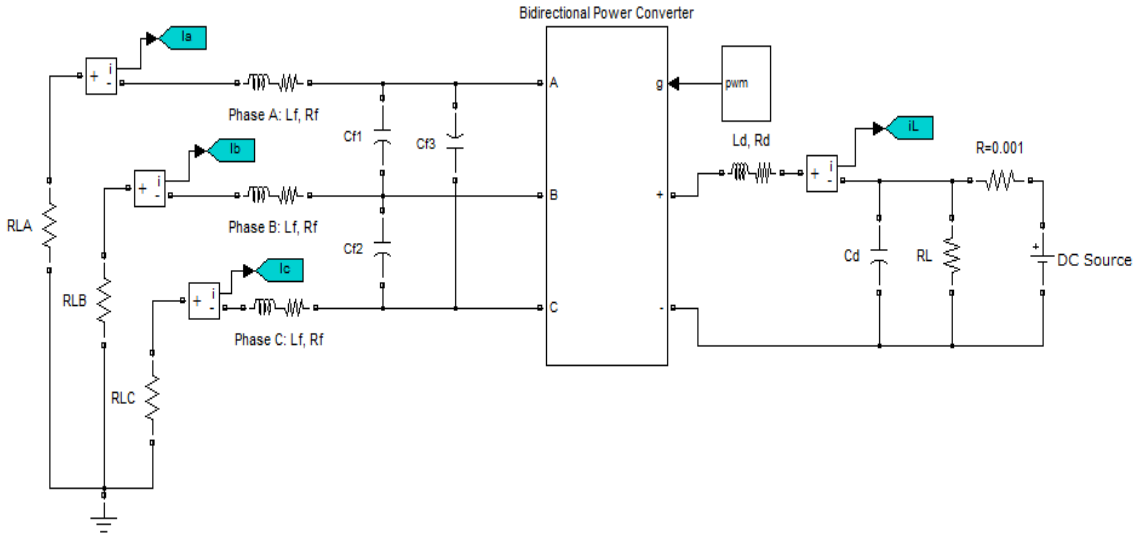


Figure 5.2: The DC-AC circuit configuration, drawn on MATLAB/Simulink

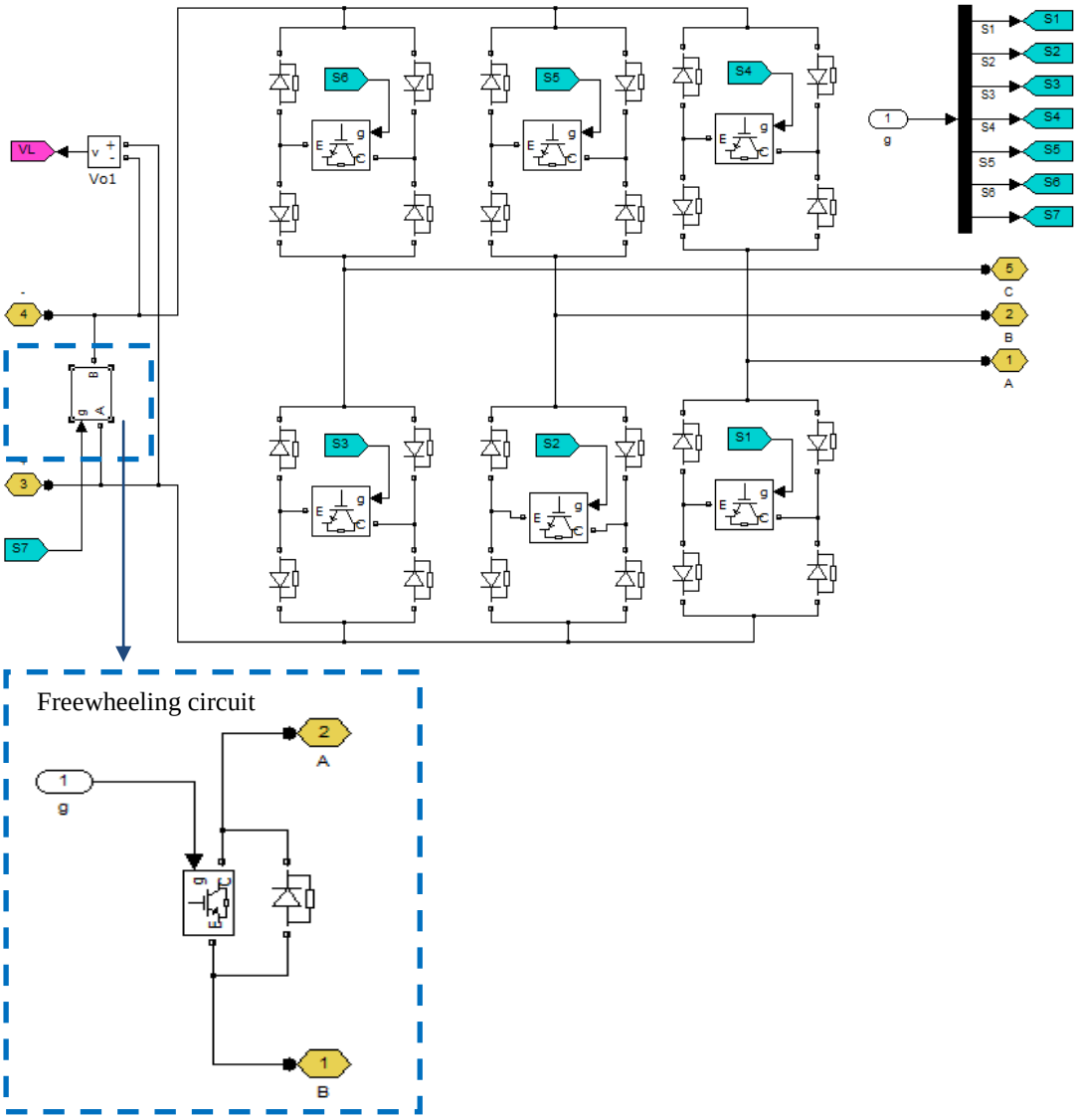


Figure 5.3: The proposed bidirectional power converter

Figures 5.4 shows the closed-loop schematic circuits of the system, involved the proposed voltage feedback controls, I-D controller (the detail of the proposed control was discussed in Chapter 4) for AC-DC operation developed in Simulink for step-changing reference, disturbance and load inputs. The schematic circuit of the proposed modulation- index-curve prediction technique is shown in Figure 5.5.

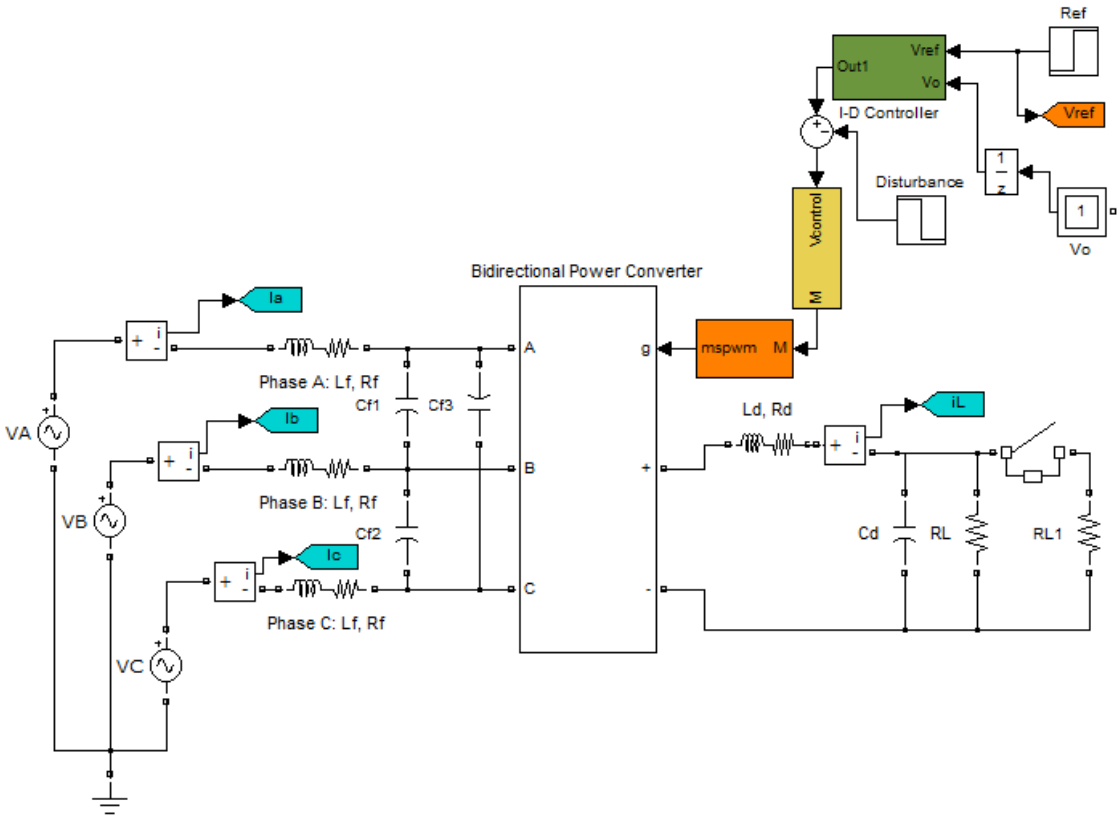


Figure 5.4: The AC-DC circuit configuration, drawn on MATLAB/Simulink, with the proposed I-D controller for step-changing of the reference/disturbance/load inputs

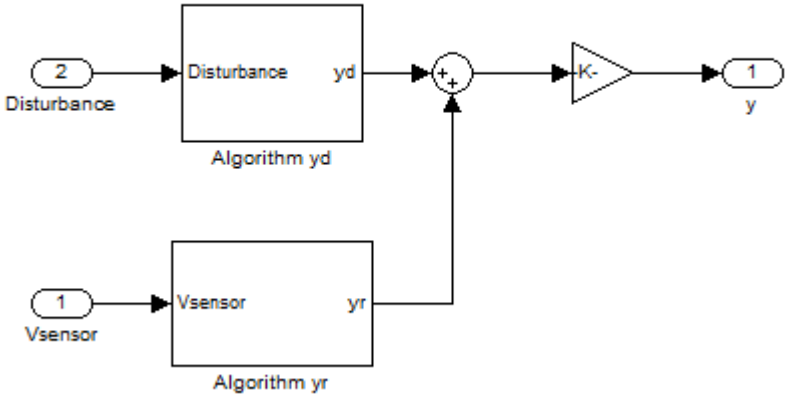


Figure 5.5: AC-DC circuit configuration with modulation-index-curve prediction control drawn in MATLAB/Simulink

5.3 Results of the Open Loop System

The simulation of open loop system was done during AC-DC and DC-AC operations for resistive (R) and inductive (R-L) loads. Its proposed circuit configuration and switching design were discussed in Chapter 3 and 4. The currents and voltages at AC and DC sides were observed. Total harmonic distortion values were also recorded.

5.3.1 AC-DC Operation

The input currents and voltage at AC side (phase A, B, C); the output voltage and currents (I_L and I_{load}) at DC side, and the bridge voltage, V_B were observed. Figures 5.6 and 5.7 respectively present AC-side and DC-side currents and voltages. The open-loop results were obtained with these specifications: modulation index M=0.85 and load resistance R=20Ω. The proposed circuit configuration and its PWM switching obtaining sinusoidal input current with near-unity power factor. The total harmonic distortion (THD) for AC mains currents and the power factor were specified as 2.8% and 0.99. Voltage and current output are 5.85A and 117V when reaching steady state. Figure 5.8 shows the variation of V_o against M in simulation and in theory (refer Equation (4.19). The graph shows V_o increasing linearly with M. In theory all parameter values are considered ideal and lossless (i.e., the input power equals the output power), thus the theoretical results differ slightly from those of the simulation (which consists voltage dropped across ESR).

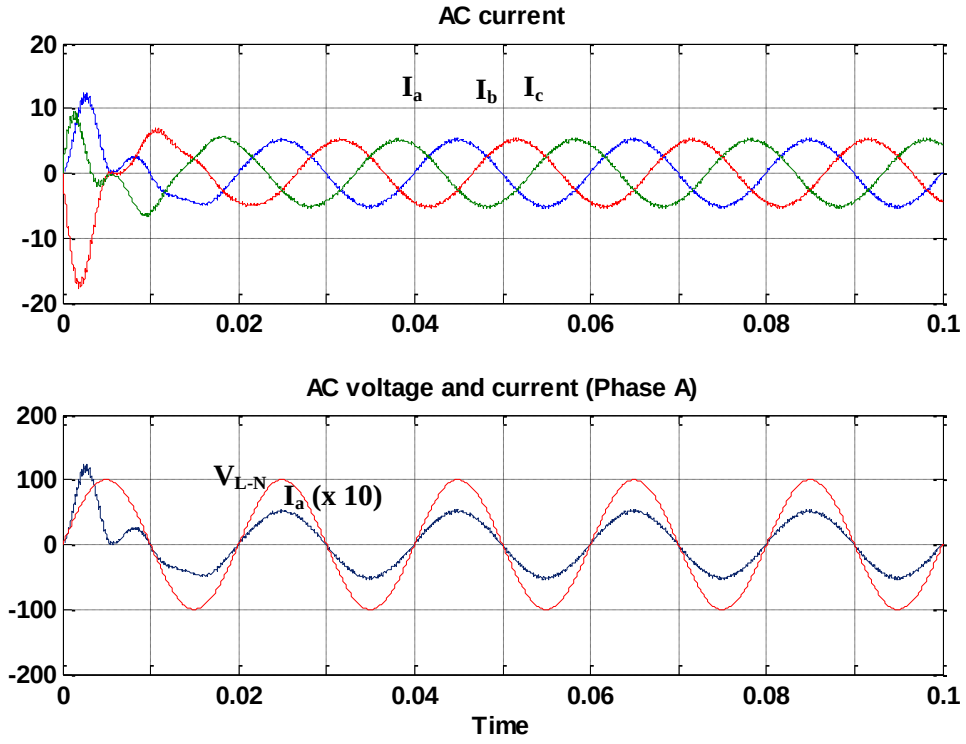


Figure 5.6: The AC-side resistive-load voltage and currents

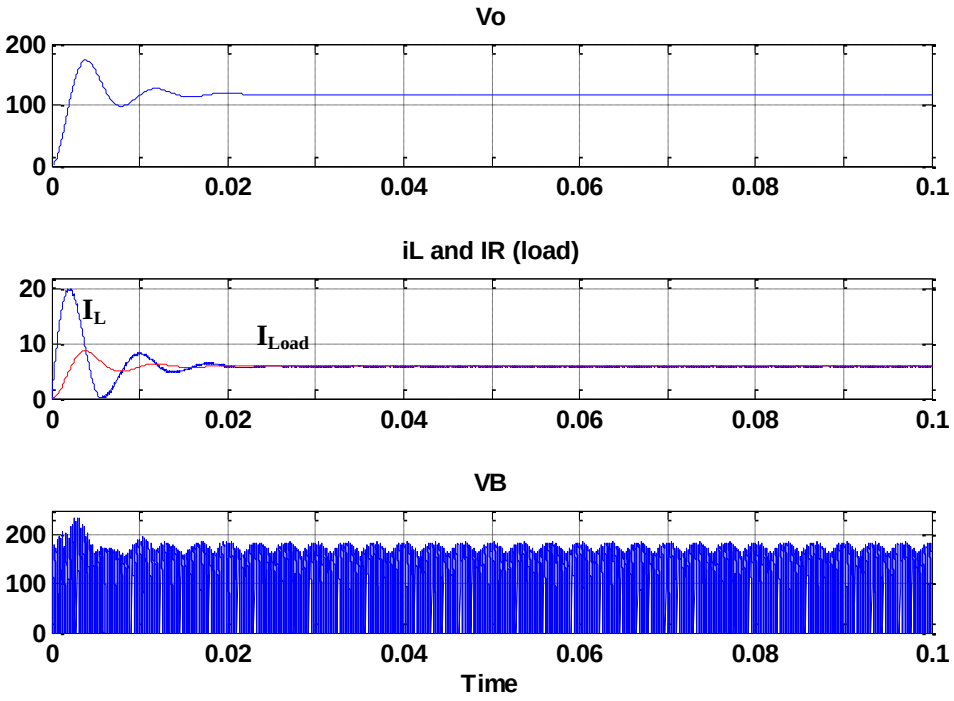


Figure 5.7: The DC-side resistive-load voltage and currents and bridge voltage (V_B)

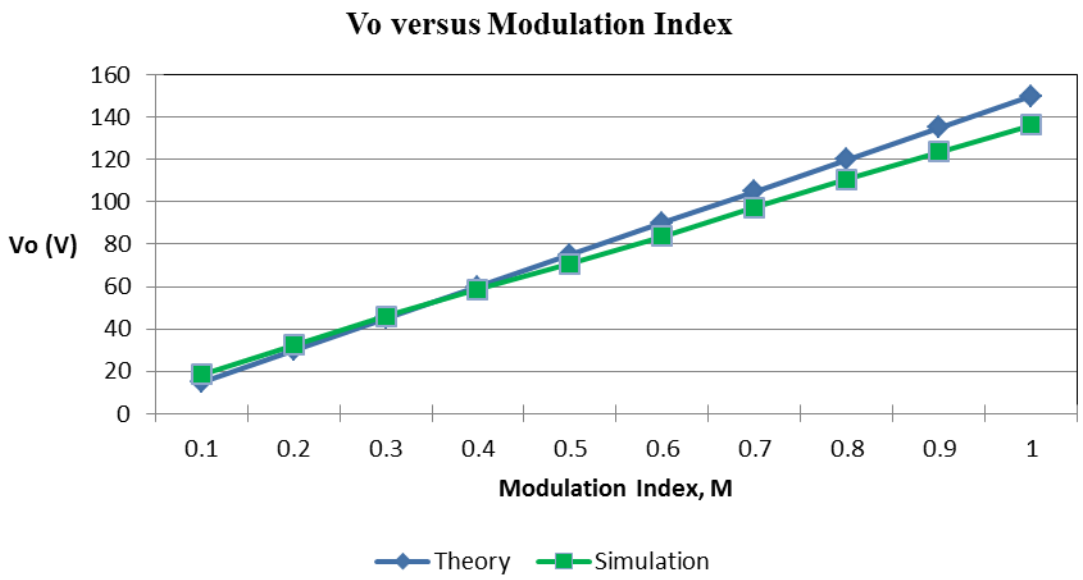


Figure 5.8: The output voltage against the modulation gain

The verification of the proposed three-phase AC-DC buck-type converter and its proposed simplified-plus-modified SPWM is then tested with an R-L load (100mH-20Ω) and M=0.85. Figures 5.9 and 5.10 respectively show the AC-side and DC-side results. The results allow conclusion that with an inductive load, the system is able to produce sinusoidal input current with near-unity power factor, and at steady state, regulated DC voltage. The DC output voltage, currents, and input–current THD (in phases A, B, and C) respectively equal 117V, 5.85A, and 2.84%. The transient response is oscillating longer than the resistive load.

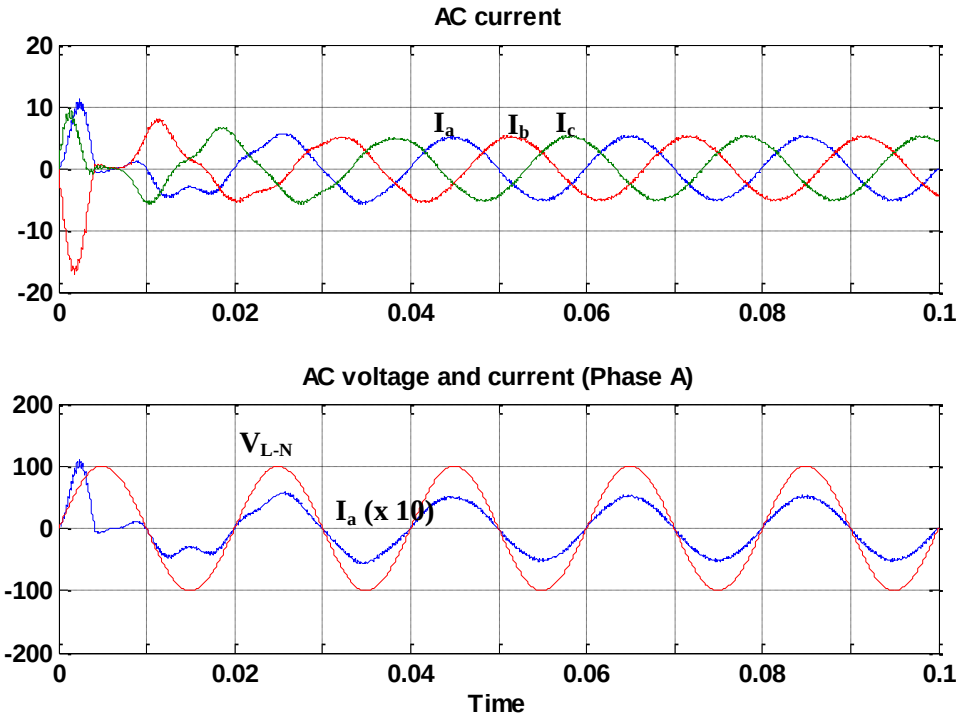


Figure 5.9: The AC-side inductive-load voltage and currents

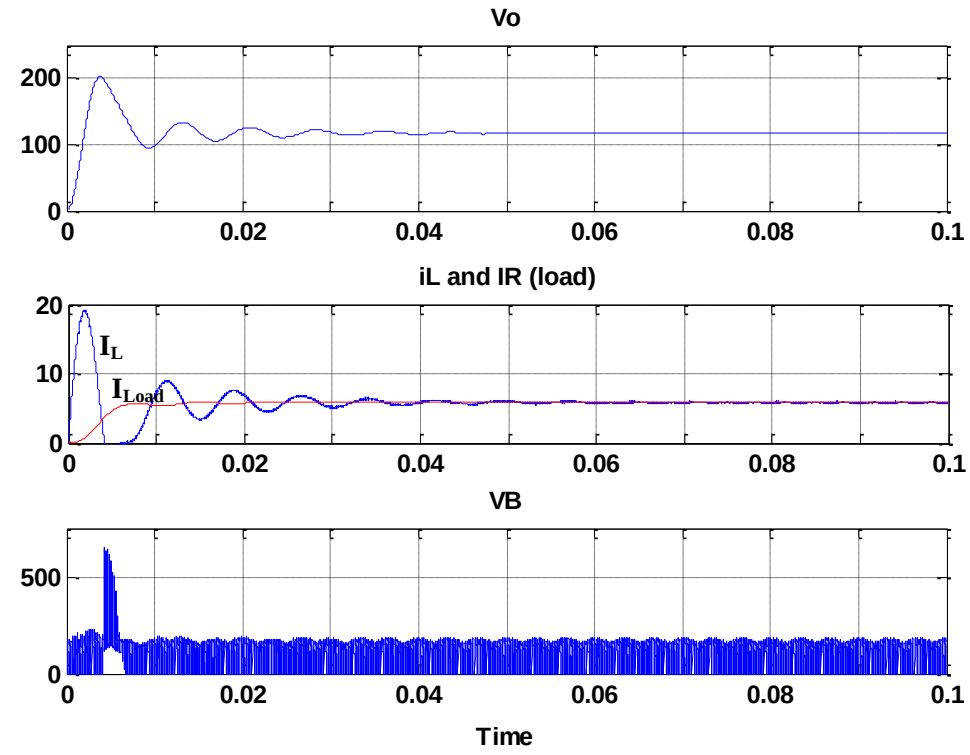


Figure 5.10: The DC-side inductive load voltage and currents and bridge voltage (V_B)

5.3.2 DC-AC Operation

The observation of output currents and voltage at AC side (in phase A, B, C); and the inductor currents I_L and bridge voltage V_B at DC side were done for DC-AC operation. Figures 5.11 and 5.12 respectively presents the AC-side and DC-side currents and voltages. The tests were run with M=0.85 and R=50Ω in each phase. The proposed circuit configuration and its PWM switching obtaining sinusoidal input currents with out-of-phase voltages (indicate the currents flow from DC to AC side). The THD of the AC voltage and currents were 2.47% and 2.47% respectively. The power factor was 0.99. The peak output voltage and currents of the output currents (in phases A, B, and C) respectively equalled 90V and 1.8A. The DC-side inductor current I_L measured 2.2A.

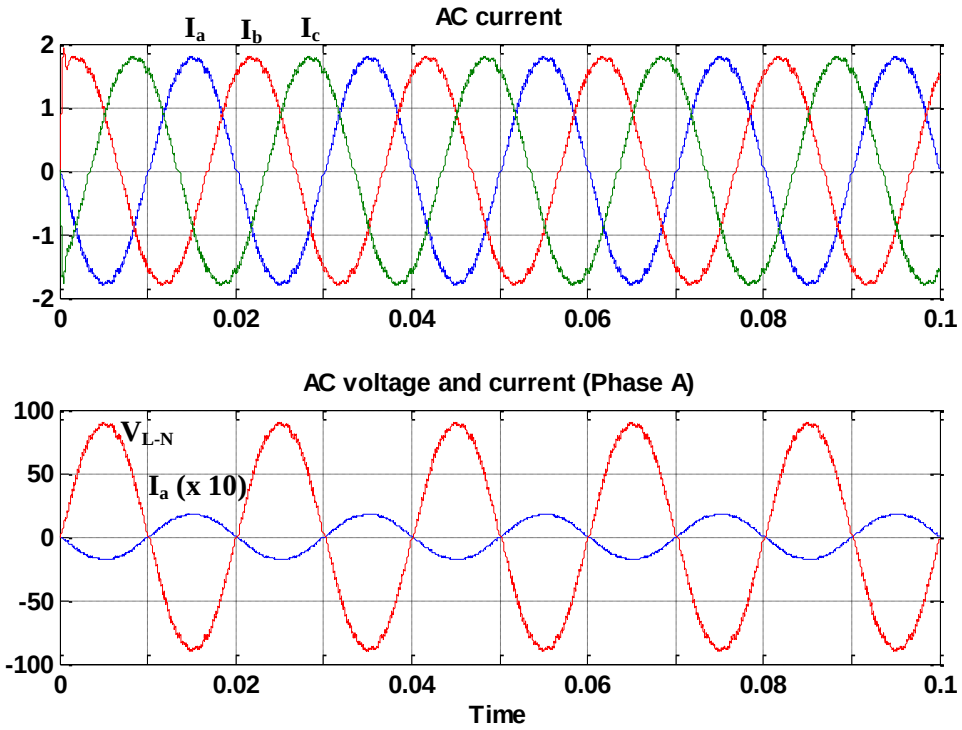


Figure 5.11: The AC-side output voltage and currents

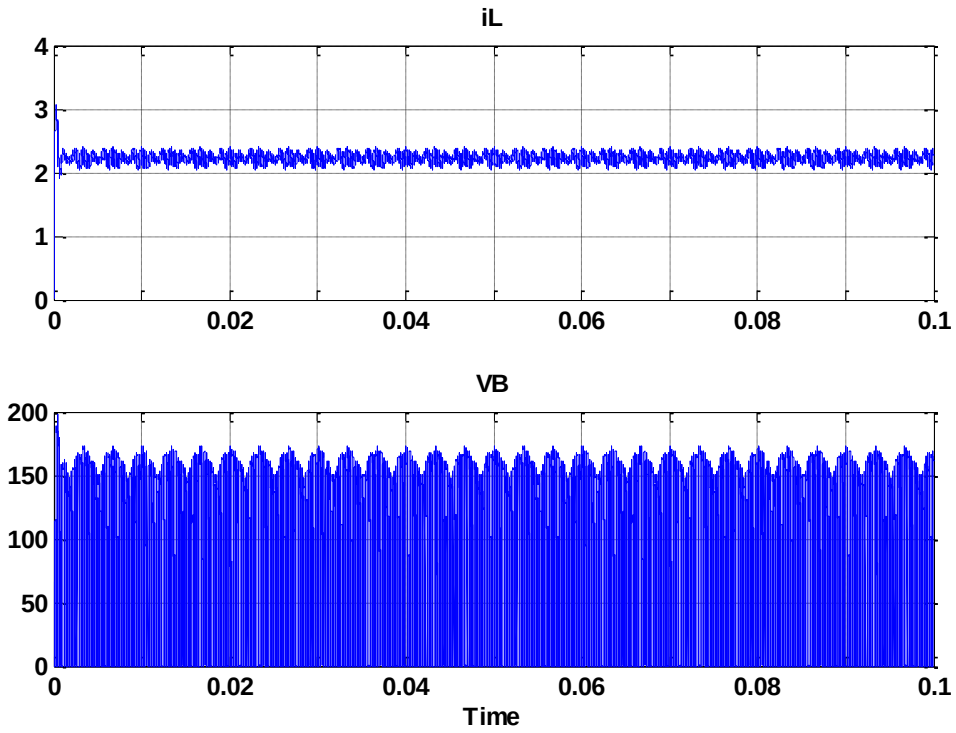


Figure 5.12: The DC-side voltage and currents and bridge voltage (V_B)

5.3.3 Comparison PWM design: Standard Switching Technique and Proposed Simplified-plus-Modified SPWM

In the standard switching technique, the modified SPWM patterns at section 60°-120° make for the "ON" pulse whenever the modulated pattern of section 0°- 60° and 120°-180° are "ON", as illustrated in Figure 5.13. The proposed simplified-plus modified SPWM technique assumes 'ON" pulse at section 60°-120° (nearer the peak of the sine wave) was comparatively studied against the standard technique (not assume "ON" state). Both the switching techniques were tested to the same conditions (M=0.9, R=50Ω) for AC-DC power flow. The result indicates that the proposed technique has advantages: lower THD value (see Figure 5.14 (a) and (b)), simpler switching design implementation, and low switching losses because the maximum switching frequency

was 20kHz. The standard technique used 40kHz switching frequency to generate the PWM pattern at Section 60°-120°. Higher switching frequencies would produce higher switching losses (Holtz, 1994).

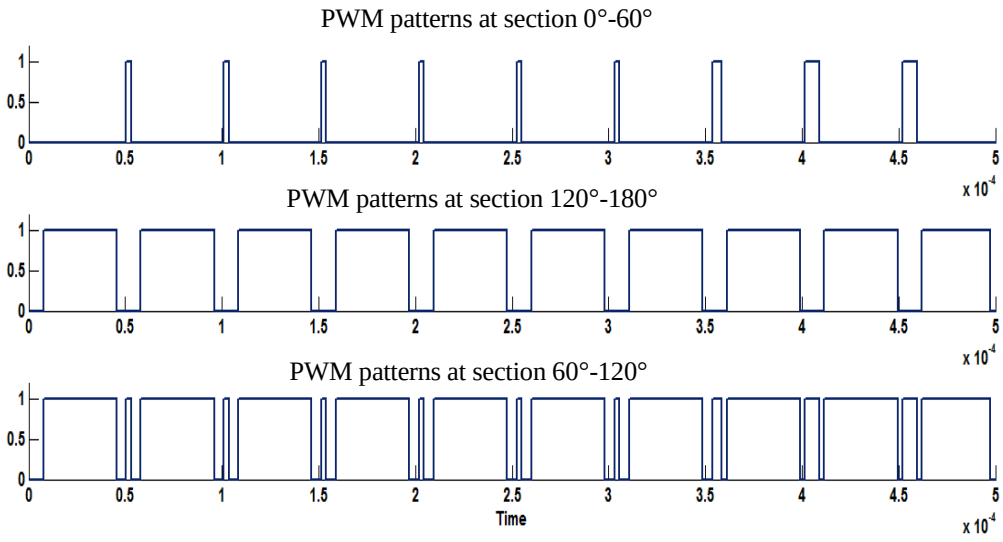
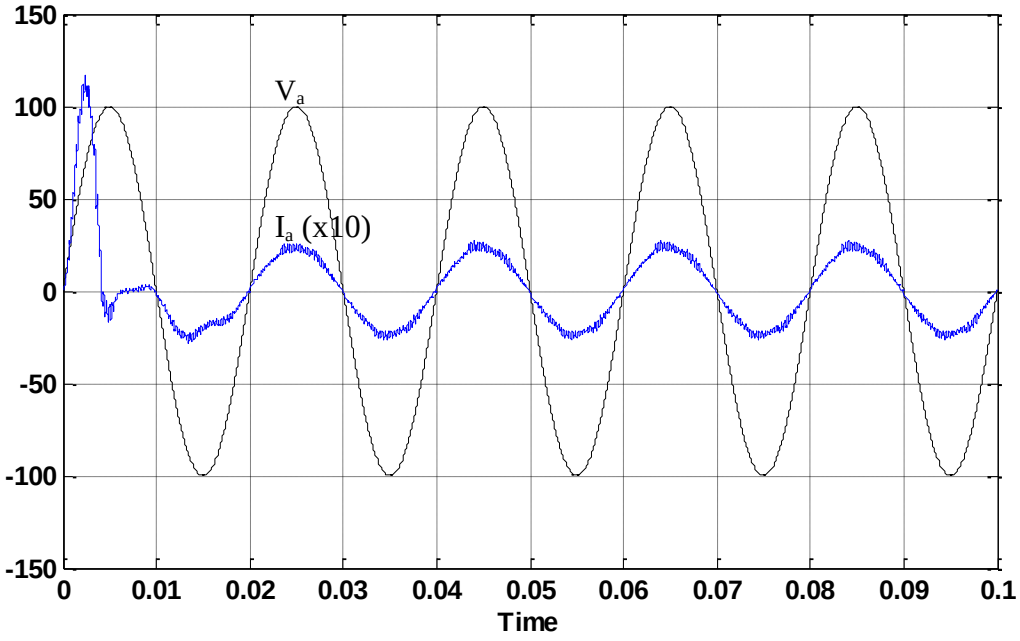
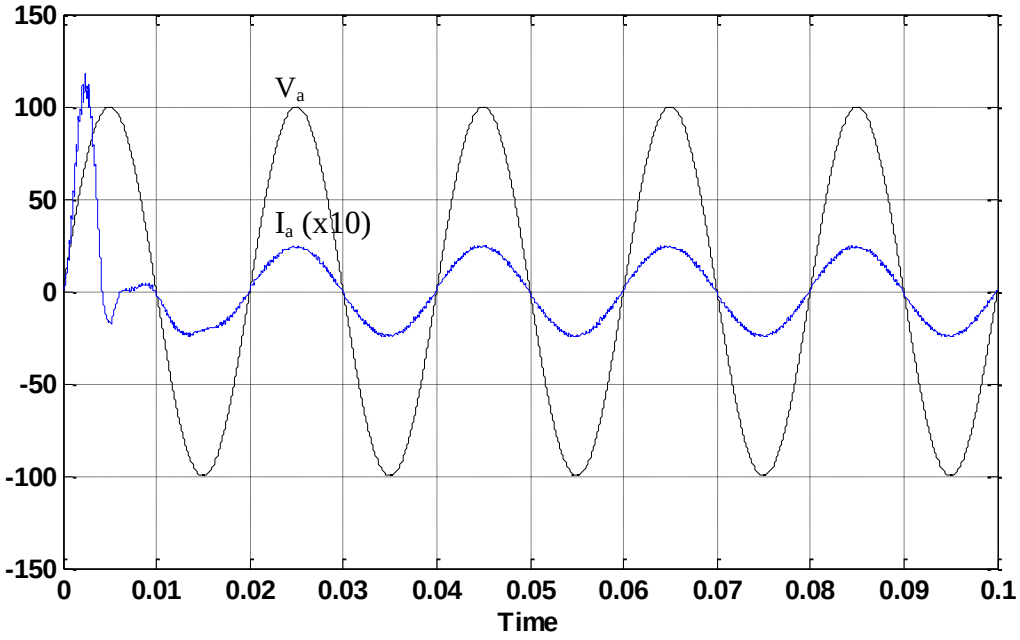


Figure 5.13: Standard SPWM switching patterns

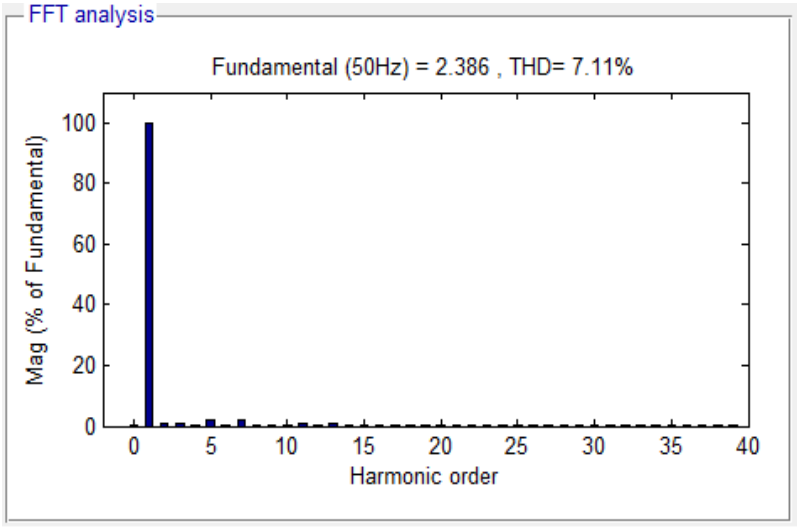


(a)

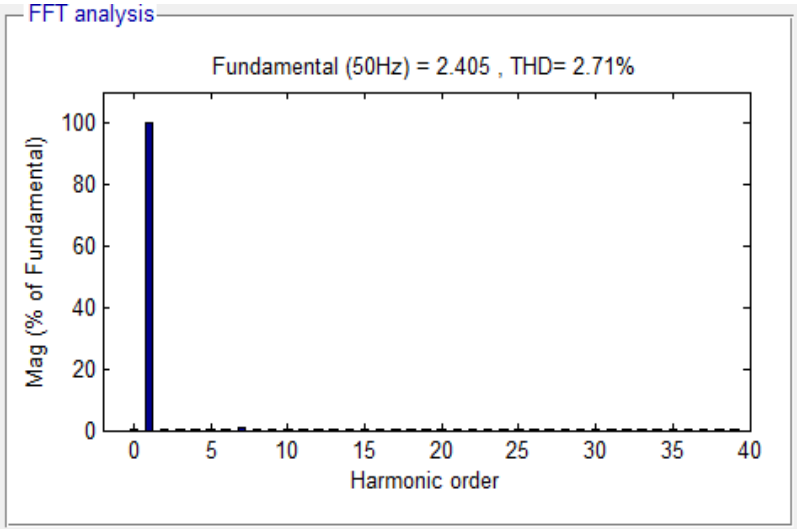


(b)

Figure 5.14(a): The waveforms of AC side (V_a and I_a) on: (i) the standard switching technique, (ii) the proposed switching technique



(a)



(b)

Figure 5.14(b): The AC-line-current THD percentage and on: (i) the standard switching technique, (ii) the proposed switching technique

5.4 Results of the Closed-loop System: the Proposed I-D Controller and the Modulation-Index-Curve Prediction Technique

The closed loop system was simulated during its AC-DC operation with resistive (R) and inductive (R-L) loads. Two techniques proposed for it are I-D controller, which is extended into M-curve-prediction. Both techniques showed similar responses in the linear analysis (refer to Chapter 4). The AC-side and DC-side currents and voltages were observed for stepped-up and stepped-down reference input and loads, and against integral gain values K_I. The test by giving a step-changed in disturbance input was also provided. For comparison, results of system without feedback controller were simulated under section 5.4.1; results of system with I-D controller and Modulation-Index-Curve Prediction Technique were demonstrated under section 5.4.2 and 5.4.3, respectively.

5.4.1 Result of Uncompensated system

The simplified-plus-modified SPWM design achieved near-unity power factor and provided steady-state system stability but not the desired transient response. To prove it, simulation tests in three transient conditions were done by step-changing the reference voltage from 20V to 120V with resistive (50Ω) and inductive (160mH-20Ω) loads, and step-changing the load from 100Ω to 50Ω. Calculation for M was based on (Equation 3.11), and assumed $V_{B(average)} = V_o$ (equals input and output powers).

Figures 5.15-5.17 show the simulation results for the phase-A voltage-source V_{L-N} and current-source I_a, the dc-voltage output V_o, the inductor dc-current I_L, and the values of M in the three transient cases. High (more than 35%) overshoot in the output voltage V_o and inductor current I_L was shown in all the cases, stressing the semiconductor current. In the third case, V_o and I_L oscillated longer before stabilizing. The settling time in the

first and third cases was 25ms, in the second case 40ms due to the added of inductive load (R-L) resonating with capacitance C_d. Steady-state error was present in all cases because of non-ideal components. The drawbacks shall now be addressed by voltage feedback control.

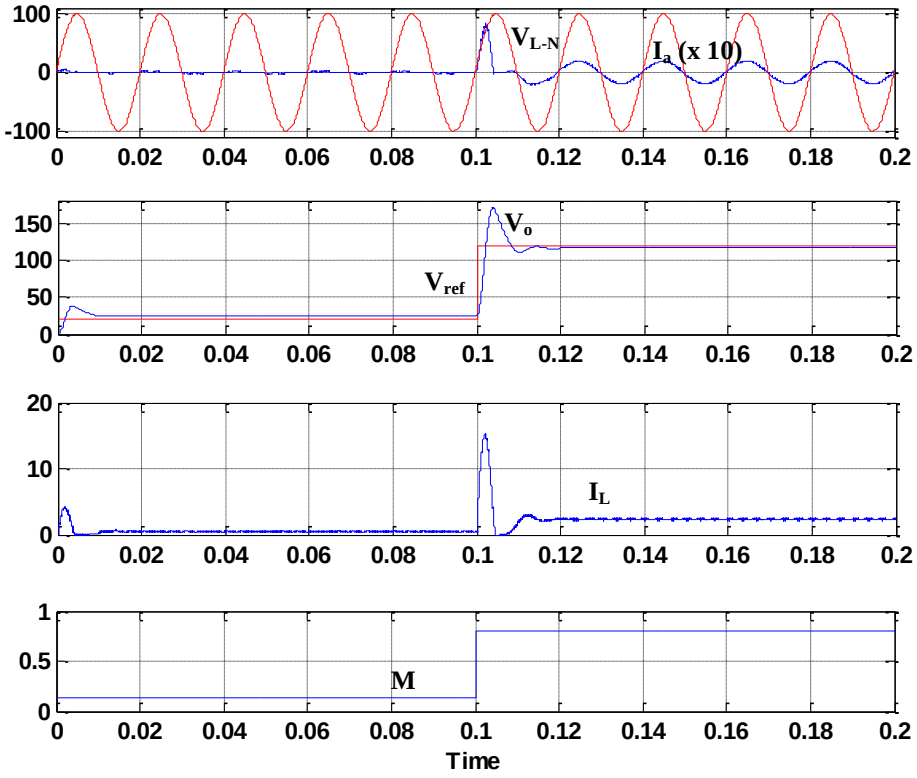


Figure 5.15: The uncompensated step response: V_{ref} is changed in the load resistance R

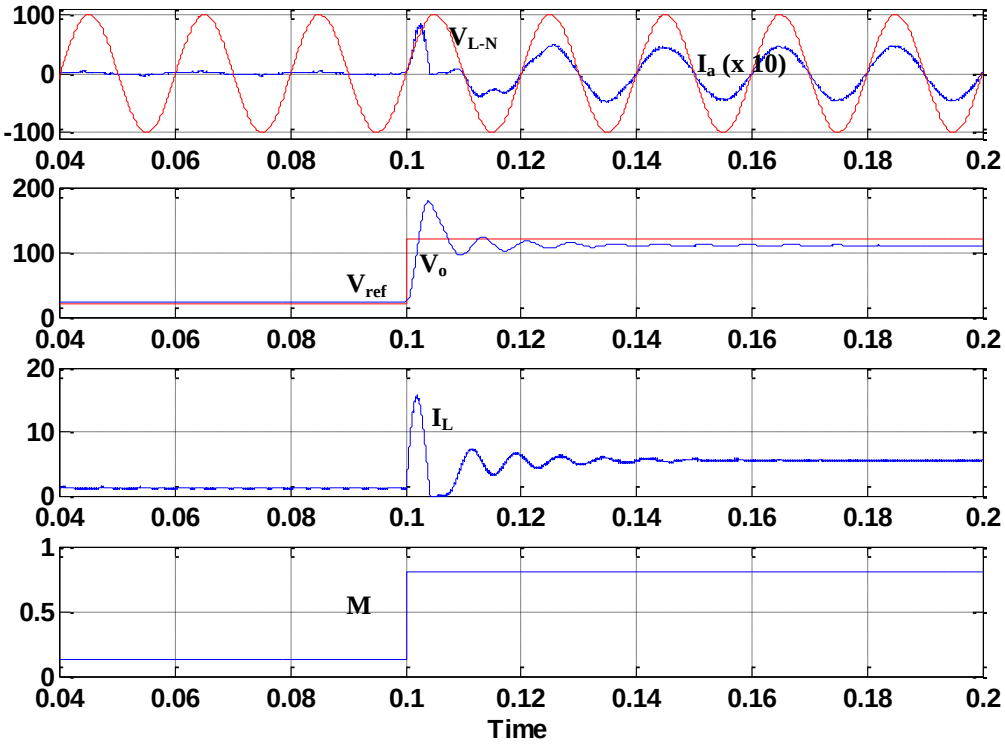


Figure 5.16: The uncompensated step response: V_{ref} is changed in the load inductance (R-L)

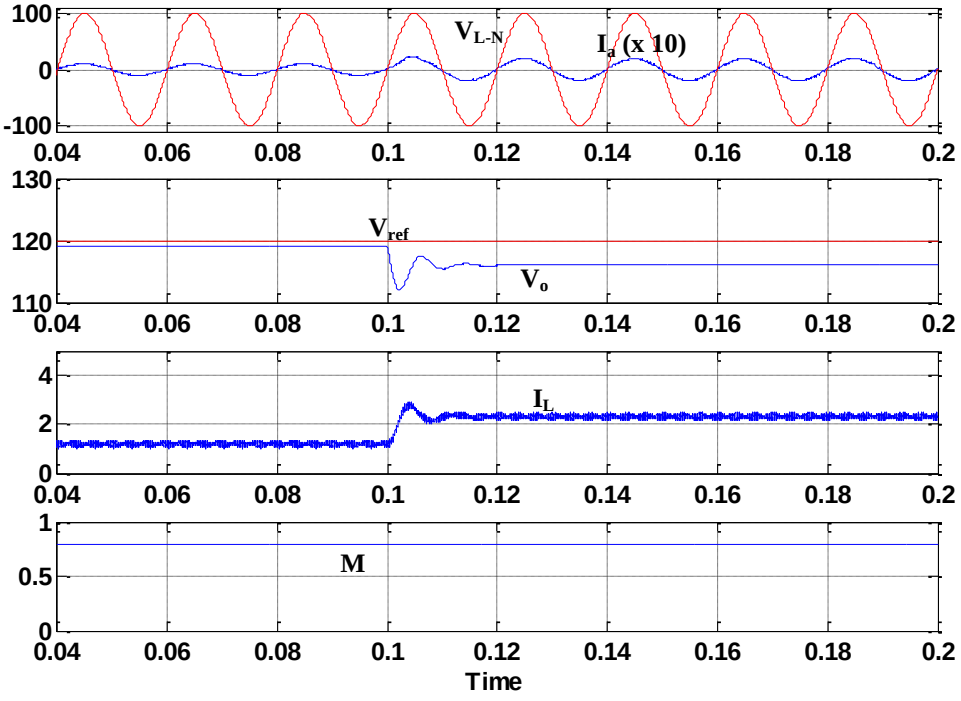


Figure 5.17: The uncompensated step response: the resistance load is reduced

5.4.2 I-D Controller Results

The main objectives of the controller design are to obtain zero steady-state error in the output voltage (V_o=V_{ref}) despite any step-changes to the reference and load and to compensate for the huge voltage/current in the system. Results show that the controller is able to track the reference voltage with zero steady-state error while compensating for the huge starting voltage/current. In practice, however, tuning to a suitable K_I may be preferred to reduce the current stress on the semiconductors during transients (Alberto Alesina & Venturini, 1981). A fast and lightly damped system gives a fast step response but with the consequence of large-amplitude capacitor-charging current.

5.4.2.1 Analysis of the reference and load step-up changes

The tests on the I-D control algorithm were done in three transient conditions: step-changing the reference voltage from 20 V to 120 V with resistance and inductive loads, and step-changing the load from 50Ω to 100Ω. The tests were done with feedback integral gain K_I =100. Figures 5.18 to 5.20 shows the results for $V_{L\text{-}N}$, I_a, V_o, I_L, and M for the three cases, where (a) V_{ref} is changed in resistance load (50Ω); (b) V_{ref} is changed in inductive load (160mH-20Ω); and (c) resistance load is changed (50Ω to 100Ω), respectively.

Compared (Figure 5.18-5.20) with the uncompensated tests (Figure 5.15-5.17), the overshoot percentage (%OS) of V_o and I_L were reduced to almost zero in the first two cases and to below 5% in third case. The settling time (V_o) in all cases was below 30ms. The I-D controller was able to compensate the steady-state error in all cases.

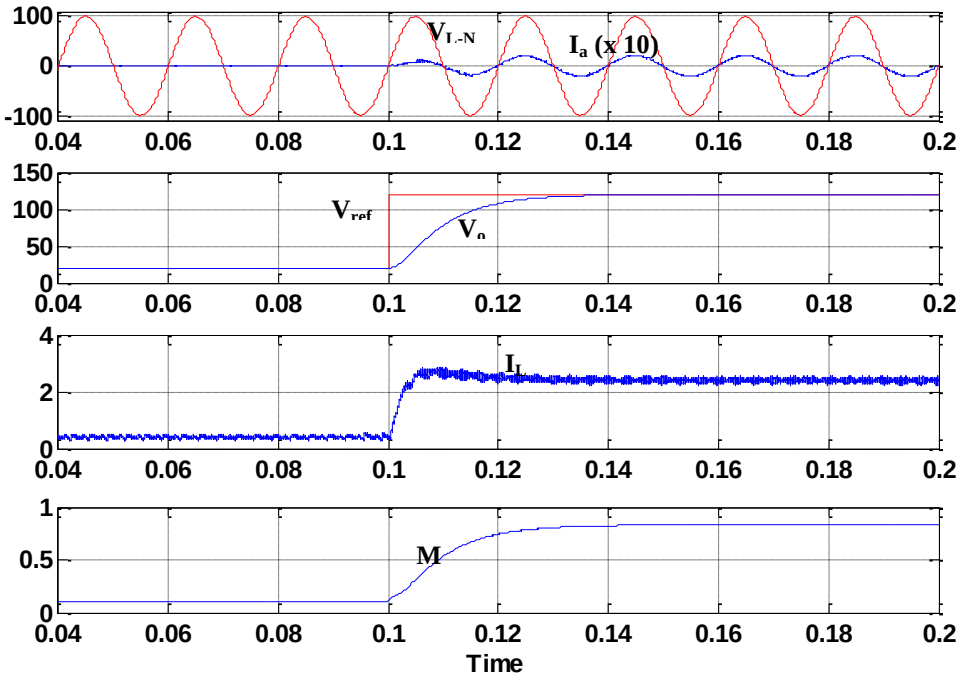


Figure 5.18: The compensated step-up response when the reference was changed for R load at t = 0.1s

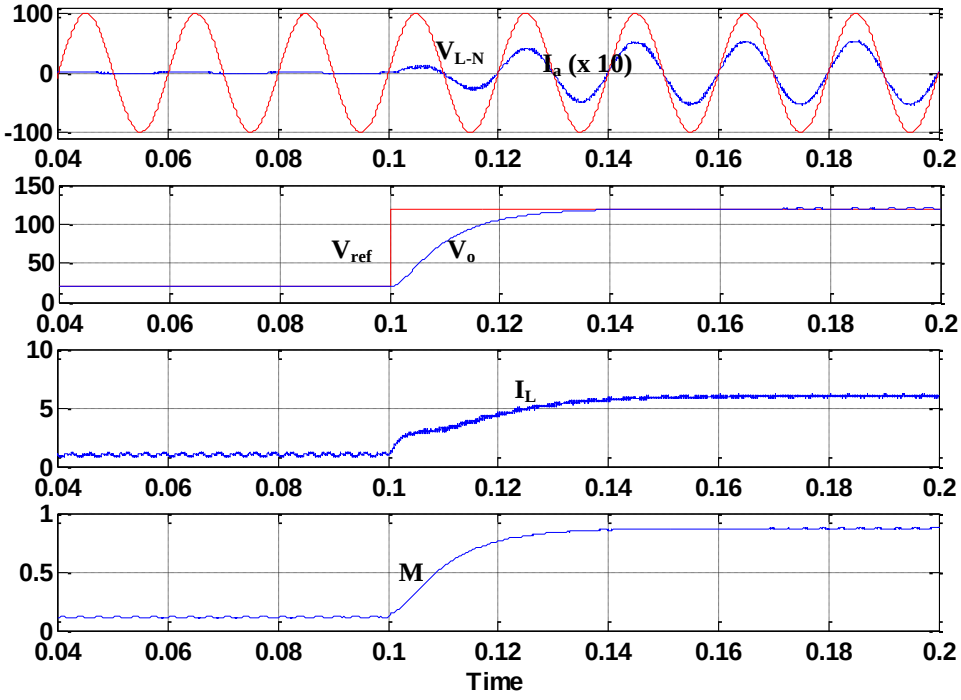


Figure 5.19: The compensated step-up response when the reference was changed for R-L load at t = 0.1s

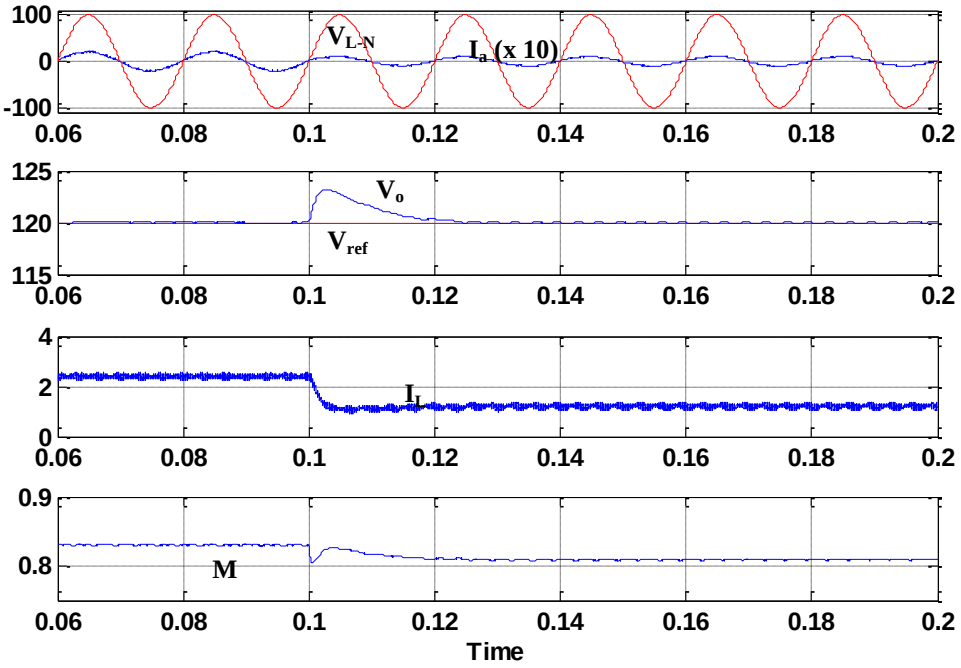


Figure 5.20: The compensated step-up response when the load R was changed at t = 0.1s

5.4.2.2 Analysis of the reference and load step-down changes

The step-down tests on the I-D control algorithm were done by step-changing the reference voltage down from 120V to 80V through the resistance and the inductance, and step-changing the load down from 100Ω to 50Ω. The tests were done with feedback integral gain K_I =100. Figures 5.21-5.223 show the results for V_{L-N}, I_a, V_o, I_L, and M for the three cases, where (a) V_{ref} is changed in the resistance load (50Ω); (b) V_{ref} is changed in the inductive load (160mH-20Ω); and (c) the resistance load is changed (100Ω to 50Ω). The controller is able to track the system reaching zero steady-state error in a better transient response (smaller %OS and low settling time) for all the step-down cases.

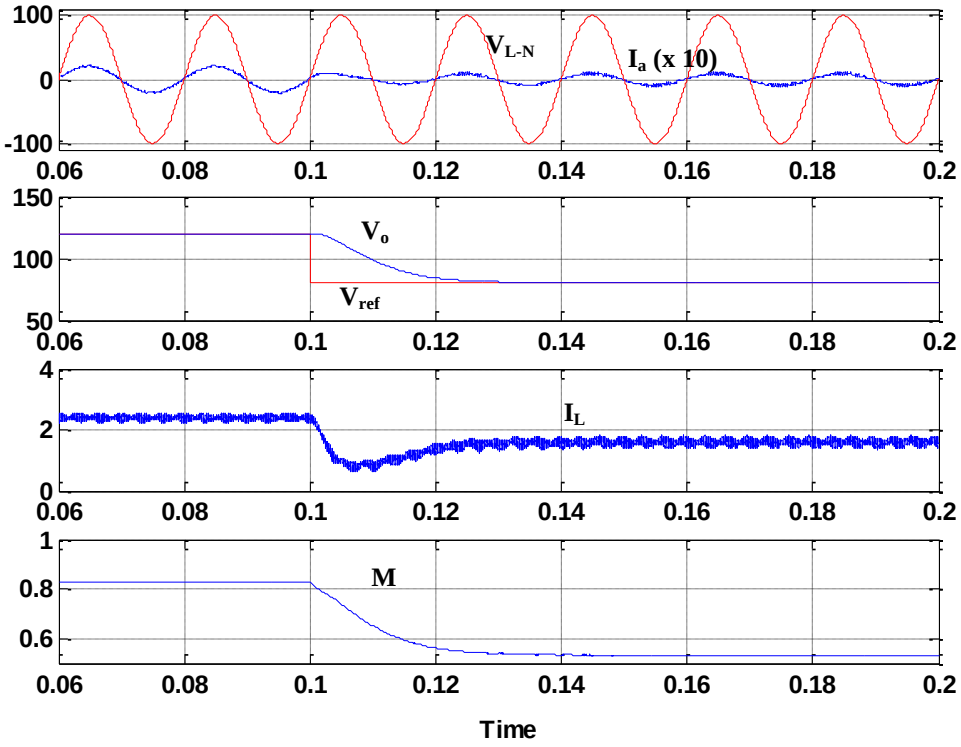


Figure 5.21: The compensated step-down response when the reference was changed at t = 0.1s for R load

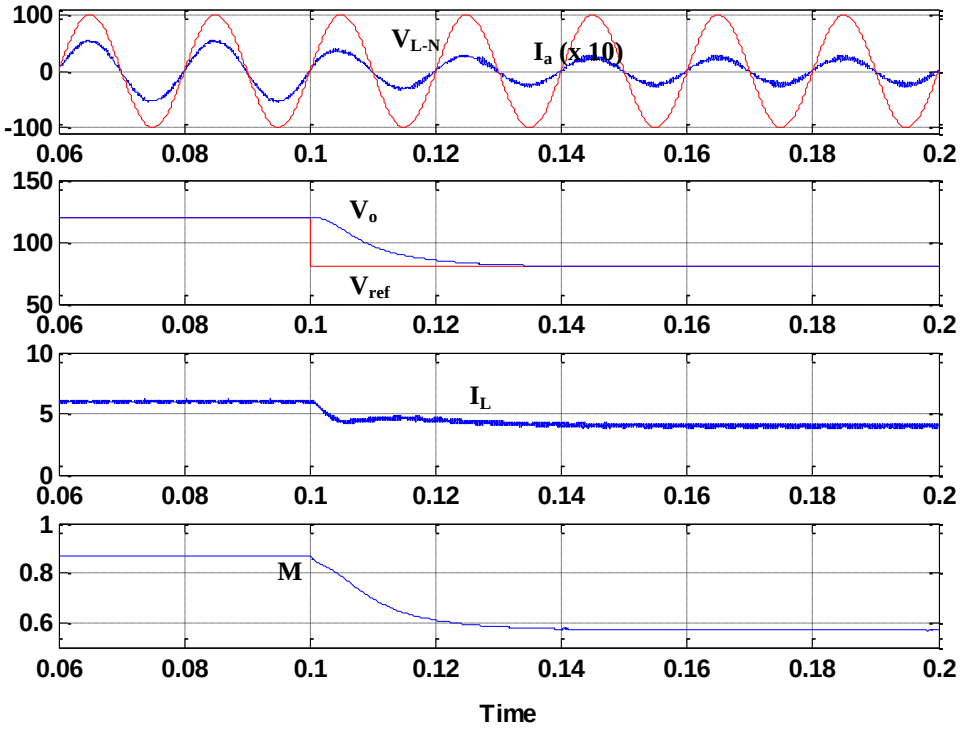


Figure 5.22: The compensated step-down response when the reference was changed at t = 0.1s for R-L load

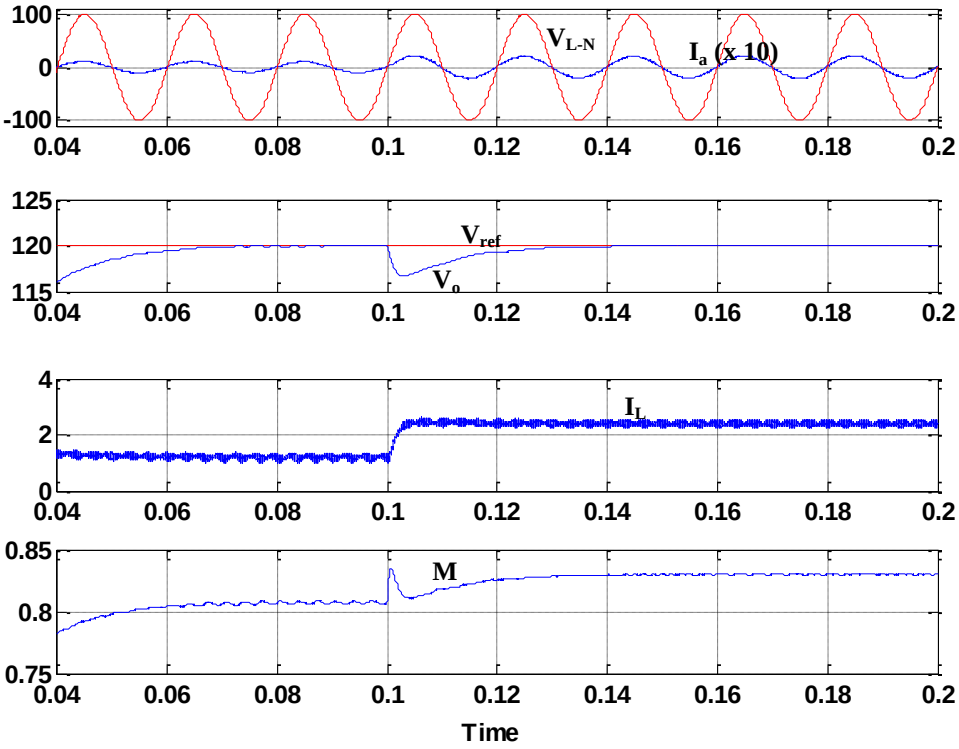
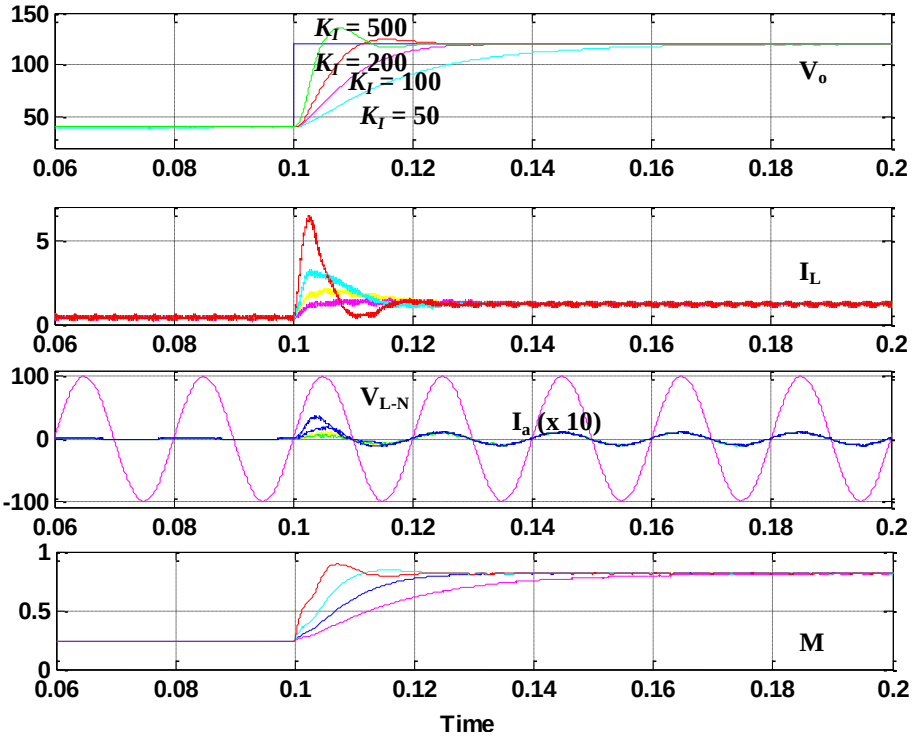


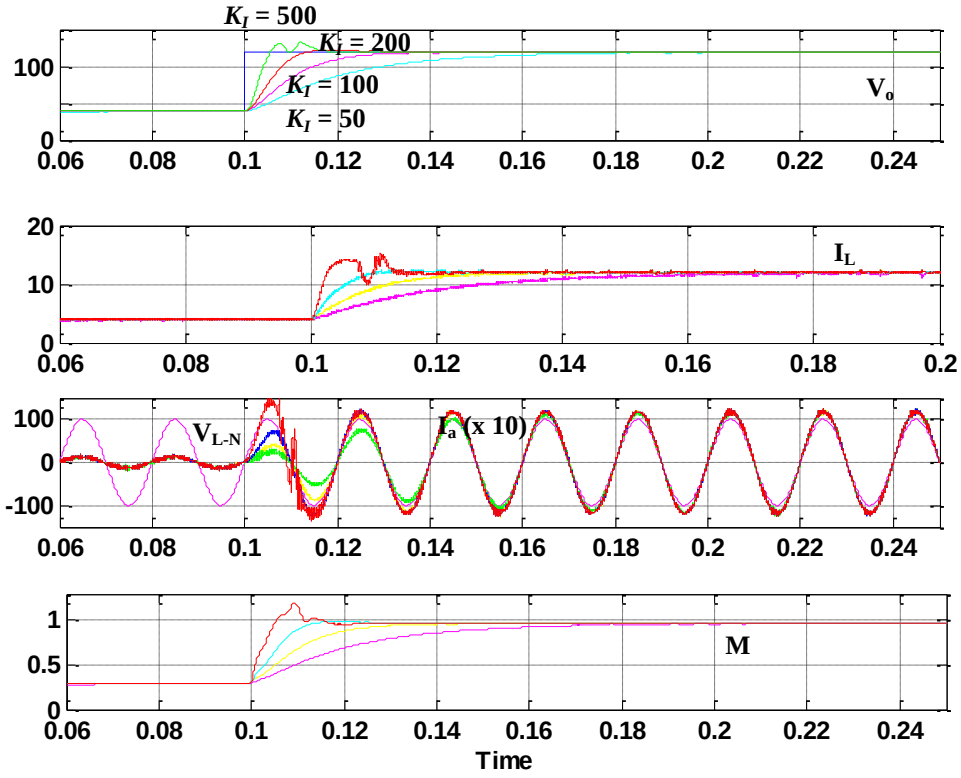
Figure 5.23: The compensated step-down response when the load R was changed at t = 0.1s

5.4.2.3 Analysis of the reference voltage step-up changes with K_I

Transient-response tests on reference-voltage step change were done for K_I = 50, 100, 200, and 500 and R=100Ω and 10Ω. Figures 5.24(a–b) show the results for V_{L-N}, I_a, V_o, I_L, and M against the values of R and K_I. The response was faster and the overshoot larger when K_I increased. The optimum design can be achieved by selecting a gain suitable to the load value. Referring to Figure 5.24(b), when K_I = 500, the modulation index exceeds 1 (overmodulated) during the transient state. It shows that the gain K_I of 500 is not a suitable gain to be chosen for load resistor 100Ω, but the gain value is suitable for load resistor 10Ω.



(a)



(b)

Figure 5.24: The compensated step response when the reference was changed at t = 0.1s for loads: (a) R=100 Ω, (b) R=10 Ω, against values of K_I

5.4.2.4 Analysis of the load-resistance step-up change against K_I

The transient-response tests on step changes in the load resistance were done with small values and large values, with controller gain K_I = 50, 100, 200, and 500. The load resistances R were 100Ω to 35Ω at 0.1s and 35Ω to 30Ω at 0.17s. Figure 5.25 shows the results for output voltage (V_o), inductor current (I_L), input voltage and current ($V_{L\text{-}N}$ and I_a), and modulation gain (M), against values of the load resistance and K_I. The controller is able to track the system to reach zero steady-state error faster with suitable controller gain in load tests (small and large values of loads).

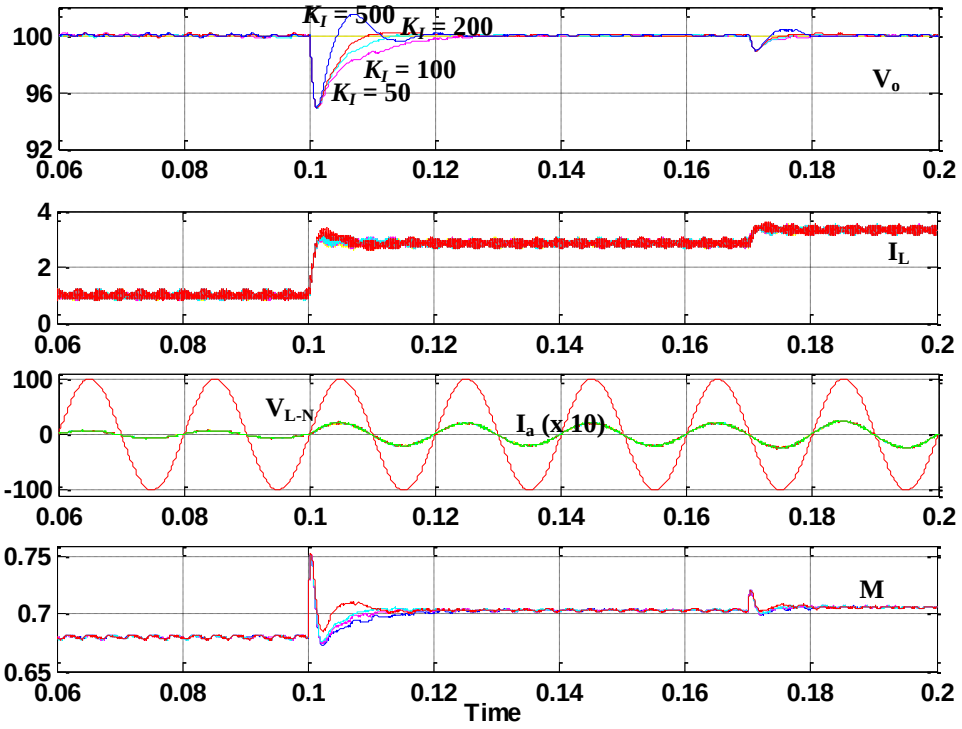


Figure 5.25: The compensated step response when the resistance load was changed (from 100Ω to 35Ω and then to 30Ω) at t=0.1s and 0.17s, against values of K_I

5.4.2.5 Analysis of the disturbance voltage step-change

The tests on the I-D control algorithm were done by step-changing the disturbance voltage from 0V to -20V (case I) and 0V to 20V (case II) through the resistance 50Ω. The test was done with feedback integral gain K_I =100 and V_{ref} = 100V. Figures 5.26 and 5.27 show the results for $V_{L\text{-}N}$, I_a, V_o, I_L, and M. The controller is able to track the system reaching zero steady-state. The M curves dropped (case I) and climbed-up (case II) speedily (about 0.001s), before following the V_o curves.

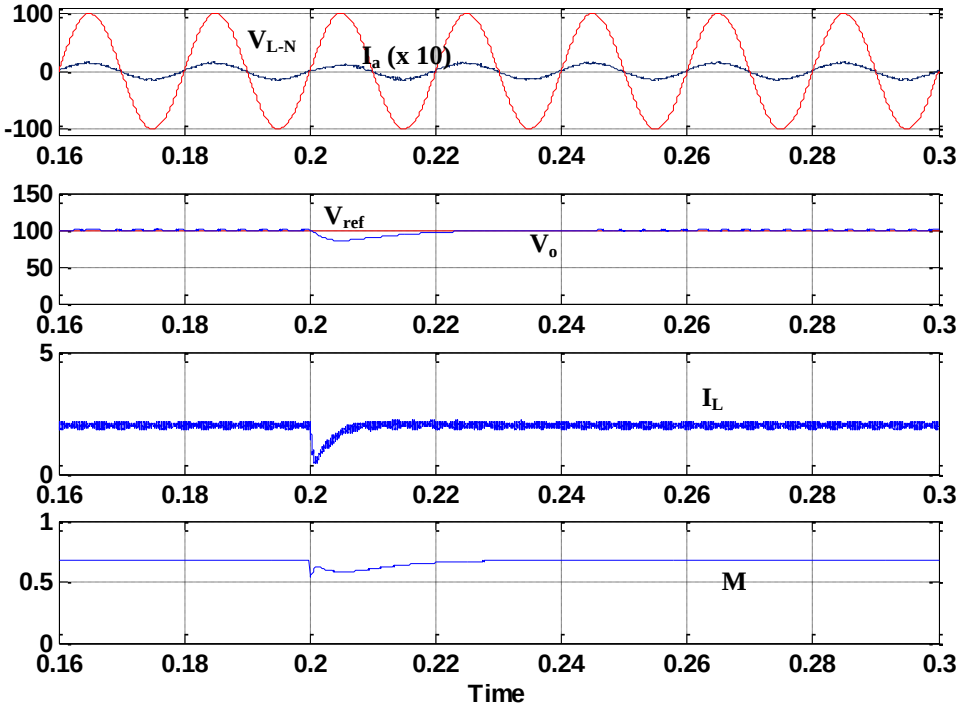


Figure 5.26: The compensated response when disturbance (-20V) was given at t = 0.2s for R load

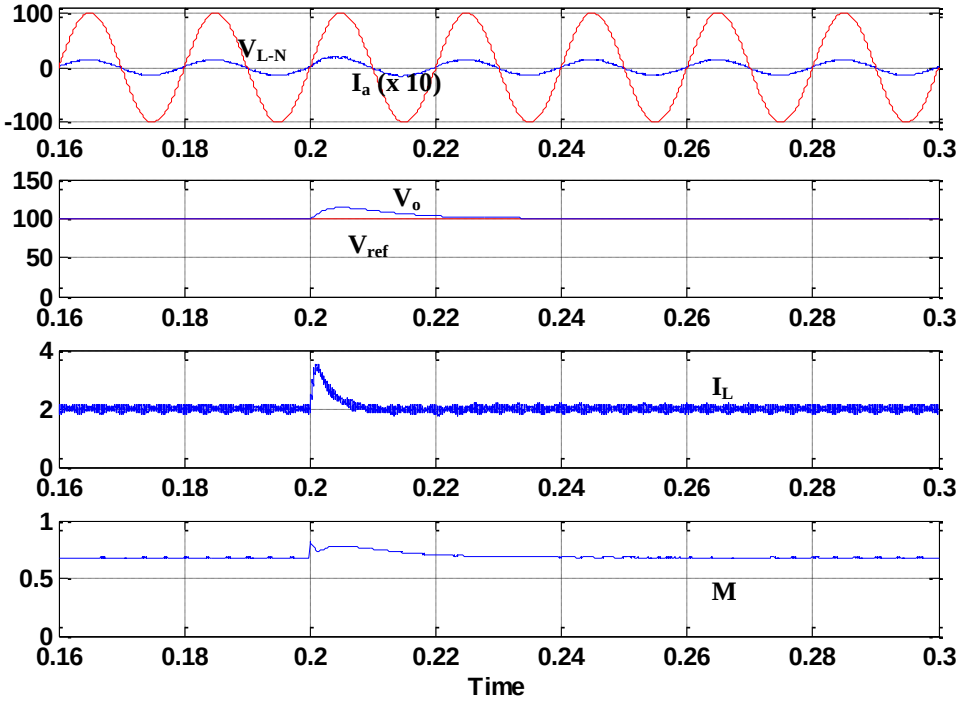


Figure 5.27: The compensated response when disturbance (20V) was given at t = 0.2s for R load

5.4.3 Results of the M-Curve Prediction Technique

The test was performed to verify the M-curve prediction control algorithm obtained in Chapter 4. The results show the controller able to track the reference voltage with steady-state error (below than 5%) while compensating the huge starting voltage/current. The sinusoidal input currents in phase with main AC source voltages.

5.4.3.1 Analysis of the reference step-up changes

The tests on the M-curve prediction control algorithm (based on Equation 4.21) were done in three transient conditions: step-changing the reference from 20V to 120V with resistance and inductive loads. Figures 5.28 to 5.29 show the results for $V_{L\text{-}N}$, I_a, V_o, I_L, and M for two cases: V_{ref} is changed in the load resistance (50Ω); and V_{ref} is changed in the load inductance (160mH-20Ω). The controller was able to track the reference in good transient response (case I: no overshoot voltage and time settling 35ms and case II: no overshoot and settling time 25ms) and small steady-state error in the step-up cases (Case I: 3.3% and Case II: 5.8%). The maximum value and the settling time of I_L respectively were 2.9A and 25ms for case I. In case II I_L shows no overshoot current and the settling time was 35ms due to the inductance has a filtering effect and also it contributes to time delay.

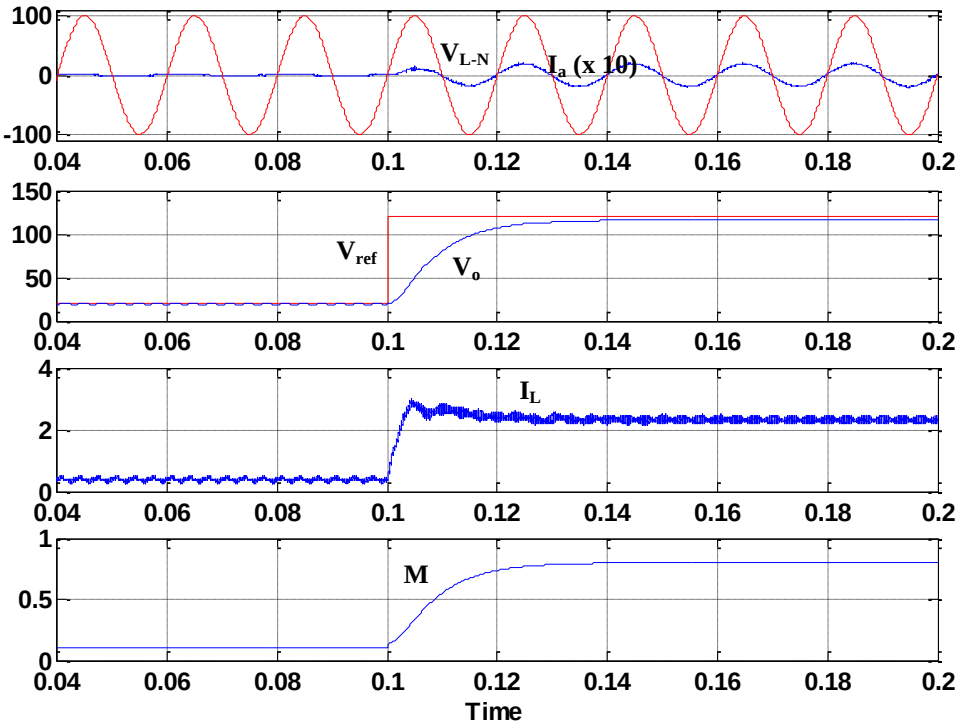


Figure 5.28: The compensated step-up response when the reference was changed at t = 0.1s for R load

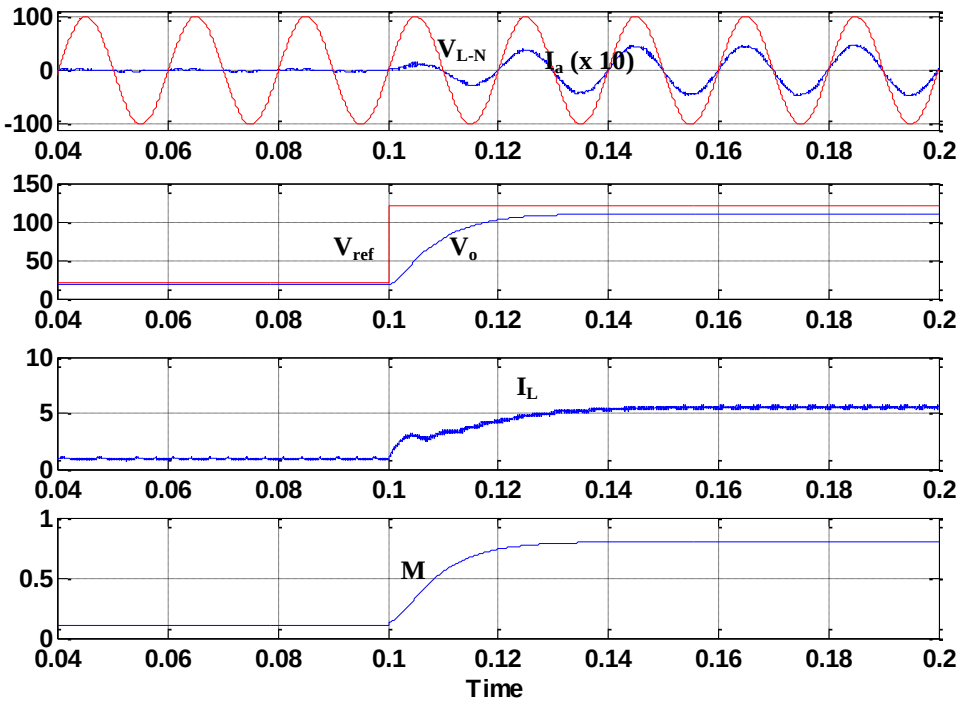


Figure 5.29: The compensated step-up response when the reference was changed at t = 0.1s for R-L load

5.4.3.2 Analysis of the reference step-down changes

The step-down tests on the prediction M curve control algorithm were done by step-down changing the reference voltage from 120 V to 80 V with resistive and inductive loads. Figures 5.30 and 5.31 show the results of V_{L-N}, I_a, V_o, I_L, and M for cases, where (a) V_{ref} is changed in resistance load (50Ω); and (b) V_{ref} is changed in inductive load (160mH-20Ω) respectively. The controller was able to track the reference in good transient response (case I: no overshoot voltage and time settling 25ms and case II: no overshoot and settling time 25ms) and small steady-state error in the step-down cases (Case I: 0% and Case II: 5%). The settling times of I_L were 15ms and 20ms for case I and case II.

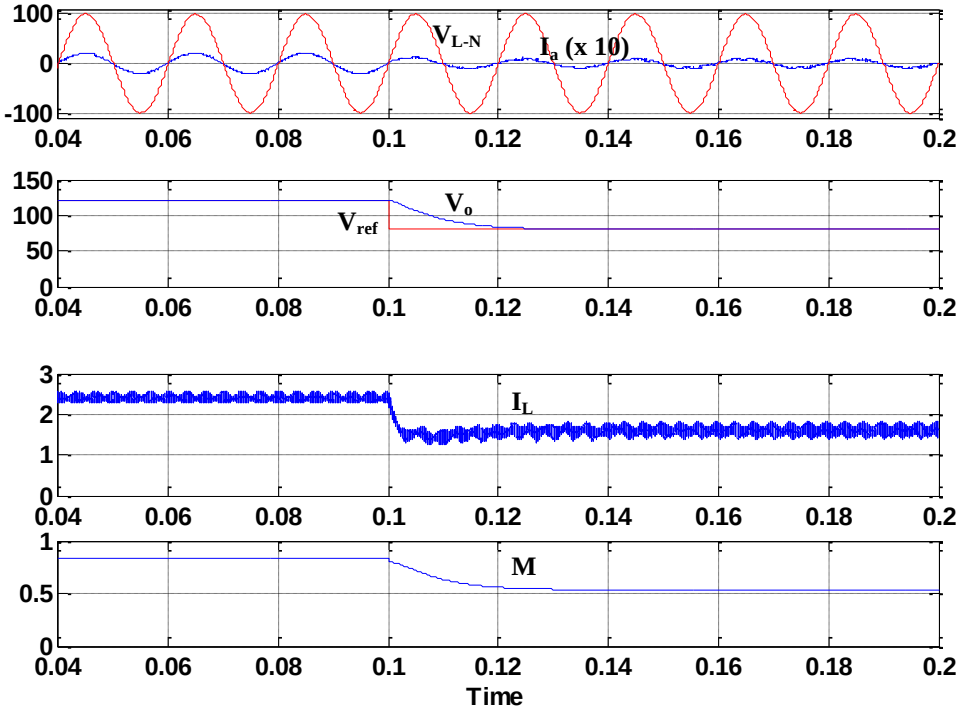


Figure 5.30: The compensated step-down response when the reference was changed for R load at t = 0.1s

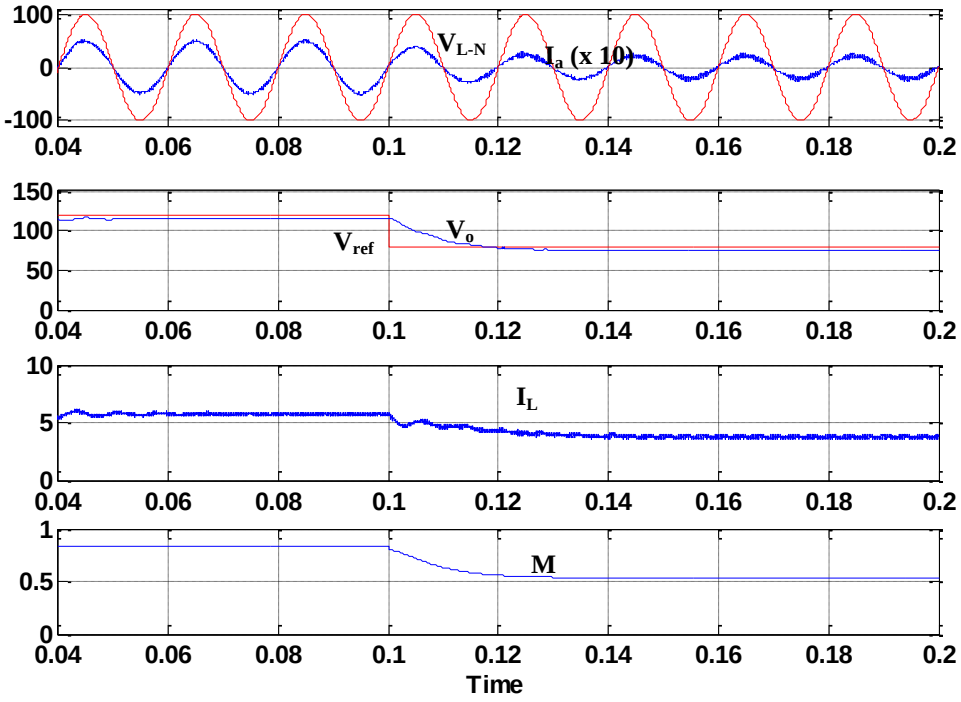


Figure 5.31: The compensated step-down response when the reference was changed at t = 0.1s for R-L load

5.4.3.3 Analysis of the disturbance voltage step-change

The tests on the M-curve prediction control algorithm were done by step-changing the disturbance voltage from 0V to 20V (case I) and 0V to -20V (case II) through the resistance 50Ω. The tests were done with V_{ref} = 120V. Figures 5.32 and 5.33 show the results for V_{L-N}, I_a, V_o, I_L, and M. The controller is able to track the system reaching zero steady-state in good transient response. The settling times were 15ms and 10ms for case I and case II.

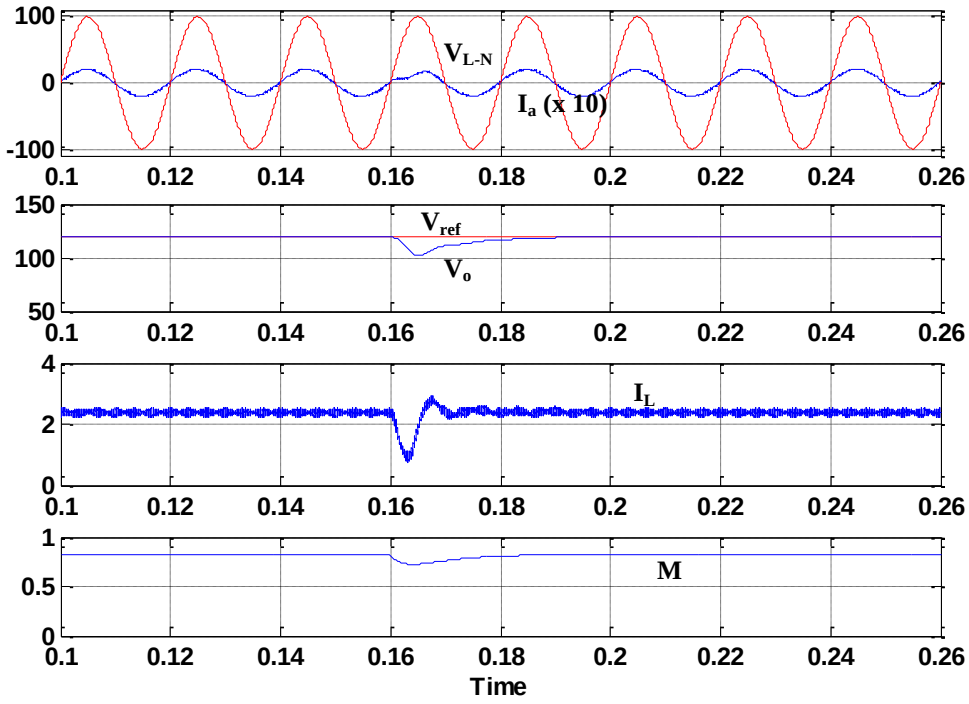


Figure 5.32: The compensated response when disturbance (20V) was given at *t* = 0.16s for R load

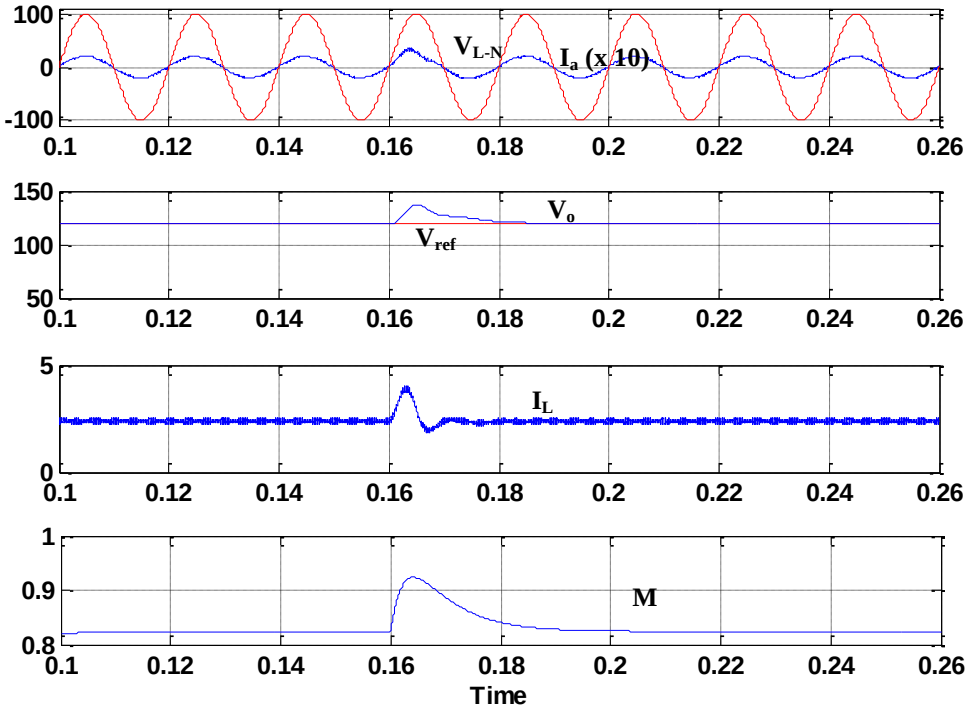


Figure 5.33: The compensated response when disturbance (-20V) was given at t = 0.16s for R load

5.5 Bidirectional Operation

The bidirectional three-phase AC-DC buck-type converter circuit configuration was developed in MATLAB/Simulink as shown in Figure 5.34. The simulation demonstrates the regenerative capability of the proposed power converter. There are two supply voltages: AC supply (100Vp line-to-line) for AC-DC operation, and DC supply (120V) for DC-AC operation. The reference voltage was set to 120V. Figure 5.35 is a block diagram of the PWM control, which consists of a switching design for the two operations (AC-DC and DC-AC). A breaker connects the DC supply to the system during DC-AC converter operation, during which the potential energy of the DC supply is bigger than that of the AC supply, forcing current to flow from the DC side to the AC side. Change in operation mode, from AC-DC to DC-AC and vice-versa, was allowed

only when I_L (on the DC side) was zero (charge is removed from the capacitor); a condition attainable by switching all the switches on.

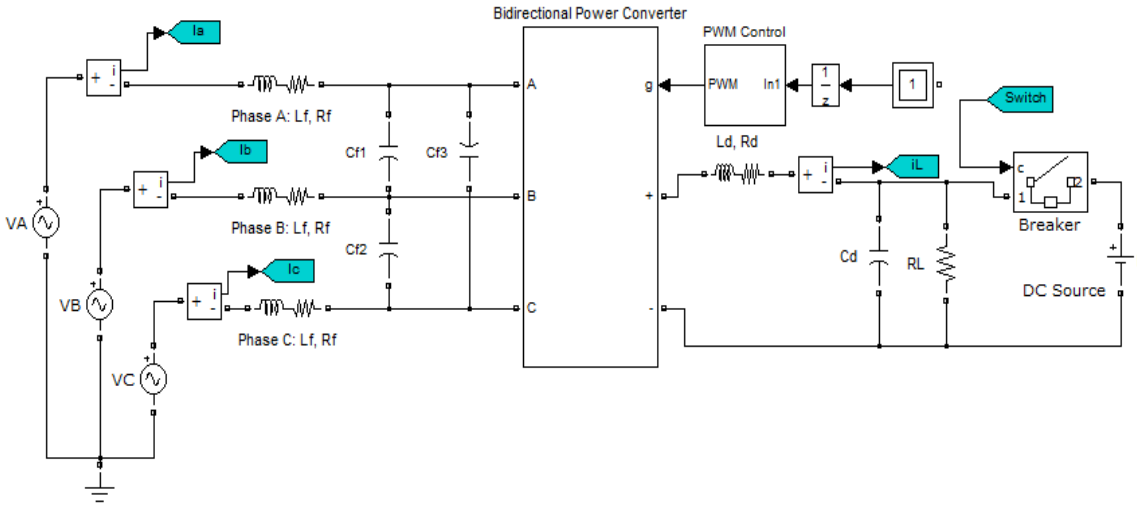


Figure 5.34: The operational bidirectional circuit configuration drawn on MATLAB/Simulink

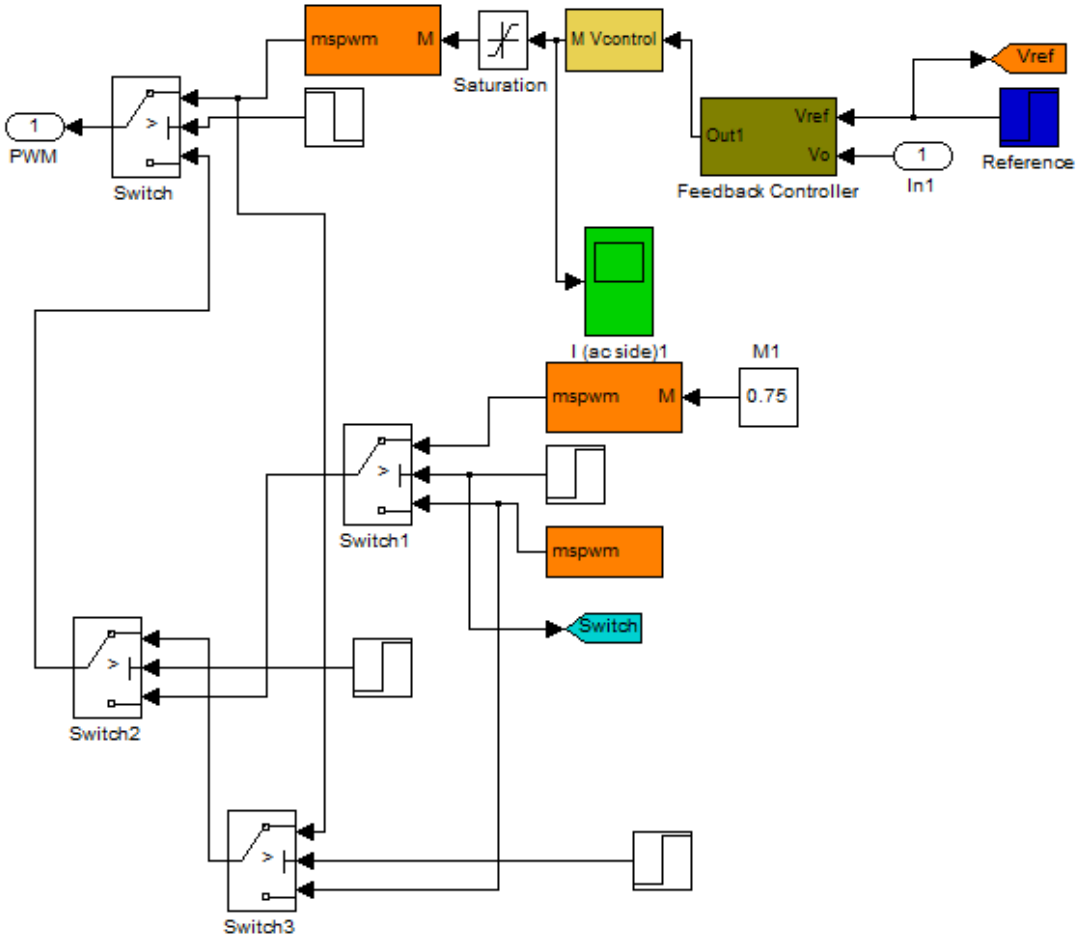


Figure 5.35: The PWM control

Figure 5.36 shows the simulation results of the AC-side current (I_a) and voltage (V_{L-N}) of phase A, and the DC-side output voltage across R_L (V_o) and currents across L_d (I_L) and R_L (I_{RL}). The current from 0 to 0.1s flows from the AC side to the DC side. After that the DC-side inductor freewheeled rapidly until dropping to nearly zero before reversing operational direction (from the DC side to the AC). At 0.2s-0.3s, the system returned to AC-DC operation. Periods between 0-0.1s and 0.2-0.3s, the converter operates as a rectifier where the currents and voltage are in phase. The voltage and current is out of phase between 0.1-0.2s, whereby the converter operates as an inverter. Both operations achieved sinusoidal input current and near-unity power factor at steady

state, and good response at transient state. The output voltage V_o remained the same as the reference voltage (120V). Inductor current I_L results show the power flowing either from the DC side to the AC side or vice-versa.

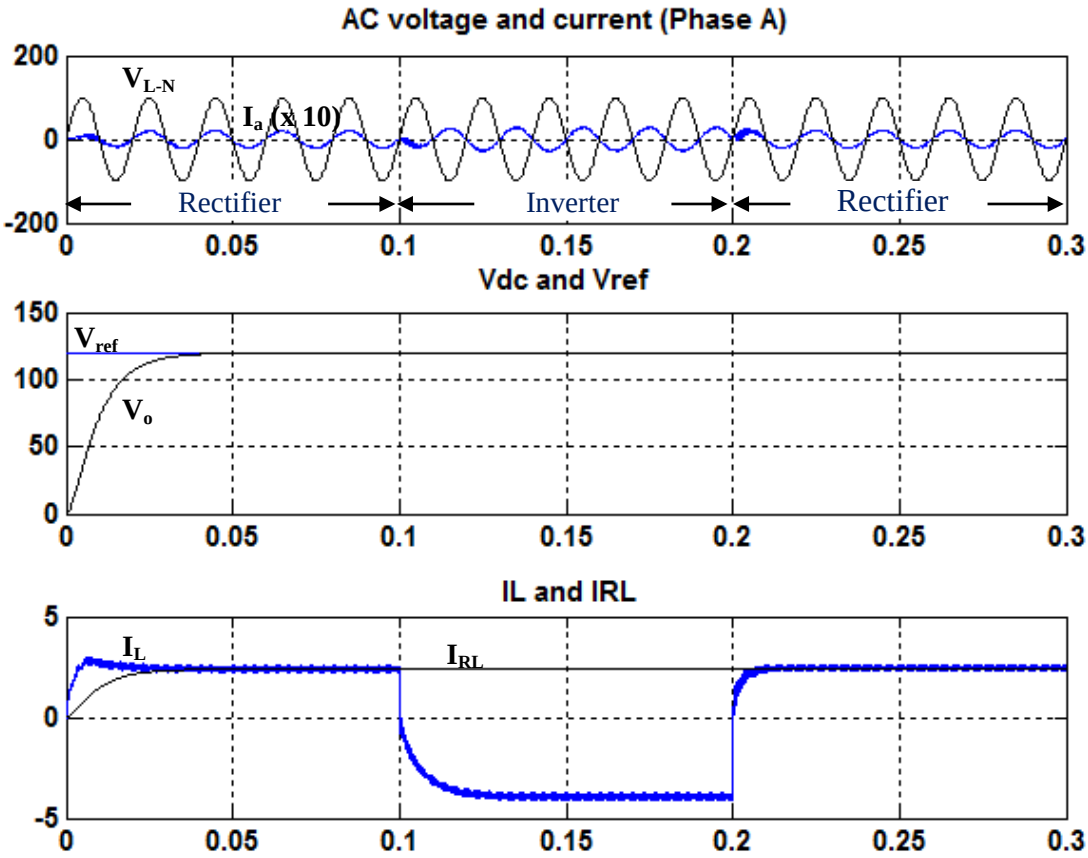


Figure 5.36: The simulation result proving the capability in providing energy back to the voltage sources

5.6 Summary

This chapter discussed the simulation results of the proposed three-phase AC-DC buck-type power converter with bidirectional capability and its proposed PWM modulation strategy. The results show unity power factor and AC sinusoidal input currents with low THD. The closed-loop system was then developed to test the dynamic response to changes in the three-transient cases, reference voltage, disturbance and load. Two types of controllers were investigated: I-D controller and M-curve prediction control technique. Both had good transient responses in their dynamic response test. In term of response performances, I-D controller is better and applicable for the three transient cases, but the M-curve prediction technique voltage simplified the control algorithm. Further investigation need to be conducted to find the modulation index curve prediction for the transient case of load changing. Hence, the simulation also demonstrated the regenerative capability of the proposed power converter.

CHAPTER 6

EXPERIMENT RESULTS

6.1 Introduction

The experiment results discussed in this chapter validate the simulation results of the proposed bidirectional AC-DC buck-type converter, whose switching design and feedback control algorithm had been implemented in a TMS320F28335 DSP. The results of the open-loop system in AC-DC and DC-AC operations were obtained to verify the operation of the proposed three-phase AC-DC buck-type converter and its proposed simplified-plus-modified SPWM. The closed-loop systems were tested to validate the capability and effectiveness of the proposed feedback controls, I-D control, and modulation-index-curve prediction technique, whether they affected good transient response and zero steady-state error during AC-DC operation. Also presented are the experiment's system parameters and the overall hardware development of the three-phase AC-DC buck-type converter.

6.2 Experiment Setup

Figure 6.1 shows the experiment prototype developed for verification. The switching frequency was 19.8kHz. The three-phase AC-DC buck-type converter used six insulated gate bipolar transistors (IGBTs) and twenty-four diodes. A parallel-

connected DC-side diode and IGBT formed the freewheeling path. To prevent circuit attenuation, the input filter resonant frequency was designed to be much lower than the switching frequency (Green et al., 1997). Table 6.1 lists the parameters of the power converter used in the AC-DC and DC-AC experiments.

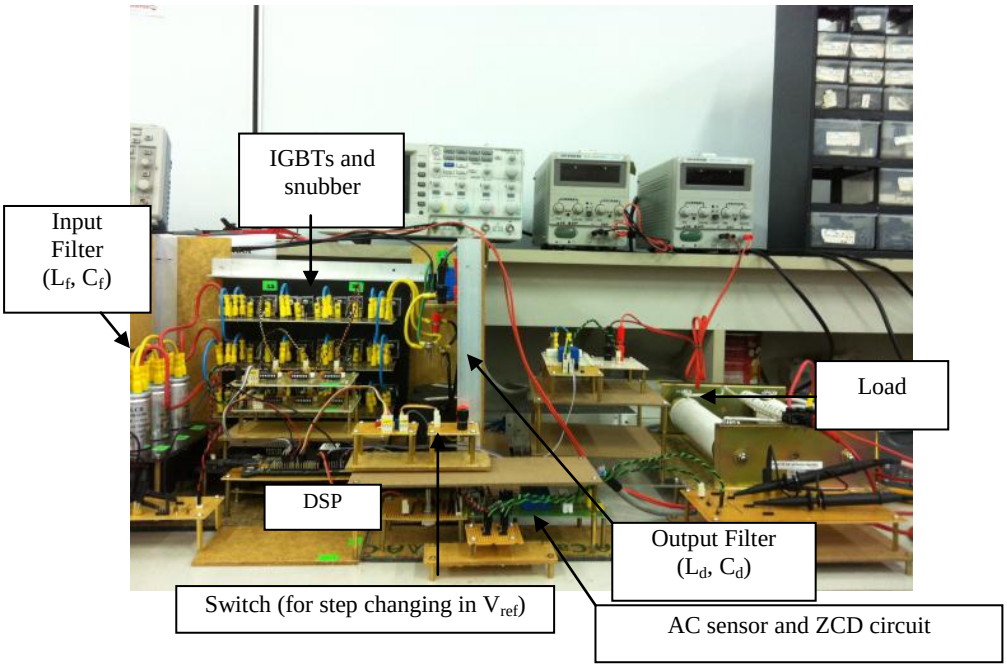


Figure 6.1: The prototype hardware

Table 6.1: The power-converter experiment parameters

Parameters	AC-DC	DC-AC
Switching frequency, f_s	19.8 kHz	19.8 kHz
Input Filter, L_f, C_f	1mH, 1μF	1mH, 1μF
Output Filter, L_d, C_d	6mH, 220μF	6mH, 220μF
Main Voltage frequency, f	50 Hz	NA

The hardware of the proposed three-phase AC-DC buck-type converter includes DSP, driver circuits, zero-crossing detector (ZCD) circuit, step-change switch circuit, AC/DC voltage sensor, and load. Figure 6.2 is a block diagram of the three-phase

simplified-plus-modified SPWM generator and its DSP-implemented control algorithm. The PWM and feedback control algorithms were written in C language, compiled in Code Composer Studio, and then downloaded onto the DSP board. A fully digitally-controlled generation of PWM gating signals complicates the hardware. Details of generating the simplified-plus-modified SPWM for each IGBT have been discussed in Chapter 3. The gating PWM signals were fired to the IGBTs via the driver circuits (Figure 6.3), which were constructed to deliver the PWM signals upon the appropriate voltage values between the DSP pins and the IGBTs (usually 3V-15V).

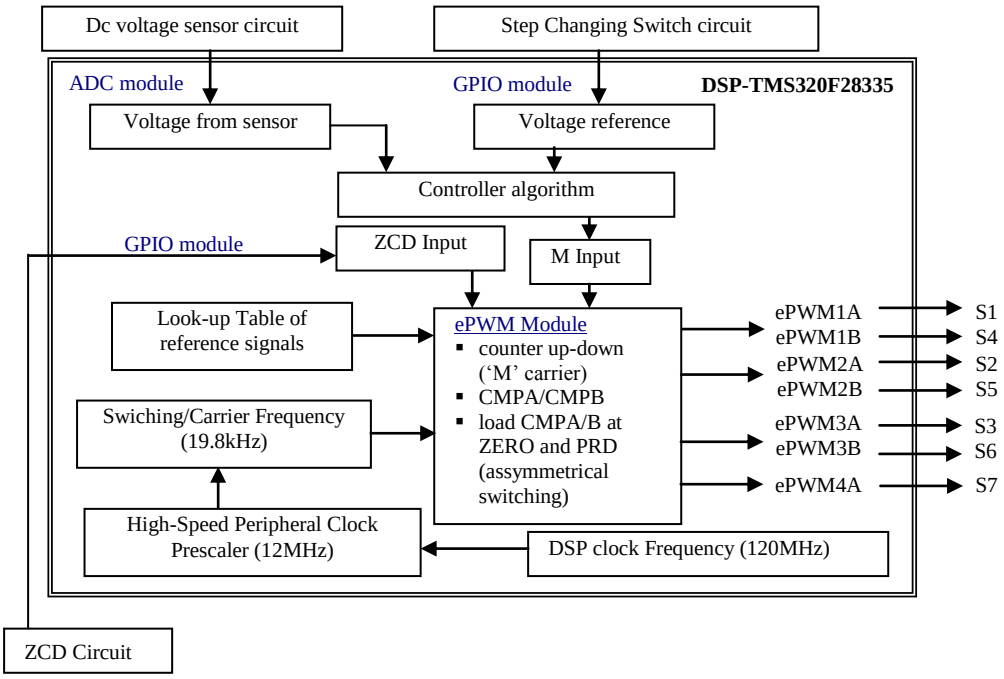


Figure 6.2: The DSP implementation of the simplified-plus-modified SPWM with feedback controller

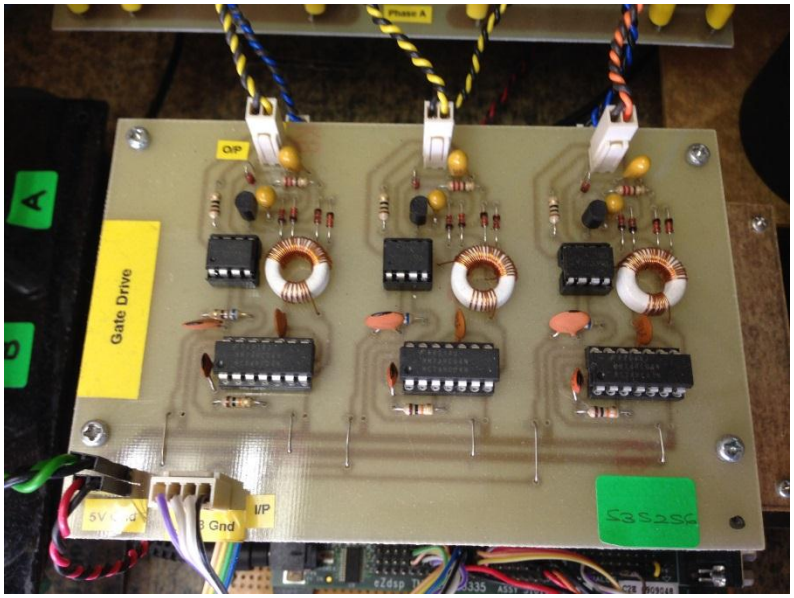


Figure 6.3: The driver circuits

For PWM synchronization with the 50Hz AC-voltage line, the AC voltage sensor was connected to the ZCD. The ZCD output was connected to the DSP's digital input in the GPIO module. Figure 6.4 shows the ZCD circuit and AC sensor. The ZCD's sinusoidal AC input and squarewave output are as shown in Figure 6.5. The positive and negative cycles of the sinusoidal AC (the ZCD input) respectively produced states 1 and 0 (the ZCD output). The algorithm of the *k* value resets to zero if the GPIO (used as input from the ZCD) indicated conditions changing from 0 to 1. The PWM phase shifting can be digitally-controlled to be either in phase, lagging, or leading. A simple four bits switches (DIP switch) circuit is used to change sixteen value of modulation index for open-loop testing purpose. The ADC module of the TMS320F28335 DSP converts the signal from the DC voltage sensor (the feedback voltage signal) for the control algorithm. Only one DC voltage sensor (not two sensors or more as in current-voltage feedback technique) is used as input to the control algorithm, making for shorter analog-to-digital (A/D) conversion time.

Figure 6.6 is a flowchart of the DSP implementation of the simplified-plus-modified SPWM with feedback controller for the three-phase AC-DC buck-type converter. The DSP initializes the values of *k*, reference voltage V_{ref}, and modulation index M. It then starts functioning by checking the condition of the interrupt in both the ZRO and the PRD. If one of them is activated, it checks the input from the ZCD circuit (the GPIO module) for synchronization with the AC voltage line. Upon a step-change in the reference voltage, the DSP reads the value of the reference voltage data (on the GPIO module) from the step-change switch circuit before sending it to the control algorithm. The data from the DC feedback sensor (the ADC module) of the ePWM module is processed by the control algorithm, which produces a control variable of the modulation index M to multiply with the appropriate data in the look-up table. This data is sent to the ePWM module to generate the PWM. The ePWM output pin is connected to a gate driver circuit before the amplified PWM signal is fired to the IGBT. The process repeats until a cycle of 50Hz mains frequency (792 samples) completes. The whole process is not executed for as long as the DSP operates.

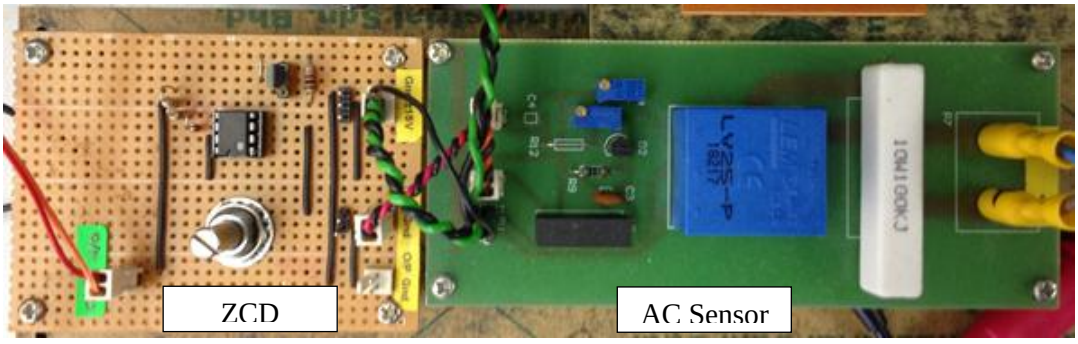


Figure 6.4: The ZCD circuit and the AC sensor

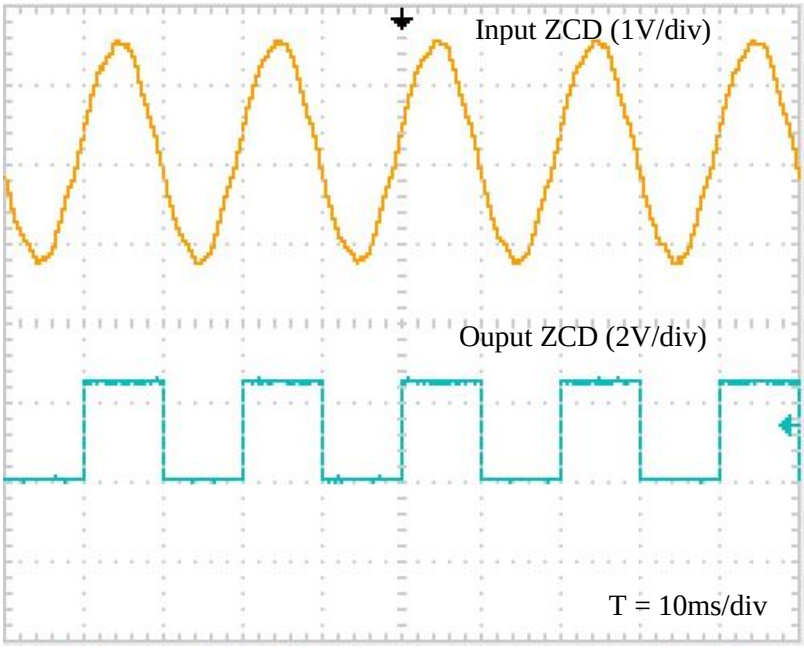


Figure 6.5: The sinusoidal AC input and the ZCD square wave output

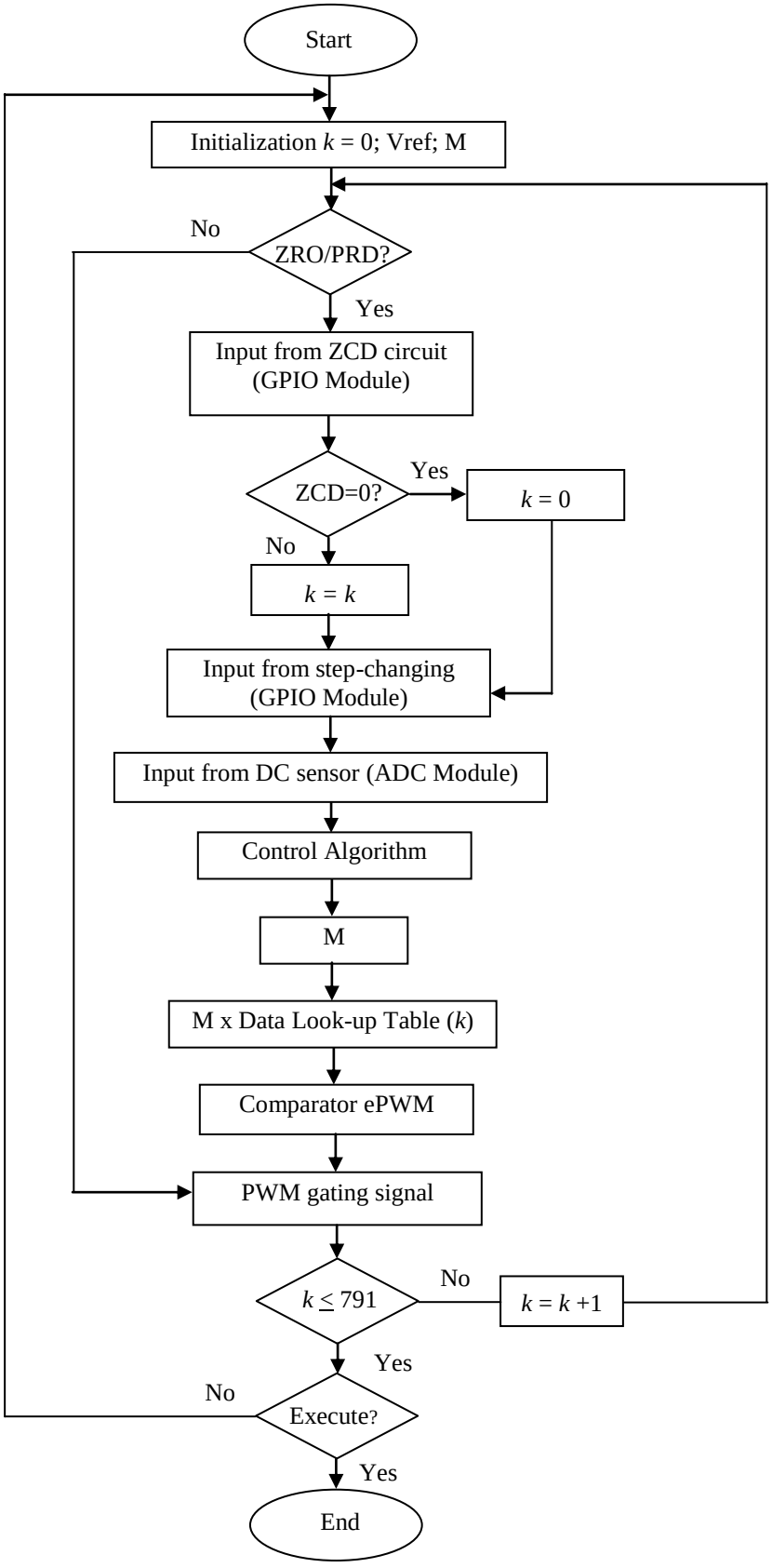


Figure 6.6: The DSP-implemented simplified-plus-modified SPWM with feedback controller

6.3 Results of the Open Loop System

The experiment on the open-loop system resistive (R) load was run in both AC-DC and DC-AC operations to verify the proposed circuit configuration and switching design. The AC-side and DC-side currents and voltages were observed, and the total harmonic distortion values recorded.

6.3.1 AC-DC Operation

A 50Ω resistive load was tested on the prototype developed of the bidirectional three-phase power converter. Figures 6.7, 6.8, and 6.9 respectively shows the AC-source voltages and currents at near-unity power factor in phases A, B, and C, proving the proposed technique to have performed well in the proposed three-phase bidirectional system during AC-DC operation. The source voltage and currents were in phase. Figure 6.10 presents the experiment results of the phase-A source voltage V_s = 128 Vrms (line-to-line voltage), the phases A, B and C source currents, and modulation index M = 0.8. The total harmonic distortions (THDs) of the phase-A input current and voltage supply were respectively 3.5% and 3.3%. The power factor was 0.98.

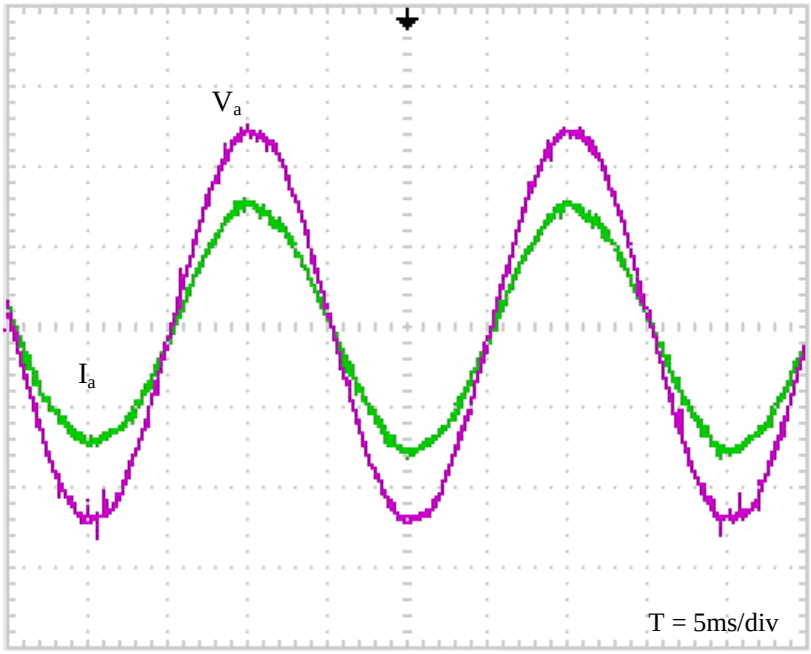


Figure 6.7: The phase-A source voltage V_a (25V/div), and source current I_a (1A/div)

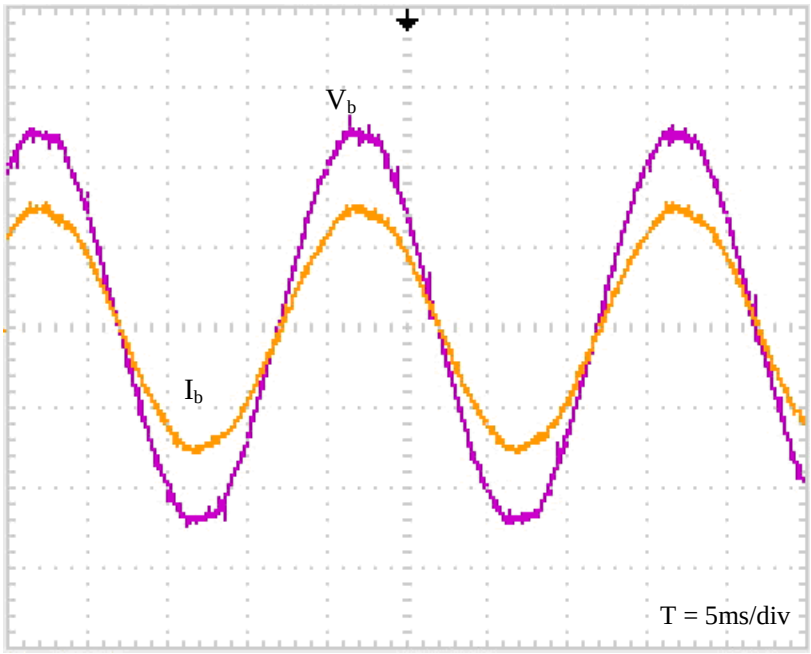


Figure 6.8: The phase-B source voltage V_b (25 V/div), and source current I_b (1A/div)

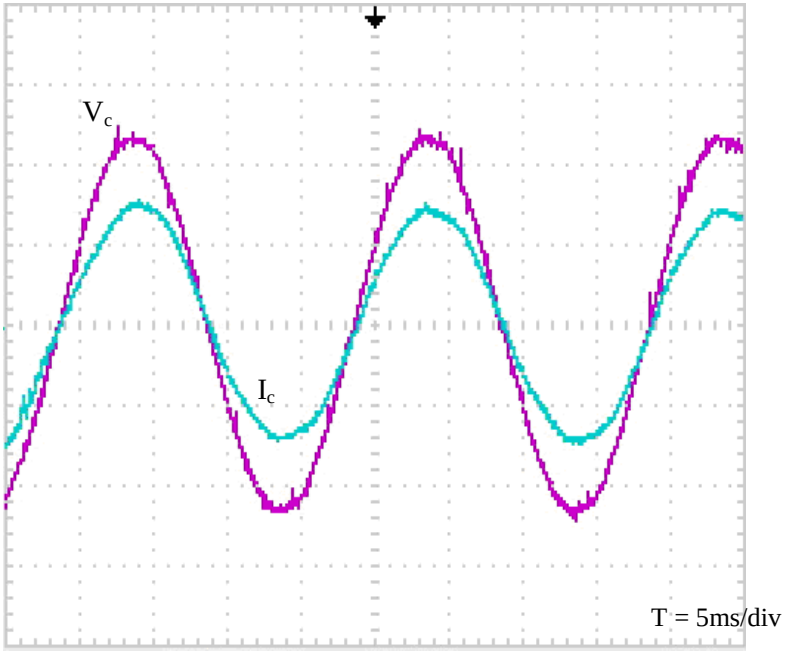


Figure 6.9: The phase-C source voltage V_c (25V/div), and source current I_c (1A/div)

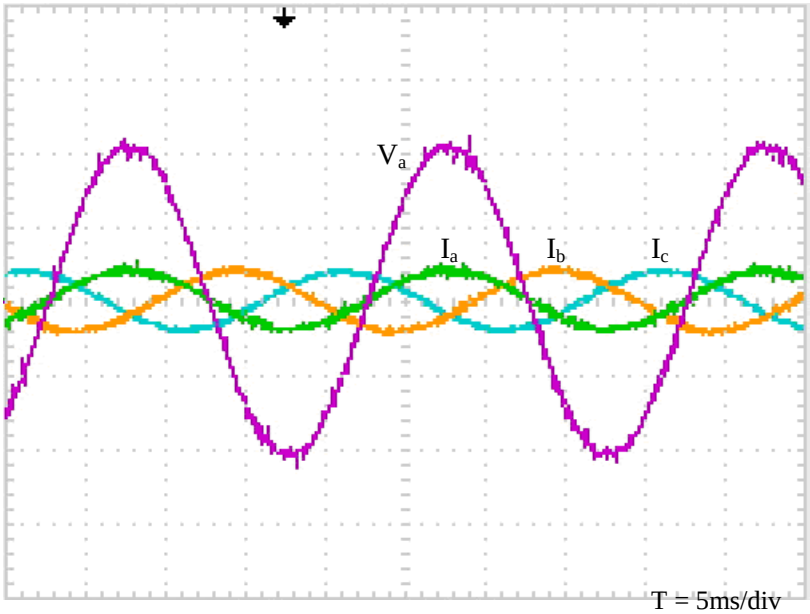


Figure 6.10: The phase-A source voltage V_a (50V/div), and phases A, B, C source currents (I_a, I_b and I_c) (5A/div)

Figure 6.11 shows the AC source voltage (V_a) and bridge voltage (V_B) (the output voltage pre-LC-filtering on the DC side). The results were obtained with $100V_p$ (line-to-neutral voltage) input AC voltage and 0.8 modulation index (M).

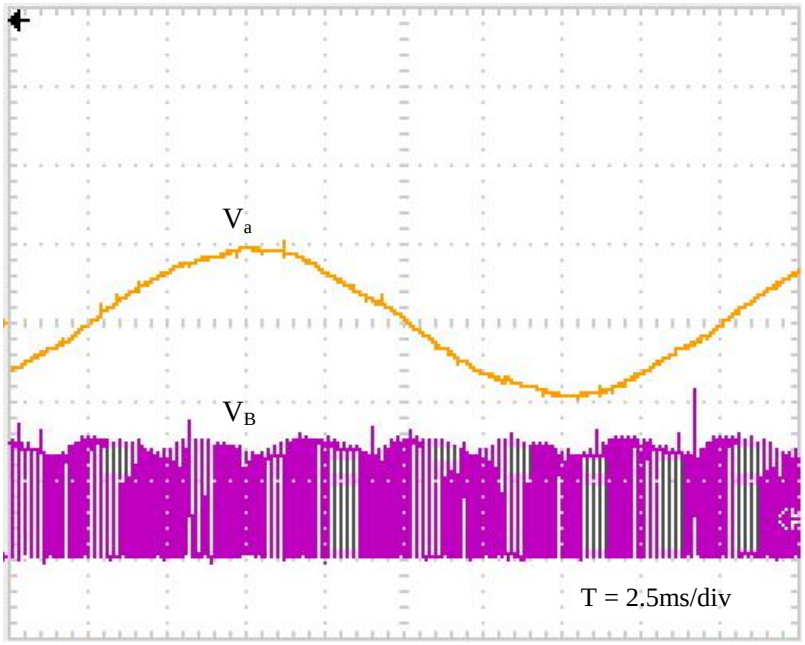


Figure 6.11: The source voltage V_a (100V/div) and pre-filtered DC voltage V_B (100V/div)

Figure 6.12 shows the DC voltage V_{dc} varying with M in both the simulation and the experiment. The graph shows the DC-voltage output increasing linearly with M. The parameters used in the simulation were ideal values, thus the simulation results differed from those of the experiment. Also, in the experiment, the DC voltage dropped (unlike in the simulation), owing to switching losses and non-ideal converter elements. Losses increased as M increased because the bigger current (from the M increase) created bigger losses in the non-ideal elements.

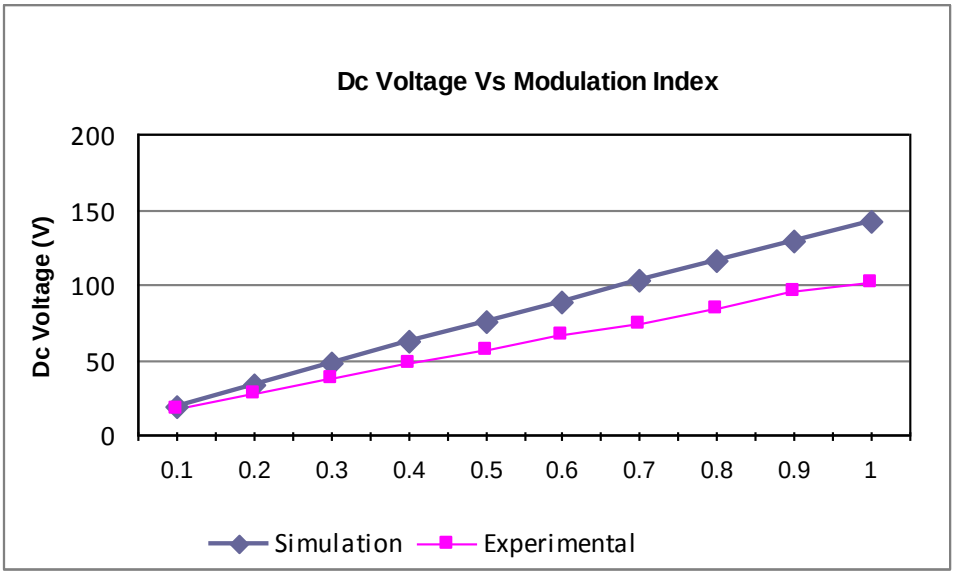


Figure 6.12: The DC voltage V_{dc} against the modulation index M

6.3.2 DC-AC Operation

The AC-side phase-A output current and voltage were observed during the DC-AC operation. Figure 6.13 presents the phase-A AC currents and voltages. Tests were obtained for each phase, with the DC voltage input V_{DC} = 70V, the modulation index M = 0.9, and the load resistance R = 40Ω. The proposed circuit configuration and its PWM switching produced sinusoidal input currents with out-of-phase voltages (indicating that the currents flowed from the DC side to the AC side). The total harmonic distortions (THDs) of the AC voltage and currents were respectively 3.7% and 4.2%. The power factor was 0.98. The output current's peak output voltage and current respectively equalled 50V and 1.25A.

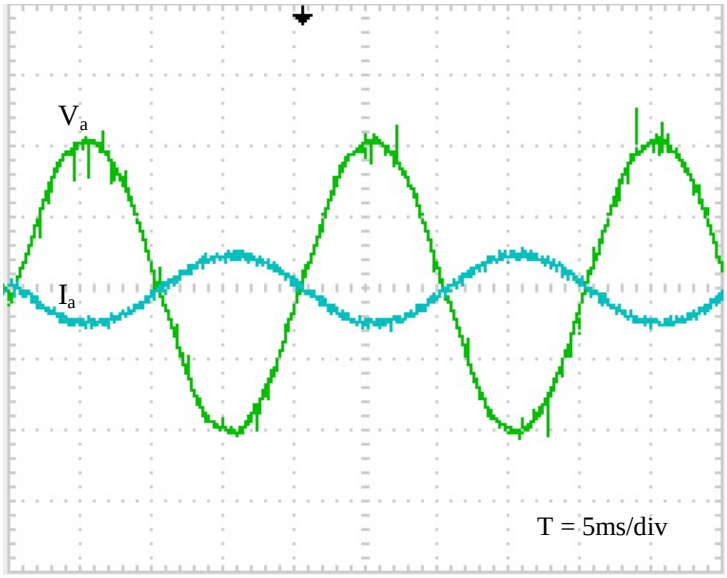


Figure 6.13: The phase-A source voltage V_S (25V/div) and source current I_a (2.5A/div) during DC-AC operation

6.4 Results of the Closed-Loop System: the Proposed I-D Controller and Modulation-Index-Curve Prediction Technique

The closed-loop-system experiment was run for the resistive (R) load in AC-DC operation. Two techniques or algorithms have been proposed to validate it: I-D controller, which was then extended to M-curve-prediction technique. The AC-side and DC-side currents and voltages were observed for the stepped-up and stepped-down reference input and stepped-up resistive load. Figure 6.14 shows the setup for the step-change experiments. For the voltage reference step-changing test, a dual-in-line-package (DIP) switch was used to change the reference voltage value; it was connected to one of the GPIO pins of the DSP. For the step-disturbed load, two resistors (100Ω each) were connected in parallel; a breaker was used to change the resistor value from 100Ω to 50Ω.

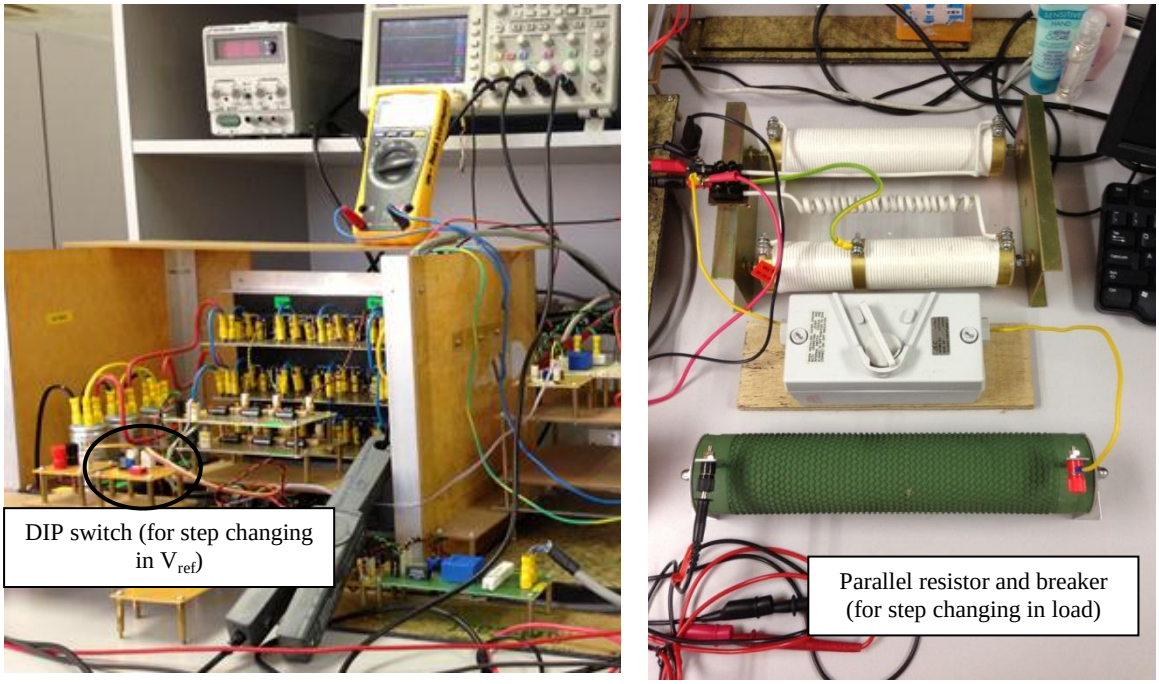


Figure 6.14: The experiment setup for the step-change tests

6.4.1 Results of the Uncompensated System

As discussed in Chapter 5, the simplified-plus-modified SPWM design achieves near-unity power factor and provides steady-state system stability but not the desired transient response. Transient tests were then done for step-disturbed load (Case I) and step-changed voltage reference (Case II) to validate the simulation results.

Figure 6.15 shows the result of step-changing the load from 100Ω to 50Ω to the phase-A voltage-source V_a and current-source I_a, DC voltage output V_o, and inductor DC current I_L. When the load changed from 100Ω to 50Ω, the output voltage significantly dropped through switching losses and non-ideal converter elements. The system without feedback controller was unable to maintain the output voltage at reference voltage (non-zero steady-state error, e_{ss}). Compared with simulation results of Figure 5.17, the trends of drop in V_o, increase in I_L are in the correct direction.

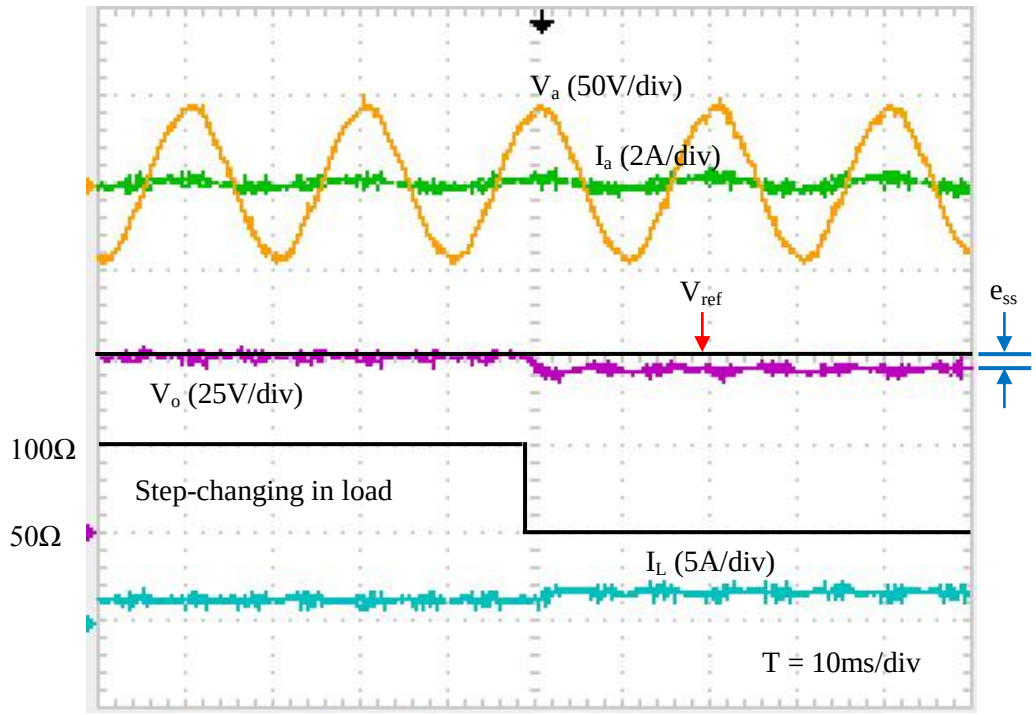


Figure 6.15: Uncompensated step response; load resistance changed from 100Ω to 50Ω

In the Case II test, V_{ref} was changed from 20V to 55V. Figure 6.16 shows the system without feedback controller producing about 25% overshoot in the DC output voltage and very high overshoot (more than 100%) in the output current, causing current stress on the semiconductors. The steady-state voltage measured 45V, with a 10V offset owing to the non-ideal converter elements. Improvement by voltage feedback control shall now be addressed. Compared with simulation results of Figure 5.15, the trends of rise in V_o, increase in I_L and the magnitude of I_a are in the correct direction.

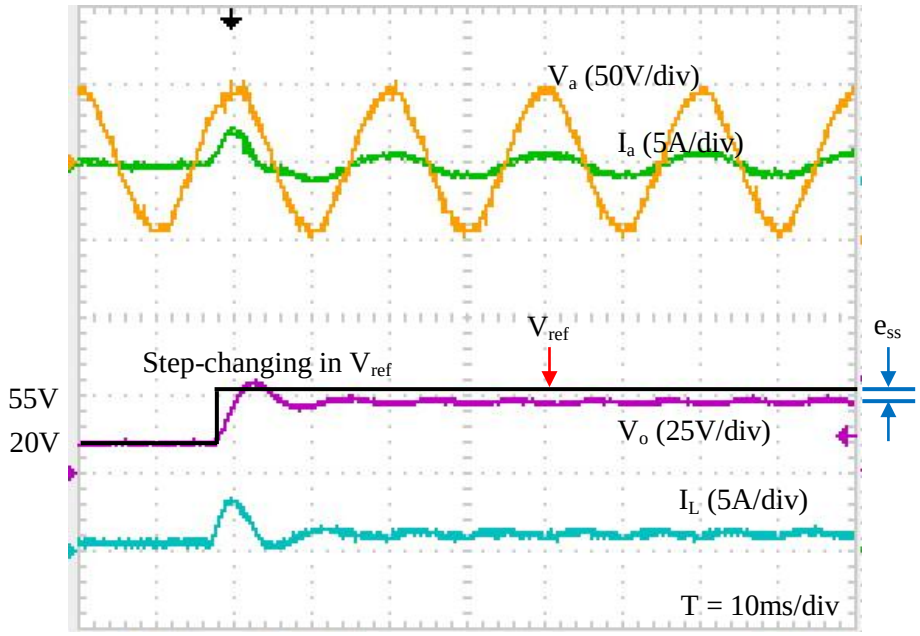


Figure 6.16: Uncompensated step response; V_{ref} changed in the load resistance

6.4.2 Results of I-D Controller

As described in Chapter 5, the objectives of the feedback controller include obtaining zero steady-state error in the output voltage (V_o=V_{ref}) and compensating for the huge voltage/current in the system (to improve transient response). The I-D controller algorithm detailed in Chapter 4 was developed and written in C language in the DSP's main program. Tests on the control algorithm were done with two transient conditions; the load was step-changed from 100Ω to 50Ω (Case I), and the reference voltage was step-changed from 20V to 50V (Case II).

In Case I, the test used feedback integral gain K_I=100, T_D=0.0003, and K_D=0.002. Figure 6.17 shows the transient results for the voltage source (V_a), current source (I_a), DC voltage (V_o), and inductor current (I_L). The controller was able to track the reference voltage V_{ref} with zero steady-state error and with good dynamic response for load

changing from 100Ω to 50Ω. Inductor current I_L was increased two times from 0.4A to 0.8A. Compared with simulation results of Figure 5.23, the experimental results of V_o, I_L and I_a follow the trends of changing the load.

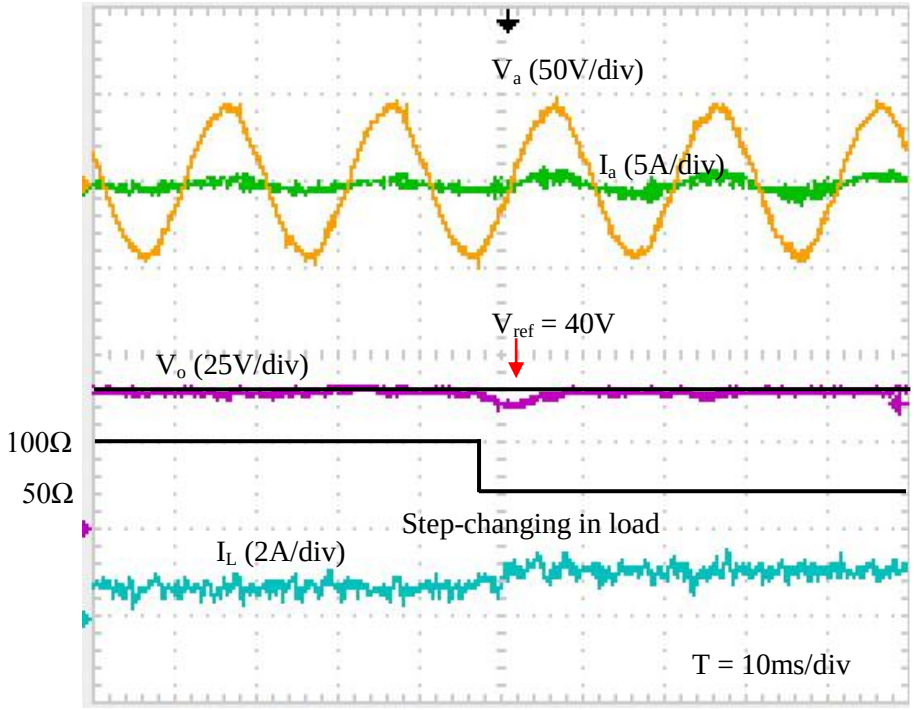


Figure 6.17: Compensated step response with I-D controller; load resistance changed

For Case II, the results of the system with the proposed I-D controller shown in Figures 6.18 to 6.21 verify that the proposed controller can eliminate steady-state error from the output voltage. The test used controller gain T_D=0.0003 and K_D=0.002 and varying K_I (50, 100, 200 and 300). Resistor load was 40Ω. The results confirm that the transient response can be controlled by tuning only the integral gain K_I. The response is faster and the percentage overshoot (especially in I_L) is larger when the controller gain K_I is increased. Compared with simulation results of Figure 5.24(a), the experimental results of V_o, I_L and I_a follow the trends of changing the gain K_I.

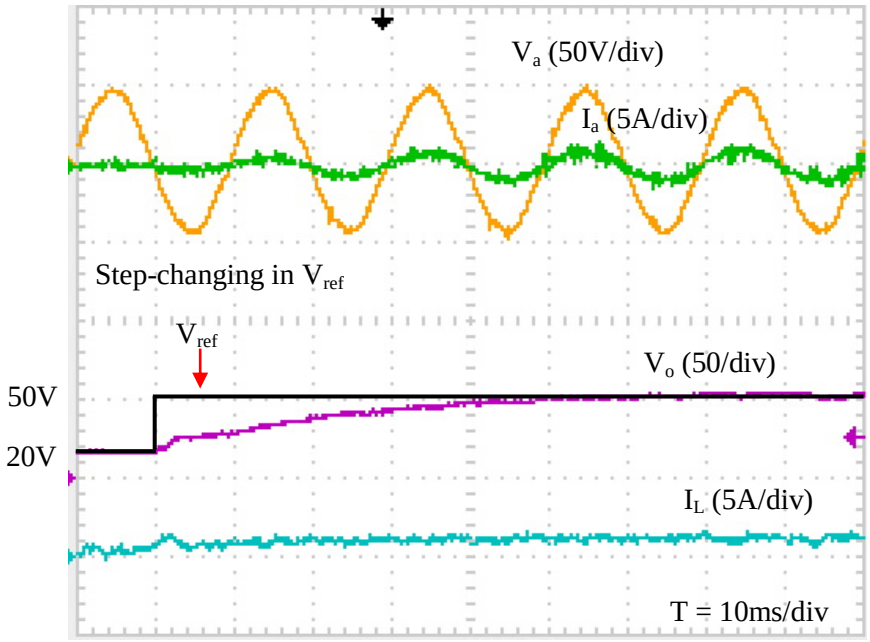


Figure 6.18: V_{ref} step-change (20V-50V) in system with proposed controller; K_I=50

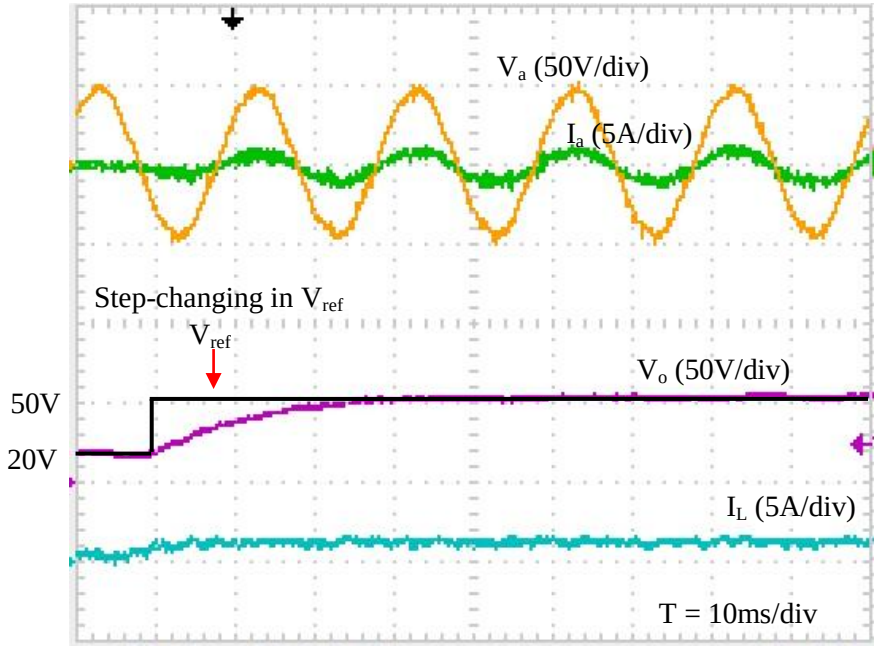


Figure 6.19: V_{ref} step-change (20V-50V) in system with proposed controller; K_I=100

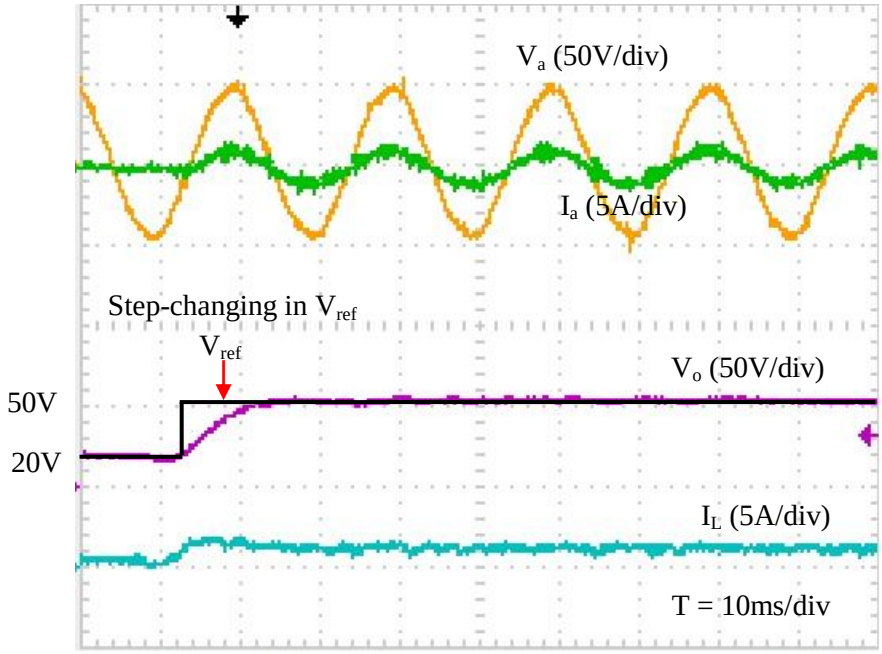


Figure 6.20: V_{ref} step-change (20V-50V) in system with proposed controller; K_I=200

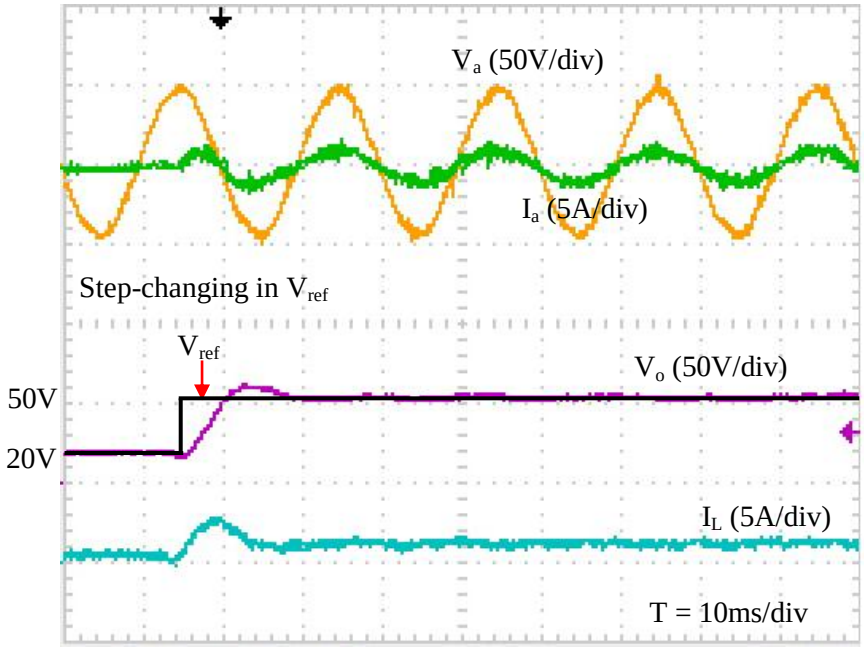


Figure 6.21: V_{ref} step-change (20V-50V) in system with proposed controller; K_I=300

Figure 6.22(a) to (d) show 'zoom in' plot of I_L responses to see the differences with varying of K_I. Inductor current I_L was increased from 0.5A to 1.25A. Table 6.2 summarizes the comparison DC output responses (V_o and I_L) between system using different of K_I. Using these experimental parameters, it concludes that the optimum value of K_I was 100 where its settling time was below 40ms and the percentage overshoot was zero for both voltage and current responses.

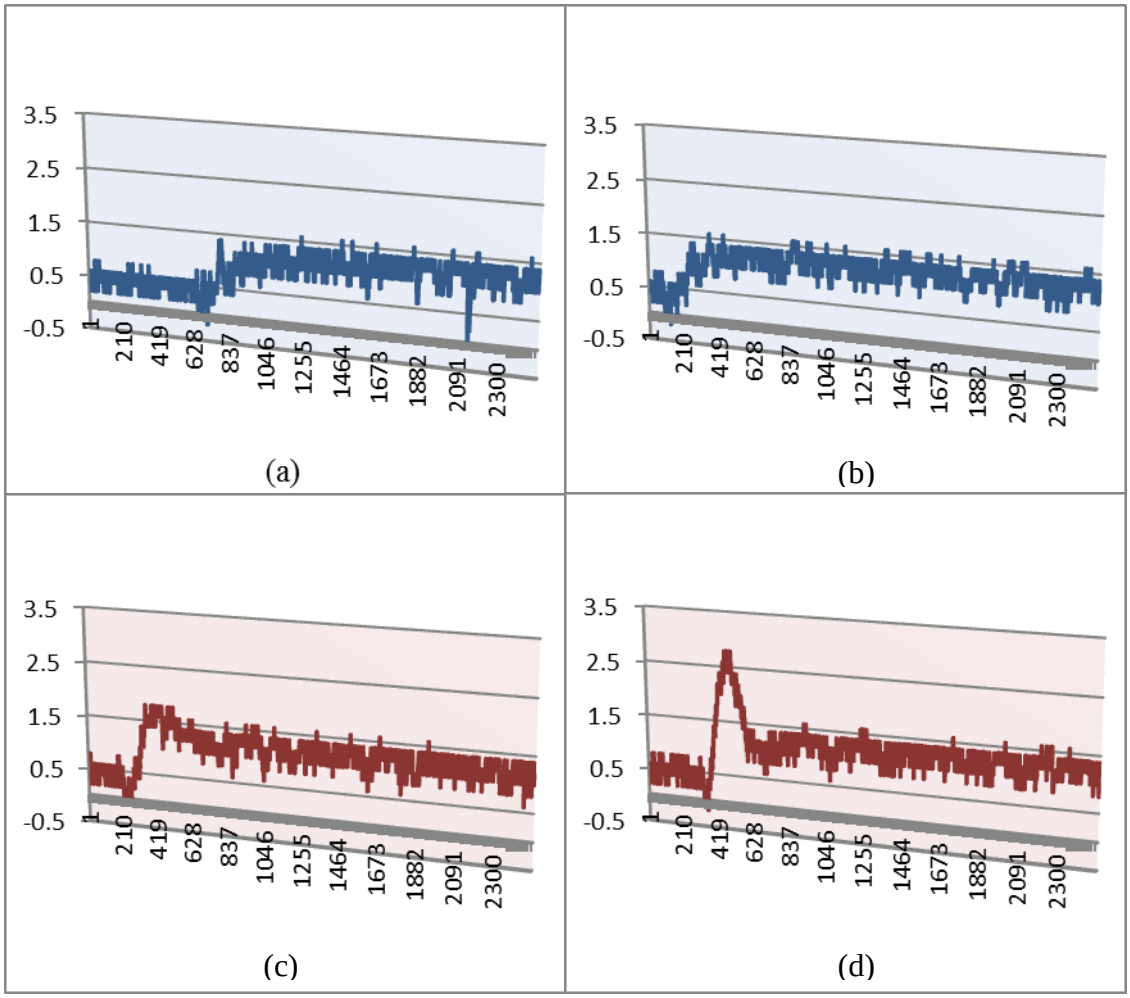


Figure 6.22: Zoom in of I_L responses for (a) K_I=50, (b) K_I=100 (c) K_I=200, and (d) K_I=300

Table 6.2: The system performance; the DC output voltage V_o and DC inductor current I_L against values of the gain controller K_I

K_I	V_o	I_L
50	• Steady-state error = zero • Settling time = 50ms • Overshoot percentage = zero	• Settling time = 20ms • Overshoot percentage = zero
100	• Steady-state error = zero • Settling time = 30ms • Overshoot percentage = 45%	• Settling time = 10ms • Overshoot percentage = zero
200	• Steady-state error = zero • Settling time = 10ms • Overshoot percentage = zero	• Settling time = 15ms • Overshoot percentage = 10%
300	• Steady-state error = zero • Settling time = 15ms • Overshoot percentage = 12%	• Settling time = 15ms • Overshoot percentage = 40%

Figure 6.23 presents the step responses to the small step-changed values of V_{ref} (10V difference). The gain K_I was 100. The I-D controller was able to eliminate the steady-state error from the output voltage and obtained good transient response for small step-changed values of V_{ref} .

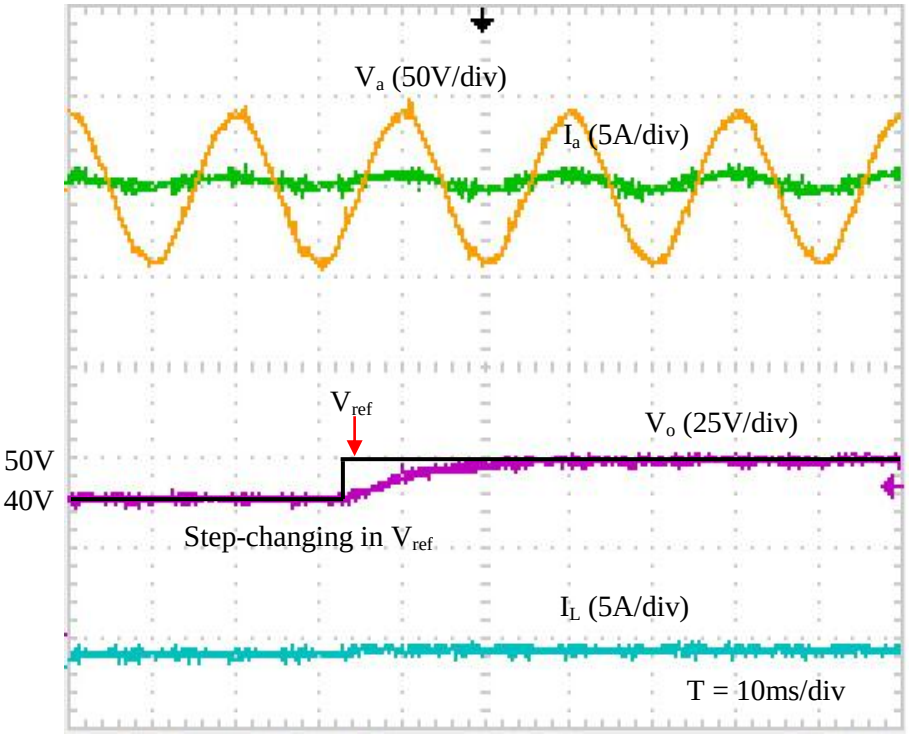


Figure 6.23: V_{ref} step-change of 40V to 50V

6.4.3 Results of the M-Curve-Prediction Control Technique

The test was performed to verify the M-curve-prediction control technique algorithm obtained in Chapter 4. The transient conditions were stepped-down and stepped-up reference. The control algorithm used the controller gains, T_D = 0.0003 and K_D = 0.002 and K_I = 100. The three-phase voltage source was 80V_p and the load resistor was 100Ω. Figure 6.24 shows the results for the phase-A voltage and current (V_a, I_a), output voltage (V_o), and inductor current (I_L) in the step-down case, with V_{ref} stepped-down from 75V to 40V.

The M-curve-prediction control technique was able to track the reference with good transient response and small steady-state error (e_{ss} = 4%). No overshoot occurred in V_o and I_L, and the settling time was 15ms. I_L was stepped-down from 0.74A to 0.39A.

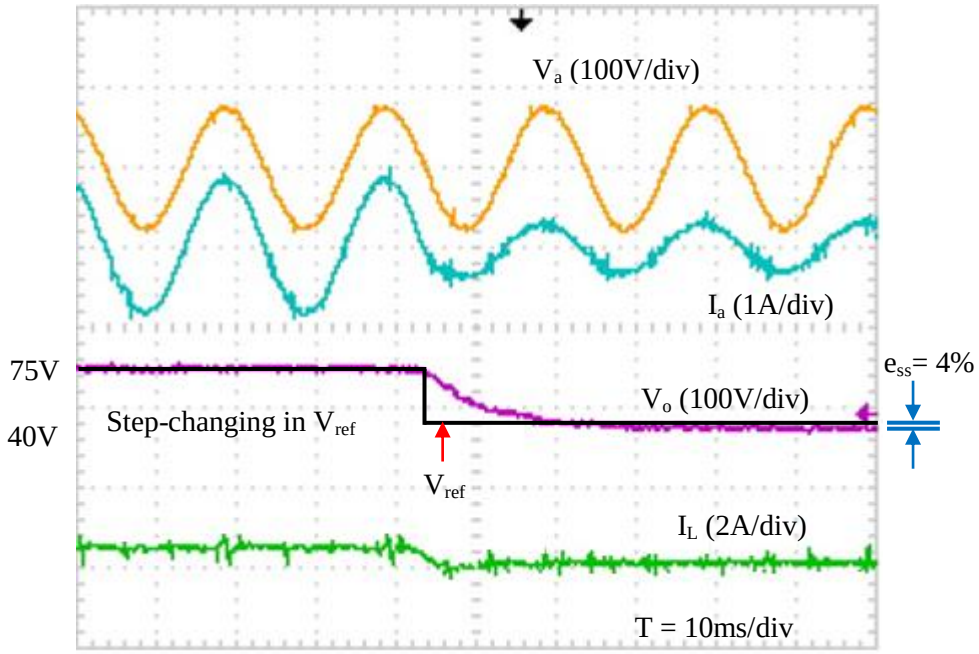


Figure 6.24: The compensated step-down response when V_{ref} was changed

In the step-up case, the tests were done with a three-phase AC voltage source input of between $50V_p$ and $100V_p$. The load was 50Ω. Figures 6.25-6.30 show the transient results of the voltage source (V_a), current source (I_a), DC voltage (V_o), and inductor current (I_L). All the cases show 25ms and 10ms settling time, respectively, of V_o and I_L. The overshoot in V_o was zero in almost all the cases. The difference between the peak and the steady-state current of I_L did not exceed 0.2A. The small steady-state error (below 5% in each case) was due to the prediction algorithm being determined with the assumption of no losses to the system. It can be corrected by adding a suitable gain to the algorithm. Table 6.3 summarizes the initial and after stepped-demand of the DC output (V_o and I_L) and the transient response of V_o on the different three-phase AC voltage sources. The experiments results show steady-state error around 4%, the settling time is 25ms and there is no overshoot for all cases. Compared with Figure 5.28, the trends of V_o, I_L and I_a in simulations and experiments agree.

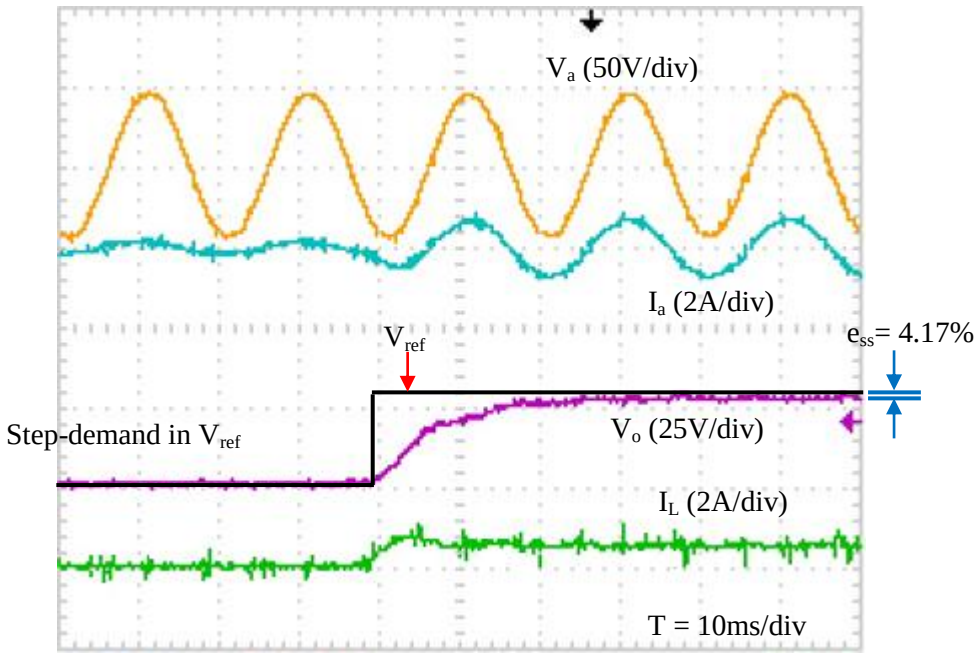


Figure 6.25: Compensated step-up response when V_{ref} was changed; AC source $50V_p$

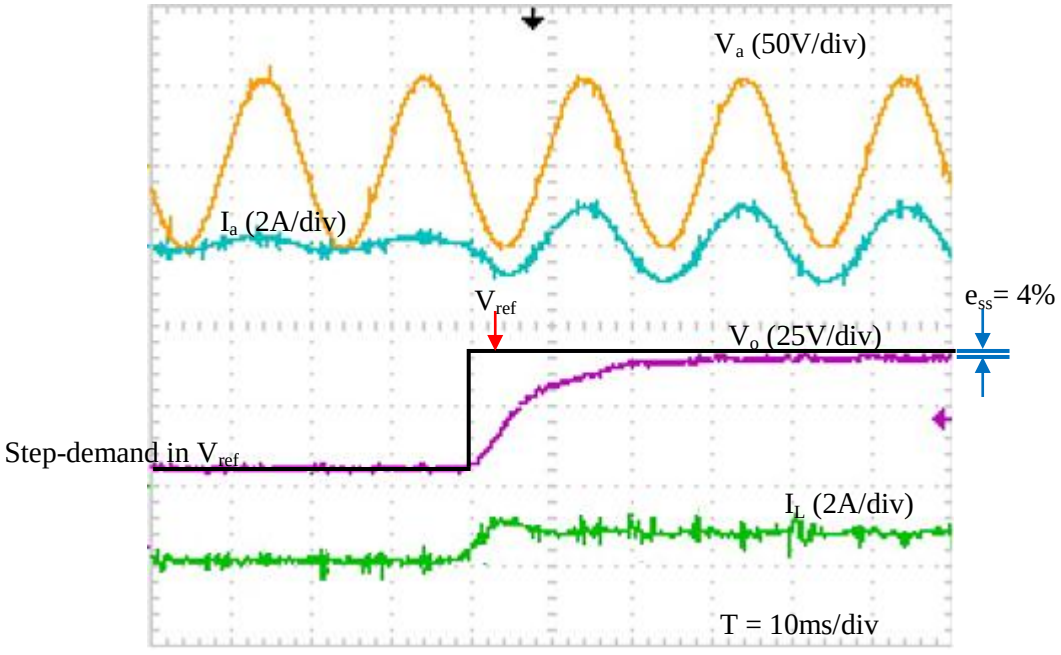


Figure 6.26: Compensated step-up response when V_{ref} was changed; AC source $60V_p$

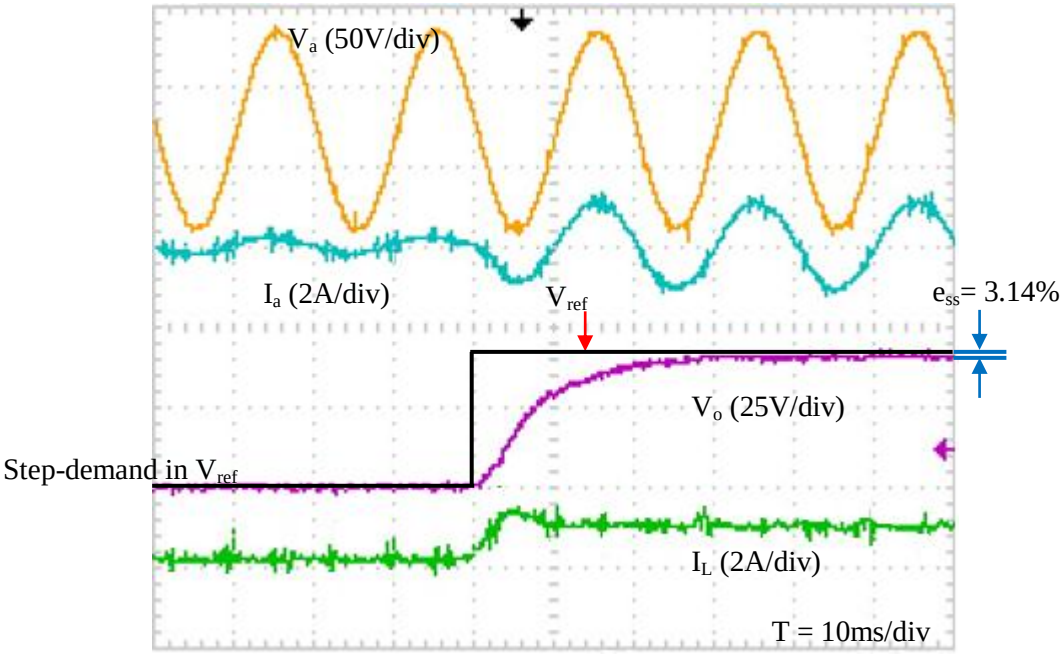


Figure 6.27: Compensated step-up response when V_{ref} was changed; AC source 70V_p

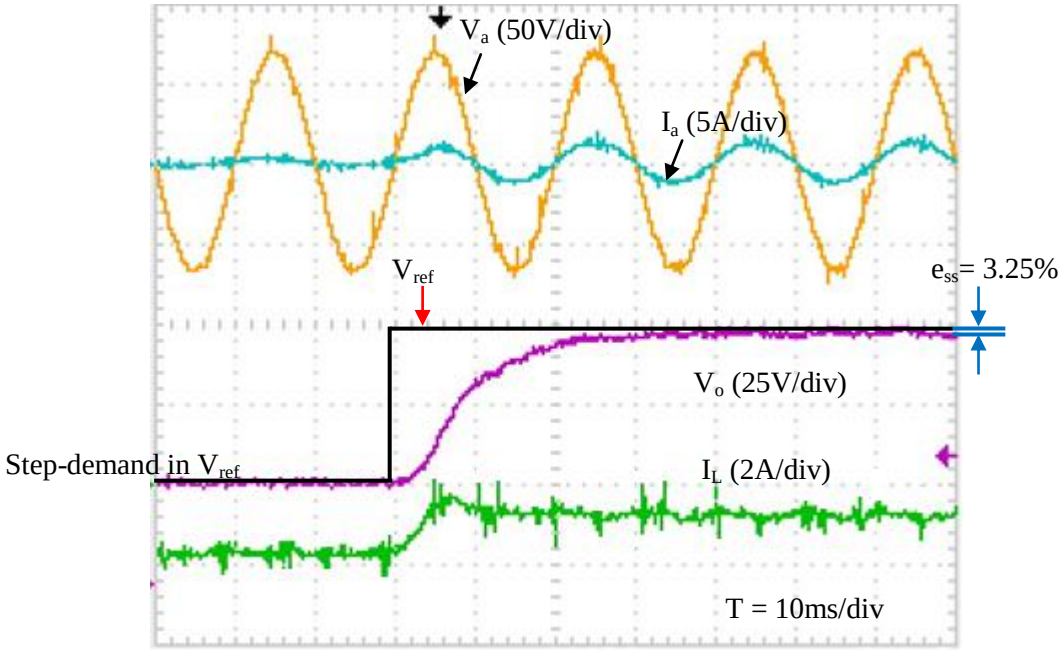


Figure 6.28: Compensated step-up response when V_{ref} was changed; AC source 80V_p

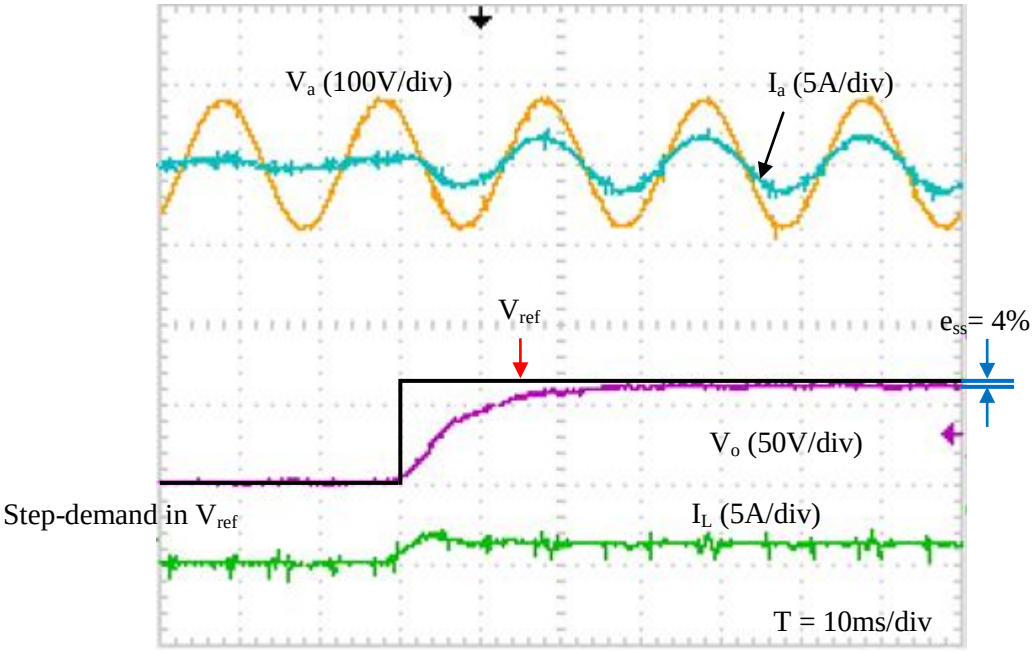


Figure 6.29: Compensated step-up response when V_{ref} was changed; AC source $90V_p$

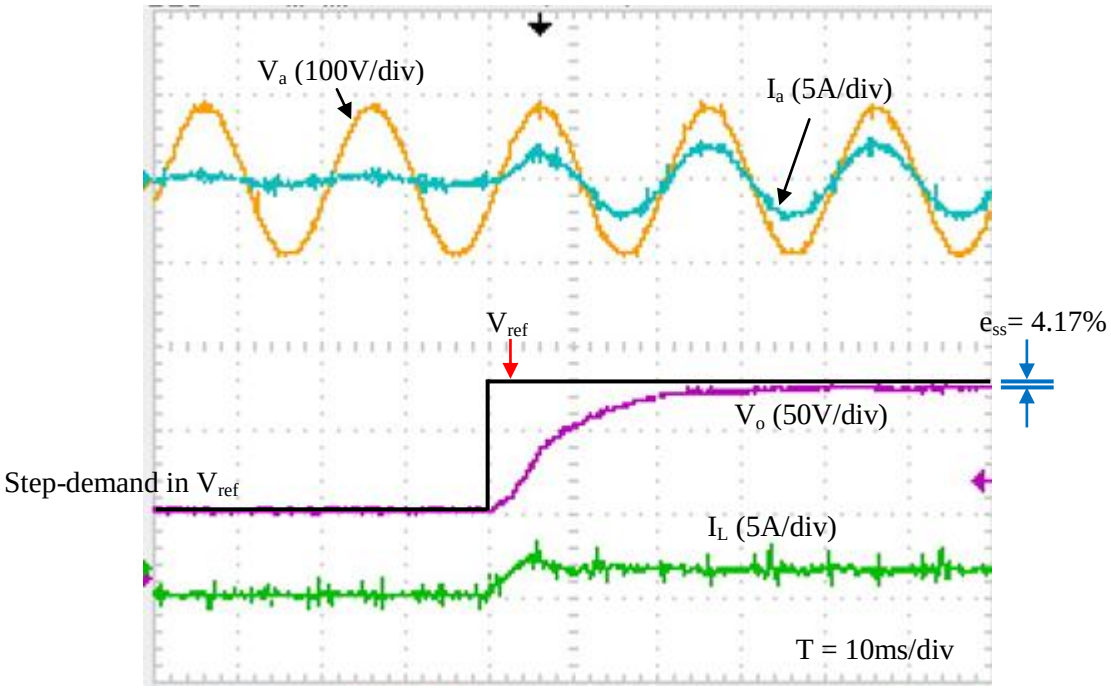


Figure 6.30: Compensated step-up response when V_{ref} was changed; AC source $100V_p$

Table 6.3: The initial and after stepped-demand of the DC output (V_o and I_L); and the %OS, T_s and e_{ss} of V_o against three-phase AC voltage sources

Three-phase AC sources (V_p)	**50**	**60**	**70**	**80**	**90**	**100**
V_{ref} (V)	48	60	70	80	100	120
$V_{o(initial)}$ (V)	19.5	23.5	27.5	30.5	36	40
$V_{o(measured)}$ (V)	46	57.6	67.8	77.4	96	115
$I_{L(initial)}$ (A)	0.393	0.474	0.55	0.625	0.728	0.815
$I_{L(measured)}$ (A)	0.93	1.156	1.37	1.54	1.945	2.26
Steady-state error percentage (e_{ss})	4.17%	4%	3.14%	3.25%	4%	4.17%
Settling time, T_s (ms)	25	25	25	25	25	25
Overshoot percentage (%OS)	zero	zero	zero	zero	zero	zero

Figures 6.31 and 6.32 show the modulation index curve M and the voltage output signal on the prediction control algorithm with size of step-changed in reference (ΔV_{ref}) 50V and 25V, respectively. The curves of both signals (M and V_o) are similar. This trend is evident in the simulation results of Figure 5.28 to 5.33. Rise time (T_r) and settling time (T_s) were recorded 16ms and 20ms respectively for both conditions with zero percentage overshoot.

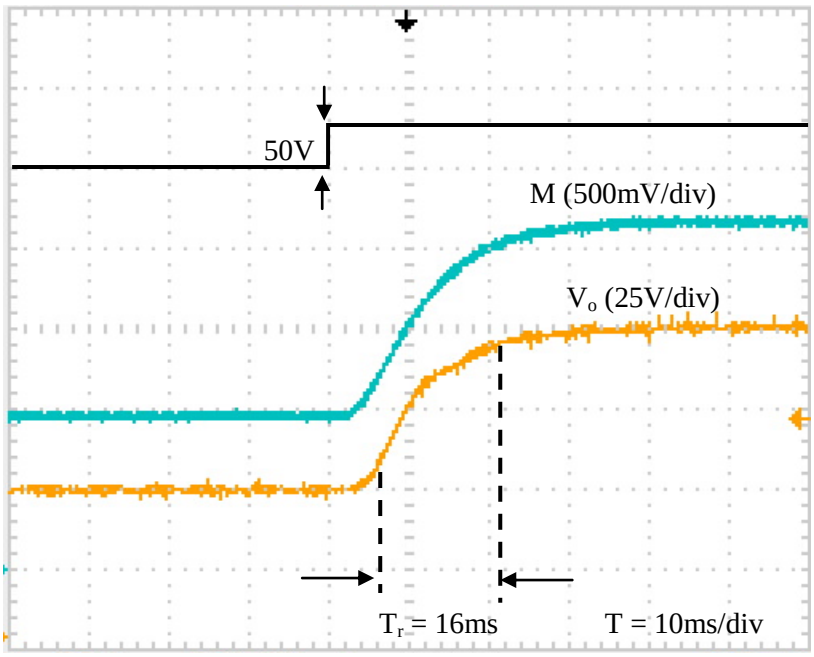


Figure 6.31: M and V_o signals; ΔV_{ref} = 50V

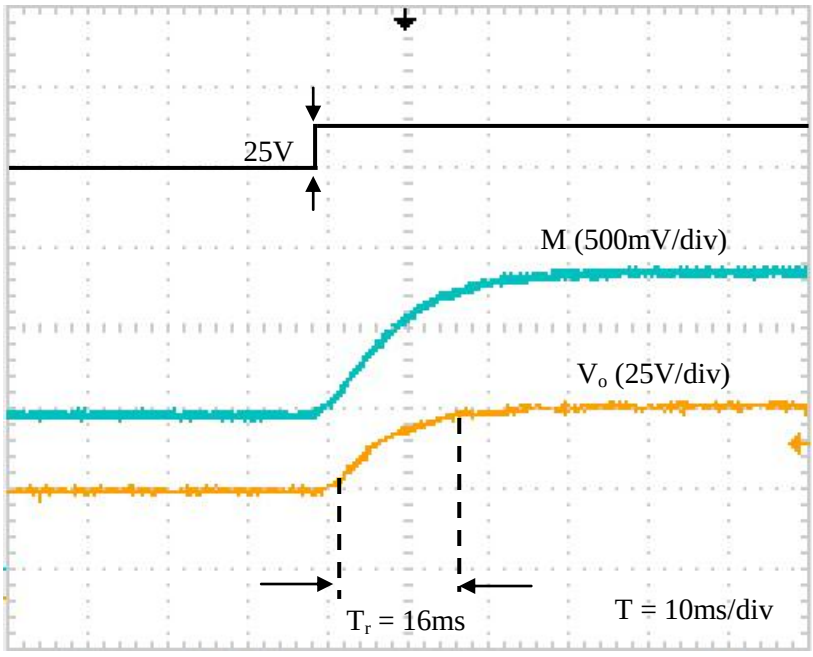


Figure 6.32: M and V_o signals; ΔV_{ref} = 25V

Figures 6.33-6.34 are the transient results for voltage source (V_a), current source (I_a), DC voltage (V_o), and inductor current (I_L); they demonstrate that the transient response (settling time and overshoot percentage) can be controlled by the M-curve-prediction algorithm, by multiplying the sampling time of the algorithm with a variable K_V greater than 0 and the same with or less than 1. The response was faster and the overshoot (especially in I_L) larger when the variable K_V was increased.

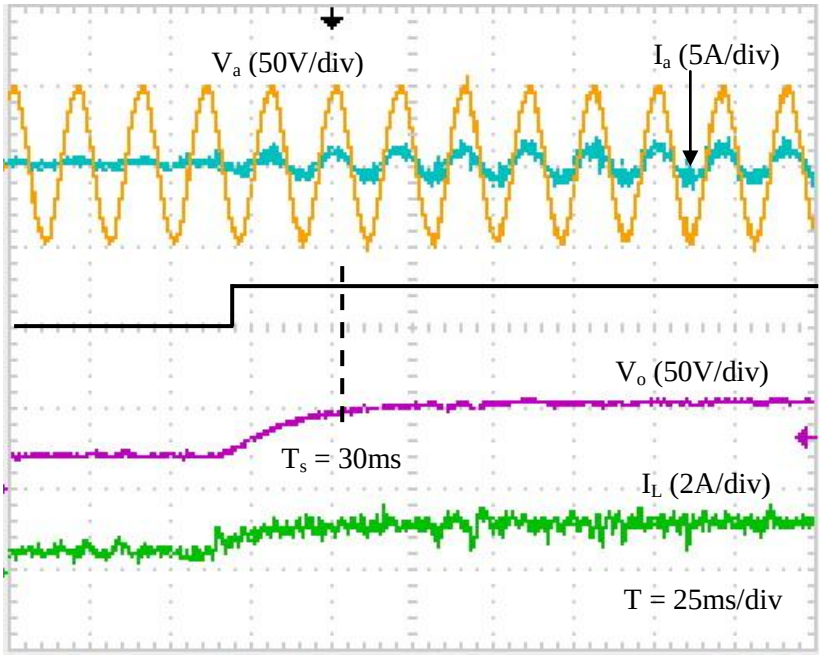


Figure 6.33: The compensated step-up response when $K_V = 0.5$

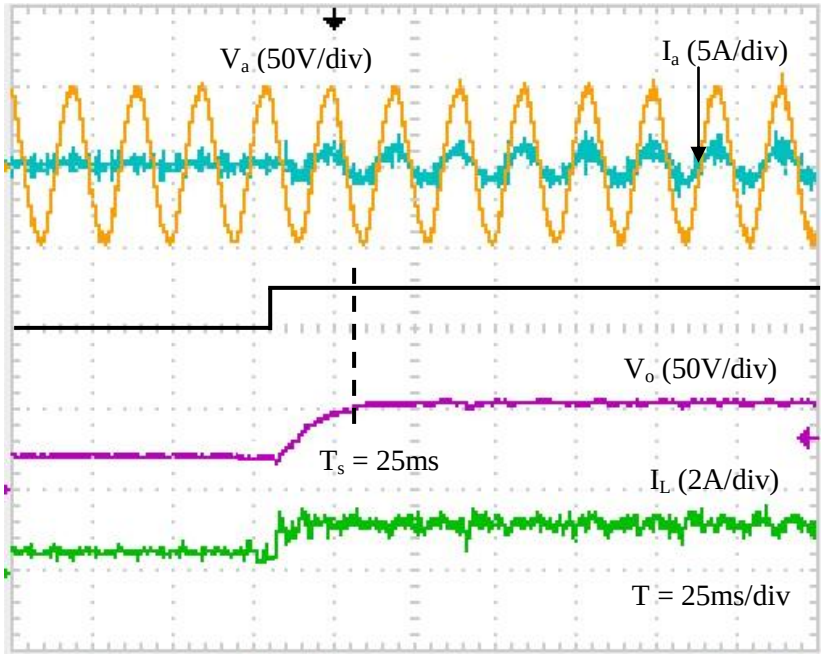


Figure 6.34: The compensated step-up response when $K_V = 1$

6.5 Summary

This chapter discusses the experiment results of the proposed three-phase AC-DC buck-type power converter with bidirectional capability and its proposed PWM modulation strategy. The technique produced the results of unity power factor and sinusoidal AC input currents. A closed-loop system was developed to test the dynamic response to changes in the reference voltage or load values, and two types of control techniques investigated: I-D control and M-curve-prediction control. Both performed well in their transient responses. In terms of steady-state error, the I-D controller produced zero steady-state error whereas the M-curve-prediction control technique produced a small steady-state error (because the prediction algorithm had been determined with the assumption of no losses to the system). A suitable gain can be added to the algorithm to correct the error. The advantage of the M-curve-prediction

control technique over the I-D controller is that it reduces dependence on the feedback-sensor reading. If the sensor detects an error, its reading is averaged and the control algorithm predicts the curve according to the difference in value with the reference. This is significant because the sensor value is sometimes inaccurate, owing to unknown noise.

CHAPTER 7

CONCLUSION AND FUTURE WORK

7.1 Concluding Remarks

In this work a theoretical analysis and verification by simulations and experiments of a bidirectional three-phase AC-DC buck-type converter with a simplified SPWM technique is presented.

The technique has a new modulation strategy that uses one reference signals (0 to 60° and 120° to 180° sine waves) and one type of carrier signal to generate PWM signals. The existing technique of modified SPWM used two references and two carrier signals and was implemented in FPGAs because of their flexibility. The proposed simplified-plus-modified SPWM provide an alternative to design the switching in the provided ePWM module of DSPTMS320F28335. Mathematical analysis and verification of simulation and experiment proved the successful on this new PWM approach.

A conventional six-switch three-phase AC-DC buck converter is extended by incorporating four diodes into each switch to achieve bidirectional power flow. The configuration reduced the number of switches compared to the existing bidirectional configurations. This circuit configuration with its simplified-plus-modified SPWM is developed in Simulink (PowerSim) to analyze the voltage/currents, THD and power factor. The prototype is developed in laboratory for testing and used a TMS320F28335

DSP as the main controller for the system. The open-loop is success but consist a few limitations, especially when step-changing of references and load disturbance are given. These limitations can be solved by a voltage feedback control.

The research is then continued by introducing new approaches of controllers. These controllers addressed the drawbacks of open-loop system by improving the steady-state and dynamic responses. The advantages of the proposed controllers over existing controllers (such as PID, Sliding Mode, Fuzzy PI) are ease of tuning and its use of only one sensor (DC voltage sensor) to achieve zero-steady-state-error output voltage with high dynamic response, whether the disturbance is small or large.

The first controller approach in this work is Integral-Derivative (I-D) that using a two-degrees-of-freedom control model. I-D controller is a SISO scheme with minor-loop voltage control, so that the transient response of the system can be controlled by tuning only the integral gain (K_I) to achieve the desired response through damping ratios 0 to 1 (and suitable values of T_d and K_d). The theoretical strategy of this controller is based on a second-order linear model in Laplace form to diminish complex mathematical equations from system step-response analysis. The proposed controller is a discrete model developed in MATLAB/SIMULINK to assist code-writing in C-program for its DSP implementation. Then, an improved voltage feedback control by designing a modulation-index-curve prediction based-on the placement of closed-loop poles (I-D control) is proposed and discussed as second controller approach. The improved control approach offer simpler implementation, minimize the digital computational burden on the digital signal processor and reduces dependence on feedback-sensor reading.

In conclusion, the thesis has demonstrated the proposed bidirectional configuration, switching strategy and its controller design are able to produce sinusoidal AC current with near-unity power factor and exhibit a desired dynamic response to the load and input reference changes via simulation and experiments.

7.2 Author's Contribution

The research findings or contributions are listed as follow:

1. An improved topology of bidirectional three-phase AC-DC buck-type converter has been developed that utilizes fewer switches than a conventional anti parallel converter.
2. A simplified voltage-based SPWM technique is developed for bidirectional power flow from AC-DC and vice versa to obtain a controllable DC voltage, sinusoidal AC current with low THD and nearly unity power factor.
3. The work has established a digital control algorithm of Integral-Derivative (I-D) controller that has only one DC-voltage feedback sensor and capable of compensating huge transient voltage/current and of achieving zero-steady-state-error output voltage. The transient response can be controlled by tuning the proportional gain (K_p) only, which is an advantage over the cascaded proportional-integral-derivative (PID) that tunes two or three parameters.
4. The work has established an improved voltage feedback control algorithm, namely a modulation-index-curve prediction control technique based-on the placement of closed-loop poles that offer simpler implementation and minimize the digital computational burden on the digital signal processor.
5. The complete controller designs procedures (such as gain tuning) have explained. The output responses has been analysed on transient conditions: step-changing the reference voltage with resistance and inductive loads, and step-changing the resistive load; using different values of gain in simulation.
6. The control principles of I-D controller and modulation-index-curve technique can be applied to any PWM AC–DC buck-type converters or DC-DC converters.

7. The voltage-based SPWM and the control algorithms are fully implemented in DSP TMS320F28335, which offer simpler hardware design.

7.3 Future Works

Future works can be performed on the existing design, to improve the overall performance of the converter in transient and steady-state response. Suggested future works are:

1. New bidirectional three-phase converter topologies need to be investigated to offer optimum performance since the current configuration contributes more losses (more diodes for each leg).
2. Research on filtering design to achieve a better THD in AC mains currents. The LC filtering at AC side need to be investigate to make it suitable to use for bigger range of modulation index. The LC used in this work only successful give lower THD (less than 5%) for $M > 0.6$.
3. Intelligent control algorithm that can decide the suitable gains value for small and large step changing systems in reference inputs and disturbance inputs, also can be considered in future work. As concluded, higher gains provide faster response and larger overshoot (especially in I_L) which suitable for small step-changing in system, and vice versa.

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PUBLICATION FROM THE WORKS

1. A. Alias, N. A. Rahim and M. A. Hussain, "A Single-Input Single-Output Approach by using Minor-Loop Voltage Feedback Compensation with Modified SPWM Technique for Three-Phase AC–DC Buck Converter", *Journal of Power Electronics*, Vol. 13, No. 5, pp. 829-840, Sept. 2013. (ISI cited)

2. A. Alias, N. A. Rahim and M. A. Hussain, "DSP-Based Modified SPWM Switching Technique with Two-degrees-of-freedom Voltage Control for Three-Phase AC-DC Buck Converter", *The Arabian Journal for Science and Engineering.* (ISI cited – Accepted (DOI: 10.1007/s13369-014-1370-6)).

3. Alias, N. A. Rahim and M. A. Hussain, "DSP-Based PWM For Bidirectional Three-Phase AC-DC Buck Converter", *Power and Energy Conversion Symposium (PECS 2012)*, 2012.

4. A. Alias, N. A. Rahim and M. A. Hussain, "Bidirectional Three Phase Power Converter", *1st Clean Energy and Technology (CET 2011)*, 2011.

5. A. Alias, N. A. Rahim and M. A. Hussain, "Simulation and Design Analysis of PWM Strategy for Three-Phase Buck Rectifier"", *2nd UMPEDAC Symposium*, 2011.

6. A. Alias, N. A. Rahim and M. A. Hussain, "An Improved Algorithm of Voltage Feedback Control for PWM Three-Phase AC-DC Buck-Type Converter", (Submitted to IEEE power Electronics (ISI cited)

APPENDIX A

Schematic Circuits

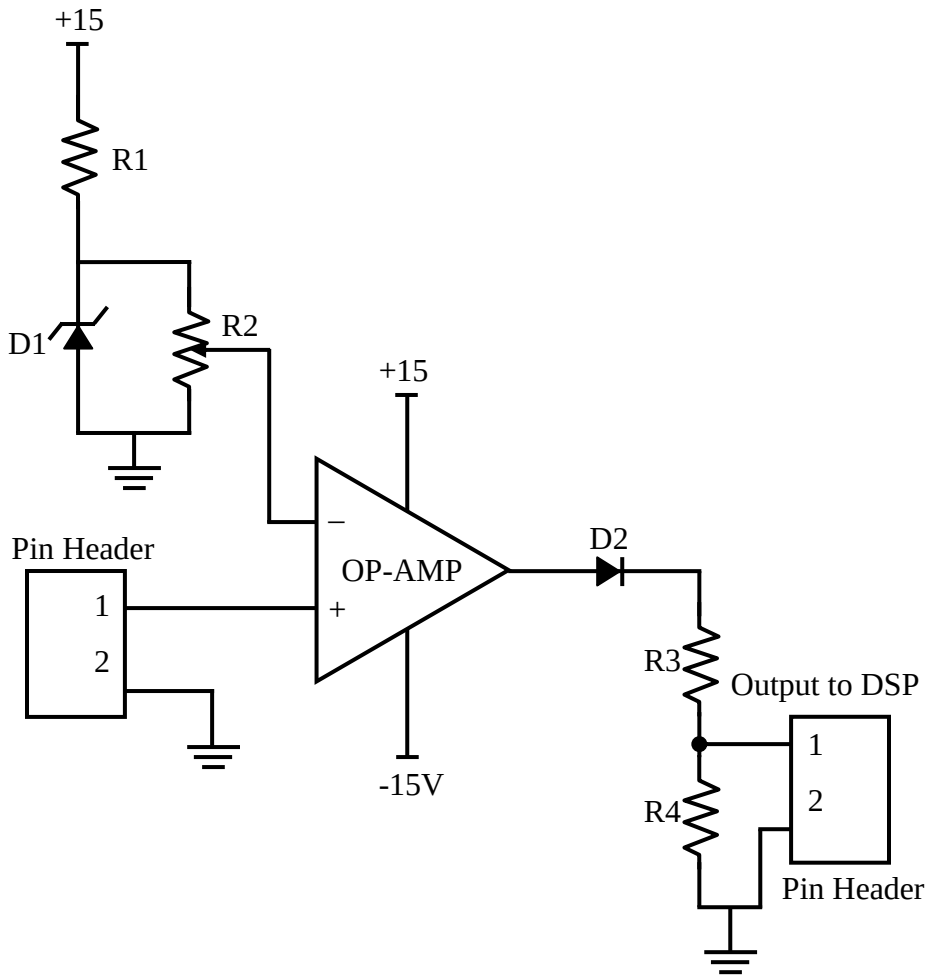

Figure A.1: Zero crossing detector circuit

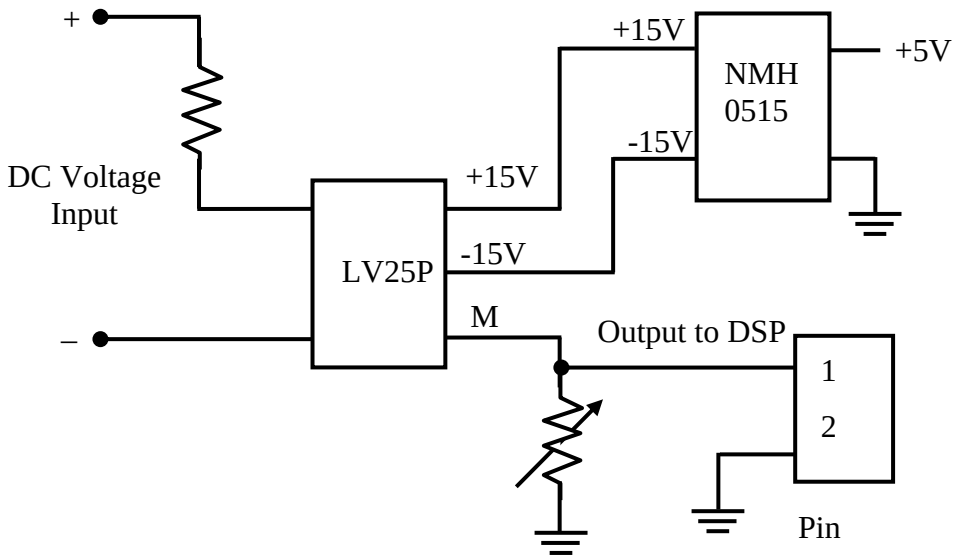

Figure A.2: Voltage sensor circuit

APPENDIX B

MATLAB Source Code

B.1 MATLAB Script to generate Plant's Transfer Functions and I-D Controller in Laplace Domain

```
clear all
R1=0.5;
Ld=6e-3;
Cd=220e-6;
d=1/(Ld*Cd);
c=1/(Ld*Cd);
b=(R1/Ld);
a=1;
num=[1/(Ld*Cd)];%Plant
den=[a b c]; %Plant
G=tf(num,den); %Plant
figure; plot (step(num,den))
wn=sqrt(c);
zeta=b/(2*wn);
OS=exp(-zeta*pi/sqrt((1-zeta^2)))*100;
%Controller parameter
Kd=0.002;
Td=0.0003;
KI=100;
num1=[Kd 0]; %H
den1=[Td 1]; %H
num2=[KI]; %A
den2=[1 0];%A
H=tf(num1,den1);%H
A=tf(num2,den2);%A
B=feedback(G,H);
C=series(A,B);
%closed loop TF
T=feedback(C,1);
figure; step(T)
zerolocation=1/Td;
```

B.2 MATLAB Coding to generate Plant's output in discrete domain

```
close all;
clear all;
fs=19800;
N = 792*10; % Set number of sample
Sampling_Clock = 39600; % Set sampling frequency
Ts=1/Sampling_Clock;
for N1=0:N
tr= (0:N1-1)/Sampling_Clock;
end
Ki=0.5*Ts;
K=7.576*100000;
K1=83.33;
K2=7.576*100000;
error(1)=0;
errorPI(1)=0;
sum(1)=0;
sum1(1)=0;
sum2(1)=0;
sum3(1)=0;
x(1)=0;
tr2(1)=0;
for k=1:N-1
tr2(k+1)=tr(k+1);
x(k+1)=K*1-(sum1(k)+sum3(k));
sum(k+1)=sum(k)+Ki*(x(k+1)+x(k));
sum1(k+1)=sum(k)*K1;
sum2(k+1)=sum2(k)+Ki*(sum(k+1)+sum(k));
sum3(k+1)=sum2(k)*K2;
end
figure, plot(tr,sum2)
```

B.3 MATLAB Coding to generate the output of Plant and I-D Controller in discrete domain

```
close all;
clear all;
fs=19800;
N = 20000; % Set number of sampled data 60000;
Sampling_Clock = 120000; % Set sampling frequency 1000000;
for N1=0:N
tr= (0:N1-1)/Sampling_Clock;
end
Ki=0.5*1/Sampling_Clock;
K=7.5758e005;
K1=83.33;
K2=7.6515e005;
```

```
Kd1=1/0.0003;
Kd2=0.002/0.0003;
Kp=100;
error(1)=0;
errorPI(1)=0;
sum(1)=0;
sum1(1)=0;
sum2(1)=0;
sum3(1)=0;
sumPI(1)=0;
sumPID(1)=0;
d(1)=0;
u(1)=100;
h(1)=0;
errorD(1)=0;
errorD1(1)=0;
errorD2(1)=0;
sumD(1)=0;
Out(1)=0;
for k=1:N-1
if k<8000
   d(k+1)=0; %disturbance is set to zero
else
   d(k+1)=-1; %disturbance is set to one
end
   u(k+1)=100;
h(k+1)=u(k)-sum2(k);
%****DERIVATIVE TERM****
errorD1(k+1)=sum2(k)-(Kd1*sumD(k));
sumD(k+1)=Ki*(errorD1(k+1)+errorD1(k))+sumD(k);
OutD(k+1)=sumD(k+1)+errorD1(k+1)*Kd2;
%****PI CONTROLLER******
sumPI(k+1)=sumPI(k)+Kp*Ki*(h(k+1)+h(k));
%****PLANT****
x(k+1)=K*(sumPI(k+1)-OutD(k+1)+d(k+1))-(sum1(k)+sum3(k)); %d is % disturbance
sum(k+1)=sum(k)+Ki*(x(k+1)+x(k));
sum1(k+1)=sum(k)*K1;  %second integrator of Plant
sum2(k+1)=sum2(k)+Ki*(sum(k+1)+sum(k));
sum3(k+1)=sum2(k)*K2;
end
figure, plot(tr,sum2)
```

APPENDIX C

Main Programming in DSP

```
//###########################################################################
// BY: AZRITA BINTI ALIAS (KHA 090028)
// DATE: 11 July 2012
// FILE: Using voltage sensor PWM example (Update data from Lookup Table -SYSCLKOUT 120MHz)
// HSPCLK-101 (SYSCLKOUT/10) & LOSPCP- 000 (SYSCLKOUT/1)
// SWITCHING FREQUENCY: 19.8kHz
// TITLE: Modified PWM switching for rectifier (6 switches)

#include "DSP28x_Project.h"     // Device Headerfile and Examples Include File

typedef struct
{
  volatile struct EPWM_REGS *EPwmRegHandle;
  Uint16 EPwmTimerIntCount;
  }EPWM_INFO;

// Prototype statements for functions found within this file.
void InitEPwm1Example(void);
void InitEPwm2Example(void);
void InitEPwm3Example(void);
void InitEPwm4Example(void);
interrupt void epwm1_isr(void);
interrupt void epwm2_isr(void);
interrupt void epwm3_isr(void);
interrupt void epwm4_isr(void);
void update_compare1(EPWM_INFO*);
void update_compare2(EPWM_INFO*);
void update_compare3(EPWM_INFO*);
void update_compare4(EPWM_INFO*);
// Global variables used in this example
EPWM_INFO epwm1_info;
EPWM_INFO epwm2_info;
EPWM_INFO epwm3_info;
EPWM_INFO epwm4_info;
//#define M         0.8 // M=0.8
#define EPWM_CMP_UP   1
#define EPWM_CMP_DOWN 0
#define N                               132
#define N1                              792
#define Amp                             303
#define ADC_MODCLK 0x5 // Change...HSPCLK = SYSCLKOUT/2*ADC_MODCLK2 = 150/(2*3)
= 25.0 MHz
#define ADC_CKPS   0x1   // ADC module clock = HSPCLK/2*ADC_CKPS   = 25.0MHz/(1*2) =
12.5MHz
#define ADC_SHCLK  0xf  // S/H width in ADC module periods
Uint16 sampletable[N1];
Uint16
dd,i,j,k,k1,k2,k3,k4,i1,i2,i3,i4,zcd=0,start=0,zcd1=0,start1=0,zcd2=0,start2=0,zcd3=0,start3=0,MI1=0,MI
2=0,MI3=0,MI4=0;
double M,ref,u;
double RefVal[N]={0,      2,      5,      7,      10,     12,     14,     17,     19,     21,
          24,     26,
29,       31,     33,     36,     38,     40,     43,     45,     47,     50,     52,     54, 57,
          59,     61,     64,     66,     68,     71,     73,     75,     78,     80,     82,
85,       87,     89,     91,     94,     96,     98,     100,    103,    105,    107,    109,
112,      114,    116,    118,    120,    123,    125,    127,    129,    131,    133,    135,
```

```
138,    140,    142,    144,    146,    148,    150,    152,    154,    156,    158,    160,
162,    164,    166,    168,    170,    172,    174,    176,    178,    180,    182,    184,
186,    188,    189,    191,    193,    195,    197,    199,    200,    202,    204,    206,
207,    209,    211,    213,    214,    216,    218,    219,    221,    223,    224,    226,
227,    229,    230,    232,    233,    235,    236,    238,    239,    241,    242,    244,
245,    247,    248,    249,    251,    252,    253,    255,    256,    257,    258,    260};
double RefVal1[N]={261, 260,    258,    257,    256,    255,    253,    252,    251,    249,
        248,    247,
245,    244,    242,    241,    239,    238,    236,    235,    233,    232,    230,    229,
227,    226,    224,    223,    221,    219,    218,    216,    214,    213,    211,    209,
207,    206,    204,    202,    200,    199,    197,    195,    193,    191,    189,    188,
186,    184,    182,    180,    178,    176,    174,    172,    170,    168,    166,    164,
162,    160,    158,    156,    154,    152,    150,    148,    146,    144,    142,    140,
138,    135,    133,    131,    129,    127,    125,    123,    120,    118,    116,    114,
112,    109,    107,    105,    103,    100,    98,     96,     94,     91,     89,     87,
85,     82,     80,     78,     75,     73,     71,     68,     66,     64,     61,     59,57,
        54,     52,     50,     47,     45,     43,     40,     38,     36,     33,     31, 29,
        26,     24,     21,     19,     17,     14,     12,     10,     7,      5,      2};
double Ki=0.5*5.05*1e-5,
Kd1=1/0.0003, Kd2=0.002/0.0003, Kp=50; // Proportional
double MM[N1],sumPID[N1],sumPI[N1],sumD[N1],sum2[N1],OutD[N1],summ1[N1];
void main(void)
 {
// Step 1. Initialize System Control:
// PLL, WatchDog, enable Peripheral Clocks
// This example function is found in the DSP2833x_SysCtrl.c file.
   InitSysCtrl();
// Step 2. Initalize GPIO:
// This example function is found in the DSP2833x_Gpio.c file and
// illustrates how to set the GPIO to it's default state.
// InitGpio();  // Skipped for this example
// For this case just init GPIO pins for ePWM1, ePWM2, ePWM3
// These functions are in the DSP2833x_EPwm.c file
   InitEPwm1Gpio();
   InitEPwm2Gpio();
   InitEPwm3Gpio();
   InitEPwm4Gpio();

// Step 3. Clear all interrupts and initialize PIE vector table:
// Disable CPU interrupts
   DINT;

// Initialize the PIE control registers to their default state.
// The default state is all PIE interrupts disabled and flags
// are cleared.
// This function is found in the DSP2833x_PieCtrl.c file.
   InitPieCtrl();

// Disable CPU interrupts and clear all CPU interrupt flags:
   IER = 0x0000;
   IFR = 0x0000;

// Initialize the PIE vector table with pointers to the shell Interrupt
// Service Routines (ISR).
// This will populate the entire table, even if the interrupt
// is not used in this example.  This is useful for debug purposes.
// The shell ISR routines are found in DSP2833x_DefaultIsr.c.
// This function is found in DSP2833x_PieVect.c.
   InitPieVectTable();
   InitAdc();  // For this example, init the ADC
// Specific ADC setup for this example:
   AdcRegs.ADCMAXCONV.all=1;  //two conversion are required,eg. if 5 conv , set it as 4 or 1 conv, set
it as 0
```

```
   AdcRegs.ADCTRL1.bit.ACQ_PS = ADC_SHCLK;
   AdcRegs.ADCTRL3.bit.ADCCLKPS = ADC_CKPS;
   AdcRegs.ADCTRL1.bit.SEQ_CASC = 1;        // 1  Cascaded mode
   AdcRegs.ADCCHSELSEQ1.bit.CONV00 = 0x0;
   AdcRegs.ADCCHSELSEQ1.bit.CONV01 = 0x1;
   AdcRegs.ADCTRL1.bit.CONT_RUN = 1;       // Setup continuous run


// Step 5. User specific code, enable interrupts:
// Start SEQ1
   AdcRegs.ADCTRL2.all = 0x2000;
// Interrupts that are used in this example are re-mapped to
// ISR functions found within this file.
   EALLOW;  // This is needed to write to EALLOW protected registers
   PieVectTable.EPWM1_INT = &epwm1_isr;
   PieVectTable.EPWM2_INT = &epwm2_isr;
   PieVectTable.EPWM3_INT = &epwm3_isr;
   PieVectTable.EPWM4_INT = &epwm4_isr;
   EDIS;    // This is needed to disable write to EALLOW protected registers

// Step 4. Initialize all the Device Peripherals:
// This function is found in DSP2833x_InitPeripherals.c
// InitPeripherals();  // Not required for this example

// For this example, only initialize the ePWM

  EALLOW;
  SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 0;
  EDIS;

   InitEPwm1Example();
   InitEPwm2Example();
   InitEPwm3Example();
   InitEPwm4Example();

   EALLOW;
   SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 1;
   EDIS;
// Step 5. User specific code, enable interrupts:
   EALLOW;
   GpioCtrlRegs.GPAPUD.bit.GPIO12= 0;   // Enable pullup on GPIO6 // ZCD
   GpioCtrlRegs.GPAMUX1.bit.GPIO12= 0;   // GPIO12 = GPIO6
   GpioCtrlRegs.GPADIR.bit.GPIO12= 0;   // GPIO12 = Input
   GpioCtrlRegs.GPAPUD.bit.GPIO19= 0;   // Enable pullup on GPIO19 // REFERENCE INPUT
CHANGING (S1)
   GpioCtrlRegs.GPAMUX2.bit.GPIO19= 0;   // GPIO19 = GPIO19
   GpioCtrlRegs.GPADIR.bit.GPIO19= 0;   // GPIO19 = Input
   EDIS;

// Enable CPU INT3 which is connected to EPWM1-3 INT:
   IER |= M_INT3;

// Enable EPWM INTn in the PIE: Group 3 interrupt 1-3
   PieCtrlRegs.PIEIER3.bit.INTx1 = 1;
   PieCtrlRegs.PIEIER3.bit.INTx2 = 1;
   PieCtrlRegs.PIEIER3.bit.INTx3 = 1;
   PieCtrlRegs.PIEIER3.bit.INTx4 = 1;

// Enable global Interrupts and higher priority real-time debug events:
   EINT;   // Enable Global interrupt INTM
   ERTM;   // Enable Global realtime interrupt DBGM

// Step 6. IDLE loop. Just sit and loop forever (optional):
```

```
//            sumPID[0]=0;
//            MM[0]=0;
//            sumPI[0]=0;
//            sumD[0]=0;
//            OutD[0]=0;
              sum2[0]=0;
              dd=0;
//            sampletable[0]=0;
//            for (i=0; i<N1;i++)
 //           {//sum2[i]=0;
 //    MM[i]=0;
 //    sumPID[i]=0;
//             sumD[i]=0;
//             OutD[i]=0;
//             sumPI[i]=0;
//             sampletable[i]=0;
//             summ1[i]=0;}
   while(1)
   {MI1=GpioDataRegs.GPADAT.bit.GPIO19; // Switch S4
    if (k4<N1)
    {k=k4;
            if(MI1==1)
    {M=0.5;
    sampletable[k]=((AdcRegs.ADCRESULT0>>4));
              summ1[k]=(sampletable[k])*1000000;
              sum2[k]=((summ1[k])*3/4096/1000000);  // ref value
    sumPID[k]=0;
              MM[k]=0.6;
              sumPI[k]=0;
              sumD[k]=0;
              OutD[k]=0;
//            sum2[k]=0;
              }
    else{
              MM[k+1]=0.3;
    ref=0.8;
              sampletable[k+1]=((AdcRegs.ADCRESULT0>>4));
              summ1[k+1]=sampletable[k+1]*1000000;
              sum2[k+1]=summ1[k+1]*3/4096/1000000;
              sumD[k+1]= Ki*((sum2[k]-(Kd1*sumD[k]))+ (sum2[k-1]-(Kd1*sumD[k-1])))+ (sumD[k]);
//Derivative
              OutD[k+1]=sumD[k+1]+Kd2*(sum2[k]-(Kd1*sumD[k])); //Derivative
              sumPI[k+1]=sumPI[k]+Kp*Ki*((ref-sum2[k+1])+ (ref-sum2[k]));
              sumPID[k+1]=sumPI[k+1]-OutD[k+1]; // Input to the plant

 //           dd=1;}
//            else {
              //MM[k+1]=sumPID[k+1]/(1.5*0.9);
              //if (MM[k+1]>= 0.99){MM[k+1]=0.95;}
                        }}//}
              //          {
              //} //0.15V=15V vinput : ratio 1.5V=150V
   //  MM[k]=0.4;}}
  // M=0.4;}}
    else {sumPID[0]=sumPID[k];
              sumD[0]=sumD[k];
              OutD[0]=OutD[k];
              sumPI[0]=sumPI[k];
//            MM[0]=MM[k];
              sum2[0]=sum2[k];
    }
              }
```

```
 }
interrupt void epwm1_isr(void)
{   // Update the CMPA and CMPB values
  zcd=GpioDataRegs.GPADAT.bit.GPIO12;
   if(zcd==0 && start==0 && EPwm1Regs.ETSEL.bit.INTSEL== ET_CTR_ZERO)
   {start=1;}
   if(start==1 && zcd==1 && EPwm1Regs.ETSEL.bit.INTSEL== ET_CTR_PRD)
   {epwm1_info.EPwmTimerIntCount=0;   //Change 528
   k1=0;   //Change 528
   start=0;
   }
  update_compare1(&epwm1_info);
   if (epwm1_info.EPwmTimerIntCount<791)
   {epwm1_info.EPwmTimerIntCount++;
   k1=epwm1_info.EPwmTimerIntCount;
   }
   else
   {epwm1_info.EPwmTimerIntCount=0;
   k1=0;
   }
   if(EPwm1Regs.ETSEL.bit.INTSEL == ET_CTR_ZERO)
   {EPwm1Regs.ETSEL.bit.INTSEL = ET_CTR_PRD;}
   else
   {EPwm1Regs.ETSEL.bit.INTSEL = ET_CTR_ZERO;}
   // Clear INT flag for this timer
    EPwm1Regs.ETCLR.bit.INT = 1;
            EALLOW;
            SysCtrlRegs.WDKEY=0x55;
            EDIS;

   // Acknowledge this interrupt to receive more interrupts from group 3
   PieCtrlRegs.PIEACK.all = PIEACK_GROUP3;
}

interrupt void epwm2_isr(void)
{  // Update the CMPA and CMPB values
   zcd1=GpioDataRegs.GPADAT.bit.GPIO12;
   if(zcd1==0 && start1==0 && EPwm2Regs.ETSEL.bit.INTSEL== ET_CTR_ZERO)
   {start1=1;}
   if(start1==1 && zcd1==1 && EPwm2Regs.ETSEL.bit.INTSEL== ET_CTR_PRD)
   {epwm2_info.EPwmTimerIntCount=0;  //Change 528
   k2=0;  //Change 528
   start1=0;
   }
  update_compare2(&epwm2_info);
   if (epwm2_info.EPwmTimerIntCount<791)
   {epwm2_info.EPwmTimerIntCount++;
   k2=epwm2_info.EPwmTimerIntCount;}
   else
   {epwm2_info.EPwmTimerIntCount=0;
   k2=0;}
   if(EPwm2Regs.ETSEL.bit.INTSEL == ET_CTR_ZERO)
   {EPwm2Regs.ETSEL.bit.INTSEL = ET_CTR_PRD;}
   else
   {EPwm2Regs.ETSEL.bit.INTSEL = ET_CTR_ZERO;}
   // Clear INT flag for this timer
    EPwm2Regs.ETCLR.bit.INT = 1;
            EALLOW;
            SysCtrlRegs.WDKEY=0x55;
            EDIS;
    // Acknowledge this interrupt to receive more interrupts from group 3
   PieCtrlRegs.PIEACK.all = PIEACK_GROUP3;
}
```

```
interrupt void epwm3_isr(void)
{  // Update the CMPA and CMPB values
   zcd2=GpioDataRegs.GPADAT.bit.GPIO12;
   if(zcd2==0 && start2==0 && EPwm3Regs.ETSEL.bit.INTSEL== ET_CTR_ZERO)
   {start2=1;}
   if(start2==1 && zcd2==1 && EPwm3Regs.ETSEL.bit.INTSEL== ET_CTR_PRD)
   {epwm3_info.EPwmTimerIntCount=0;    //Change 528
   k3=0;  //Change 528
   start2=0;
   }
  update_compare3(&epwm3_info);
   if (epwm3_info.EPwmTimerIntCount<791)
   {epwm3_info.EPwmTimerIntCount++;
   k3=epwm3_info.EPwmTimerIntCount;}
   else
   {epwm3_info.EPwmTimerIntCount=0;
   k3=0;}
   if(EPwm3Regs.ETSEL.bit.INTSEL == ET_CTR_ZERO)
   {EPwm3Regs.ETSEL.bit.INTSEL = ET_CTR_PRD;}
   else
   {EPwm3Regs.ETSEL.bit.INTSEL = ET_CTR_ZERO;}
   // Clear INT flag for this timer
    EPwm3Regs.ETCLR.bit.INT = 1;
            EALLOW;
            SysCtrlRegs.WDKEY=0x55;
            EDIS;
    // Acknowledge this interrupt to receive more interrupts from group 3
   PieCtrlRegs.PIEACK.all = PIEACK_GROUP3;
}
interrupt void epwm4_isr(void)
{   // Update the CMPA and CMPB values
  //zcd=GpioDataRegs.GPADAT.bit.GPIO12;
 //  if(zcd3==0 && start3==0 && EPwm4Regs.ETSEL.bit.INTSEL== ET_CTR_ZERO)
 //  {start3=1;}
//   if(start3==1 && zcd3==1 && EPwm4Regs.ETSEL.bit.INTSEL== ET_CTR_PRD)
//   {epwm4_info.EPwmTimerIntCount=528;   //Change 528
//   k4=528;   //Change 528
//   start3=0;
//   }

  update_compare4(&epwm4_info);
   if (epwm4_info.EPwmTimerIntCount<N1)
   {epwm4_info.EPwmTimerIntCount++;
   k4=epwm4_info.EPwmTimerIntCount;}
   else
   {epwm4_info.EPwmTimerIntCount=0;
   k4=0;}
  // if(EPwm4Regs.ETSEL.bit.INTSEL == ET_CTR_ZERO)
  // {EPwm4Regs.ETSEL.bit.INTSEL = ET_CTR_PRD;}
  // else
  // {EPwm4Regs.ETSEL.bit.INTSEL = ET_CTR_ZERO;}
   // Clear INT flag for this timer
    EPwm4Regs.ETCLR.bit.INT = 1;
            EALLOW;
            SysCtrlRegs.WDKEY=0x55;
            EDIS;

   // Acknowledge this interrupt to receive more interrupts from group 3
   PieCtrlRegs.PIEACK.all = PIEACK_GROUP3;
}

void InitEPwm1Example()
```

```
{ // Setup TBCLK
  EPwm1Regs.TBPRD = 303;          // Set timer period 801 TBCLKs
  EPwm1Regs.TBPHS.half.TBPHS = 0x0000;          // Phase is 0
  EPwm1Regs.TBCTR = 0x0000;                     // Clear counter
    // Set Compare values
  EPwm1Regs.CMPA.half.CMPA = 0;     // Set compare A value
  EPwm1Regs.CMPB = 0;               // Set Compare B value
    // Setup counter mode
  EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Count up
  EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE;       // Disable phase loading
  EPwm1Regs.TBCTL.bit.HSPCLKDIV = 0x5;       // Clock ratio to SYSCLKOUT
  EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;
  // Setup shadowing
  EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
  EPwm1Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
  EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO_PRD;  // Load on Zero
  EPwm1Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO_PRD;
  // Set actions
  EPwm1Regs.AQCTLA.bit.CAU = AQ_SET;            // Set PWM1A on event A, up count
  EPwm1Regs.AQCTLA.bit.CAD = AQ_CLEAR;          // Clear PWM1A on event A, down count
  EPwm1Regs.AQCTLB.bit.CBU = AQ_SET;            // Set PWM1B on event B, up count
  EPwm1Regs.AQCTLB.bit.CBD = AQ_CLEAR;          // Clear PWM1B on event B, down count
   // Interrupt where we will change the Compare Values
  EPwm1Regs.ETSEL.bit.INTSEL = ET_CTR_PRD;
  EPwm1Regs.ETSEL.bit.INTEN = 1;                // Enable INT
  EPwm1Regs.ETPS.bit.INTPRD= ET_1ST;           // Generate INT on 1st event
  //epwm1_info.EPwm_CMPA_Direction = EPWM_CMP_UP;   // Start by increasing CMPA &
 // epwm1_info.EPwm_CMPB_Direction = EPWM_CMP_UP; // decreasing CMPB
  epwm1_info.EPwmTimerIntCount = 0;             // Zero the interrupt counter
  epwm1_info.EPwmRegHandle = &EPwm1Regs;         // Set the pointer to the ePWM module
  }

void InitEPwm2Example()
{   // Setup TBCLK
  EPwm2Regs.TBPRD = 303;          // Set timer period 801 TBCLKs
  EPwm2Regs.TBPHS.half.TBPHS = 0x0000;          // Phase is 0
  EPwm2Regs.TBCTR = 0x0000;                     // Clear counter
  // Set Compare values
  EPwm2Regs.CMPA.half.CMPA = 0;     // Set compare A value
  EPwm2Regs.CMPB = 0;               // Set Compare B value
  // Setup counter mode
  EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Count up
  EPwm2Regs.TBCTL.bit.PHSEN = TB_DISABLE;       // Disable phase loading
  EPwm2Regs.TBCTL.bit.HSPCLKDIV = 0x5;       // Clock ratio to SYSCLKOUT
  EPwm2Regs.TBCTL.bit.CLKDIV = TB_DIV1;
  // Setup shadowing
  EPwm2Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
  EPwm2Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
  EPwm2Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO_PRD;  // Load on Zero
  EPwm2Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO_PRD;
  // Set actions
  EPwm2Regs.AQCTLA.bit.CAU = AQ_SET;            // Set PWM1A on event A, up count
  EPwm2Regs.AQCTLA.bit.CAD = AQ_CLEAR;          // Clear PWM1A on event A, down count
  EPwm2Regs.AQCTLB.bit.CBU = AQ_SET;            // Set PWM1B on event B, up count
  EPwm2Regs.AQCTLB.bit.CBD = AQ_CLEAR;          // Clear PWM1B on event B, down count
  // Interrupt where we will change the Compare Values
  EPwm2Regs.ETSEL.bit.INTSEL = ET_CTR_PRD;      // Select INT on Zero event
  EPwm2Regs.ETSEL.bit.INTEN = 1;                // Enable INT
  EPwm2Regs.ETPS.bit.INTPRD = ET_1ST;           // Generate INT on 1st event
 // epwm2_info.EPwm_CMPA_Direction = EPWM_CMP_UP;   // Start by increasing CMPA &
//  epwm2_info.EPwm_CMPB_Direction = EPWM_CMP_DOWN; // decreasing CMPB
  epwm2_info.EPwmTimerIntCount = 0;             // Zero the interrupt counter
  epwm2_info.EPwmRegHandle = &EPwm2Regs;         // Set the pointer to the ePWM module
```

```
  }
void InitEPwm3Example()
{   // Setup TBCLK
   EPwm3Regs.TBPRD = 303;          // Set timer period 801 TBCLKs
   EPwm3Regs.TBPHS.half.TBPHS = 0x0000;          // Phase is 0
   EPwm3Regs.TBCTR = 0x0000;                     // Clear counter
   // Set Compare values
   EPwm3Regs.CMPA.half.CMPA = 0;     // Set compare A value
   EPwm3Regs.CMPB = 0;              // Set Compare B value
   // Setup counter mode
   EPwm3Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Count up
   EPwm3Regs.TBCTL.bit.PHSEN = TB_DISABLE;        // Disable phase loading
   EPwm3Regs.TBCTL.bit.HSPCLKDIV = 0x5;       // Clock ratio to SYSCLKOUT
   EPwm3Regs.TBCTL.bit.CLKDIV = TB_DIV1;
   // Setup shadowing
   EPwm3Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
   EPwm3Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
   EPwm3Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO_PRD;  // Load on Zero
   EPwm3Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO_PRD;
   // Set actions
   EPwm3Regs.AQCTLA.bit.CAU = AQ_SET;             // Set PWM1A on event A, up count
   EPwm3Regs.AQCTLA.bit.CAD = AQ_CLEAR;           // Clear PWM1A on event A, down count
   EPwm3Regs.AQCTLB.bit.CBU = AQ_SET;             // Set PWM1B on event B, up count
   EPwm3Regs.AQCTLB.bit.CBD = AQ_CLEAR;           // Clear PWM1B on event B, down count
   // Interrupt where we will change the Compare Values
   EPwm3Regs.ETSEL.bit.INTSEL = ET_CTR_PRD;      // Select INT on Zero event
   EPwm3Regs.ETSEL.bit.INTEN = 1;                // Enable INT
   EPwm3Regs.ETPS.bit.INTPRD = ET_1ST;           // Generate INT on 1st event
  // epwm3_info.EPwm_CMPA_Direction = EPWM_CMP_UP;   // Start by increasing CMPA &
  // epwm3_info.EPwm_CMPB_Direction = EPWM_CMP_DOWN; // decreasing CMPB
   epwm3_info.EPwmTimerIntCount = 0;              // Zero the interrupt counter
   epwm3_info.EPwmRegHandle = &EPwm3Regs;         // Set the pointer to the ePWM module
   }
void InitEPwm4Example()
{ // Setup TBCLK
   EPwm4Regs.TBPRD = 303;          // Set timer period 801 TBCLKs
   EPwm4Regs.TBPHS.half.TBPHS = 0x0000;          // Phase is 0
   EPwm4Regs.TBCTR = 0x0000;                     // Clear counter
     // Set Compare values
   EPwm4Regs.CMPA.half.CMPA = 0;     // Set compare A value
   EPwm4Regs.CMPB = 0;              // Set Compare B value
     // Setup counter mode
   EPwm4Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Count up
   EPwm4Regs.TBCTL.bit.PHSEN = TB_DISABLE;        // Disable phase loading
   EPwm4Regs.TBCTL.bit.HSPCLKDIV = 0x5;       // Clock ratio to SYSCLKOUT
   EPwm4Regs.TBCTL.bit.CLKDIV = TB_DIV1;
   // Setup shadowing
   EPwm4Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
   EPwm4Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
   EPwm4Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO_PRD;  // Load on Zero
   EPwm4Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO_PRD;
   // Set actions
   EPwm4Regs.AQCTLA.bit.CAU = AQ_SET;             // Set PWM1A on event A, up count
   EPwm4Regs.AQCTLA.bit.CAD = AQ_CLEAR;           // Clear PWM1A on event A, down count
   EPwm4Regs.AQCTLB.bit.CBU = AQ_SET;             // Set PWM1B on event B, up count
   EPwm4Regs.AQCTLB.bit.CBD = AQ_CLEAR;           // Clear PWM1B on event B, down count
    // Interrupt where we will change the Compare Values
   EPwm4Regs.ETSEL.bit.INTSEL = ET_CTR_PRD;
   EPwm4Regs.ETSEL.bit.INTEN = 1;                // Enable INT
   EPwm4Regs.ETPS.bit.INTPRD= ET_1ST;           // Generate INT on 1st event
   //epwm1_info.EPwm_CMPA_Direction = EPWM_CMP_UP;   // Start by increasing CMPA &
  // epwm1_info.EPwm_CMPB_Direction = EPWM_CMP_UP; // decreasing CMPB
   epwm4_info.EPwmTimerIntCount = 0;              // Zero the interrupt counter
```

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  epwm4_info.EPwmRegHandle = &EPwm4Regs;          // Set the pointer to the ePWM module
  }

void update_compare1(EPWM_INFO *epwm_info)
{  // Every event, change the CMPA/CMPB values
 // Every event, change the CMPA/CMPB values
  if (k1 < 132)
  {EPwm1Regs.CMPA.half.CMPA=RefVal[k1]*MM[k4];
          EPwm1Regs.CMPB=EPwm1Regs.CMPA.half.CMPA;
          EPwm1Regs.AQCTLA.bit.CBU = AQ_CLEAR;
          EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;
          EPwm1Regs.AQCTLA.bit.CAD = AQ_SET;
          EPwm1Regs.AQCTLA.bit.CBD = AQ_SET;
          EPwm1Regs.AQCTLB.bit.CAU = AQ_CLEAR;
          EPwm1Regs.AQCTLB.bit.CBU = AQ_CLEAR;
          EPwm1Regs.AQCTLB.bit.CAD = AQ_CLEAR;
          EPwm1Regs.AQCTLB.bit.CBD = AQ_CLEAR;
          }
  else if (k1 == 132)
  {EPwm1Regs.CMPA.half.CMPA = RefVal[0]*MM[k4];
          EPwm1Regs.CMPB = Amp-(RefVal1[0]*MM[k4]);
          EPwm1Regs.AQCTLA.bit.CAU = AQ_SET;
          EPwm1Regs.AQCTLA.bit.CBU = AQ_SET;
   EPwm1Regs.AQCTLB.bit.CAU = AQ_CLEAR;   //Change
          EPwm1Regs.AQCTLB.bit.CBU = AQ_CLEAR;}
  else if(k1 < 264)
  {i1= k1-132;
   EPwm1Regs.CMPA.half.CMPA=RefVal[i1]*MM[k4];
          EPwm1Regs.CMPB=Amp-(RefVal1[i1]*MM[k4]);
   EPwm1Regs.AQCTLA.bit.CAD = AQ_SET;
   EPwm1Regs.AQCTLA.bit.CBD = AQ_SET;
          EPwm1Regs.AQCTLA.bit.CAU = AQ_SET;
          EPwm1Regs.AQCTLA.bit.CBU = AQ_SET;
   EPwm1Regs.AQCTLB.bit.CBD = AQ_CLEAR;   //Change
          EPwm1Regs.AQCTLB.bit.CAD = AQ_CLEAR;
   EPwm1Regs.AQCTLB.bit.CAU = AQ_CLEAR;  //Change
          EPwm1Regs.AQCTLB.bit.CBU = AQ_CLEAR;
  }
   else if (k1 == 264)
  {EPwm1Regs.CMPB = 0;
   EPwm1Regs.CMPA.half.CMPA = Amp-(RefVal1[0]*MM[k4]);
   EPwm1Regs.AQCTLA.bit.CBU = AQ_CLEAR;
   EPwm1Regs.AQCTLA.bit.CAU = AQ_SET;
          EPwm1Regs.AQCTLB.bit.CBU = AQ_CLEAR;
   EPwm1Regs.AQCTLB.bit.CAU = AQ_CLEAR;
   }
   else if(k1 < 396)
   {i1=k1-264;
          EPwm1Regs.CMPA.half.CMPA=Amp-(RefVal1[i1]*MM[k4]);
          EPwm1Regs.CMPB=EPwm1Regs.CMPA.half.CMPA;
          EPwm1Regs.AQCTLA.bit.CAU = AQ_SET;
          EPwm1Regs.AQCTLA.bit.CBU = AQ_SET;
          EPwm1Regs.AQCTLA.bit.CAD = AQ_CLEAR;
   EPwm1Regs.AQCTLA.bit.CBD = AQ_CLEAR;
   EPwm1Regs.AQCTLB.bit.CAU = AQ_CLEAR;
          EPwm1Regs.AQCTLB.bit.CBU = AQ_CLEAR;
          EPwm1Regs.AQCTLB.bit.CAD = AQ_CLEAR;
   EPwm1Regs.AQCTLB.bit.CBD = AQ_CLEAR;}
          else if(k1 < 528)
  {i1=k1-396;
   EPwm1Regs.CMPA.half.CMPA=RefVal[i1]*MM[k4];
   EPwm1Regs.CMPB=EPwm1Regs.CMPA.half.CMPA;
   EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;
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   EPwm1Regs.AQCTLA.bit.CAD = AQ_CLEAR;
   EPwm1Regs.AQCTLA.bit.CBU = AQ_CLEAR;
   EPwm1Regs.AQCTLA.bit.CBD = AQ_CLEAR;
   EPwm1Regs.AQCTLB.bit.CAU = AQ_CLEAR;
   EPwm1Regs.AQCTLB.bit.CBU = AQ_CLEAR;
   EPwm1Regs.AQCTLB.bit.CAD = AQ_SET;
   EPwm1Regs.AQCTLB.bit.CBD = AQ_SET;}
  else if (k1 == 528)
  {EPwm1Regs.CMPA.half.CMPA = RefVal[0]*MM[k4];
          EPwm1Regs.CMPB = Amp-(RefVal1[0]*M);
          EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;     //Change
          EPwm1Regs.AQCTLA.bit.CBU = AQ_CLEAR;
          EPwm1Regs.AQCTLB.bit.CAU = AQ_SET;
          EPwm1Regs.AQCTLB.bit.CBU = AQ_SET;}
  else if (k1 < 660)
  {i1= k1-528;
          EPwm1Regs.CMPA.half.CMPA=RefVal[i1]*MM[k4];
          EPwm1Regs.CMPB=Amp-(RefVal1[i1]*MM[k4]);
          EPwm1Regs.AQCTLA.bit.CBD = AQ_CLEAR;   //Change
          EPwm1Regs.AQCTLA.bit.CAD = AQ_CLEAR;
   EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;   //Change
          EPwm1Regs.AQCTLA.bit.CBU = AQ_CLEAR;
          EPwm1Regs.AQCTLB.bit.CAD = AQ_SET;
          EPwm1Regs.AQCTLB.bit.CBD = AQ_SET;
          EPwm1Regs.AQCTLB.bit.CAU = AQ_SET;
          EPwm1Regs.AQCTLB.bit.CBU = AQ_SET;}
  else if (k1 == 660)
 {EPwm1Regs.CMPA.half.CMPA = Amp-(RefVal1[0]*MM[k4]);
  EPwm1Regs.CMPB =0;
  EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;
  EPwm1Regs.AQCTLA.bit.CBU = AQ_CLEAR;
  EPwm1Regs.AQCTLB.bit.CAU = AQ_SET;
  EPwm1Regs.AQCTLB.bit.CBU = AQ_CLEAR;}
  else
  {i1= k1-660;
          EPwm1Regs.CMPA.half.CMPA=Amp-(RefVal1[i1]*MM[k4]);
          EPwm1Regs.CMPB= EPwm1Regs.CMPA.half.CMPA;
          EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;
          EPwm1Regs.AQCTLA.bit.CBU = AQ_CLEAR;
          EPwm1Regs.AQCTLA.bit.CAD = AQ_CLEAR;
          EPwm1Regs.AQCTLA.bit.CBD = AQ_CLEAR;
          EPwm1Regs.AQCTLB.bit.CAU = AQ_SET;
          EPwm1Regs.AQCTLB.bit.CAD = AQ_CLEAR;
          EPwm1Regs.AQCTLB.bit.CBU = AQ_SET;
          EPwm1Regs.AQCTLB.bit.CBD = AQ_CLEAR;
          EALLOW;
          SysCtrlRegs.WDKEY=0xAA;
          EDIS;
  }
    return;
}

void update_compare2(EPWM_INFO *epwm_info)
{   // Every event, change the CMPA/CMPB values
  if (k2 == 0)
  {EPwm2Regs.CMPA.half.CMPA = RefVal[0]*MM[k4];
          EPwm2Regs.CMPB = Amp-(RefVal1[0]*MM[k4]);
          EPwm2Regs.AQCTLA.bit.CAU = AQ_CLEAR;  //Change
          EPwm2Regs.AQCTLA.bit.CBU = AQ_CLEAR;
   EPwm2Regs.AQCTLB.bit.CAU = AQ_SET;
          EPwm2Regs.AQCTLB.bit.CBU = AQ_SET;}
  else if(k2 < 132)
  {EPwm2Regs.CMPA.half.CMPA=RefVal[k2]*MM[k4];
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        EPwm2Regs.CMPB=Amp-(RefVal1[k2]*MM[k4]);
        EPwm2Regs.AQCTLA.bit.CAU = AQ_CLEAR;    //Change
        EPwm2Regs.AQCTLA.bit.CBU = AQ_CLEAR;
        EPwm2Regs.AQCTLA.bit.CAD = AQ_CLEAR;
        EPwm2Regs.AQCTLA.bit.CBD = AQ_CLEAR;   //Change
        EPwm2Regs.AQCTLB.bit.CAU = AQ_SET;
        EPwm2Regs.AQCTLB.bit.CBU = AQ_SET;
        EPwm2Regs.AQCTLB.bit.CAD = AQ_SET;
        EPwm2Regs.AQCTLB.bit.CBD = AQ_SET;}
else if (k2 == 132)
{EPwm2Regs.CMPA.half.CMPA = Amp-(RefVal1[0]*MM[k4]);
        EPwm2Regs.CMPB = 0;
        EPwm2Regs.AQCTLA.bit.CAU = AQ_CLEAR;
        EPwm2Regs.AQCTLA.bit.CBU = AQ_CLEAR;
 EPwm2Regs.AQCTLB.bit.CAU = AQ_SET;
        EPwm2Regs.AQCTLB.bit.CBU = AQ_CLEAR;}
else if(k2 < 264)
{i2= k2-132;
 EPwm2Regs.CMPA.half.CMPA=Amp-(RefVal1[i2]*MM[k4]);
 EPwm2Regs.CMPB= EPwm2Regs.CMPA.half.CMPA;
 EPwm2Regs.AQCTLA.bit.CAU = AQ_CLEAR;
 EPwm2Regs.AQCTLA.bit.CBU = AQ_CLEAR;
 EPwm2Regs.AQCTLA.bit.CAD = AQ_CLEAR;
 EPwm2Regs.AQCTLA.bit.CBD = AQ_CLEAR;
 EPwm2Regs.AQCTLB.bit.CAU = AQ_SET;
 EPwm2Regs.AQCTLB.bit.CBU = AQ_SET;
 EPwm2Regs.AQCTLB.bit.CBD = AQ_CLEAR;
 EPwm2Regs.AQCTLB.bit.CAD = AQ_CLEAR;}
else if(k2 < 396)
{i2=k2-264;
        EPwm2Regs.CMPA.half.CMPA=RefVal[i2]*MM[k4];
        EPwm2Regs.CMPB=EPwm2Regs.CMPA.half.CMPA;
        EPwm2Regs.AQCTLA.bit.CAU = AQ_CLEAR;
        EPwm2Regs.AQCTLA.bit.CBU = AQ_CLEAR;
        EPwm2Regs.AQCTLA.bit.CAD = AQ_SET;
        EPwm2Regs.AQCTLA.bit.CBD = AQ_SET;
        EPwm2Regs.AQCTLB.bit.CAU = AQ_CLEAR;
        EPwm2Regs.AQCTLB.bit.CBU = AQ_CLEAR;
        EPwm2Regs.AQCTLB.bit.CAD = AQ_CLEAR;
        EPwm2Regs.AQCTLB.bit.CBD = AQ_CLEAR;}
else if (k2 == 396)
{EPwm2Regs.CMPA.half.CMPA = RefVal[0]*MM[k4];
        EPwm2Regs.CMPB = Amp-(RefVal1[0]*MM[k4]);
 EPwm2Regs.AQCTLA.bit.CAU = AQ_SET;
 EPwm2Regs.AQCTLA.bit.CBU = AQ_SET;
 EPwm2Regs.AQCTLB.bit.CAU = AQ_CLEAR;    //Change
 EPwm2Regs.AQCTLB.bit.CBU = AQ_CLEAR;}
  else if(k2 < 528)
{i2=k2-396;
 EPwm2Regs.CMPA.half.CMPA=RefVal[i2]*MM[k4];
 EPwm2Regs.CMPB=Amp-(RefVal1[i2]*MM[k4]);
 EPwm2Regs.AQCTLA.bit.CAU = AQ_SET;
 EPwm2Regs.AQCTLA.bit.CAD = AQ_SET;
 EPwm2Regs.AQCTLA.bit.CBU = AQ_SET;
 EPwm2Regs.AQCTLA.bit.CBD = AQ_SET;
 EPwm2Regs.AQCTLB.bit.CAU = AQ_CLEAR;     //Change
 EPwm2Regs.AQCTLB.bit.CAD = AQ_CLEAR;
 EPwm2Regs.AQCTLB.bit.CBU = AQ_CLEAR;
 EPwm2Regs.AQCTLB.bit.CBD = AQ_CLEAR;}    //Change
        else if (k2 == 528)
{EPwm2Regs.CMPA.half.CMPA = Amp-(RefVal1[0]*MM[k4]);
        EPwm2Regs.CMPB = 0;
        EPwm2Regs.AQCTLA.bit.CAU = AQ_SET;
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        EPwm2Regs.AQCTLA.bit.CBU = AQ_CLEAR;
    EPwm2Regs.AQCTLB.bit.CAU = AQ_CLEAR;
        EPwm2Regs.AQCTLB.bit.CBU = AQ_CLEAR;}
  else if (k2 < 660)
  {i2= k2-528;
        EPwm2Regs.CMPA.half.CMPA=Amp-(RefVal1[i2]*MM[k4]);
        EPwm2Regs.CMPB=EPwm2Regs.CMPA.half.CMPA;
    EPwm2Regs.AQCTLA.bit.CAU = AQ_SET;
        EPwm2Regs.AQCTLA.bit.CBU = AQ_SET;
        EPwm2Regs.AQCTLA.bit.CBD = AQ_CLEAR;
        EPwm2Regs.AQCTLA.bit.CAD = AQ_CLEAR;
        EPwm2Regs.AQCTLB.bit.CAU = AQ_CLEAR;
        EPwm2Regs.AQCTLB.bit.CBU = AQ_CLEAR;
        EPwm2Regs.AQCTLB.bit.CBD = AQ_CLEAR;
        EPwm2Regs.AQCTLB.bit.CAD = AQ_CLEAR;}
  else
  {i2= k2-660;
        EPwm2Regs.CMPA.half.CMPA=RefVal[i2]*MM[k4];
        EPwm2Regs.CMPB=EPwm2Regs.CMPA.half.CMPA;
        EPwm2Regs.AQCTLA.bit.CAU = AQ_CLEAR;          // Set PWM1A on event A, up count
        EPwm2Regs.AQCTLA.bit.CAD = AQ_CLEAR;
        EPwm2Regs.AQCTLA.bit.CBU = AQ_CLEAR;          // Set PWM1A on event A, up count
        EPwm2Regs.AQCTLA.bit.CBD = AQ_CLEAR;
        EPwm2Regs.AQCTLB.bit.CAU = AQ_CLEAR;
        EPwm2Regs.AQCTLB.bit.CBU = AQ_CLEAR;
        EPwm2Regs.AQCTLB.bit.CAD = AQ_SET;
    EPwm2Regs.AQCTLB.bit.CBD = AQ_SET;
        EALLOW;
        SysCtrlRegs.WDKEY=0xAA;
        EDIS;
  }
    return;
 }
void update_compare3(EPWM_INFO *epwm_info)
{   // Every event, change the CMPA/CMPB values
  if (k3 == 0)
  {EPwm3Regs.CMPA.half.CMPA = Amp-(RefVal1[0]*MM[k4]);
        EPwm3Regs.CMPB = 0;
        EPwm3Regs.AQCTLA.bit.CAU = AQ_SET;
        EPwm3Regs.AQCTLA.bit.CBU = AQ_CLEAR;
        EPwm3Regs.AQCTLB.bit.CAU = AQ_CLEAR;
        EPwm3Regs.AQCTLB.bit.CBU = AQ_CLEAR;}
  else if (k3 < 132)
  {EPwm3Regs.CMPA.half.CMPA=Amp-(RefVal1[k3]*MM[k4]);
        EPwm3Regs.CMPB=EPwm3Regs.CMPA.half.CMPA;
        EPwm3Regs.AQCTLA.bit.CAU = AQ_SET;
        EPwm3Regs.AQCTLA.bit.CBU = AQ_SET;
        EPwm3Regs.AQCTLA.bit.CAD = AQ_CLEAR;
        EPwm3Regs.AQCTLA.bit.CBD = AQ_CLEAR;
        EPwm3Regs.AQCTLB.bit.CAU = AQ_CLEAR;
        EPwm3Regs.AQCTLB.bit.CBU = AQ_CLEAR;
        EPwm3Regs.AQCTLB.bit.CAD = AQ_CLEAR;
        EPwm3Regs.AQCTLB.bit.CBD = AQ_CLEAR;}
  else if(k3 < 264)
  {i3= k3-132;
    EPwm3Regs.CMPA.half.CMPA=RefVal[i3]*MM[k4];
        EPwm3Regs.CMPB=EPwm3Regs.CMPA.half.CMPA;
    EPwm3Regs.AQCTLA.bit.CAU = AQ_CLEAR;
        EPwm3Regs.AQCTLA.bit.CBU = AQ_CLEAR;
        EPwm3Regs.AQCTLA.bit.CAD = AQ_CLEAR;
        EPwm3Regs.AQCTLA.bit.CBD = AQ_CLEAR;
        EPwm3Regs.AQCTLB.bit.CAU = AQ_CLEAR;
        EPwm3Regs.AQCTLB.bit.CBU = AQ_CLEAR;
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 EPwm3Regs.AQCTLB.bit.CAD = AQ_SET;
 EPwm3Regs.AQCTLB.bit.CBD = AQ_SET;}
        else if(k3 == 264)
{EPwm3Regs.CMPA.half.CMPA = RefVal[0]*MM[k4];
        EPwm3Regs.CMPB = Amp-(RefVal1[0]*MM[k4]);
        EPwm3Regs.AQCTLA.bit.CAU = AQ_CLEAR;     //Change
        EPwm3Regs.AQCTLA.bit.CBU = AQ_CLEAR;
 EPwm3Regs.AQCTLB.bit.CAU = AQ_SET;
        EPwm3Regs.AQCTLB.bit.CBU = AQ_SET;}
        else if(k3 < 396)
        {i3=k3-264;
        EPwm3Regs.CMPA.half.CMPA=RefVal[i3]*MM[k4];
        EPwm3Regs.CMPB=Amp-(RefVal1[i3]*MM[k4]);
        EPwm3Regs.AQCTLA.bit.CAU = AQ_CLEAR;    //Change
        EPwm3Regs.AQCTLA.bit.CAD = AQ_CLEAR;
        EPwm3Regs.AQCTLA.bit.CBU = AQ_CLEAR;
 EPwm3Regs.AQCTLA.bit.CBD = AQ_CLEAR;     //Change
 EPwm3Regs.AQCTLB.bit.CAU = AQ_SET;
        EPwm3Regs.AQCTLB.bit.CAD = AQ_SET;
        EPwm3Regs.AQCTLB.bit.CBU = AQ_SET;
 EPwm3Regs.AQCTLB.bit.CBD = AQ_SET;}
else if(k3 == 396)
{EPwm3Regs.CMPA.half.CMPA = Amp-(RefVal1[0]*MM[k4]);
        EPwm3Regs.CMPB = 0;
        EPwm3Regs.AQCTLA.bit.CAU = AQ_CLEAR;
        EPwm3Regs.AQCTLA.bit.CBU = AQ_CLEAR;
        EPwm3Regs.AQCTLB.bit.CAU = AQ_SET;
        EPwm3Regs.AQCTLB.bit.CBU = AQ_CLEAR;}
        else if(k3 < 528)
{i3=k3-396;
 EPwm3Regs.CMPA.half.CMPA=Amp-(RefVal1[i3]*MM[k4]);
        EPwm3Regs.CMPB=EPwm3Regs.CMPA.half.CMPA;
        EPwm3Regs.AQCTLA.bit.CAU = AQ_CLEAR;
 EPwm3Regs.AQCTLA.bit.CAD = AQ_CLEAR;
 EPwm3Regs.AQCTLA.bit.CBU = AQ_CLEAR;
 EPwm3Regs.AQCTLA.bit.CBD = AQ_CLEAR;
 EPwm3Regs.AQCTLB.bit.CAU = AQ_SET;
 EPwm3Regs.AQCTLB.bit.CAD = AQ_CLEAR;
 EPwm3Regs.AQCTLB.bit.CBU = AQ_SET;
 EPwm3Regs.AQCTLB.bit.CBD = AQ_CLEAR;}
        else if(k3 < 660)
{i3=k3-528;
 EPwm3Regs.CMPA.half.CMPA=RefVal[i3]*MM[k4];
        EPwm3Regs.CMPB=EPwm3Regs.CMPA.half.CMPA;
        EPwm3Regs.AQCTLA.bit.CAU = AQ_CLEAR;
 EPwm3Regs.AQCTLA.bit.CAD = AQ_SET;
 EPwm3Regs.AQCTLA.bit.CBU = AQ_CLEAR;
 EPwm3Regs.AQCTLA.bit.CBD = AQ_SET;
 EPwm3Regs.AQCTLB.bit.CAU = AQ_CLEAR;
 EPwm3Regs.AQCTLB.bit.CAD = AQ_CLEAR;
 EPwm3Regs.AQCTLB.bit.CBU = AQ_CLEAR;
 EPwm3Regs.AQCTLB.bit.CBD = AQ_CLEAR;}
else if (k3 == 660)
{EPwm3Regs.CMPA.half.CMPA = RefVal[0]*MM[k4];
        EPwm3Regs.CMPB = Amp-(RefVal1[0]*(M));
        EPwm3Regs.AQCTLA.bit.CAU = AQ_SET;
        EPwm3Regs.AQCTLA.bit.CBU = AQ_SET;
 EPwm3Regs.AQCTLB.bit.CAU = AQ_CLEAR;     //Change
        EPwm3Regs.AQCTLB.bit.CBU = AQ_CLEAR;}
else
        {i3= k3-660;
        EPwm3Regs.CMPA.half.CMPA=RefVal[i3]*MM[k4];
        EPwm3Regs.CMPB=Amp-(RefVal1[i3]*MM[k4]);
```

```
            EPwm3Regs.AQCTLA.bit.CAU = AQ_SET;
            EPwm3Regs.AQCTLA.bit.CAD = AQ_SET;
            EPwm3Regs.AQCTLA.bit.CBU = AQ_SET;
            EPwm3Regs.AQCTLA.bit.CBD = AQ_SET;
            EPwm3Regs.AQCTLB.bit.CAU = AQ_CLEAR;    //Change
   EPwm3Regs.AQCTLB.bit.CAD = AQ_CLEAR;
            EPwm3Regs.AQCTLB.bit.CBU = AQ_CLEAR;
            EPwm3Regs.AQCTLB.bit.CBD = AQ_CLEAR;     //Change
            EALLOW;
            SysCtrlRegs.WDKEY=0xAA;
            EDIS;
  }
    return;
 }
 void update_compare4(EPWM_INFO *epwm_info)
{  // Every event, change the CMPA/CMPB values
            if (k4 < N1)
  {EPwm4Regs.CMPA.half.CMPA=sum2[k4]*303;
            EPwm4Regs.CMPB=MI1*303;
            EPwm4Regs.AQCTLA.bit.CBU = AQ_NO_ACTION;
            EPwm4Regs.AQCTLA.bit.CAU = AQ_CLEAR;
            EPwm4Regs.AQCTLA.bit.CAD = AQ_SET;
            EPwm4Regs.AQCTLA.bit.CBD = AQ_NO_ACTION;
            EPwm4Regs.AQCTLB.bit.CAU = AQ_NO_ACTION;
            EPwm4Regs.AQCTLB.bit.CBU = AQ_CLEAR;
            EPwm4Regs.AQCTLB.bit.CAD = AQ_NO_ACTION;
            EPwm4Regs.AQCTLB.bit.CBD = AQ_SET;
// else
//   {EPwm4Regs.CMPA.half.CMPA=0;
//            EPwm4Regs.CMPB=EPwm4Regs.CMPA.half.CMPA;
//            EPwm4Regs.AQCTLA.bit.CAU = AQ_CLEAR;           // Set PWM1A on event A, up count
//            EPwm4Regs.AQCTLA.bit.CAD = AQ_CLEAR;
//            EPwm4Regs.AQCTLA.bit.CBU = AQ_CLEAR;           // Set PWM1A on event A, up count
//            EPwm4Regs.AQCTLA.bit.CBD = AQ_CLEAR;
//            EPwm4Regs.AQCTLB.bit.CAU = AQ_CLEAR;
//            EPwm4Regs.AQCTLB.bit.CBU = AQ_CLEAR;
//            EPwm4Regs.AQCTLB.bit.CAD = AQ_CLEAR;
//    EPwm4Regs.AQCTLB.bit.CBD = AQ_CLEAR;
            EALLOW;
            SysCtrlRegs.WDKEY=0xAA;
            EDIS;}
    return;
}
//===========================================================================
=
// No more.
//===========================================================================
=
```

APPENDIX D

Design of a Cascaded PID Controller

The PID's transfer function, C(s)

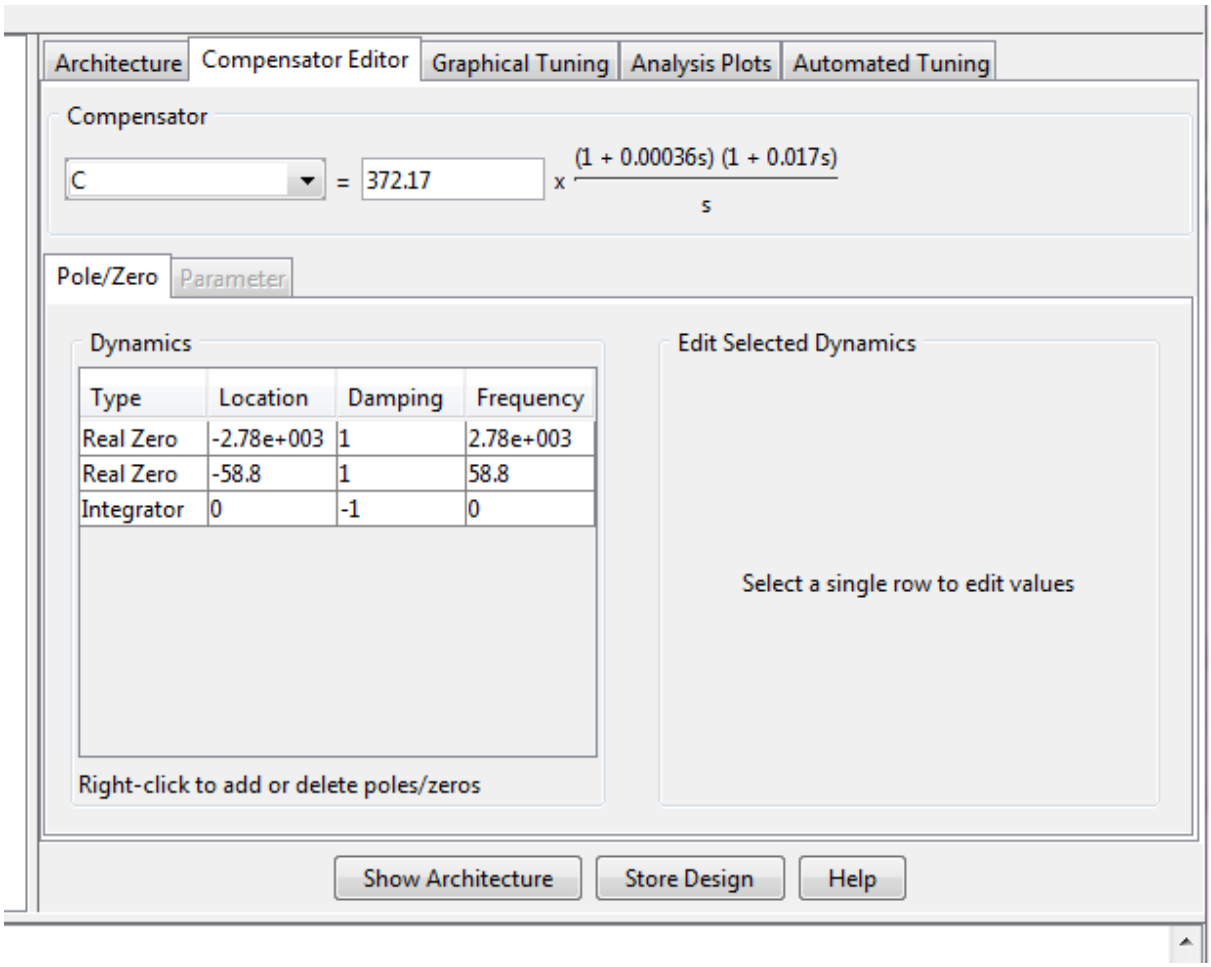

Figure D.1: The PID's transfer function, C(s)

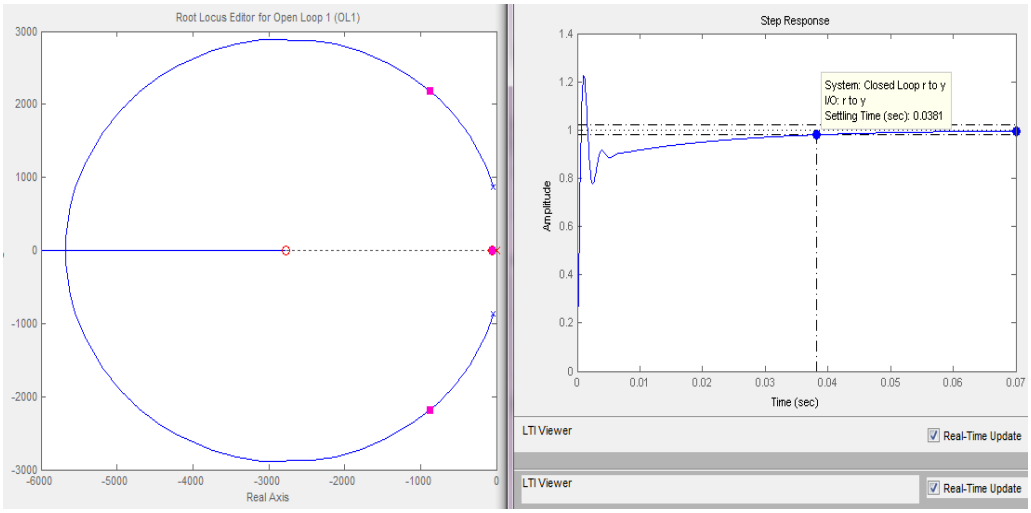

Figure D.2: The root locus of the closed loop system and its step response

```
Transfer function:
   1726 s^2 + 4.895e006 s + 2.82e008
-------------------------------------
s^3 + 1809 s^2 + 5.652e006 s + 2.82e008
```

Figure D.3: The closed-loop transfer function, T(s)

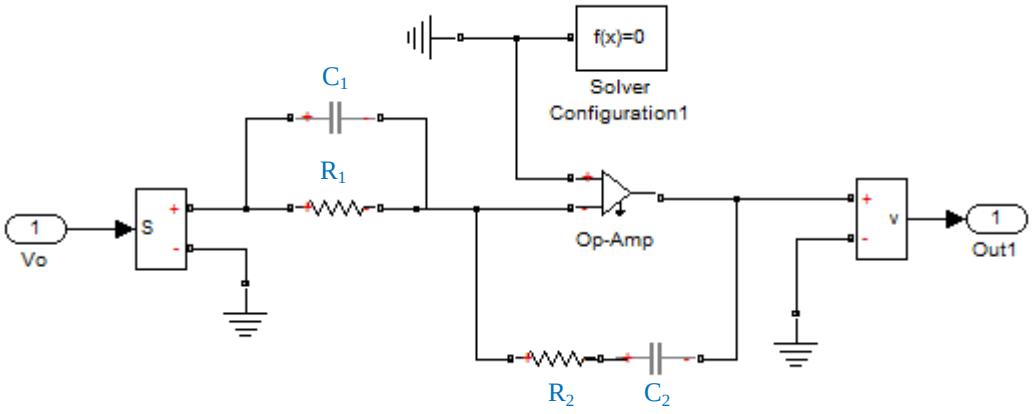

Figure D.4: Analog PID controller using active-circuit realization

$$C = -\left[\left(\frac{R_2}{R_1} + \frac{C_1}{C_2}\right) + R_2 C_1 s + \frac{\frac{1}{R_1 C_2}}{s}\right] = K_P + \frac{K_I}{s} + K_D s$$

$$K_P = \left(\frac{R_2}{R_1} + \frac{C_1}{C_2}\right) = 6.461; \qquad K_I = \frac{1}{R_1 C_2} = 372.2; \qquad K_D = R_2 C_1 = 2.278 \times 10^{-3}$$

Selecting $C_2 = 0.1\mu F$, the remaining values are found to be:

$R_1 = 26.867$ KΩ, $R_2 = 170$ KΩ and $C_1 = 0.0134\mu F$

APPENDIX E

Partial Fraction Expansion Method

To determine the output response in time domain through dominant poles location using Partial Fraction Expansion Method:

Poles: -408, -139

$$c(s) = \frac{1}{s(s+408)(s+139)}$$

$$c(s) = \frac{1}{s(s+408)(s+139)} = \frac{A}{s} + \frac{B}{(s+408)} + \frac{C}{(s+139)}$$

To solve the value of A, B and C:

Using partial method, we get:

$$A = \left.\frac{56712}{(s+408)(s+139)}\right|_{s=0} = \frac{56712}{56712} = 1$$

$$B = \left.\frac{56712}{s(s+139)}\right|_{s=-408} = \frac{56712}{109752} = 0.5167$$

$$C = \left.\frac{56712}{s(s+408)}\right|_{s=-139} = \frac{56712}{-37391} = -1.5167$$

Taking inverse Laplace to obtain time response, c(t), to a unit step input, we obtain:

$$c(s) = \frac{1}{s} + \frac{0.5167}{(s+408)} + \frac{-1.5167}{(s+139)}$$

$$c(t) = 1 + 0.5167e^{-408t} - 1.5167e^{-139t}$$