CHAPTER 1

INTRODUCTION

1.1 Background

Today, the human population has passed 7 billion. The great expansion of the human population has threatened the environment. Global warming, air pollution, acid precipitation and ozone depletion are the serious issues arise. Besides, the finite reserve of traditional energy resources such as coal, fossil fuel and natural gas has raised urgent concern to look for alternative energy resources. To overcome these problems, renewable energy resources such as wind energy, biomass energy, solar energy and geothermal energy are considered the best option because they are naturally available, pollution free and inexhaustible(Rahim, Chaniago, & Selvaraj, 2011; Selvaraj & Rahim, 2009).

Among the renewable energy, solar energy has recently experienced an exponential growth all over the world. The electricity is simply generated by converting the solar irradiance into the electricity via the solar cells. Unlike the dynamic wind turbine, the photovoltaic (PV) installation is static. It does not require strong tall towers and produces no vibration and noise. On the other hand, the advancement of the power electronics industry and the in-depth research further encourage the PV applications. The development of the power semiconductor devices such as Isolated Gate Bipolar Transistor (IGBT) and power MOSFET makes the high-efficiency PV systems possible (Calais, Myrzik, Spooner, & Agelidis, 2002; Petrone, Spagnuolo, Teodorescu, Veerachary, & Vitelli, 2008).

Parasitic capacitance is formed when the solar panel is grounded. The magnitude of the parasitic capacitance depends on the surface of PV arrays and the grounded frame,

distance of PV cell to the module, atmospheric conditions, dust and humidity (Kerekes, Teodorescu, & Borup, 2007). Leakage current is generated when the voltage charges and discharges the parasitic capacitance. This voltage is also known as common-mode voltage (CMV). The CMV is very much dependent of the inverter topology as well as the modulation technique.

An inverter is used to convert DC power generated from the solar modules into AC power. This inverter, also known as PV inverter, is the heart of a PV system since it is an important element in converting energy from one form to another. Generally, grid-connected PV inverters can be classified into two categories, i.e., with and without transformer (Araujo, Zacharias, & Mallwitz, 2010; Jia-Min, Jou, & Jinn-Chang, 2012; Lopez, Teodorescu, Freijedo, & Doval-Gandoy, 2007). Traditionally, the PV inverters are designed with transformers. In order to step up the input voltage, either high-frequency transformers or bulky low-frequency transformers are used in the dc- or ac-side of the inverters respectively. Besides, the low-power input and the high power output of the PV inverters are completely isolated by the transformers. It isolates the PV modules from the grid. Thus, leakage current has no path to flow. Such galvanic isolation is important to guarantee the safety of the users. Nevertheless, the transformer adds burden to the cost, weight, size and the efficiency of the entire PV inverters.

Therefore, transformerless grid-connected PV inverters are introduced recently. The PV inverters become smaller, lighter, cheaper and highly efficient (Alajmi, Ahmed, Adam, & Williams, 2013; Kerekes, Teodorescu, Klumpner, et al., 2007; Yunjie et al., 2013). However, safety issue is the main concern for the transformerless PV inverters The CMV charges and discharges the parasitic capacitance, generating high leakage current. Without galvanic isolation, a direct path can be formed for the leakage current to flow between the PV modules and the grid. Besides safety issue, this leakage current increases grid current ripples, system losses and electromagnetic interference

(Koutroulis & Blaabjerg, 2013; Li, Kai, Lanlan, Hongfei, & Yan, 2013; Meneses et al., 2013).

Therefore, many research works have been done to design a transformerless PV with reduced leakage current to comply with the German VDE-0126-1-1 standard. The standard limits the leakage current below 300 mA, or the PV systems should be disconnected within 0.3s. For single-phase PV inverters, either dc- or ac-decoupling methods have been proposed to reduce the leakage current. These methods employ additional switches or diodes in dc- or ac-side of the PV inverter to provide galvanic isolation. For three-phase PV inverters, modulation techniques have been designed to reduce the CMV to reduce the leakage current.

In order to study the common-mode behavior of the transformerless PV systems, a common-mode model circuit is used. This common-mode model includes the parasitic parameters of the transformerless PV systems such as parasitic capacitance, ground resistance, the filter inductance and etc. It is found that common-mode voltage (CMV) is the key for leakage current reduction. Based on the analysis, two types of transformerless PV inverters, i.e., single-phase and three-phase inverters, are proposed to reduce the CMV in order to reduce the leakage current to meet the requirement of the standard.

For single-phase PV systems, a high-efficiency transformerless PV inverter is proposed to eliminate the leakage current. A fast-recovery diode is added to the existing HBZVR topology structure to improve the clamping branch performance. With the improved clamping branch of the proposed topology, the CMV is completely eliminated and the leakage current is significantly reduced to the half of the existing HBZVR topology.

On the other hand, a three-phase transformerless H7 inverter, adapted from the single-phase H5 topology, is investigated. An additional switch is added to the

conventional full-bridge structure to disconnect the PV arrays from the grid during the freewheeling period. Leakage current is reduced due to galvanic isolation. In addition, a novel modulation technique is proposed here based on the conventional discontinuous pulsewidth modulation (DPWM). Besides CMV and leakage current reduction, the proposed modulation technique generates three-level unipolar output voltage, i.e., $+V_{DC}$, 0, $-V_{DC}$, which reduces the voltage stress and losses across the filter inductors.

The validity of both proposed topologies are verified through simulations and laboratory prototypes. The PWM algorithms and the control schemes are implemented in DSP TMS320F28335. The overall performance of the proposed topologies, in terms of CMV, leakage current, total harmonic distortion (THD) and efficiency, are compared with various recently proposed transformerless PV inverters.

1.2 Universal Inverter Prototype

Figure 1.1 shows the single-phase universal inverter configuration. S_1–S_4 are the switches of conventional full-bridge inverter. “DC-bypass 1”, “DC-bypass 2” and “AC-bypass” are the dc- or ac-decoupling branch respectively which plays a role as galvanic isolator by disconnecting the PV modules from the grid during the freewheeling period. “Clamping Branch” is the key to ensure the CMV is completely clamped to the constant. The modulation techniques and the control algorithms are implemented in DSP TMS320F28335. All the components with the corresponding parameters are listed in Table 1.1.

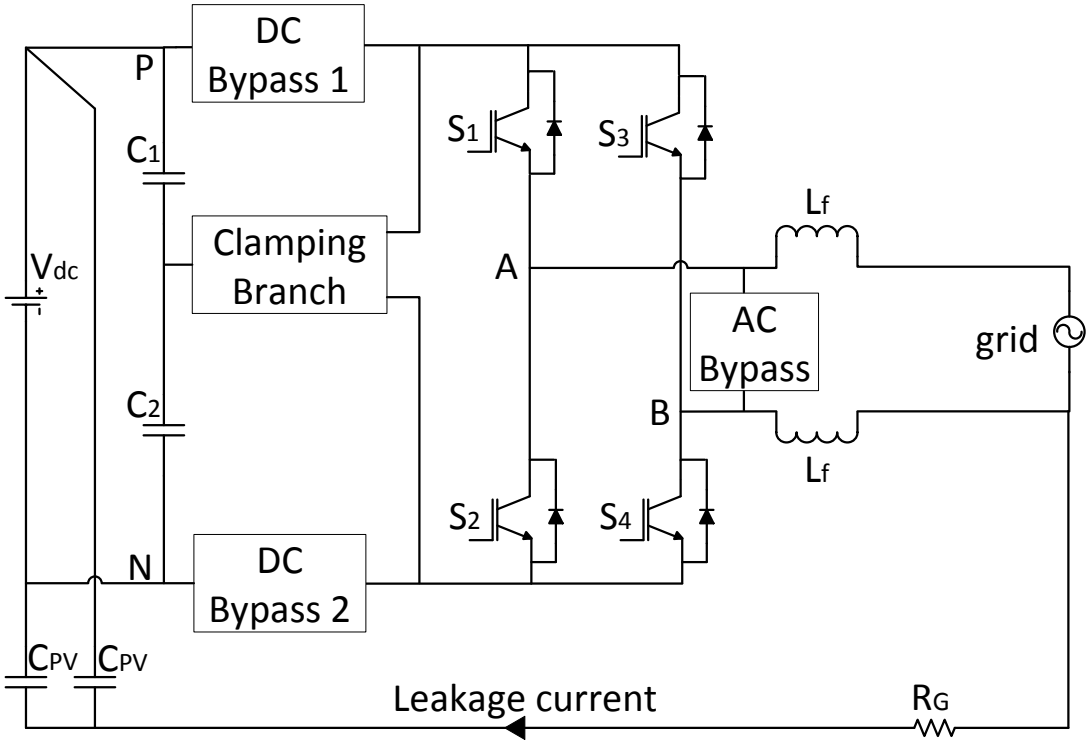


Figure 1.1: Single-phase universal transformerless topologies.

Table 1.1: Universal single-phase transformerless prototype and parameters

Stray capacitors, C_{PV}	100 nF, V_{DC}=1000V (Ceramic)
Ground resistors, R_G	11 Ω
DC-link capacitors, C_1 and C_2	1000 uF, V_{DC}=385V (Aluminum Electrolytic)
Filter inductors, L_f	AC filtering Inductance of 3mH
Switches S_1 - S_4	IGBT GT50J325, V_{CE}=600V I_C=50A.
Diodes	Fast Recovery Diode RHRP30120 V_{RR}=1200V, I=30A
DSP	TMS320F28335
Input voltage	400 V_{DC}
Rated power	1 kW
Switching frequency	10 kHz
Dead time	2.5 us

A three-phase universal inverter configuration is presented in Figure 1.2. S_1–S_6 are the switches of conventional full-bridge inverter. "DC-bypass" is the dc-decoupling branch of H7 inverter. The modulation techniques and the control algorithms are implemented in DSP TMS320F28335. Table 1.2 lists the inverter specifications.

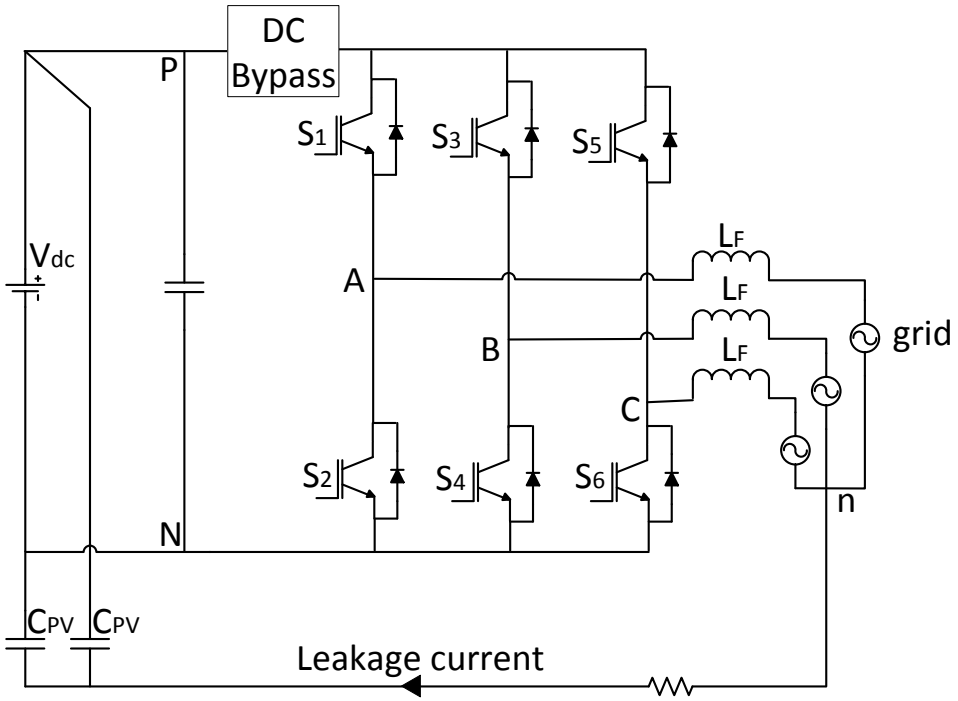


Figure 1.2: Three-phase universal transformerless topologies.

Table 1.2: Universal single-phase transformerless prototype and parameters

Stray capacitors, C_{PV}	100 nF, V_{DC}=1000V (Ceramic)
Ground resistors, R_G	11 Ω
DC-link capacitors, C_1 and C_2	1000 uF, V_{DC}=385V (Aluminum Electrolytic)
Filter inductors, L_f	AC filtering Inductance of 5mH
Switches S_1 - S_4	IGBT GT50J325, V_{CE}=600V I_C=50A.
DSP	TMS320F28335
Input Voltage	600 V_{DC}
Dead time	2.5 us

1.3 62150H Programmable DC Power Supply

The 62150H programmable dc power supply is optimized for maximum power-point tracking (MPPT) and PV inverter testing. It provides a simulation of real PV array performance which takes into consideration of irradiation, temperature and partial shading. The simulator offers open-circuit voltage (V_{oc}) up to 1000V and short-circuit current (I_{sc}) up to 25A for PV array simulation. The 62150H programmable dc power supply is capable of simulating the I-V curve from the early morning to nightfall for PV inverter testing or dynamic I-V curve transient testing. The V_{oc}, I_{sc}, V_{mp}, and I_{mp} parameters for I-V curve simulation can be programmed easily. The key features include:

- Voltage range : 0 ~1000V
- Simulation of multiple solar cell material's I-V characteristic (fill factor)
- Simulation of dynamic irradiation intensity and temperature level from clear day to cloud cover conditions
- Shadowed I-V curve output simulation (up to 4096 data points)
- Static & dynamic MPPT efficiency test (accumulated energy methods)
- Real time analysis of PV inverter's MPPT tracking via softpanel
- Real world weather simulation fast I-V curve update rate : 1s

1.4 TMS 320F28335 DSP

The TMS320F28335 DSP is a super-fast computer chip, optimized for detection, processing, and generation of real signals. It is a 32-bit floating point device, which utilizes less memory and computation time for mathematical operation. This feature is very suitable for the use of PWM generation algorithm which often includes complex mathematical calculation. On the other hand, the implementation of some complex

modulation techniques which requires the simultaneous use of two different triangular carriers (up-down and down-up triangular carriers) is made possible with the enhanced PWM (EPWM) module of TMS320F28335 DSP.

The eZdspTM F28335 is a stand-alone card used to examine whether the TMS320F28335 DSP met application requirements. The module is an excellent platform to develop and to run software for the TMS320F28335 processor. The eZdspTM is shipped with a TMS320F28335 DSP which is a highly integrated high performance solution for demanding control applications such as PV inverters. The eZdspTM F28335 features:

- TMS320F28335 floating-point digital signal controller
- 150 MHz operation
- 68kB on-chip RAM
- 512kB on-chip flash memory
- 30 MHz clock
- expansion connectors (analog, I/O)
- 12-bit ADC with 16 input channels

1.5 VDE 0126-1-1 Standard

The German VDE0126-1-1 standard is a comprehensive standard which covers transformerless PV inverter. According to the standard, a residual current monitoring unit (RCMU) is required to continuously monitor the leakage current. The RCMU employs current sensors to measure the leakage current. The RCMU has to be triggered within 0.3s to disconnect the PV array from the grid if the leakage current exceeds 300 mA. In other words, the VDE0126-1-1 standard limits the leakage current below 300 mA for transformerless PV inverters.

1.6 Research Objectives

The objectives of this work are:

- To design and develop a single-phase transformerless PV inverter to reduce the leakage current.
- To design and develop a three-phase transformerless PV inverter to reduce the leakage current.
- To compare the common-mode voltage, leakage current, efficiency and THD between the proposed topologies and the others recently proposed topologies.

1.7 Research Methodology

A universal transformerless inverter prototype has been built in the laboratory lab. The PV array is simulated with programmable dc power supply. The stray capacitance (C_{PV}) is modeled with two capacitors, each connected to the PV terminal and the ground. The filter is made up of inductors (L_f). The modulation techniques and the control algorithms are implemented in DSP TMS320F28335.

Analysis are done theoretically and via simulation studies, and further validated with experimental results. The simulation is carried out via Matlab/ Simulink. The loss analysis is simulated via thermal module in PSIM. The experimental work is tested via a 1kW universal inverter.

1.8 Scope of work

The main focus of this work is to reduce the leakage current in transformerless PV inverters to comply with the VDE 0126-1-1 standard. Both single-phase and three-phase PV inverters are covered here. The different inverter topologies, together with their modulation techniques, are first simulated in Matlab/Simulink to confirm their performance, before they are implemented and tested using hardware setup. As mentioned above, the leakage current is generated due to CMV, which is very much influenced by modulation technique and inverter topology. Generally, the utility grid does not influence the common-mode behavior of the PV systems. Even though this increases the impedance of the leakage current path and changes the magnitude of the leakage currents, it does not affect the validity of the comparisons, since the same resistor loads are used in all topologies. Hence for the experiments in this work, resistors load are used in replacement of the grid. The maximum point power tracking (MPPT) and anti-islanding are not covered in the scope of this work. It is worth nothing that the mismatch of the circuit parameters will undoubtedly contribute to leakage current. However, in this work, all the circuit parameters such as filter inductors, stray capacitors and other parasitic parameters are assumed to be matching to one another. In other words, the mismatch of the circuit parameters is beyond the scope of this work.

1.9 Outline

The remainder of this thesis is organized as follow:

Chapter 2 discusses the common-mode behavior for both single-phase and three-phase transformerless PV systems. A common-mode model circuit, includes the parasitic parameters, is derived and simplified stage by stage. The equivalent simplest model is then used to derive the differential-mode voltage and the CMV.

Chapter 3 is a survey of recently proposed topologies for both single-phase and three-phase transformerless PV inverters.

Chapter 4 proposes a single-phase transformerless PV inverter based on the analysis of chapter 2 and 3. It provides an in-depth analysis of the circuit configuration, operation principle and its hardware implementation. The overall performance, in terms of CMV, leakage current, losses, efficiency and THD, is compared with other topologies. Finally, the simulation and experimental results are presented.

Chapter 5 proposes a three-phase transformerless PV inverter based on the analysis of chapter 2 and 3. The H7 conversion structure with the novel modulation technique are proposed. The operation principle of the circuit configuration as well as the software implementation of the proposed modulation technique is presented. The overall performance, in terms of CMV, leakage current, dc-link voltage ripples and THD, is compared with other topologies. The simulation and experimental results are presented.

Chapter 6 summarizes the overall conclusions and recommendations for future works.

CHAPTER 2

COMMON-MODE MODEL: AN OVERVIEW

2.1 Introduction

Transformerless PV inverters are popular nowadays because they are small, cheap and highly efficient. However, when the transformer is removed from the inverter, there is a galvanic connection between the PV arrays and the grid. The galvanic connection forms the leakage current path. When the CMV is generated by the inverter topology with corresponding PWM, the CMV charges and discharges the parasitic capacitance. As a result leakage current is generated, flowing through the leakage current path between the PV arrays and the grid (Bo, Wuhua, Yunjie, Wenfeng, & Xiangning, 2012; Kerekes, Teodorescu, Rodriguez, Vazquez, & Aldabas, 2011).

In order to design a suitable transformerless PV inverter topology with reduced leakage current, the theoretical analysis must first be understood. Therefore, in this chapter, the common-mode behaviors for both single-phase and three-phase transformerless PV systems are investigated. A common-mode model circuit is derived and simplified stage by stage to study the common-mode behavior of the transformerless PV systems. This chapter provides an overview for the researchers to understand the operation principle when the transformer is removed from the PV inverter.

2.2 Common-Mode Model for Single-Phase PV Systems

When the transformer is removed from the inverter, a resonant circuit is formed as shown in Figure 2.1. This resonant circuit includes the parasitic capacitance (C_{PV}), the filter inductors (L_1 and L_2), leakage current (I_L).

Here, the power converter is represented by a block with four terminals to allow a general representation of various converter topologies. On the dc side, P and N are connected to the positive and negative terminal of the dc-link respectively; while on the ac side, terminals A and B are connected to the single-phase grid via filter inductors.

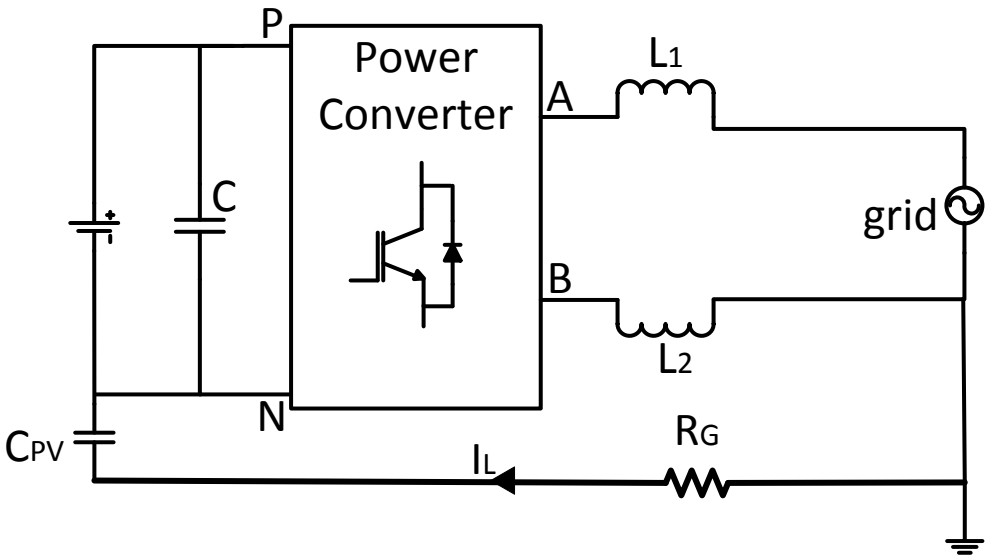


Figure 2.1: Resonant circuit for single-phase transformerless PV inverter.

From the view of point of grid, the power converter block as shown in Figure 2.1 can be considered as voltage sources, generating into equivalent circuit which consists of V_{AN} and V_{BN} (Gubía, Sanchis, Ursúa, López, & Marroyo, 2007; Huafeng & Shaojun, 2010). Obviously, the leakage current is a function of V_{AN}, V_{BN}, grid voltage, filter inductance and parasitic capacitance. Since the grid is a low-frequency voltage source (50 Hz), the impact on the common-mode model will be ignored here. Therefore,

a simplified common-mode is obtained as shown in Figure 2.2 by expressing voltages V_{AN} and V_{BN} as the functions of V_{CM} and V_{DM}.

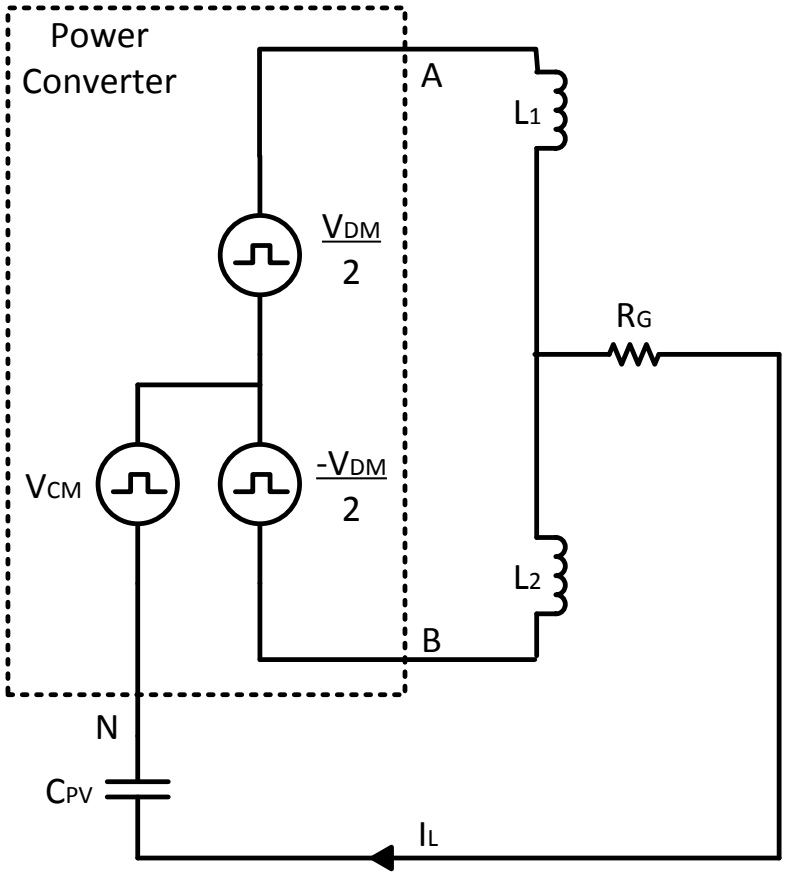


Figure 2.2: Simplified resonant circuit for single-phase transformerless topology.

The CMV V_{CM} and differential-mode voltage V_{DM} can be defined as (Baojian, Jianhua, & Jianfeng, 2013; Bo et al., 2012; R. Gonzalez, Gubia, Lopez, & Marroyo, 2008)

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} \tag{2.1}$$

$$V_{DM} = V_{AN} - V_{BN} \tag{2.2}$$

Rearranging (2.1) and (2.2), the output voltages can be expressed in terms of V_{CM} and V_{DM} as

$$V_{AN} = V_{CM} + \frac{V_{DM}}{2} \tag{2.3}$$

$$V_{BN} = V_{CM} - \frac{V_{DM}}{2} \tag{2.4}$$

Using (2.3) and (2.4) and considering only the common-mode components of the circuit, a simplified common-mode model can be obtained as in Figure 2.3, following the steps in (Gubía, Sanchis, Ursúa, López, & Marroyo, 2007; Huafeng & Shaojun, 2010). The equivalent CMV (V_{ECM}) is defined as

$$V_{ECM} = V_{CM} + \frac{V_{DM}}{2}\frac{L_2 - L_1}{L_1 + L_2} \tag{2.5}$$

Since identical filter inductors (L1=L2) are considered in this work, the V_{ECM} is equal to V_{CM}

$$V_{ECM} = V_{CM} = \frac{V_{AN} + V_{BN}}{2} \tag{2.6}$$

From the common-mode model, it can be concluded that the leakage current is very much dependent of the CMV. Therefore, the converter structure and the modulation technique must be designed to generate constant CMV in order to eliminate the leakage current. It is worth mentioning that the simplest model in Figure 2.3 has been commonly used for describing the common-mode behavior of the conventional

full-bridge (H4) topology. However, due to the generality of the model, it is obvious that the model is valid for other topologies discussed here, apart from H4.

As a matter of fact, the same model has been used to analyze the common-mode behavior of various transformerless converter topologies (Gubía et al., 2007; Huafeng & Shaojun, 2010, 2012; Huafeng, Shaojun, Yang, & Ruhai, 2011). Nevertheless, since different topology has different V_{AN} and V_{BN}, the expression for V_{CM} and V_{DM} will differ from one another, which yield different common-mode behavior. Hence, to evaluate the common-mode behavior of a particular topology, V_{AN} and V_{BN} under different switching condition need to be evaluated, as will be shown later chapter.

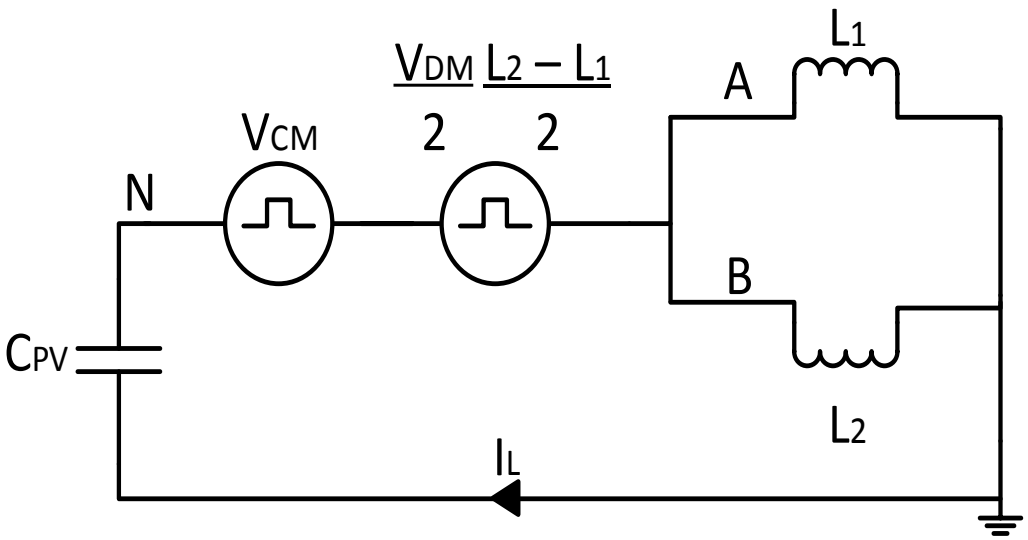


Figure 2.3: Simplest resonant circuit for single-phase transformerless topology.

2.3 Common-Mode Model for Three-Phase PV Systems

The resonant circuit for three-phase transformerless inverter is shown in Figure 2.4. Similar to single-phase system, this resonant circuit includes the stray capacitance (C_{PV}), the filter inductors (L_1, L_2 and L_3), leakage current (I_L). Here, the power converter is represented by a block with four terminals to allow a general representation of various converter topologies.

On the dc side, P and N are connected to the positive and negative terminal of the dc-link respectively; while on the ac side, terminals A, B and C are connected to the three-phase grid via filter inductors.

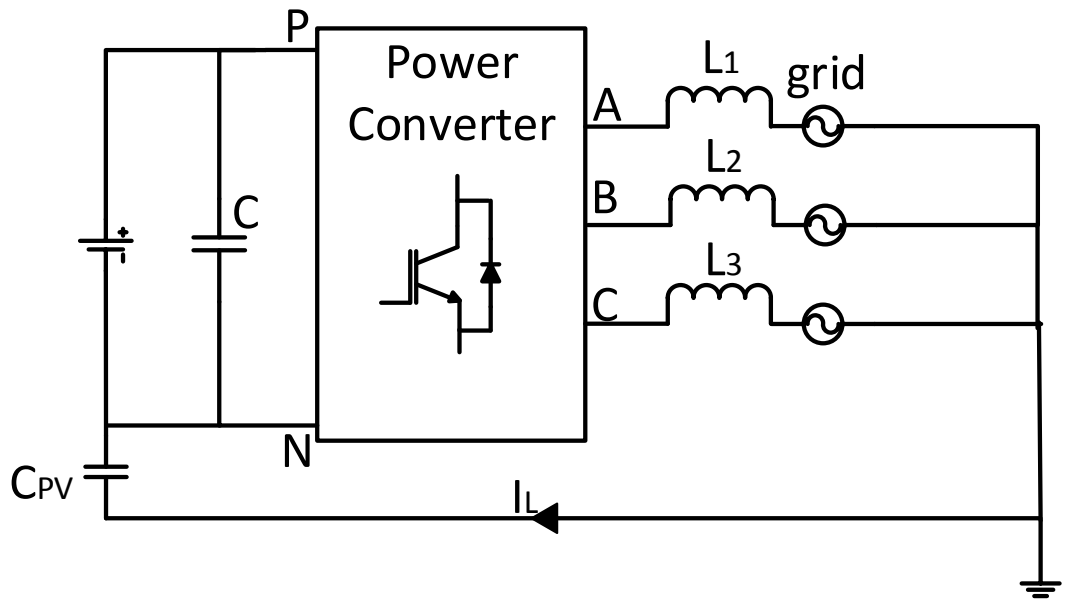


Figure 2.4: Resonant circuit for three-phase transformerless PV inverter.

From the view of point of grid, the power converter block as shown in Figure 2.4 can be considered as voltage sources, generating into equivalent circuit which consists of V_{AN}, V_{BN} and V_{CN} as shown in Figure 2.5 (Cavalcanti et al., 2010; Kerekes, Teodorescu, Klumpner, et al., 2007). The leakage current is thus a function of V_{AN}, V_{BN}, V_{CN}, grid voltage, filter inductance and stray capacitance.

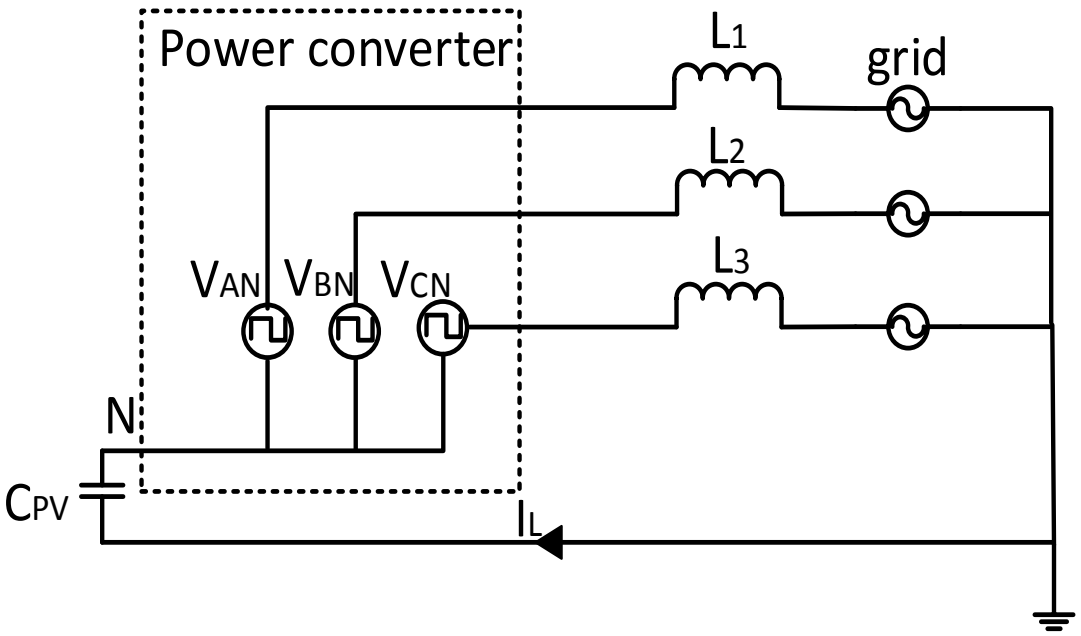


Figure 2.5: Simplified resonant circuit for three-phase transformerless topology.

In order to investigate the common-mode model circuit of the three-phase PV inverter, V_{CM} and V_{DM} are derived between each phase, i.e., phase A and B, phase B and C, and phase C and A. Here, phase A and phase B is considered. Considering identical filter inductors are used ($L_1 = L_2 = L_3$), the common-mode model circuit is the same as the single-phase PV system as shown in Figure 2.1 to Figure 2.3 and likewise for the derivations of V_{CM}, V_{DM}, V_{AN} and V_{BN} as in (2.1)-(2.6).

The same derivation principle above can be applied to other phases (phase B and C, and phase C and A) and the equivalent three-phase common-mode model circuit is

obtained as shown in Figure 2.6. The CMV for three-phase PV system is calculated as (Cavalcanti et al., 2010; Kerekes, Teodorescu, Klumpner, et al., 2007)

$$V_{CM} = \frac{V_{AN} + V_{BN} + V_{CN}}{3} \tag{2.7}$$

From the common-mode model, it can be concluded that the leakage current is very much dependent of the CMV. Therefore, the converter structure and the modulation technique must be designed to generate constant CMV in order to eliminate the leakage current.

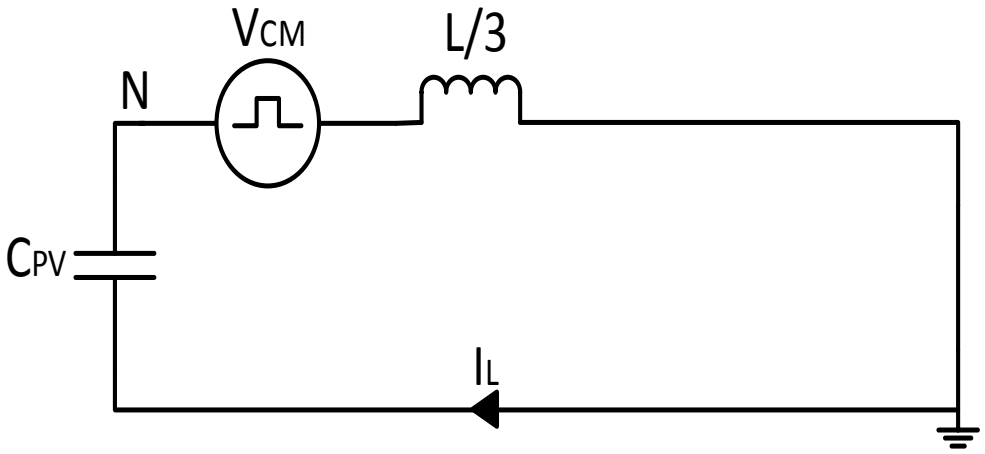


Figure 2.6: Simplest resonant circuit for three-phase transformerless topology.

2.4 Conclusion

The common-mode behaviors of transformerless PV inverter for both single- and three-phase system are investigated in this chapter. A common-mode model circuit is developed according to the resonant circuit. It is then simplified stage by stage and a simplest common-model circuit is obtained. Based on the model, the leakage current is very dependent of CMV. This analytical result is valid for both single- and three-phase transformerless PV inverters.

This chapter provides a rule of thumbs to design a transformerless PV inverter with reduced current. From the common-mode model analysis, it is proven that the CMV contributes to the leakage current flowing between the PV and the grid. In order to eliminate the leakage current, the inverter topology and modulation techniques must be carefully designed to generate constant CMV (Bo et al., 2012; Huafeng & Shaojun, 2010). The inverter topology and modulation techniques will be reviewed in the following chapter.

CHAPTER 3

TRANFORMERLESS PV INVERTERS: AN OVERVIEW

3.1 Introduction

Various transformerless PV inverters topologies are investigated here. This chapter provides a survey of the conventional and recently proposed topologies for both single- and three-phase PV inverters. The circuit configuration, operation principles for various topologies are studied and analyzed.

For single-phase system, the topologies such as full-bridge inverter (Figure 3.1), H5 inverter (Figure 3.4), HERIC inverter (Figure 3.6), H6 inverter (Figure 3.8), oH5 inverter (Figure 3.10) and HBZVR inverter (Figure 3.12) are discussed. The leakage current reduction method via galvanic isolation and CMV clamping is presented. Conventional unipolar and bipolar modulation techniques are included here as well.

For three-phase system, both modulation techniques and inverter structure are investigated. Conventional modulation techniques such as space vector PWM (SVPWM) and discontinuous PWM (DPWM) are first reviewed. The recently proposed modulation techniques include active zero-state PWM (AZPWM), near-state PWM (NSPWM), and remote-state (RSPWM).

3.2 Single-Phase transformerless PV Inverters

Single-phase PV system is usually used for low power and small scale applications such as home users and private sector. The majority of the single-phase system can reach up to 5kW (Kerekes, Teodorescu, Klumpner, et al., 2007).

3.2.1 Full-Bridge Inverter

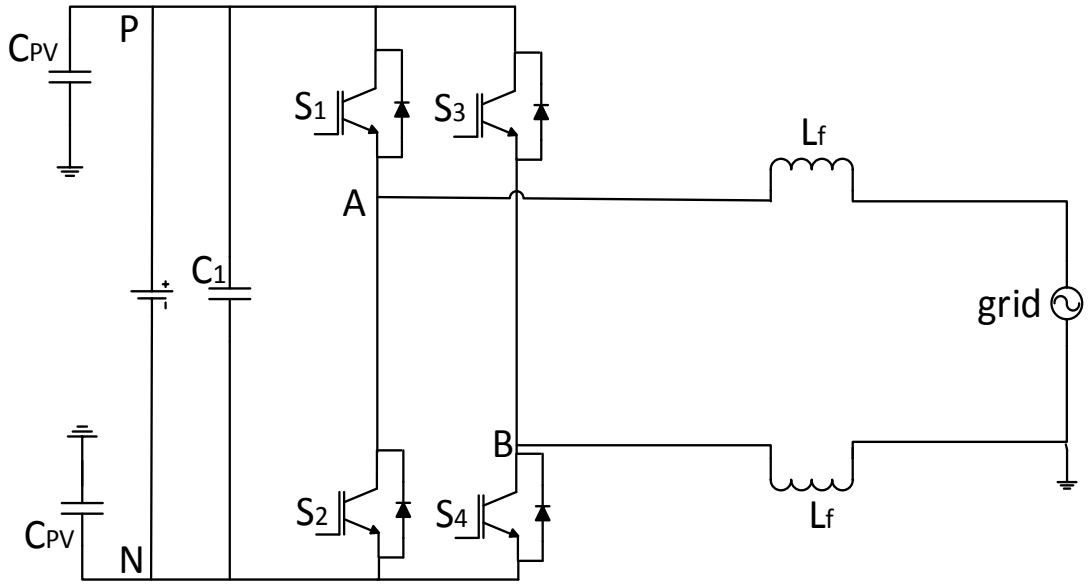


Figure 3.1: Full-bridge inverter.

Full-bridge inverter is widely used for various applications due to the simplicity of design and low cost. It consists of four switches, S_1-S_4, as shown in Figure 3.1. Conventionally, the full-bridge inverter is modulated by unipolar PWM and bipolar PWM.

3.2.1.1 Unipolar PWM

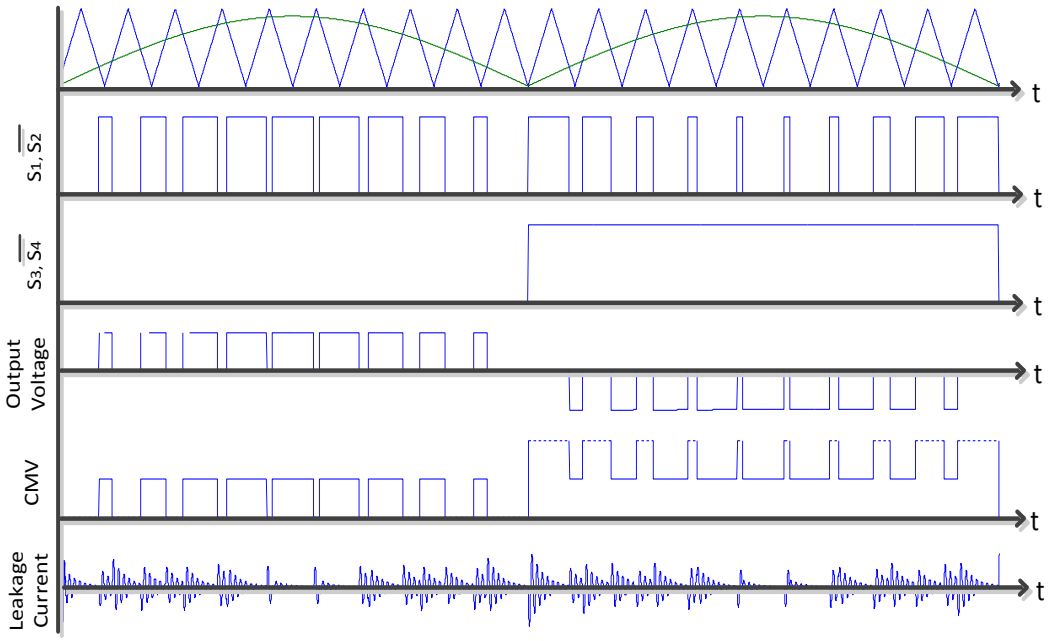


Figure 3.2: Unipolar modulation.

Unipolar PWM is also known as three-level modulation (Rashid et al., 2004; Mohan et al., 2003). As shown in Figure 3.2, it generates three-level output voltage, i.e., $+V_{DC}$, 0, and - V_{DC}. Therefore, the output voltage varies with double switching frequency as compared to that of bipolar PWM. In every switching transition, the voltage changes across the filter inductor by V_{DC} only. As a result, unipolar PWM reduces change of voltage (dv/dt), ripple current, losses and filter size in both switches and filter inductors. High efficiency is achieved with unipolar PWM.

Nevertheless, unipolar PWM is not suitable for transformerless full-bridge inverter application. CMV is generated, varying between 0 and V_{DC} as shown in the figure. The CMV charges and discharges the parasitic capacitance which leads to dangerous leakage current up to few amperes.

3.2.1.2 Bipolar PWM

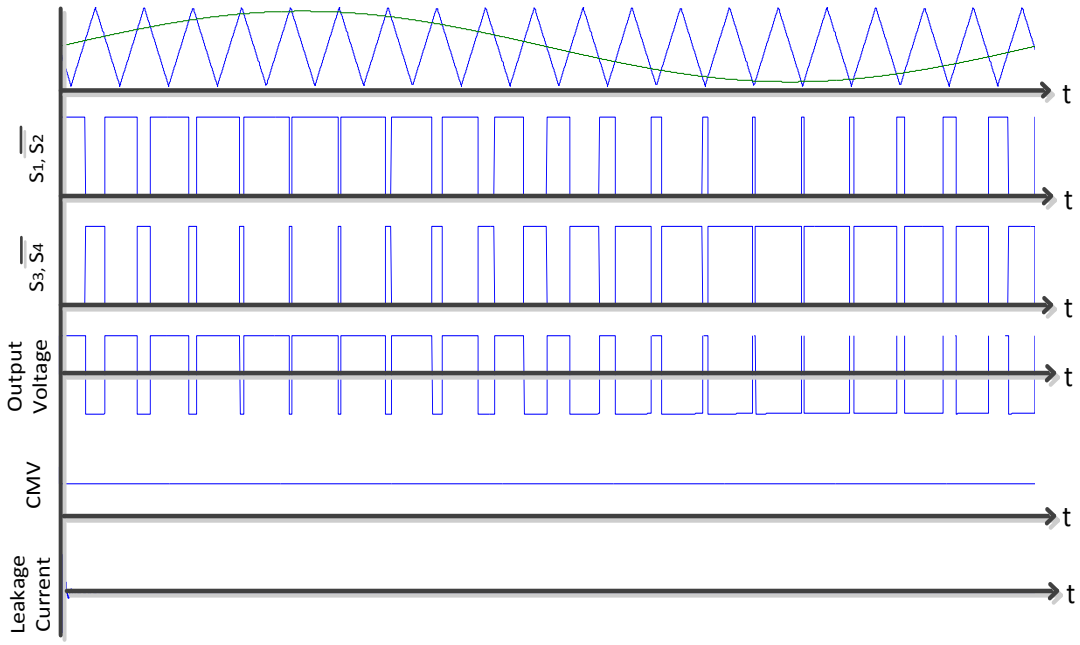


Figure 3.3: Bipolar modulation.

Bipolar PWM, also known as two-level modulation (Rashid et al., 2004; Mohan et al., 2003). As shown in Figure 3.3, it generates two-level output voltage, i.e., $+V_{DC}$, and $-V_{DC}$. In every switching transition, the voltage changes across the inductor by twice of input voltage, 2 V_{DC}. This doubles the voltage stress, current ripples and losses across the filter inductors. As a result, the overall efficiency is reduced. Larger filter inductors are required to compensate the high PWM ripple which leads to higher cost.

Bipolar PWM generates constant CMV, which reduces the leakage current significantly. It is suitable for transformerless PV inverter applications, however, with very poor overall performances (high loss, low efficiency).

3.2.2 Recently Proposed Transformerless Inverter Topologies

In order to combine the advantages of both high-performance unipolar PWM and constant-CMV bipolar PWM, various transformerless PV inverter topologies have been proposed recently such as H5 inverter (Victor, Greizer, Bremicker, & Hübler, 2008), H6 inverter (Roberto Gonzalez, Lopez, Sanchis, & Marroyo, 2007), HERIC inverter (Ketterer, Schmidt, & Siedle, 2003), oH5 inverter (Huafeng & Shaojun, 2010; Huafeng et al., 2011) and HBZVR inverter (Kerekes et al., 2011).

These topologies employ either dc- or ac-decoupling method to provide galvanic isolation. Unipolar PWM is employed to achieve high efficiency. The circuit configuration, modulation techniques and operation principles of these topologies are reviewed in this section.

3.2.2.1 H5 Inverter

H5 inverter (Victor et al., 2008) is patented by SMA. Given that a total of five switches are utilized, this topology is referred to as H5 inverter. A dc-bypass switch, S_5, is added in the input dc-side of the conventional full-bridge inverter structure as shown in Figure 3.4. The introduction of the dc-bypass switch is to provide galvanic isolation, to disconnect the leakage current path during the freewheeling period.

The upper pair of switches S_1 and S_3 is operated at grid frequency while the lower pair of switches S_2 and S_4 is operated at switching frequency. During the conduction period of positive half-cycle, S_1, S_4 and S_5 are ON to generate the desired output voltage. Current flows through S_5, S_1, grid, and S_4. During the freewheeling period of positive half-cycle, S_4 and S_5 are OFF, disconnecting the PV from the grid. Current freewheels through S_1 and the anti-parallel diode of S_3.

On the other hand, S_2, S_3 and S_5 are ON to generate the desired output voltage during the conduction period of negative half-cycle. Current flows through S_5, S_3, grid, and S_2. During the freewheeling period of negative half-cycle, S_2 and S_5 are OFF, disconnecting the PV from the grid. Current freewheels through S_3 and the anti-parallel diode of S_1.

With the galvanic isolation of H5 inverter, leakage current is reduced significantly. Hence, it is suitable for transformerless PV inverter applications. Moreover, high efficiency is achieved with unipolar PWM.

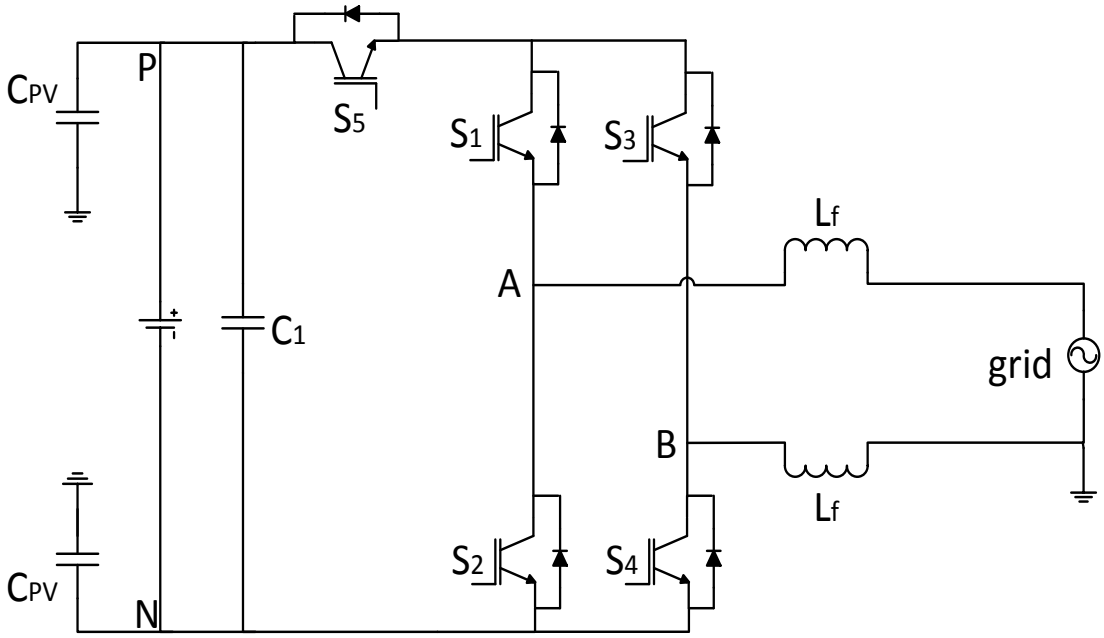


Figure 3.4: H5 inverter.

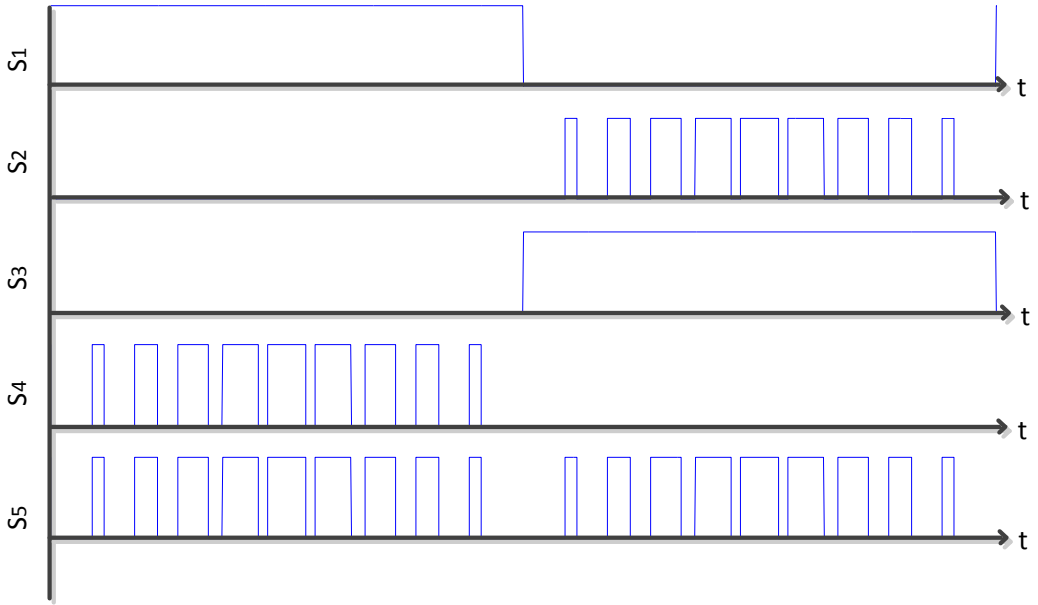


Figure 3.5: Switching pattern for H5 inverter.

3.2.2.2 HERIC Inverter

HERIC inverter (Ketterer, Schmidt, & Siedle, 2003) is known as Highly Efficient and Reliable Inverter Concept. A freewheeling path is added to the output ac-side of conventional full-bridge inverter structure as shown in Figure 3.6. The freewheeling path is made up of two freewheeling switches, i.e., S_5 and S_6.

Each pair of the diagonal switches, i.e., S_1, S_4 and S_2, S_3, is operated simultaneously at switching frequency during the positive and negative half-cycle respectively. Current flows through the corresponding pair of diagonal switches to generate the desired output voltage.

On the other hand, the freewheeling switches, S_5 and S_6, are ON throughout the negative and positive half-cycle respectively. During the freewheeling period of positive half-cycle, current freewheels through S_6, the anti-parallel diode of S_5 and through S_6, the anti-parallel diode of S_5 and the grid during the freewheeling period of negative half-cycle.

Galvanic isolation is provided via the freewheeling path. As a result, leakage current is reduced significantly. Hence, it is suitable for transformerless PV inverter applications. HERIC inverter is well-known with the high-efficiency performance among the proposed topology. This is because the freewheeling switches is operated only at grid frequency, which reduces the switching loss significantly.

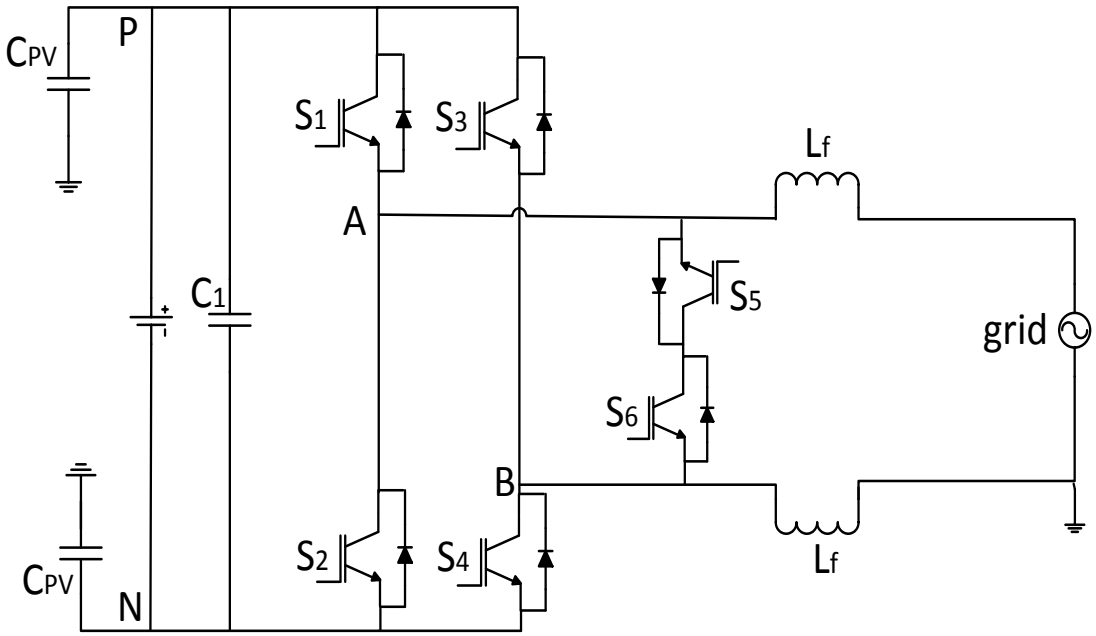


Figure 3.6: HERIC inverter.

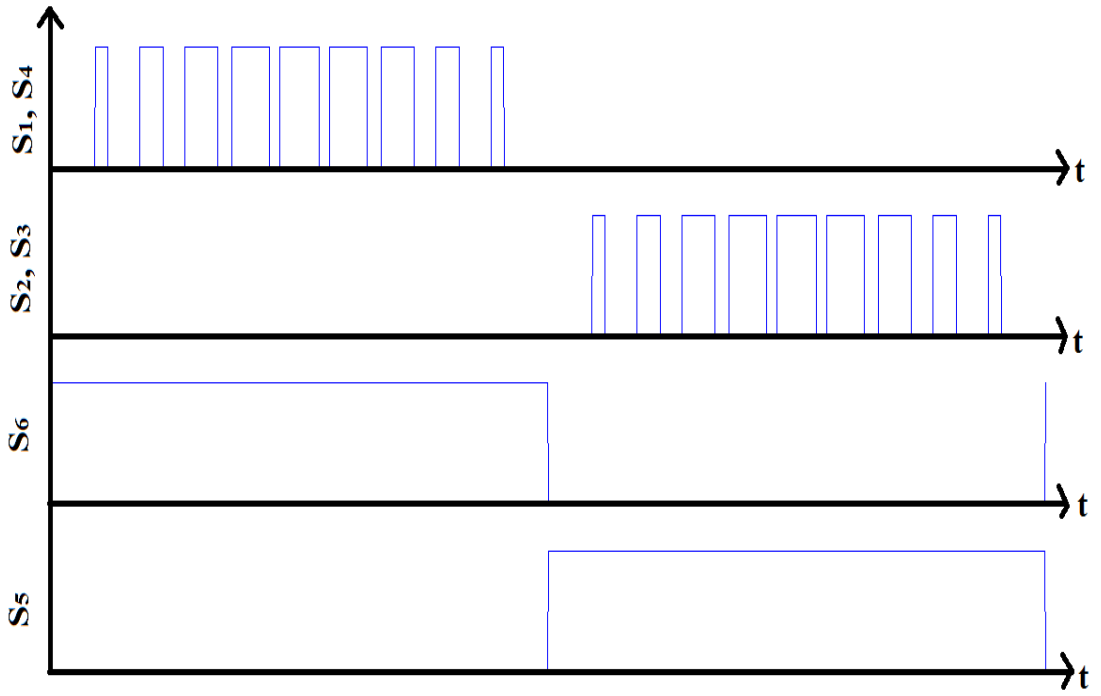


Figure 3.7: Switching pattern for HERIC inverter.

3.2.2.3 H6 Inverter

H5 and HERIC focus only on providing galvanic isolation while neglecting the effect of the CMV. In fact, the CMV of these topologies is still floating due to the influence of switches' junction capacitances and parasitic parameters (Barater, Buticchi, Lorenzani, & Malori, 2012; Bo et al., 2012). This issue is solved by the clamping diodes of H6 inverter topology (Roberto Gonzalez, Lopez, Sanchis, & Marroyo, 2007). Two dc-bypass switches, S_5 and S_6 and two clamping diodes, D_5 and D_6, are added to the conventional full bridge inverter as indicated in Figure 3.8.

Throughout the positive half-cycle, S_1 and S_4 are ON. S_5 and S_6 commutate simultaneously at switching frequency to generate the desired output voltage. S_2 and S_3 commutate together but complementarily to S_5 and S_6. Current flows through S_5, S_1, S_4 and S_6. During the freewheeling period of positive half-cycle, S_5 and S_6 are OFF and S_2 and S_3 are ON. Thus, freewheeling current finds its path in two ways, i.e., S_1 and the anti-parallel diode of S_3, and S_4 and the anti-parallel diode of S_2. At this moment, the clamping diodes clamp the freewheeling path completely to constant, $V_{DC}/2$.

Throughout the negative half-cycle, S_2 and S_3 are ON. S_5 and S_6 commutate simultaneously at switching frequency while S_1 and S_4 commutate together but complementarily to S_5 and S_6. During the freewheeling period of negative half-cycle, S_5 and S_6 are OFF and S_1 and S_4 are ON. Freewheeling current finds its path in two ways, i.e., S_3 and the anti-parallel diode of S_1, and S_2 and the anti-parallel diode of S_4. The PV is disconnected from grid by the use dc-bypass switches, S_5 and S_6. At this moment, the clamping diodes clamp the freewheeling path completely to constant, at $V_{DC}/2$.

With the clamping diodes, the CMV is clamped to the constant. Thus, the leakage current is eliminated. H6 topology is suitable for transformerless PV inverter applications. Nevertheless, H6 topology suffers from high conduction losses as the bypass switches have been added into the conduction path.

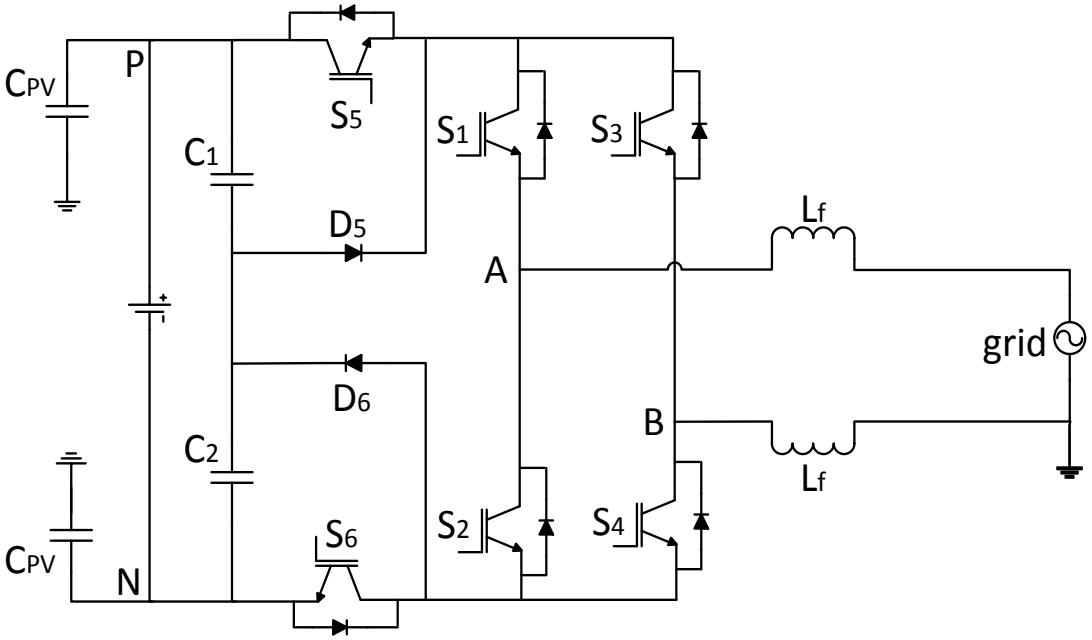


Figure 3.8: H6 inverter.

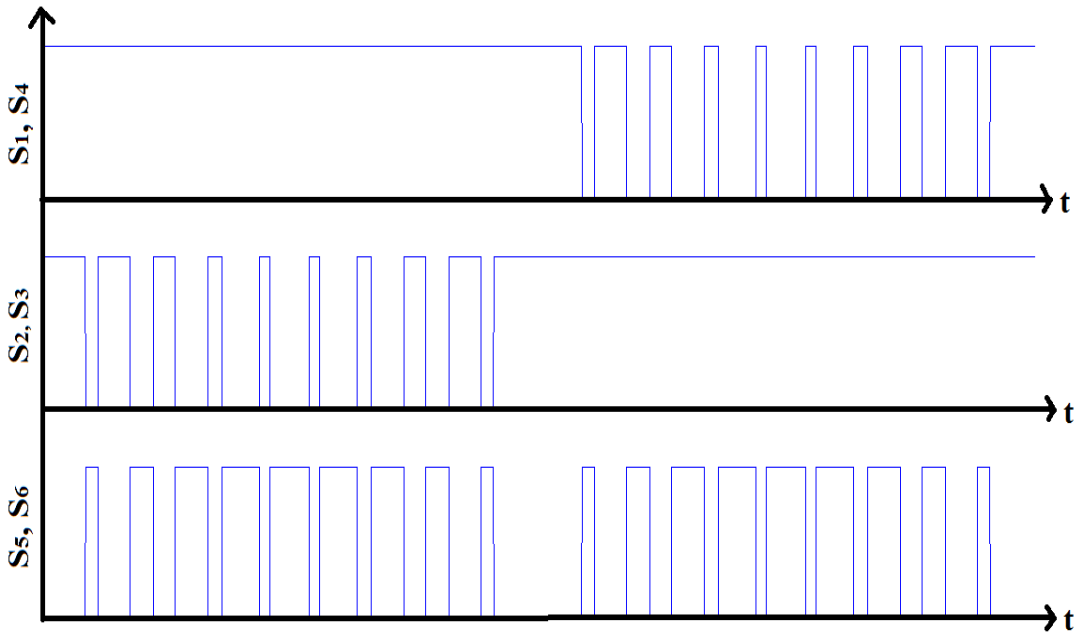


Figure 3.9 Switching pattern for H6 inverter.

3.2.2.4 oH5 Inverter

Similar to H6, oH5 inverter (Huafeng & Shaojun, 2010; Huafeng et al., 2011) is designed with CMV clamping branch. A dc-bypass switch S_5 and a clamping switch S_6 are added into the conventional full-bridge inverter structure as indicated in Figure 3.10. The voltage divider is made up of two capacitors.

Throughout the positive half-cycle, S_1 is ON. S_4 and S_5 commutate simultaneously at switching frequency but complementarily to S_3 and S_6. During the conduction period of positive half-cycle, current flows through S_2, S_3 and S_5 to generate the desired output voltage. The current freewheels through S_1 and anti-parallel diode of S_3 during the freewheeling period. At this moment, the clamping switch is ON to clamp the freewheeling path completely to constant, $V_{DC}/2$.

Throughout the negative half-cycle, S_3 is ON. S_2 and S_5 commutate simultaneously at switching frequency but complementarily to S_1 and S_6. During the conduction period of positive half-cycle, current flows through S_1, S_4 and S_5 to generate the desired output voltage. The current freewheels through S_3 and anti-parallel diode of S_1 during the freewheeling period. At this moment, the clamping switch is ON to clamp the freewheeling path completely to constant, $V_{DC}/2$.

With the clamping switch, the CMV is clamped completely to the constant. As a result, the leakage current is eliminated. oH5 topology is suitable for transformerless PV inverter applications. Similar to H6 topology, oH5 topology suffers from high conduction losses as the bypass switches have been added into the conduction path.

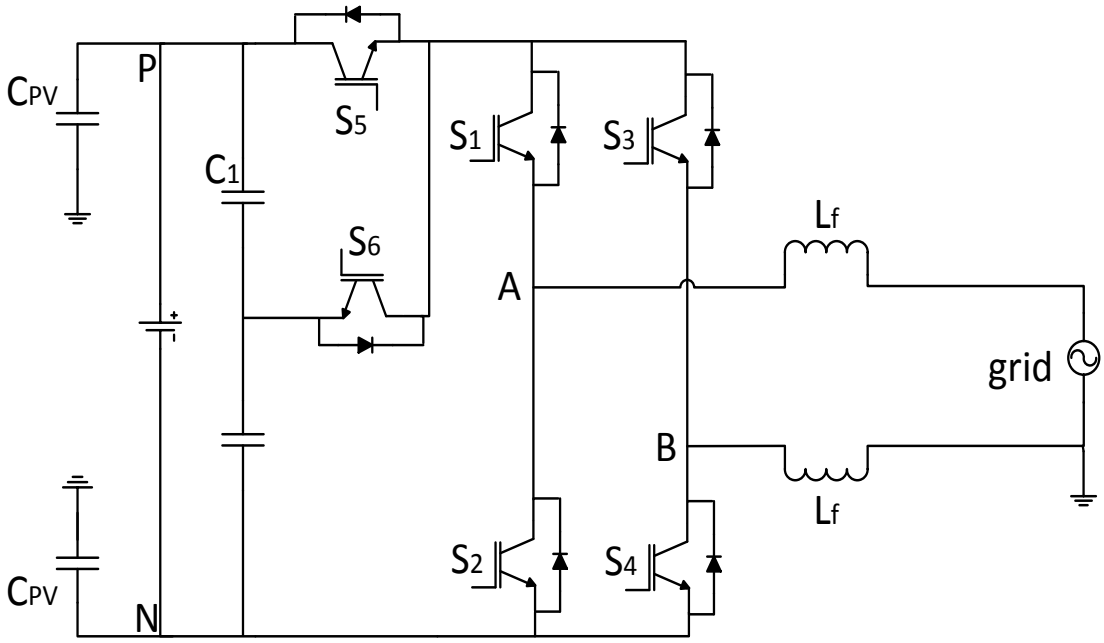


Figure 3.10: oH5 inverter.

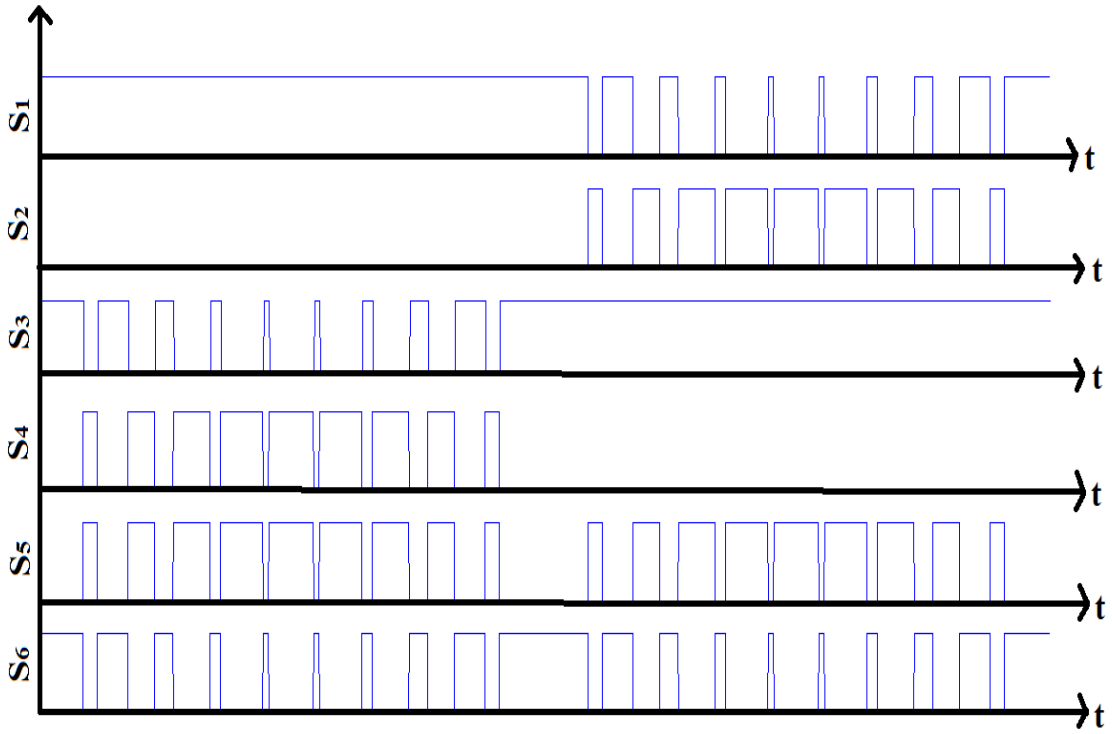


Figure 3.11: Switching pattern for oH5 inverter.

3.2.2.5 HBZVR Inverter

HBZVR inverter (Kerekes et al., 2011) is designed by adding a bi-directional freewheeling path in the ac-side of the conventional full-bridge inverter structure as shown in Figure 3.12. The freewheeling path consists of a bi-directional switch, S_5, a full-bridge rectifier (four diodes) and a clamping diode, D_5. The voltage divider is made up of two capacitors.

Each pair of the diagonal switches, i.e., S_1, S_4 and S_2, S_3, is operated simultaneously at switching frequency during the positive and negative half-cycle respectively. Current flows through the corresponding pair of diagonal switches to generate the desired output voltage. On the other hand, the bi-directional switch, S_5, is ON during the freewheeling period. Current freewheels through D_2 and D_3, and, D_1 and D_4 during the positive and negative half-cycle respectively. At the same time, D_5 conducts and clamps the CMV to constant, $V_{DC}/2$.

Galvanic isolation is provided via the bi-directional freewheeling path. As a result, leakage current is reduced significantly. Hence, it is suitable for transformerless PV inverter applications. It is worth noting that the clamping diode does not working optimally. The CMV is still floating in one half-cycle. The detail of which will be covered in the following section.

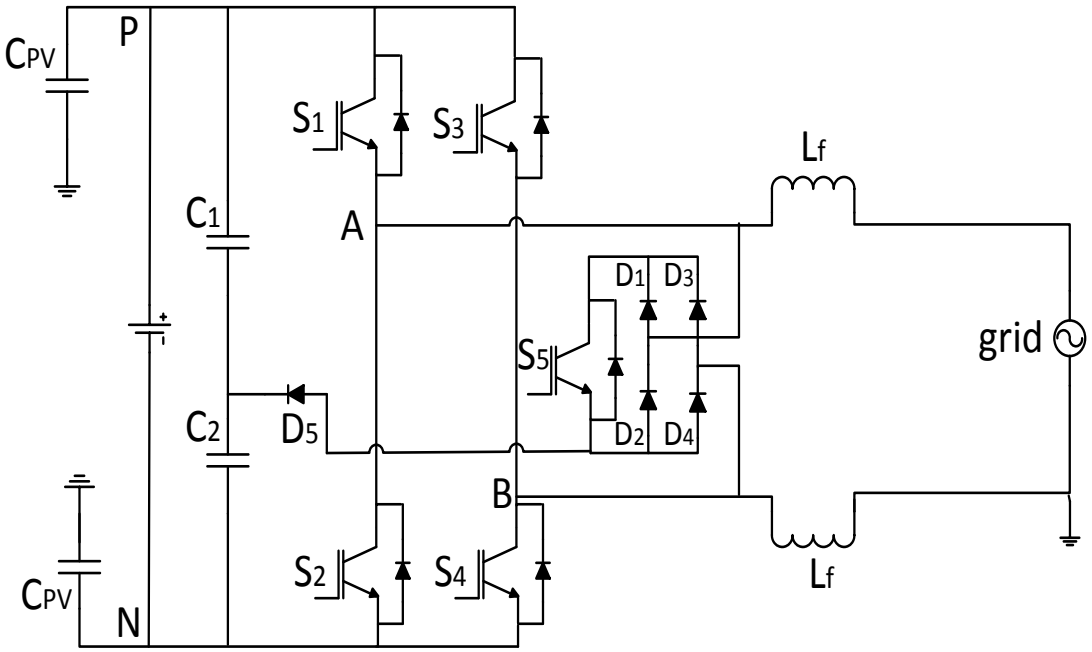


Figure 3.12: HBZVR inverter.

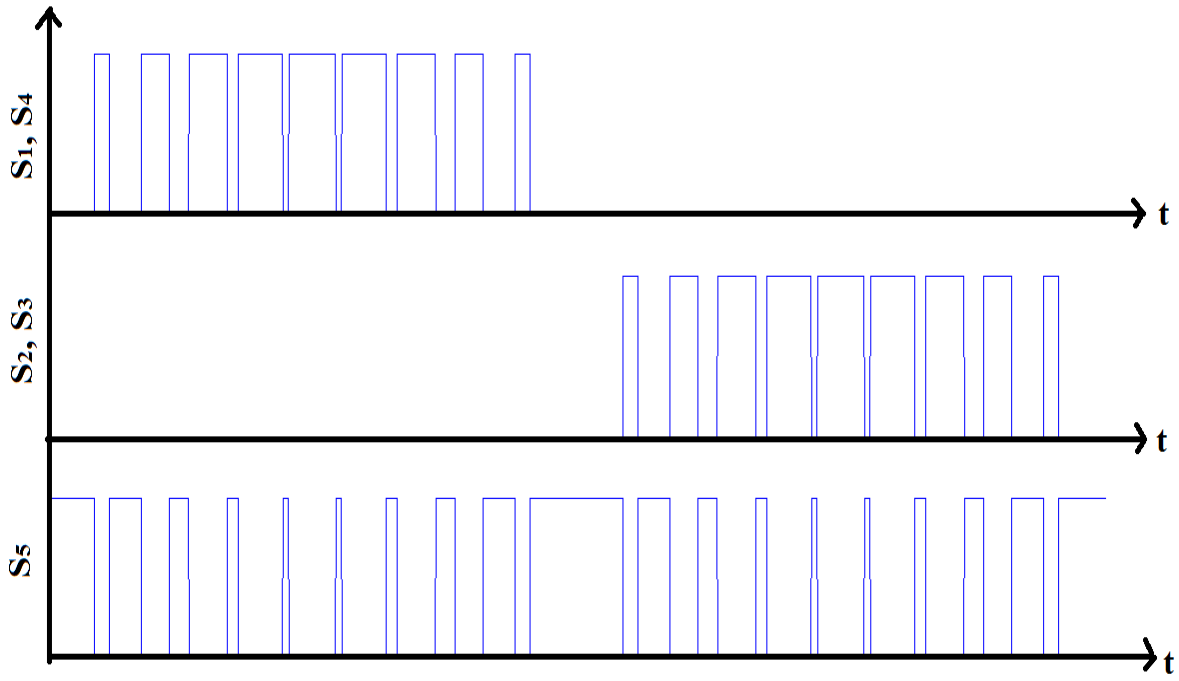


Figure 3.13: Switching pattern for HBZVR inverter.

3.2.3 Leakage Current Reduction Method

Conventional half-bridge inverter is used in transformerless PV systems to generate constant CMV to reduce the leakage current. However, a 700 V dc-link voltage is required for the half-bridge and diode-clamped topologies (Cavalcanti, Farias, Oliveira, Neves, & Afonso, 2012; R. Gonzalez et al., 2008; Huafeng & Shaojun, 2012).

Therefore, many research works have been proposed recently to eliminate leakage current via galvanic isolation and CMV clamping techniques. Galvanic isolation topologies such as H5 inverter, H6 family (Baojian et al., 2013; Bo et al., 2012; Li, Kai, Yan, & Mu, 2014; Wensong, Jih-Sheng, Hao, & Hutchens, 2011) and HERIC inverter introduce dc-decoupling and ac-decoupling to disconnect the PV from the grid. It is found that ac-decoupling provides lower losses due to reduced switch count in the conduction path.

Nevertheless, the galvanic isolation alone cannot completely eliminate the leakage current due to the influence of switches' junction capacitances and parasitic parameters (Barater, Buticchi, Lorenzani, & Malori, 2012; Bo et al., 2012). Therefore, CMV clamping has been used in oH5 inverter, H6 inverter and HBZVR inverter to completely eliminate the leakage current. However, the clamping branch of HBZVR inverter does not perform optimally. It is shown in the later section that the leakage current is as high as those of galvanic isolation topologies.

3.2.3.1 Galvanic Isolation

In transformerless PV inverters, the galvanic connection between the PV and the grid allows the leakage current to flow. Hence, in topologies such as H5 and HERIC, galvanic isolation is provided to reduce the leakage current.

The galvanic isolation can be basically be categorized into dc-decoupling and ac-decoupling methods. For dc-decoupling method, dc-bypass switches are added on the dc side of the inverter to disconnect the PV arrays from the grid during the freewheeling period. However, the dc-bypass branch, which consists of switches or diodes, is included in the conduction path as shown in Figure 3.14. Hence, conduction losses increase due to the increased number of semiconductors in the conduction path.

On the other hand, bypass branch can also be provided on the ac side of the inverter (i.e. ac-decoupling method) such as seen in HERIC. This ac-bypass branch functions as a freewheeling path which is completely isolated from the conduction path, as shown in Figure 3.14. As a result, the output current flows through only two switches during the conduction period. Therefore, topologies employing ac-decoupling techniques (Kerekes et al., 2011; Ketterer et al., 2003) are found to be higher in efficiency as compared to dc-decoupling dc-decoupling topologies (Baojian et al., 2013; Bin et al., 2013; Huafeng et al., 2011; Li et al., 2014; Wensong et al., 2011).

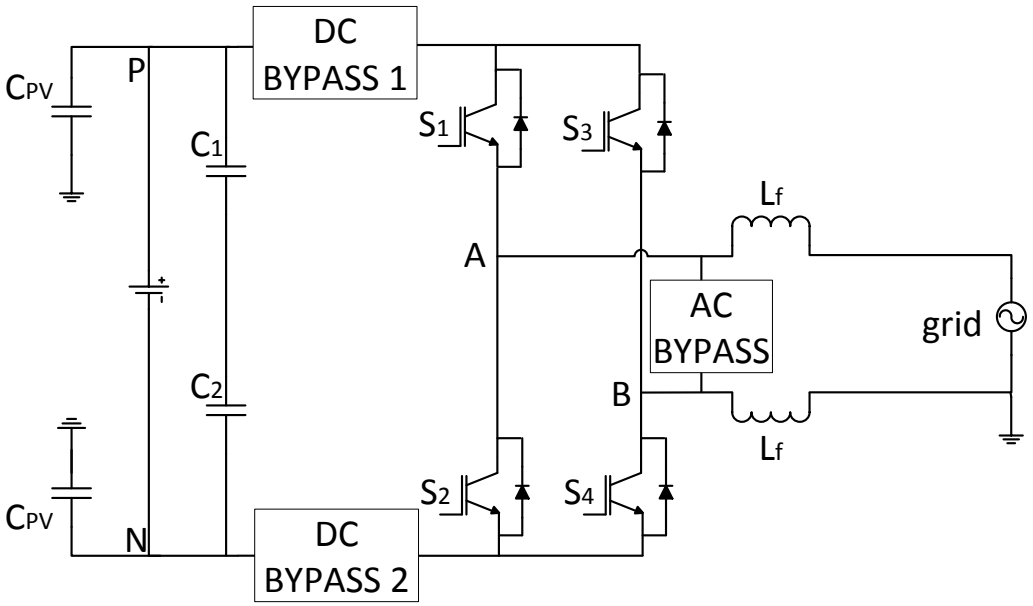


Figure 3.14: Universal transformerless topologies.

One setback of galvanic isolation is that there is no way of controlling the CMV by PWM during the freewheeling period. Figure 3.15 shows operation modes of galvanic isolation which employs dc-decoupling method. As shown in Figure 3.15, during the conduction period, S_1 and S_4 conduct to generate the desired output voltage. At the same time, V_A is directly connected to V_{DC} and V_B is connected to the negative terminal (N) of the dc-link. Thus, the CMV becomes

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2}(V_{DC} + 0) = \frac{V_{DC}}{2} \qquad (3.1)$$

Nevertheless, during the freewheeling period, the dc-bypass switches disconnect the dc-link from the grid. Therefore, point A and point B are isolated from the dc-link, and V_A and V_B are floating with respect to the dc-link as shown in Figure 3.16. The CMV during this period of time is not determined by the switching state, instead, is oscillating with amplitude depending on the parasitic parameters and the switches' junction capacitances of the corresponding topology. As a result, leakage current can still flow during freewheeling period. The same is the case for converters using ac-decoupling method.

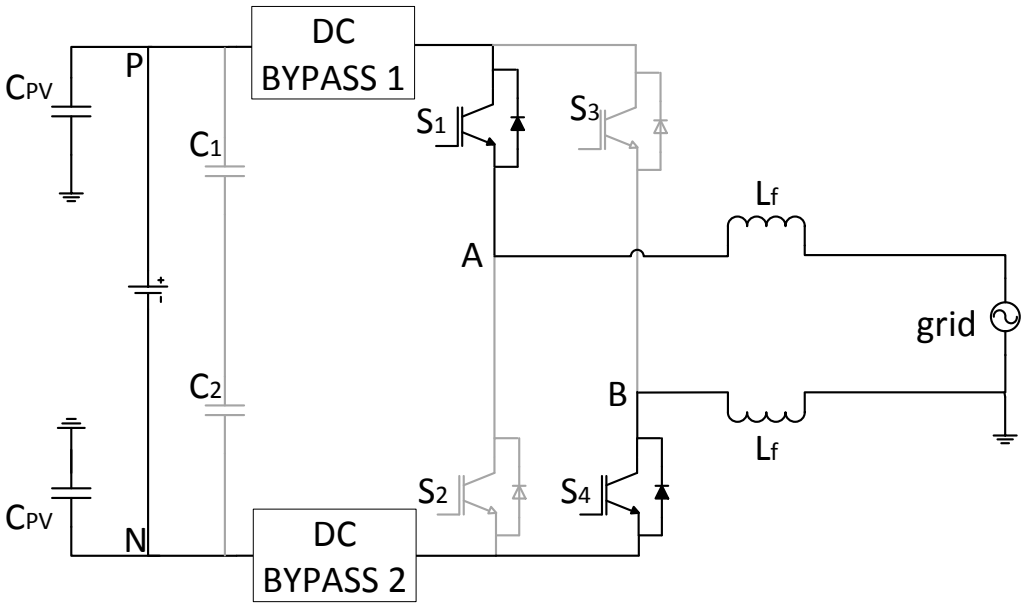


Figure 3.15: Conduction mode for dc-decoupling topology.

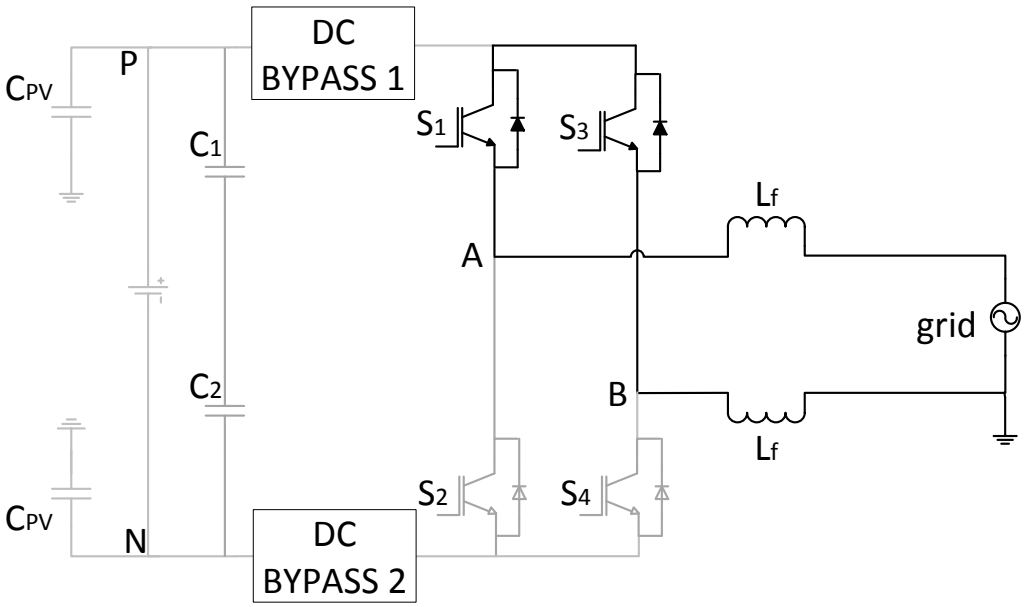


Figure 3.16: Freewheeling mode for dc-decoupling topology.

3.2.3.2 CMV Clamping

As mentioned earlier, CMV is one of the main causes for leakage current. H5 and HERIC inverter topologies focus only on providing isolation while neglecting the effect of the CMV. Unlike conventional topologies, the CMV in these topologies cannot be manipulated via PWM, due to the use of galvanic isolation as explained previously. In order to generate constant CMV, clamping branch is introduced in oH5 and H6 inverter topologies. Generally, the clamping branch consists of diodes or switches and a capacitor divider which ensures the freewheeling path is clamped to the half of the input voltage. With the combined effect of galvanic isolation and CMV clamping, leakage current is completely eliminated.

Nevertheless, both H6 and oH5 inverter topologies utilize dc-decoupling method, which suffers from lower efficiency. HBZVR topology also employs CMV clamping technique but it is found that the clamping branch does not function optimally. It is shown in both the simulation and experimental results in chapter 4 that the CMV and the leakage current in HBZVR topology are as high as those in the topologies which use only galvanic isolation.

3.3 Three-Phase Transformerless PV Inverters

The reliability of the inverter mainly depends on the dc-link capacitors (Wang & Blaabjerg, 2014). In a three-phase balance system, there is a constant output power. Therefore, smaller dc-link capacitors are required. This improves the robustness and increases the lifetime for the PV inverter (Cavalcanti et al., 2010; Kerekes, Teodorescu, Klumpner, et al., 2007). Three-phase system achieves higher power up to 20 kW applications.

Three-phase full-bridge inverter, as shown in Figure 3.17, is widely used due to its simplicity of hardware design and software implementation. Conventional pulse width modulation (PWM) such as sinusoidal PWM (SPWM), SVPWM or DPWM, are used as the PWM for the full-bridge inverter. Nevertheless, these conventional PWMs are not suitable for three-phase transformerless PV applications due to high leakage current. In order to reduce the leakage current to meet the requirement of the standard, several converter structures and modulation techniques have been proposed recently.

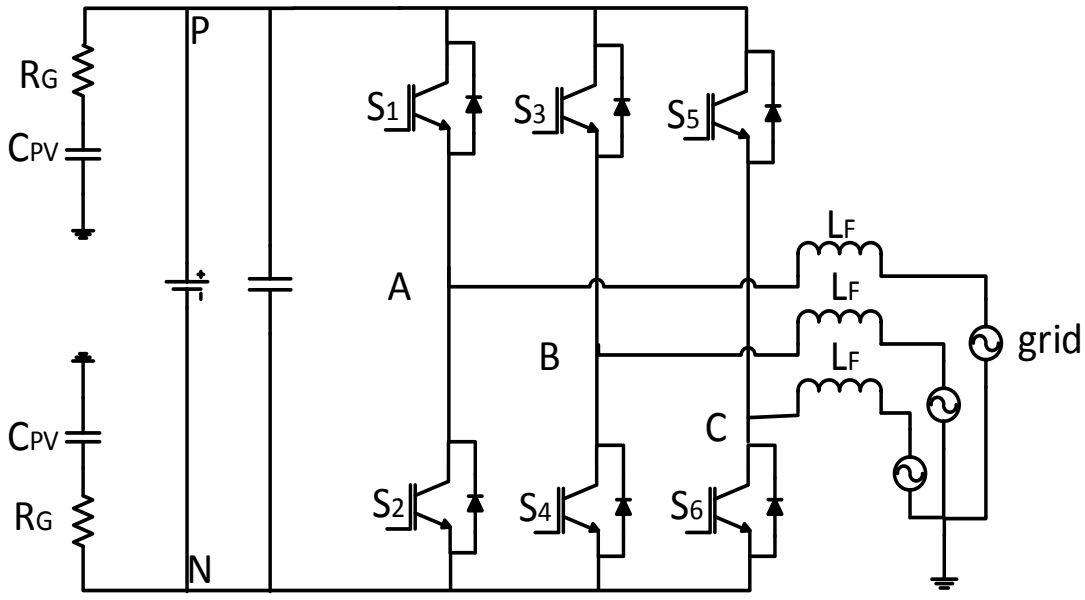


Figure 3.17: Three-phase full-bridge inverter.

Reduced CMV PWM (RCMV-PWM) methods such as AZPWM (Oriti, Julian, & Lipo, 1997), NSPWM (Un & Hava, 2009) and RSPWM (Cacciato, Consoli, Scarcella, & Testa, 1999), are proposed recently. Without zero vectors, RCMV-PWM methods are able to reduce the CMV to reduce the leakage current.

Besides, several inverter structures have been proposed lately. (Kerekes, Teodorescu, Klumpner, et al., 2007) connects the grid neutral to the midpoint of the dc-link capacitors to clamp the CMV to constant. As a result, the leakage current is eliminated. Two bidirectional freewheeling path are added to the conventional full-bridge inverter structure to provided galvanic isolation in (Vazquez et al., 2010). The recently proposed modulation techniques and the converter structures are reviewed and investigated in this section.

3.3.1 Modulation Techniques

Conventional SVPWM and DPWM methods are widely used due to their high performances, i.e., high voltage linearity, low switching loss and low harmonic distortion (Hava, x, & etin, 2011). Nevertheless, these PWM methods generate high CMV which results high leakage current. This leakage current injects high ripples which increase the losses and harmonic distortion. In other words, the overall performances of the PV inverter are degraded.

In order to reduce the CMV to reduce the leakage current, several modulation techniques, which are termed as RCMV-PWM, have been proposed recently. The modulation techniques can be classified into two types: A and B, based on the way the space vector sectors are partitioned, as shown in Figure 3.18. Those belong to type A voltage vector state include SVPWM (Hava et al., 2011), AZPWM (Oriti et al., 1997) and RSPWM (Cacciato et al., 1999). DPWM (Hava et al., 2011) and NSPWM (Un & Hava, 2009) employ type B voltage vector state. The pulse pattern for various PWM methods are listed in Table I (Hava & Un, 2009, 2011).

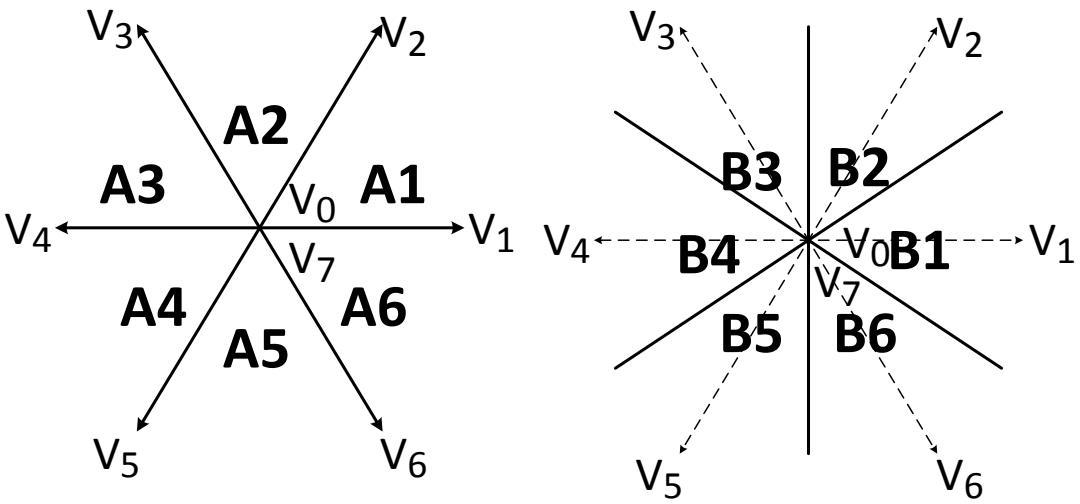


Figure 3.18: Voltage vector states for RCMV-PWM methods with different way of partioning the space vectors: (a) Type A and (b) type B.

Table 3.1: Pulse patterns for various PWM methods

	A1	**A2**	**A3**	**A4**	**A5**	**A6**
SVPWM	7210127	7230327	7430347	7450547	7650567	7610167
AZPWM	6123216	4321234	2345432	6543456	4561654	2165612
RSPWM	31513	31513	31513	31513	31513	31513
	B1	**B2**	**B3**	**B4**	**B5**	**B6**
NSPWM	21612	32123	43234	54345	65456	16561

DPWM	**B1**	**A1**	**B2**	**A2**	**B3**	**A3**	**B4**	**A4**	**B5**	**A5**	**B6**	**A6**	**B1**
	72127		23032		74347		45054		76567		61016		
		21012		72327		43034		74547		65056		76167	

3.3.1.1 AZPWM

AZPWM (Oriti et al., 1997) employs only active vectors to program the output voltage. The choice of the active vectors is the same as those in conventional SVPWM. The zero vectors (V_0 and V_7) are replaced with a pair of opposite active vectors with equal duration, i.e., V_1 and V_4, V_2 and V_5, or V_3 and V_6. The pulse pattern of which is listed in Table 3.1 (Hava & Un, 2009).

The pair of opposite active vectors that is adjacent to the active vectors is chosen. For instance, V_3 and V_6 pair is chosen to replace V_0 and V_7 respectively in region A1 as shown in Figure 3.14. V_3 and V_6 pair is chosen because it is adjacent to the active vectors V_1 and V_2. The same approach is applied to all the regions (A1-A6).

Without any zero vectors, the CMV is reduced by 2/3, varying between 1/3 and 2/3. As a result, the leakage current is reduced. Nevertheless, the performance is degraded. Figure 3.19 shows the switching pattern, line-to-line output voltage and the CMV for AZPWM in region A1. It is found that simultaneous switching of two switches appears. Practically, the simultaneous switching of two switches is impossible due to the dead time effect and the non-identical power electronic devices. This will lead to higher CMV than that of conventional SVPWM and DPWM.

In addition, the replacement of zero vectors with opposite active vectors pair results bipolar line-to-line output voltage as shown in Figure 3.19. The two-level bipolar voltage, i.e., $-V_{DC}$ and $+V_{DC}$, doubles the losses and stresses across filter inductors. This increases the losses, current ripples, and thus, filters size and cost.

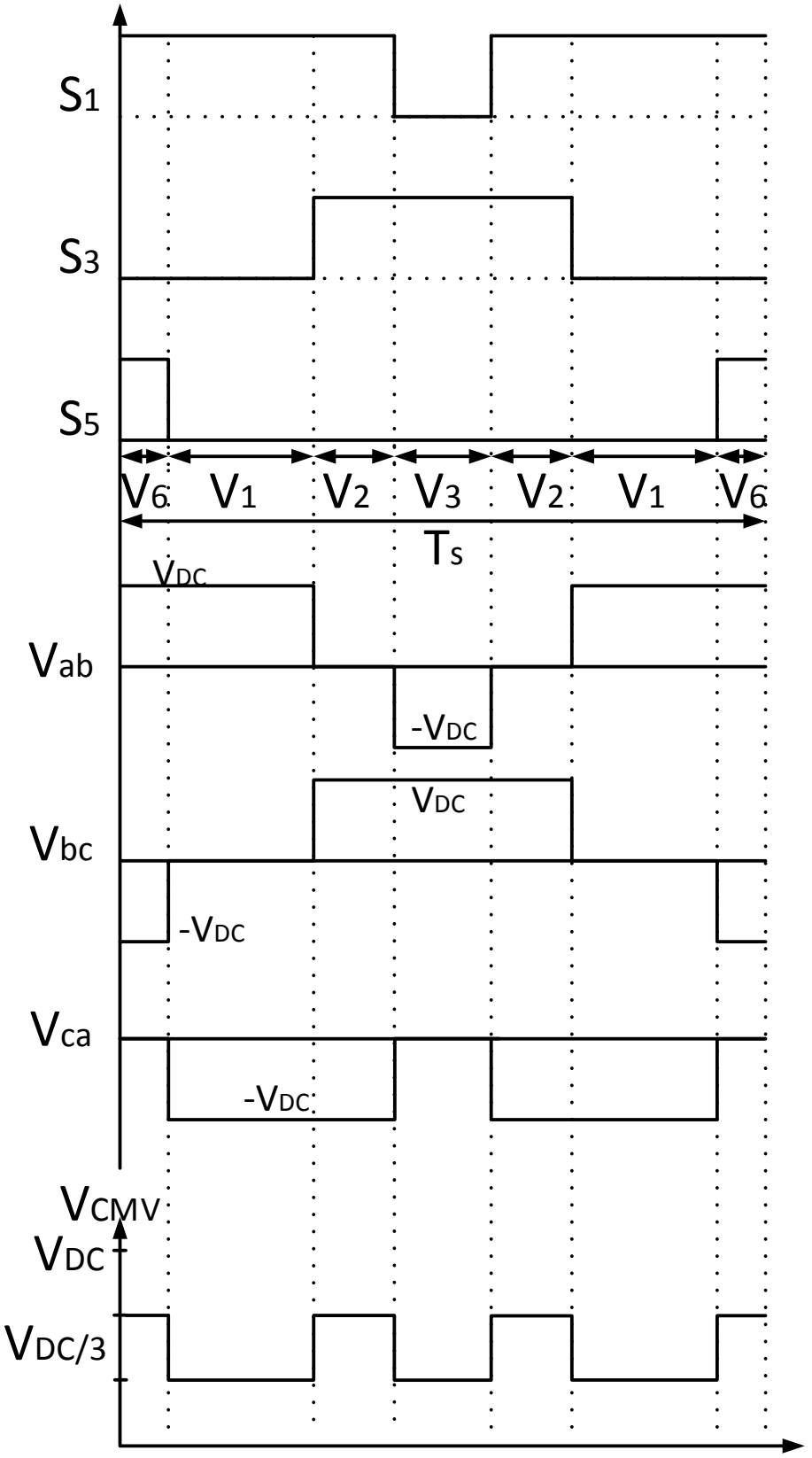


Figure 3.19: Switching pattern, line-to-line output voltages and CMV for AZPWM.

3.3.1.2 NSPWM

NSPWM (Un & Hava, 2009) utilizes only three adjacent active vectors to program the desired output voltage, i.e., V_1, V_2, V_3 or V_2, V_3, V_4 and so on. Therefore, it is termed as near-state PWM (NSPWM). The complete pulse pattern of NSPWM is listed in Table 3.1.

The active vector is carefully chosen such that minimum switch count is obtained. Similar to conventional DPWM, one of the inverter is clamped to the dc bus in region. For example, pulse pattern in region B1 is V_6 V_2 V_1 V_2 V_6 as shown in Figure 3.20. Obviously, phase A is clamped to the positive dc bus in region B1. As a result, the switching loss decreases as one of the phase is not modulated in each region. Besides, the simultaneous switching issue of AZPWM is avoided in NSPWM.

Without any zero vectors, the CMV is reduced by 2/3, varying between 1/3 and 2/3. As a result, the leakage current is reduced. Figure 3.20 shows the switching pattern, line-to-line output voltage and the CMV for AZPWM in region A1. Nevertheless, the elimination of zero vectors still results unfavorable bipolar line-to-line output voltage as shown in Figure 3.20. The two-level bipolar voltage increases the losses, voltage stresses and current ripples across. Therefore, larger filter inductors are required which increases the weight and cost of the PV inverter.

On the other hand, the voltage linearity (modulation range) is compromised. NSPWM operates linearly only for $0.61 < m < 0.907$ (m is modulation index). Beyond this region, the CMV and the leakage current generated could be higher than that of conventional PWM.

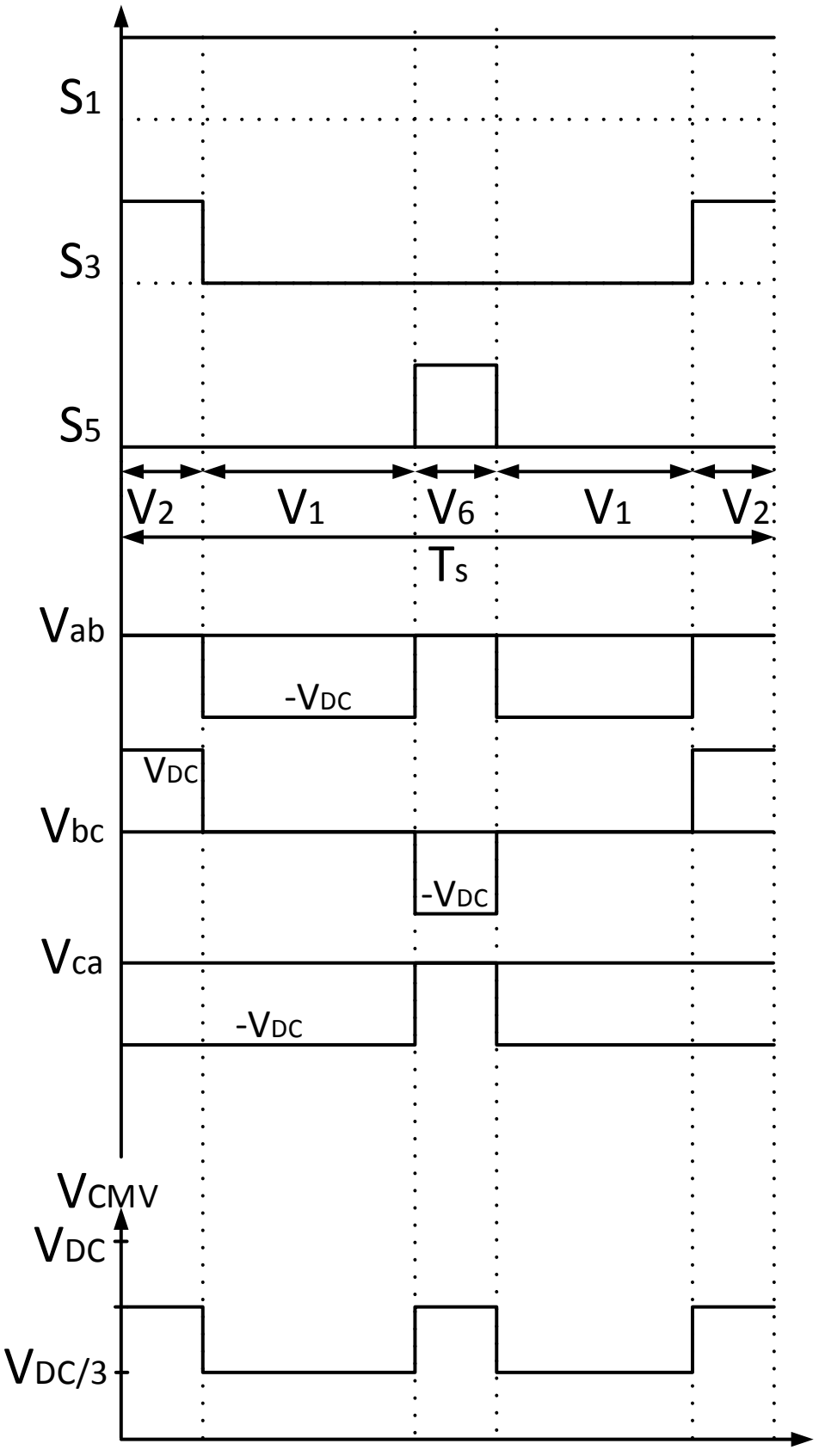


Figure 3.20: Switching pattern, line-to-line output voltages and CMV for NSPWM.

3.3.1.3 RSPWM

In RSPWM (Cacciato et al., 1999; Cavalcanti et al., 2010), a group of odd active vectors (V_1, V_3 and V_5) or even active vectors (V_2, V_4 and V_6) is used to generate desired output voltage throughout the regions. As a result, RSPWM achieves best common-mode behavior among the RCMV-PWM methods, with constant CMV at 1/3, as shown in Figure 3.21. This eliminates the leakage current, merely zero leakage current.

Nevertheless, RSPWM only focus on leakage current elimination and neglect the overall performance of the PV inverter. Figure 3.21 shows switching pattern, line-to-line output voltages and CMV for RSPWM. Although RSPWM achieves constant CMV at 1/3, it suffers from reduced voltage linearity. The maximum magnitude of phase voltage is only 1/3 V_{DC}. In other words, RSPWM is only applicable for $m < 0.52$. Up to 1100 V dc bus voltage is required for 230V grid system. As a result, very high operational losses occur. Hence, it is not practical for PV application systems.

RSPWM suffers from severe bipolar line-to-line output voltage. Two-level bipolar voltage waveform appears in all the three phases (phase A, phase B and phase C). Such phenomenon increases the loss, current ripples and harmonic distortion significantly. Thus, RSPWM has very low efficiency.

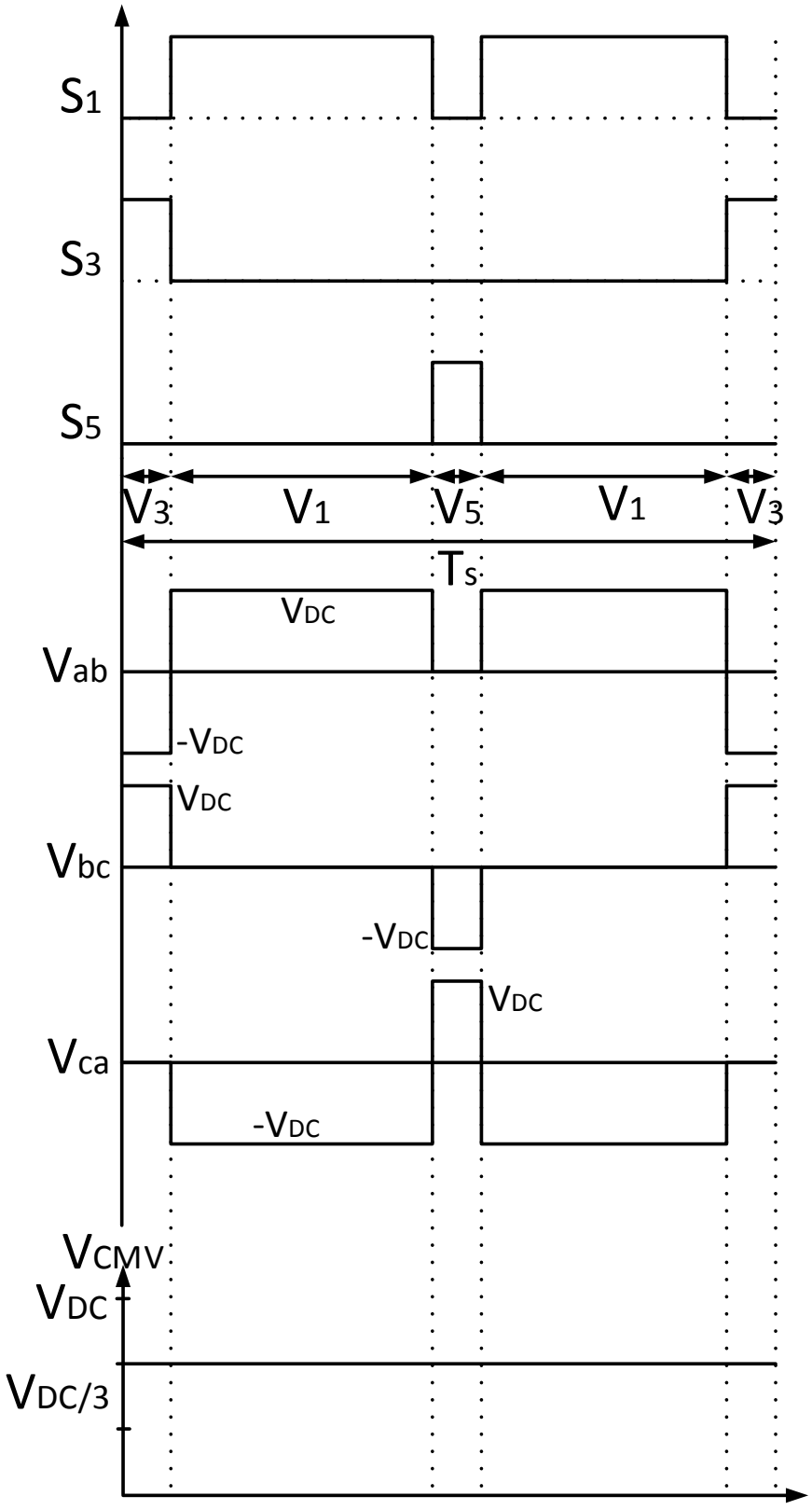


Figure 3.21: Switching pattern, line-to-line output voltages and CMV for RSPWM.

3.3.2 Converter Structures

When the transformer is removed, the galvanic connection between the PV arrays and the grid allows the leakage current to flow. Therefore, many works have been done in (Baojian et al., 2013; Bo et al., 2012; Kerekes et al., 2011; Ketterer et al., 2003; Li et al., 2014; Victor et al., 2008; Wensong et al., 2011) to design conversion structure which provides galvanic isolation to reduce the leakage current. Either dc-decoupling or ac- decoupling methods are utilized to disconnect the PV arrays from the grid during the freewheeling period. The modulation techniques are also carefully designed with the corresponding conversion structure in order to generate the desired output voltage and to reduce the leakage current. Such topologies yield satisfactory overall performance. Nevertheless, most of the galvanic isolation topologies are found in single-phase PV inverters. For three-phase PV inverters, modulation techniques are much more complicated and galvanic isolation methods are therefore difficult to be implemented.

As shown in Figure 3.22, (Kerekes, Teodorescu, Klumpner, et al., 2007) proposes the connection between the neutral of the grid to the midpoint of the dc-link capacitors. Such connection ensures constant voltage across the stray capacitance which leads to zero leakage current. Nevertheless, this is not practical because such connection creates the inductance in the neutral line (Cavalcanti et al., 2010; Cavalcanti et al., 2012). This inductance generates high-frequency potential between the PV array and the ground which leads to leakage current higher than the permissible level recommended in the standard.

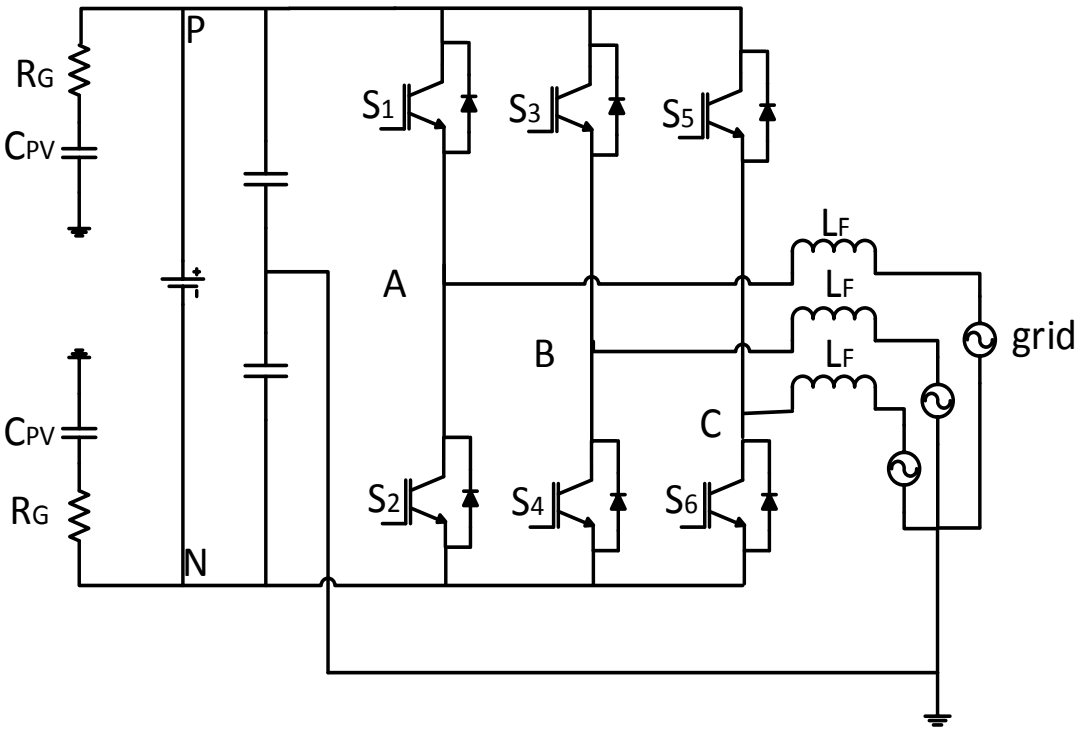


Figure 3.22: Three-phase inverter with split capacitor topology.

A new conversion topology with corresponding PWM has been proposed in (Vazquez et al., 2010) to reduce the CMV. Two freewheeling path are added to the conventional three-phase full-bridge inverter structure as shown in Figure 3.23. These freewheeling path provides galvanic isolation which disconnects the PV from the grid during the freewheeling period to reduce the leakage current.

Nevertheless, the freewheeling path is made up of two switches and fourteen diodes as shown in Figure 3.23. The excessive additional components significantly increase the cost, the losses and the size of the entire PV inverter. Moreover, the leakage current is still relatively high, 280mA, as reported in (Vazquez et al., 2010).

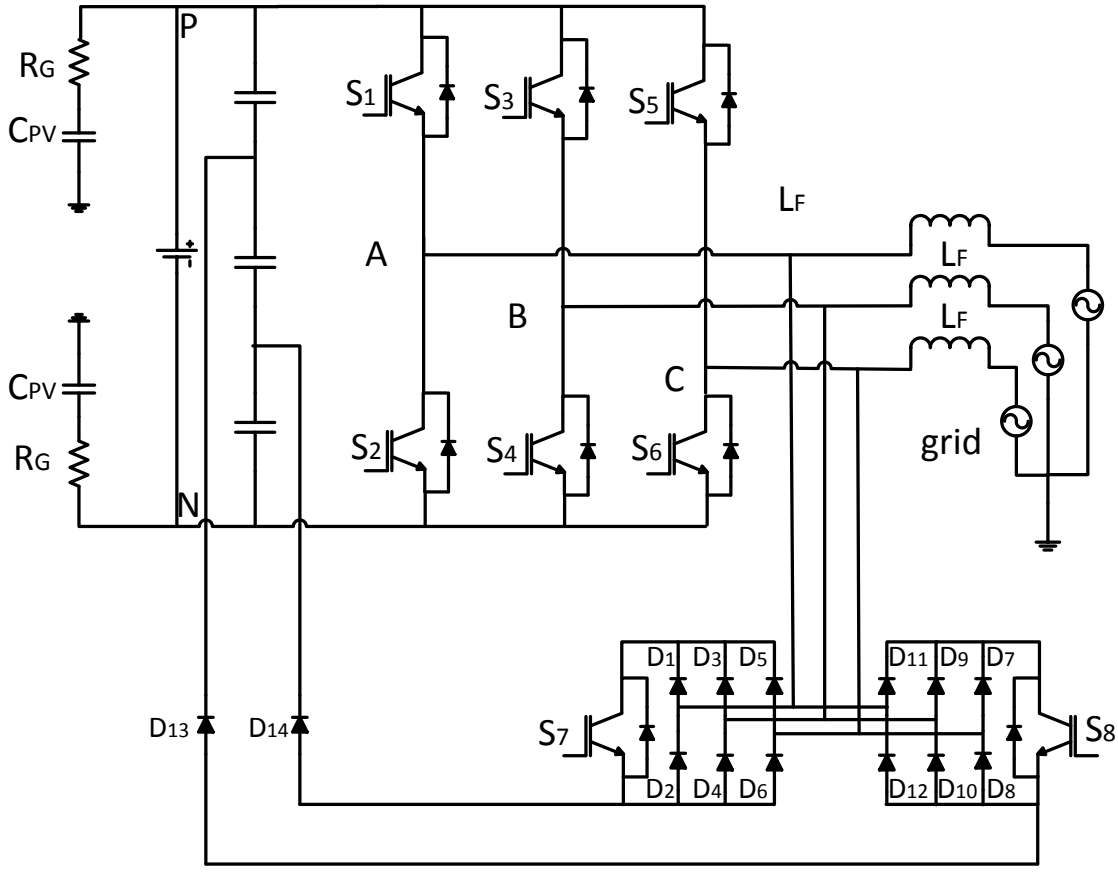


Figure 3.23: Three-phase inverter with freewheeling path.

3.4 Conclusion

This chapter provides a comprehensive review of recently proposed transformerless PV inverter for both single- and three-phase systems. In the past, various transformerless PV inverter topologies have been introduced, with leakage current minimized by the means of modulation techniques and conversion structure. The circuit configuration, modulation techniques and operation principles for various topologies are studied and analyzed.

Generally, single-phase transformerless PV inverter employs either dc- or ac-decoupling method to disconnect the PV from the grid during the freewheeling period. The latter method is more attractive due to higher efficiency. In addition, CMV clamping branch is introduced by oH5 and H6 inverter topologies. With the clamping branch, the CMV is completely clamped to constant. The leakage current is thoroughly eliminated.

For three-phase system, RCMV-PWM methods such as AZPWM, NSPWM and RSPWM have been proposed recently. These modulation techniques employ only active vectors to reduce the CMV. However, the overall performances in terms of voltage linearity, voltage waveform, and harmonic distortion are neglected.

CHAPTER 4

PROPOSED SINGLE-PHASE TRANSFORMERLESS PV INVERTER

4.1 Introduction

In this chapter, a single-phase transformerless PV inverter is proposed based on the analysis of previous chapters. An in-depth analysis of the circuit configuration, operation principle and its hardware implementation is discussed and studied.

Galvanic isolation topologies such as H5, H6 and HERIC introduce dc-decoupling and ac-decoupling to disconnect the PV from the grid. It is found that ac-decoupling provides lower losses due to reduced switch count in the conduction path. Nevertheless, the galvanic isolation alone cannot completely eliminate the leakage current. Therefore, CMV clamping has been introduced in oH5, H6 and HBZVR to completely eliminate the leakage current. However, the clamping branch of HBZVR does not perform optimally.

This chapter explains how the proposed topology to solve the abovementioned issues. The overall performance, in terms of CMV, leakage current, losses, efficiency and THD, is compared with other topologies. Finally, the simulation and experimental results are presented.

4.2 Structure of Proposed Topology

Based on the analysis of previous chapters, a simple modified H-bridge zero state rectifier (HBZVR-D) is proposed to combine the benefits of the low-loss ac-decoupling method and the complete leakage current elimination of the CMV clamping method. HBZVR-D is modified by adding a fast-recovery diode, D_6, to the existing HBZVR as shown in Figure 4.1. The voltage divider is made up of C_1 and C_2. S_1-S_4 are the switches for the full-bridge inverter. The anti-parallel diodes, D_1-D_4, as well as S_5, provide a freewheeling path for the current to flow during the freewheeling period. Diodes D_5 and D_6 form the clamping branch of the freewheeling path.

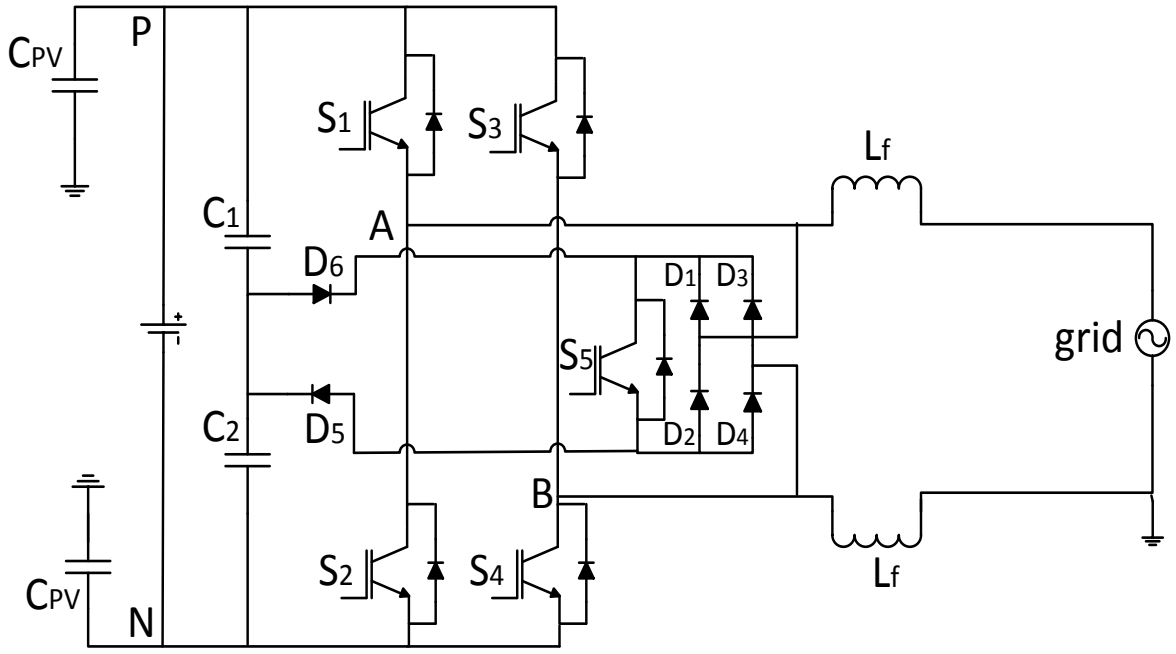


Figure 4.1: The conversion structure of the proposed HBZVR-D topology.

4.3 Operation Modes and Analysis

Figure 4.2 illustrates the switching patterns of the proposed HBZVR-D. Switches S_1-S_4 commutate at switching frequency to generate unipolar output voltage. S_5 commutates complementarily to S_1-S_4 to create freewheeling path. All the four operation modes are shown in Figure 4.3 to Figure 4.6 to generate unipolar output voltage.

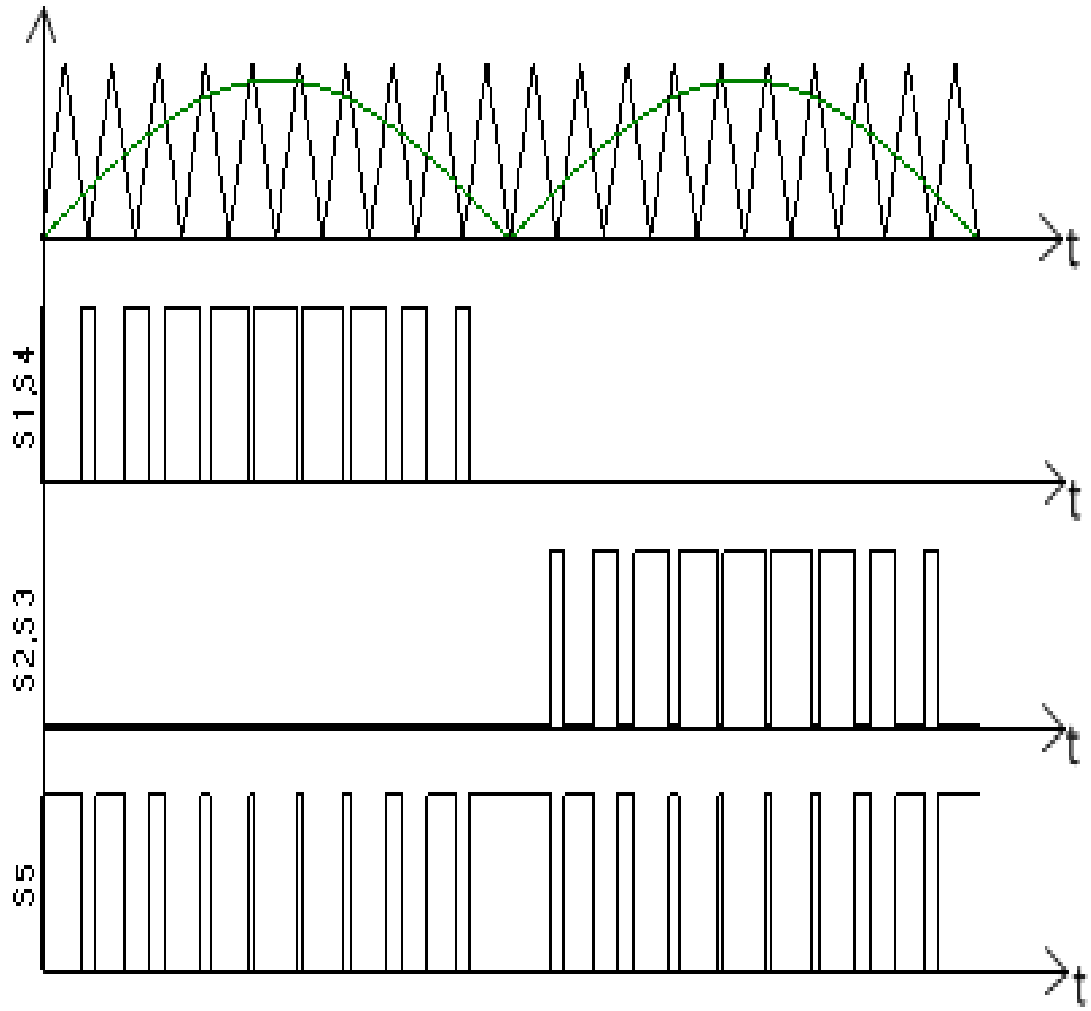


Figure 4.2: Switching pattern of the proposed HBZVR-D topology.

In mode 1, S_1 and S_4 are ON while S_2, S_3 and S_5 are OFF. Current increases and flows through S_1 and S_4. $V_{AB} = +V_{DC}$. The CMV becomes

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2}(V_{DC} + 0) = \frac{V_{DC}}{2} \qquad (4.1)$$

In mode 2, S_1 and S_4 are OFF. S_5 is ON to create a freewheeling path. Current decreases and freewheels through diodes D_3, D_2 and the grid. The voltage V_{AN} decreases and V_{BN} increases until their values reach the common point, $V_{DC}/2$, such that $V_{AB} = 0$. The CMV becomes

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2}(\frac{V_{DC}}{2} + \frac{V_{DC}}{2}) = \frac{V_{DC}}{2} \qquad (4.2)$$

In mode 3, S_2 and S_3 are ON while S_1, S_4 and S_5 are OFF. Current increases and flows through S_2 and S_3. $V_{AB} = -V_{DC}$. The CMV becomes

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2}(0 + V_{DC}) = \frac{V_{DC}}{2} \qquad (4.3)$$

In mode 4, S_1 and S_4 are OFF. S_5 is ON to create a freewheeling path. Current decreases and freewheels through diodes D_1, D_4 and the grid. The voltage V_{AN} decreases and V_{BN} increases until their values reach the common point, $V_{DC}/2$, such that $V_{AB} = 0$. The CMV is as derived in (4.2)

Obviously, modulation techniques are designed to generate constant CMV in all four operation modes. All the research works are designed based on the principles above. Practically, V_{AN} and V_{BN} do not reach the common point during the freewheeling period (mode 2 and mode 4). It is shown in simulation (section 4.5) and experimental results (section 4.6) later that the CMV is not constant without clamping branch. During the freewheeling period, both V_{AN} and V_{BN} are not clamped to $V_{DC}/2$ and is oscillating with amplitude depending on the parasitic parameters and junctions' capacitance of those topologies.

The improved clamping branch of HBZVR-D ensures the complete clamping of CMV to $V_{DC}/2$ during the freewheeling period. It is well noted that the output current flows through only two switches in every conduction period (mode 1 and mode 3) as shown in Figure 4.3 and Figure 4.5. This explains why HBZVR-D has relatively higher efficiency than those of dc-decoupling topologies.

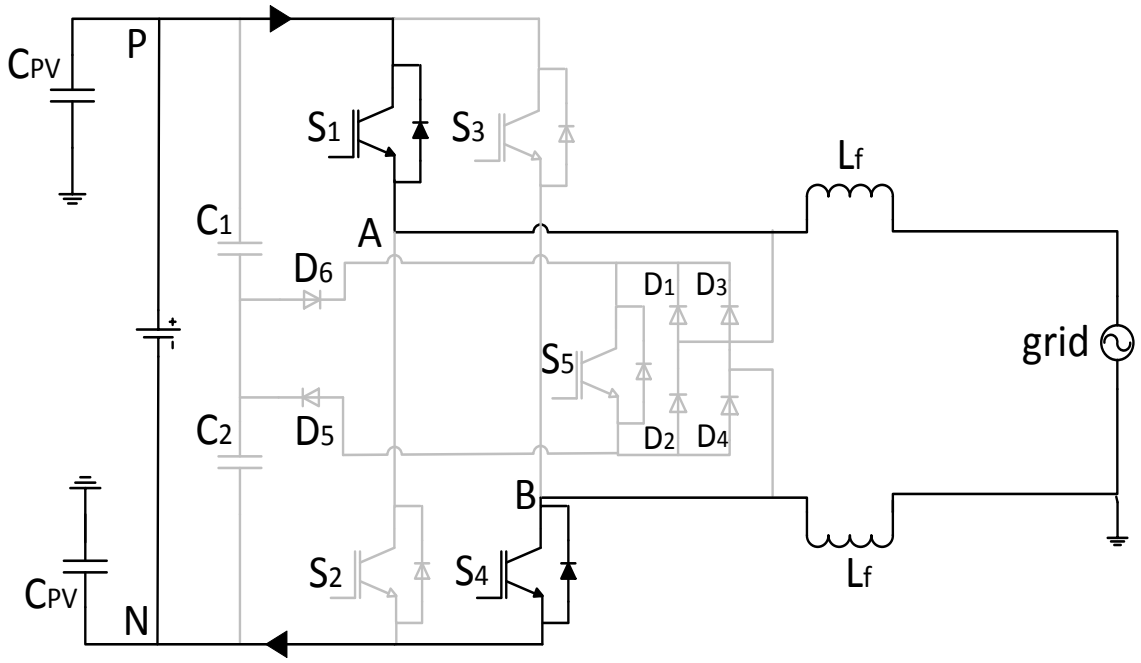


Figure 4.3: Mode 1 – conduction mode during positive half cycle.

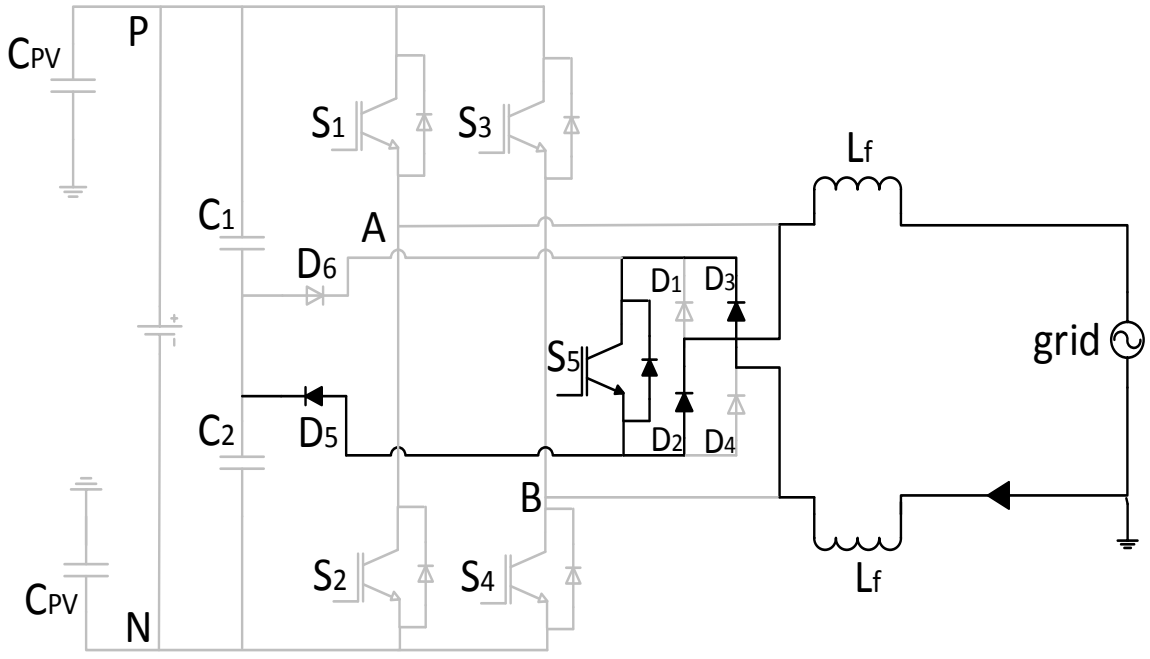


Figure 4.4: Mode 2 – freewheeling mode during positive half cycle.

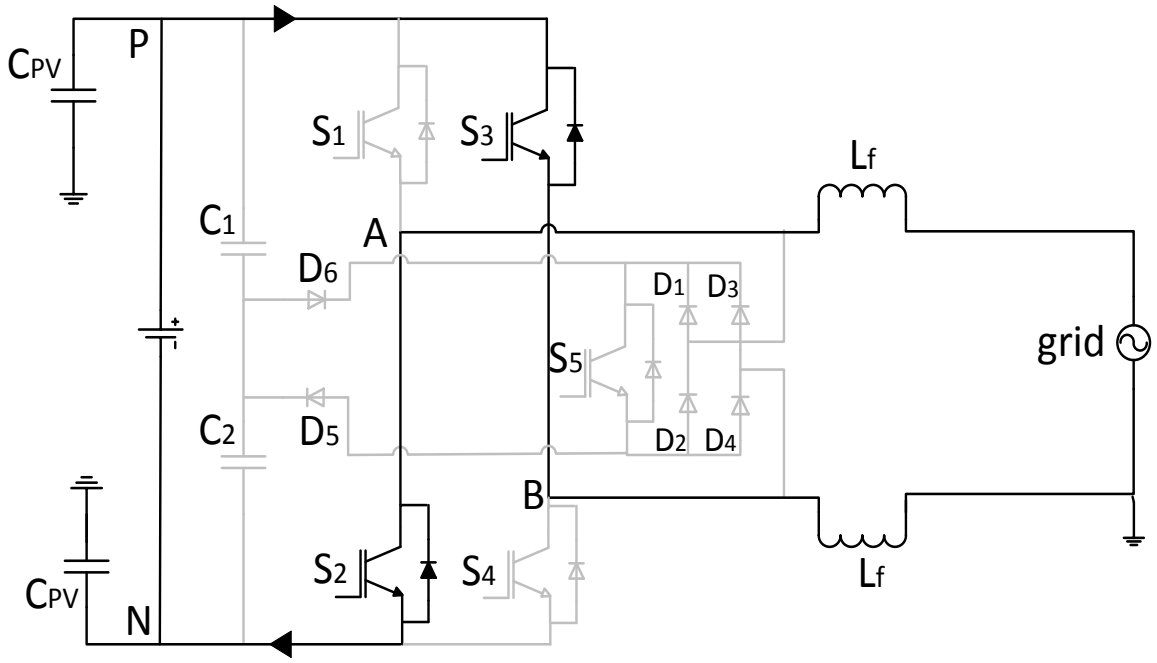
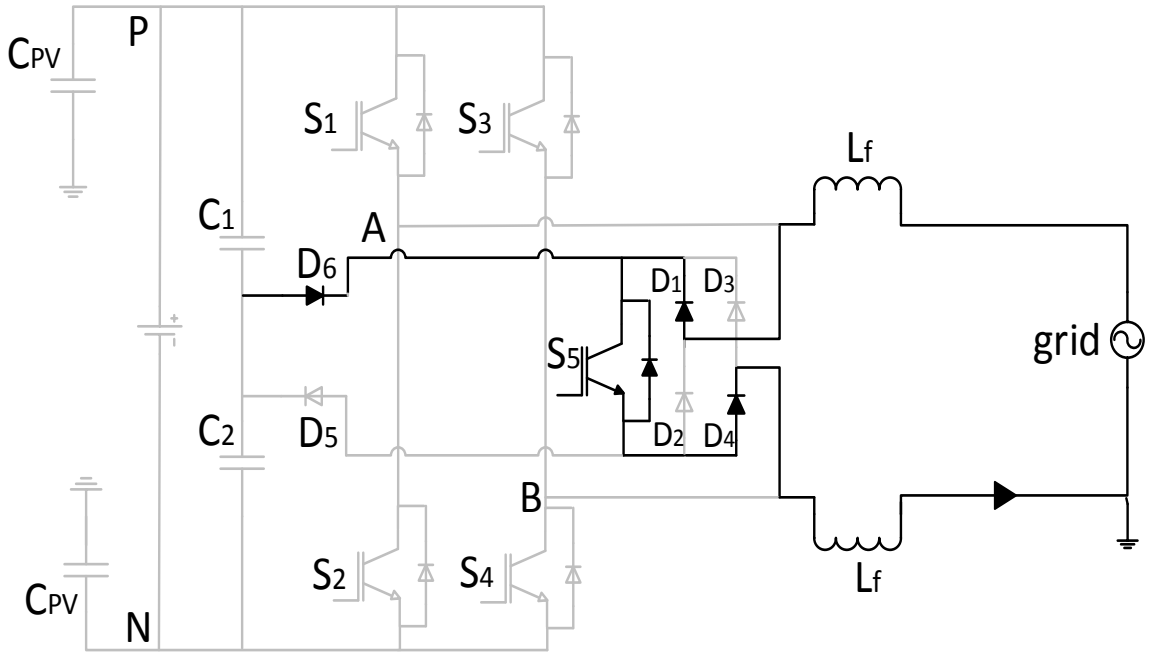


Figure 4.5: Mode 3 – conduction mode during negative half cycle.



(d)

Figure 4.6: Mode 4 – freewheeling mode during negative half cycle.

4.4 Operation Principles of Improved Clamping Branch

During the freewheeling period, S_5 is ON, connecting point A and B. Freewheeling path voltage V_{FP} can be defined as $V_{FP} = V_{AN} \approx V_{BN}$, since the voltage drops across diodes and *S*5 are small compared to V_{DC}. There are two possible modes of operation (mode 2 and mode 4) depending on whether D_5 or D_6 is forward biased. When V_{FP} is greater than $V_{DC}/2$, D_5 is forward biased and D_6 is reversed biased. Current flows from the freewheeling path to the midpoint of the dc-link via the clamping diode D_5, as shown in Figure 4.4, which completely clamps the V_{FP} to $V_{DC}/2$. On the other hands, when the V_{FP} is less than $V_{DC}/2$, D_6 is forward biased and D_5 is reversed biased. As shown in Figure 4.6, current freewheels from the midpoint of the dc-link to the freewheeling path via the added clamping diode D_6, to increase the V_{FP} to $V_{DC}/2$. It should be noted that during the dead time between the conduction period and freewheeling period, the freewheeling path is not well-clamped and the CMV can be oscillating with the grid voltage. Nevertheless, with proper selection of dead time, this effect can be minimized.

In HBZVR, the clamping branch consists of D_5 only. Thus, the clamping of the freewheeling path is limited only for the period when V_{FP} is more than $V_{DC}/2$. When V_{FP} is less than $V_{DC}/2$, the clamping branch does not function because D_5 is reversed biased. During such condition, the CMV in HBZVR will oscillate, causing the flow of the leakage current. This setback is rectified by adding a fast-recovery diode D_6 in the proposed HBZVR-D topology. With both D_5 and D_6, the improved clamping branch guarantees the complete clamping of the CMV to $V_{DC}/2$ throughout the freewheeling period. As a result, the leakage current, which is very much dependent on the CMV, is completely eliminated.

4.5 Matlab Simulation

Simulations are carried out using Matlab/ Simulink to investigate the operation and the performance of the PV systems. Figure 4.7 to Figure 4.12 indicate the simulation setup for the all the discussed topologies. The PV systems comprise of a full-bridge inverter with either dc- or ac-decoupling branch, current controller and pulse generator.

All the simulations are carried out based on the same parameters (Bo et al., 2012; Huafeng et al., 2011; Kerekes et al., 2011). The PV array is simulated with dc voltage source of 400 V. The stray capacitance (C_{PV}) is modeled with two capacitors of 100 nF, each connected to the PV terminal and the ground. The ground resistance (R_G) is 11 Ω. The filter is made up of two inductors (L); each has a value of 3 mH. The grid line to neutral voltage is 230 V (rms) with frequency (f) of 50 Hz. The switching frequency (f_s) is 10 kHz.

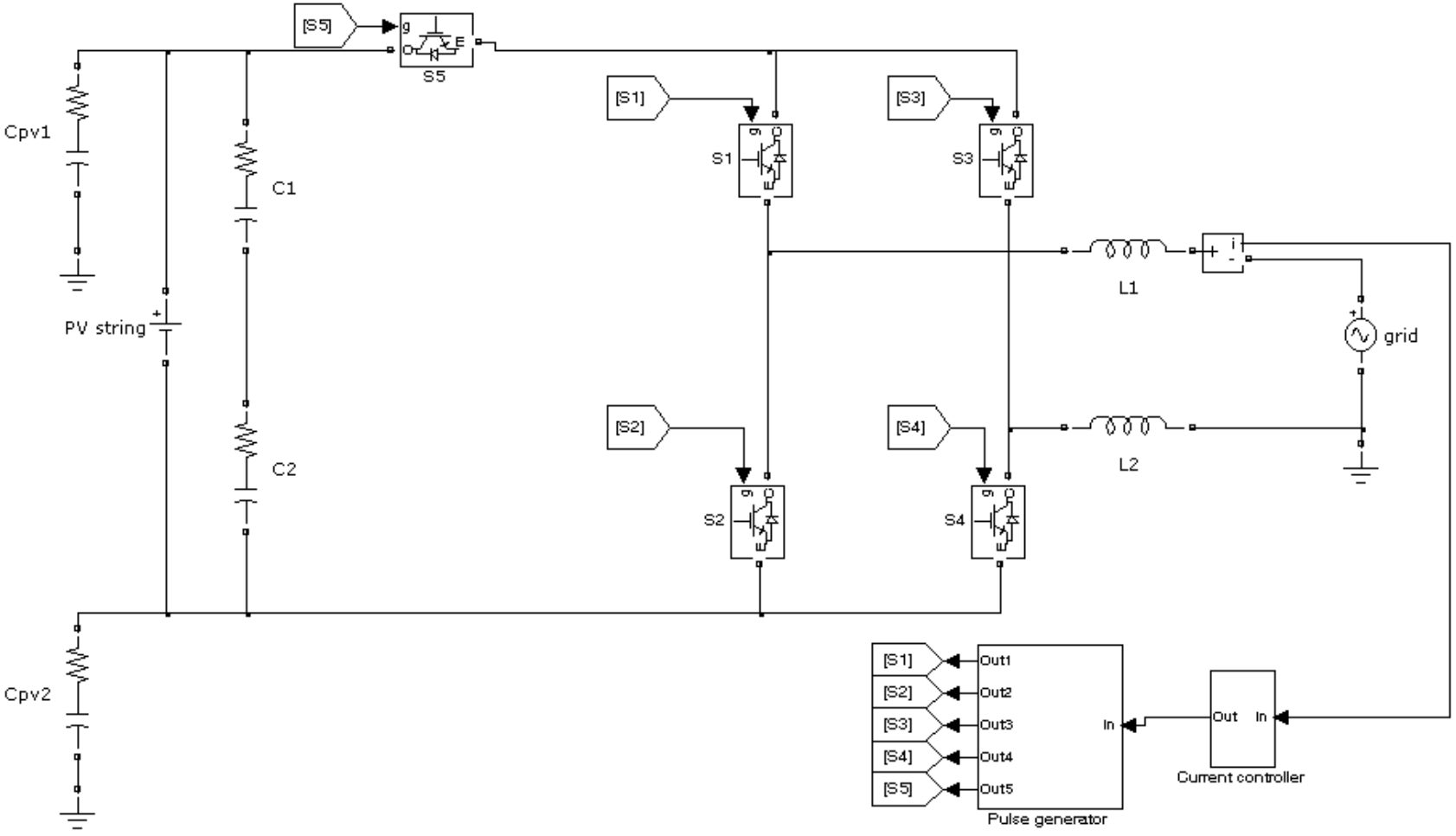


Figure 4.7: Simulation setup for H5 topology.

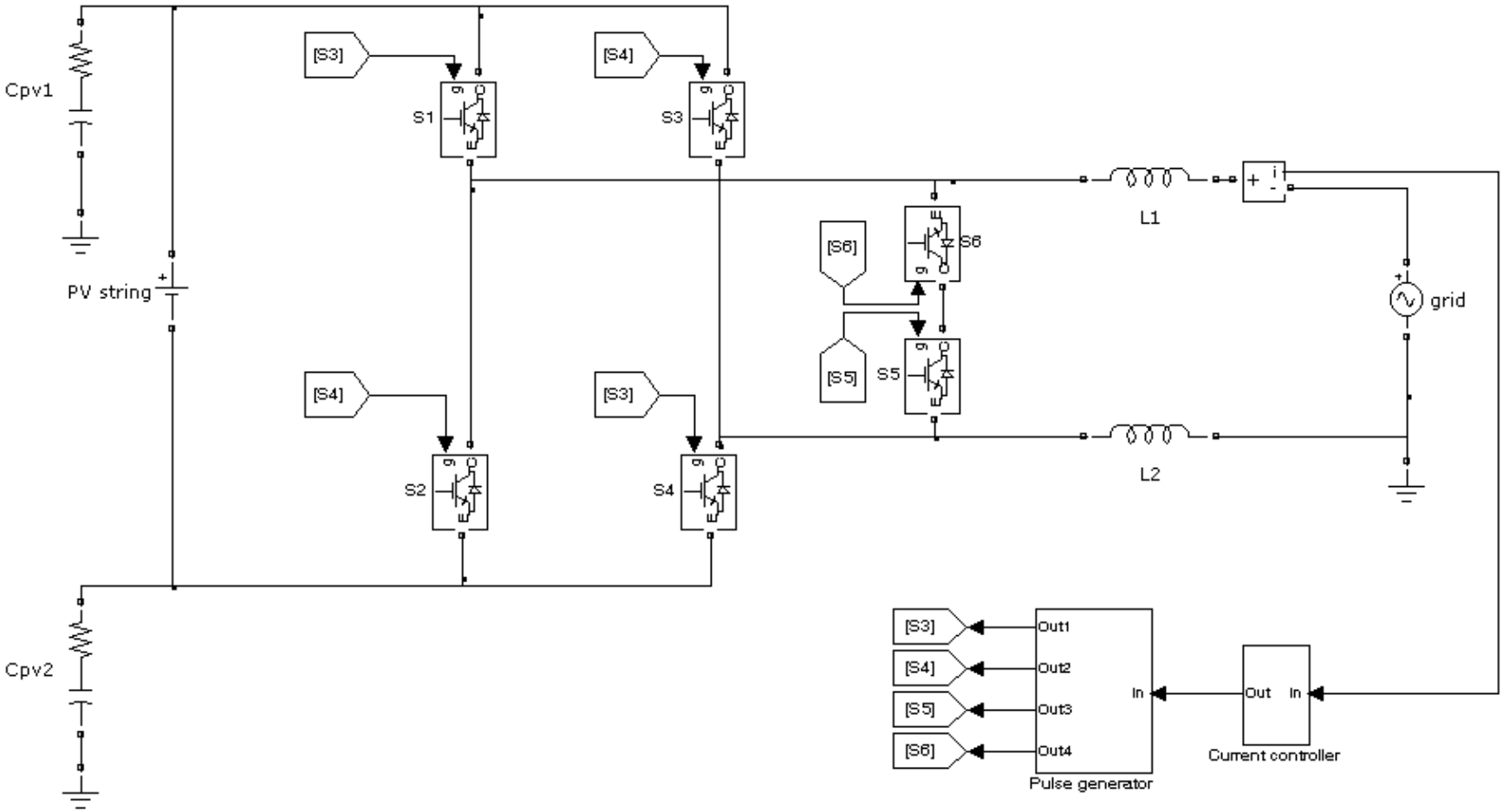


Figure 4.8: Simulation setup for HERIC topology.

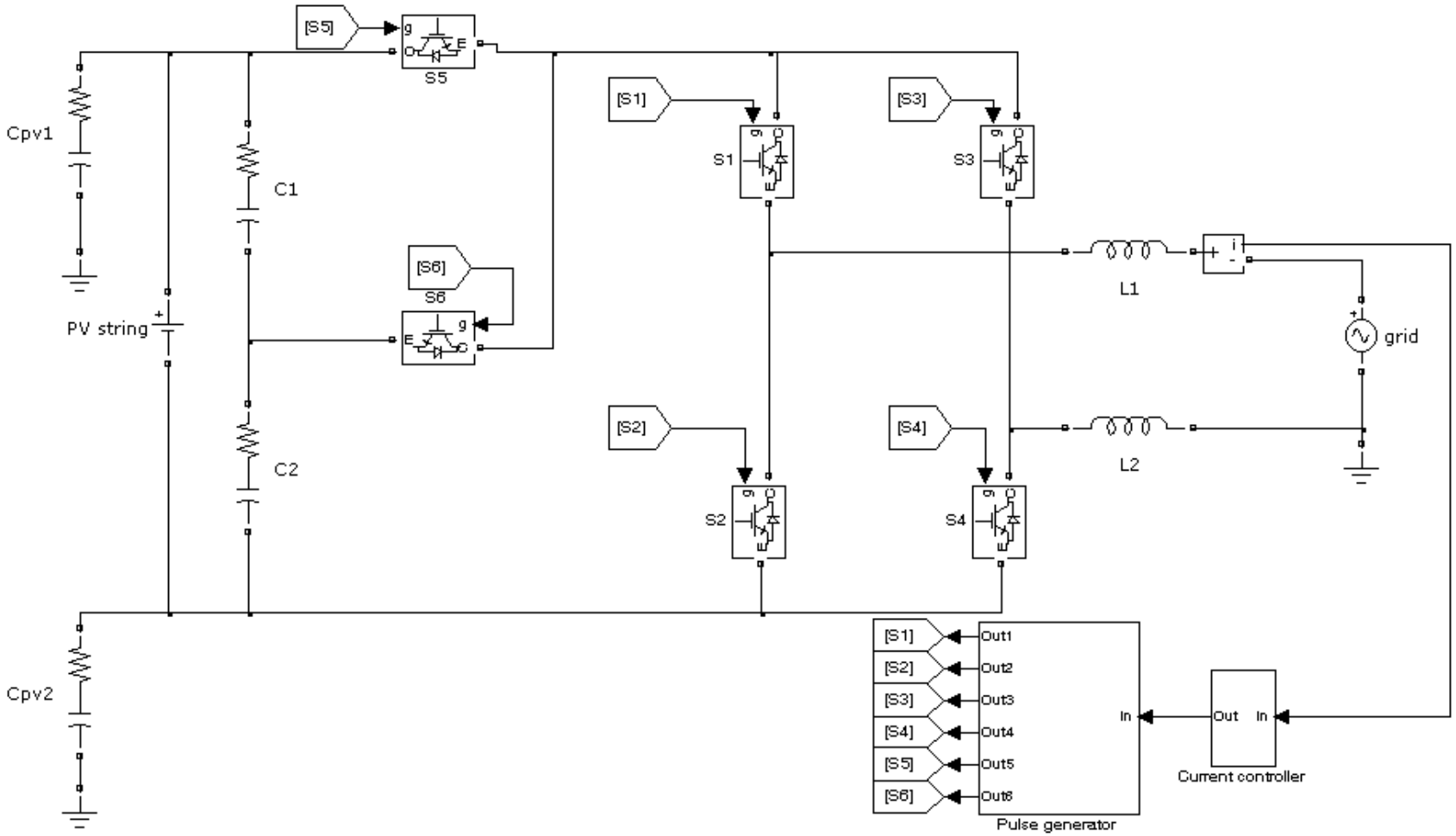


Figure 4.9: Simulation setup for oH5 topology.

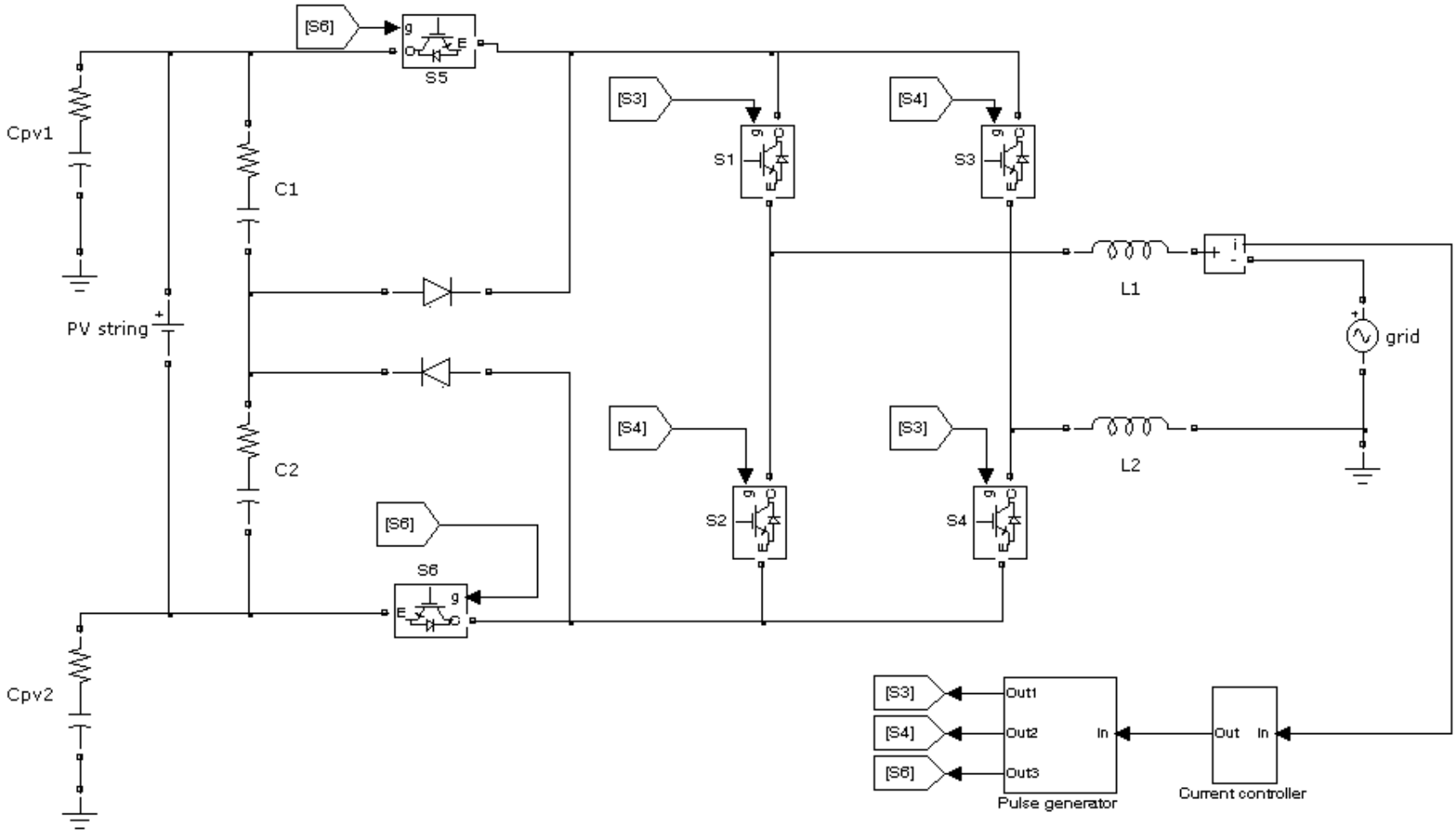


Figure 4.10: Simulation setup for H6 topology.

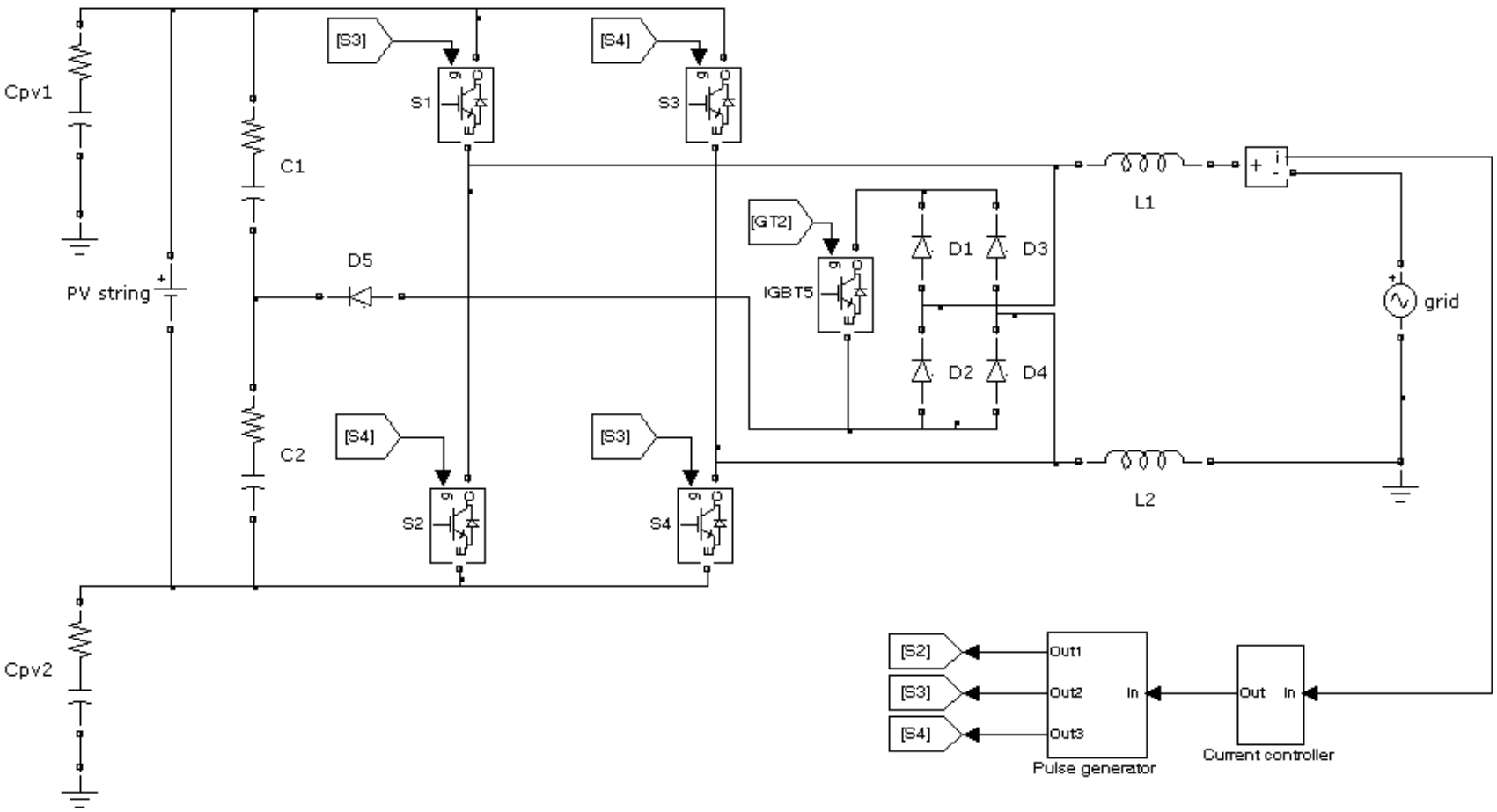


Figure 4.11: Simulation setup for HBZVR topology.

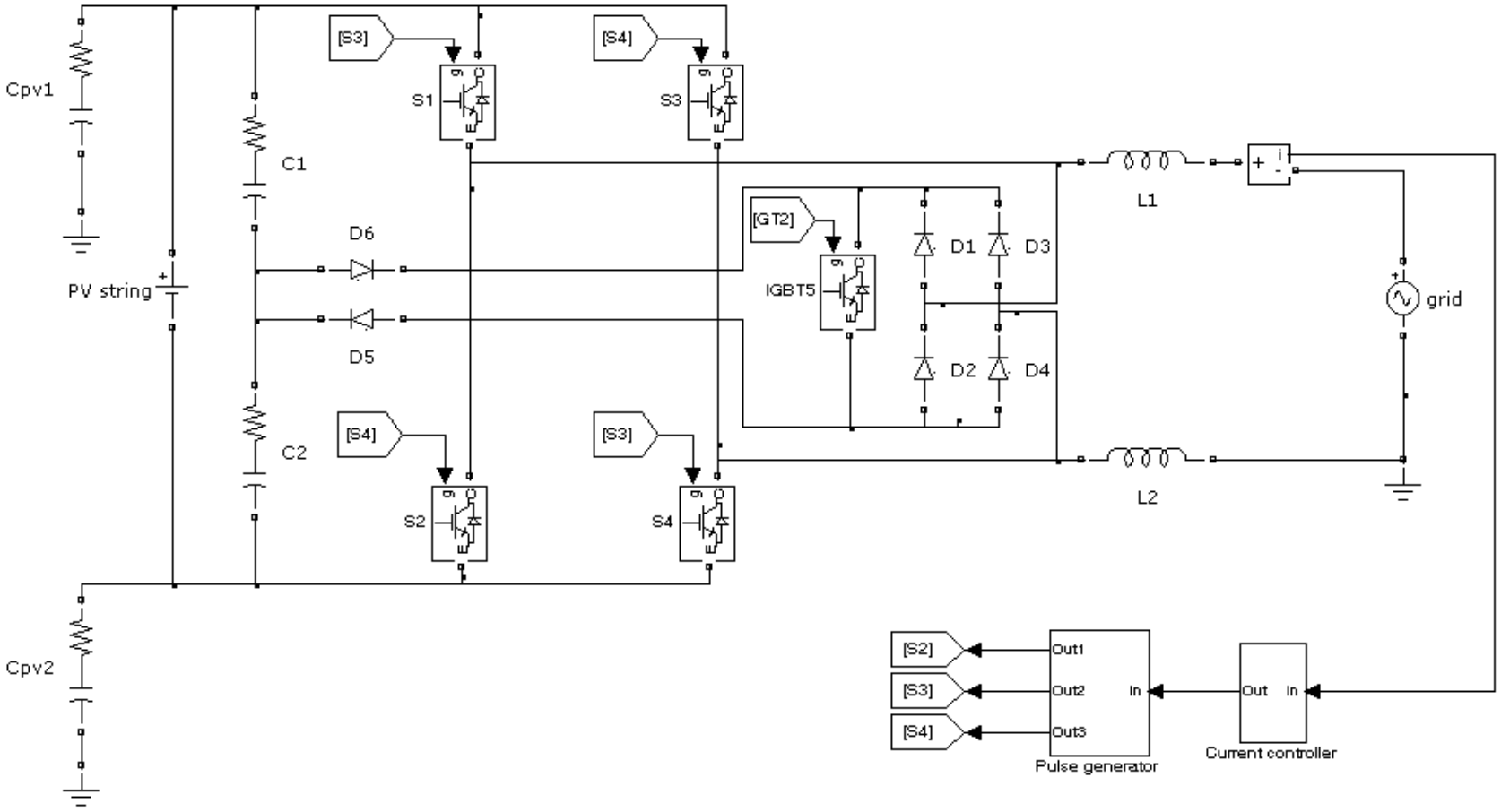


Figure 4.12: Simulation setup for HBZVR-D topology.

4.5.1 Output Performance

Figure 4.13 to Figure 4.18 show the simulations of line-to-line output voltage and grid current characteristic for various topologies. It can be observed that all the topologies share one common characteristic. They are generating three-level line-to-line output voltage, i.e., $+V_{DC}$, 0 and $-V_{DC}$. As compared to bipolar voltage which reads $+V_{DC}$ to $-V_{DC}$, the effective switching frequency is doubled and the voltage amplitude is halved in each PWM cycle. Undoubtedly, the harmonic content of the output voltage waveform is reduced. As a result, smooth sinusoidal grid current with very low current ripples is generated as indicated in Figure 4.13 to Figure 4.18 and smaller filter inductors are required.

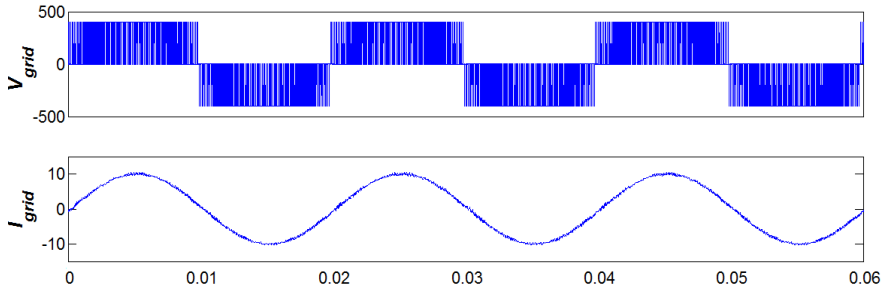


Figure 4.13: Line-to-line output voltage (top) and grid current (bottom) for H5.

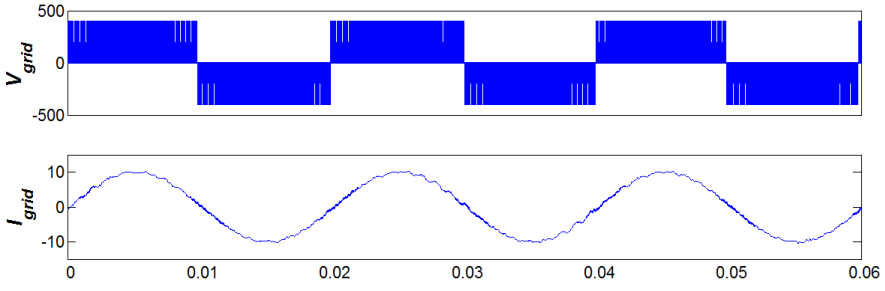


Figure 4.14: Line-to-line output voltage (top) and grid current (bottom) for HERIC.

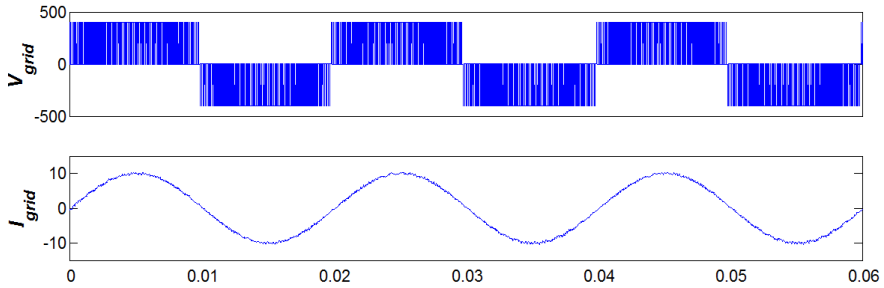


Figure 4.15: Line-to-line output voltage (top) and grid current (bottom) for oH5.

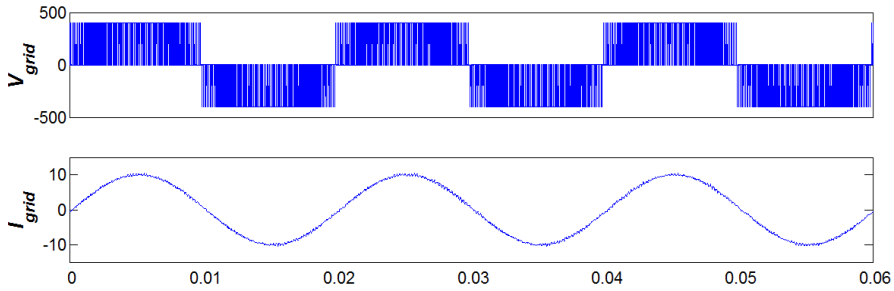


Figure 4.16: Line-to-line output voltage (top) and grid current (bottom) for H6.

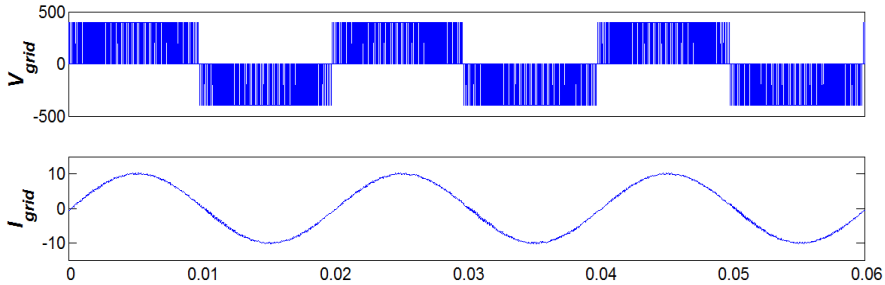


Figure 4.17: Line-to-line output voltage (top) and grid current (bottom) for HBZVR.

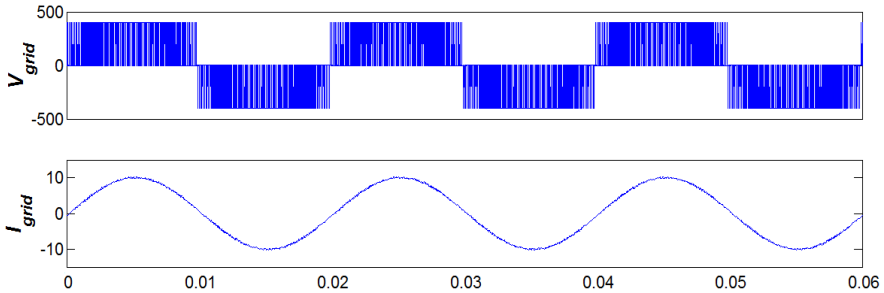


Figure 4.18: Line-to-line output voltage (top) and grid current (bottom) for proposed HBZVR-D.

4.5.2 Common-Mode Behavior

As shown in Figure 4.19, large oscillations with the magnitude up to 100 V are observed in both V_{AN} and V_{BN} for H5 topology. Moreover, the CMV is not constant and is oscillating with the magnitude up to 200 V. Therefore, the leakage current is not completely eliminated. The common-mode behavior of H5 topology can be studied in detail with microscopic waveform as shown in Figure 4.21. It is clearly shown that V_{AN} and V_{BN} are well clamped to V_{DC} and 0 during the conduction period. Nevertheless, during the freewheeling period, both V_{AN} and V_{BN} are floating and hence CMV is not constant. Practically, this proves that the galvanic isolation and modulation technique alone are not able to generate constant CMV.

HERIC topology shares the similar common-mode performance as H5 topology. Although the switches commutate diagonally to generate constant CMV, the CMV is still floating. As shown in Figure 4.22, V_{AN}, V_{BN} and the CMV are oscillating. Therefore, the leakage current (Figure 4.24) cannot be simply eliminated by the galvanic isolation as well as modulation techniques.

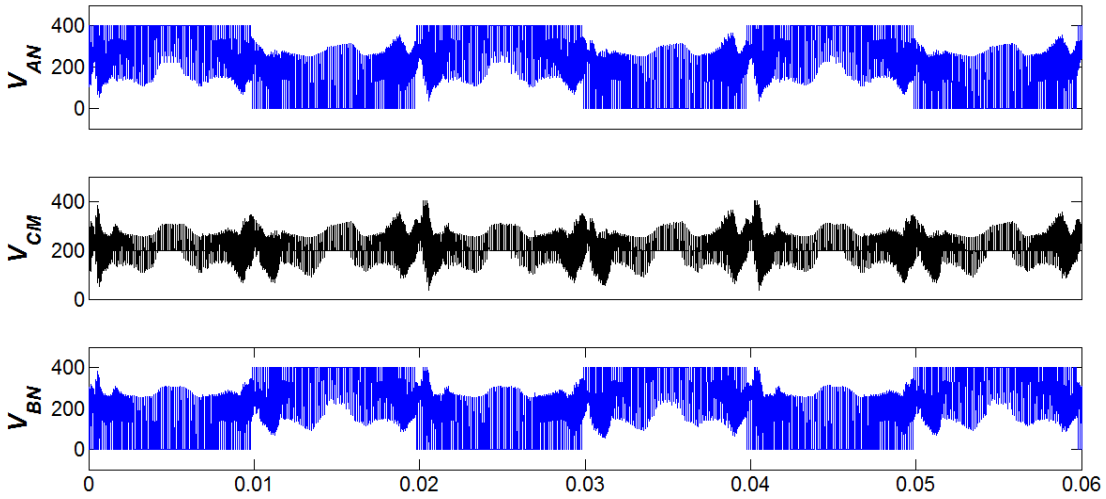


Figure 4.19: V_{AN} (top), CMV (middle), and V_{BN} (bottom) for H5 topology.

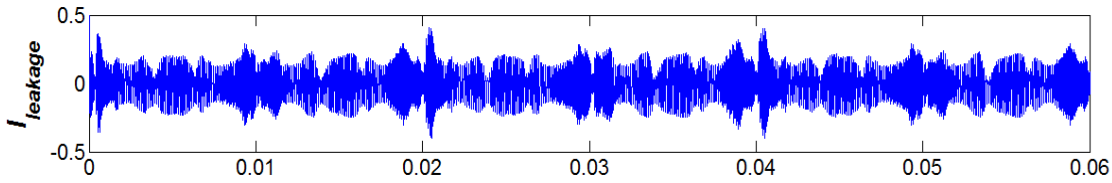


Figure 4.20: Leakage current for H5 topology.

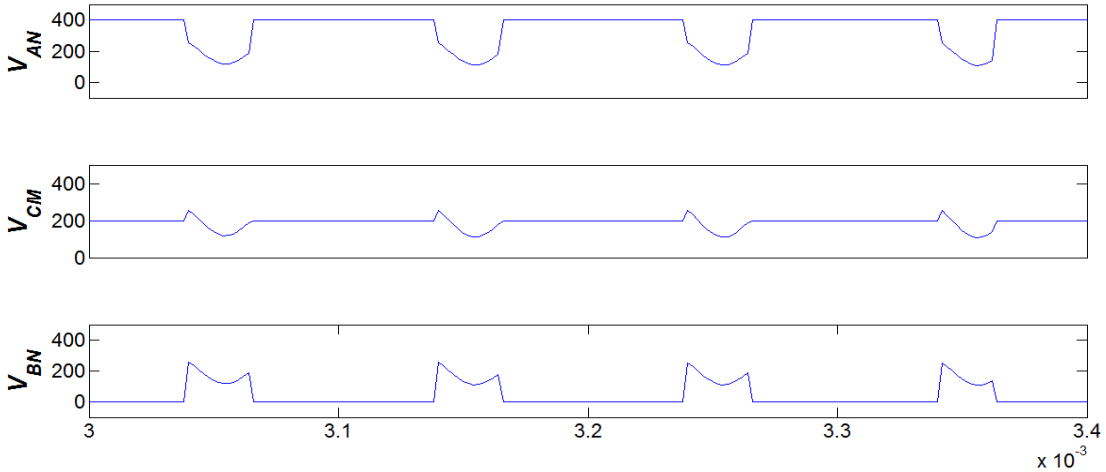


Figure 4.21: Microscopic waveform - V_{AN} (top), CMV (middle), and V_{BN} (bottom) for H5 topology.

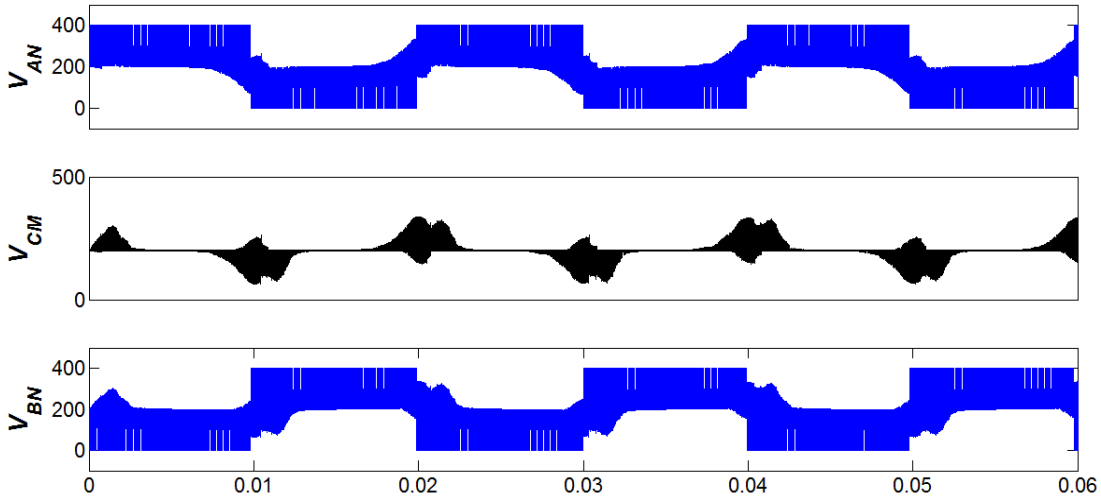


Figure 4.22: V_{AN} (top), CMV (middle), and V_{BN} (bottom) for HERIC topology.

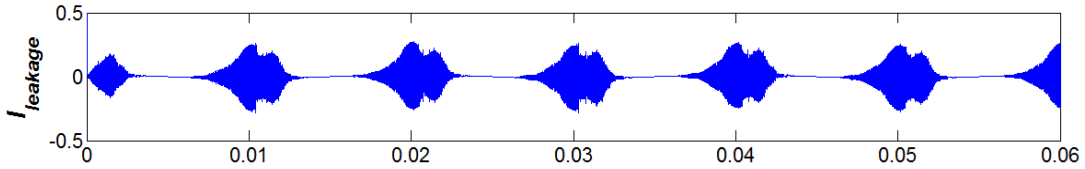


Figure 4.23: Leakage current for HERIC topology.

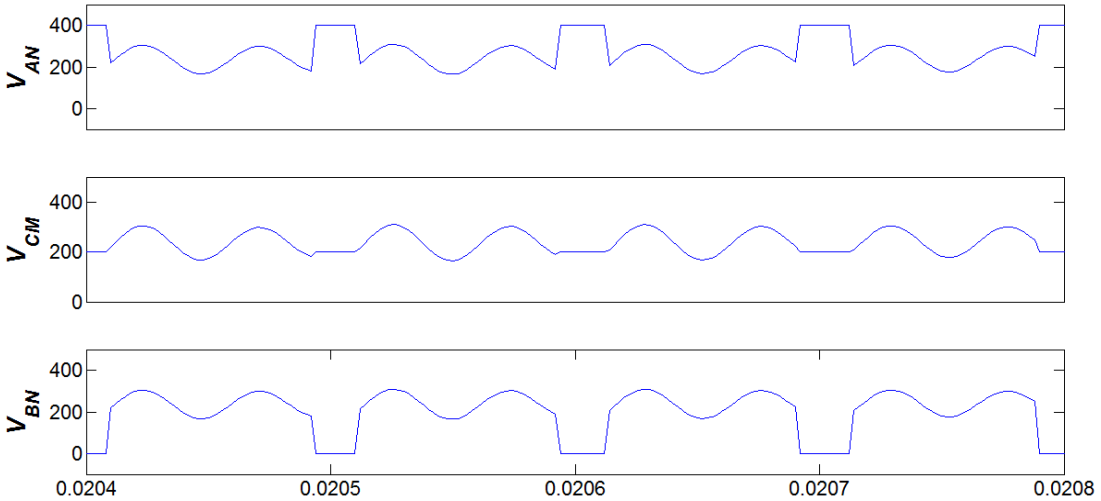


Figure 4.24: Microscopic waveform - V_{AN} (top), CMV (middle), and V_{BN} (bottom) for HERIC topology.

The abovementioned issues have been solved by the use of clamping branch in oH5 and H6 topologies. As shown in Figure 4.25 and Figure 4.27, V_{AN} and V_{BN} are totally complementary to one another and the CMV is completely constant at 200 V in both conduction period and freewheeling period. As a result, leakage current is completely eliminated in both oH5 and H6 topologies as shown in Figure 4.26 and Figure 4.28 respectively.

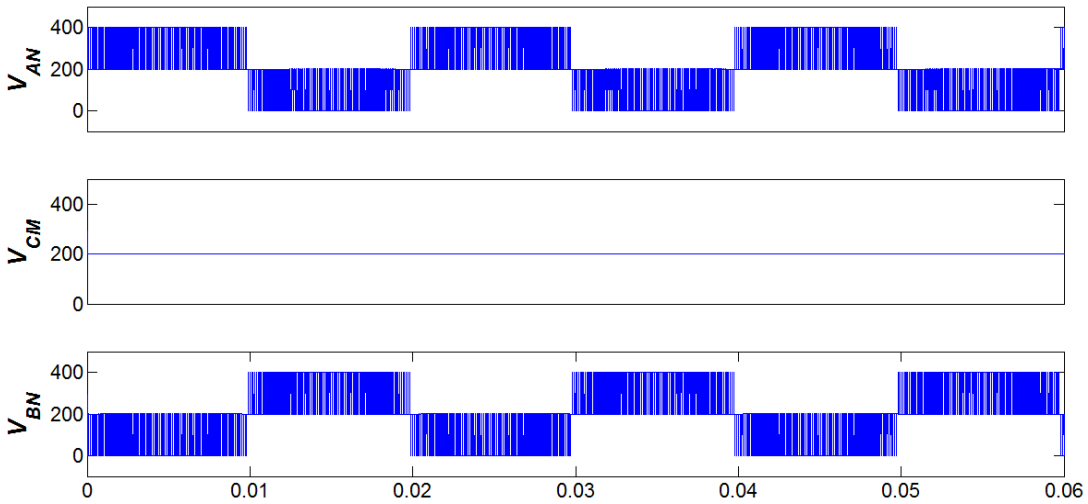


Figure 4.25: V_{AN} (top), CMV (middle), and V_{BN} (bottom) for oH5 topology.

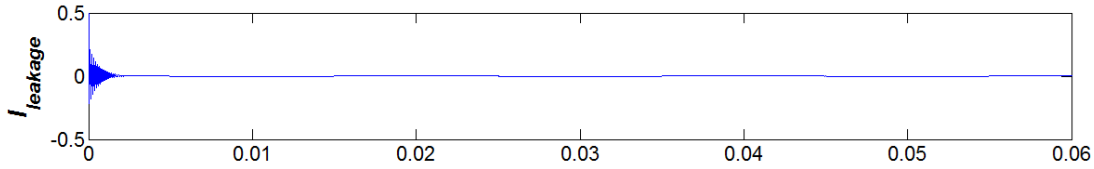


Figure 4.26: Leakage current for oH5 topology.

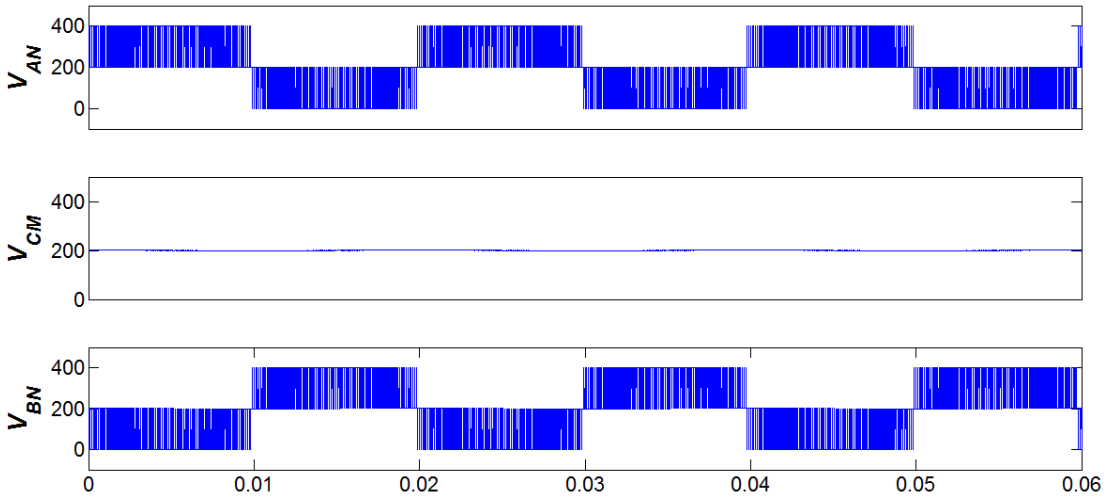


Figure 4.27: V_{AN} (top), CMV (middle), and V_{BN} (bottom) for H6 topology.

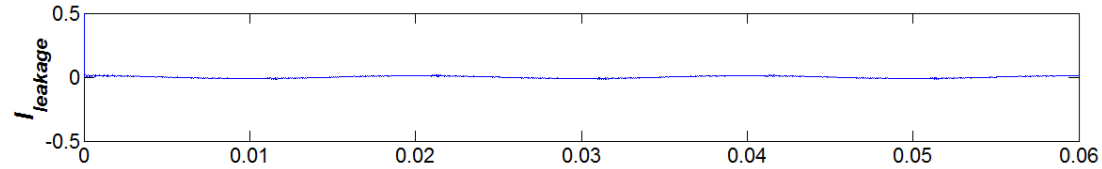


Figure 4.28: Leakage current for H6 topology.

Although HBZVR employs CMV clamping technique, it is mentioned earlier that the clamping branch does not perform satisfactorily. As shown in Figure 4.29, voltage spikes with magnitudes up to 150 V are observed in the CMV. As a result, the leakage current is not eliminated. The common-mode behavior is the same as those of galvanic isolation family.

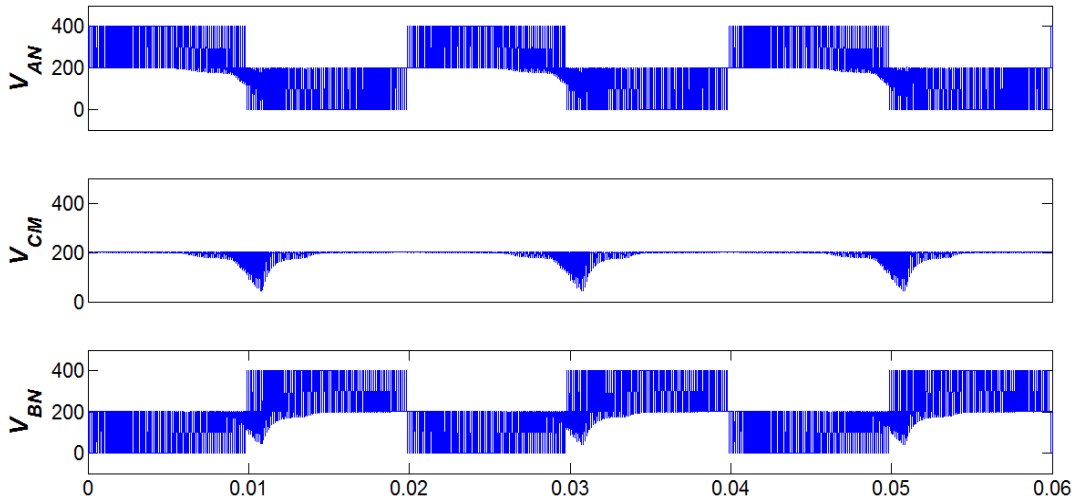


Figure 4.29: V_{AN} (top), CMV (middle), and V_{BN} (bottom) for HBZVR topology.

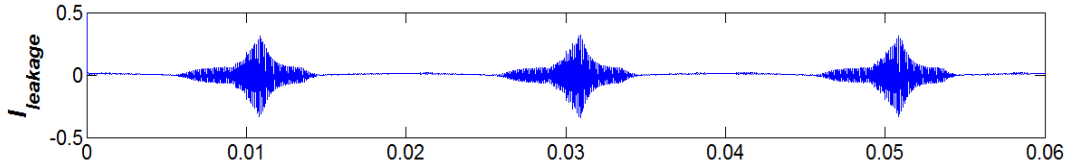


Figure 4.30: Leakage current for HBZVR topology.

Proposed HBZVR-D has improved the performance of the clamping branch as shown in Figure 4.31. Obviously, the CMV is clamped at 200 V throughout the operation period. V_{AN} and V_{BN} are totally complementary to one another. Thus, leakage current can be eliminated as shown in Figure 4.32.

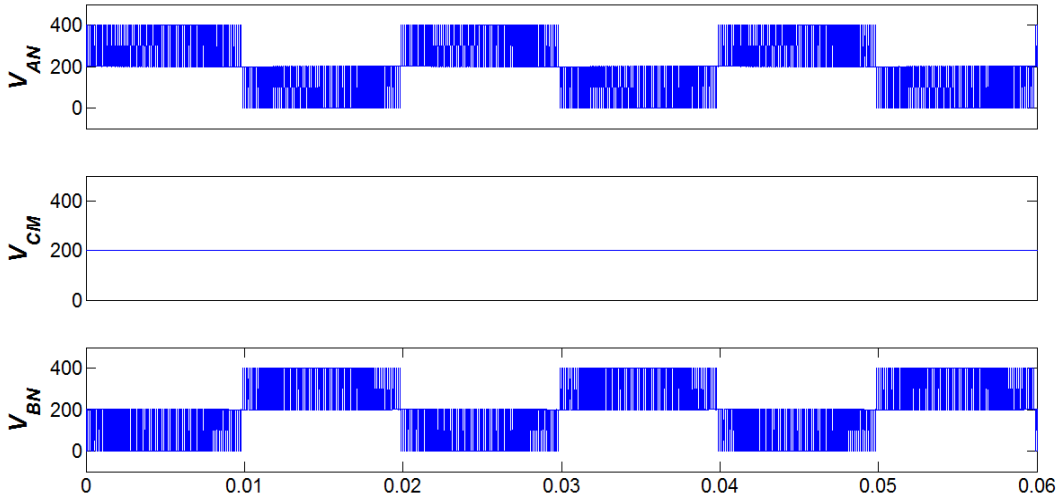


Figure 4.31: V_{AN} (top), CMV (middle), and V_{BN} (bottom) for HBZVR-D topology.

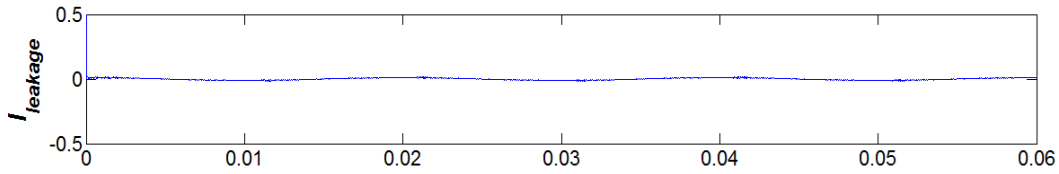


Figure 4.32: Leakage current for HBZVR-D topology.

4.5.3 Losses Analysis

The loss analysis is simulated via thermal module in PSIM. The simulations for all topologies are carried out based on the device parameters as listed in Table 4.1.

Table 4.1: Parameters for losses simulation

Parameter	Value
Device	GT50J325
Frequency	50 Hz
Saturation voltage, $V_{CE(SAT)}$	2V
Forward voltage, V_F	2.5V
Junction temperature, $T_{j(max)}$	150ºC
Turn-on energy losses, E_{ON} @ V_{DC} = 300V	1.30mJ
Turn-off energy losses, E_{OFF} @ V_{DC} = 300V	1.34mJ
Pcond_Q calibration factor	1
Psw_Q calibration factor	1
Pcond_D calibration factor	1
Psw_D calibration factor	1

There are two major types of losses in PV systems; i.e., conduction losses and switching losses. Practically, when the IGBT conducts, there is certain voltage drop across the switch, namely saturation voltage ($V_{CE(SAT)}$). Hence, the conduction losses of IGBT (P_{CON_IGBT}) are calculated by (Baojian et al., 2013; Vazquez et al., 2009; Wensong et al., 2011)

$$P_{CON\_IGBT} = V_{CE(SAT)} \bullet I_C \tag{4.4}$$

where I_C is the on-state current.

Similarly, when the freewheeling diode conducts, the forward voltage (V_F) drop across the diode which results in conduction losses which are calculated by (Baojian et al., 2013; Vazquez et al., 2009; Wensong et al., 2011)

$$P_{CON\_D} = V_F \bullet I_F \tag{4.5}$$

where I_F is the freewheeling current.

Switching losses are calculated by

$$P_{SW\_ON} = E_{ON} \bullet f \bullet V_{DC} / V_{DC\_DATASHEET} \tag{4.6}$$

$$P_{SW\_OFF} = E_{OFF} \bullet f \bullet V_{DC} / V_{DC\_DATASHEET} \tag{4.7}$$

where P_{SW_ON} and P_{SW_OFF} are the losses during turn on and turn off respectively, E_{ON} and E_{OFF} are the turn-on and turn-off energy losses of the IGBT, V_{DC} is the actual dc bus voltage, and $V_{DC\_DATASHEET}$ is the dc bus voltage in the E_{ON} and E_{OFF} characteristic of the datasheet. The total switching losses are

$$P_{SW\_IGBT} = P_{SW\_ON} + P_{SW\_OFF} \tag{4.8}$$

The total losses (where $P_{\_T}$) are

$$P_{\_T} = P_{CON\_IGBT} + P_{SW\_IGBT} \tag{4.9}$$

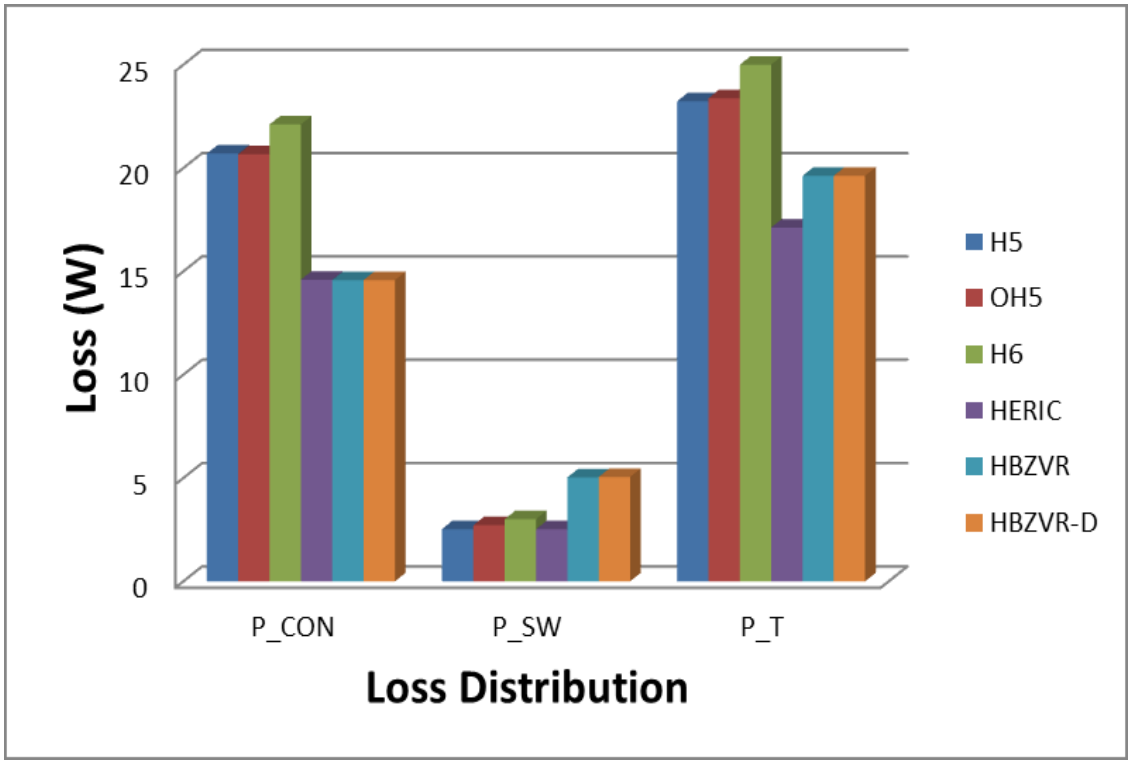


Figure 4.33: Simulated losses results at 1 kW prototype.

Figure 4.33 shows the losses results for various topologies. H5 and oH5 add one additional switch whereas H6 adds two additional switches and diodes into the conduction path. This explains why all the dc-decoupling topologies (H5, oH5 and H6) have higher losses as compared to the ac-decoupling topologies (HERIC, HBZVR, HBZVR-D). H6 topology yields the highest device losses due to excessive components that are added into the conduction path. As expected, HERIC topology has the lowest device losses. HBZVR and HBZVR-D have slightly higher losses than HERIC but they are still much lower than those of the dc-decoupling family.

Obviously, the conduction losses are the main contributor as shown in Figure 4.33. The influence of the dc-link voltage on the switching losses is very small because the same dc-link voltage is applied to all the topologies. The influence of the filter inductor current ripples is considered negligible since all the topologies are generating three-level unipolar output voltage.

It is worth noting that the conduction losses can be further reduced via proper choice of power electronics switches, such as using MOSFETs instead of IGBTs (Bin et al., 2013; Wensong et al., 2011). However, MOSFETs implementation is only limited to certain topologies because of the slow reverse-recovery of the body diode. For HERIC, HBZVR and HBZVR-D, all the switches can be replaced by MOSFETs because the body diodes of MOSFETs are not utilized. This means the efficiency of these topologies can be improved further. In other words, ac-decoupling topologies are good solutions for high-efficiency applications. Nevertheless, the selection of switches is beyond the scope of this paper, and hence not discussed further. For this paper, IGBTs are used in all the topologies.

Therefore, ac-decoupling family is more preferable in terms of efficiency. This is because the ac-bypass branch is isolated and independent from the conduction path. It functions only as a freewheeling path and this decreases the conduction losses significantly. The losses analysis and study is useful for the engineer to choose and design the high-efficiency transformerless topology.

4.6 Experimental Results

In order to verify the theoretical simulation results for different topologies, a universal inverter has been built using the same components as shown in Figure 4.34. S_1–S_4 are the switches of conventional full-bridge inverter. “DC-bypass 1” and “DC-bypass 2” are the corresponding dc-decoupling branches of H5, H6 and oH5 while “AC-bypass” belongs to those of HBZVR and proposed HBZVR-D. “Clamping Branch” is the CMV clamping branch of oH5 and the proposed HBZVR-D.

Table 4.2 lists the inverter specifications. Resistor loads are used in replacement of grid (Kerekes et al., 2011). Even though this increases the impedance of the leakage current path and changes the magnitude of the leakage current, it does not affect the validity of the comparisons, since the same resistor loads are used in all topologies. All the control algorithms are implemented in Texas Instrument’s TMS320F2812 DSP.

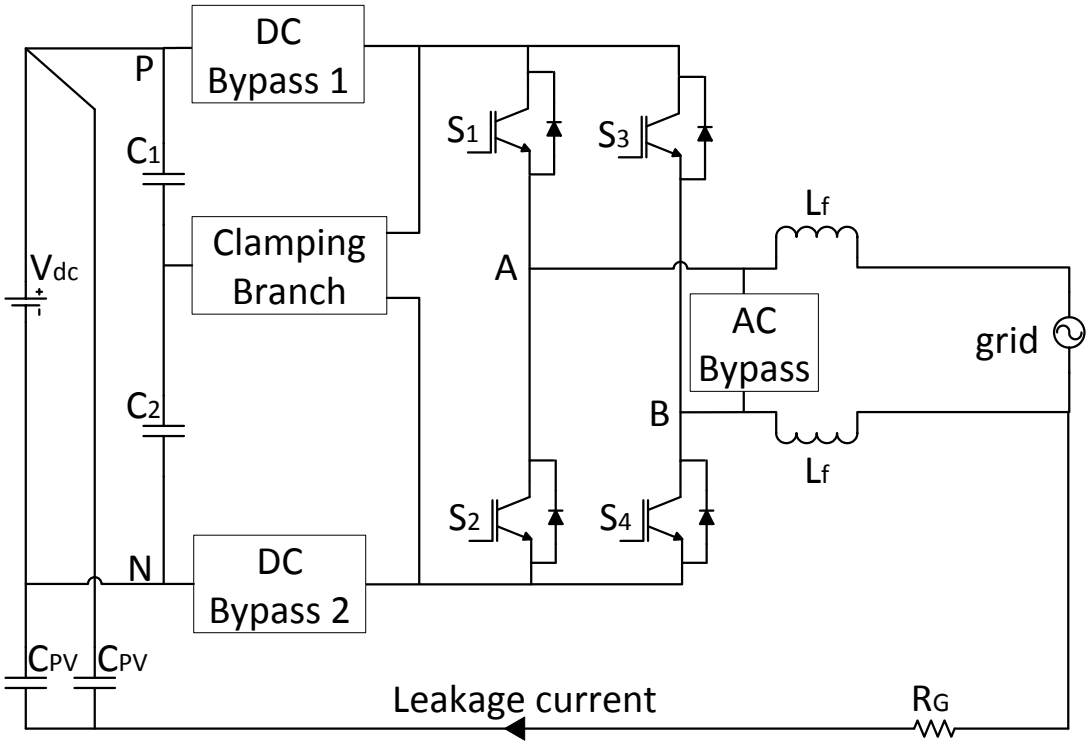


Figure 4.34: Experimental setup.

Table 4.2: Parameters of universal inverter

Parameter	Value
Input voltage	400 V_{DC}
Load	100 ohm
Rated power	1 kW
Switching frequency	10 kHz
Dead time	2.5 us
DC-link capacitors	2200 uF, V_{DC}=400V
IGBT	GT50J325 V_{CE}=600V, I_C= 60A
Fast-recovery diodes	RHRP30120 V_{RR}=1200V, I=30A
Filter inductors	3 mH
Filter capacitors	6 nF
Stray capacitors	100 nF

Figure 4.35 to Figure 4.40 show the output performance for various topologies. Similar to the simulation results, all the topologies are generating unipolar output line to line voltage and sinusoidal load current. However, it is shown in Figure 4.38 and Figure 4.39 that the output voltage is not completely unipolar for HBZVR and HBZVR-D topologies respectively. Spike with magnitude up to 200 V are observed. This problem arises due to the dead time between the operation period and freewheeling period. At this moment, the freewheeling path is not yet functioning because the freewheeling switch, S_5, is still OFF. Current freewheels through the corresponding anti-parallel diodes of the switches and the load. This phenomenon will slightly increase the THD of the load current.

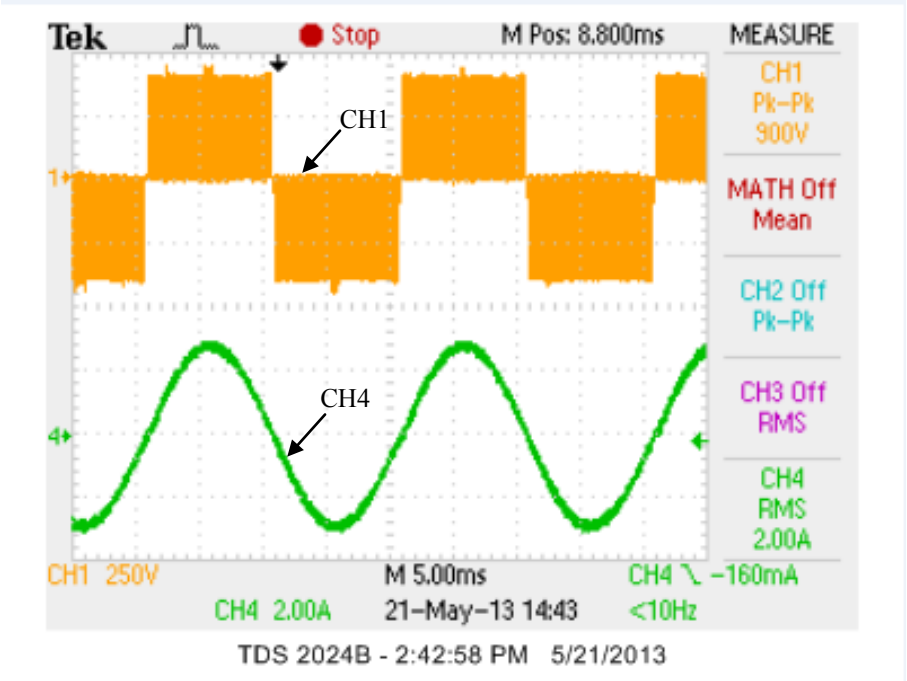


Figure 4.35: Output voltage (CH1) and output current (CH4) for H5.

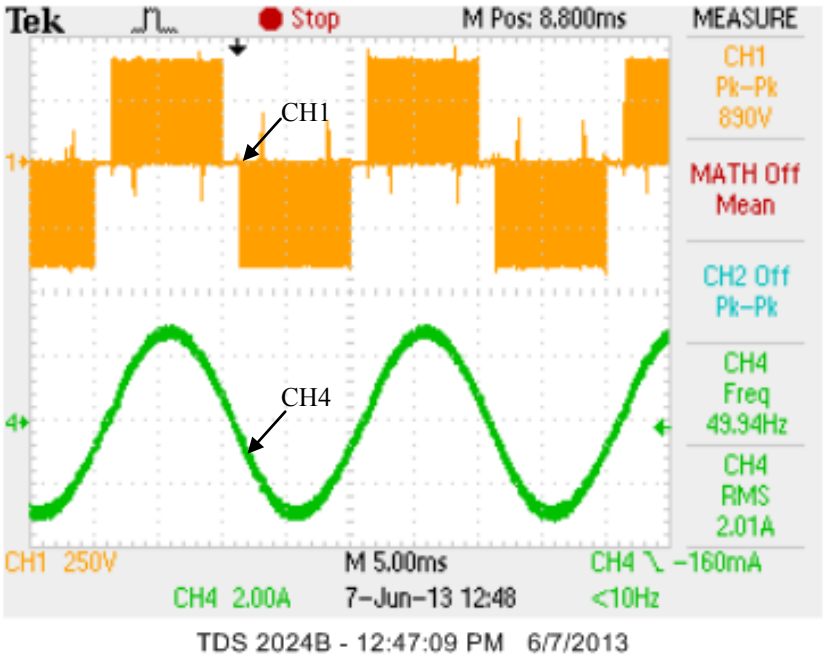


Figure 4.36: Output voltage (CH1) and output current (CH4) for HERIC.

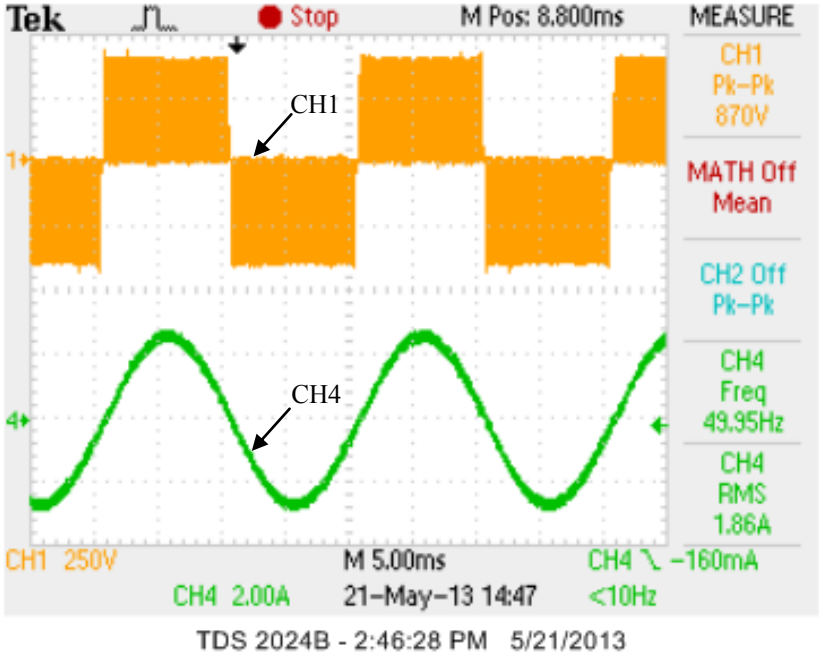


Figure 4.37: Output voltage (CH1) and output current (CH4) for H6.

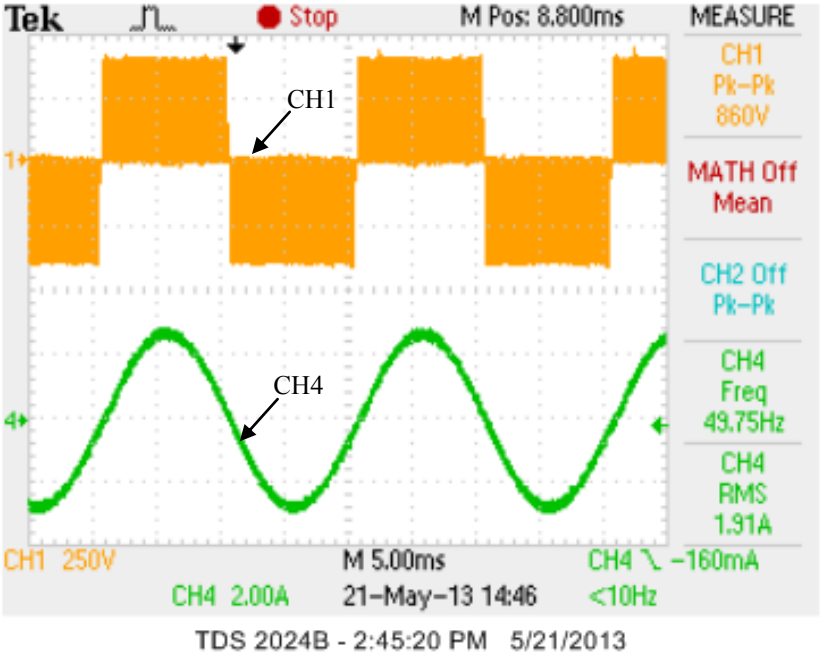


Figure 4.38: Output voltage (CH1) and output current (CH4) for oH5.

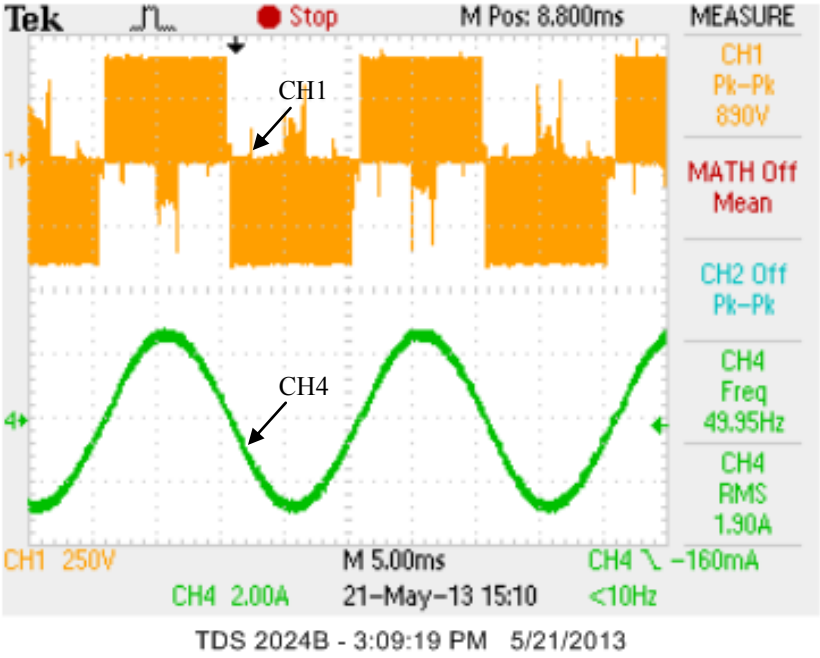


Figure 4.39: Output voltage (CH1) and output current (CH4) for HBZVR.

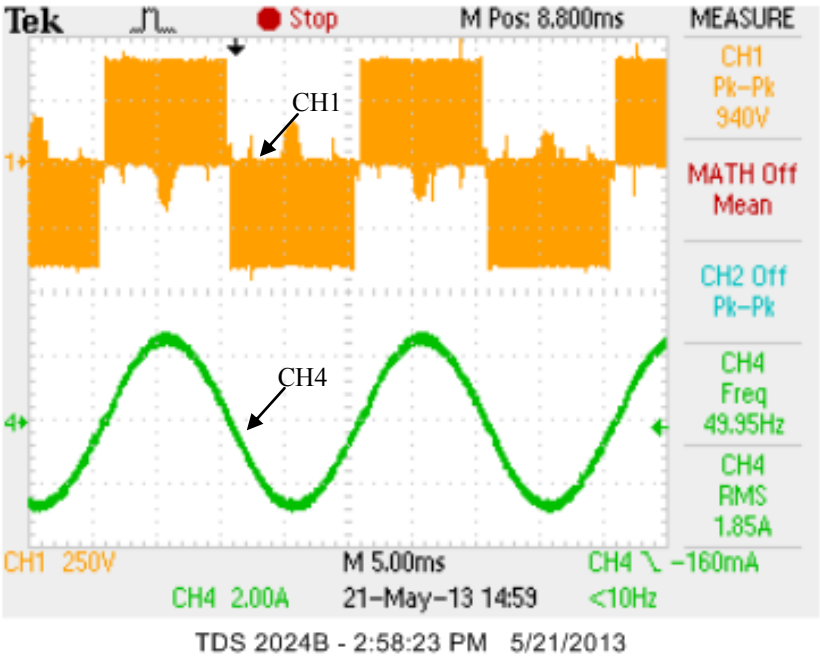


Figure 4.40: Output voltage (CH1) and output current (CH4) for HBZVR-D.

Figure 4.41 to Figure 4.46 show the common-mode behavior for different topologies. The magnitude of the leakage current for H5, HERIC, H6, oH5, HBZVR and HBZVR-D are 89.4, 84.3, 45.8, 44.9, 74.5, and 42.7 mA (rms) respectively. Even though, all of them meet the requirement of VDE 0126-1-1 standard, the proposed HBZVR-D topology gives the lowest leakage current. It is obvious that the leakage current of H5, HERIC and HBZVR are double of the H6, oH5 and HBZVR-D. This is mainly because the high frequency CMV is not completely clamped. As shown in Figure 4.41, Figure 4.42 and Figure 4.45, V_{AN}, V_{BN} and CMV of H5, HERIC and HBZVR are oscillating with the magnitude up to 200 V. Therefore, leakage currents are relatively higher. This proves that modulation technique alone fails to generate constant CMV. With clamping branch, the CMV is practically constant for oH5, H6 and HBZVR-D. This explains why the leakage currents are reduced significantly.

As shown in Figure 4.45, the CMV of the HBZVR is only well-clamped in one half cycle when V_{FP} is > $V_{DC}/2$. V_{AN}, V_{BN} and CMV are oscillating with high frequency when V_{FP} is < $V_{DC}/2$. This is due to the limitation of the clamping branch, where D_5 could only operate when V_{FP} is > $V_{DC}/2$ as explained earlier. The complete clamping has been provided by the additional diode, D_6, in the proposed HBZVR-D. As shown in Figure 4.46, the CMV is constant in both positive and negative half cycle. This explains why the leakage current is reduced to 42.7 mA (rms) which is half of that of HBZVR. The experimental results verified the theoretical analysis.

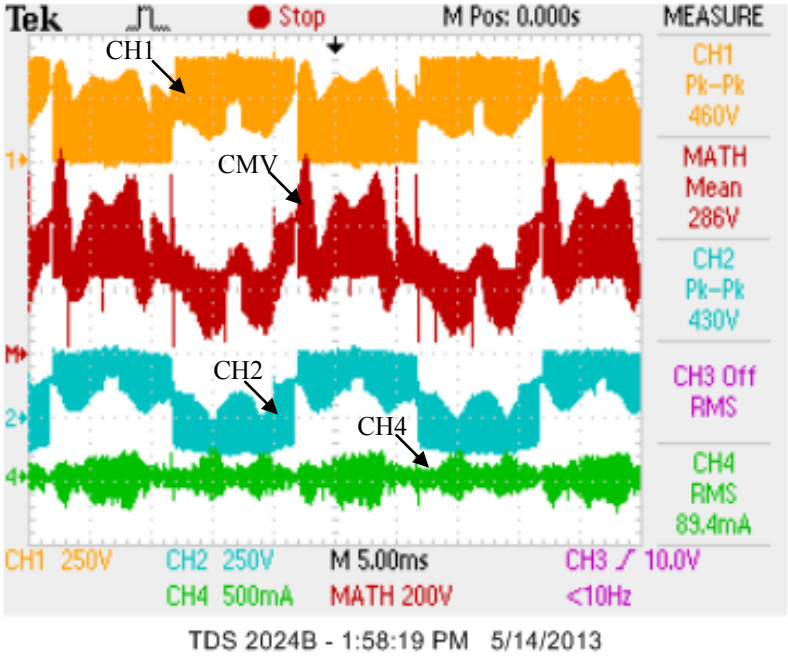


Figure 4.41: V_{AN} (CH1), CMV (M), V_{BN} (CH2) and leakage current (CH4) for H5.

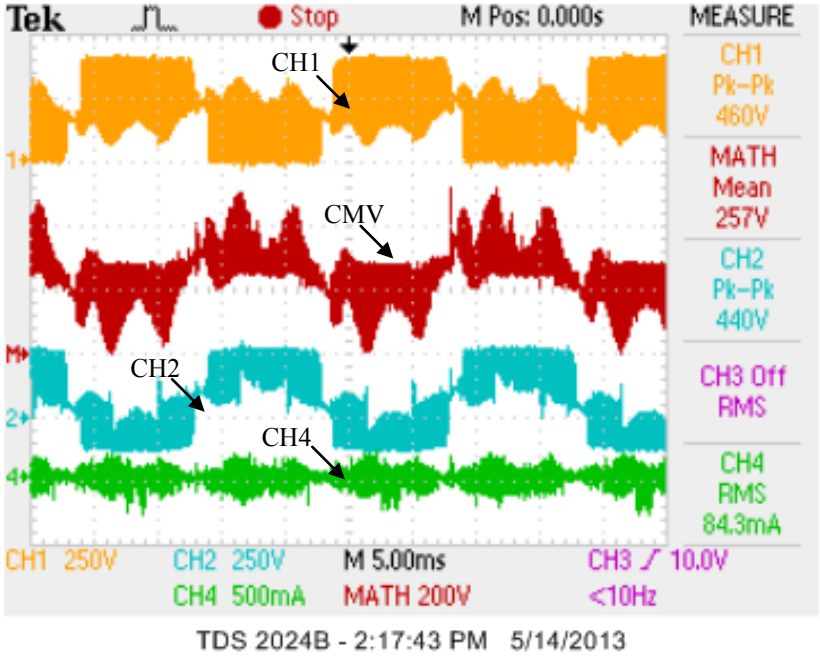


Figure 4.42: V_{AN} (CH1), CMV (M), V_{BN} (CH2) and leakage current (CH4) for HERIC.

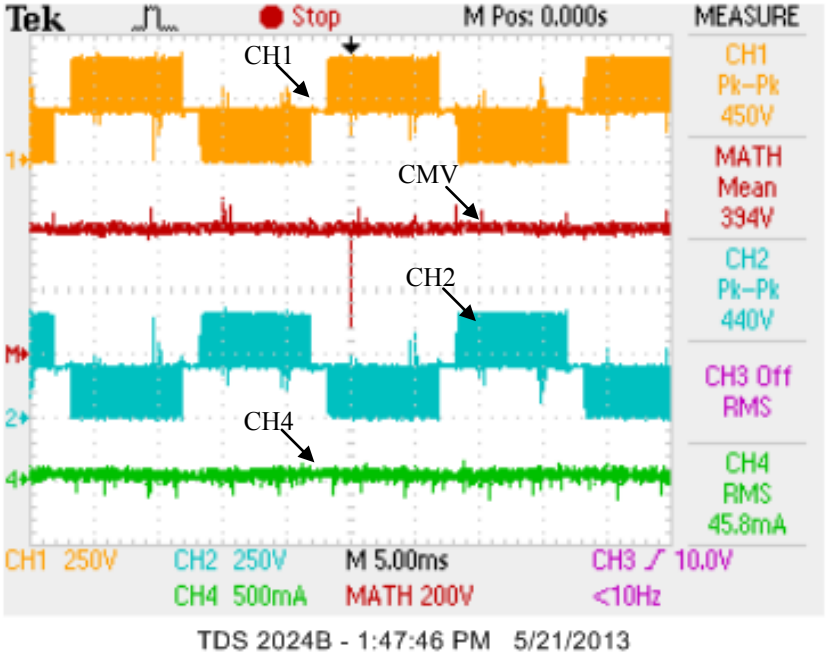


Figure 4.43: V_{AN} (CH1), CMV (M), V_{BN} (CH2) and leakage current (CH4) for H6.

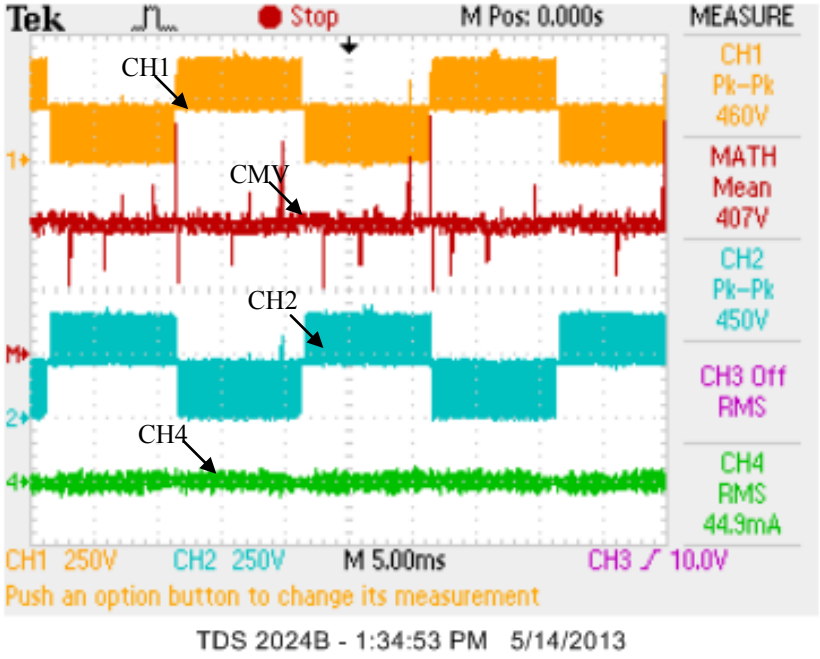


Figure 4.44: V_{AN} (CH1), CMV (M), V_{BN} (CH2) and leakage current (CH4) for oH5.

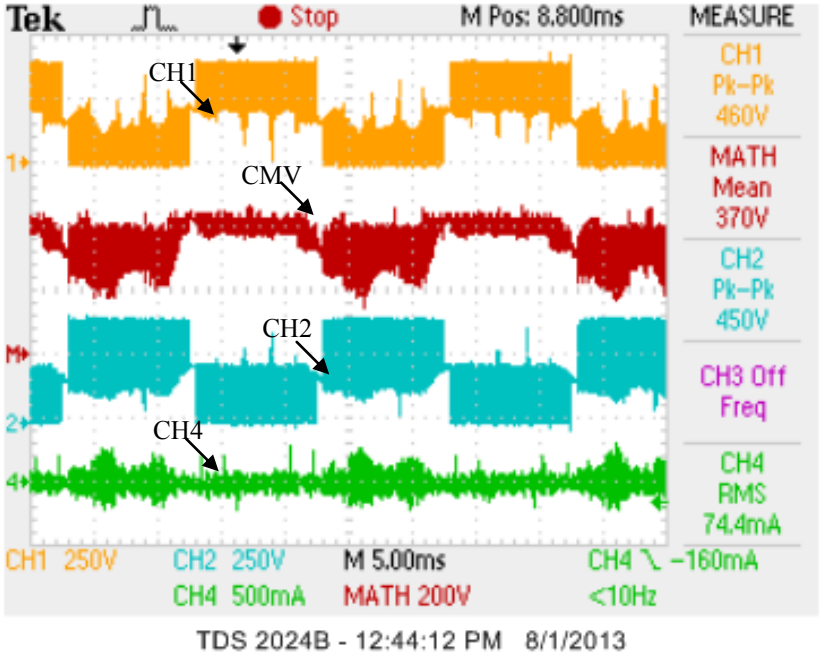


Figure 4.45: V_{AN} (CH1), CMV (M), V_{BN} (CH2) and leakage current (CH4) for HBZVR.

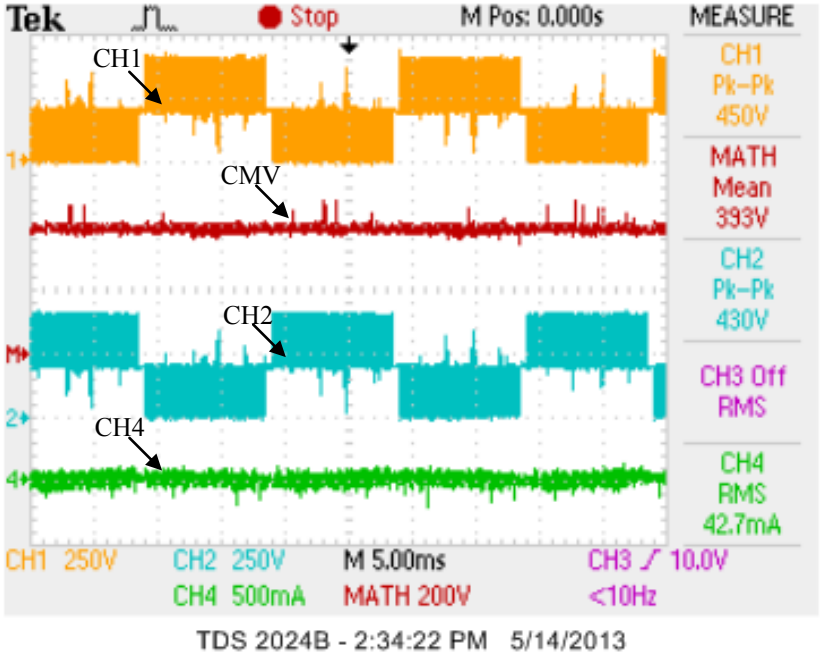


Figure 4.46: V_{AN} (CH1), CMV (M), V_{BN} (CH2) and leakage current (CH4) for HBZVR-D.

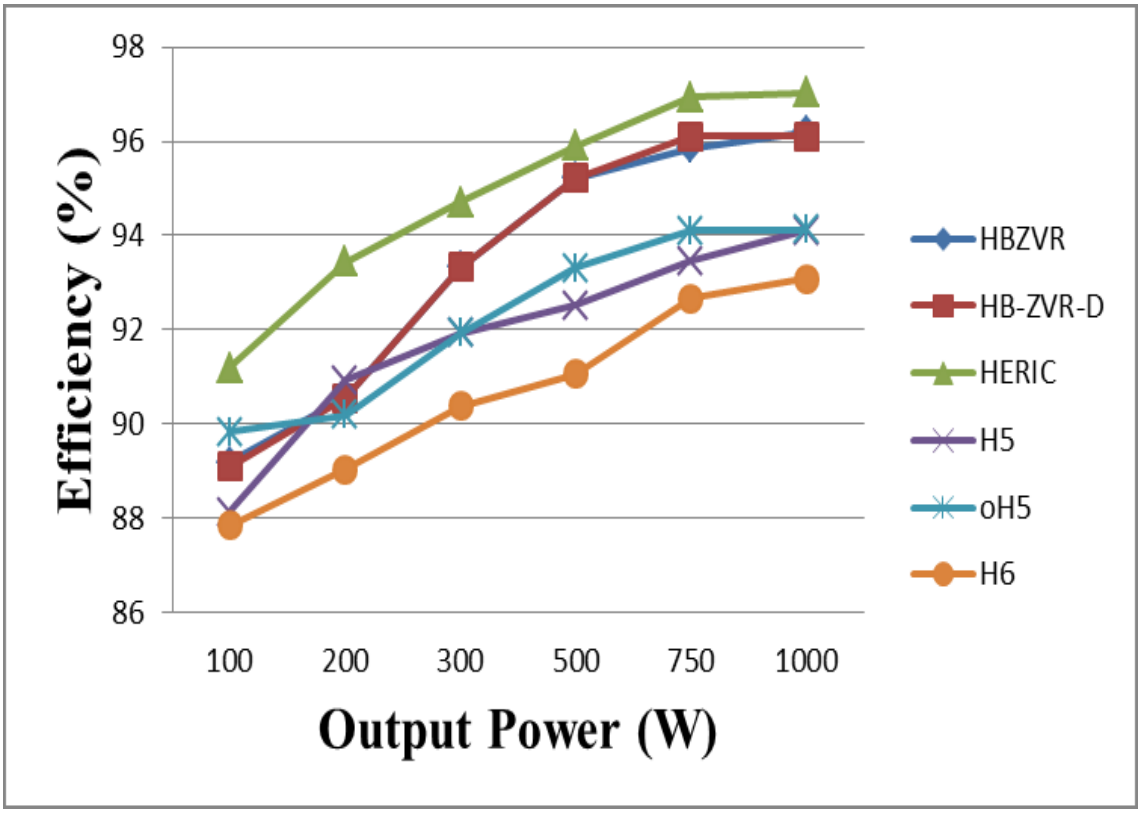


Figure 4.47: Measured efficiency for different topologies.

Figure 4.47 shows the measured efficiency for different topologies. The Californian efficiency is calculated based on

$$\eta_{CEC} = 0.04\eta_{10\%} + 0.05\eta_{20\%} + 0.12\eta_{30\%} + 0.21\eta_{50\%} + 0.53\eta_{75\%} + 0.05\eta_{100\%} \quad (4.8)$$

The calculated Californian efficiency for H5, oH5, H6, HERIC, HBZVR and HBZVR-D are 92.77, 93.32, 91.7, 96.06, 94.91 and 95.03% respectively. As expected, all the ac-decoupling family has better efficiency than those of dc-decoupling family. Proposed HBZVR-D has the second highest efficiency after HERIC topology. This is because the bidirectional switch S_5 of the proposed HBZVR-D is switched at high frequency whereas the bidirectional switch of HERIC is switched at grid frequency.

The THD of the load currents for different topologies are measured by FLUKE 434 Series II Energy Analyzer. All the results are listed in Table 4.3. It can been observed that both HBZVR and proposed HBZVR-D yield higher THD. The increase of the THD is caused by the output voltage spike due to the dead time between the operation period and freewheeling period, which has been addressed earlier. This explains why the THD of the load current is slightly higher than others.

The experimental performance comparisons for all the topologies are summarized in Table 4.3. It is experimentally proven that proposed HBZVR-D topology combines the superior performance of clamping branch family (constant CMV with low leakage current) and ac-decoupling family (low losses and high efficiency), at a cost of a slight increase in THD.

Table 4.3: Performance comparisons for various transformerless topologies

	H5	**oH5**	**H6**	**HERIC**	**HBZVR**	**HBZVR-D**
Number of switches conduct in each conduction period	3	3	4	2	2	2
V_{LL} pattern	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar
CMV	Floating (~200 V)	constant	constant	Floating (~200 V)	Semi-floating (~200 V)	constant
Leakage current (mA_{rms})	89.4	44.9	45.8	84.3	74.5	42.7
THD (%)	1.5	1.5	1.5	1.5	1.9	1.9
Californian efficiency (%)	92.77	93.32	91.7	96.06	94.91	95.03

4.7 Conclusion

Based on the merits and demerits of the various topologies reviewed in previous chapter, a modified HBZVR topology is proposed by addition of a fast-recovery diode in this chapter. The proposed topology (known as HBZVR-D) combines the advantages of the low-loss ac-decoupling method and the complete leakage current elimination of the CMV clamping method. The operating principles of the HBZVR-D configuration are explained in detail.

The performance of the transformerless topologies, including the proposed HBZVR-D, is compared in terms of CMV, leakage current, losses, THD and efficiency via simulation and further validated with experimental results. It is experimentally proven that HBZVR-D topology gives the best overall performance and is suitable for transformerless PV applications for 230V (rms) grid system.

CHAPTER 5

PROPOSED THREE-PHASE TRANSFORMERLESS PV INVERTER

5.1 Introduction

In this chapter, a three-phase transformerless PV inverter is proposed based on the analysis of previous chapters. An in-depth analysis of the circuit configuration, operation principle and its hardware implementation is discussed and studied.

RCMV-PWM methods such as AZPWM, NSPWM and RSPWM are proposed recently to reduce the leakage current. Without zero vectors, RCMV-PWM methods are able to reduce the CMV to reduce the leakage current. Nevertheless, the overall performances are degraded.

This chapter proposes a H7 inverter with novel modulation technique to eliminate the leakage current. The overall performance, in terms of CMV, leakage current, losses, efficiency and THD, is compared with other topologies. Finally, the simulation and experimental results are presented.

5.2 Proposed MDPWM

Conventional DWPM yields the outstanding performances in terms of voltage linearity, switching losses and THD of the output current (Hava et al., 2011). Nevertheless, such optimum performances of the DPWM are degraded in transformerless PV applications. DPWM generates very high leakage current which causes high output current ripples. As a result, the THD of the output current also increases. In order to maintain the unique characteristic of DPWM, a modified DPWM based on conventional DPWM is proposed here to reduce the leakage current.

Unlike RCMV-PWM methods, the proposed MDPWM uses both active vectors and zero vectors to program the output voltage. However, zero vectors (V_0 and V_7) produce high CMV (0 and V_{DC}). Instead of two zero vectors, proposed MDPWM uses only one zero vector (V_7). Therefore, the CMV is reduced by 1/3, varying from $V_{DC}/3$ to V_{DC} as shown in Table 5.1.

Table 5.1: Vectors combination and corresponding CMV for MDPWM

S_1	S_3	S_5	Vector	CMV
1	0	0	V_1	$V_{DC}/3$
1	1	0	V_2	$2V_{DC}/3$
0	1	0	V_3	$V_{DC}/3$
0	1	1	V_4	$2V_{DC}/3$
0	0	1	V_5	$V_{DC}/3$
1	0	1	V_6	$2V_{DC}/3$
1	1	1	V_7	V_{DC}

In every odd regions (B1, B3 and B5), the pulse patterns of MDPWM remains the same as in the conventional DPWM. The difference appears only in even regions where V_0 is replaced by V_7 in MDPWM. For example, as shown in Figure 5.1, MDPWM uses V_1, V_2 and V_7 in region A1 ∩ B1. In region A1 ∩ B2, V_1, V_2 and V_7 (instead of V_1, V_2 and V_0) are used as shown in Figure 5.2. Obviously, V_7 has replaced V_0. The same approach is applied to the rest of the regions and the pulse patterns are listed in Table 5.2.

Table 5.2: Pulse pattern for proposed MDPWM

B1	**A1**	**B2**	**A2**	**B3**	**A3**	**B4**	**A4**	**B5**	**A5**	**B6**	**A6**	**B1**
72127		23732		74347		45754		76567		61716		
	21712		72327		43734		74547		65756		76167	

MDPWM is proposed to reduce the CMV by reserving the use of zero vectors. Zero vectors are important as it determines the output voltage patterns. The elimination of the zero vectors in RCMV-PWM reduces the CMV at the cost of generating bipolar output voltage which gives overvoltage transients and increased current ripples. On the other hand, MDPWM does not suffer from such problem, as it generates unipolar line-to-line output voltage, as seen in Figure 5.1 and Figure 5.2. The main drawback of MDPWM is the simultaneous switching of two inverter legs which leads to increased switching losses. However, applying MDPWM is the only condition to reduce the leakage current while maintaining unique characteristic of DPWM.

It is worth noting that ideally the CMV should be kept at a constant value to eliminate leakage current, as in RSPWM. However, RSPWM suffers from the problem of limited modulation region which increases its dc-link voltage requirement and the corresponding losses. Here, the MDPWM does not maintain the CMV at a constant value as in RSPWM. Instead, it merely reduces the CMV, in a similar manner as the NSPWM and AZPWM. This reduction in CMV, while being able to reduce the leakage current, may not be sufficient to lower the leakage current enough to satisfy the current standard of 300 mA_{rms}. Hence, in the H7 topology, additional switch S7 is utilized to provide galvanic isolation to the leakage current path to further reduce the leakage current. This is explained in the next section.

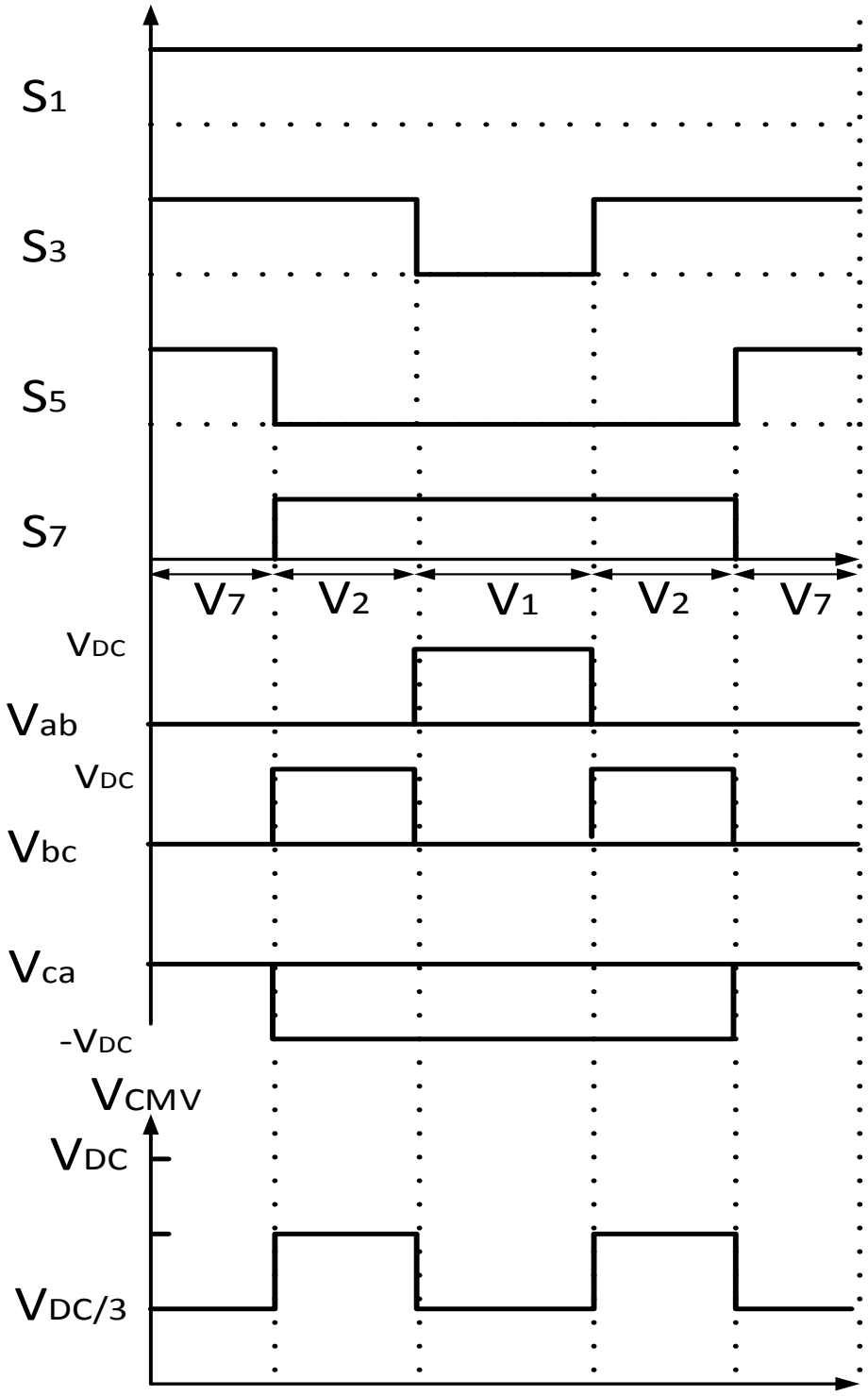


Figure 5.1: Switching pattern, corresponding line-to-line output voltages and CMV for MDPWM in A1 ∩ B1.

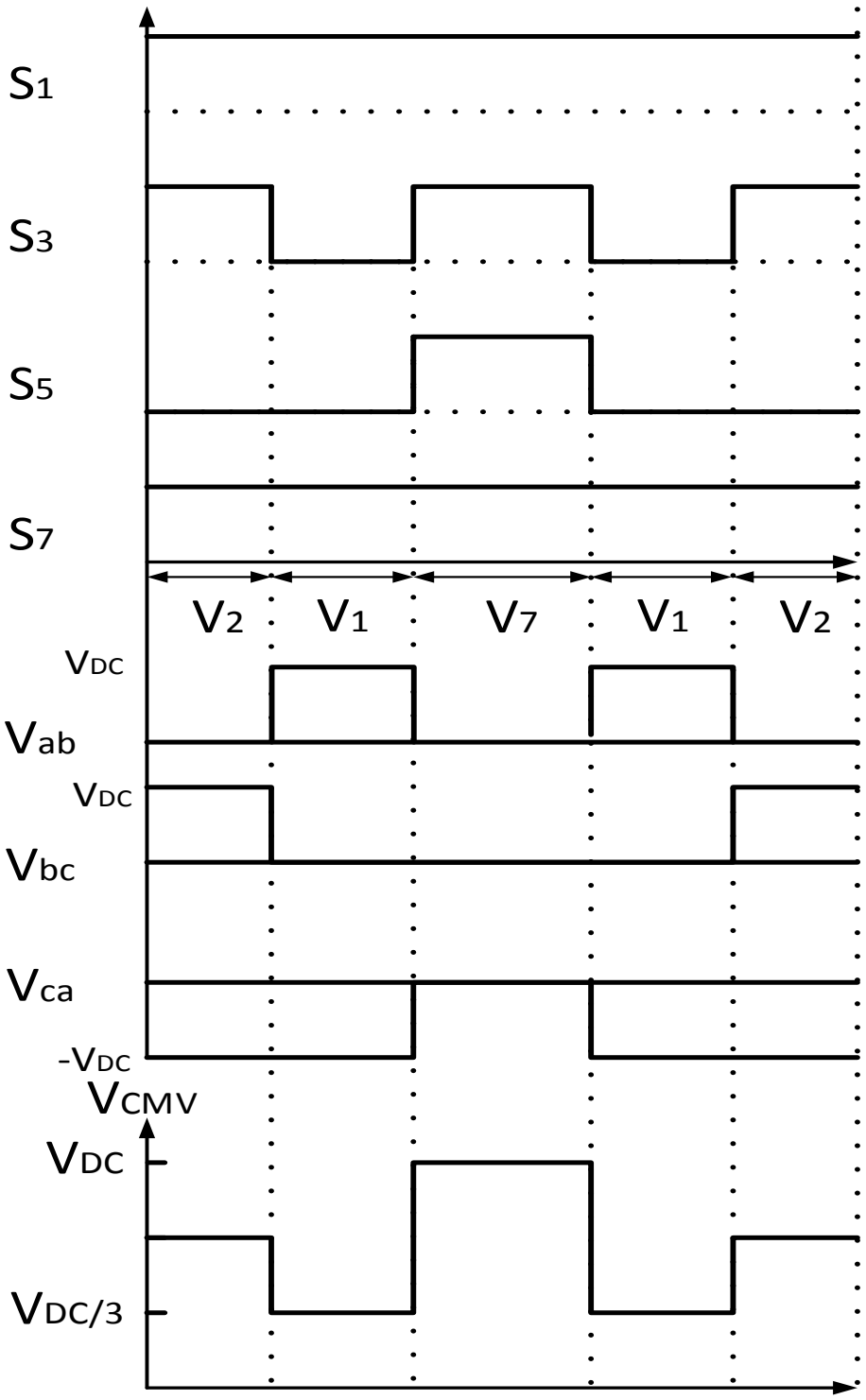


Figure 5.2: Switching pattern, corresponding line-to-line output voltages and CMV for MDPWM in A1 ∩ B2.

5.3 Operation of H7 Conversion Structure

When the transformer is removed from the inverter, it forms a direct path for the leakage current to flow between the PV and the grid. This happens during the freewheeling period when all the upper switches turns on or turns off at the same time. In other words, freewheeling period is the moment when zero vector is applied. Hence, an additional switch, S_7, is added to the three-phase full bridge inverter to provide the galvanic isolation between the PV array and the grid during the freewheeling period. The circuit configuration of H7 inverter is shown in Figure 5.3.

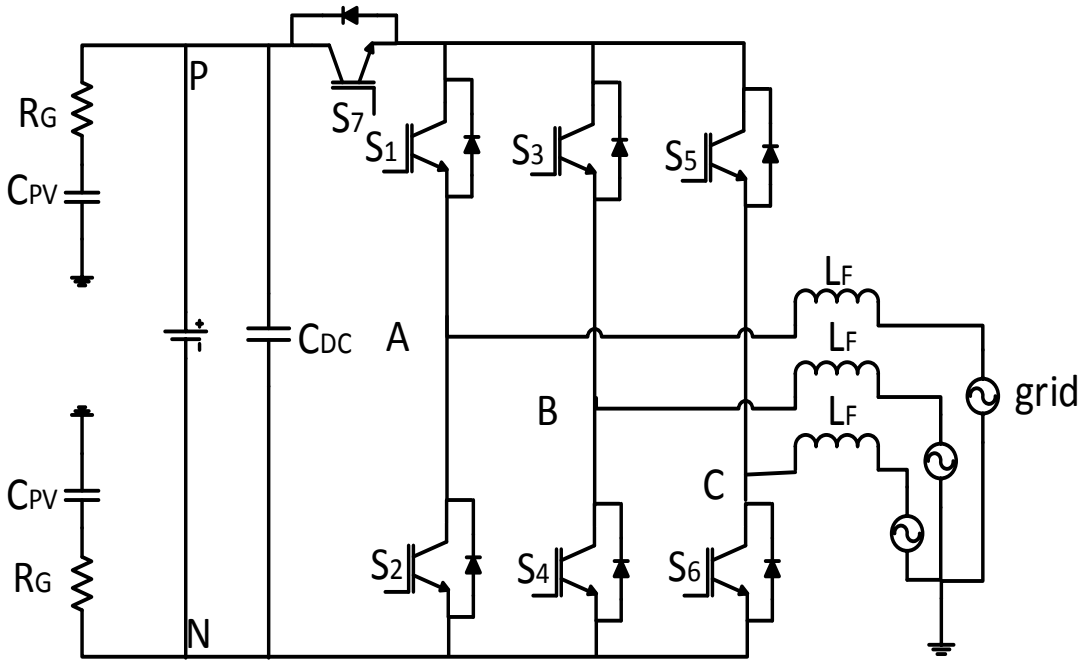


Figure 5.3: H7 conversion structure.

MDPWM clamps each phase leg of the inverter to the positive of the dc-link voltage while the other two phases are modulated at switching frequency. Figure 5.4 shows the simplified equivalent circuit of H7 inverter when both active vectors and zero vector are applied in region A1 ∩ B1 where S_a and S_b are the equivalent single-pole double-throw switches for the half-bridge of each phase. Phase A of the H7 inverter is clamped to the positive dc-link voltage.

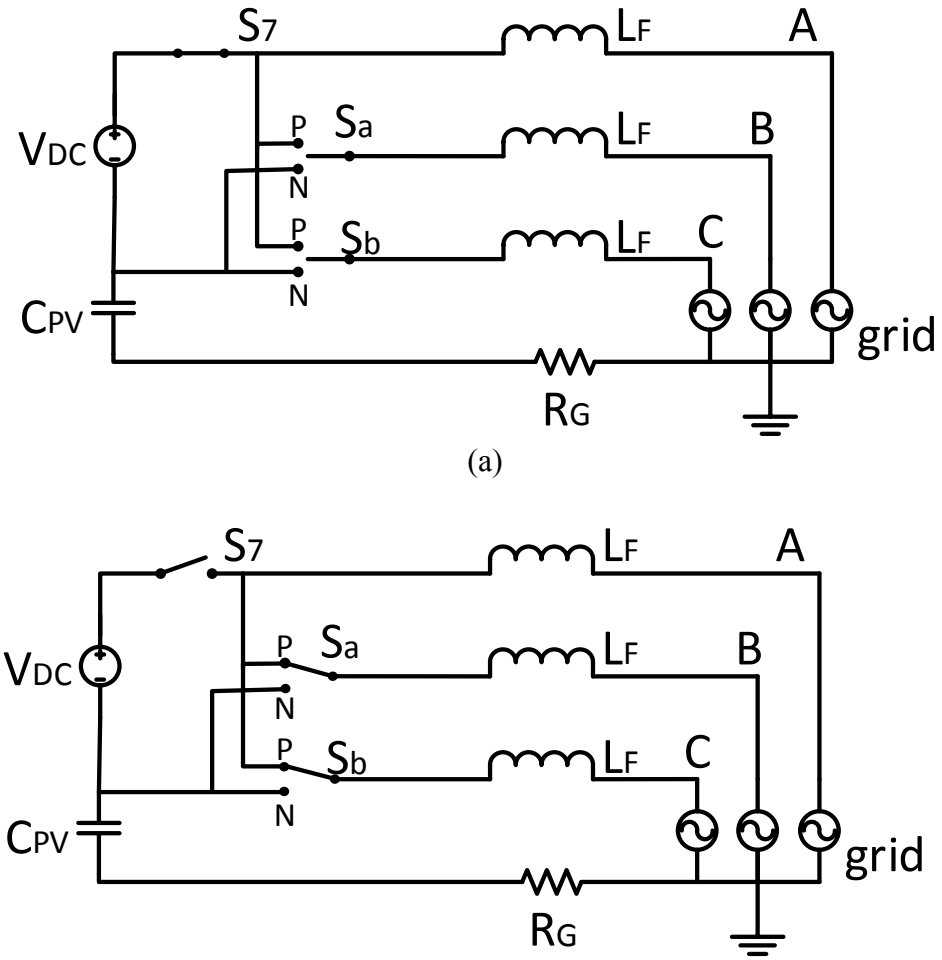


Figure 5.4: Simplified equivalent circuit of H7 inverter during (a) active vectors and (b) zero vectors in region A1 ∩ B1.

As shown in Figure 5.4 (a), when active vectors (V_1, V_2) are applied, S_7 is turned on to generate the desired output voltage and the corresponding CMV becomes $V_{DC}/3$ and $2V_{DC}/3$ respectively. On the other hand, when zero vector V_7 is applied, all the upper switches S_1, S_3 and S_5 are turned on and connected to positive (P) of the dc-link voltage. At this moment, S_7 is turned off to disconnect the PV from the grid. Therefore, leakage current finds no path to flow as shown in Figure 5.4 (b). The voltage V_{AN} and V_{BN} decrease and V_{CN} increases until their values reach the common point, $V_{DC}/3$. The CMV becomes

$$V_{CM} = \frac{V_{AN} + V_{BN} + V_{CN}}{3} = \frac{1}{3}\left(\frac{V_{DC}}{3} + \frac{V_{DC}}{3} + \frac{V_{DC}}{3}\right) = \frac{V_{DC}}{3} \tag{5.1}$$

The switching pattern and corresponding CMV for both region A1 ∩ B1 and A1 ∩ B2 is shown in Figure 5.1. In region A1 ∩ B2, S_7 is turned on all the time to generate the desired output voltage. Voltage vectors V_1, V_2 and V_7 are used and the CMV is $V_{DC}/3$, $2V_{DC}/3$ and V_{DC} respectively. The same principles are applied to all the other regions. Obviously, CMV reduces and varies between $V_{DC}/3$ and V_{DC}. Besides CMV reduction, galvanic isolation further reduces the leakage current. Thus, H7 topology with the proposed MDPWM combines the optimum behavior for both DPWM and RCMV-PWM methods.

It is worth noting that voltage V_{AN}, V_{BN} and V_{CN} are impossible to reach the common point, $V_{DC}/3$ during the disconnection of the S_7. In practical applications, they are floating and oscillating due to the switches' junction capacitances and resonant circuit effects. This effect will be seen clearer in the simulation results shown in Figure 5.16. In fact, this effect can be avoided using the CMV clamping branch which have been proposed in (Huafeng & Shaojun, 2010; Huafeng et al., 2011). However, the CMV clamping for three-phase system requires additional hardware configuration which may

add burden to the cost, efficiency and complexity of design for both hardware and software. The CMV clamping method is not within the scope of this paper and will be discussed in future work.

5.4 Scalar Implementation of MDPWM

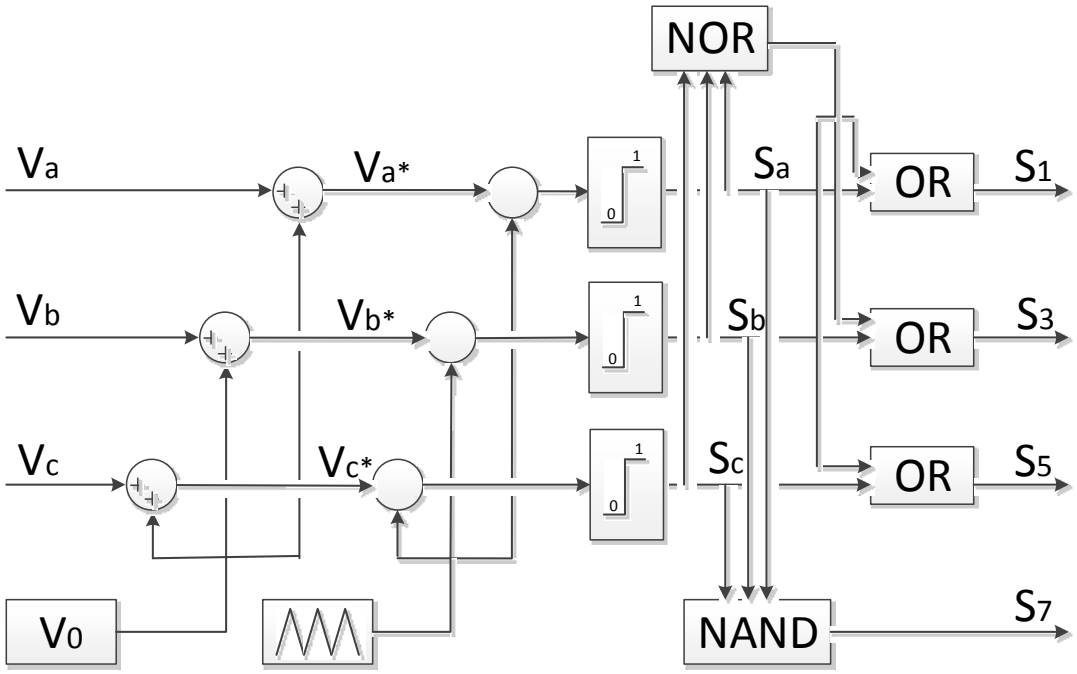


Figure 5.5: Proposed PWM modulator.

In this section, the implementation of the proposed MDPWM is discussed. The overall block diagram for the proposed PWM is shown in Figure 5.5. It is simple and straightforward as in conventional DPWM. It can be easily implemented using scalar approach as follow:

$$V_a^* = V_a + V_0 = m \sin(\text{wt}) + V_0 \tag{5.2}$$

$$V_b^* = V_b + V_0 = m \sin(\text{wt} - 2/3\,\pi) + V_0 \tag{5.3}$$

$$V_c^* = V_c + V_0 = m \sin(\text{wt} + 2/3\,\pi) + V_0 \tag{5.4}$$

where V_a, V_b and V_c are the original sinusoidal reference signals, V_0 is the zero sequence signal and m is the modulation index. V_0 is calculated via magnitude test as follow:

$$V_0 = [\text{sign}(V_{max})](V_{dc}/2) - V_{max} \quad (5.5)$$

where V_{max} is the original sinusoidal reference (V_a, V_b or V_c) with the maximum magnitude.

After the injection of V_0, the resultant modulation signals (V_a*, V_b* and V_c*) are then compared with a triangular carrier wave to generate the logic signals S_a, S_b and S_c. These logic signals (S_a, S_b and S_c) are the pulse patterns of conventional DPWM. In order to generate MDPWM with only one zero vector (V_7), simple logic operations are utilized to generate the desired gating signals (S_1, S_3, S_5 and S_7). In other words, the implementation of the proposed MDPWM is in the same manner as in conventional DPWM. Only additional simple logic operations are required.

5.5 Performance Analysis of MDPWM

5.5.1 Simplicity of Design and Cost

Unlike RCMV-PWM methods, the implementation of the proposed MDPWM is simple and straightforward. This is because the AZPWM, NSPWM and RSPWM methods require the simultaneous use of two different triangular carriers (up-down and down-up triangular carriers) (Hava & Un, 2009, 2011; Hou, Shih, Cheng, & Hava, 2013) which needs advance DSP, such as Texas Instrument's TMS320F28335 with enhanced PWM (EPWM) module, for implementation. Hence, it is difficult to be realized on low cost microcontrollers with limited carrier configuration flexibility. On the other hand, the proposed MDPWM method requires only one carrier (up-down or down-up) for all

three of its phases. Furthermore, the implementation of the MDPWM is as simple as the conventional DPWM with only additional logic operations which can be digitally implemented into the DSP.

5.5.2 Line to Line Output Voltage Pattern

The elimination of the zero vectors reduces the CMV in RCMV-PWM. Nevertheless, zero vectors are important as it determines the line-to-line output voltage pattern. Generally, zero vectors produce zero output voltage. When the zero vectors are replaced with active vectors in RCMV-PWM methods, bipolar line-to-line output voltage is expected. This is because the PWM generates voltage throughout the PWM cycles. MDPWM inherits the unique characteristic of unipolar line-to-line output voltage by reserving the utilization of zero vector. In every PWM cycle, the polarity of the voltage remains the same. Overvoltage transients and PWM current ripples are reduced and thus smaller filter inductors can be used.

5.5.3 Voltage Linearity

Each PWM modulation technique has a specific linear modulation region. Outside this region, the overall performance in terms of THD of output current, current ripples, voltage magnitude and common mode behavior are degraded. Therefore, a wide linear modulation range is preferable. MDPWM maintains the superior voltage linearity characteristic of conventional DPWM. By injecting the zero sequence signal, MDPWM is able to extend the utilization of the dc-link voltage by 15% which enable it to operate linearly for $0 < m < 0.907$.

5.6 Matlab Simulation

In order to verify the operation and overall performance of the PV system, simulations are carried out via Matlab/ Simulink. The simulation setup for RCMV-PWM and H7 inverter with proposed MDPWM is shown in Figure 5.6 and Figure 5.7 respectively. The whole PV system comprises of a full-bridge inverter, current controller and pulse generator. For H7 inverter, additional switch is added between the dc-link and the full-bridge inverter. Figure 5.8 and Figure 5.9 indicate the pulse generator configuration for both RMCV-PWM and proposed MDPWM respectively.

All the simulations are done based on the same parameters (Bradaschia et al., 2011; Cavalcanti et al., 2010; Hou et al., 2013). The PV array is simulated with dc voltage source of 600 V. The stray capacitance (C_{PV}) is modeled with two capacitors of 220 nF, each connected between the PV terminal and the ground. The dc-link capacitor (C_{DC}) is 2mF. The ground resistance (R_G) is 11 Ω. The filter is made up of three inductors (L_F); each has a value of 5 mH. The load resistance is 100 Ω and the modulation index m = 0.9. For fair comparison, switching frequency is selected such that all the modulation techniques have equal average switch commutation, i.e., SVPWM, AZPWM and proposed MDPWM are modulated at 10 kHz while DPWM and NSPWM at 15 kHz (Hava & Un, 2009; Hou et al., 2013). RSPWM is not taken into discussion due to its impracticality in grid-connected applications. It is worth nothing that DPWM and NSPWM will incur fewer switching events if the same frequency was chosen for all discussed topologies. This undoubtedly reduces the switching losses. Nevertheless, it is not implemented here because the analysis must be carried out based on equal switch count for fair comparison and performance analysis purpose.

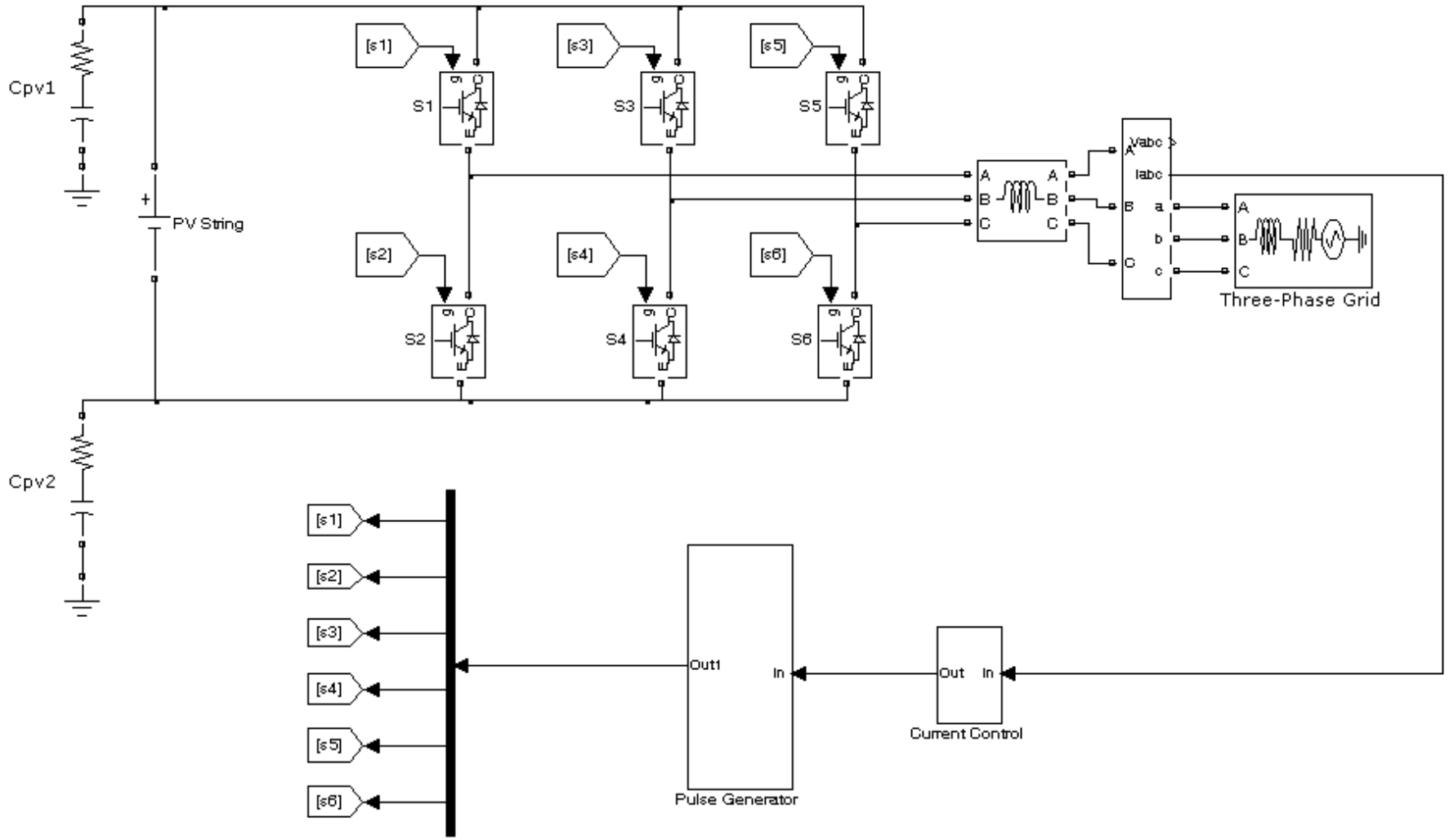


Figure 5.6: Simulation setup for RCMV-PWM.

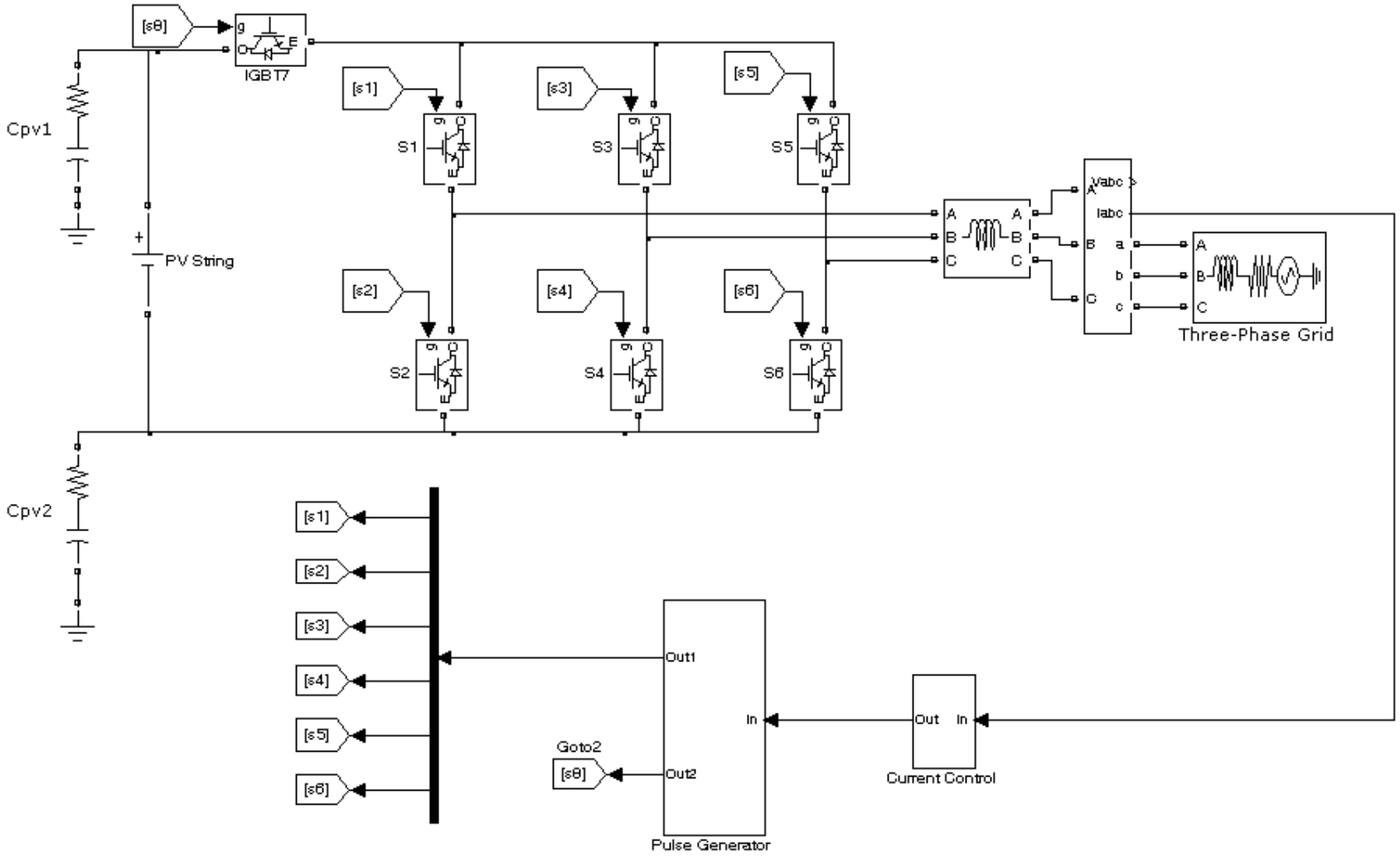


Figure 5.7: Simulation setup for H7 inverter with MDPWM.

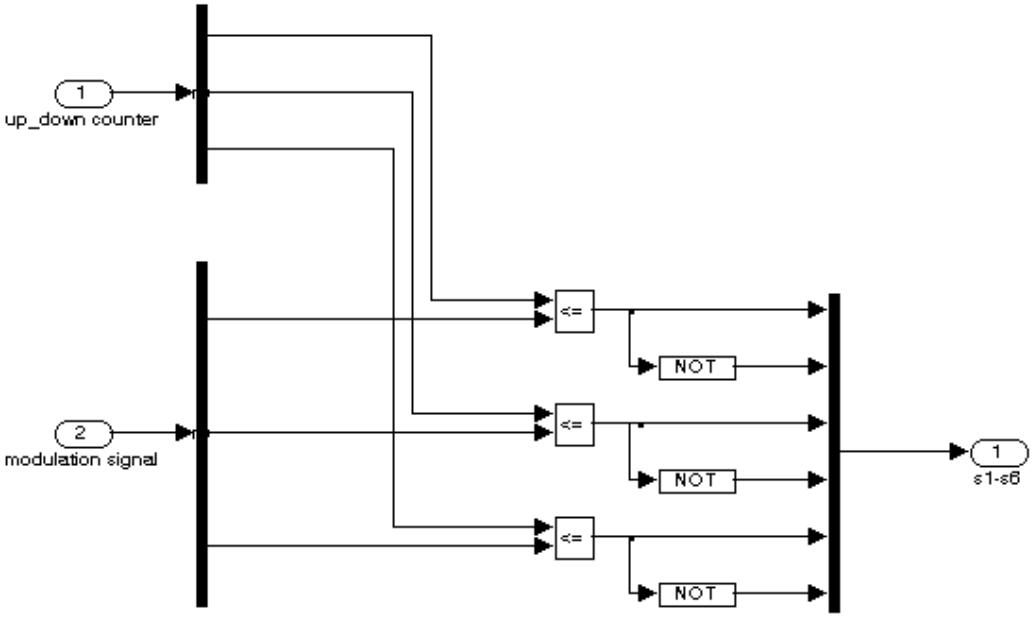


Figure 5.8: Pulse generation for RCMV-PWM.

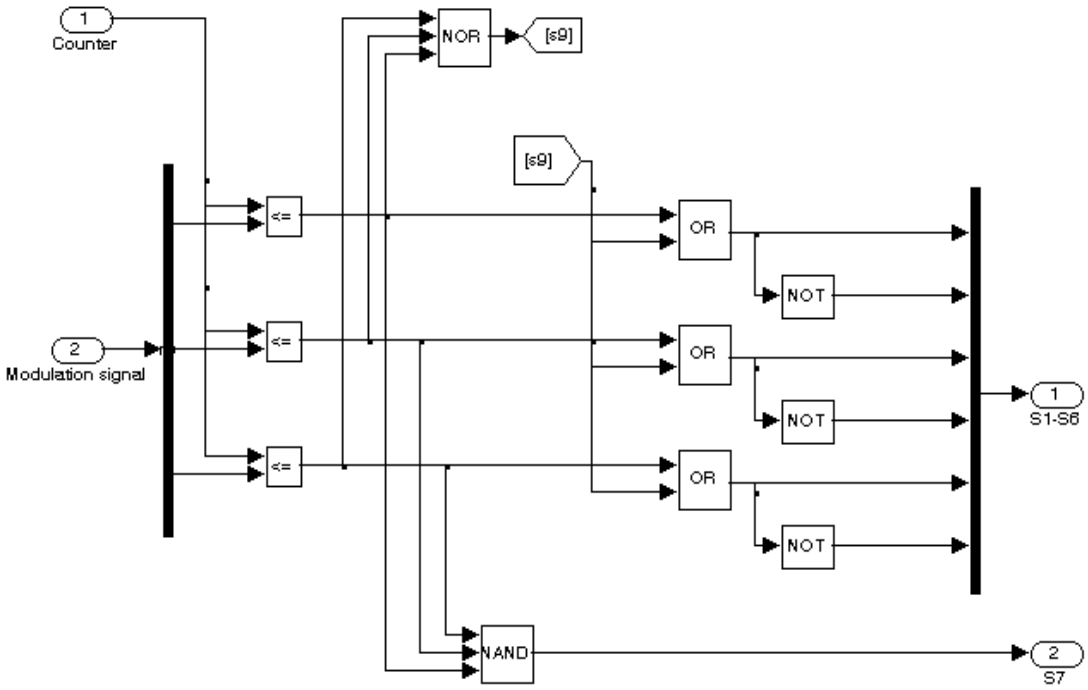


Figure 5.9: Pulse generation for MDPWM.

5.6.1 Simulation Results

Figure 5.10 to Figure 5.14 show the line-to-line output voltage waveforms and the output currents for various modulation techniques. As shown in Figure 5.9 and Figure 5.10, conventional SVPWM and DPWM generate unipolar line-to-line output voltage. Even though SVPWM and DPWM have superior harmonic distortion performance as reported in (Hava & Un, 2009), it generates load current with high current ripples as shown in Figure 5.10 and Figure 5.11 respectively. This is because high leakage current is generated as shown later. The leakage current injects ripples into the load current which undoubtedly increases the harmonic distortion.

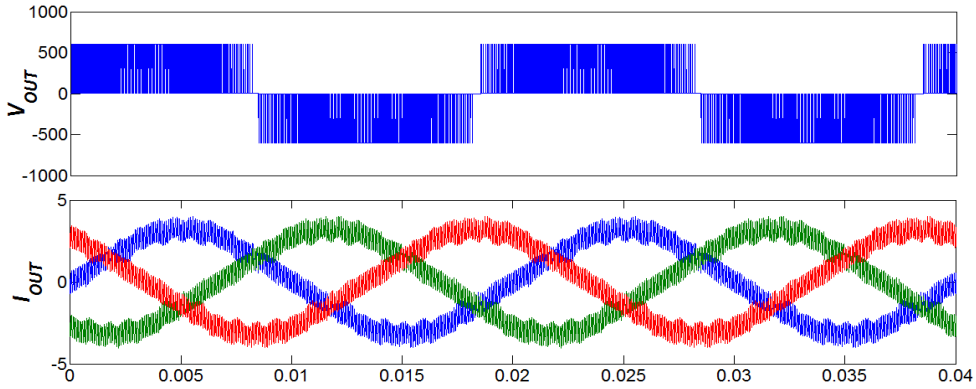


Figure 5.10: Line-to-line output voltage (top) and grid current (bottom) for SVPWM.

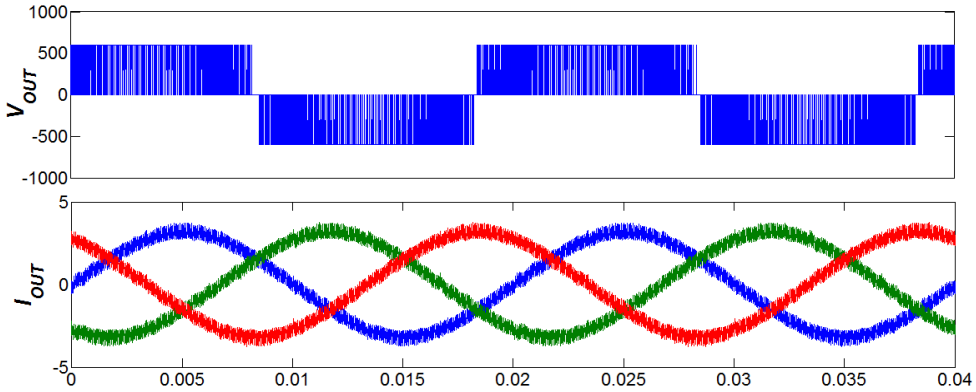


Figure 5.11: Line-to-line output voltage (top) and grid current (bottom) for DPWM.

Both AZPWM and NSPWM use only active vectors to program the output voltage. Therefore, the output voltage waveform has altered, generating undesirable bipolar output voltage waveform. As observed in Figure 5.12 and Figure 5.13, the output voltage varies from $+V_{DC}$ to $-V_{DC}$. This doubles the voltage stress across the inductors by twice of the input voltage. As a result, losses and current ripples double which requires the use of larger filter inductors.

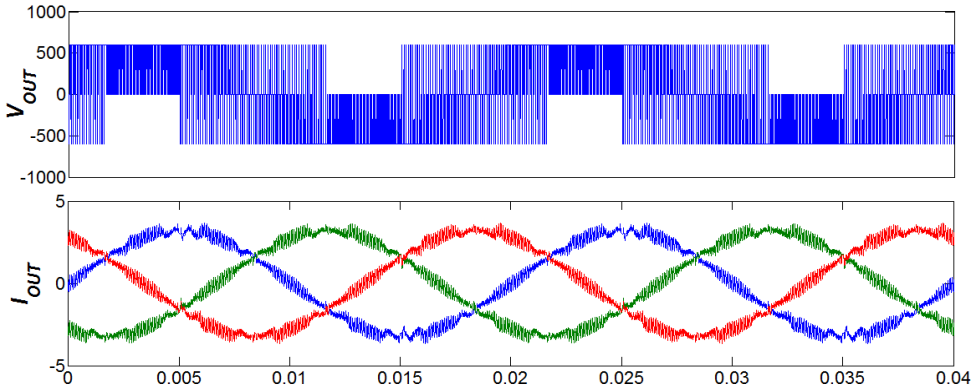


Figure 5.12: Line-to-line output voltage (top) and grid current (bottom) for AZPWM.

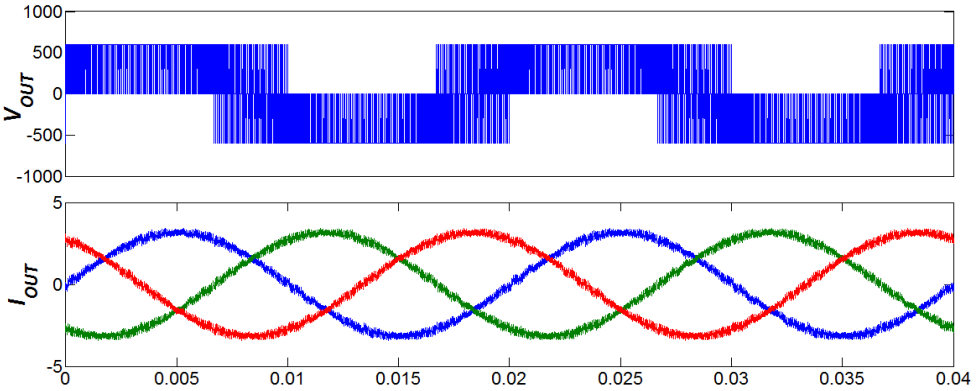


Figure 5.13: Line-to-line output voltage (top) and grid current (bottom) for NSPWM.

Proposed MDPWM shares the similar characteristic of conventional DPWM. It generates unipolar output voltage as shown in Figure 5.14. It is proven that the proposed MDPWM inherits the unique characteristic of DPWM by reserving the utilization of zero vectors. Although it replaces V_0 by V_7, the output voltage pattern does not change. In every PWM cycle, the polarity of the voltage remains the same, varying from 0 to $+V_{DC}$, or from 0 to $-V_{DC}$. The unipolar output voltage reduces the losses and the current ripples as compared to bipolar. As a result, smaller filter inductors are required and hence the size and the cost are reduced.

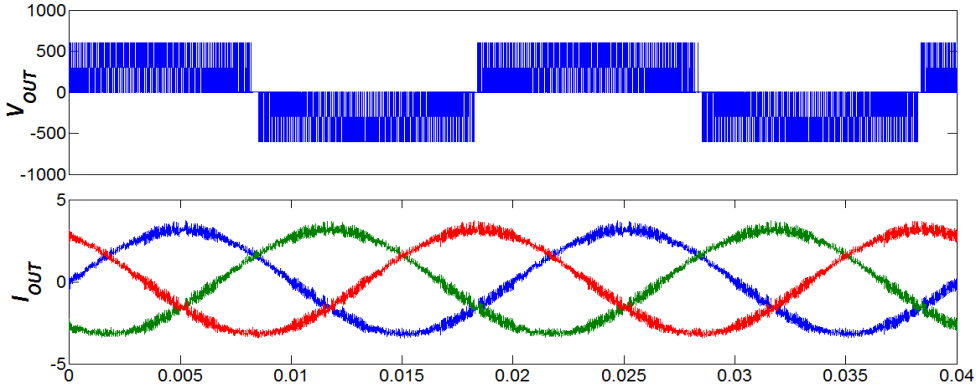


Figure 5.14: Line-to-line output voltage (top) and grid current (bottom) for H7 inverter with proposed MDPWM.

Figure 5.15 to Figure 5.19 indicate the common-mode behavior for various topologies. Due to the utilization of zero vectors, both SVPWM and DPWM have the poorest common-behavior. As shown in Figure 5.15 and Figure 5.16, the CMVs vary from 0 to V_{DC} and thus high leakage currents are generated. This also explains why the output current ripples are higher than the other topologies as observed in the Figure 5.10 and Figure 5.11.

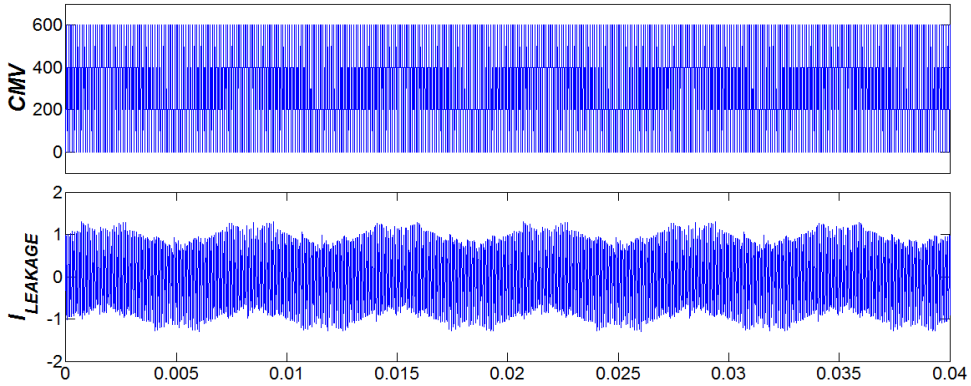


Figure 5.15: CMV (top) and leakage current (bottom) for SVPWM.

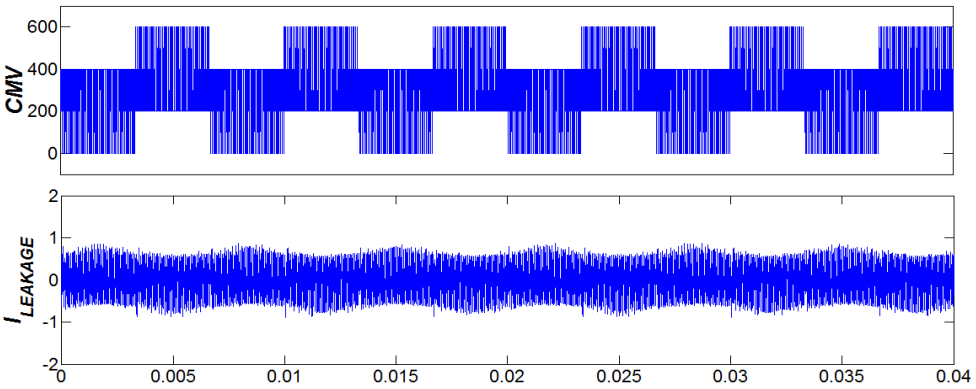


Figure 5.16: CMV (top) and leakage current (bottom) for DPWM.

By eliminating the zero vectors to program the output voltage, both AZPWM and NSPWM are able to reduce the CMV by 2/3, varying from $V_{DC}/3$ to $2V_{DC}/3$ as shown in Figure 5.17 and Figure 5.18 respectively. The reduction of the CMV reduces the charging and discharging voltage across the stray capacitors. Therefore, leakage currents are significantly reduced.

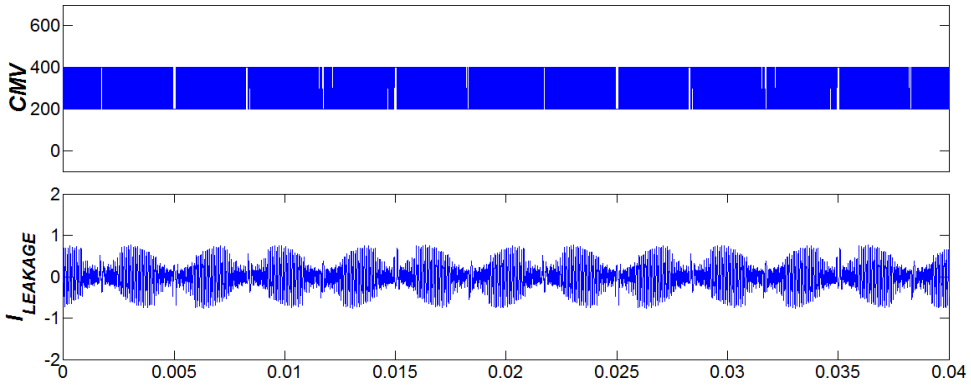


Figure 5.17: CMV (top) and leakage current (bottom) for AZPWM.

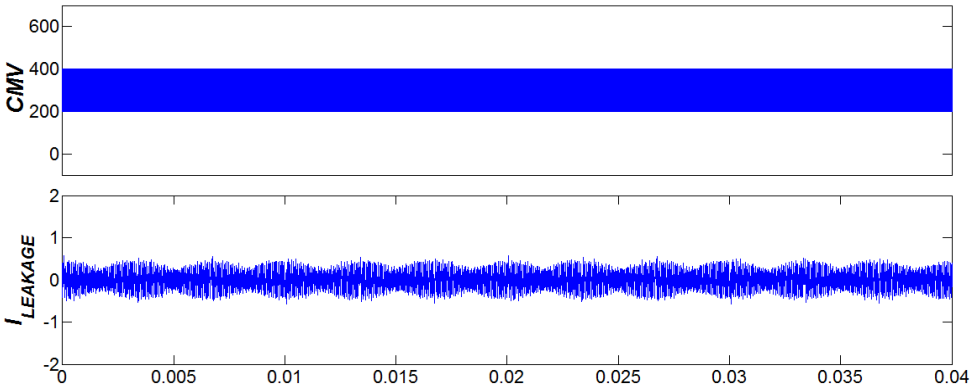


Figure 5.18: CMV (top) and leakage current (bottom) for NSPWM.

With proposed MDPWM, the CMV is reduced by 1/3 by employing only V_7 as zero vectors to program the output voltage. The CMV changes depending on S_7. When S_7 is turned on, the CMV varies from $V_{DC}/3$ to $2V_{DC}/3$ and from $V_{DC}/3$ to V_{DC} when it is turned off. In addition, galvanic isolation is provided by H7 topology as discussed earlier. S_7 turns off during freewheeling period to disconnect the PV from the grid. With both the galvanic isolation of H7 topology and the reduced CMV of proposed MDPWM, the leakage current is significantly reduced as indicated in Figure 5.19.

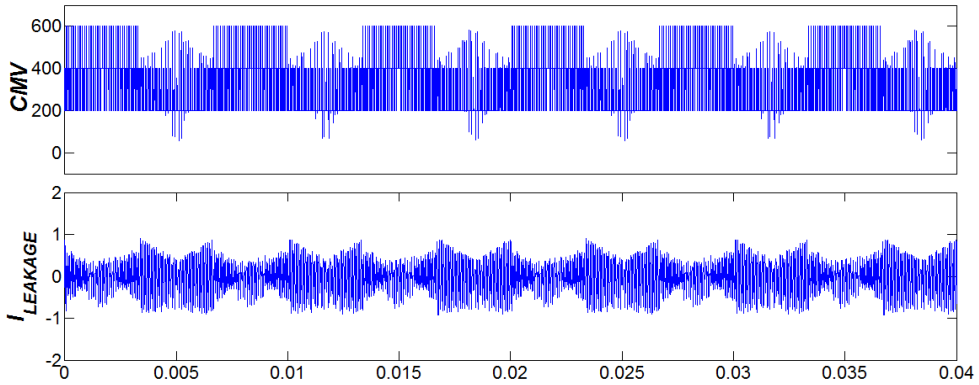


Figure 5.19: CMV (top) and leakage current (bottom) for H7 inverter with proposed MDPWM.

Figure 5.20 shows the microscopic view of the CMV waveform for the proposed MDPWM. Instead of $V_{DC}/3$ and $2V_{DC}/3$, small oscillation with magnitude up to 100 V is observed in the CMV waveform. This oscillation occurs when S_7 is turned off to provide galvanic isolation during the freewheeling period. Practically, V_{AN}, V_{BN} and V_{CN} are impossible to reach the common voltage of $V_{DC}/3$ due to the switches' junction capacitances and resonant circuit effects as explained earlier.

However, it is worth mentioning that H7 topology with the proposed MDPWM still has the best overall performance which combines the advantages of the unipolar output voltage pattern, reduced switching losses of DPWM and the low CMV, low leakage currents of the RCMV-PWM methods.

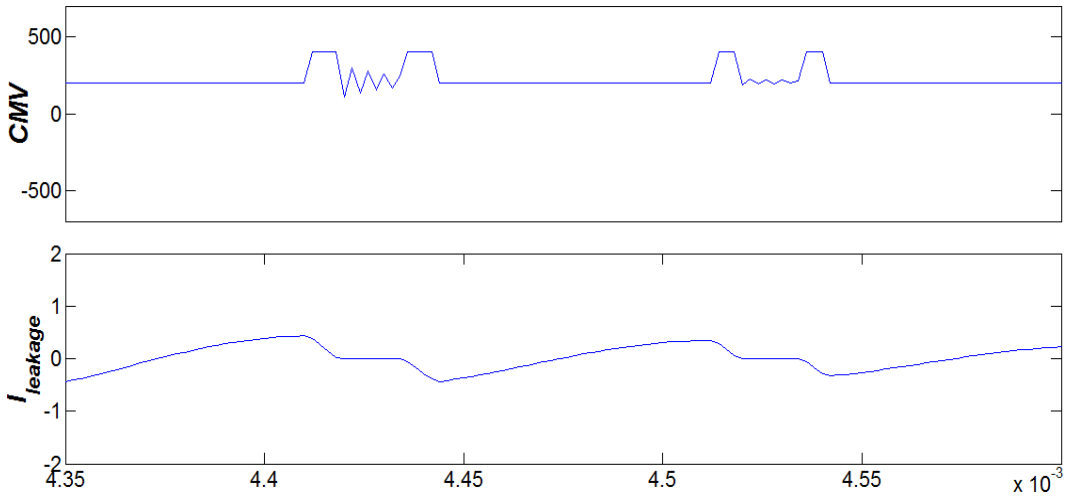


Figure 5.20: Zoom-in waveforms of CMV (top) and leakage current (bottom) for H7 with proposed MDPWM, showing CMV oscillation during freewheeling period.

5.7 Experimental Results

The experimental setup is shown in Figure 5.21. S_1–S_6 are the switches of conventional full-bridge inverter. “DC-bypass” is the dc-decoupling branch of H7 inverter. Table 5.3 lists the inverter specifications. All the control algorithms are implemented in DSP TMS320F28335.

For fair comparison, switching frequency is selected such that all the modulation techniques have equal average switch commutation, i.e., SVPWM, AZPWM and proposed MDPWM are modulated at 10 kHz while DPWM and NSPWM at 15 kHz. RSPWM is not taken into discussion due to its impracticality in grid-connected applications.

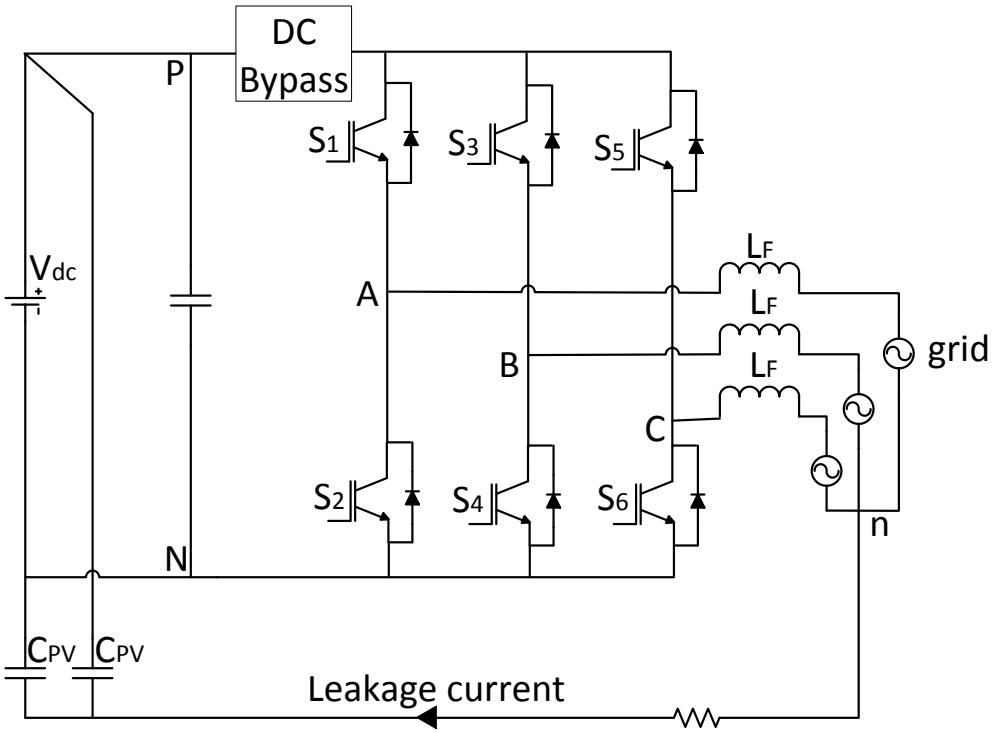


Figure 5.21: Experimental setup.

Table 5.3: Parameters of universal inverter

Parameter	Value
Input voltage	600 V_{DC}
Load	100 ohm
Rated power	1 kW
Dead time	2.5 us
DC-link capacitors	2200 uF, V_{DC}=400V
IGBT	IRGP30B120KD-EP V_{CE}=1200V, I_C= 60A
Filter inductors	5 mH
Stray capacitors	220 nF

Figure 5.22 to Figure 5.26 show the experimental results of line-to-line output voltage, output current and leakage current for various topologies. Both conventional SVPWM and DPWM share similar unipolar output voltage and sinusoidal output current waveforms. Nevertheless, high current ripples are observed as shown in Figure 5.22 and Figure 5.23 respectively due to high leakage currents. The magnitude of the leakage current for SVPWM and DPWM are 610 and 414 mA (rms) respectively which have exceeded the requirement of VDE 0126-1-1 standard. Moreover, common-mode noise is observed. Therefore, they are not suitable for transformerless PV applications.

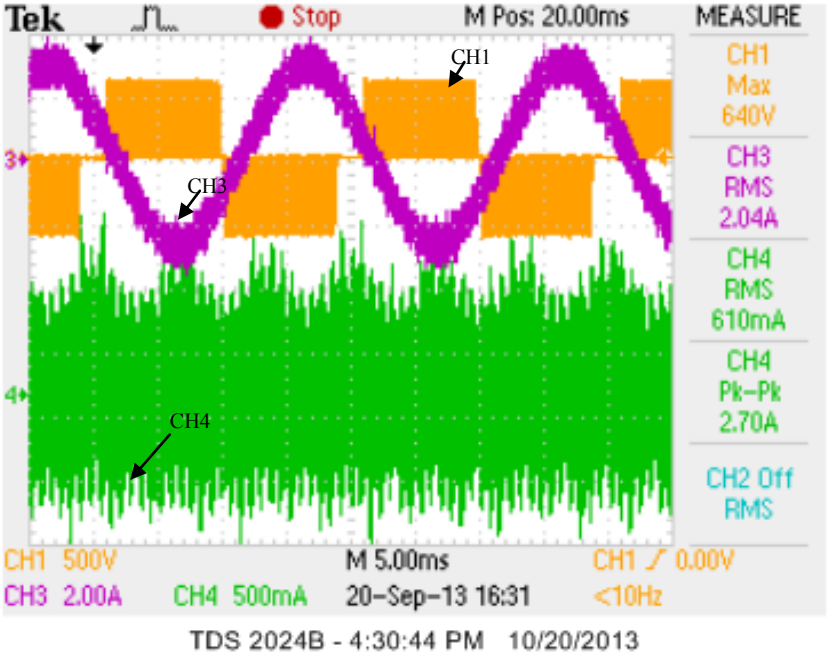


Figure 5.22: Line-to-line voltage (CH1), output current (CH3), and leakage current (CH4) for SVPWM.

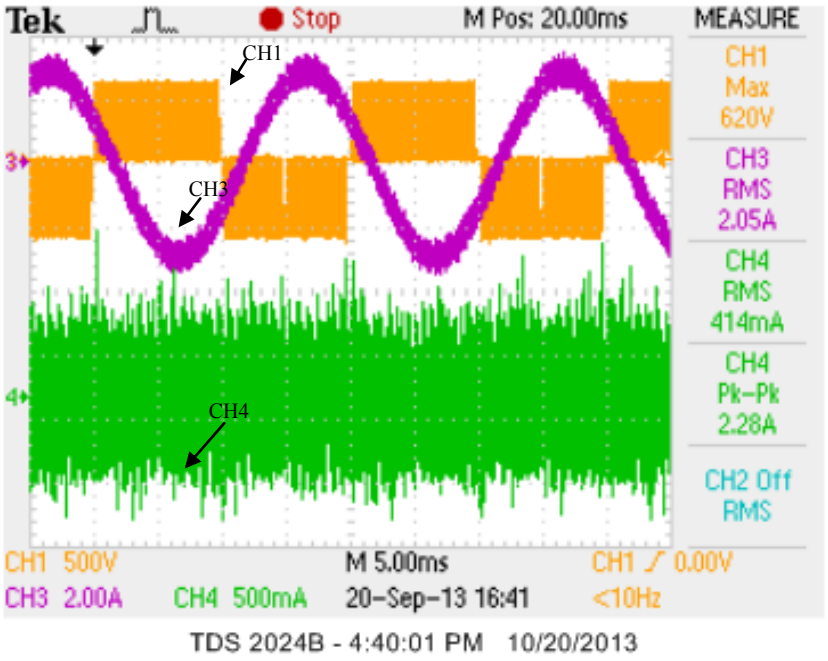


Figure 5.23: Line-to-line voltage (CH1), output current (CH3), and leakage current (CH4) for DPWM.

As shown in Figure 5.24, the leakage current is reduced significantly to 240 mA (rms) for AZPWM. This is because AZPWM utilizes only active vectors to program the output voltage, resulting reduced CMV. This also explains why the output current ripples are smaller compared to the conventional modulation techniques. However, the replacement of the zero vectors causes the bipolar output voltage issues. As shown in Figure 5.24, in certain PWM cycles, the output voltage varies from $+V_{DC}$ to $-V_{DC}$. This doubles the voltage stress across the filter inductors and hence reduces the overall efficiency. Issues such as overvoltage transients may arise.

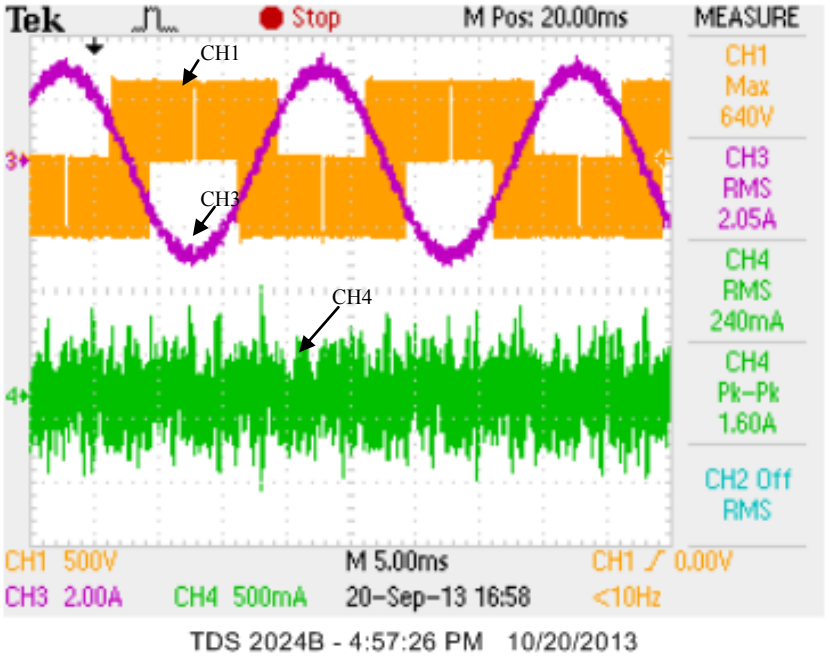


Figure 5.24: Line-to-line voltage (CH1), output current (CH3), and leakage current (CH4) for AZPWM.

NSPWM employs adjacent active vectors to program the output voltage. This helps to reduce the CMV as well as the switch count. As a result, NSPWM is able to be modulated at higher frequency as compared to AZPWM. This explains why the leakage current is reduced significantly to 229 mA (rms).

The output current ripple is smaller due to reduced leakage current. Nevertheless, NSPWM still suffers from the bipolar output voltage issues. As shown in Figure 5.25, in certain PWM cycles, the output voltage varies from $+V_{DC}$ to $-V_{DC}$. This doubles the voltage stress across the filter inductors and hence reduces the overall efficiency. Issues such as overvoltage transients may arise.

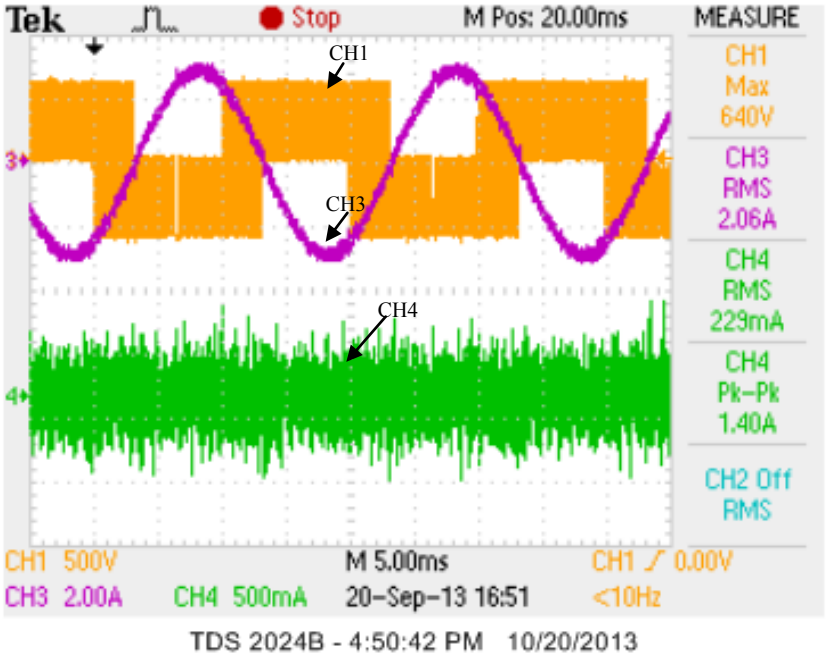


Figure 5.25: Line-to-line voltage (CH1), output current (CH3), and leakage current (CH4) for NSPWM.

DPWM and MDPWM have the same modulation signal. Hence, MDPWM demonstrates the same attributes as DPWM. With the use of zero vectors, it generates the favorable unipolar output voltage waveform as shown in Figure 5.26. On the other hand, leakage current is reduced to 217 mA (rms) due to reduced CMV and galvanic isolation of H7 topology. Even though, both AZPWM and NSPWM meet the requirement of VDE 0126-1-1 standard, the proposed method gives the lowest leakage current.

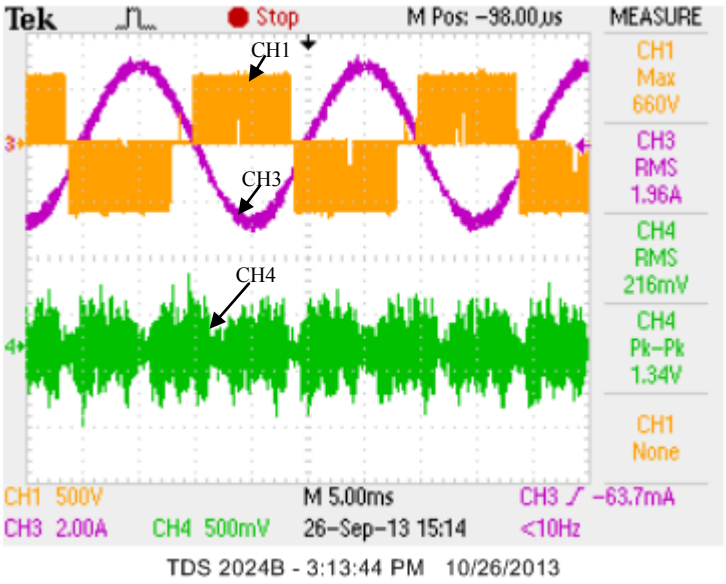


Figure 5.26: Line-to-line voltage (CH1), output current (CH3), and leakage current (CH4) for H7 inverter with proposed MDPWM.

Voltage ripple performance is another critical factor as they determine the dc-link capacitor size and life time and hence cost. Therefore, lower ripples are preferred. The dc-link voltage ripple waveforms for various PWM methods are captured as shown in Figure 5.27. The peak-to-peak voltage ripples for SVPWM, DPWM, AZPWM, NSPWM and H7 with the proposed MDPWM are 3.88 V, 1.66 V, 1.68 V, 1.62 V and 1.60 V respectively. Although conventional SVPWM and DPWM are more superior in terms of dc-link current ripples as reported in (Hava & Un, 2009), they are not valid for transformerless PV applications due to the very high leakage current. As expected, SVPWM has the highest dc-link voltage ripples. H7 inverter with the proposed MDPWM inherits the superior characteristics of DPWM. This explains why the proposed topology yields the lowest dc-link voltage ripples among all methods.

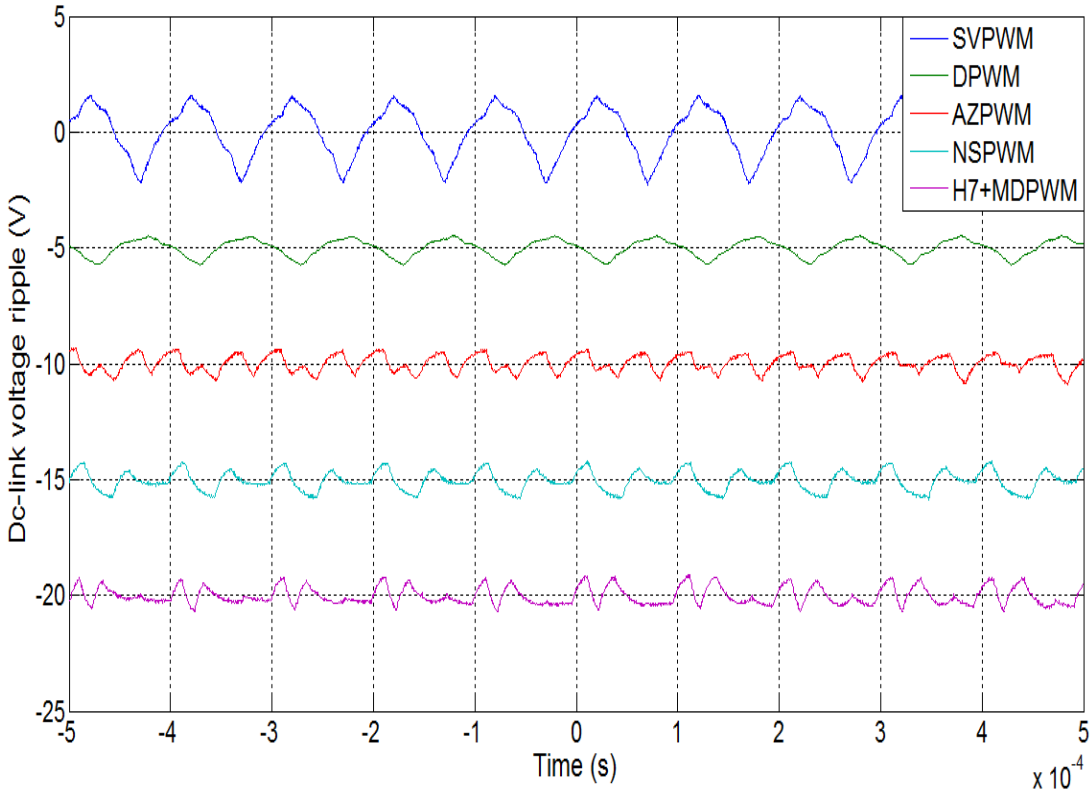


Figure 5.27: Experimental result of dc-link voltage ripples for various modulation techniques.

The THD of the output currents for different topologies are calculated via the FFT analysis of the Matlab/Simulink and summarized in Table 5.4. Although conventional SVPWM and DPWM are expected to have the best THD performance, this is not valid in transformerless PV applications. The high leakage currents of both conventional SVPWM and DPWM increase the current ripples significantly which degrade the THD which reads 19.87% and 10.87% respectively.

Although leakage current is reduced in AZPWM, AZPWM presents relatively higher THD among the recently proposed topologies. This is because AZPWM suffers from the bipolar output voltage and the simultaneous switching of two phases. The bipolar output voltage that changes between V_{DC} and -V_{DC} in certain PWM cycle, doubles the ripples which deteriorates the current THD performance

Even though NSPWM has bipolar output voltage, its reduced switch count pulse pattern (similar to DPWM), which allows NSPWM to switch at higher frequency, has improved the THD performance. As a result, NSPWM has the best THD performance of 5.27% among the other topologies, i.e. SVPWM, DPWM, AZPWM and H7 with proposed MDPWM.

H7 inverter with the proposed MDPWM yields slightly higher THD than the NSPWM due to the simultaneous switching of proposed MDPWM. However, the THD performance is still the best after NSPWM.

Table 5.4: Performance comparisons for various PWM

	SVPWM	**DPWM**	**AZPWM**	**NSPWM**	**H7 with MDPWM**
V_{LL} pattern	Unipolar	Unipolar	Bipolar	Bipolar	Unipolar
Switching frequency(kHz)	10	15	10	15	10
Voltage linearity	0 – 0.91	0 – 0.91	0 – 0.91	0.61 – 0.91	0 – 0.91
Phase current(A_{rms})	2.04	2.05	2.05	2.06	2.04
CMV	0 – V_{DC}	0 – V_{DC}	1/3 V_{DC} – 2/3 V_{DC}	1/3 V_{DC} – 2/3 V_{DC}	1/3 V_{DC} – V_{DC}
Leakage current (mA_{rms})	610	414	240	229	217
DC-link voltage ripples (V)	3.88	1.66	1.68	1.62	1.60
Voltage stress across inductors	V_{DC}	V_{DC}	2 V_{DC}	2 V_{DC}	V_{DC}
Current THD (%)	19.87	10.87	6.43	5.27	5.98

The experimental performance comparisons for all the modulation techniques including the proposed topology are summarized in Table 5.3. Although DPWM is well-known for its superior performance in terms of switching losses, current ripples and voltage linearity, such optimum performance is distorted in transformerless PV applications due to high leakage current. These issues have been solved with the H7 inverter with proposed MDPWM topology.

It is experimentally proven that H7 inverter with the proposed MDPWM combines the superior performance of both DPWM (unipolar line-to-line output voltage, voltage linearity, low output current ripples and low dc-link current ripples, low THD) and RCMV-PWM (reduced CMV with low leakage current). This indicates that the proposed topology has the potential to be applied in three-phase transformerless grid-connected PV applications.

5.8 Conclusion

In this chapter, a three-phase transformerless inverter, adapted from the single-phase H5 topology, is investigated. Since the H5 topology has been conventionally developed for single-phase system, its adaptation in the three-phase system requires the development of corresponding three-phase modulation techniques. Given that a total of seven switches are utilized, this topology is referred to as the H7 topology. Thus, modulation techniques are proposed based on conventional DPWM.

The performances of the proposed PWM, in terms of common-mode voltage (CMV), leakage current, voltage linearity, output current ripples, dc-link current ripples and harmonic distortion are studied and discussed via simulation and experiment. It is proven that the proposed topology is able reduce the leakage current without sacrificing the overall performance of the system. It combines the superior performance of both DPWM (unipolar line-to-line output voltage, voltage linearity, low output current ripples and low dc-link current ripples, low THD) and RCMV-PWM (reduced CMV with low leakage current).

CHAPTER 6

CONCLUSION AND FUTURE WORKS

6.1 Concluding Remarks

This work thoroughly presents the comparison and analysis of various recently-proposed for both single-phase and three-phase transformerless PV inverter topologies.

In single-phase PV system, two strategies have been commonly used for reducing leakage current, i.e. galvanic isolation and CMV clamping. Based on the characteristic of the two strategies, performance of the different topologies can be evaluated. The patented works, such as H5 and HERIC, provide galvanic isolation for safety purpose. Nevertheless, their CMVs are not clamped and leakage currents are not completely eliminated. Other topologies, such as oH5 and H6, eliminate the leakage current with the use of both galvanic isolation and CMV clamping, at the expense of reduced system efficiency. By using ac-decoupling method instead of dc-decoupling method for galvanic isolation, HBZVR and HERIC manage to achieve higher efficiency than the rest but perform poorly in terms of common-mode behavior.

With the understanding on the merits and demerits of the different approaches, a modified HBZVR topology is obtained by addition of a fast-recovery diode. The proposed topology (known as HBZVR-D) combines the advantages of the low-loss ac-decoupling method and the complete leakage current elimination of the CMV clamping method. It is experimentally proven that HBZVR-D topology gives the best overall performance and is suitable for transformerless PV applications for 230V (rms) grid system.

For three-phase PV systems, a three-phase transformerless PV inverter, together with its PWM technique, has been investigated for leakage current reduction. A

MDPWM based on conventional DPWM is proposed here.

Many research works have shown that DPWM has superior performances in terms of dc-link voltage ripples, output current ripples and THD. However, these merits are invalid in transformerless PV applications due to high leakage current. Besides safety issues, the leakage current has deteriorated the overall performances of the PV systems. The present solutions which utilizes RCMV-PWM, solves the leakage current issues by reducing the CMV through the elimination of zero voltage vector switching. However, these RCMV-PWM methods only focus on leakage current elimination while neglecting the overall performance of the PV systems. Issues such as voltage linearity, output current ripples, dc-link current ripples and harmonic distortion have been compromised.

The H7 topology with the proposed MDPWM combines the advantages of both DPWM and RCMV-PWM methods. By reducing the CMV and providing breaking the leakage current conduction path during freewheeling period, the leakage current can be reduced to meet the requirements of the standards without compromising the overall performances of the PV systems. Performance of H7 with the MDPWM is compared with other available RCMV-PWM methods in terms of CMV, leakage current, output current ripples, dc-link current ripples, and THD. It is experimentally proven that H7 topology gives the best overall performance and is suitable for transformerless PV applications.

6.2 Future Works

Suggested future works are listed here as below:

1) Introducing CMV clamping branch into H7 inverter to improve the common-mode behavior.
2) Modulation technique for three-phase transformerless PV H7 inverter can be proposed based on conventional SVPWM. (MSVPWM)
3) A high-performance PWM with reduced CMV and satisfactory overall performance can be proposed by combining MDPWM and MSVPWM.

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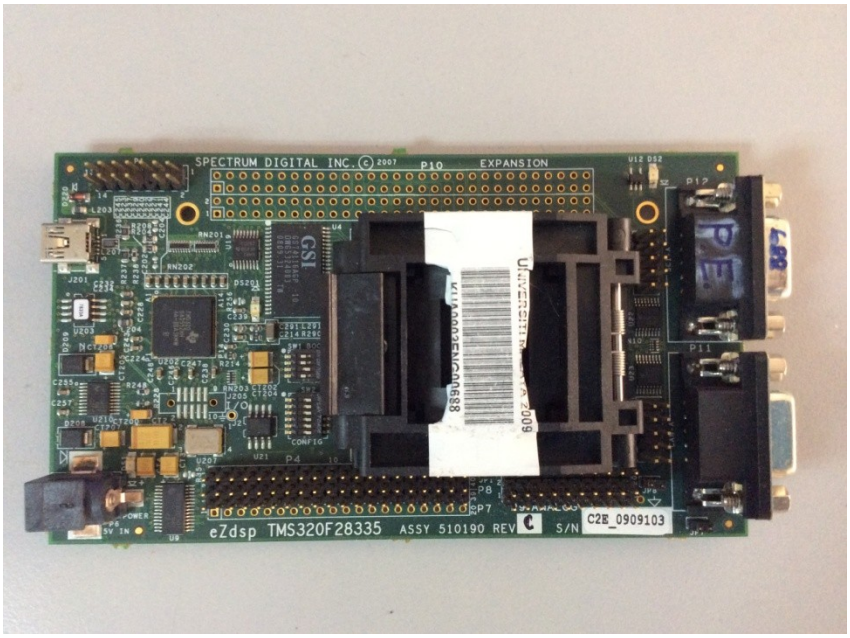
Appendix – Hardware Set Up

62150H Series Programmable DC Power Supply



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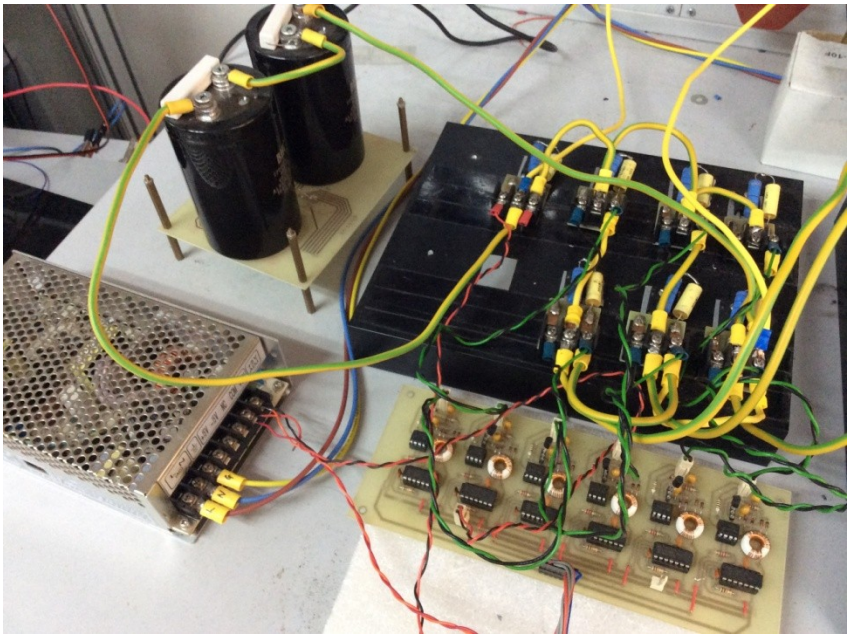

Universal Inverter Prototype