NEGATIVE BIAS TEMPERATURE INSTABILITY AND PERMITTIVITY DEPENDENT DELAY MITIGATION IN HIGH-K METAL OXIDE COMPATIBLE CMOS DIELECTRIC

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ABSTRACT

Negative Bias Temperature Instability (NBTI) and oxide delay are considered as threats to Complementary Metal Oxide Semiconductor (CMOS) transistors. Improving these issues result in improved performance in terms of reliability. In this thesis, to ensure reliability in transistors, the results on the basis of NBTI and oxide delay have been reported by incorporating SiO_2 dielectric with different aged samples of high-K metal oxides. ZnO, TiO_2 and CuO are chosen for the incorporation. NBTI occurs due to negative biasing and high temperature. And, oxide delay occurs due to high resistance and high capacitance inside dielectric. In this thesis the objectives are: to mitigate oxide delay; to mitigate threshold voltage change due to NBTI effect in CMOS device; and having mitigated NBTI in device level, to analyze the compatibility of radio frequency in circuit level considering NBTI effect. Precursor ageing of the incorporated materials is carried out for 2, 3 and 4 days. Each aged sample is treated under UV light for 1, 2 and 3 hours. From the experiments 9 samples are prepared for each type of metal oxide incorporation. From all these samples, the minimum and maximum dielectric constant after ageing and UV treatment were extracted. The minimum valued sample with the lowest dielectric constant is chosen for obtaining the lowest time delay. The maximum value is employed to check threshold voltage increase due to NBTI since a high value of dielectric constant will minimize threshold voltage and will increase the drive current. A PerkinElmer Lambda 35 Filmetrics system, Scanning Electron Microscopy and Energy Dispersive X-ray Microanalysis are employed to characterize the films. For ZnO, results show that the smallest obtainable dynamic dielectric constant is 1.1925 which is found by examining the one hour UV exposed precursor sample after four days. For TiO_2, Results show that the smallest obtainable dynamic dielectric constant is 1.0294 which is found by examining the one hour UV exposed precursor sample after two days.

And, for CuO, Results show that the smallest obtainable dynamic dielectric constant is 4e-08 which is found by examining the one hour UV exposed precursor sample after three days. While exploiting the maximum refractive index in NBTI predictive model, significant improvements were found in TiO_2 and CuO. The extracted dielectric constants parameters from refractive index were employed and simulated inside the predictive model. Under DC stress, exploiting cured sample (4 days aged and 3 hours UV exposed) of TiO_2 results in a 70% increase in drive current and exploiting cured sample (4 days aged and 2 hours UV exposed) of CuO results in 98% increase in drive current. Under AC or dynamic bias stress, exploiting cured sample (4 days aged and 3 hours UV exposed) of TiO_2 results in a 65% increase in drive current and exploiting cured sample (4 days aged and 2 hours UV exposed) of CuO results in 98% increase in drive current. Having been able to perform the device level NBTI induced performance enhancement for cured TiO_2 and cured CuO, a forecasting algorithm was developed for circuit level to predict frequency compatibility under NBTI effect. The analysis is carried out under different radio frequency spectrums. An oscillator was selected as a target circuit to elaborate the NBTI circuit level algorithm which resulted in 2~4 GHz frequency spectrum as the most compatible frequency range for the circuit under NBTI effect since this range obtains highest gain for pure SiO_2, TiO_2 incorporated SiO_2 and CuO incorporated SiO_2. TiO_2 incorporation shows 45% increment in gain over pure SiO_2. And CuO incorporation shows 46% increment in gain over pure SiO_2. This data was found by employing experimentally obtained refractive index data into the developed algorithm.

ABSTRAK

Bagi memastikan keandalan transistor Semiconductor Komplimentari Logam Oksida (CMOS), Ketidakstabilan pincangan negatif suhu dan lambatan oksida dianggap sebagai ancaman kepada Transistor Oksida Logam Pelengkap Semikonduktor (CMOS). Pembaikan isu-isu ini membawa kepada kenaikan prestasi dalam aspek kebolehpercayaan. Tesis in melaporkan kebolehpercayaan dalam transistor, keputusan atas dasar NBTI dan kelambatan oksida dengan menggabungkan SiO_2 dielektrik dengan sampel K-tinggi logam oksida sol-gel. ZnO, TiO2 dan CuO yang berbeza usia dipilih untuk pemerbadanan. NBTI berlaku disebabkan pincangan negatif dan suhu yang tinggi. Serta, kelambatan oksida berlaku disebabkan oleh rintangan yang tinggi dan kemuatan yang tinggi di dalam dielektrik. Kajian ini bertujuan untuk mengurangkan kelambatan oksida dan kesan NBTI dalam peranti CMOS; dan mengurangkan NBTI di tahap peranti, untuk menganalisis kesesuaian frekuensi radio di tahap litar dengan mempertimbangkan kesan NBTI. Prekursor penuaan bahan-bahan yang diperbadankan dijalankan untuk 2, 3 dan 4 hari. Setiap sampel penuaan dirawat di bawah cahaya UV untuk 1, 2 dan 3 jam. Dari kesembilan eksperimen-eksperimen sampel disediakan bagi setiap jenis oksida logam diperbadankan. Dari kesemua sampel-sampel ini, pemalar-pemalar dielektrik minimum dan maksimum selepas penuaan dan rawatan UV telah diekstrak. Nilai minimum sampel yang mempunyai dielektrik rendah dipilih untuk mendapatkan kelambatan masa terendah. Nilai maksimum diambil untuk memeriksa ambang peningkatan voltan disebabkan NBTI kerana nilai pemalar dielektrik yang tinggi akan mengurangkan voltan ambang dan akan meningkat semasa pemanduan arus. Sistem PerkinElmer Lambda 35 Filmetrics, Scanning Electron Mikroskopi dan Sebaran Tenaga X-ray Mikroanalisis digunakan untuk perincian filem. Untuk ZnO, keputusan menunjukkan bahawa pemalar dielektrik dinamik yang paling kecil diperolehi adalah 1.1925 dengan memeriksa sampel precursor yang terdedah kepada UV selama satu jam

selepas empat hari. Bagi TiO_2, keputusan menunjukkan bahawa pemalar dielektrik dinamik yang paling kecil diperolehi adalah 1.0294 dengan memeriksa UV terdedah ke atas sampel precursor selama satu jam selepas dua hari. Dan, untuk CuO, keputusan menunjukkan bahawa pemalar dielektrik dinamik yang paling kecil diperolehi adalah 0.00000004 dengan memeriksa UV terdedah ke atas sampel precursor selama satu jam selepas tiga hari. Dalam mengeksploitasi indeks biasan maksimum bagi NBTI peningkatan yang ketara telah ditemui di TiO2 dan CuO. Di bawah tekanan DC, pengeksplotasian sampel yang tersembuh (4 hari pengusiaan dan 3 jam pendedahan UV) TiO2 membawa kepada peningkatan 70% dalam pemanduan arus dan pengeksplotasian sampel yang tersembuh (4 hari pengusiaan dan 2 jam pendedahan UV) CuO membawa kepada peningkatan 98% dalam pemanduan arus. Di bawah AC atau tekanan biasan dinamik, pengeksplotasian sampel tersembuh (4 hari pengusiaan dan 3 jam pendedahan UV) TiO2 membawa kepada peningkatan 65% dalam pemanduan arus dan pengeksplotasian sampel tersembuh (4 hari pengusiaan dan 2 jam pendedahan UV) CuO membawa kepada peningkatan 98% di dalam pemanduan arus. Setelah dapat melaksanakan peningkatan prestasi NBTI tahap peranti untuk TiO_2 tersembuh dan CuO tersembuh, algoritma ramalan telah dibangunkan untuk peringkat litar bagi meramalkan keserasian kekerapan di bawah kesan NBTI . Analisis ini dijalankan di bawah spektrum frekuensi radio yang berbeza. Pengayun telah dipilih sebagai litar sasaran untuk menghuraikan tahap algoritma litar NBTI yang membawa kepada 2 ~ 4 GHz spektrum frekuensi sebagai julat frekuensi yang paling serasi untuk litar di bawah kesan NBTI kerana julat ini mendapat keuntungan tertinggi bagi SiO_2 tulen, integrasi TiO_2 dengan SiO2 dan integrasi CuO dengan SiO2. Diperbadankan TiO2 menunjukkan kenaikan 45% dalam keuntungan lebih SiO2 tulen. Dan CuO diperbadankan menunjukkan kenaikan 46% dalam keuntungan lebih SiO2 tulen. Data

ini didapati dengan menggunakan data indeks biasan, yang diperoleh daripada ujikaji, ke dalam algoritma maju.

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LIST OF ABBREVIATIONS

Abbreviation	*Signification*
CMOS	Complementary Metal Oxide Semiconductor
CuO	Copper(II) Oxide
EM	Electromigration
HCI	Hot Carrier Injection
LER	Line Edge Roughness
NBTI	Negative Bias Temperature Instability
PBTI	Positive Bias Temperature Instability
RC	Resistive-Capacitive
RD	Reaction-Diffusion
RDF	Random Dopant Fluctuation
TiO_2	Titanium Dioxide
UV	Ultraviolet
WFF	Work Function Fluctuation
ZnO	Zinc Oxide

LIST OF SYMBOLS

Symbol	*Description*	*Unit*
μ_{eff}	Effective mobility	$cm^{-2}/V\text{-}s$
ε_{SiO2}	Dielectric constant of SiO_2	
ε_{Si}	Dielectric constant of Si	
ε_{0}	Electric permittivity of vacuum	F/cm
ε_{IL}	Dielectric constant of the interfacial layer	
C_{ox}	Oxide capacitance	F
F	Frequency	Hz
g_m, G_m	Transconductance	S
I_d	Drain current	A
L	Mask channel length	Mm
N_{it}	Interface trap density	cm^{-2}
n_i	Intrinsic carrier concentration in Si substrate	cm^{-3}
Q	One electron charge	C
R	Refractive Index	-
T	Temperature	^oC
V_d	Drain voltage	V
V_{fb}	Flat band voltage	V
V_g	Voltage applied on the gate	V
V_t	Threshold voltage	V
ΔV_t	Threshold voltage shift	V
W	Mask channel width	µm

CHAPTER 1 INTRODUCTION

1.1 Background

In 1947; John Bardeen, Walter Brattain and William Shockley invented transistor in the Bell Laboratory. It became popular as Bipolar Junction Transistor (BJT) where two junctions of metal semiconductor were connected (Bardeen, 1950). Later in the 60s a voltage controlled metal oxide semiconductor field effect transistor (MOSFET) was invented. This invention replaced current controlled BJT since MOSFET offered very low power consumption. One of the contemporary inventions to MOSFET was integrated circuits (ICs). IC was invented in 1958 by Jack Kilby and Robert Noyce. And in 1963, Frank Wanlass from Fairchild Semiconductor had demonstrated the first complementary metal oxide semiconductor (CMOS) logic gate (NMOS and PMOS). All these inventions allowed designers to place large numbers of transistors inside a single chip having low power consumption. In order to make the system low powered, semiconductor industries have been through significant scaling in transistor dimensions. In 1965, Gordon Moore predicted that the complexity of the ICs will be double every one and half years (Moore, 1965). Though, it appeared unexpected that this hypothesis will come true someday and today it has come true. The first IC produced in the early seventies had only a few hundred transistor. As downscaling continues, the number of transistors in the microprocessor increases as mentioned in Fig. 1.1. And today 15-Core Xeon Ivy Bridge-EX microprocessor has 4.31 billion transistors exploiting 22nm technology. In such constricted dimension reliability issues are becoming important due to different types of transistor defects according to (Bernstein et al., 2006). Undoubtedly, scientists are looking for lowering the process technology since technology scaling will create new opportunities in terms of power and chip area. But if seen from the context of circuit reliability, system performance may get affected due to defects.

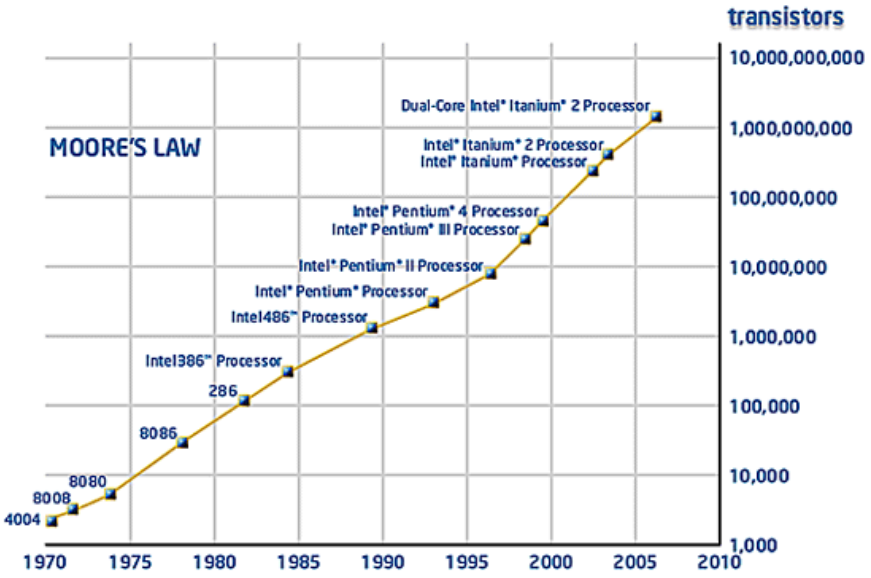


Fig. 1.1 Microprocessor Transistor Counts 1971-2006 [*Source: http://www.intel.com*]

1.1.1 Evolution of CMOS Defect

In order to forecast the future of transistor reliability, it is important to know its past. In 1966 (Dennehy, Brucker, & Holmes-Siedle, 1966) reported a radiation induced defect in MOS transistors. And, a very similar type of charge trapping event was reported in 1967 by (Deal, Sklar, Grove, & Snow, 1967). Before these trapping instability saw a positive outcome, ion contamination was reported in the transistors in late 70s by (Pantelides, 1978). Later this problem of ion contamination was solved by employing clean room in device handling. But charge trapping still remained a problem and researchers continued their work. In the 80s a new problem cropped up in the NMOS due to scaling. Even though the scaling of the device dimensions continued, the source voltage was maintained at a constant 5 V. This resulted in higher electrical field in the drain of the NMOS and this became popular among researchers as hot carrier injection (HCI) (Takeda, Shimizu, & Hagiwara, 1983).

As we mentioned earlier, charge trapping was first reported in 1966 and 1967. In 1967, (Deal et al., 1967) reported the formation of interface charge when negative bias at elevated temperature (350-400) was applied to the gate of transistor. Later this defect was named as Negative Bias Temperature Instability (NBTI) by (Goetzberger, Lopez, & Strain, 1973) & (Nakagiri, 1974). To forecast the physical mechanism, Reaction-diffusion (R-D) (Jeppson & Svensson, 1977) framework has always been one of the prior predictive models for both NBTI and HCI; which was initially developed in the late 70s. Since the classical framework had some flaws, researchers came up with new models based on the classical RD theory. In the 90s the gate oxide thickness reached 3nm and this yielded leakage current inside the transistor. Leakage current was found to form due to excess electric field on a thin oxide layer (Suehle, Chaparala, Messick, Miller, & Boyko, 1994). To solve these problems researchers have been working continuously over the years. Lifetime prediction through modelling, incorporating high-K metal oxides, developing new fabrications methods have been there for the last few decades to overcome these transistors defects.

Now, if seen from the context of crystallography, there are different forms of defects like Frenklen defect, stackling faults, Schottky defects and dislocations during the crystal growth (Sasaki et al., 1996) & (Dadgour, Endo, De, & Banerjee, 2008). When foreign materials are incorporated into CMOS interface, there can be crystalline defects between the interface crystal structure and the structure of foreign material. It happens due to the lattice mismatch of the crystals. To get rid of these defects oxide layers go through a series of purifying process known as gettering steps. Beside this, there are many other types of defects which will be discussed in the next chapter (**Chapter 2**).

For the last two decades, scientists considered charge trapping and intense electric field in the drain region as the major threats for reliable CMOS system (Kimizuka et al., 1999) & (K. Kang, Park, Roy, & Alam, 2007). Fig. 1.2 shows the source voltage as a function of the oxide thickness of gate. The more technology is downscaling, charge trapping issue like negative bias temperature instability (NBTI) limiting region is getting bigger. And in 2 nm region electric field driven defects (like HCI) have less influence under low source voltage. Therefore, in low dimensioned nodes NBTI has more impact to cause damage.

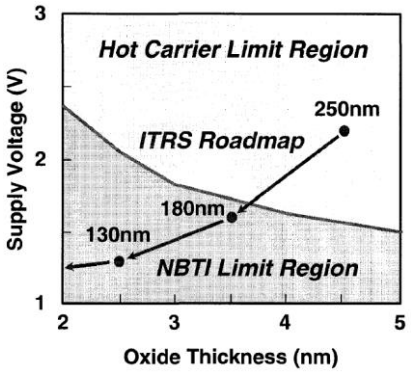


Fig. 1.2 The transition of lifetime limitation mechanisms as a function of gate oxide thickness (Source: (Kimizuka et al., 1999) & (http://www.itrs.net)

Though, NBTI is the dominant defect in very thin oxide layer, resistance of the oxide layer remains very high due to the incorporation of different materials in order to suppress leakage current. This can make the total value of resistance-capacitance (RC) high inside oxide layer and the CMOS circuit operation will become slow. Therefore, it is considered here that NBTI and delay caused due to high-K incorporation onto oxide layer is going to be the future CMOS threats.

1.2 Motivation

As mentioned in the earlier section, two of the most significant reliability factors are NBTI and time delay. So far, many research works have been undertaken to mitigate both of the factors. These research works will be discussed elaborately in the following chapters. But before moving forward into the next chapters, it is imperative to mention that very few research works have been done to mitigate RC delay in device level. On RC delay, researchers have done lots of works in circuit level. But if delay can be reduced at device level from the very beginning, the overall delay in the circuit level can be mitigated further. Now a days, high-K metal oxides are incorporated onto the transistor dielectric to get rid of leakage current. Incorporation of high-K metal oxides increases dynamic dielectric constant and therefore the overall time delay increases since dynamic dielectric constant increases capacitance. From the literature, it is found that in order to reduce time delay, previously researchers exploited only low-K dielectric. Hypothetically, it can be considered that exploiting high-K will increase the delay since dynamic dielectric constant is proportional to the oxide capacitance. But it is still a question, how to decrease the delay incorporating high-K metal oxides.

On the other hand, NBTI is a dominant reliability issue in p-MOSFET and it affects the lifetime. NBTI issue has been taken into account by predictive modelling and guardbanding. Circuit level techniques also have been developed to get rid of NBTI. NBTI exhibits a decrease in drain current and an increase in threshold voltage. Hypothetically, it is considered that a low threshold voltage or a high drain current can mitigate the effect of NBTI as per (J. B. Yang et al., 2010). But, it is a question how NBTI degradation can be further improved by increasing the drive current or decreasing the threshold voltage increment.

Along with this, prediction of circuit's frequency compatibility is a concern since the predictive R-D frameworks fail to explain frequency behaviour due to NBTI effect. As the R-D framework is unable to interpret frequency dependence with NBTI, in circuit level there has not been any research showing the frequency compatibility under NBTI effect. Hence, it is expected that a new technique can be developed to overcome this issue.

1.3 Objectives

CMOS defect generation is a wide spectrum area of research where oxide delay and NBTI are integral parts of it; which affects the lifetime of any type of electronic product. In this research, the goals have been derived from the hypotheses and research questions discussed in the previous section. The objectives are as follows

1) To investigate and reduce dynamic dielectric constant in high-K metal oxide incorporated Si-SiO_2 dielectrics so that oxide delay decreases. As high-K metal oxides ZnO, TiO_2 and CuO were chosen.
2) NBTI induces a positive shift in threshold voltage. Therefore, one of the three objectives is to cure the samples in such a way so that the threshold voltage remains low in a fresh device. Having employed aged high-K metal oxide precursors (ZnO, TiO_2 and CuO) onto the dielectric, to gradually diminish the threshold voltage increment up to a certain degree due to NBTI is one of three objectives of this research.
3) Based on the performance enhancement from Objective (2), to develop a circuit level forecasting algorithm which will predict radio frequency compatibility under NBTI by taking gain transformation into account.

1.4 Organization of the thesis

This thesis is organized as follows:

Chapter 1 describes the background and rationale of this work. A short history relating this work, the major impulse behind this research and the intent of this research has been delineated in this chapter.

Chapter 2 discusses different reliability factors elaborately. The importance of time delay and NBTI are also discussed. And lastly time delay and NBTI mitigation methods done by other researchers are explicated. As it is mentioned earlier that the goal is to improve reliability of the MOS device by analysing the RC delay and NBTI, different reliability issues along with the objected features are discussed. Therefore, an attempt is made to justify the significance of RC delay and NBTI over other reliability factors.

Chapter 3 provides of the comprehensive demonstration of the method in obtaining the objectives. In order to meet the objectives, one common methodology has been designed for both NBTI and RC delay for device level. First, the dynamic dielectric constant is extracted. Based on a wide variety of population of dielectric constant the necessary samples have been selected and exploited to meet the objectives. The methodology is applied in between the conventional CMOS fabrication step. In order to forecast NBTI induced gain transformation in circuit level, a statistical approach is followed and hence an algorithm is developed.

Chapter 4 discusses the results and analysis obtained from the methodology. In order to get the best possible data from a range of population, statistical analysis is performed. Therefore, to verify the data, structural analysis is done using Scanning Electron Microscopy (SEM) and Energy Dispersive X-ray Micro-Analysis (EDXMA). Having done the verification for the obtained data, evaluation was done for NBTI. By comparing degradation due to NBTI with an unincorporated SiO_2 dielectric, the boost in drain current is measured. Based on the drain current improvements, metal oxide exhibiting better NBTI behaviour was employed into the proposed algorithm to analyse radio frequency behaviour in circuit level under NBTI effect.

Having obtained the results and having analyzed it through different means of characterizations, **Chapter 5** explores how to use the device and circuit level techniques to improve the accuracy of NBTI lifetime prediction models, RC circuit topologies and NBTI circuit level mitigation methods. The possible implementations and re-innovations through the means of the proposed technique have been pictured here with analogous estimations and comparisons. Therefore, many RC and NBTI related analogies have been attempted to link with the proposed research techniques. Simultaneously, the proposed work is compared and validated with the previous works.

In Chapter 6, a summary is presented on the work presented in this thesis. Finally the direction for future work is suggested.

CHAPTER 2 LITERATURE REVIEW

2.1 Introduction

In this Chapter, different CMOS reliability factors will be discussed. The list includes work function fluctuation (WKF), random defect fluctuation (RDF), electromigration (EM), line edge roughness (LER), 1/f noise, positive bias temperature instability (PBTI, hot carrier injection (HCI), RC delay and negative bias temperature instability (NBTI). Compared to all these reliability issues, the significance of time delay and NBTI also will be discussed. Time delay and NBTI mitigation methods done by other researchers will be explicated. The reason for incorporating ZnO, CuO and TiO_2 onto the dielectric will be explained. As it has been mentioned earlier that the goal is to improve reliability of the MOS device by analysing the RC delay and NBTI, different reliability issues along with the targeted features will be discussed.

2.2 Work Function Fluctuation

Work Function Fluctuation (WKF) occurs in metallic gate of multiple gate MOSFETs due to manufacturing process. The use of metal as gate material changes the grain orientation. Metal is used as gate material to reduce the leakage current. But while doing device fabrication, the grain orientation of metal is not controllable during the growth of nanoscaled metal grains since the metal grains remain non-uniformly distributed. This changes the threshold voltage and other dependent functions of threshold voltage as per (Y. Li & Cheng, 2012) & (Cheng & Li, 2010).

2.3 Random Dopant Fluctuation

From the basics of electronics, it is known that dopant atoms are diffused in the active regions of transistors to create conductivity. The dopant atoms are not uniformly distributed over the active regions. Because of this statistical variation of the dopant atoms, drain current shifts from its normal value. This fluctuation is termed as random dopant fluctuation (RDF) as per (Asenov, 1998) & (Mizuno, Okumtura, & Toriumi, 1994).

2.4 Electromigration

Electromigration (EM) generally refers to transportation of the carriers inside metal under the influence of an electric field. Inside the metal, the mobility of the carriers creates diffusion according to Nerst-Einstein relationship. This relationship is shown Equation 2.1.

$$v_d = F\mu = F\frac{D}{KT} \tag{2.1}$$

In Equation 2.1, μ is the carrier mobility, D is the diffusivity, K is Boltzmann's Constant, F is the driving force due to electric field and T is the absolute temperature. Diffusion caused due to EM causes loss of connection inside the integrated circuit. Due to miniaturization of the ICs, diffusion takes place since the metal interconnections have a very short distance in between and the high drift velocity due to high current density loses the connections in the metals. The metal interconnects inside a chip are made of grain of lattice. While conducting, the electrons interact with atoms in the lattice. Therefore these lattice change its direction to the direction of the electron flow as

mentioned in (Dziubakiewicz & Buszewski, 2013) & (Yim, Bae, & Kyung, 1999). This results in metal atom deposition in the direction of electron flow according to (Scorzoni, Neri, Caprile, & Fantini, 1991) & (Hau-Riege, 2004). As a result, trap is formed. Due to the formation of trap, mechanical stress is built up and hence, it creates a crack.

2.5 Line Edge Roughness

Due to shrinkage in size, the atomicity of matter inside transistor suffers from substantial variation in characteristics. This fluctuation affects the smoothness of the nanostructures inside the transistor. The fabrication process manifests rough lines due to the fluctuation of the nanostructure. This random deviation of structures from their smooth behavior is referred to as line edge roughness (LER). As per (Asenov, Kaya, & Brown, 2003) & (Asenov, Brown, Davies, & Saini, 1999), when MOSFET transistors are scaled to below 50 nm dimensions, LER becomes the dominant fluctuation factor over RDF and causes deviation in device parameters like threshold voltage and drain current.

2.6 1/f Noise

1/f noise is commonly referred as flicker noise. It is caused due to the spatial and ununiformed distribution of the oxide defects in both low-K and high-K incorporated dielectric as per (Morshed, 2007) & (Xiong et al., 2007). Inside the dielectric the channel carriers maintain a specific frequency. But during penetrating inside and outside of a defect, the frequency of the carrier gets a shift. Defects located near to the interface will have high frequency and vice versa. That also means flicker noise can be reduced if the oxide defects are reduced.

2.7 Positive Bias Temperature Instability

Positive bias temperature instability (PBTI) is an exact complementation of NBTI (Zhang & Eccleston, 1998). It occurs in NMOS where positive biasing and/or temperature shifts the threshold voltage, drain current and mobility. PBTI results in interface trap generation and hence causes shift in transistor parameters.

2.8 Hot Carrier Injection

Like PBTI, Hot carrier Injection (HCI) also manifests the degradation of NMOS device parameters due to the trapping of carriers in the gate dielectric. Hot carriers refer to those carriers (among electrons or holes) which are not in thermal equilibrium with the rest of the crystal lattice in Silicon. This occurs when the electric field in NMOS is very high to change the mean energy as mentioned by (Shah, 1992). The HCI ageing effect causes shift in drain current and threshold voltage at sub-nanometer technology nodes. As the dimension of NMOS shrinks, HCI becomes an increasing concern because supply voltage at the source of NMOS lowers at a slower rate than the length of NMOS channel. The illustration of HCI is shown in Fig. 2.1. Since carriers move from the source towards the drain, the electric field accelerates the mean energy of electrons in NMOS channels. These high energy electrons are referred to as “hot carriers” by (Frey, 1991). The electrons with a high energy passes through the barrier of oxide and result in a trap inside the oxide.

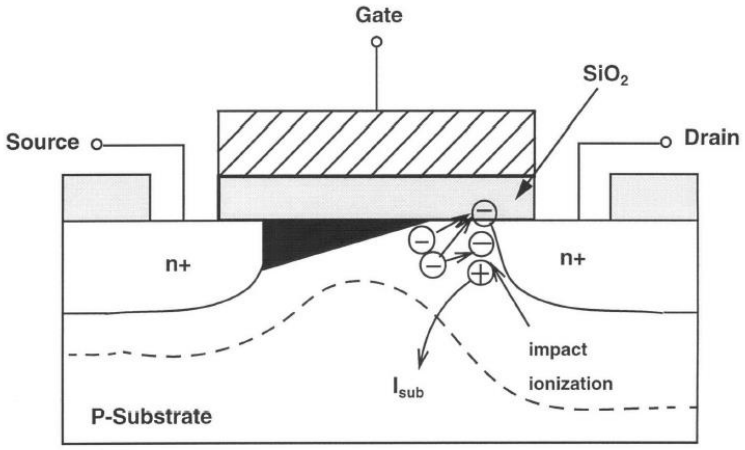


Fig. 2.1 Illustration of HCI

2.8.1 Hot Carrier Injection Models

There are three classical predictive models commonly used by the researchers in the pre-80s, with each model having the same carrier heating mechanism. These three models are: the substrate/drain current ratio model, the substrate current model and the drain–source voltage acceleration model. The substrate current (I_{sb}) is a direct measurement of the impact ionization in the drain region, and hence it is used as a way of carrier heating. In 1985, (Hu et al., 1985) modeled HCI as a function of the ratio of the substrate current to drain current which is expressed in the form of Equation 2.2.

$$T = H(I_{sb})^{-2.9}(I_d)^{1.9}(\Delta V_{th})^{1.5}W \tag{2.2}$$

Here, T is the device lifetime defined as the stress time required for achieving a targeted threshold voltage shift, I_{sb} is substrate current, I_d is drain current, V_{th} is the threshold voltage, W is the channel width and H is the dielectric technology scaling factor. This relationship is derived from fundamental device physics and is calibrated

using empirical data. Equation 2.2 is mainly applicable for long gate length. However, for sub-micron NMOS, Equation 2.3 is more common

$$T * I_d = H(I_B * I_d)^{-M} W \quad (2.3)$$

The above model in Equation 2.3 is used commonly in industry as per (JESD28-1, Association, 2001). Here *M* is derived from experimental data and *H* can be obtained from V_{th}. The third model was proposed by (Takeda, Nakagome, Kume, & Asai, 1983) which is known as drain-source voltage acceleration model. This is expressed in Equation 2.4. It is based on the carrier heating that is due to the voltage applied on the drain and is related to substrate current changes.

$$T = t_0 \exp(B * V_{DS}) \quad W \quad (2.4)$$

Here, t_0 and *B* are fitting parameters. All of the above models were mainly for the sub-micron technology of the 80s decade. As the gate length started shrinking, researchers looked for new models. In 1994, (Kurachi, Hwang, & Forbes, 1994) related drain conductance with HCI and predicted a degradation behavior. But again, this work is only applicable for long channel lengths.

In the year 2005, (Hatzopoulos, Tassis, Hastas, Dimitriadis, & Kamarinos, 2005) described a prediction topology for NMOS polysilicon thin film transistors (TFT). This work was done by characterizing the properties of a damaged region due to stress and hence the (Hatzopoulos et al., 2005) depicted a degradation model related to the carrier mobility of the NMOS.

One of the prediction models, linking drain current and width was shown by (Haggag et al., 2006). This work is one of the first works to depict the effect of energy on HCI. Though, (Haggag et al., 2006) did not focus on circuit energy degradation.

An improvement of classical Reaction–Diffusion (R-D) Model by (Jeppson & Svensson, 1977) was applied to HCI by (Lachenal, Monsieur, Rey-Tauriac, & Bravaix, 2007). (Reisinger et al., 2006) showed that the classical R–D model follows the power law dependency, but in recovery stage the R–D model moves slower and cannot be validated against the experimental data.

2.9 RC Delay

RC delay or oxide delay reduction is a well discussed topic in circuit level. But if time delay in device level can be mitigated, circuit level delay can be mitigated through an extra mile. Work by (Cheong & Jasni, 2007) dealt with device level RC delay in low K dielectric. This work (Cheong & Jasni, 2007) did not exploit any of the transitional metal oxides. Hence, for high-K dielectric there are scopes to do much work. On the other hand, the low oxide thickness in recent MOS transistors is offset by a higher resistance of metal trace and the increased effect of intra and inter-layers of insulating dielectric as per (Wolf, 2002). When resistance becomes high, the total value of signal propagation delay becomes high as well. In such case, the T=RC value can be reduced by lowering the capacitance value as R remains high. As the resistance becomes higher, the time delay given by T=RC also increases. If the resistance remains high, the capacitance must be reduced in order to reduce the time delay.

(Hong, Yang, Jo, Park, & Choi, 1997) attempted to lower the capacitance and dielectric constant in order to achieve higher operating speeds. Since the dielectric constant is directly proportional to the capacitance, reducing the dielectric constant reduces capacitance and therefore time delay. The dielectric constant is reduced by performing successive surface modifications exploiting Trimethylchlorosilane on SiO_2. The samples were prepared using sol-gel method. Trimethylchlorosilane performs surface modification and hence increases porosity. Surface modification was done for 2 hours at a temperature of 60°C. (Hong et al., 1997) obtained a refractive index of 1.26. The problem is that this process is only compatible with larger-dimension transistors and low-K dielectric.

(Almaral-Sanchez, Rubio, & Calderon-Guilleni, 2005) reduced the dielectric constant of thin films by using organic materials. The authors performed sol-gel process on SiO_2. And once it was prepared, they coated it with polymethylmethacrylate. The objective was to modify the surface as done by (Hong et al., 1997). The minimum obtainable refractive index by (Almaral-Sanchez et al., 2005) is 1.36 in low-K dielectric medium. But like (Hong et al., 1997), the authors did not employ high-K metal oxide in dielectric.

Research by (Cheong & Jasni, 2007) explored low-K based dielectrics for time delay reduction. In this work of (Cheong & Jasni, 2007), the results were reported in terms of refractive index where sol–gel derived low dielectric constant SiO_2 was treated with UV light as a function of precursor ageing time and post-deposition UV exposure time. SiO_2 was prepared using sol-gel method and three different samples of gel were

aged for three different days. For different precursor aged samples, the researchers came up with different values of refractive index for low-K dielectric. From this research, the least obtained refractive index is 1.35.

In 2010, (Joshi & Mahajan, 2010) made gains in his attempt to obtain a reduced dielectric constant for Ultra Large Scale Integration (ULSI) applications. The authors exploited Hydrochloric Acid (HCl), Hydrofluoric Acid (HF) and Methylmethacrylate on SiO_2 dielectric. Methylmethacrylate was used as organic material to modify the surface. HCl and HF were used as catalyst during the deposition of SiO_2 sol-gel. Along with HCl, carbon was added which helped to lower the refractive index significantly. Methylmethacrylate were deposited in three different samples with three different concentrations. The least obtained refractive index is 1.313 in low-K dielectric.

Work done by (Joshi, More, & Mahajan, 2010) was able to reduce the dielectric constant in another study by incorporating Methylmethacrylate. It has a similar look like the previous study of the author. The major difference is that it did not consider HCl as a catalyst. Instead of HCl, it considered Carbon incorporated HF as a catalyst. It showed having low concentration of Methylmethacrylate results in least refractive index. The least obtained refractive index is 1.31o in low-K dielectric.

By using Tween 80/Polysorbate (Mhaisagar & Mahajan, 2012) lowered the dielectric constant. The process was a combination of SiO_2 deposition by sol-gel method, incorporation of HF acid to catalyze and the deposition of polysorbate 80 with

different volumetric concentrations. Polysorbate was exploited to modify the surface by increasing porosity. The authors obtained a refractive index of 1.199.

2.10 Negative Bias Temperature Instability

NBTI is a PMOS based reliability factor under inversion mode of operation. It creates a shift in threshold voltage, sub-threshold voltage, mobility, drain current, linear drain current and transconductance. It increases the threshold voltage and therefore the drain current gets reduced. NBTI accelerates with scaling and incorporation of new material. Both the negative gate voltages and/or elevated temperature in PMOS can generate NBTI effect. For NMOS, the parameters shift due to NBTI is negligible for either positive or negative gate voltages according to (Makabe, Kubota, & Kitano, 2000). NBTI occurs due to a large negative bias stress. This stressing ranges from 5 – 12 MV/cm at temperatures starting from the 25°C to elevated temperatures (100° C - 200° C)

.

2.11 Prediction Models for Negative Bias Temperature Instability

This section describes the prior and recent degradation models. These degradation models are mathematically derived equations to forecast the parameter shift after a certain period of time. There are good numbers of research works to explicate the physical mechanism of NBTI. Based on the physical mechanisms, this section reports developed equations to predict the future performance of an NBTI affected device. Having predicted the degradation suitable guardband can be put for better reliability and sustainability. Here the classical reaction- diffusion (R-D) model for NBTI will be discussed along with hole trapping model, two component model, as-grown generation

model, CET mapping model, Tsetseri's model, modified form of R-D model by (Alam, Kufluoglu, Varghese, & Mahapatra, 2007) and modified form of R-D model by (Kumar et al., 2009a).

2.11.1 Reaction Diffusion Model

Jeppson and Svennsson proposed R-D model in 1977 (Jeppson & Svensson, 1977). The model explains a field driven reaction in SiO_2 interface. This reaction impacts the Si-H bond and due to elevated temperature and negative stress, bond energy gets weakened. This either creates a dangling bond and breaks the bond by releasing hydrogen. This model also describes the movement of hydrogen from SiO_2 interface to dielectric. Generated NBTI due to hole-produces interface trap has been explicated by RD model. RD model explains the following equations for NBTI. As per RD model, the degradation is started by the electrochemical reaction at the SiO_2/Si interface, and releases a hydrogenous species which can be both hydrogen ions and hydrogen molecules. The hydrogen ions and hydrogen molecules diffuse away from the interface and create trap to block electron flow. The kinetic equations (Equation 2.5, 2.6 & 2.7) that describes the interface reaction is as below

$$\frac{dN_{IT}(t)}{dt} = k_f(N_0 - N_{IT}(t)) - k_r N_{IT}(t)) - k_r N_{IT}(t) N_H^0(t) \tag{2.5}$$

$$\frac{dN_H}{dt} = D_H \frac{d^2 N_H}{dx^2} \tag{2.6}$$

$$\frac{dN_{IT}}{dt} = D_H \frac{d\ N_H(x,t)}{dx}\Big|_{x=0} \tag{2.7}$$

Equation 2.5 describes the process of reaction whereas equation 2.6 describes diffusion process during the operation of NBTI. Flux condition is described by the third equation (Equation 2.7) when interface trap starts to generate. N_0 denotes the initial number of Si-H bonds before applying the stress in the gate. Acceleration of the reaction from forward and reverse sides are respectively denoted by $k_f$and k_r. After the stress is applied and removed, a certain amount of hydrogen is formed at SiO_2 interface. Concentration and diffusion coefficient of hydrogen is defined by N_H and D_H respectively. NBTI can be divided into two phases namely stress phase and recovery phase and as per (Alam et al., 2007) RD model is unable to predict degradation in recovery phase.

Fig. 2.2 delineates the schematic description of the RD model to interpret trap formation. Broken and dangled Si-H bonds at the Si-SiO_2 interface create interface traps, H+ ion and some H converts to hydrogen molecules, H_2. Interface traps result in NBTI. Thinner oxides bring the polychrystalline silicon gate nearer to the Si/SiO_2 interface and enhance NBTI vulnerability. It happens because hydrogen diffuse away much faster in polychrystalline silicon than that of in oxide (Mahapatra, Bharath Kumar, & Alam, 2003). From the Fig. 2.2, it is clear that if the gate oxide is further scaled down to meet the power and area demand, the interface trap concentration would go high and instigate NBTI effect more and more.

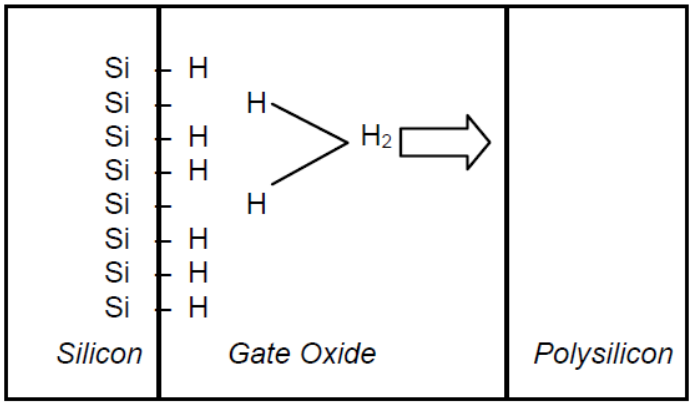


Fig. 2.2 Schematic of the RD model to interpret NBTI induced trap formation

2.11.2 Hole Trapping Model

As per (Tibor Grasser, Goes, & Kaczer, 2009), classical RD model by (Jeppson & Svensson, 1977) cannot reproduce recovery characteristics. This fact was also supported by (V Huard, Denais, & Parthasarathy, 2006), (Reisinger et al., 2006), (Alam et al., 2007), (Tibor Grasser, Gos, Sverdlov, & Kaczer, 2007) & (Kaczer et al., 2008). Therefore, based on the framework of doping and dispersion of hydrogen species, the theory of hole trapping is implemented to explain NBTI. The process of tunnelling is exploited to model the theory of hole trapping. The holes tunnel into pre-existing traps formed due to hydrogen species at various distances near and away from the interface. Hole trapping is independent of temperature and linearly dependent to the stress field according to (Tewksbury III, 1992).

There are many other hole trapping models which are based on the dispersion of activation energies. This results in flicker noise behaviour for a homogeneous distribution inside the dielectric. According to this type of hole traping, the holes are captured via a thermally energized and temperature dependent multi-phonon-emission (MPE) process into interfacial states/border traps (Fleetwood et al., 2002) & (Kirton et al., 1989). The difference between the MPE from the conventional tunnelling is that the

MPE is temperature dependent and its mechanism is negligibly dependent on electric field. Hence, due to this non-field dependence, it is not easy to use MPE to interpret NBTI. An extension of the MPE is the multiphonon-field-assisted tunnelling (MPFAT), which is described in (Makram-Ebeid & Lannoo, 1982) & (Ganichev, Prettl, & Yassievich, 1997). Here the mechanism is dependent on electric field. Fig. 2.3 presents the energy band diagram of the MPFAT hole trapping process.

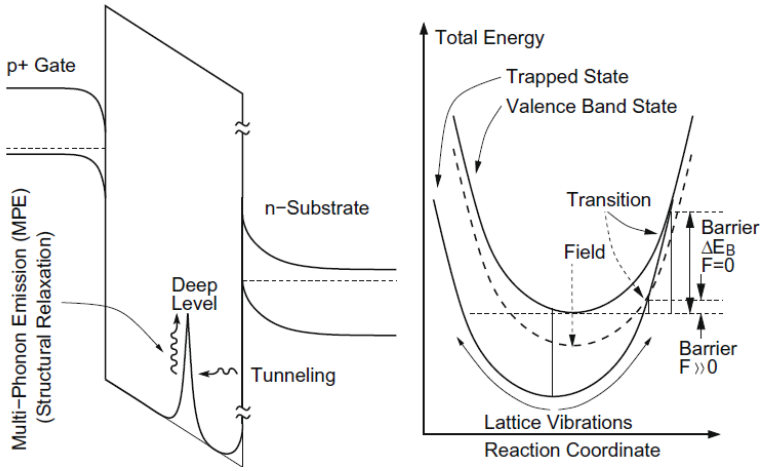


Fig. 2.3 The multiphonon-field-assisted tunneling (MPFAT) process used. Tunneling into deep states is only allowed when the excess energy of holes can be released via a multiphonon emission process during structural relaxation through the dependence of temperature and electric field (Tibor Grasser, Kaczer, et al., 2009)

Hole trapping follows the first order reaction model with two well separated capture cross sections, σ according to Equation 2.8:

$$N_e = \sum_{i=1}^{2} N_i \left[1 - e^{Qh\sigma_i}\right] \qquad (2.8)$$

Ne is the effective density of trapped holes by assuming all traps are at the oxide/Si interface (Zhang, Sii, Groeseneken, & Degraeve, 2001), (Zhang et al., 2004), (Zhang, 2009) & (Zhang et al., 2002). N_i is the saturation level of traps with a captured cross section of σ_i. *Qh* is the number of holes injected into the oxide that can fill traps. The

two extracted capture cross sections are in the order of 10^{-13} ~ 10^{-14} cm^2 and 10^{-15} cm^2, respectively (Zhang et al., 2001), (Zhang et al., 2004), (Zhang, 2009) & (Zhang et al., 2002). However, the concept of hole trapping can be easily eliminated since it does not comply with the intial experimental data of 1s as per (Deora, Maheta, & Mahapatra, 2010).

2.11.3 Huard's Two Component Model

As per (V Huard et al., 2007) from STMicroelecronics, NBTI is made up of two independent constituents. These are namely the recoverable component and the permanent component and each of these exhibits variable levels of voltage, temperature and process dependences. Fig. 2.4 shows the schematic of the model. The permanent component consists of equal proportions of the interface states and positive fixed charges. The permanent component reaches total recovery after long thermal annealing process according to (Vincent Huard, 2010).

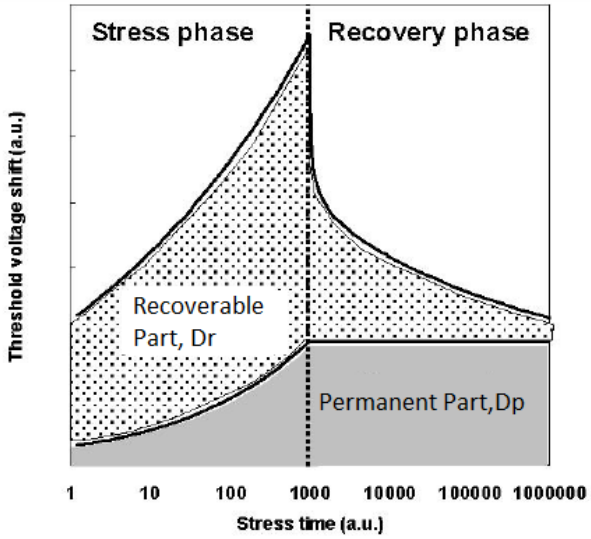


Fig. 2.4 NBTI degradation having permanent and recoverable parts (V Huard et al., 2007)

2.11.4 As-Grown Generation Model

Ageing analysis by exploiting dc-based characterization exhibits inaccuracies due to the error in recovery data which occurs during the measurement of the device. Hence, the use of ultra-fast pulse measurements came into account where the interval measurement period was reduced to the magnitude of microseconds to measure gate voltage acceleration of CMOS device. Report by (Ji, Lin, Zhang, Kaczer, & Groeseneken, 2010) mentioned significant inaccuracies of the ageing prediction. At the worst case when the recovery is suppressed and the gate voltage-acceleration method was used, the model did not comply with experimental data.

2.11.5 CET Mapping Model

The model by (T Grasser et al., 2011) captured the BTI degradation mechanism during DC stress and dynamic stress. It also captured the NBTI mechanism in recovery stage. The model is an inspiration from the theory of capture/emission time (CET) maps by (Reisinger, Grasser, Gustin, & Schlunder, 2010) & (Reisinger et al., 2011). CET maps are used to extract NBTI-relevant defect parameters. The extraction of capture and emission time constants (τ_c and $\tau_{e)}$ refer to stress and recovery time respectively and these were presented in previous works by (V Huard, Parthasarathy, & Denais, 2005) & (Ma, Chiu, Tang, Wang, & Chang, 2009). Change in threshold voltage is measured by integrating the CET maps from 0 to τ_c and τe to ∞.

2.11.6 Tsetseri's Model

Tsetseri's model is a proton based dissociation model by (Tsetseris, Zhou, Fleetwood, Schrimpf, & Pantelides, 2005). This model explains NBTI induced Si-H bond breaking in the oxide dielectric. According to (Tsetseris et al., 2005), the removed hydrogen species transport to a far located Si-Si bond. But this process of transportation increases the energy of the system by 1.9eV. The interlayer barrier leads the dissociation activation energy of 2.4eV. This value complies with the experimental data which is 2.6 eV as found by (Zhang, Ji, Chang, Kaczer, & Groeseneken, 2007). This activation energy reduces to 2.1 eV with the presence of holes. At negative voltage, the free protons move to the oxide interface. The energy barrier to cross the oxide interface is very high (1 eV). As a result, the protons transport along the interface. When the hydrogen atom diffuses faster than the molecular hydrogen in the dielectric, Tsetseris' model results in a time exponent of n = 0.25 (Chakravarthi, Krishnan, Reddy, & Krishnan, 2007). This does not comply with the measurement data of (Entner, 2007).

2.11.7 Modified RD Model by Alam

As per(Alam et al., 2007), NBTI is interface trap driven phenomena associated with broken Si-H bonds and it does not state the impact of recoverable portion after the impact of stress voltage. Though (Alam et al., 2007) summarizes the pre-2003 literatures and based on that the authors reinterpreted RD model with the help of 2003-2005 models (Sufi Zafar, Lee, & Stathis, 2004) & (Tsetseris et al., 2005). From the pre-2005 literatures (Alam et al., 2007), developed new features of NBTI which are incompatible with the definition of the classical RD model. Hence, the reinterpretation of this model took place, which gives a solution for the contradictions of those seven key features. Though the re-puzzled form of RD model explained stress time exponent, activation energy, field acceleration and frequency independence which comply with

the key features of NBTI. But, this model fails to predict the initial recovery phase as stated by (Kumar et al., 2009a).

2.11.8 Modified RD Model by Kumar

DC Stress

According to (Kumar et al., 2009a), if the time required for hydrogen to diffuse to poly is equal or more than the total time frame of calculation, then density of interface traps is given as per Equation 2.9,

$$N_{IT} = k_{IT}(2D_{ox}t)^{1/6} \tag{2.9}$$

And if the time required for hydrogen to diffuse to poly is equal or more than the total time frame of calculation, then density of interface traps is explained as Equation (2.10),

$$N_{IT} = k_{IT}(D_{ox}(1+f)) + \sqrt[1/3]{2 * D_p(t-t_1) * f} \tag{2.10}$$

and the change in threshold voltage is as per Equation 2.11,

$$v_{th} = q * N_{IT}/c_{ox} \tag{2.11}$$

Here,

D_{ox}= Diffusion coefficient in the oxide; D_p=Diffusion coefficient in the poly; k_{it}=Reaction Rate; e_0=vacuum dielectric constant; c_{ox}= dynamic dielectric constant*e0/oxide thickness.

AC Stress:

According to (Kumar et al., 2009a), if the time required for hydrogen to diffuse to poly is equal or more than the total time frame of calculation, then density of interface traps is given by Equation 2.12,

$$N_{IT} = k_{IT}((\frac{N_{IT}T}{k_{IT}})^6 + (2D_{ox}t))^{1/6} \quad (2.12)$$

Otherwise it follows Equation 2.13,

$$N_{IT} = k_{IT}((\sqrt[6]{\frac{N_{IT}T}{k_{IT}}}) + (2D_{ox})^2) + \sqrt{2 * D_p(t - t_1)} \quad (2.13)$$

$N_{it}T$= Interface trap after time T (T=2*180 degree)

2.12 Applicability of Kumar's Model

According to (Kumar et al., 2009a), an NBTI predictive model must predict the number of interface traps, must be able to capture the initial recovery phase, must predict a higher fractional recovery for a PMOS device with a larger oxide thickness for the same duration of stress. The model must predict larger fractional recovery with lower stress times (in AC) and must be frequency independent. These are the key issues typically absent in other NBTI models. Most importantly, the model by (Kumar et al., 2009a) complies well with experimentally obtained data as per Fig. 2.5. by (Krishnan et al., 2005). Fig. 2.5 shows the stress and recovery phase of the model in blue line. '◊' refers to the experimental data for interface trap N_{it}. The experimental data of N_{it}

matches with the blue curve obtained from the model. Moreover, the model by (Kumar et al., 2009a) takes all the above mentioned physical features into account. Therefore, to minimize the NBTI induced threshold voltage the model by (Kumar et al., 2009a) will be exploited in this research.

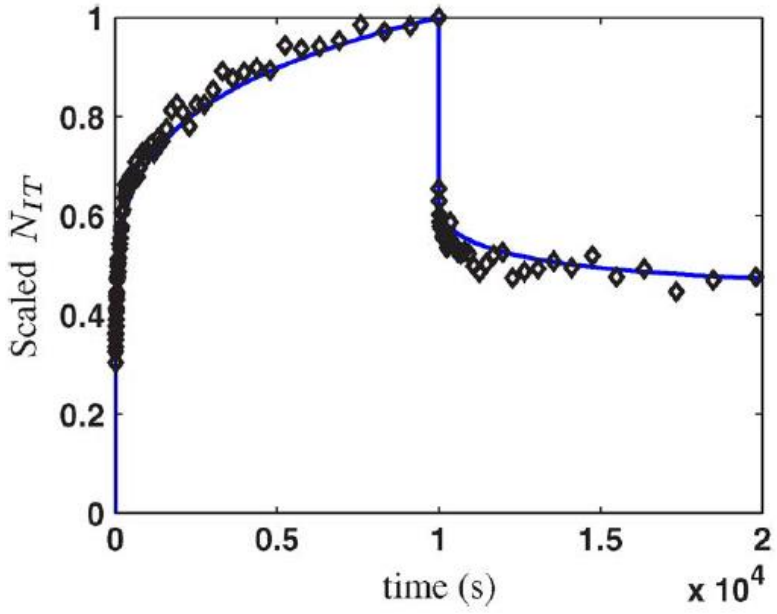


Fig. 2.5 Experimental data for interface trap over time by (Krishnan et al., 2005) complies with (Kumar et al., 2009a). The blue line is obtained from the model and the dotted points refer experimental data.

2.13 NBTI Mitigation Techniques

Works by (X. Chen, Wang, Cao, Ma, & Yang, 2009) & (Kumar, Kim, & Sapatnekar, 2009b) reported that rather than using a fixed guardband over the entire lifetime, ageing can be reduced by using a lower supply voltage in the early lifetime and by increasing the supply as necessary to counter ageing. Power or ageing benefits of using a lower voltage in the early lifetime, but degradation soon converges to long time framework as per (Chan, Sartori, Gupta, & Kumar, 2011).

(Srinivasan, Adve, Bose, & Rivers, 2004) and (Srinivasan, Adve, Bose, & Rivers, 2005) monitored and adapted to the estimated lifetime and makes sure that a circuit reaches a desired lifetime target before failing. These circuit techniques predict ageing by averaging failure over the entire lifetime. It assumes that degradation happens steadily over processor lifetime, rather than in a front-loaded nature. This may lead to inaccuracies.

In 2010, (L. Li, Zhang, Yang, & Zhao, 2010) described a mitigation of NBTI in the recovery stage where the focus was on the critical transistors in a circuit. Rather than directly mitigating the change in NBTI degradation, this method emphasizes on the recovery of a degraded device in a microprocessor circuit. It is a work done to find out the worst case transistors in circuit and cure them. The work did not implement any method to prevent NBTI degradation rather it cures the degraded transistors due to NBTI.

(Yu Wang, Chen, et al., 2011) optimized ageing and leakage power. It is a circuit level technique which is mainly based on delay relaxation in the circuit but it did not consider the change in threshold voltage in device level. If device level threshold voltage shift can be mitigated, the overall circuit level NBTI can be mitigated.

Another circuit level technique was employed by (Yu Wang, Luo, et al., 2011). Though the authors implemented a device level model but the overall mitigation was performed in the circuit level. Like (Yu Wang, Chen, et al., 2011), this work considered

the impact of leakage current. But, had NBTI been mitigated in device level, this technique could have been implemented with better result.

Stress memorization technique (SMT) is one of the ways to enhance device level performance under reliability constraints as per (C.-H. Chen et al., 2004). The objective of this technique is to increase the drive current through stress enhancement. Poly amorphorization implantation and activation capping layer is used to increase stress. An increment of 15% drive current was obtained using this process.

Dual stress liner (DSL) technique was opted by (H. S. Yang et al., 2004). Conventionally, one FET is stressed with one type of liner (Si_3N_4) and the other FET is degraded or not stressed. But (H. S. Yang et al., 2004) stressed both of the FETs by applying stress liners simultaneously. For PMOS this technique exhibits a drive current of 32%.

Wang et al. in 2012 (Yao Wang, Cotofana, & Fang, 2012) demonstrated a FinFET based technique to mitigate NBTI. The authors used a separate gate to control threshold voltage. Undoubtedly a good technique to control the change in threshold voltage but employing an additional gate will take an extra area while implementing the overall circuit.

Based on the impact of stress on NBTI, (J. B. Yang et al., 2010) came up with a solution on NBTI degradation on stress temperature and stress voltage. This technique

is an optimization between the gate voltage and operating temperature to suppress NBTI induced threshold voltage up to a certain level. This method decreases threshold voltage of PMOS by 19%, which also depends on stress time, stress temperature and stress voltage. It is expected to decrease the threshold voltage further in this proposed research.

Having looked into the above literatures the following limitations are found:

1) Many of these works are circuit level/ architectural level techniques. Architectural level techniques are subject to the design of the circuits. If device level NBTI can be mitigated, all these circuit level works can be reduced further.

2) two of the device based works by (Yao Wang et al., 2012) & (H. S. Yang et al., 2004) exploited another device to control the parameter degradation due to NBTI. Using another device will take an extra area and increase power dissipation.

3) SMT & SDL technique resulted in a threshold voltage reduction of 15% and 32%.

4) The literature of (J. B. Yang et al., 2010) and worked on device level and by applying stress proximity technique (SPT) it reduced threshold voltage reduction by 19%.

5) SMT, SDL and SPT will be taken as the benchmarks to compare by mitigating NBTI further in **Chapter 5**.

2.14 Significance of RC Delay over other Reliability Issues

From the previous works it has been observed that NBTI, PBTI and HCI are basically related to either PMOS or NMOS. But, RC delay can result in electrical parametric change in both N and PMOS. Having studied the literary work on RC delay, it was found that the previous efforts focused mainly on reducing the dielectric constant in a low-K medium. But, high-K dielectrics are important when dealing with leakage current and boron penetration. Now days, high-K metal oxides are widely incorporated into transistors and there is still scope to lower the dielectric constant by considering the effect of high-K metal oxides.

2.15 Significance of NBTI over other Reliability Issues

As per (R Mishra, Ioannou, Mitra, & Gauthier, 2008), NBTI is the most dominant among NBTI, HCI and PBTI. In comparison with HCI and PBTI, for lower technology nodes, NBTI is the most catastrophic reliability issue to cause shift in threshold voltage, drain current, linear drain current, saturation current, channel mobility, subthreshold slope, off current and transconductance as per (Islam & Alam, 2011) & (Rahul Mishra et al., 2007). Hence, along with RC reliability issue NBTI is also considered in this work.

2.16 Use of High-K in CMOS

For leakage current reduction high-K is generally used in CMOS. There are other applications of high-K which will be discussed in the next sections. Over here, the problems with high-K will be discussed in brief as per (Chau, 2003).

2.16.1 Issues with High-K Incorporation

(Chau, 2003) figured out the following issues with high-K incorporation in CMOS.

1. High-K ignites the threshold voltage to go too high when Polychrystalline-silicon is used as the gate material. This boosts up the NBTI induced threshold voltage.
2. When hydrogen species are broken away from Si, Si forms a bonding with high-K metal and creates defect as per Fig. 2.6. This reduces the mobility and increases threshold voltage as per Fig. 2.7 and Fig. 2.8.
3. High-K metal oxides increase dielectric constant and hence capacitance. Once, capacitance increases, delay increases in the device since T=RC.

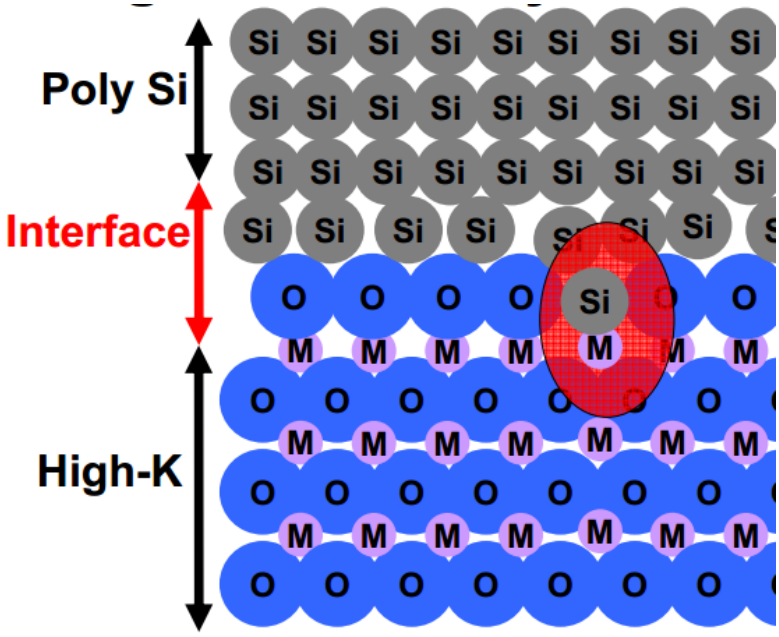


Fig. 2.6 Schematic showing formation of defect due to high-K incorporation in SiO_2 dielectric

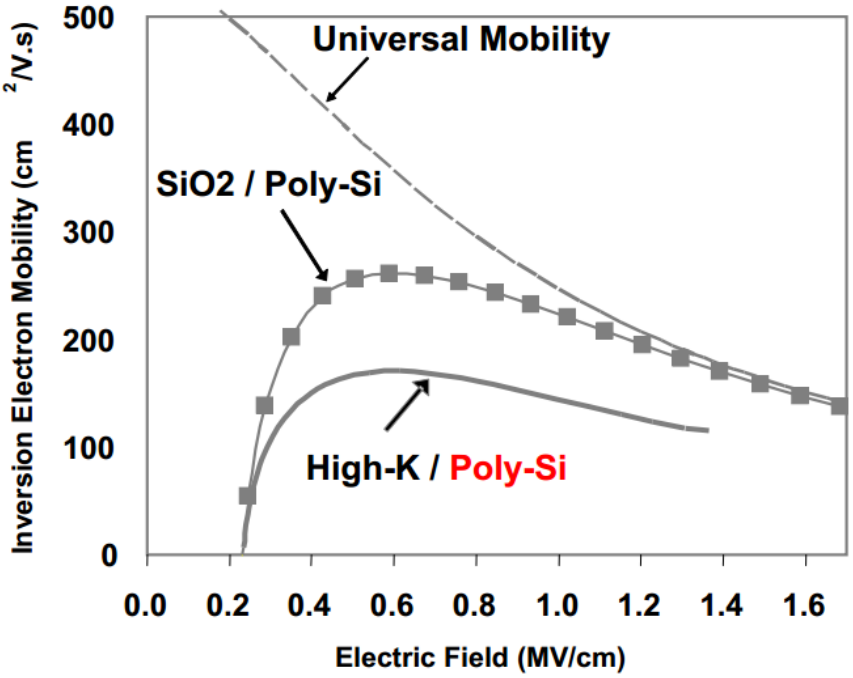


Fig. 2.7 Mobility degradation due to the incorporation of high-K

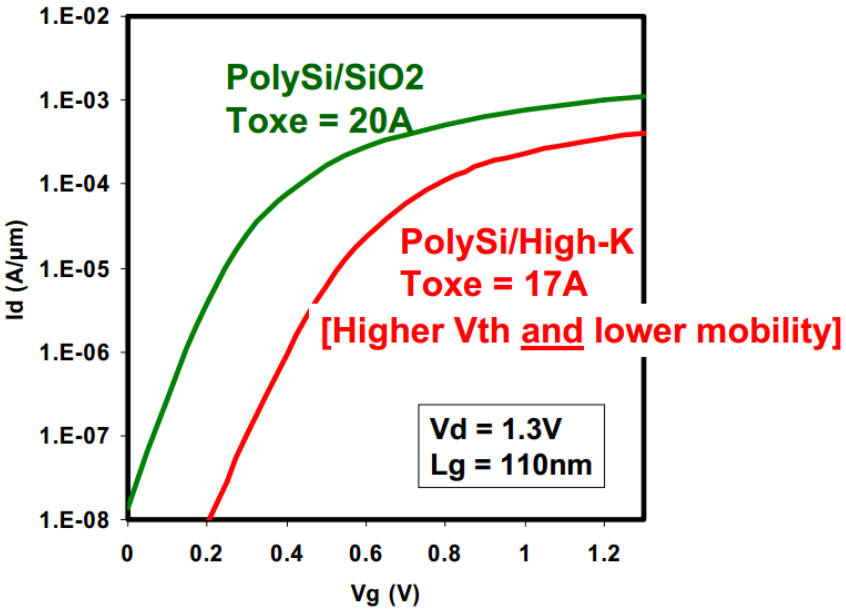


Fig. 2.8 Drain current degradation due to the incorporation of high-K in dielectric of the transistor

2.16.2 Possible Hypothetical Solution for NBTI & RC under High-K Incorporation

Having been through the problems with high-K incorporation, it is imperative to come up with a hypothesis which can lead to a solution of the problem. The proposed research work initially mentioned the following problems.

- RC delay in device due to the incorporation of high-K
- NBTI induced threshold voltage increment due to leakage current which is the result of high-K

From the literatures of RC delay, it is found that the previous literatures are based on low-K dielectric where deposition of foreign organic and inorganic materials took place. (Cheong & Jasni, 2007) is an exception in this regard since it did not deposit any foreign material to meet the objective. The literature by (Cheong & Jasni, 2007) focused on curing device dielectric through sol-gel ageing instead of modifying surface with different organic or inorganic materials. The method of (Cheong & Jasni, 2007) is able to reduce the amount of refractive index in low-K dielectric. On the other side, incorporation of different organic and inorganic element can lead to defect due to a possible electrochemical reaction with high-K metal oxides. Hence, hypothetically it can be stated curing device dielectric through sol-gel ageing can result in reduced value of time delay.

Increment of threshold voltage under high-K incorporation and under NBTI effect is a concern for researchers. And as per the NBTI prediction model by (Kumar et al., 2009a), a high value of oxide capacitance will result in a low threshold voltage. A high

oxide capacitance can be obtained by taking the sample with a high refractive index. And this will result in a high drain current and low threshold voltage.

2.17 Reasons for Employing the Targeted High-K Oxides

Exploiting high-K materials in SiO_2 is of great advantage due to the following reasons.

- High-K materials exhibit low bandgap energy since K (permittivity) is inversely proportional to bandgap energy.
- High-K materials help to mitigate wearout mechanisms like leakage current.
- High-K materials manifest thermal sustainability.

Due to the above reasons, high-K metal oxides are often used in the SiO_2 dielectric of the transistors. Here, different high-K metal oxides and their use to mitigate the reliability issues will be discussed. These reliability issues which are also known as transistor defects show resonant properties as per (Jason P Campbell, Lenahan, Cochrane, Krishnan, & Krishnan, 2007) & (J P Campbell, Lenahan, Krishnan, & Krishnan, 2007). And, shift in resonance results in shift in electrical parameter. Due to oxide defects, the shift in electrical parameters is more in pure SiO_2 interface.

Studies (A. Y. Kang, Lenahan, Conley, & Solanki, 2002), (Kirsch et al., 2006) & (Triplett et al., 2007) based on Electron Spin Resonance (ESR) experiment reports that the exploitation of high-K results in less change in resonance. Moreover, another study

by (Stesmans & Afanasev, 2003) shows that there has been lesser resonance shift in high-K induced dielectric compared to the conventional SiO_2 dielectric. Based on the literatures in (A. Y. Kang et al., 2002), (Kirsch et al., 2006), (Triplett et al., 2007) & (Stesmans & Afanasev, 2003); it can be said that incorporating high-K can mitigate the interfacial defects like NBTI, HCI, EM and PBTI up to the minimal level. But, in case of RC delay it is needed to reduce the value of permittivity to reduce capacitance. Hence, in high-K material incorporated dielectric, reducing permittivity becomes a challenge. Hence, one of the objectives in this research focus on mitigating RC delay in high-K dielectric.

For this research, ZnO, CuO and TiO_2 was selected and the reasons for employing this into dielectric will be explained here.

According to (Seo, Song, An, & Kim, 2013), among the various binary oxide materials, ZnO shows excellent resistive switching behaviors like fast switching, large on/off resistance ratio, and good reproducibility. And, (C. Chen, Pan, Wang, Yang, & Zeng, 2012) supported the compatibility of ZnO in CMOS technology. As per (Mourey et al., 2009), ZnO is compatible for thin-film applications because it allows high-mobility thin-film-transistors using low-temperature deposition processes. Moreover, ZnO is abundant in nature and is inexpensive. Apart from all these reasons, ZnO based CMOS transistors have been found effective for many applications like gas sensing and ethanol sensing according to the reports by (Pan, Zhao, Bermak, & Fan, 2012) & (Santra et al., 2010). There are works on ZnO combining with CMOS technology based on microwave frequency as mentioned in (Bayraktaroglu, Leedy, & Neidhard, 2009).

Therefore, it can be said that incorporation of ZnO onto CMOS dielectric has significance.

TiO_2 is one of those binary metal oxides which is used because of its stability, wide range of temperature compatibility and switching capability as per (Lee, Ho, & Yao, 2011) & (Argall, 1968).

According to (Liao et al., 2009)CuO is one of those binary metal oxides which is used for gas sensing applications since gas sensors made from CuO exhibit high response to CO gas in air at 200◦C.

2.18 Refractive Index of the Targeted High-K Oxides

Refractive index is the common parameter to decide performance for both RC and NBTI. The target of this project is to change the refractive index of different dielectric samples through sol-gel ageing. But, before curing mechanism is applied on the samples, it is imperative to know the behavior of refractive index under normal case (without ageing and adhesive UV exposure). Fig. 2.9, 2.10 & 2.11 depict the values for refractive index for ZnO, TiO_2 and CuO respectively under normal condition.

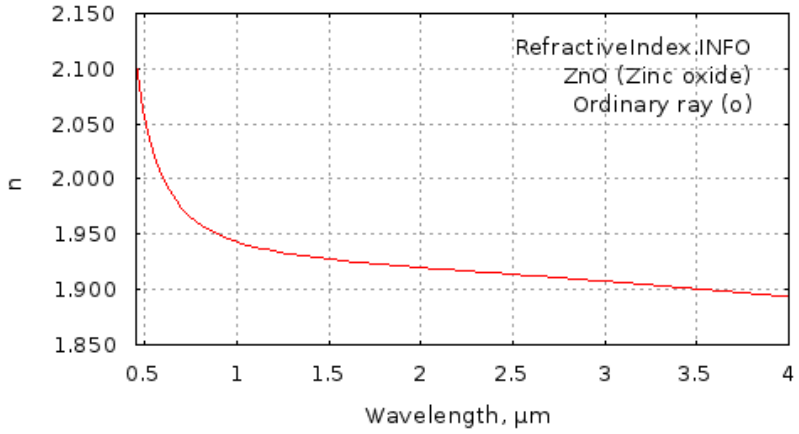


Fig. 2.9 Refractive index for ZnO under normal condition

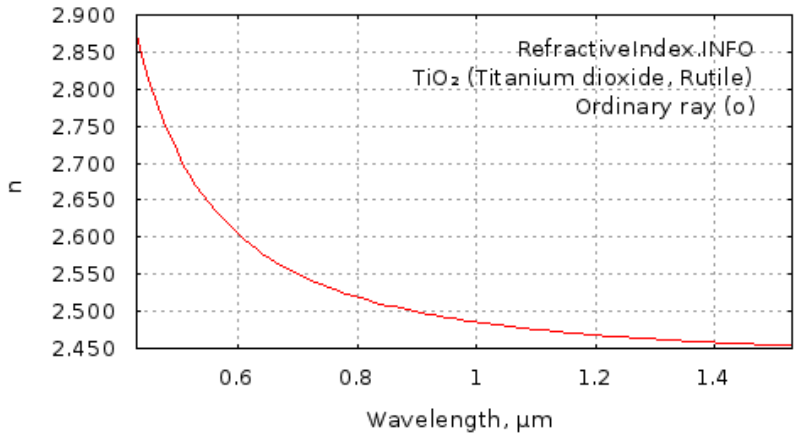


Fig. 2.10 Refractive index for TiO_2 under normal condition

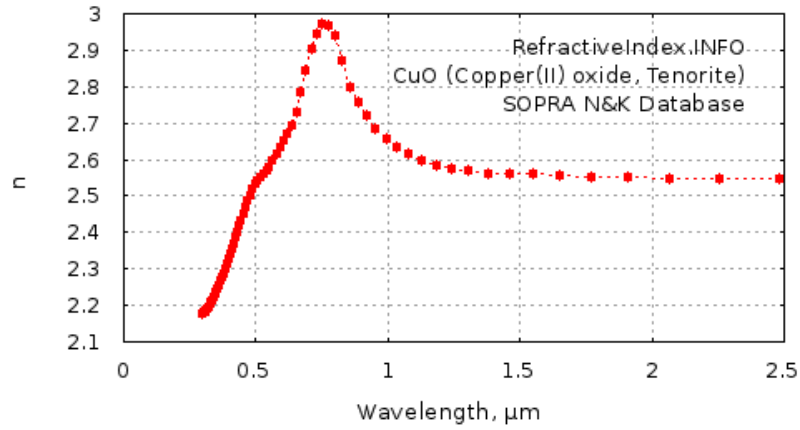


Fig. 2.11 Refractive index for CuO under normal condition

2.19 Conventional CMOS Fabrication Step

Before proceeding for the next chapter to impart methodology, it is imperative to have a look into the conventional fabrication steps since the proposed research will be employed inside the conventional fabrication steps. The conventional CMOS fabrication steps followed by the academia and the industry are more or less similar. The steps are shown below In Fig. 2.12 as per (Hsieh, 1983) and ("CMOS Processing," 2013). The proposed research will be employed in between Fig. 2.12(a) and 2.12(b).

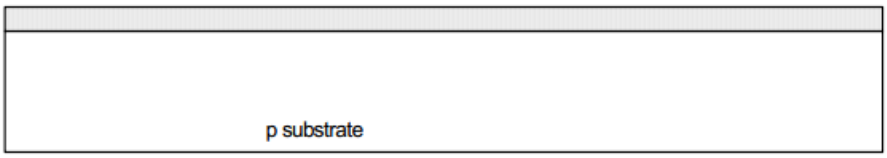


Fig. 2.12(a) Incorporation of high-K metal oxide on SiO_2 coated p-substrate

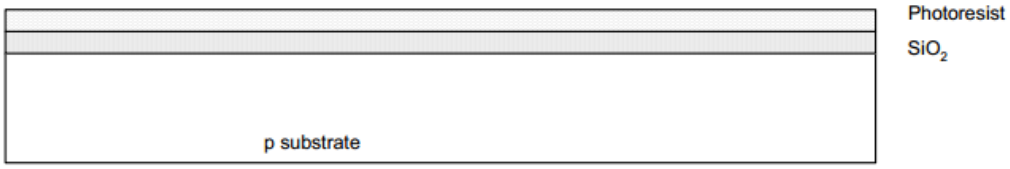


Fig. 2.12(b) Applying photoresist on high-K incorporated SiO_2

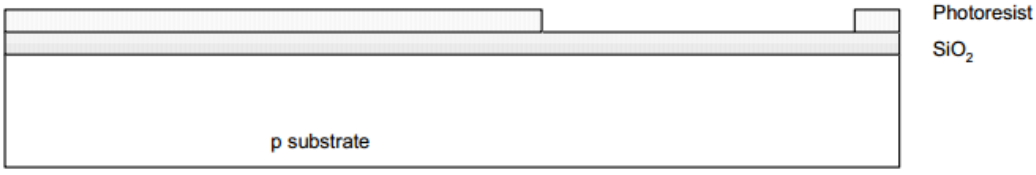


Fig. 2.12 (c) Stripping photoresist using organic solvents

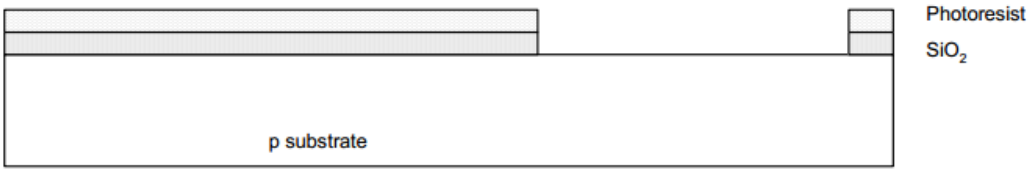


Fig. 2.12 (d) Etching remaining photoresist and SiO_2 using acid

Fig. 2.12(e) Formation of n-well using diffusion process

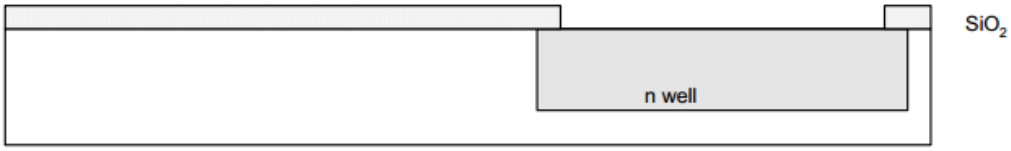


Fig. 2.12(f) Formation of n-well using diffusion process

Fig. 2.12(g) Stripping off the oxide using HF

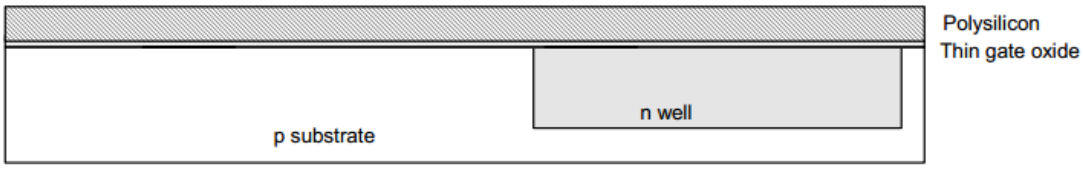


Fig. 2.12(h) Reformation of high-K incorporated gate oxide with polysilicon on it

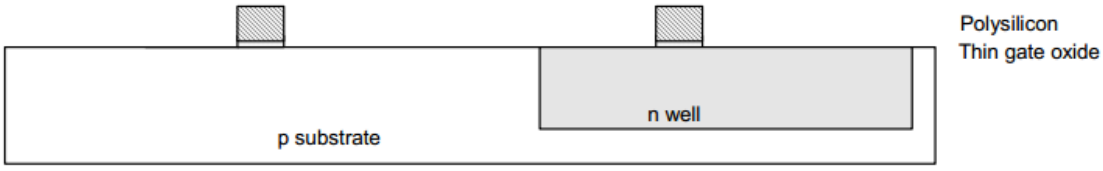


Fig. 2.12(i) Patterning poly

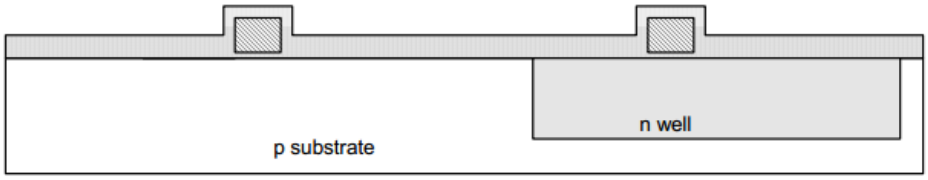


Fig. 2.12(j) Defining n-diffusion region

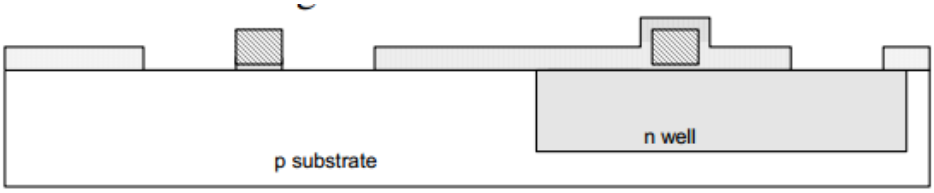


Fig. 2.12(k) Pattering oxide using n+ active mask

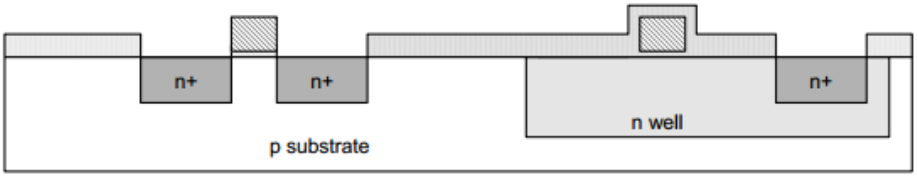


Fig. 2.12(l) Formation of n diffusion region

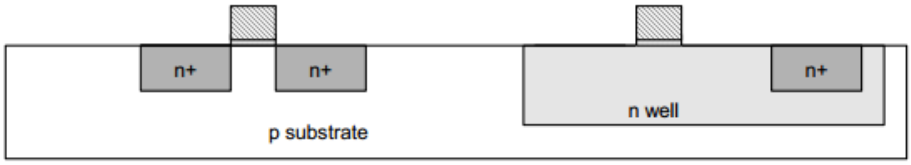


Fig. 2.12(m) Stripping off the oxide on the poly

Fig. 2.12(n) Formation of p diffusion region

2.20 Summary

The objective of this chapter was to support the research questions and to support the proposed methodology in **Chapter 3**. At the beginning of this Chapter different types of reliability issues are discussed to give a clear idea about MOS defects. Based on the literature works it is found that NBTI and RC delay are two of those factors to create maximum damage. Therefore, NBTI and RC delay is discussed with an extra emphasis. Along with the basics of the reliability factors, NBTI and RC delay mitigation techniques are discussed in this chapter. Different NBTI models are explained and out of those models the most applicable model was chosen for this work. Issues related to high-K incorporation are discussed and hence, the possible hypothetical solutions for those problems are reported. At the end, the discussion was focused on the reason behind employing ZnO, CuO and TiO_2 in CMOS.

CHAPTER 3 METHODOLOGY

3.1 Introduction

This chapter describes the methodology in order to obtain the objectives of this thesis. The methodology is shown by depicting a flow chart. The flowchart shows a series of experimental procedures which is also described in detail.

3.2 Overall Project Method

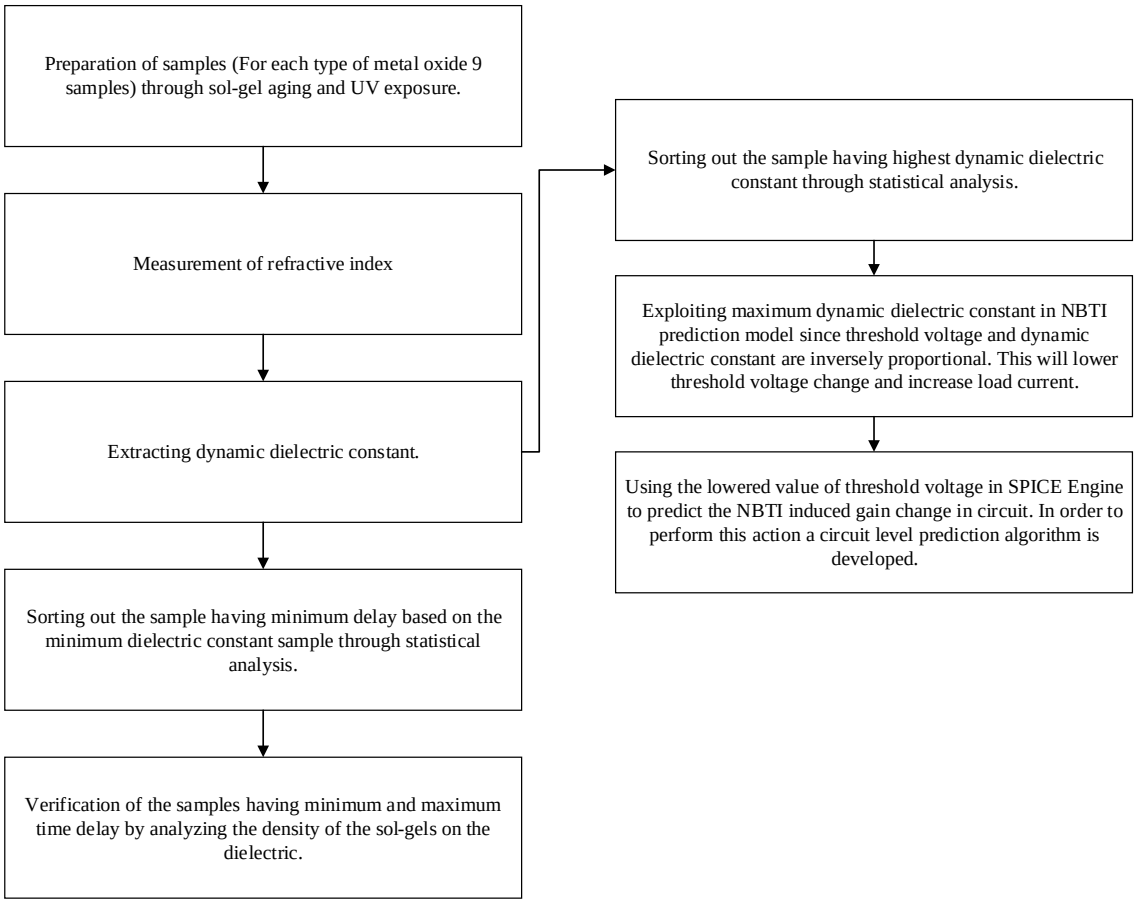


Fig. 3.1 Methodology of the project

Fig. 3.1 explains the methodology of the work. ZnO, TiO_2 and CuO incorporated SiO_2 dielectric samples are produced in such a way so that the refractive index changes from its normal value. This will help to sort out the sample with high refractive index and low refractive index. The lowest refractive index value will be exploited to mitigate delay. The highest valued sample will be employed to subside NBTI effect.

Fig. 3.2 shows the flowchart of the work in detail. This is a diagram for the better understanding of the proposed methodology above.

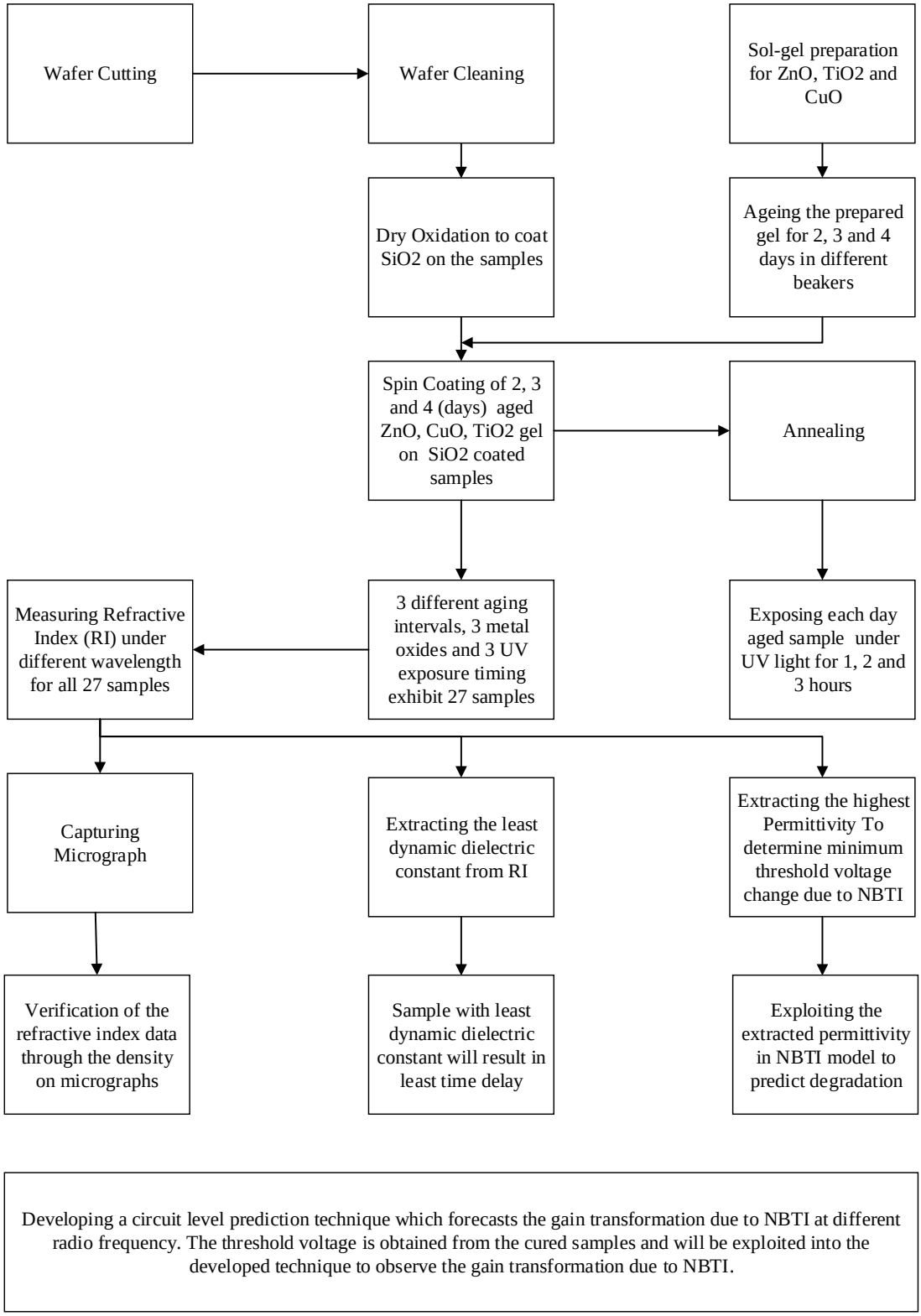


Fig. 3.2 Flowchart and the fabrication process

3.3 Wafer Cutting, Cleaning & Sample Preparation

It is important to mention that this research exploits 9 wafer samples for each type of metal oxide incorporation. Precursor ageing exhibits 3 types of wafer samples and under each type of aged samples there will be 3 different hours of UV exposure. The ageing is performed for 2, 3 and 4 days. This operation (ageing) is not exceeded for more than 4 days, the reason is elaborated here. As per (Shahini, Askari, & Sadrnezhaad, 2011)**,** ageing of sol-gel manifests larger size of crystal structures of nanopowders. (Shahini et al., 2011) also confirms that the crystal size increases along with ageing. (Shahini et al., 2011) finds that after 4 days of ageing the color of the sol-gel precursors get changed. Once, the size of the nanoparticles get bigger; the ions start forming molecules, get back to its basic color and hence, the sol-gel does not remain as a sol-gel as it starts showing undissolved particles. Due to the above mentioned reasons, ageing of the precursors are not done for more than 4 days. Adhesive UV exposure is done for 1,2 and 3 days since this operation is one of the key factors to change refractive index as mentioned by (Cheong & Jasni, 2007). On the dielectric there can be certain portions which are supposed to be thick and normal annealing process cannot cure these thick portions as per (Norland & Martin, 1993)**.** The process of adhesive UV exposure cures the thick portions with a minimum stress for 3 different hours. Though, It is mentioned by (Norland & Martin, 1993) despite of excessive UV exposure a certain amount of roughness remains on the surface. Hence, in this research UV exposure after the 3rd hour is not performed. As a whole, this research limits its boundary with 3 consecutive days of ageing and 3 consecutive hours of adhesive UV exposure. Therefore, at the end, this operation exhibits 9 samples for each type of metal oxide incorporation.

Si wafer is employed for the design of substrate. Normally, for substrate a thin slice of semiconductor material is used. Si wafer is grown from a crystal. These crystal structures have different types of orientations. Orientation is defined by Miller index like <100>, <111> and <110>. In this research, a 4 inch diameter <110> wafer is selected. <110> was employed because <110> shows larger transconductance degradation due to NBTI compared to <111> and <100> as per Fig. 3.3 by (Momose et al., 2003). Therefore, the degradation of other parameters due to NBTI is worst in <110> due to its poor interface quality. Considering the better interface quality of <111> and <100>, the worst type of case was selected for the betterment of NBTI degradation. If <110> shows a significant result, it is expected to get a better result from the other types (<111> and <100>).

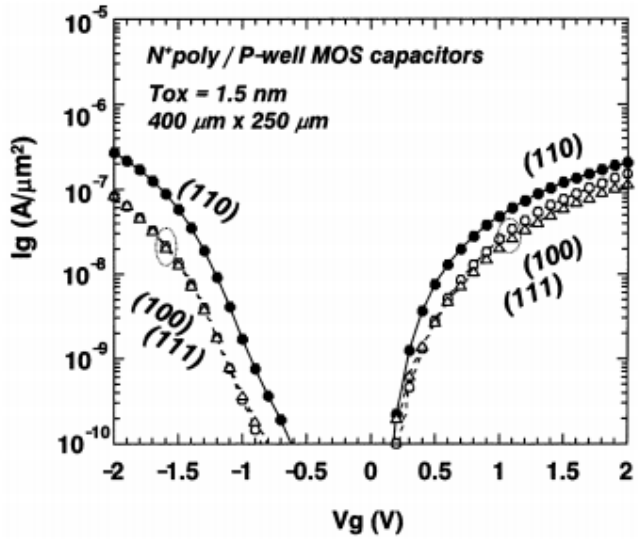


Fig. 3.3 Transconductance degradation due to NBTI in <110>, <100> and <111> Si wafer (Momose et al., 2003)

For cleaning and preparing sol-gel, different chemical compounds are used. Deionized (DI) water, Hydrogen per Oxide, Ammonium Hydroxide and Hydrochloric Acid were used for cleaning purpose. For preparing ZnO sol-gel; Zinc Acetate, Ethanol and Monoethanolamine are exploited. Titanium Butoxide, Ethanol and Acetic Acid is used to prepare TiO_2 gel. Copper Acetate Monohydrate, Methanol and Potassium Hydroxide are exploited to prepare CuO gel.

The four-inch diameter [Si (110)] wafer is cut into parts and a rectangle of 1.5 cm by 1 cm was taken. Having done this, the cut sample was cleaned to remove the native oxide. This cleaning process is often referred as Radio Corporation of America (RCA) standard cleaning process as per (Kern, 1990). The cleaning happens in two stages according to the standard. For the first stage, a mixture of DI-water, hydrogen per oxide and ammonium hydroxide was made at a ratio of 5:1:1 and the samples were cleaned. The second mixture was made using DI-water, hydrogen per oxide and hydrochloric acid in the 5:1:1 ratio.

3.4 Sol-gel Preparation

A sol-gel is an oxide based liquid environment formed through condensation reaction of a molecular precursor in a liquid. Sol-gel process can be divided into the following parts.

Hydrolysis: Hydrolysis is the process of mixing materials with water. Once the materials react with water, a polymer network is formed.

Condensation: Condensation results in the conversion of “hydrogen” type species into water.

Gelation: When the nanoparticles reach a critical size they stop growing and begin to agglomerate with other nanoparticles. These critical sized nanoparticles join together and forms gel.

Ageing: Ageing is performed to control structural, electrical and optical properties in sol-gel. As ageing increases the particles continue to grow.

The idea behind sol-gel synthesis is to "dissolve" the compound in a liquid in order to bring it back as a solid in a controlled manner. The sol-gel method is a physical chemistry based polymerization. It is a way for designing new materials for electrical characterization where attention is focused on the design of silica-based material along with transitional metal oxides. The major advantage of the method is that it offers the possibility to obtain materials with predetermined ageing, depending on experimental conditions. Predetermined ageing is not easy to achieve by conventional methods reported in (Liz-Marzán, 2006) and (Teixeira et al., 2001) because of burning at high temperature. As per (Vives & Meunier, 2008) and (Milea, Bogatu, & Duţă, 2011), the advantages of sol-gel method are stated below:

- It provides high purity homogeneous materials which need to be exploited in this work.
- It offers an easy way to trace elements.
- It allows the use of chemical techniques for the reaction control.
- It allows the formation of a "pre"-inorganic network in solution.
- It allows the densification to inorganic solids.

- It allows the introduction of permanent organic groups in solution (thus leading to inorganic-organic hybrid materials).
- It allows the synthesis of special materials such as films, reactive ceramic powders, fibres.
- It allows formation of new crystalline phases from the non-crystalline solids.
- It allows the preparation of new glass composition with superior properties determined by the specific properties of gel.
- Low processing temperatures allow energy saving, minimizes the evaporation losses, ensures purity by avoiding contamination with the containers during heat treatment, and avoids undesirable separation and crystallization of microphases.
- It allows the synthesis of special materials such as films, reactive ceramic powders, fibres.
- Multi component compounds may be prepared with a controlled stoichiometry by mixing sols of different compounds.
- The sol-gel method prevents the problems with co-precipitation, which may be inhomogeneous.
- Enables mixing at an atomic level.
- Results in small particles, which are easily sinterable.

Since, this research needs to control the ageing of the precursors; it is important to employ sol-gel ageing. The ageing carries a significance in this research because (Cheong & Jasni, 2007) showed, different precursor ageing changes refractive index in low-K dielectric. At the same time (Cheong & Jasni, 2007) showed that UV exposure

shifts the value of refractive index. These facts were exploited in this research by incorporating high-K dielectric.

In order to make sol-gel, magnetic stirrer [APPENDIX B] is used. It generates a rotating magnetic flux which yields the magnetic bar immersed inside a beaker full of liquid to spin**.** The spinning of the magnetic bar stirs the liquid inside the beaker. It has options to control the rotation per minute (RPM), temperature and time. In this work, stirrer is employed to stir the solution in order to make sol-gel.

According to (Shahini et al., 2011)**,** sol-gel ageing results in bigger dimension of crystal structures of nanopowders. The same reference (Shahini et al., 2011) confirms when the ageing increases, the crystal size increases. And from this research (Shahini et al., 2011), it has been found that after 4 days of ageing, the color of the sol-gel precursors get changed. Once, the size of the nanoparticles get bigger; the ions start forming molecules, get back to its basic color and hence, the sol-gel does not remain as a sol-gel as it starts showing undissolved particles. Due to these phenomena, in this research ageing the precursors is not done for more than 4 days.

3.4.1 Preparation of ZnO Gel

Once the cleaning is done the ZnO gel is prepared as per (Muhammad & Willander, 2012) and (Foo, Kashif, Hashim, & Ali, 2013). In order to make a gel of ZnO, a solution of Zinc Acetate powder in Ethanol is mixed first at a temperature of 60°C. The solution is stirred at 1000 rpm for 2 hours. While the stirring operation is taking place, Monoethanolamine is added to stabilize the solution. And once the solution appears as

transparent, the gel is prepared. While preparation of sol-gel was performed and optimized by (Foo et al., 2013). In this research the exact same method was employed. In order to get a crystal clear gel, the molarity of Zinc Acetate was increased to 0.3 mol and decreased to 0.1 mol. Using 0.1 mol resulted in undissolved particles inside the gel. On the other hand, 0.3 mol started showing brown color in the sol-gel due to excessive density of Zinc based compound. Hence, 0.2 mol was chosen as the optimum level of molarity which showed clearer gel.

3.4.2 Preparation of TiO_2 Gel

In order to prepare a gel of TiO_2, a solution of Titanium Butooxide, Ethanol and acetic acid by a ratio of 1:9:0.1 is prepared. The solution is stirred at 1000 rpm for 5 hours and the gel is prepared as per (Nadzirah & Hashim, 2013). The optimization and the procedure for this sol-gel process was previously performed by (Nadzirah & Hashim, 2013). In this research, in order to optimise further the Titanium Butooxide ratio was increased which gave a reddish colored sol-gel due to excessive amount of Titanium derivatives. Therefore, at the end 1:9:0.1 ratio was kept.

3.4.3 Preparation of CuO Gel

In order to make a sol-gel of CuO (Ibupoto, Khun, Liu, & Willander, 2013), 0.249 gm of Copper Acetate Monohydrate is dissolved in 0.125 l of Methyl Alcohol. Potassium Hydroxide is made by dissolving 0.109 g of Potassium Hydroxide with 0.065 l of Methyl Alcohol. The second solution was added drop wise in the first solution (stirred) at a temperature of 60°C till the first solution turns into milky blue. The procedure of this sol-gel was taken from (Ibupoto et al., 2013). The amount of Copper

Acetate Monohydrate was reduced t0 0,1 gm and was increased to 0.3 gm in two different precursors. But, in both cases undissolved green particles were seen since Copper derivatives could not react with Methyl Alcohol and Potassium Hydroxide properly. Hence, the amount used in (Ibupoto et al., 2013) was not changed.

3.4.4 Ageing of Gel

Gel of three different metal oxides (ZnO, TiO_2 and CuO) is kept inside 9 different beakers where each metal oxide was for three beakers. Once the gel is prepared using sol-gel method, these gels are aged for 2,3 and 4 days and are labelled accordingly.

3.5 Dry Oxidation Process

In dry oxidation process dry oxide is flown on the samples at an elevated temperature of 700-1200°C and at 0.1 ~ 25 atmospheric pressure.

$$Si + O_2 \rightarrow SiO_2$$

The main advantage is-this process does not involve water while coating SiO_2 on Si substrate. Growth rate of oxide in this process is slower than that of wet oxidation process. A waterless environment and slow oxide growth rate results in thin oxide. The oxide layer formed in this process is denser and have better electrical breakdown than that of wet-oxidation process.

The formation of SiO_2 on Si wafer is performed inside oxidation furnace [APPENDIX C] through a process called thermal oxidation. As the name implies, the process uses a very high temperature to grow SiO_2 crystal. Before proceeding further, it is imperative to mention that Si has a property of oxidizing itself even at normal environment. The high temperature accelerates this oxidizing process. The oxidation furnace consists of:

1. Chamber
2. Heater
3. Temperature measurement unit
4. Control unit
5. Process tubes where the wafers are kept for oxidation purpose
6. A system to control the flow of gases inside and outside of the process tube

While preparing the gels, Si wafers are processed inside the oxidation furnace in order to coat the wafers with SiO_2. Before proceeding with the dry oxidation process, it is made sure that the heat exhaust lines are turned on. The furnace is turned on and the main control temperature is set to 600°C initially. Having set the initial temperature, the N_2 chamber is turned on. The wafers are placed perpendicular to the ground and kept on the boat. When the furnace temperature reaches at 600°C, the wafers are loaded inside the furnace. Having loaded the wafers, the temperature inside the furnace is ramped up to 1000°C. Once the temperature reaches at 1000°C, N_2 pressure is turned off and O_2 chamber is turned on for oxidation purpose. After two hours, O_2 chamber is turned off and N_2 chamber is again turned on. At this time the temperature of the

furnace is set to 300°C to ramp down. Once the furnace reaches 300°C, the wafers are taken out. The oxidation process is conducted for 27 pieces of Si wafer. It is made sure that the wafer height, wafer width and the thickness of SiO2 layer remains uniform in all samples. For this F-20 thickness measurement device is used.

3.6 Spin Coating Process

A spin coater or a spin processor [APPENDIX D] is a machine used to deposit uniform thin films on flat substrate. In this research spin processor is used to deposit sol-gel on SiO_2 coated Si substrate. The spin processor has a speed control unit to control the rotation of the processor. Rotation is controlled to maintain thickness uniformity on the film. It has been mentioned earlier, spin coating is an integral process of this work which is used to coat the gels on SiO_2 coated Si wafers. This process involves depositing a small puddle of gel onto the SiO_2 coated Si wafers and spinning the process at a high speed. Centrifugal acceleration causes the puddle of gel to spread to and off the edge of the wafer. The spin coating process used in this work is described using Fig. 3.4. An excess amount ($1cm^3$) of gel solution is dropped on top of each wafer. The substrate is then rotated at high speed at an angular velocity defined by rotation per minute (rpm), in order to spread the fluid by centrifugal force and reducing fluid thickness. A common method is applied for all samples to maintain uniformity.

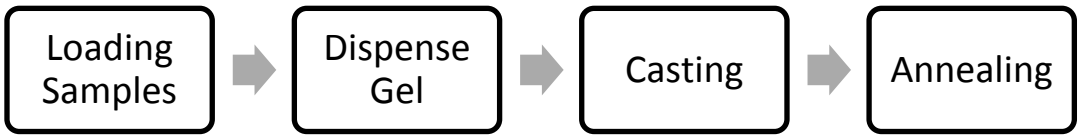


Fig. 3.4 Flowchart of the spin coating process

Once loading and dispensing is done, casting or speeding was performed. The rotation per minute of the wafer affects the centrifugal force applied to the gels as well as the angular velocity. In particular, the high speed generally defines the final film thickness. Speeding is an important factor to keep the thickness optimum and the process of speeding was kept same for all cases. In order to do spin coating, three successive steps were followed with three different levels of speed. For the first step, the spin coater was accelerated up to a speed of 2000 rpm over 20 seconds. The second step is the processing step where the spinner was rotated for 20 seconds at a speed of 2000 rpm. The last step is to slow down and stop the spinner, which was done for over a twenty-second time period. The speed was increased to 2500 rpm and 3000 rpm. But in both cases gels were wiped away from the surface. Hence, 2000 rpm was chosen for the first two steps. At the third step, a sudden stop in speed was generated by reducing the speed to zero so that a uniform ridge can be obtained at the edge. This helps to maintain uniformity all over the surface.

3.7 Annealing

Here, the annealing process for this research will be discussed. In this work, oven is used to anneal the samples by inducing ductility, relieving internal stress, softening material and improving structures as per (Alonzo-Medina, González-González, Sacedón, & Oliva, 2013)**.** Inside the oven annealing was performed in two stages; namely-heating stage and cooling stage. Once the spin coating is done, all the samples are inserted inside an oven at a temperature of 60°C to bake or anneal. This process continues for an hour. Having performed the spin coating and annealing, it was made sure that there is uniformity in the oxide thickness for all samples by using F-20 thickness measurement device. In this research the target of the annealing was to harden

the gel on the Si-SiO_2 substrate. But at the same time it was imperative to make sure that thin and hardened gel do not get cracked. At a temperature more than 60°C small the gel layer started to show up small amount of cracks. Therefore, the annealing temperature was kept up to 60°C.

3.8 Adhesive UV Exposure

The samples are cured with adhesive UV light to change the value of refractive index. The adhesive UV exposure has a significance because (Cheong & Jasni, 2007) showed, UV exposure changes refractive index in low-K dielectric to cure the samples for different time spans for better crystallization. And hence, this research method applies suitable for high-K metal oxide. The purpose of adhesive UV exposure is to cure the samples. In a thin film, there can be certain portions which are supposed to be thick. Normal annealing process cannot cure these thick portions as per (Norland & Martin, 1993)**.** Adhesive UV exposure cabinets [APPENDIX E] cure the thick portions with a minimum stress. While curing the thick sections with normal annealing, the stress due to the shrinkage of the film becomes an issue. Adhesive UV exposure cabinet solves this issue by making the surface thickness as uniform as possible.

After annealing, the aged samples are exposed under UV light for 1, 2 and 3 hours adhesively. Hence, 9 different samples of CuO incorporated dielectric by combining 3 different days of ageing and 3 different exposure times are prepared. Similarly, 9 samples of ZnO incorporated dielectric and 9 samples of TiO_2 incorporated dielectric are prepared.

3.9 Measurement of Refractive Index

Having fabricated the dielectric samples, refractive index is measured using PerkinElmer Lambda 35 UV-vis refractometer [APPENDIX F]. Each sample was aligned vertical to the ground level by keeping a dark environment inside the chamber. This helps to get rid of external optical interference. The refractometer is connected to Winlab software which shows the optical graph by collecting data from the refractometer. A detailed analysis on refractive index, extraction of dielectric constant, derivation on the relationship between refractive index and dielectric constant considering the effect of impedance spectroscopy has been described in Section 4.7 by combining the analysis with experimentally obtained results.

3.10 Statistical Analysis

Statistical analysis is a key part of testing the hypothesis of this research, since it sorts out the highest and lowest refractive indexed samples. A major portion of the hypothesis of this work is based on the work of (Cheong & Jasni, 2007) . (Cheong & Jasni, 2007) experimented on low-K dielectric and hypothetically this thesis considers that the same technique can help to reduce dielectric constant in high-K incorporated dielectric. In order to test this hypothesis it is imperative to consider different samples of dielectric prepared and cured under different conditions. Statistical analysis helps to determine the least and highest value of the refractive index and dynamic dielectric constant from these samples. In this work both of these values have significance. The lowest value will be exploited to obtain the least time delay. The highest value will be used for NBTI induced threshold voltage minimization, since as per (Kumar et al., 2009a) high dynamic dielectric constant results in low threshold voltage.

3.11 Result Verification

In order to verify the results, the density of the metal oxide will be taken into consideration through analysing surface morphology using Scanning Electron Microscopy (SEM) and Energy Dispersive X-ray Micro-Analysis (EDXMA). Report by (Kucharczyk & Shigorin, 1989) shows density and refractive index are directly proportional to each other. Hence, the sample having least refractive index will exhibit less density on its surface and the sample having highest refractive index will yield more density of the incorporated metal oxides on its surface. This yields this research to capture surface morphological information. From the density of the metal oxides on the surface, the validity of the obtained results is verified in this research.

3.12 Exploiting the Extracted Dielectric Constant into NBTI Model

Based on the results obtained from the samples, a statistical analysis is performed (**Chapter 4**) to find out the highest refractive index and hence dynamic dielectric constant is extracted according to the formula given by (Cheong & Jasni, 2007). Once the highest dielectric constant is extracted, it is used in NBTI predictive model [APPENDIX G]. One of the updated form of classical Reaction-Diffusion model (Jeppson & Svensson, 1977) by (Kumar et al., 2009a) is exploited in this method. The R-D framework provides with an opportunity to explore both the short-term NBTI degradation and fast transient relaxation as per (Islam, Kufluoglu, Varghese, Mahapatra, & Alam, 2007). In this case, the R-D framework by (Kumar et al., 2009a) can be exploited because it allows us to use the dielectric constant since dielectric constant is one of the key functions in R-D equations. Though, the classical R-D model by (Jeppson & Svensson, 1977) is criticized for its inability to predict the change in

threshold voltage recovery, particularly at shorter time scale as mentioned by (Reisinger et al., 2006) and (Tibor Grasser, Kaczer, & Goes, 2008). As a result, in order to ensure accuracy a repuzzled version of RD framework is exploited which is employed by (Kumar et al., 2009a). Since the model of (Kumar et al., 2009a) successfully complies with experimental data on both stress and recovery phase according to (Krishnan et al., 2005) and (M. F. Li et al., 2004), the drawback of the classical RD framework can be solved by exploiting the model given by (Kumar et al., 2009a). While considering the predictive model to mitigate NBTI degradation, 16nm technology node is considered. Both constant and dynamic bias stresses were taken into account.

3.12.1 DC Mode Simulation Algorithm for Device

It has been clarified in **Chapter 2**, the reason behind choosing the model by (Kumar et al., 2009a). **Chapter 2** also describes the details of the model of (Kumar et al., 2009a). In order to predict the change in threshold voltage, the change in interface trap is simulated in MATLAB considering 10 years of ageing [APPENDIX G]. This model considers the hydrogen diffusion in poly interface and time required for this action is considered as one of the simulation variables. This required time of hydrogen diffusion in poly is lower than that of in oxide according to (Krishnan et al., 2005). The expression for the change in threshold voltage as per this model is shown in Equation 3.1.

$$v_{th} = q * N_{IT}/c_{ox} \tag{3.1}$$

The expression for the change in interface trap inside the oxide is simulated as per Equation 3.2,

$$N_{IT} = k_{IT}(2D_{ox}t)^{1/6} \quad (3.2)$$

Considering the diffusion coefficient in poly interface, the equation (Equation 3.3) of N_{IT} change is simulated here. This considers a slow stress phase compared to the diffusion in oxide, since the required time to diffuse in poly is less than the total ageing time of 10 years,

$$N_{IT} = k_{IT}(D_{ox}(1+f)) + \sqrt[1/3]{2 * D_p(t-t_1) * f} \quad (3.3)$$

Here, D_{ox}= Diffusion coefficient in the oxide; D_p=Diffusion coefficient in the poly; k_{it}=Reaction Rate; e_0=vacuum dielectric constant; c_{ox}= dynamic dielectric constant*e0/oxide thickness. The simulation algorithm has been set in Fig. 3.5

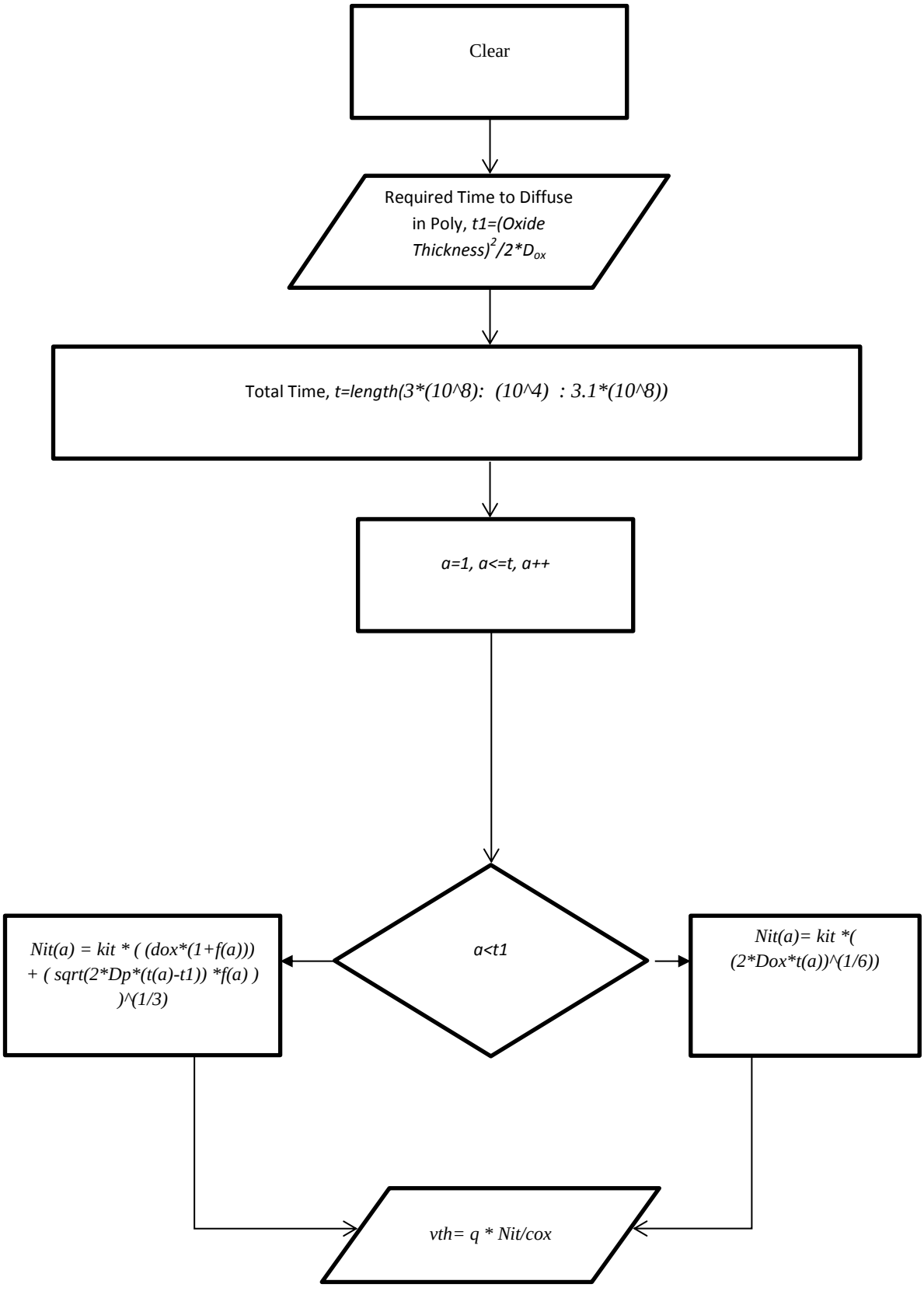


Fig. 3.5 Flowchart of the algorithm for DC stress

3.12.2 AC Mode Simulation Algorithm for Device

For a dynamic mode operation, where an ac stress is applied on the device, with an equal stress time with the relaxation time T, for (n+1)th cycle the expression for interface trap is given by two different equations for each phase (stress & recovery). The first equation represents the stress time from 2nT to (2n+1)T. The second equation represents relaxation mode which starts from (2n+1)T to 2(n+1)T.

For stress phase, if it is considered that each stress phase(t) is 1000s long and if t is less than or equal to the time (t1) for hydrogen species to migrate to poly then the interface change equation is shown in Equation 3.4,

$$N_{it} = k_{it}(\frac{N_{it}T}{k_{it}})^6 + (2D_{ox}t(a)))^{1/6} \quad (3.4)$$

Any other case apart from that in stress phase will follow the Equation 3.5,

$$N_{it} = k_{it}\sqrt{(\frac{N_{it}T}{k_{it}})^6 + (2D_{ox}t)^2} + \sqrt{(2D_p(t - t1)))^{1/3}} \quad (3.5)$$

For recovery phase, if it is also considered that each relaxation phase (t) is 1000s long and if t is less than or equal to the time (t2) for hydrogen species to migrate to poly then the interface change simulation is based on the Equation 3.6,

$$N_{it}(b) = N_{it}((2n + 1)T/(1 + h1(b)) \quad (3.6)$$

Any other case apart from that in stress phase will be simulated by the Equation 3.7,

$$N_{it}(b) = N_{it}((2n + 1)T + t2)(1 - h2(b)) \quad (3.7)$$

Here, h1 and h2 are constant which depend on oxide thickness and diffusion coefficient in poly. The flowchart of the algorithm is as depicted in Fig. 3.6 & Fig. 3.7,

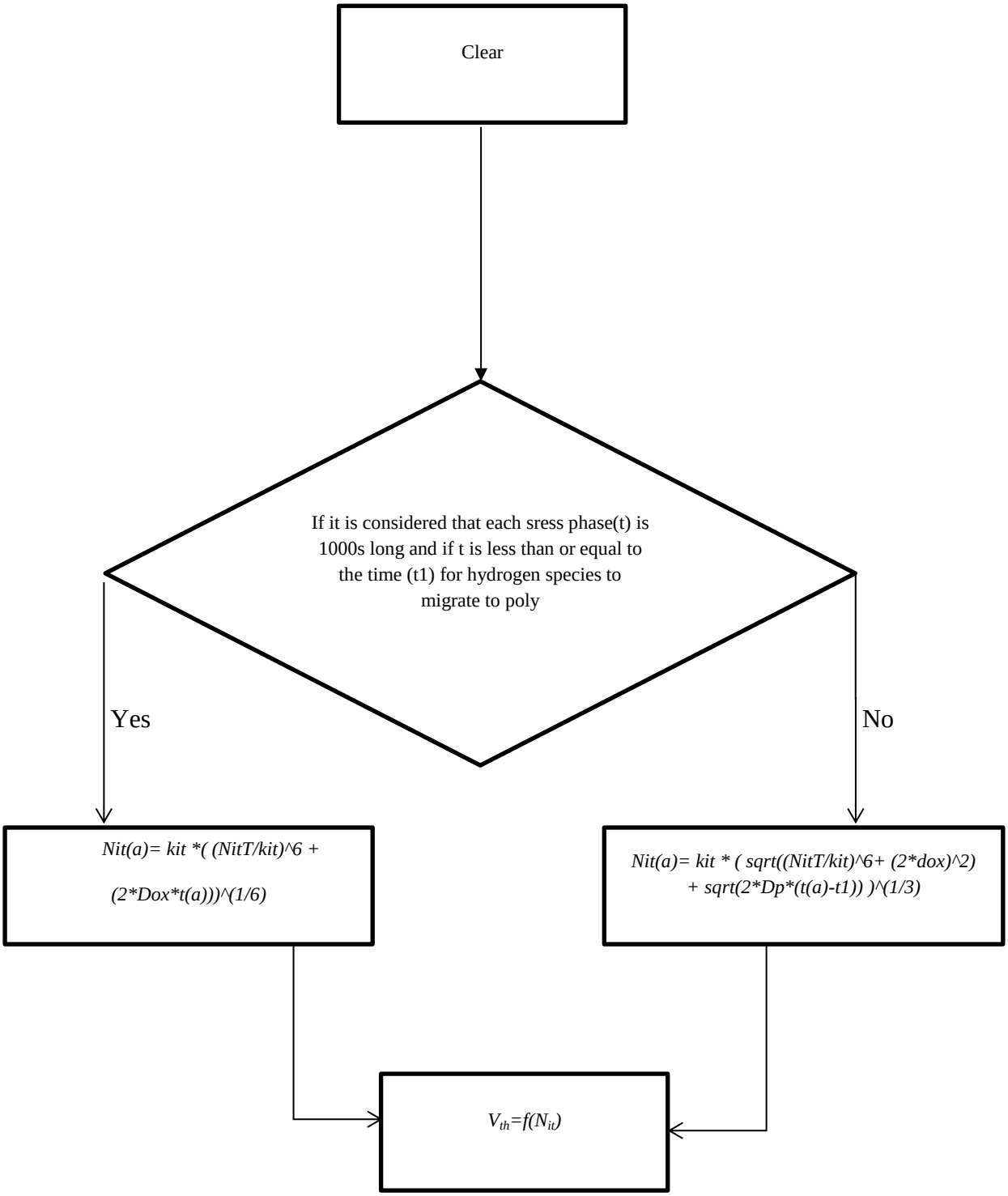


Fig. 3.6 Flowchart of the algorithm for AC under stress phase

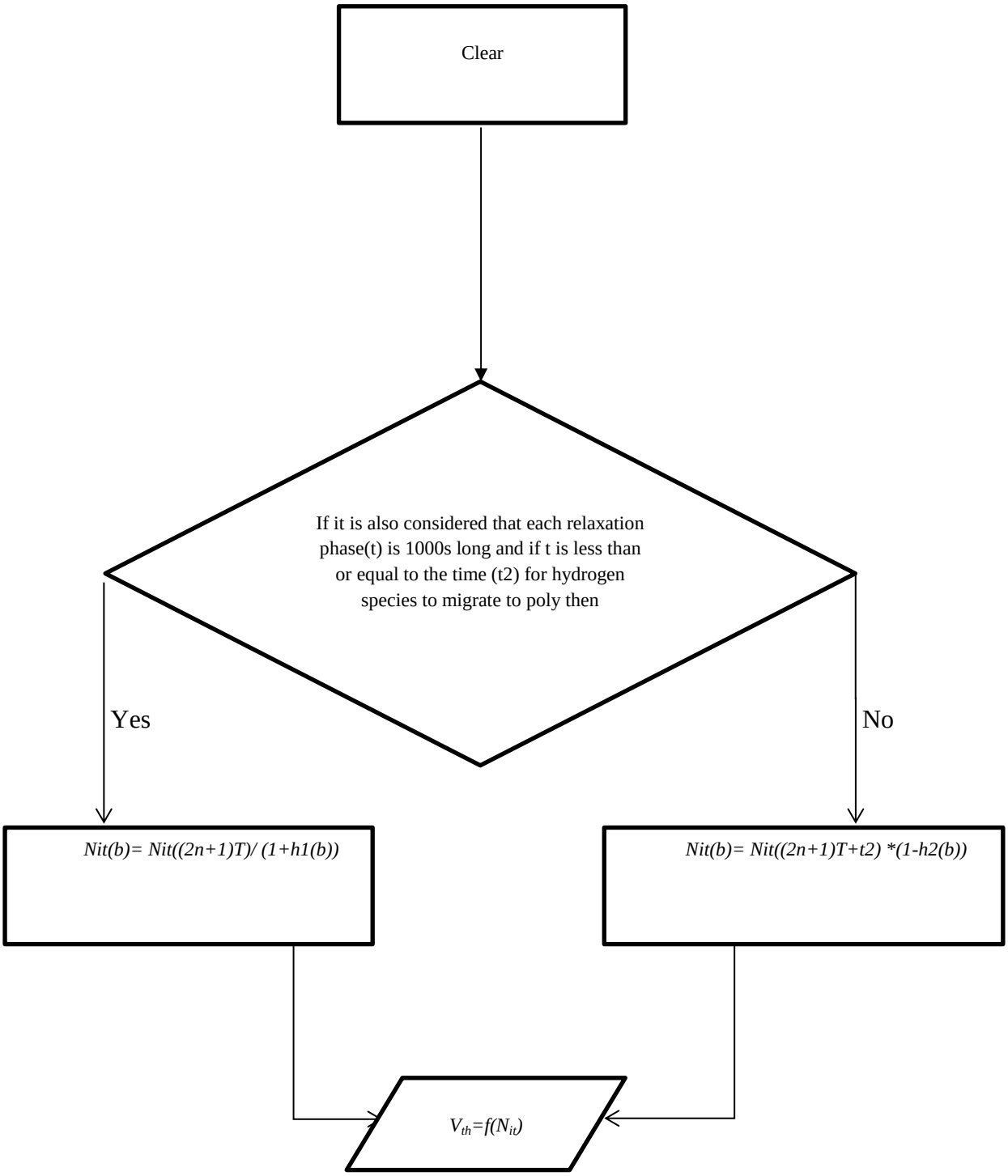


Fig. 3.7 Flowchart of the algorithm for AC under recovery phase

3.13 NBTI Forecasting Algorithm for Circuit

After doing the device level mitigation, it is important to analyse the circuit level performance by employing the obtained device level parameters. Here, circuit level analysis is imperative, since it helps to predict the behaviour of any circuit's radio frequency compatibility under NBTI. Therefore, a circuit level algorithm is implemented to observe the gain transformation due to NBTI over different range of radio frequency. In order to simulate CMOS circuit, 16nm Predictive Technology Model (PTM) is used inside the Cadence HSPICE engine [APPENDIX H] (Chao, 2008). The obtained parameters from device level analysis are employed inside the PTM model. Hence, ageing analysis is performed using Cadence Rel Xpert software.

To implement the algorithm, a conventional RF oscillator (Razavi, 2011) and [APPENDIX K] is selected on which ageing simulations for 10, 15 and 20 years were performed. Ageing simulation is performed by employing the upgraded version of R-D model(Kumar et al., 2009a) inside Virtuoso Rel Xpert simulator, a shift in circuit gain is observed.

NBTI induced ageing analysis is performed on a variety of radio frequency spectrum segments. 1 to 10 GHz frequency is divided in 5 equal segments and hence, the gain shift for each segment is observed (Shown in the result section in **Chapter 4**). The transformation in gain vs. frequency graph is plotted (Shown in the result section in **Chapter 4**). The algorithm is depicted in Fig. 3.8.

The threshold voltage shift obtained from device level AC simulation is used in the algorithm of Fig. 3.8. In this case, the materials with better drain current performance are considered since high drain current refers to high gain. This algorithm helps one to know the NBTI induced gain changing behavior of a circuit. Basically, here the results obtained from the device level data to be used in circuit level algorithm to observe NBTI driven gain changing behavior in circuit.

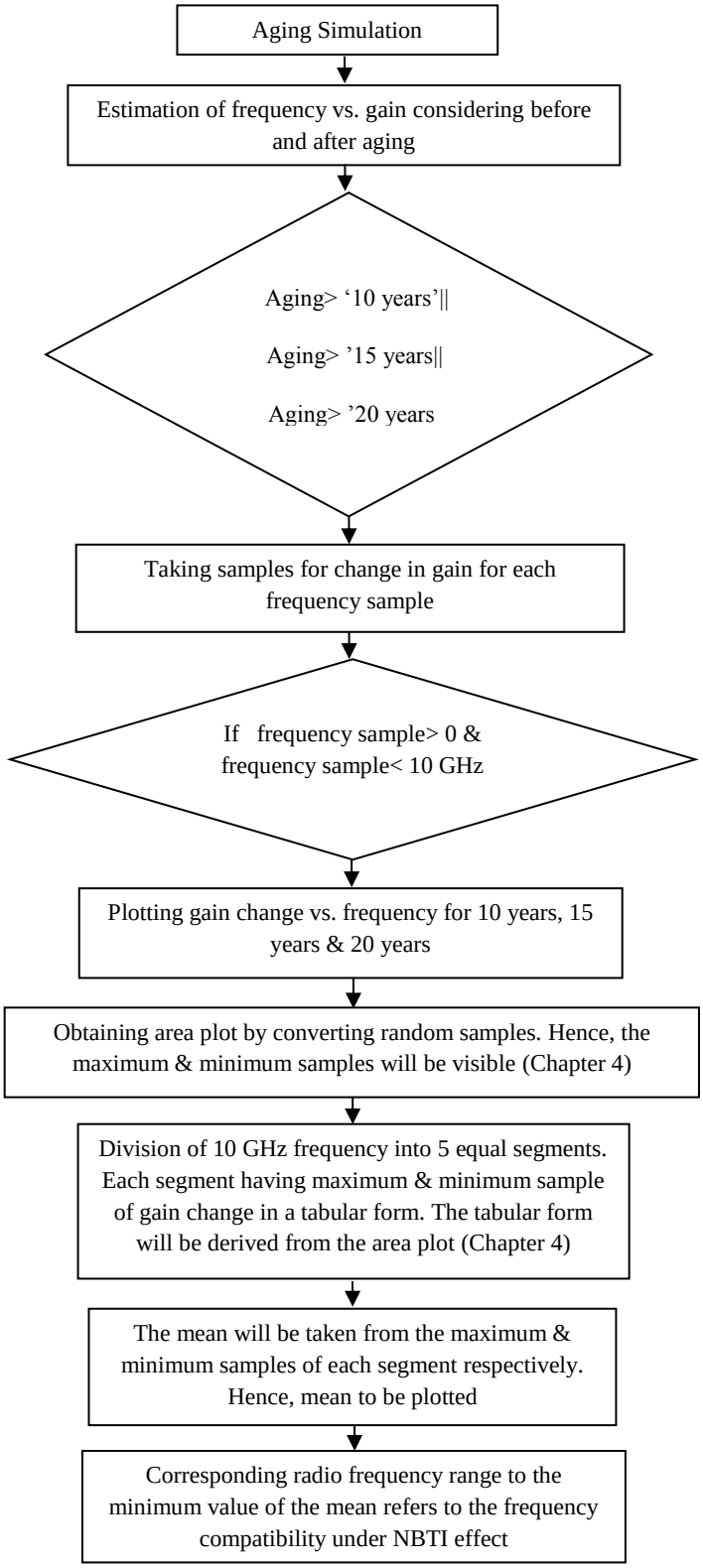


Fig. 3.8 Block diagram for the forecasting algorithm

3.14 Summary

The issue of delay and NBTI has been a matter of concern over decades and different methods have been applied by different researchers to get rid of these problems. Though, by considering these two issues, a unidirectional method is proposed in this research for the first time. It is important to mention that for oxide delay mitigation this research investigates high-K dielectric material for the first time as well. The methodology proposed to mitigate the delay factor focuses more on changing the process of fabrication rather than depositing different organic/inorganic materials. Similarly, to mitigate NBTI, researchers employed different circuit level and device level techniques. But, the method proposed by this work focuses on modifying the fabrication steps. The modification took place to change the refractive index of the dielectric. By incorporating the modified precursors of different high-K metal oxides, refractive index is changed from its actual value. From this change, the samples with highest and lowest refractive index are to be sorted out. Considering the results from AC simulation, a circuit algorithm is developed which follows a statistical method to analyse the radio frequency compatibility under NBTI.

CHAPTER 4 RESULTS & ANALYSIS

4.1 Introduction

This chapter reports the results of ZnO, TiO_2 and CuO incorporations. By incorporating these materials onto Si-SiO_2 surface, refractive index data is obtained which will be projected in this chapter. The results will be analysed into two phases. At first phase, a statistical analysis will be performed to sort out the highest and lowest refractive index from the samples. The second analysis is done to validate the results with the help of morphological density of the sample surface. While showing results, the normal case (no material incorporation) will also be considered. Having done the analysis on the samples, the analysis on the evaluation of NBTI will be carried out based on the obtained results. For different types of material incorporation, NBTI will be analysed under DC stress and dynamic stress. The algorithms (APPENDIX G) based on the models were employed to study NBTI and significant results are found with high-K materials incorporation. And in each case, the shift in threshold voltage is compared with the normal case of Si-SiO_2 interface. Since, the change in threshold voltage is inversely proportional to the change in drain current according to (Weste & Eshraghian, 1985), the materials generating high drain current is determined and is used to analyse circuit level NBTI driven gain transformation.

4.2 Results for Refractive Index

4.2.1 Normal Case

Before proceeding to the experimental results in the next sections, it is imperative to recall the nature of refractive index for ZnO (**Chapter 2**), CuO (**Chapter 2**) and TiO_2 (**Chapter 2**) in normal case. When the gel is aged; the refractive index of the materials starts changing. It happens due to the density of the gel materials (Kucharczyk &

Shigorin, 1989). So, theoretically obtained refractive index remains impossible to use in the practically implemented transistors.

4.2.2 Case of ZnO Incorporation

Extraction of the refractive index is performed for ZnO coated SiO_2 using the PerkinElmer Lambda 35 Filmetric System as per Fig. 4.1-4.3. In Fig. 4.1 the refractive index for 2 days old samples are shown where the samples are exposed under UV for 1, 2 and 3 hours. Among the 2 days old samples, the 1-hour UV exposed sample shows the lowest refractive index. Similarly, among the 3 days aged precursors, the sample with 2 hours of UV exposure shown in Fig. 4.2 shows the lowest result. For 4 days ageing, the 1-hour UV exposed sample shows the minimum refractive index in (Fig. 4.3).

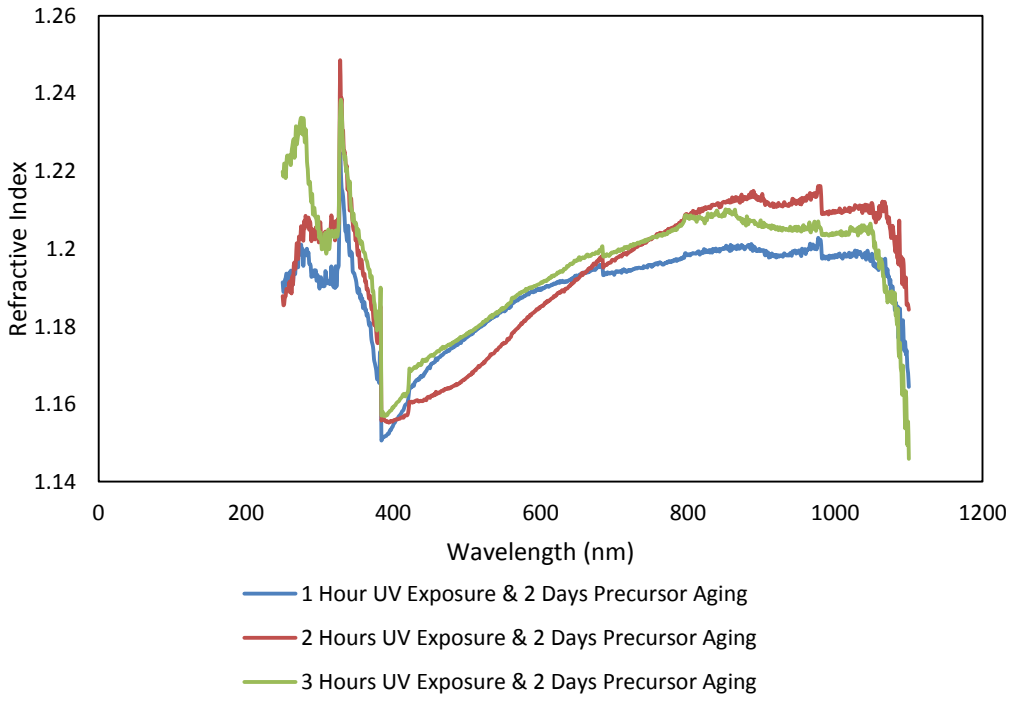


Fig. 4.1 Experimentally obtained refractive index data for ZnO after 2 days precursor ageing

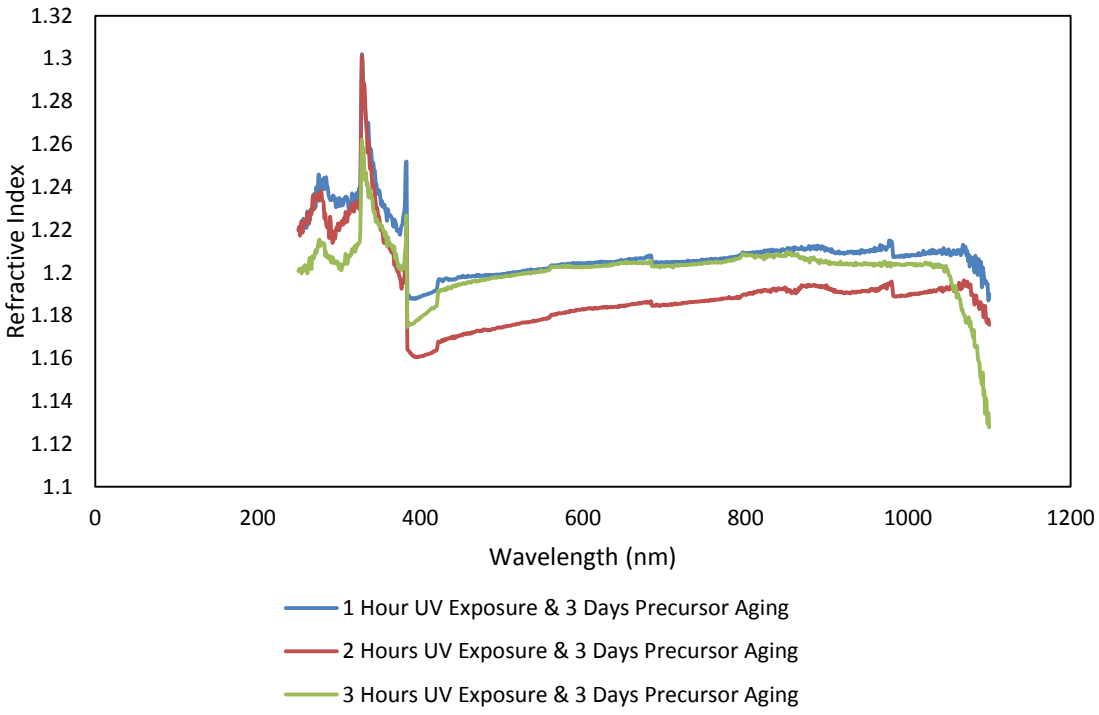


Fig. 4.2 Experimentally obtained refractive index data for ZnO after 3 days precursor ageing

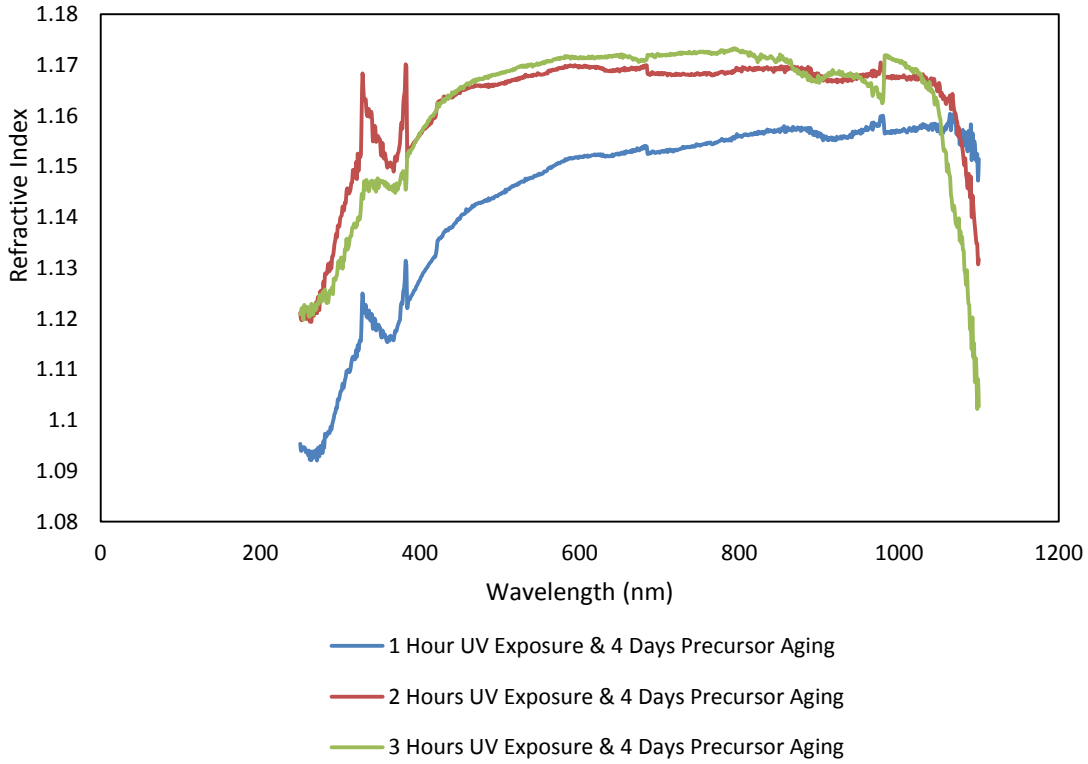


Fig. 4.3 Experimentally obtained refractive index data for ZnO after 4 days precursor ageing

4.2.3 Case of TiO_2 Incorporation

Refractive index extraction is done for TiO_2 coated SiO_2 using the PerkinElmer Lambda 35 Filmetric System as per Fig 4.4-4.6. In Fig 4.4 the refractive index for 2 days aged samples are shown where the samples are exposed under UV for 1, 2 and 3 hours. Among the 2 days old samples, the 1-hour UV exposed sample shows the lowest refractive index. Similarly, among the 3 days aged precursors, the sample with 1 hour of UV exposure shown in Fig 4.5 shows as the lowest result. For 4 days ageing, the 2-hour UV exposed sample shows the minimum refractive index in (Fig 4.6).

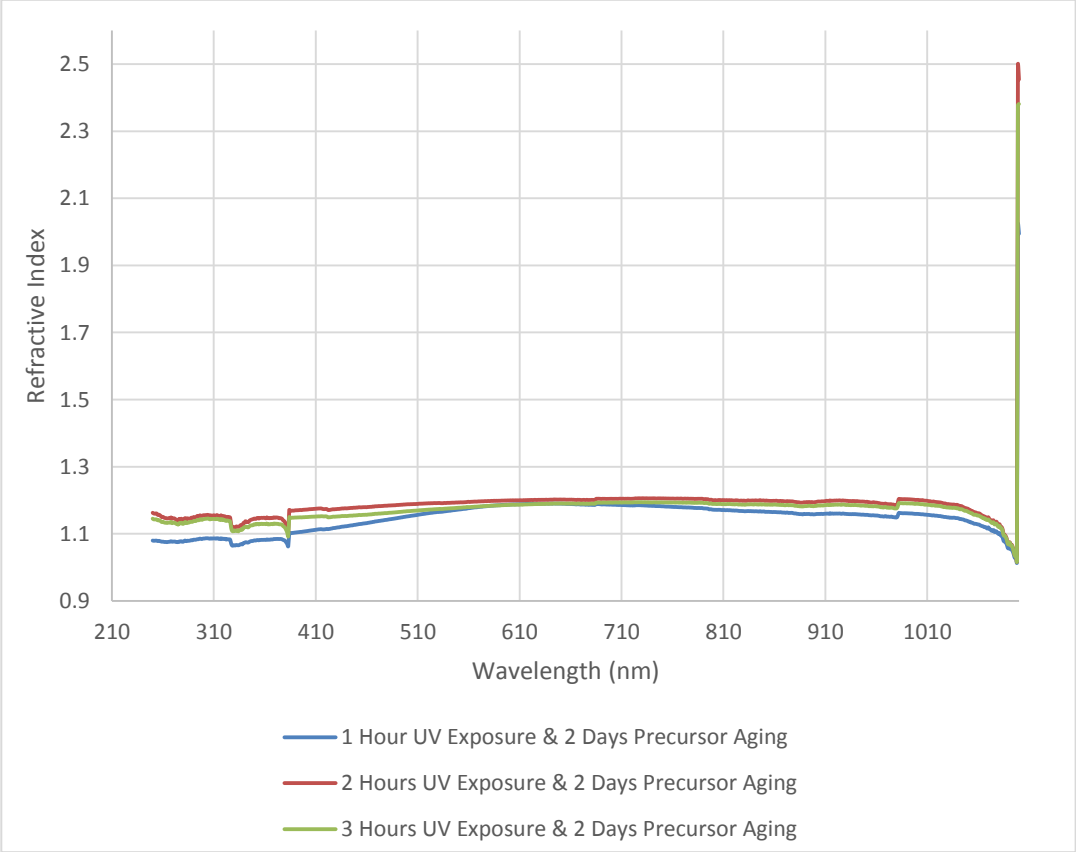


Fig. 4.4 Experimentally obtained refractive index data for TiO_2 after 2 days precursor ageing

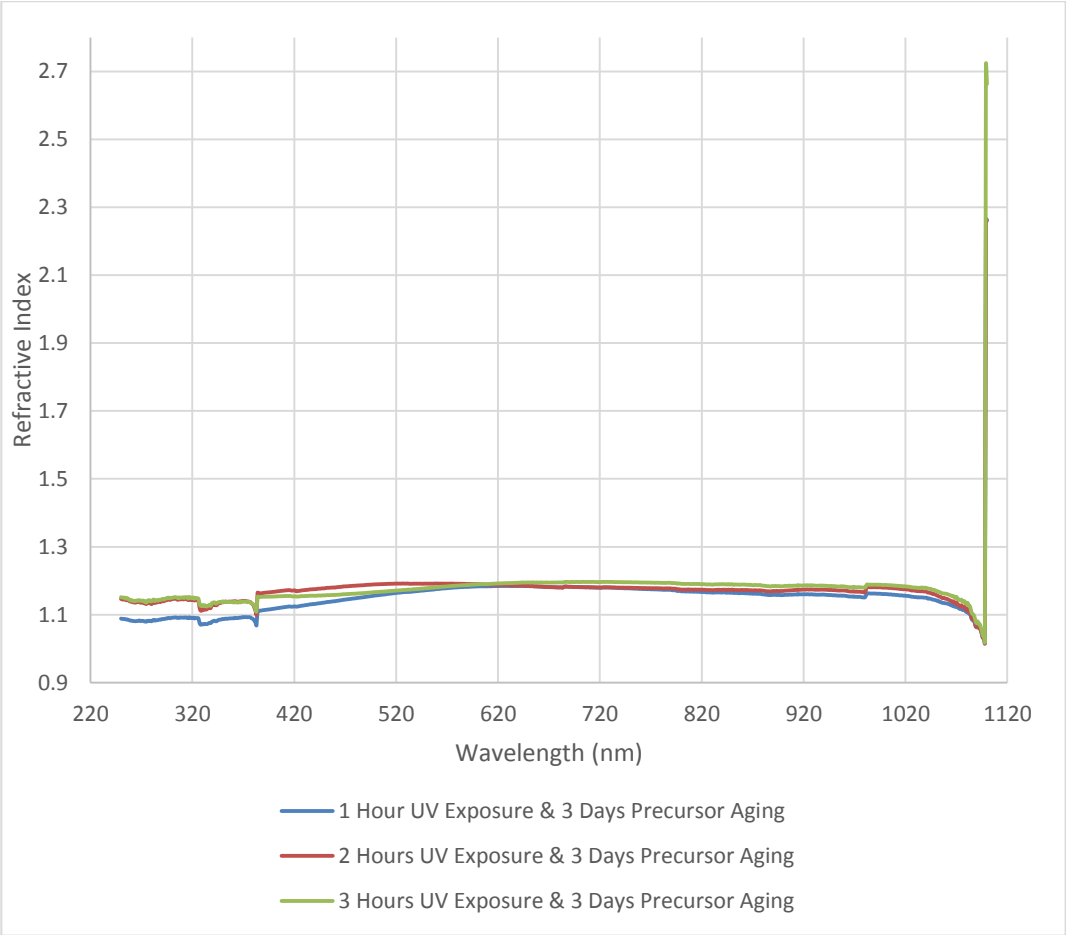


Fig. 4.5 Experimentally obtained refractive index data for TiO_2 after 3 days precursor ageing

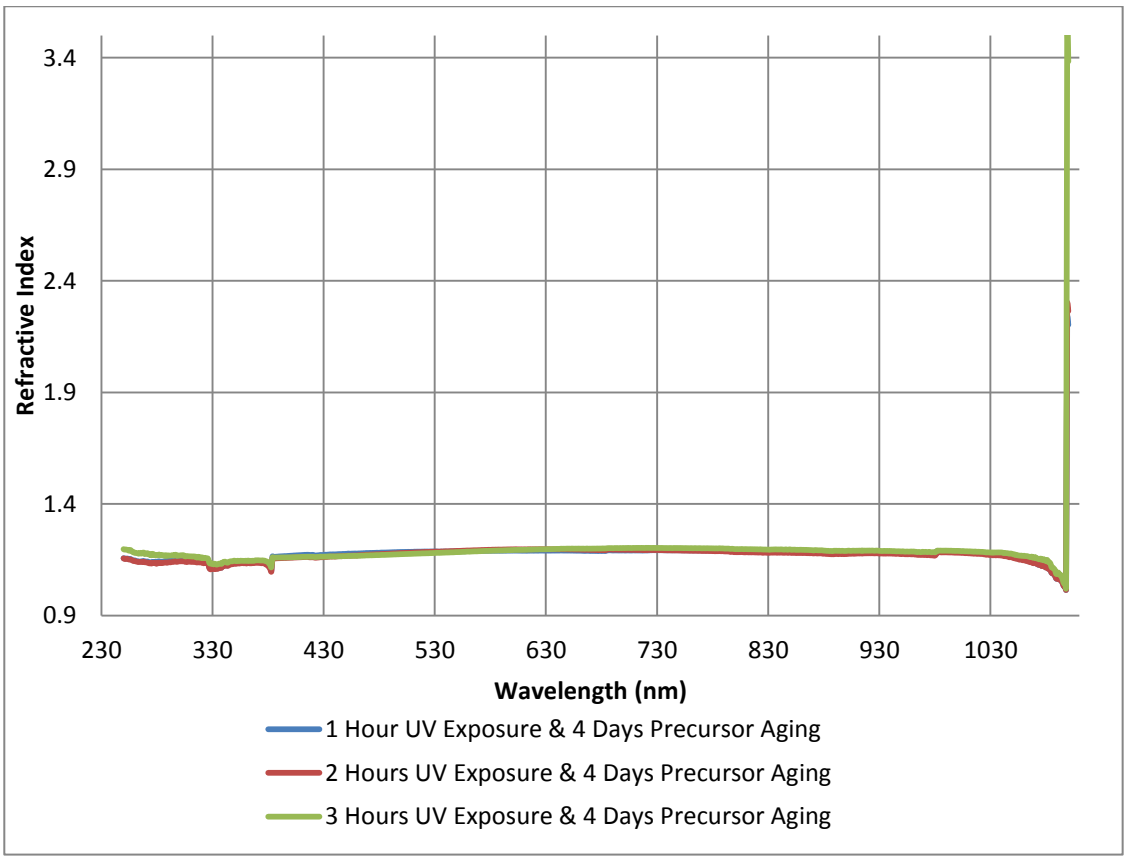


Fig. 4.6 Experimentally obtained refractive index data for TiO_2 after 4 days precursor ageing

4.2.3 Case of CuO Incorporation

Extraction of the refractive index is carried out for CuO coated SiO_2 using the PerkinElmer Lambda 35 Filmetric System as per Fig. 4.7-4.9. In Fig 4.7 the refractive index for 2 day aged samples are shown where the samples were exposed under UV for 1, 2 and 3 hours. Among the 2 days old samples, the 3-hour UV exposed sample shows the lowest refractive index. Similarly, among the 3 days aged precursors, the sample with 1 hour of UV exposure shown in Fig 4.8 shows as the least value. For 4 days ageing, the 3-hour UV exposed sample shows the minimum refractive index in (Fig 4.9). The difference in refractive index values have been explained in Section 4.3.

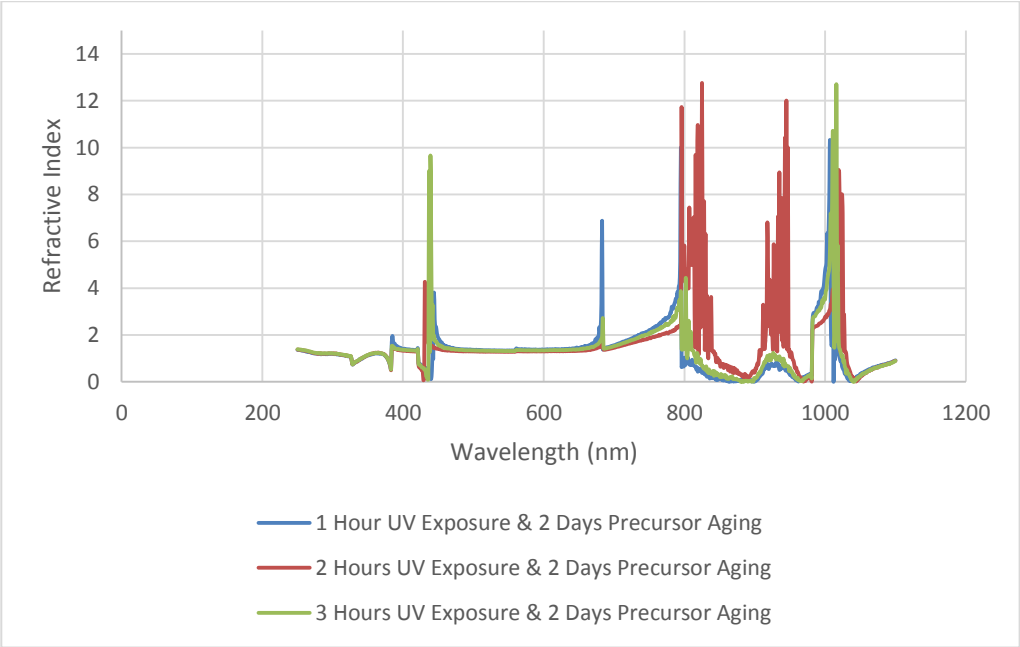


Fig. 4.7 Experimentally obtained refractive index data for CuO after 2 days precursor ageing

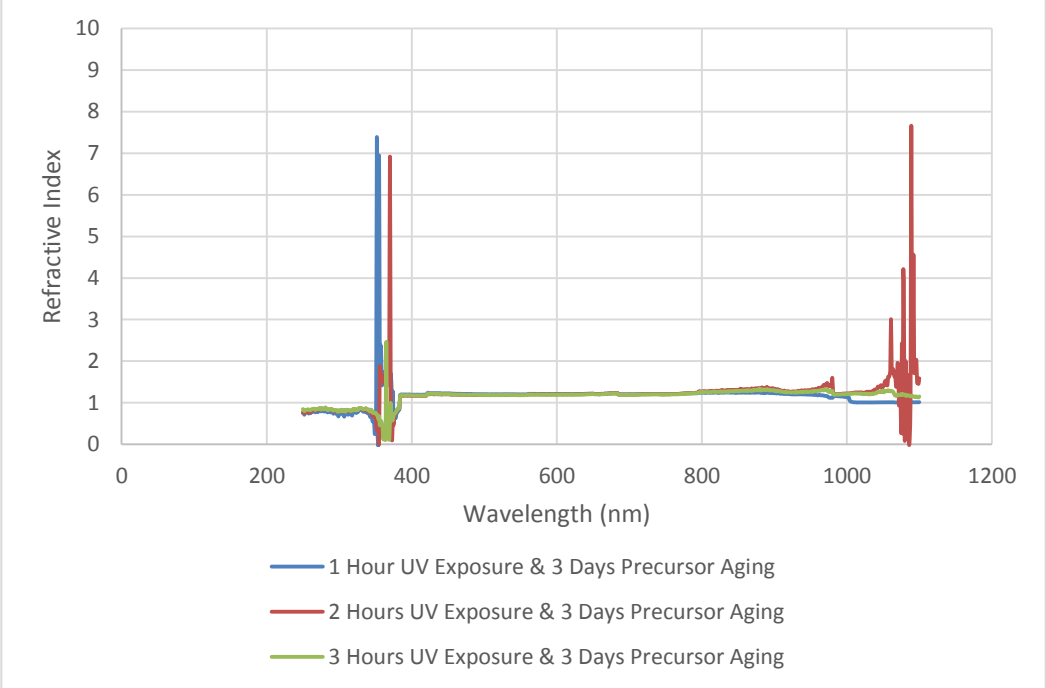


Fig. 4.8 Experimentally obtained refractive index data for CuO after 3 days precursor ageing

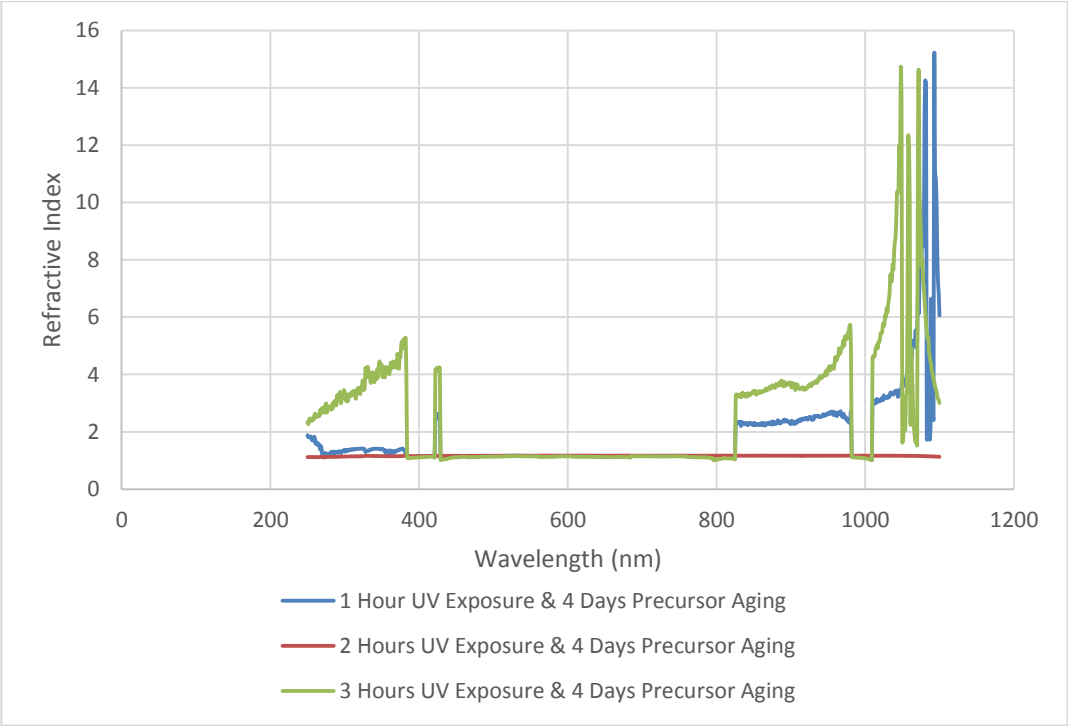


Fig. 4.9 Experimentally obtained refractive index data for CuO after 4 days precursor ageing

4.3 Analysis on the Deviation in Refractive Index

According to (Bass et al., 2009) the theoretical refractive index of ZnO, TiO_2 and CuO depends on the wavelength of the UV light and this is explained by Equation 4.1

$$n = \sqrt{(2.80333 + \frac{0.94470\lambda^2}{\lambda^2 - 0.3004^2} - 0.00714\lambda^2)} \quad (4.1)$$

The above mentioned equation is not applicable for thin film since thin film surface and the sol-gel go through various modifications. Due to the modification of the surface and ageing of the sol-gel, the value of refractive index changes as per (Hong et al., 1997),(Almaral-Sanchez et al., 2005),(Joshi & Mahajan, 2010), (Joshi et al., 2010) and (Cheong & Jasni, 2007).

In CMOS dielectric, the refractive index deviates from the theoretical value due to the following reasons (Hong et al., 1997),(Almaral-Sanchez et al., 2005),(Joshi & Mahajan, 2010), (Joshi et al., 2010) and (Cheong & Jasni, 2007).

- Uniformity in the dielectric dimensions
- Molarity of the precursors
- Ageing of the precursors
- Adhesive UV exposure time
- Energy level of the UV ray
- Orbital structure of material

While fabricating CMOS dielectric, it is imperative to maintain the uniformity of the dielectric dimension as much as possible and this research followed this fact while oxidizing and spin-coating. But, at certain random points the thickness can vary slightly as per (Norland & Martin, 1993). This results in a roughness on the surface which redirects the ray.

Theoretical value has been estimated considering solid crystals and while estimating the theoretical value, a high molarity of sol-gel was considered as per (Bass et al., 2009). In this research, the molarity of the sol-gel was considered lower compared to the molarity considered in (Bass et al., 2009). As a result, theoretical refractive index and measured refractive index was different. As a result, refractive index deviates.

Depending on the material property, ageing of the precursors exhibit changes in the values of refractive index as per (Cheong & Jasni, 2007). (Cheong & Jasni, 2007)

showed that the sol-gel ageing impacts the refractive index in low-K based dielectric where Si-SiO_2 was exploited. Based on that fact this research ages the precursors in the dielectric to exhibit a changed value of refractive index.

Adhesive UV exposure is one of the key factors to change refractive index as per (Cheong & Jasni, 2007). On the dielectric there can be certain portions which are supposed to be comparatively thick and normal annealing process cannot cure these thick portions as per (Norland & Martin, 1993)**.** The process of adhesive UV exposure cures the thick portions with a minimum stress. Though, despite of UV exposure a certain amount of roughness remains on the surface as per (Norland & Martin, 1993).

If the factors like molarity, precursor ageing and UV exposure time would not have taken into account, the energy level/intensity of the adhesive UV ray would made the maximum change in refractive index. At lower wavelength, the frequency of the ray remains high. From the equation of Max Planck we know,

$$E = hf \tag{4.2}$$

Here, h is the Plancks constant, E is the energy intensity and f is frequency. Hence, at lower wavelength the energy level remains high. A highly energized UV ray is more effective in modifying the surface of the dielectric than that of a low wavelength ray. As a result in normal case, at low wavelength the refractive index remains high and vice versa. But, since precursor ageing and UV exposure curing takes place in the experiment, the value of refractive index also varies with ageing and UV exposure. All these oxides absorve high energy UV light. But it cannot absorve low energy UV light.

At lower energy due to less absorbance the refractive index is higher. For ZnO,there is very less sudden peak since rather it maintain a linearity compared to the other graphs. The reason is the outer shell is number 4 with comparatively higher energy where the low energy photons cannot reach easily all of a sudden. Hence, over a range of wavelength it maintains a linearity.

As per (Fujishima & Honda, 1972) in Ti, the outer shell is in no 3. It requires less energy for a photon to go through the holes. Since there are only 4 holes at the outer layer it shows less number of peak. At the highest wavelength the energy of the electron remains very low, this cannot be absorbed by the holes. And the refraction takes place. It is in high energy shell and 9 holes. A low energized photon is observed by high energy shells where there are 8 holes. As a result, there are more number of peaks.

Zn(30) $1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^6\ 3d^{10}\ 4s^2$

Ti(22) $1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^6\ 3d^4$

Cu(29) $1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^6\ 3d^{10}\ 4s^1$

4.4 Statistical Analysis

In this section, the goal is to sort out the minimum and maximum values of refractive index. In this research, once the aged samples are exposed under adhesive UV light, the value of refractive index starts to vary with respect to its normal value (which appears without precursor ageing and UV exposure). These variation in values results in a very low refractive index at certain wavelengths. Similarly, at certain wavelengths it results in a very high refractive index. The minimum value of refractive index in this research carries a significant role, since the aim is to find out the least refractive index sample for RC delay reduction. At the same time, the highest refractive indexed sample

will be exploited for threshold voltage mitigation under NBTI effect. Therefore, the minimum refractive index value is plotted for ZnO, TiO_2 and CuO incorporations in Fig. 4.10, Fig. 4.11 and Fig. 4.12.

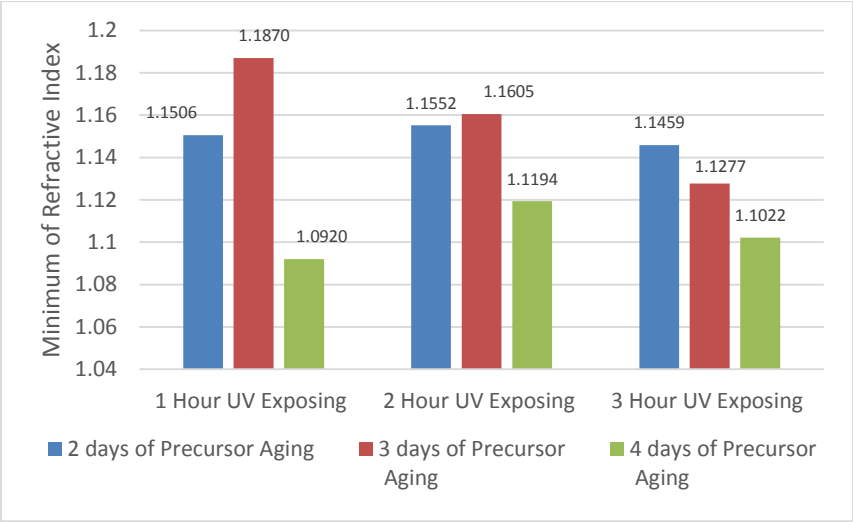


Fig. 4.10 The minimum refractive index values for each sample in ZnO

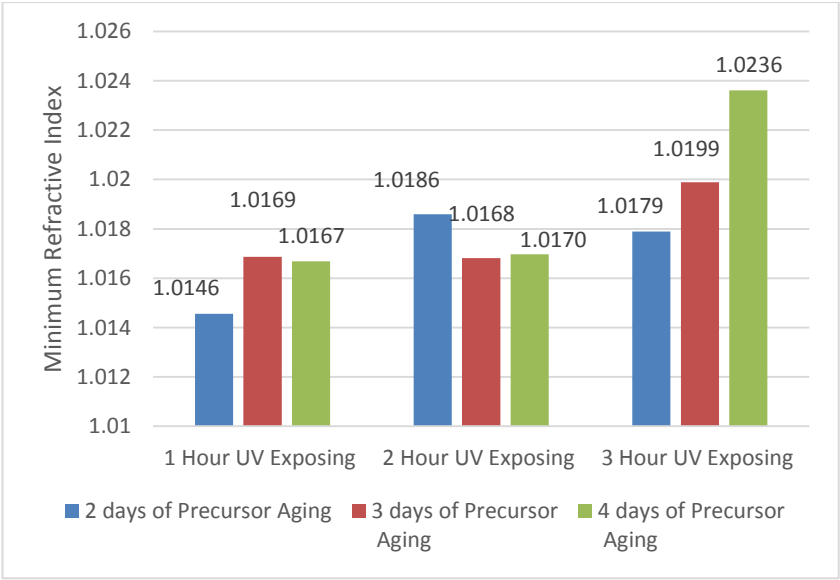


Fig. 4.11 The minimum refractive index values for each sample in TiO_2

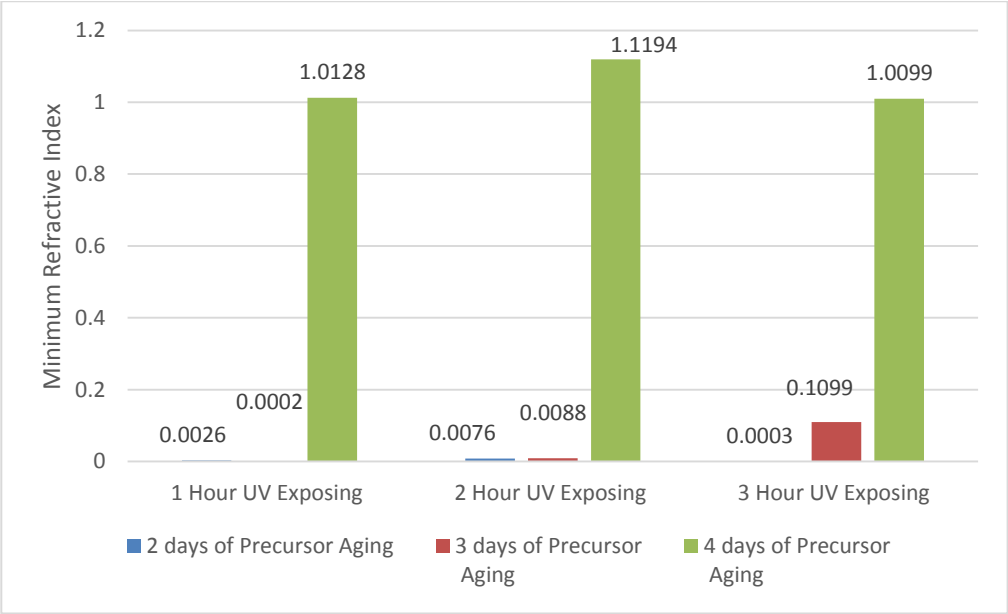


Fig. 4.12 The minimum refractive index values for each sample in CuO

For the case of ZnO, Fig. 4.10 shows that the sample with 1 hour UV exposure and 4 days of precursor ageing exhibits the least value for refractive index. For the case of TiO_2, Fig. 4.11 portrays that the sample with 1 hour UV exposure and 2 days of precursor ageing exhibits the least value for refractive index. Fig. 4.12 shows, the CuO sample with 1 hour UV exposing and 3 days of precursor ageing exhibits the least value for refractive index. The reason behind the deviation in the values of refractive index has been discussed in section 4.3.

Along with the measurement of the minimum value for refractive index, the mean of all refractive indexes was measured for each sample in Fig. 4.13. While taking the averages of the refractive indexes as per Fig. 4.13, it is found that the results obtained from Fig. 4.13 comply with the results obtained from Fig. 4.10. Like Fig. 4.10, Fig. 4.13 shows that the sample with 1 hour of UV exposure and 4 days of precursor ageing

exhibits the least value for refractive index. Sample with 1 hour of UV exposure and 3 days of precursor ageing shows the highest value of refractive index.

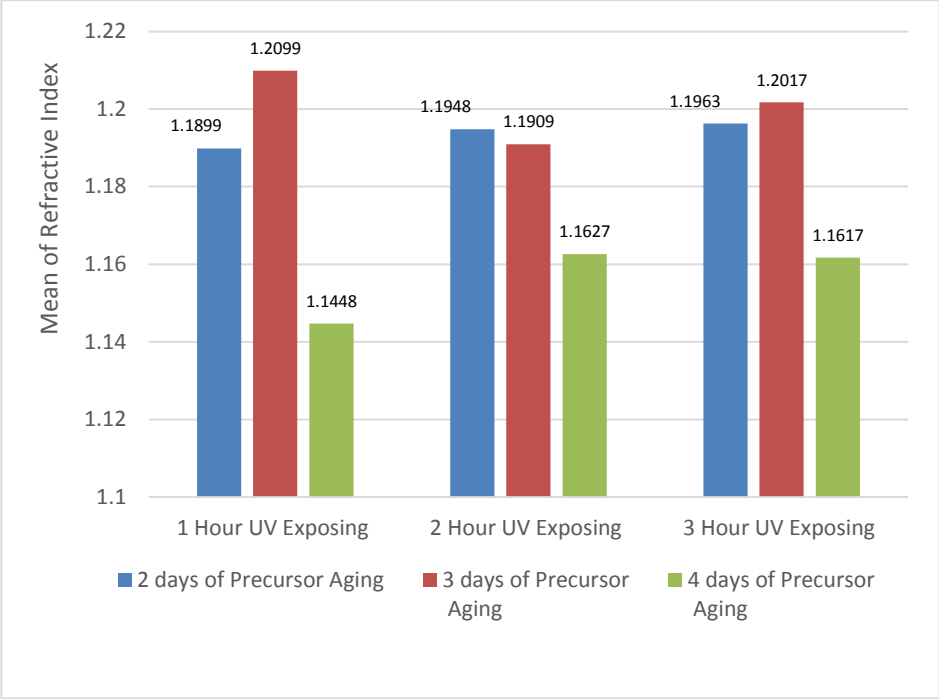


Fig. 4.13. Mean value of refractive index for all samples of ZnO

Hence, from these two statistical tests on ZnO samples, it is observed that the 4 days precursor aged sample with 1 hour of UV exposure shows the least value for refractive index. And 3 days precursor aged sample with 1 hour of UV exposure shows the highest value for refractive index.

The mean of all refractive indexes in TiO_2 was measured for each sample in Fig 4.14. It is found that the results attained from Fig 4.14 comply with the results obtained from Fig 4.11. Like Fig 4.11, Fig 4.14 shows that the sample with 1 hour of UV exposure and 2 days of precursor ageing exhibit the least value for refractive index. Similarly, sample with 3hours of UV exposure and 4 days of precursor ageing shows the highest value of refractive index for TiO_2 incorporated sample.

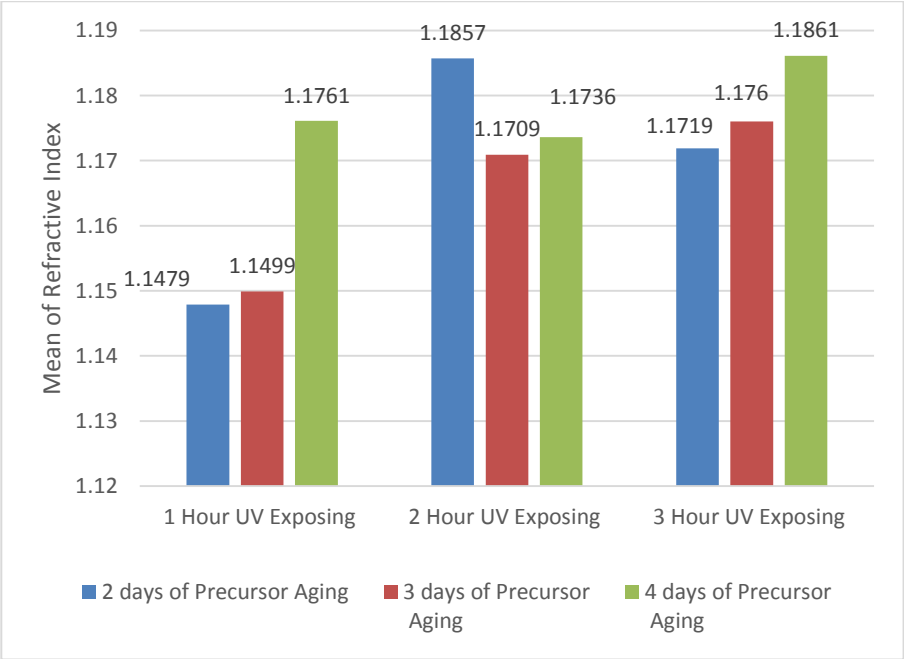


Fig. 4.14. Mean value of refractive index for all samples of TiO_2

From these two statistical tests, it is found that the 2 days precursor aged and 1 hour UV exposed sample shows the least value for refractive index in TiO_2 incorporated Si-SiO_2 dielectric. Similarly, the highest value of refractive index is exhibited by the sample with 4 days precursor ageing and 3 hours exposed sample.

The mean of all refractive indexes for CuO are measured for each sample in Fig. 4.15. While taking the mean of the refractive indexes as per Fig. 4.15, it is found that the results obtained from Fig. 4.12 comply with the results obtained from Fig. 4.15. Like Fig. 4.12, Fig. 4.15 shows that the sample with 1 hour of UV exposing and 3 days of precursor ageing exhibits the least value for refractive index. And, 3 hours of UV exposed and 4 days of precursor aged sample shows the maximum result of refractive index in CuO.

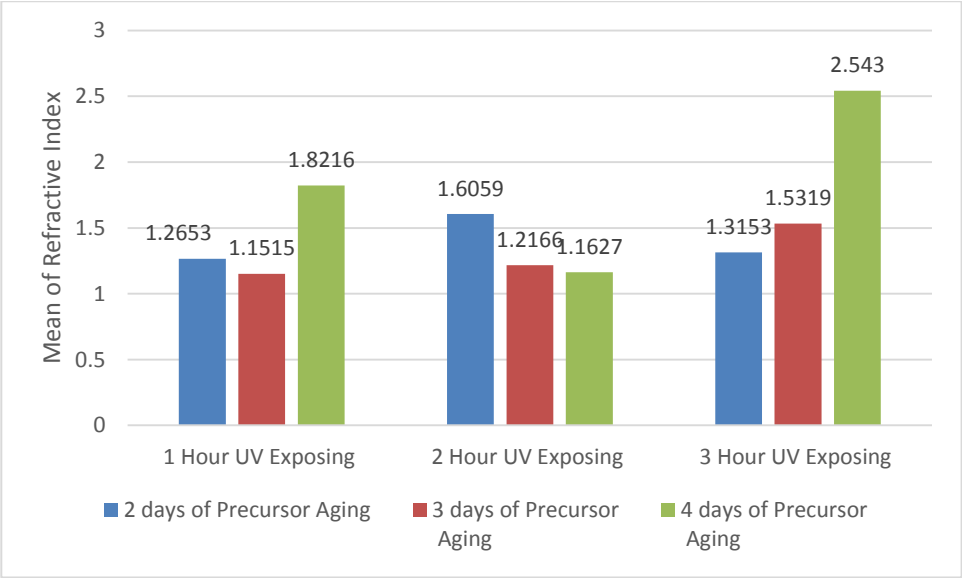


Fig. 4.15. Mean value of refractive index for all samples of CuO

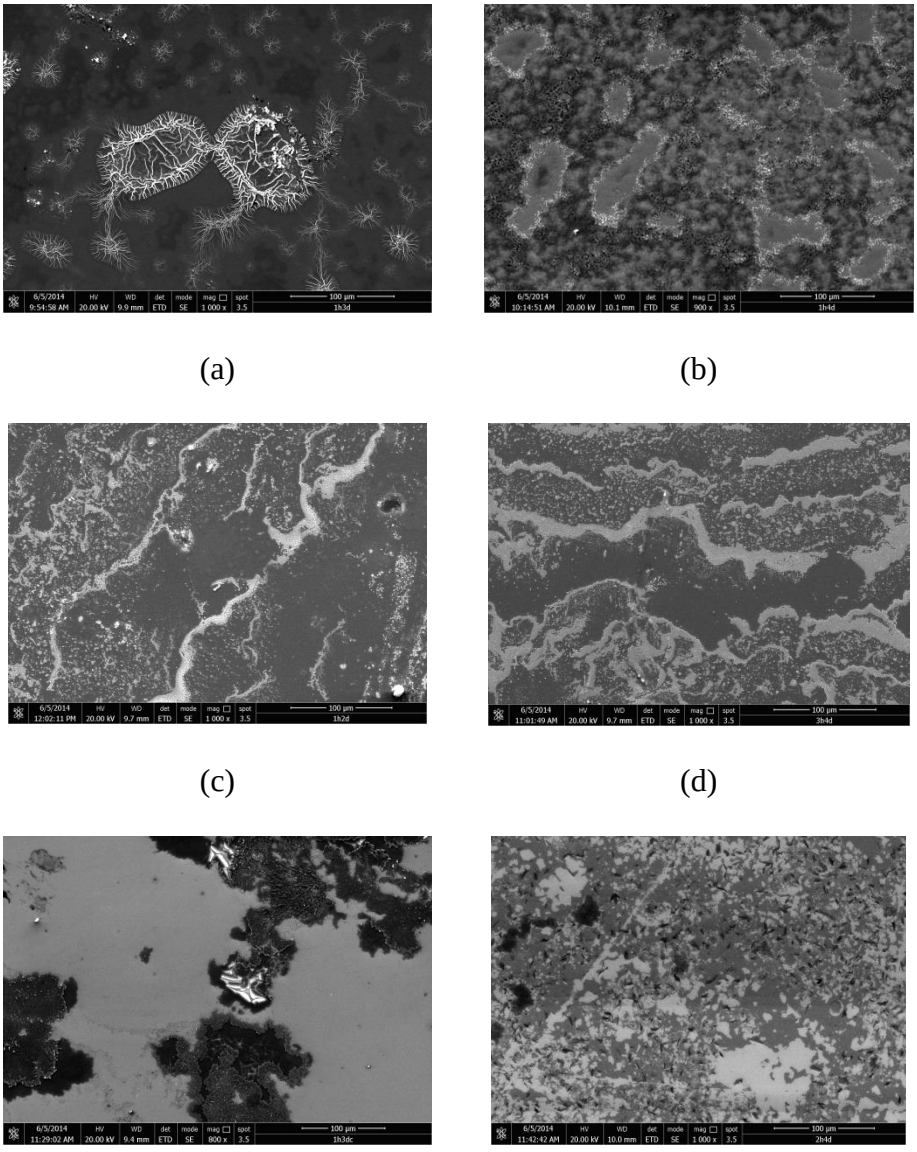
4.5 Morphological Analysis on Surface

Having obtained the data, it is important to validate the data. In this research, morphological analysis helps to determine whether the samples exhibit correct order of refractive index or not. The surface morphology of the lowest and highest refractive indexed samples are captured using Scanning Electron Microscopy (SEM) [APPENDIX I]. In order to validate the results of highest and lowest refractive index, the morphological analysis is performed. But, before proceeding further, it is important to mention that the reason behind not employing infrared (IR) spectroscopy to validate the data.

As per (Christian et al., 2003), the presence of homonuclear diatomic molecules shows weak IR features. In metal oxide incorporated Si-SiO_2 dielectric due to trapping phenomena H_2 will remain present which is a homonuclear diatomic molecule. This might lead to an inaccurate data by IR spectroscopy.

Taking the above factor into account, Scanning Electron Microscopy (SEM) is employed to analyze the surface morphology. Observing the density of the material incorporation, the samples are verified. Column A shows less dense material structures and Column B shows a denser structure in Fig, 4.16. According to (Kucharczyk & Shigorin, 1989) surface density of sol-gel in a sample is proportional to refractive index. From Fig. 4.16 it is observed that the sol-gel samples with low density exhibits low refractive index. As a result, it can be said that the obtained data of this thesis confirms with (Kucharczyk & Shigorin, 1989), since sol-gel density and refractive index are proportional.

Column A **Column B**



(a) (b)

(c) (d)

(e) (f)

Fig 4.16 Surface morphology of the ZnO incorporated SiO_2 samples having (a) lowest and (b) highest refractive index, TiO_2 incorporated SiO2 samples having (c) lowest and (d) highest refractive index and CuO incorporated SiO_2 samples having (e) lowest and (f) highest refractive index captured using SEM

In case of ZnO, Zinc and Oxygen both have one electrons in their outer orbitals and create an s-p bond

Zn(30) $1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^6\ 3d^{10}\ 4s^2$

O(8) $1s^2\ 2s^2\ 2p_x^2 p_y^1 p_z^1$

Since, both Zinc and Oxygen share one electrons and there is no free electron in the ZnO bond, Zinc and oxygen are heavily bonded and maintains an optimum porosity on the sol-gel surface. In normal case, ZnO sol-gel image is shown in Fig. 4.17

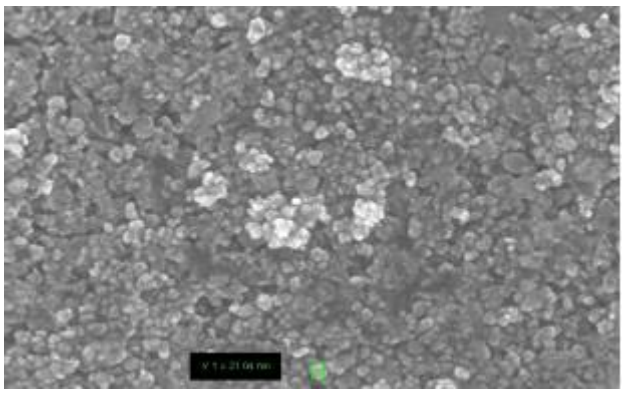


Fig. 4.17 ZnO sol-gel surface porosity without ageing and UV exposure (Source: (Ali, 1999))

Similarly, if Titanium and Oxygen are analysed, it can be seen that two oxygen atoms make bond with one titanium atom and form TiO_2 molecule through two different s-p bonds. Due to two s-p bonds in TiO_2 the porosity is lower than that of ZnO as shown in Fig. 4.18.

Ti(22) $1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^6\ 3d^4$

O(8) $1s^2\ 2s^2\ 2p_x^2 p_y^1 p_z^1$

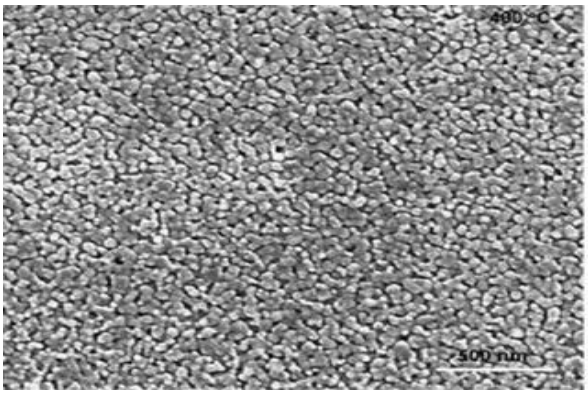


Fig. 4.18 TiO_2 sol-gel surface porosity without ageing and UV exposure (Source:(Meher & Balakrishnan, 2014))

The formation of CuO is very much different than ZnO and TiO_2. The s orbital of Copper and the p_z orbital of Oxygen share one pair of electron whereas in case of ZnO and TiO_2 more than one pair of electrons are involved. Therefore CuO is formed through a comparatively weaker bonding. As a result the porosity in CuO is higher than ZnO and TiO_2 in normal case as per Fig. 4.19.

Cu(29) $1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^6\ 3d^{10}\ 4s^1$

O(8) $1s^2\ 2s^2\ 2p_x^2 p_y^1 p_z^1$

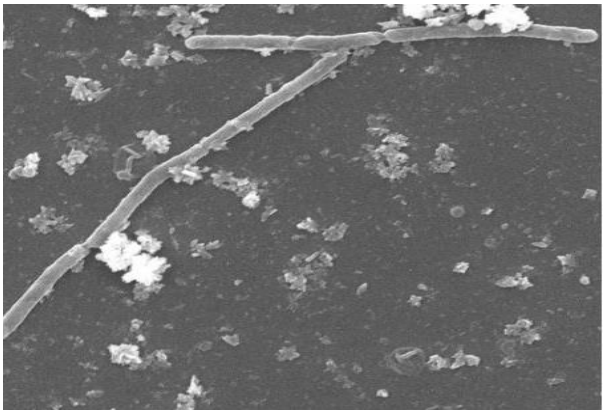


Fig. 4.19 CuO sol-gel surface porosity without ageing and UV exposure (Source: (Pandey et al., 2014))

The samples obtained through ageing and UV exposure exhibit a drastic change in porosity compared to the normal cases as shown above. After treatment, the low dense and highly porous sample shows lowest value of refractive index and the high dense and highly low porosity sample shows highest value of refractive index. This data complies with (Kucharczyk, 1989).

4.6 Energy Dispersive X-ray Microanalysis

According to (Kucharczyk & Shigorin, 1989) surface density of sol-gel in a sample is proportional to refractive index. Therefore, the percentage of Si in a sample is inversely proportional to refractive index. In this research, the sample having higher percentage of Si is supposed to result in lower value of refractive index. In order to measure the percentage of Si, Energy Dispersive X-ray Microanalysis (EDXMA) is used [APPENDIX J]. Fig. 4.20-4.25 show the percentage of Si and other gel materials (O, C, Zn, Ti, Cu and K) on the samples. In case of ZnO incorporated samples, the sample having lower refractive index shows higher percentage of Si in it. On the other hand, the sample having higher refractive index shows lower percentage of Si. This is also true for TiO_2 and CuO incorporated samples.

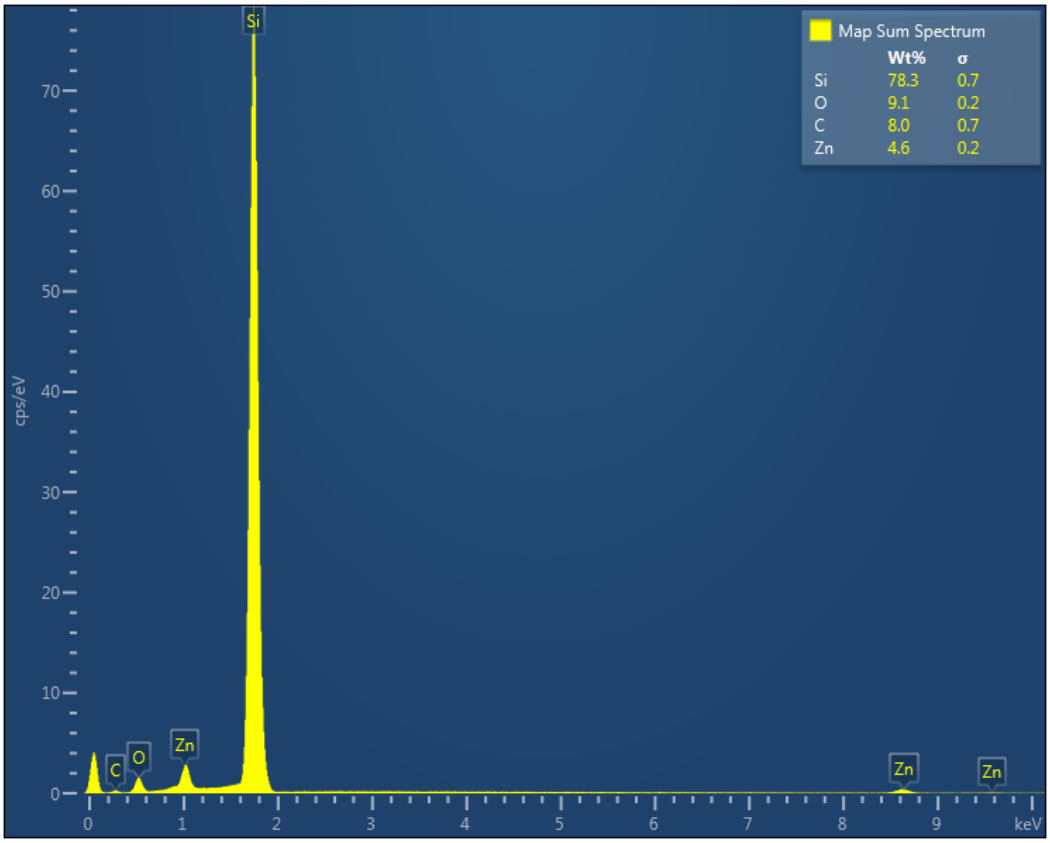


Fig 4.20 EDXMA measured result for ZnO incorporated low refractive index sample

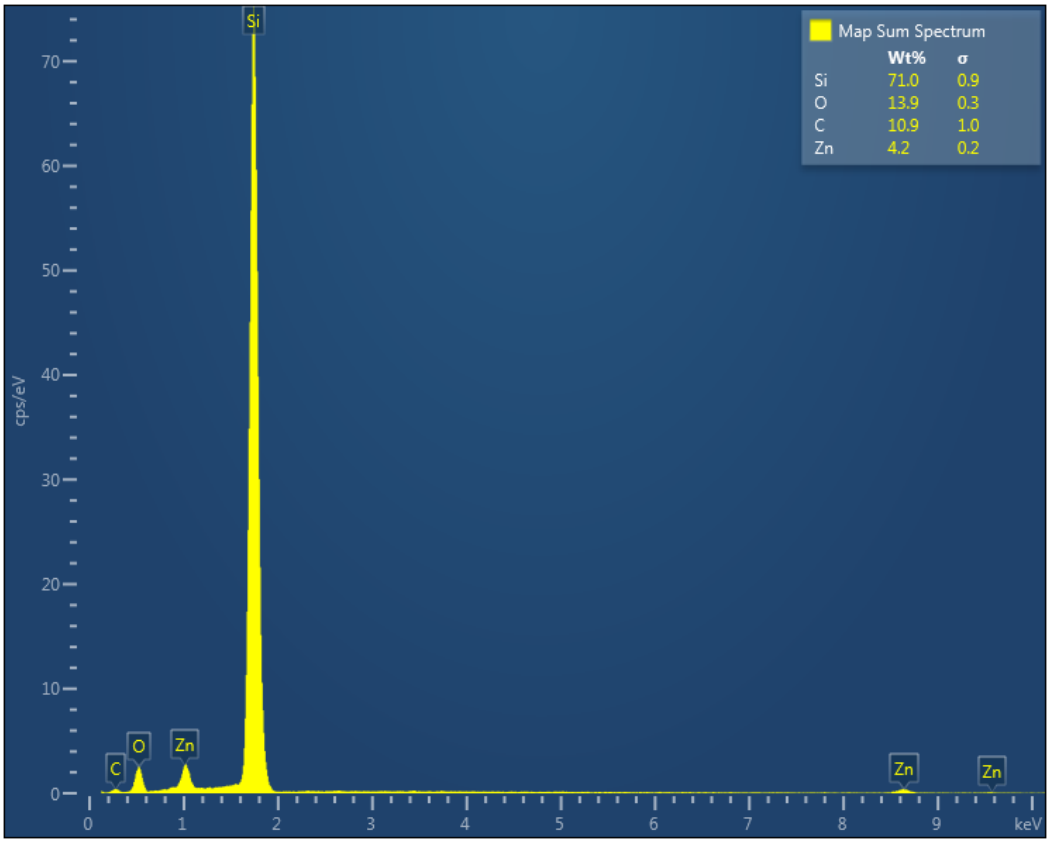


Fig 4.21 EDXMA measured result for ZnO incorporated high refractive index sample

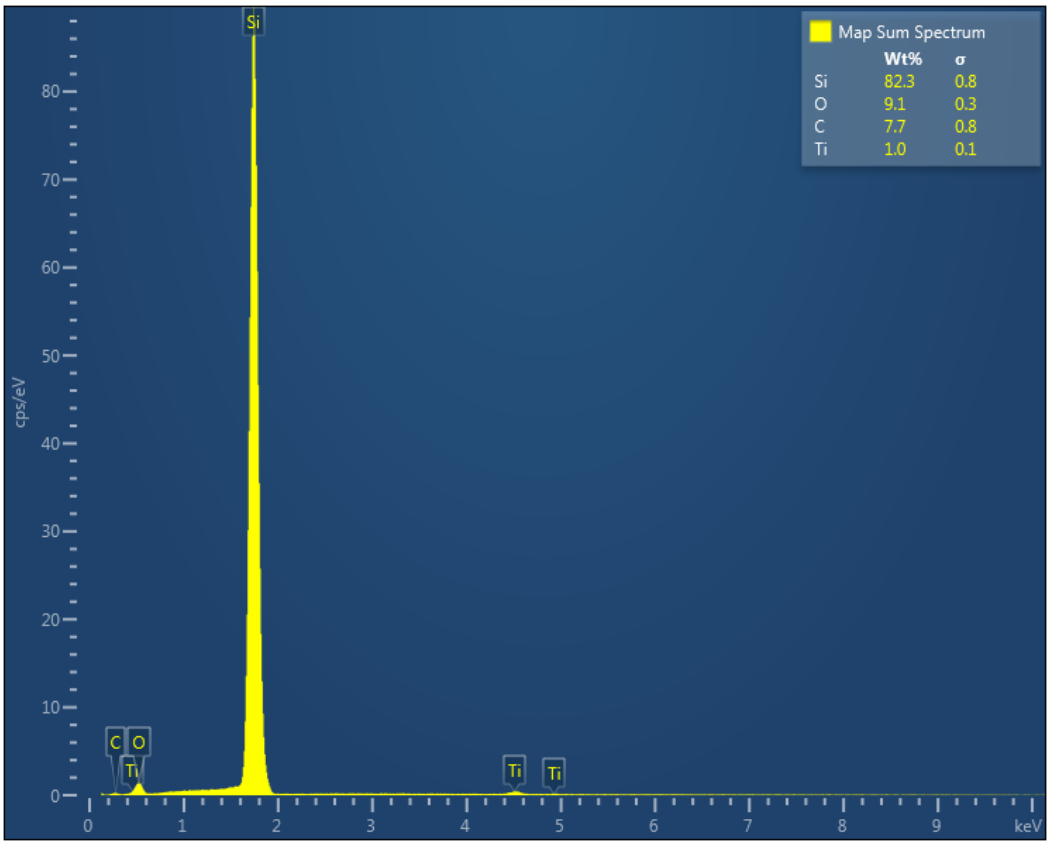


Fig 4.22 EDXMA measured result for TiO_2 incorporated low refractive index sample

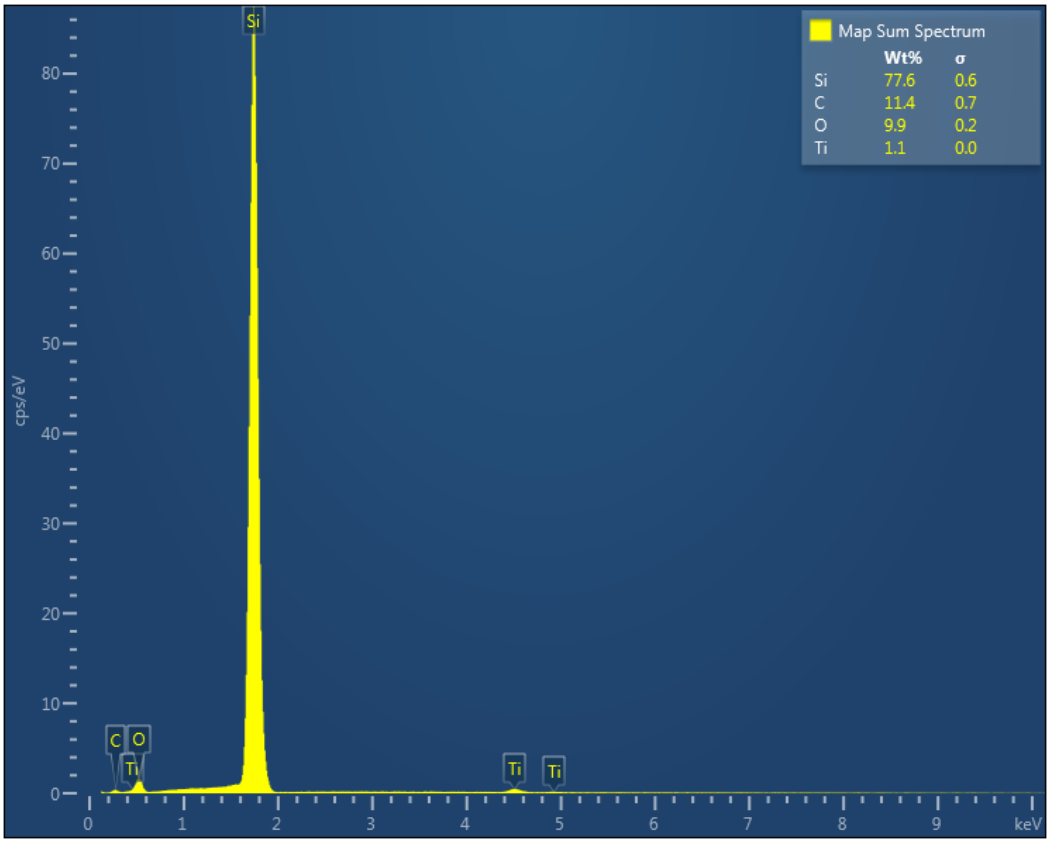


Fig 4.23 EDXMA measured result for TiO_2\incorporated high refractive index sample

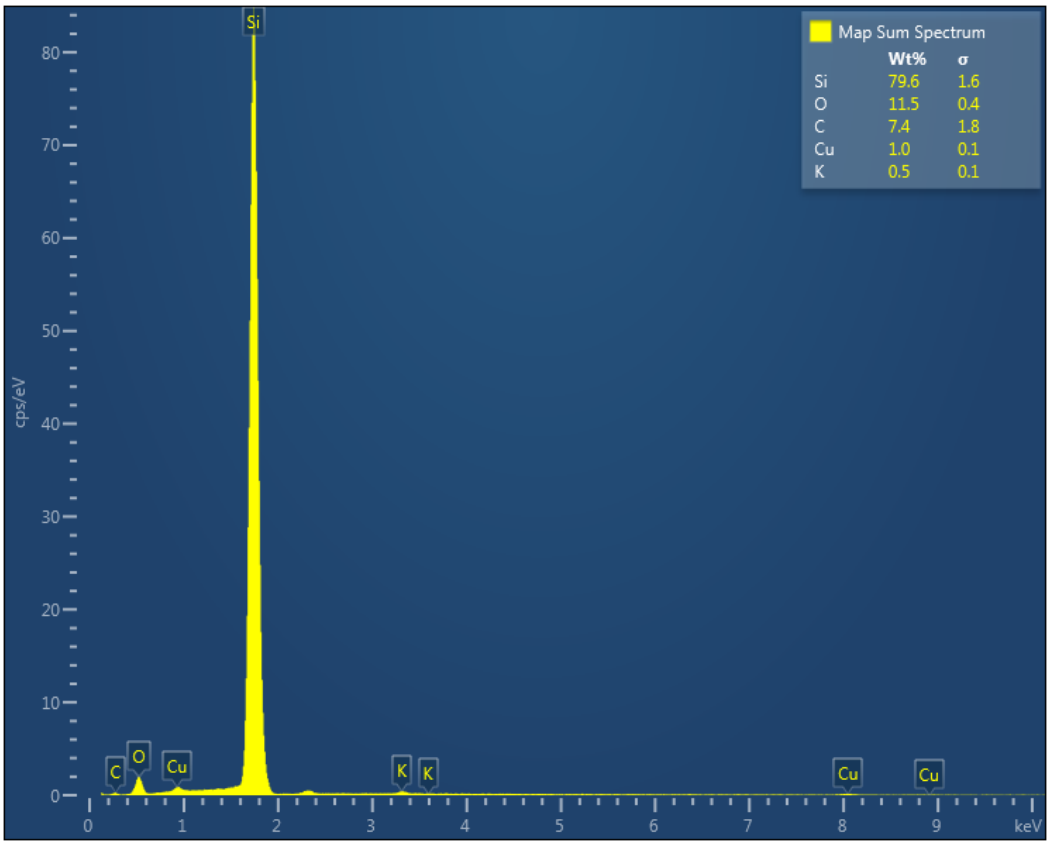


Fig 4.24 EDXMA measured result for CuO\incorporated low refractive index sample

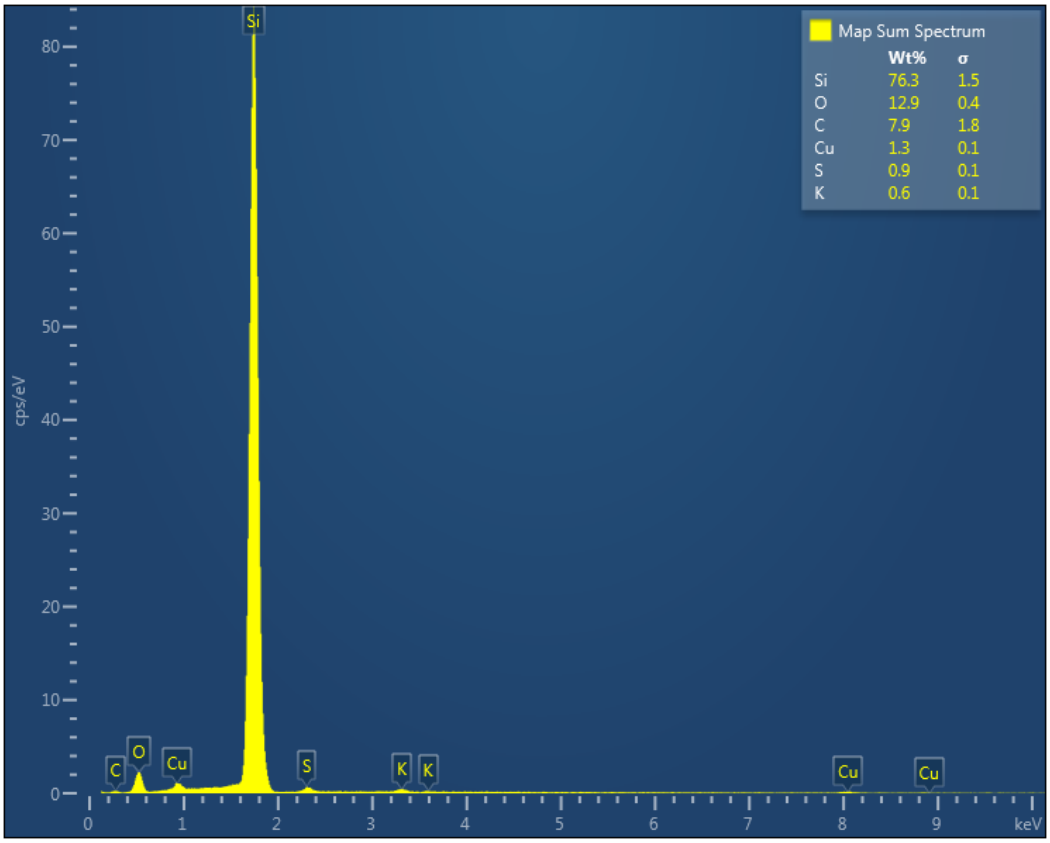


Fig 4.25 EDXMA measured result for CuO\incorporated high refractive index sample

From Fig. 4.17-4.22, it is observed that the sol-gel samples with low density or Si percentage with higher weight density exhibits low refractive index. As a result, it can be said that the data of this thesis confirms with (Kucharczyk & Shigorin, 1989), since sol-gel density and refractive index are proportional.

(Kucharczyk & Shigorin, 1989) referred the following relationships

The density of sol-gel ∞ Refractive Index

The density of substrate ∞ 1/Refractive Index

Hence, the content of Si substrate is inversely proportional to refractive index in this research. The EDXMA data is presented in the tables (Table 4.1-4.3) below. Here, the amount of Si and the amount of Silicon and the amount of sol-gel constitutes 100%.

And As per, (Kucharczyk, 1989) the amount of sol-gel is proportional to refractive index. Therefore, the following relationship can be obtained for Si-SiO_2 substrate.

The density of substrate ∞ 1/Refractive Index

Table 4.1

Si and sol-gel content in ZnO incorporated samples

Si Content in low RI sample	**Sol-gel Content in low RI sample**	**Si Content in low RI sample**	**Solgel Content in high RI sample**
78.3%	21.7%	71%	29%

Table 4.2

Si and sol-gel content in TiO_2 incorporated samples

Si Content in low RI sample	**Solgel Content in low RI sample**	**Si Content in low RI sample**	**Solgel Content in high RI sample**
82.3%	17.7%	77.6%	22.4%

Table 4.3

Si and sol-gel content in CuO incorporated samples

Si Content in low RI sample	**Solgel Content in low RI sample**	**Si Content in low RI sample**	**Solgel Content in high RI sample**
79.6%	20.4%	76.3%	23.7%

In the tables (Table 4.1-4.3), the samples showing high amount of Si results in low refractive index and the samples showing low amount of Si results in high refractive index. This confirms with the literature of (Kucharczyk, 1989) and validates the data.

4.7 Extraction of Dielectric Constant

Compared to the previous works, this work contributes in lowering the dielectric constant considering the effect of ZnO, TiO_2 and CuO incorporation since the square of refractive index is equal to dielectric constant (Cheong & Jasni, 2007) as mentioned in Equation 4.3.

$$\varepsilon = R^2 \tag{4.3}$$

Here, Here, ε= Dielectric Constant, R= Refractive Index,

Hence, the lowest obtained dynamic dielectric constant is 1.1924 for the 4-day precursor aged sample with 1 hour of UV exposure for ZnO. For TiO_2, Results show that the smallest obtainable dynamic dielectric constant is 1.0294 which is found by examining the one hour UV exposed precursor sample after two days ageing. And, for

CuO, Results show that the smallest obtainable dynamic dielectric constant is 4E-08 which is found by examining the one hour UV exposed precursor sample after three days ageing.

4.7.1 Derivation of the Extraction of dielectric Constant

From Maxwell's Equation (Ward & Pendry, 1996) and (Cambridge, 1999),

$$\nabla XE = -\partial B/\partial t \tag{4.4}$$

$$\nabla XB = \mu\varepsilon\partial E/\partial t \tag{4.5}$$

Here, *E*= Electric Field and *B*= Magnetic Field. Taking a curl in Equation (4.4) we get,

$$\nabla X(\nabla XE) = -\frac{\partial(\nabla XB)}{\partial t} \tag{4.6}$$

Putting the value of Equation (4.5) into Equation (4.6) we get,

$$\nabla X(\nabla XE) = -\mu\varepsilon\partial^2 E/\partial t^2 \tag{4.7}$$

If Equation (4.7) is considered in 1D and $X(\nabla XE) = -\nabla^2 E + \nabla.(\nabla.E)$,

$$\frac{\partial^2 E}{\partial x^2} = \mu\varepsilon\partial^2 E/\partial t^2 \tag{4.8}$$

A possible solution to Equation (4.8) is a sinusoidal wave as per Equation (4.9) where $\boldsymbol{\lambda}$ and C are wavelength and speed of light respectively.

$$E = E_0 Sin(\frac{2\pi(x-ct)}{\lambda})$$

Differentiating the above equation with respect to distance, *x* and time, *t*

$$\frac{\partial^2 E}{\partial x^2} = -E_0(\frac{2\pi}{\lambda})^2 Sin(2\pi(x-ct)/\lambda) \tag{4.9}$$

$$\frac{\partial^2 E}{\partial t^2} = -E_0(\frac{2\pi c}{\lambda})^2 Sin(2\pi(x - ct)/\lambda) \quad (4.10)$$

Substituting the values of Equation (4.9) and (4.10) in Equation (4.8),

$$-E_0(\frac{2\pi}{\lambda})^2 Sin(2\pi(x - ct)/\lambda) = -E_0\mu\varepsilon(\frac{2\pi c}{\lambda})^2 Sin(2\pi(x - ct)/\lambda) \quad (4.11)$$

After simplifying Equation (4.11)

$$C = (\mu\varepsilon)^{-1/2} \quad (4.12)$$

In this research, ZnO, CuO and TiO_2 are used as incorporations. None of these materials are ferromagnetic and the permeability is considered as μ_0 and if the dielectric constant is considered ε_0 in vacuum (in vacuum $\varepsilon_0 = 1$)

$$C = (\mu_0)^{-1/2} \quad \text{[For vacuum]} \quad (4.13)$$

$$C_m = (\mu_0\varepsilon)^{-1/2} \quad \text{[For any nonmagnetic material]} \quad (4.14)$$

And, $\frac{C}{C_m} = R$

From Equation (4.13) and (4.14),

$$\varepsilon = R^2 \quad (4.15)$$

Derived Equation (4.15) complies with the Equation (4.3) which was used to extract dielectric constant. At the same time the derivation of Equation (4.15) also complies with the equation used by (Cheong & Jasni, 2007).

4.7.2 Considering Impedance Spectroscopy

The extraction performed in Section 4.7.1 considered a single dielectric. The other literary works which reduced dielectric constant also considered a dielectric. But, if a full transistor is fabricated then the value of dielectric constant will be different due to parasitic capacitance of electrodes. In this research the full formation of the transistor was not implemented in order to eliminate parasitic. But, this section investigates the theoretical analysis on the dielectric constant considering the effects of impedance spectroscopy. The following analysis gives a relationship between refractive index, *R* and frequency, f as per Equation 4.16. Equation (4.16) is obtained from (Němec, Kadlec, Kužel, Duvillaret, & Coutaz, 2006). From this equation dielectric constant is extracted through the use of experimentally obtained refractive indices.

$$R = 1 + (\frac{c}{2\pi fd})(2\pi T_0 + 2\pi (\frac{(z^2+2z+1)}{4z} + 2\pi s \quad (4.16)$$

Here, $z = \sqrt{(\mu/\varepsilon)}$, T_0=Measurement Time, C=Speed of light, S is an integer value which returns to unity in a complete cycle of 2π, μ=Permeability and ε= Dielectric constant.

Simplifying Equation (4.16),

$$z^2 - z\left[\left(\frac{fd}{c}\right)(R-1) - T_0 - \frac{1}{2} - 2s\right] + 1 = 0 \quad (4.17)$$

Considering,

$$\left[\left(\frac{fd}{c}\right)(R-1) - T_0 - \frac{1}{2} - 2s\right] = b$$

Therefore, Equation (4.17) can be written as,

$$z^2 - zb + 1 = 0 \quad (4.18)$$

Therefore, $z = (b + (\sqrt{b^2 - 4}))/2$ (4.19)

And, $z = (b - (\sqrt{b^2 - 4}))/2$ (4.20)

Equation (4.20) generates a negative value for z which is not practically possible since μ and ε are positive.

Considering the value of $z = \sqrt{(\mu/\varepsilon)}$ in Equation (4.19)

$$\sqrt{(\mu/\varepsilon)} = (b + (\sqrt{b^2 - 4}))/2 \quad (4.21)$$

Hence, by squaring both sides of Equation (4.21)

$$\mu/\varepsilon = (b + (\sqrt{b^2 - 4}))^2/4 \quad (4.22)$$

At the same time,

$$\mu = (R^2)/\varepsilon$$

Putting the value of μ in Equation (4.22),

$$R^2/\varepsilon^2 = (b + (\sqrt{b^2 - 4}))^2/4 \quad (4.22)$$

Simplifying Equation (4.22)

$$\varepsilon = 2R/(b + (\sqrt{b^2 - 4})) \quad (4.23)$$

Considering, T_0 =1 s for a fresh device, s=1 for a total 2π cycle, c=3X10^8 m/s and=2X10^{-9} m, the value of b can be simplified as,

$$b = 6.7fX10^{-16}X(R - 1) - 7/2$$

Putting the value of in Equation (4.23),

$$\varepsilon = 2R/((6.7fX10^{-16}X(R-1) - \frac{7}{2}) + (\sqrt{(6.7fX10^{-16}X(R-1) - 7/2)^2 - 4}))$$

…… (4.24)

From the experimentally obtained values of R for ZnO, TiO2 and CuO, Fig. 4.26-4.28 were plotted over 1~10 GHz frequency.

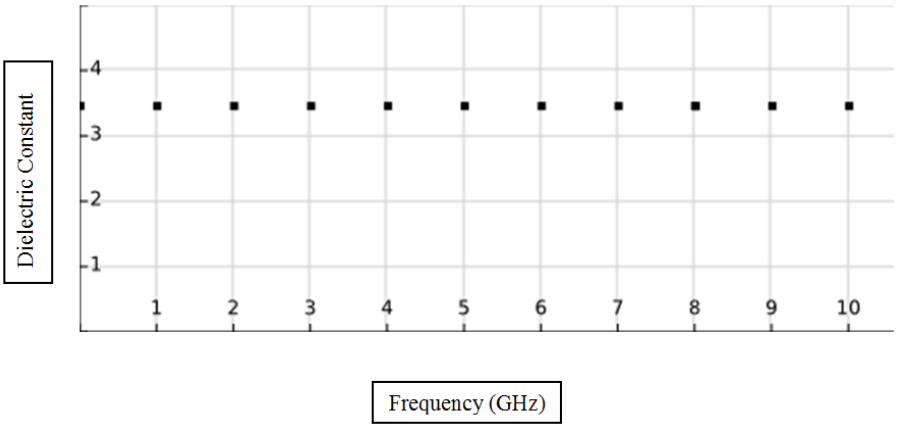


Fig. 4.26 Dielectric constant (3.47) for ZnO incorporation considering theoretical derivation on impedance spectroscopy

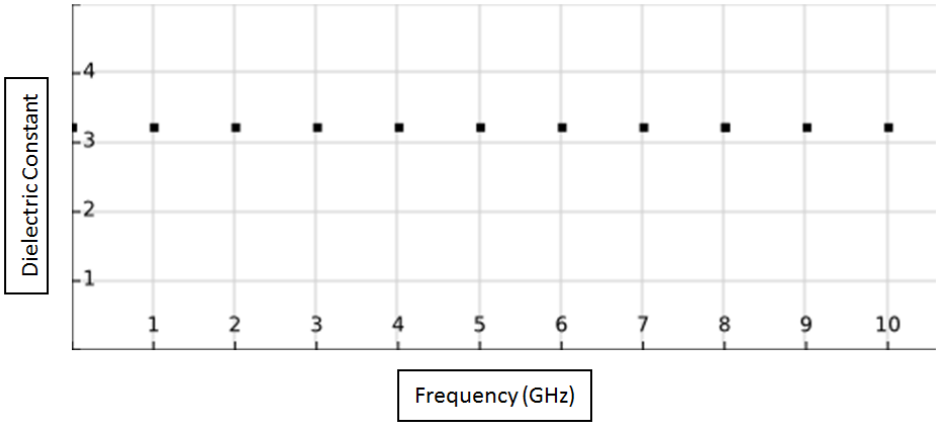


Fig. 4.27 Dielectric constant (3.23) for TiO_2 incorporation considering theoretical derivation on impedance spectroscopy

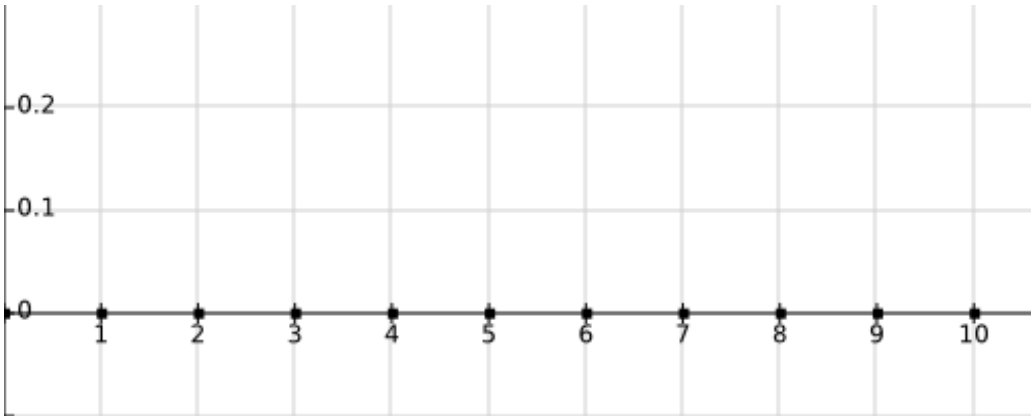


Fig. 4.28 Dielectric constant ($6.37X10^{-4}$) for CuO incorporation considering theoretical derivation on impedance spectroscopy

Considering the impedance effect in a MOSFET the dielectric constant of ZnO, TiO_2 and CuO are 3.47, 3.23 and $6.37X10^{-4}$ respectively. These values are different compared to the experimentally obtained values since in experiment the effect of parasitic capacitance is excluded. With respect to AC frequency these values do not change since the parameters adjacent to the frequency in Equation (4.24) exhibit very negligible values which do not make much difference in dielectric constant over time.

These values are obtained from the experimentally obtained refractive index values. In the future analysis in this thesis, the obtained dielectric constants through impedance analysis will not be taken into account since only a dielectric is fabricated in this research and the previous literary works also considered their research with dielectric.

4.8 Evaluation of NBTI

Since NBTI affects the shift in threshold voltage and in a worn-out device the threshold voltage shift remains high (Alam et al., 2007). Considering this, one of the aims of this work is to lower the change in threshold voltage. In order to evaluate NBTI induced threshold voltage shift, the model by (Kumar et al., 2009a) is employed. The reason behind exploiting this model is described in the literature review (**Chapter 2**).

According to (Kumar et al., 2009a), the change in threshold voltage is inversely proportional to the oxide capacitance and hence, refractive index. In such case, if a high valued sample of refractive index is considered, there will be a small shift in threshold voltage. To mitigate NBTI, it is imperative consider the maximum value for refractive index to see a small increment in threshold voltage by exposing the sample under a wavelength which gives highest refractive index. The length of the device is set to 16nm while evaluating the change in threshold voltage.

This evaluation of NBTI under both DC and AC stress is performed in this section. Under both types of stress, normal case (Si-SiO_2 dielectric), ZnO, TiO_2 and CuO incorporations are considered for the purpose of evaluation. Therefore, based on this evaluation, results are estimated.

4.8.1 Evaluation of NBTI under DC Stress

For evaluating NBTI under DC stress, the following conditions are considered according to Table 4.4. The values are derived from (Kumar et al., 2009a).

Table 4.4

Parameter values for evaluating NBTI under DC stress

Parameters	**Values**
Diffusion Coefficient in oxide	$4X10^{-17}$ (cm^2/s)
Diffusion Coefficient in poly	10^{-17} (cm^2/s)
Forward Rate Constant	4.66 (cm^3/s)
Reverse Rate Constant	$4.48X10^{-19}$ (cm^3/s)
Oxide Thickness	$9.5X10^{-10}$ (m)
Oxide Capacitance in normal case	$3.9X(8.854X10^{-14})$/oxide thickness (F)
Oxide Capacitance for ZnO incorporation	Dynamic Dielectric Constant for cured ZnO X $(8.854X10^{-14})$/oxide thickness (F)
Oxide Capacitance for TiO_2 incorporation	Dynamic Dielectric Constant for cured TiO_2 X $(8.854X10^{-14})$/oxide thickness (F)
Oxide Capacitance for CuO incorporation	Dynamic Dielectric Constant for cured CuO X $(8.854X10^{-14})$/oxide thickness (F)

Normal Case

To mitigate NBTI, it is imperative consider the maximum value for refractive index to see a small increment in threshold voltage by exposing the sample under a wavelength which gives highest refractive index.

In this section, the threshold voltage shift for Si-SiO_2 dielectric is considered so that it can be compared with the threshold voltage shift for other high-K metal oxide incorporation. Figure 4.29 shows the change in threshold voltage due to NBTI with respect to 10 years of time.

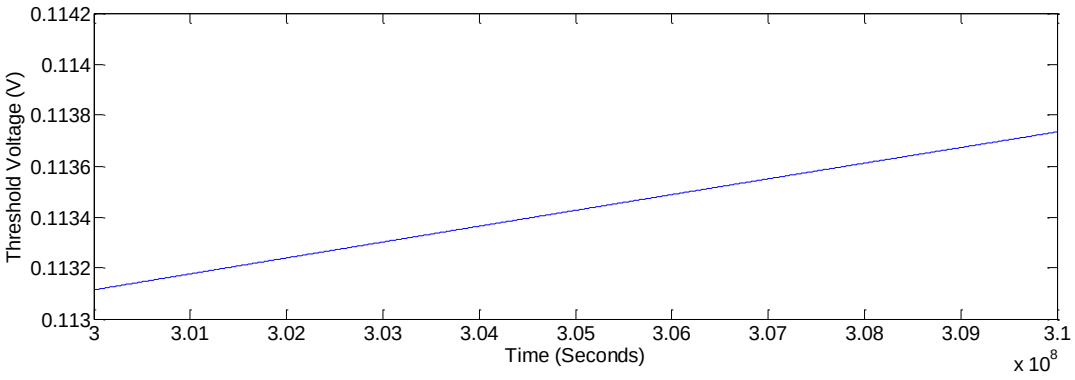


Fig 4.29. Threshold voltage change due to NBTI considering normal case under DC stress

Case of ZnO Incorporation

This section refers to aged and UV exposed ZnO incorporated dielectric where the maximum value of refractive index and dynamic dielectric constant were selected out of all samples by changing the wavelength. Fig 4.30 shows the change in threshold voltage due to NBTI with respect to 10 years of time. The threshold voltage change under ZnO incorporation is not less than pure Si-SiO_2 incorporation. Hence, ZnO does not manifest an increment in drive current. Before it is explained, it is imperative to mention that according to R-D framework (Jeppson & Svensson, 1977),(Alam et al., 2007) & (Kumar et al., 2009a), once the stress is applied hydrogen ions and molecules form traps. But being amphoteric oxide; ZnO does not react with H_2; though it accepts H+ ion as per (Shi, Saboktakin, Stavola, & Pearton, 2004) & (Shi et al., 2005). As a result, ZnO does not get absorbed by H_2 and the hydrogen induced trap remains which does not let the drain current to go high under ZnO incorporation.

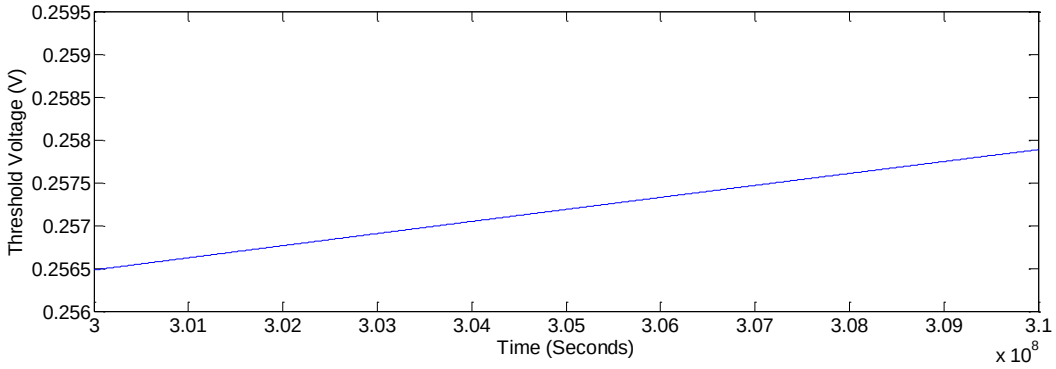


Fig. 4.30. Threshold voltage change due to NBTI considering aged and UV exposed ZnO Incorporation under DC stress

Case of TiO_2 Incorporation

This section refers to aged and UV exposed TiO_2 incorporated dielectric where the maximum value of refractive index and dynamic dielectric constant were considered among all samples by changing the wavelength. Fig 4.31 shows the change in threshold voltage due to NBTI with respect to 10 years of time. The interaction of hydrogen species with TiO_2 is a debated topic. Though, so far no researcher denied the absorption of TiO_2 by H2. In 1981, studies by (Henrich & Kurtz, 1981) showed that despite of chemical reaction TiO_2 does not react with H_2 molecule very strongly. Later, this study was refuted by (Göpel, Rocker, & Feierabend, 1983). According to (Göpel et al., 1983), two hydrogen atoms in a hydrogen molecule make bond with two oxygen atoms in TiO_2. Hence, if oxygen atoms get bonded with the hydrogen atoms; yet the remaining H+ ion remain as traps inside the dielectric. This results in a small amount of trap inside the dielectric. Though, a major portion of the trap is passivated by TiO_2 incorporation. Since, trap gets passivated; there is a boost in drain current.

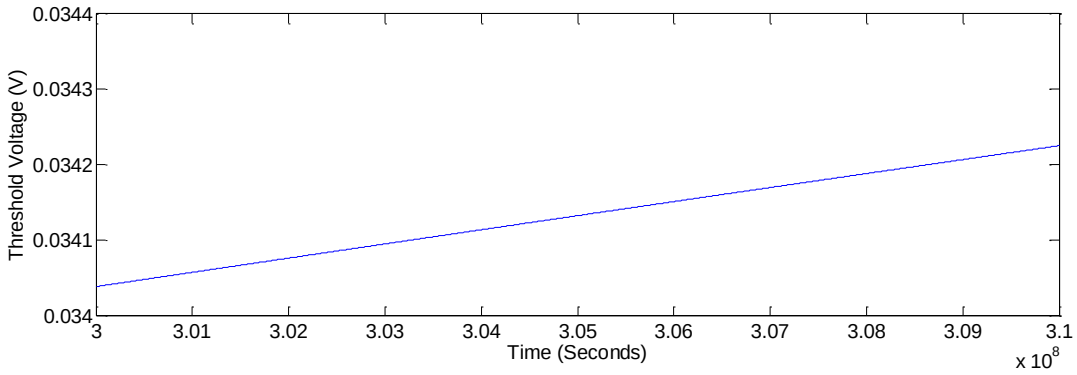


Fig. 4.31. Threshold voltage change due to NBTI considering aged and UV exposed TiO_2 Incorporation under DC stress

Case of CuO Incorporation

It refers to aged and UV exposed CuO incorporated dielectric where the maximum value of refractive index and dynamic dielectric constant are sorted out of all samples by changing the wavelength. Figure 4.32 shows the change in threshold voltage due to NBTI with respect to 10 years of time. In case of CuO incorporation, CuO reduces the traps by reacting with H+ ion and H_2 molecule. Since, CuO is an amphoteric oxide; it accepts hydrogen ion in a chemical reaction and reacts with hydrogen molecule as mentioned in (Kim, Rodriguez, Hanson, Frenkel, & Lee, 2003). And a major portion of trap gets passivated and drain current goes high.

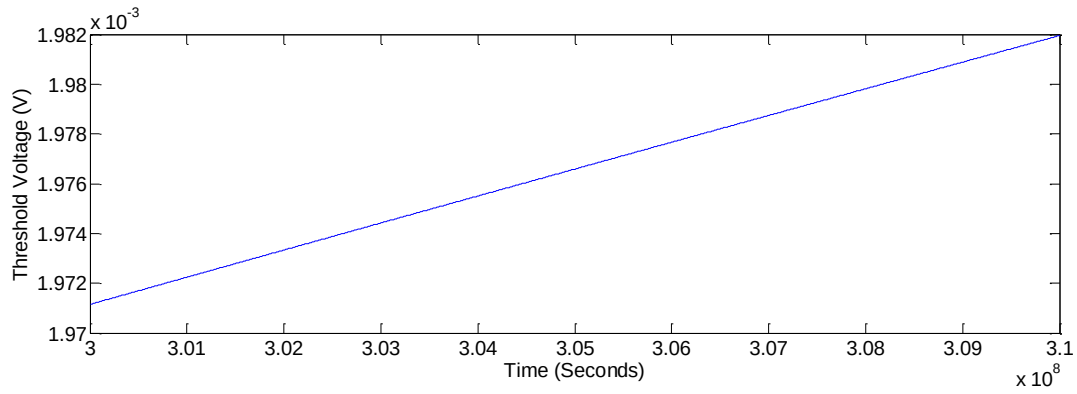


Fig. 4.32. Threshold voltage change due to NBTI considering aged and UV exposed CuO Incorporation under DC stress

4.8.2 Evaluation of NBTI under AC Stress

For evaluating NBTI under AC stress, the following conditions are considered according to Table 4.5. The values have been derived from (Kumar et al., 2009a).

Table 4.5

Parameter values for evaluating NBTI under AC stress

Parameters	**Values**
Diffusion Coefficient in oxide	$4X10^{-17}$ (cm^2/s)
Diffusion Coefficient in poly	10^{-17} (cm^2/s)
Forward Rate Constant	4.66 (cm^3/s)
Reverse Rate Constant	$4.48X10^{-19}$ (cm^3/s)
Oxide Thickness	$9.5X10^{-10}$ (m)
Oxide Capacitance in normal case	$3.9X(8.854X10^{-14})$/oxide thickness (F)
Oxide Capacitance for ZnO incorporation	Dynamic Dielectric Constant for cured ZnO X $(8.854X10^{-14})$/oxide thickness (F)
Oxide Capacitance for TiO_2 incorporation	Dynamic Dielectric Constant for cured TiO_2 X $(8.854X10^{-14})$/oxide thickness (F)
Oxide Capacitance for CuO incorporation	Dynamic Dielectric Constant for cured CuO X $(8.854X10^{-14})$/oxide thickness (F)

Normal Case

This section is about Si-SiO_2 dielectric. Fig. 4.33 shows the change in threshold voltage due to NBTI with respect to 10 years of time.

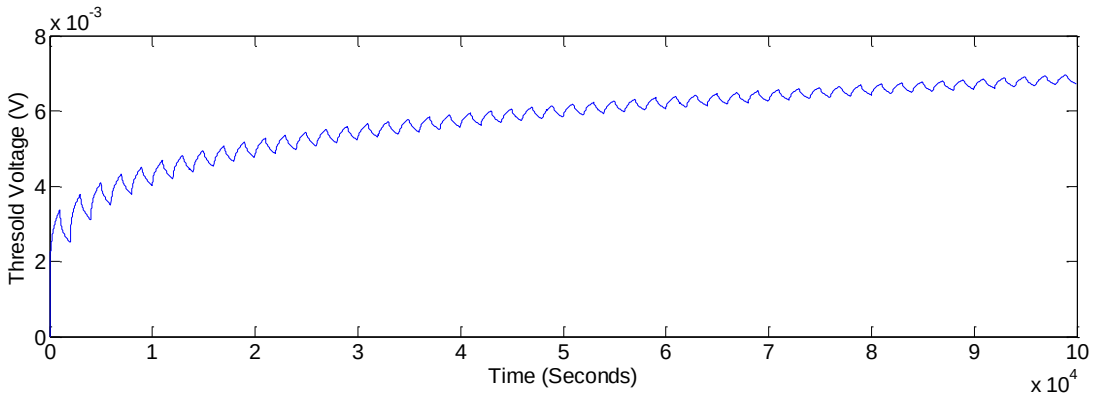


Fig. 4.33. Threshold voltage change due to NBTI considering normal case under dynamic stress

Case of ZnO Incorporation

Here, the elaboration is about aged and UV exposed ZnO incorporated dielectric where the maximum value of refractive index is considered out of all samples. Fig. 4.34 shows the change in threshold voltage due to NBTI with respect to 10 years of time. The reason behind low drain current in ZnO refers back to Section 4.8.2.

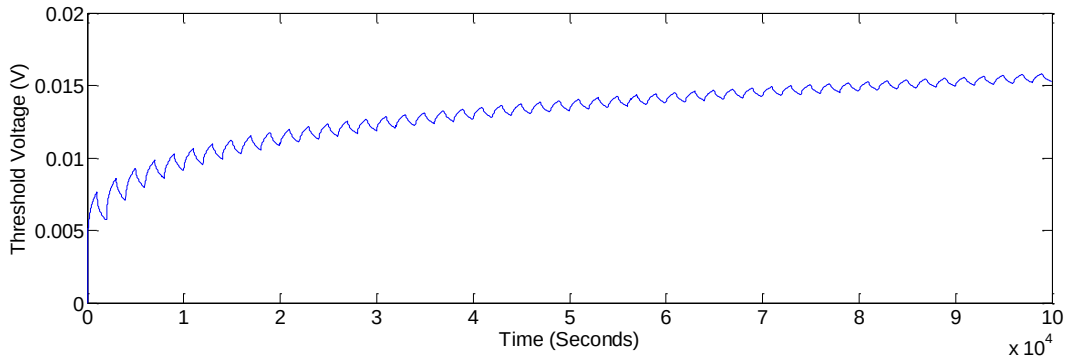


Fig. 4.34. Threshold voltage change due to NBTI considering aged and UV exposed ZnO under dynamic stress

Case of TiO_2 Incorporation

It refers to aged and UV exposed TiO_2 incorporated dielectric where the maximum value of refractive index is sorted out of all samples by changing the wavelength. Fig. 4.35 shows the change in threshold voltage due to NBTI with respect to 10 years of time. The reason behind drain current increment and trap passivation in TiO_2 incorporation refers back to Section 4.8.2.

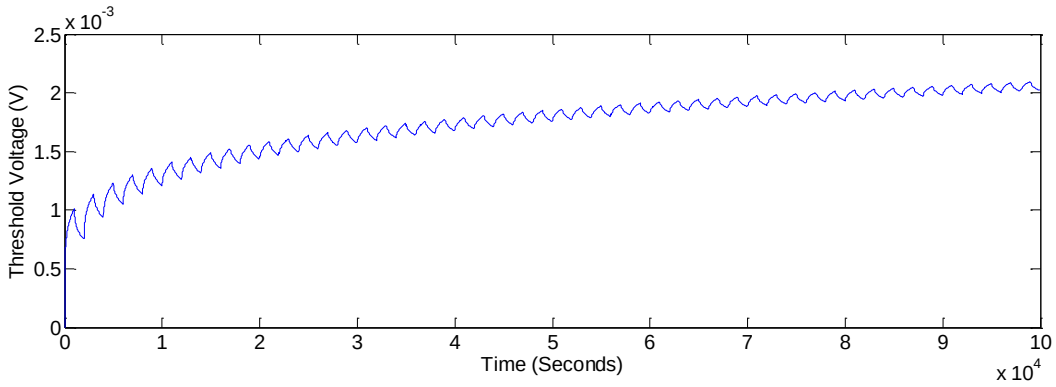


Fig. 4.35. Threshold voltage change due to NBTI considering aged and UV exposed TiO_2 under dynamic stress

Case of CuO Incorporation

It refers to aged and UV exposed CuO incorporated dielectric where the maximum value of refractive index is exploited out of all samples by changing the wavelength. Fig. 4.36 shows the change in threshold voltage due to NBTI with respect to 10 years of time. The reason behind drain current increment and trap passivation in CuO incorporation refers back to Section 4.8.2.

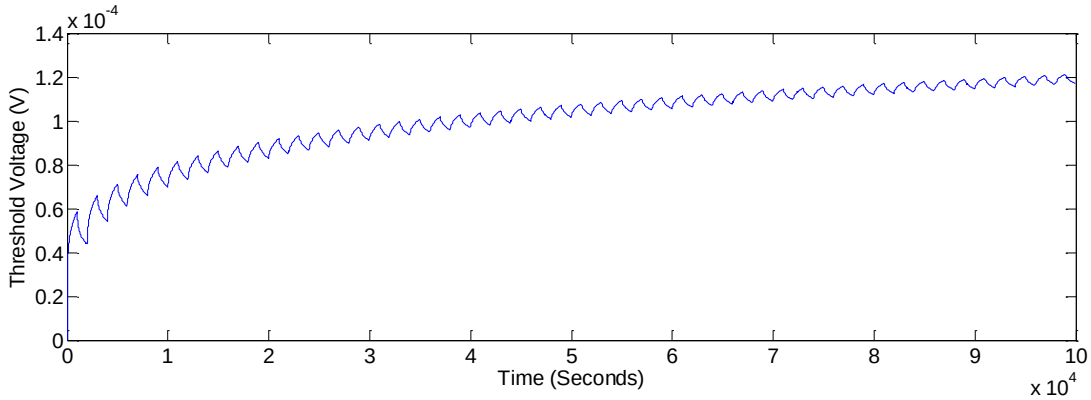


Fig. 4.36. Threshold voltage change due to NBTI considering aged and UV exposed CuO under dynamic stress

The percentage decrement in threshold voltage due to NBTI is calculated as follows,

$$v_{th} = 1 - \frac{v_{th} in\ Si-SiO_2}{v_{th} in\ Si-SiO_2\ with\ metal\ oxide\ incorporation} X100\% \quad (4.4)$$

Here, both DC and AC stress were evaluated for 10 years of ageing. Under DC stress, exploiting cured sample (4 days aged and 3 hours UV exposed) of TiO_2 results in a 70% increase in drive current and exploiting cured sample (4 days aged and 2 hours UV exposed) of CuO results in 98% increase in drive current. Table of comparison among three metal incorporations under DC stress is presented in Table 4.6.

Table 4.6

Comparison of drain current increment under NBTI effect and DC stress

Incorporation Type	**Drain Current Increment Under NBTI Effect**
ZnO incorporation	No increment in drain current
TiO_2 incorporation	70%
CuO incorporation	98%

Under AC or dynamic bias stress, exploiting cured sample (4 days aged and 3 hours UV exposed) of TiO_2 results in a 65% increase in drive current and exploiting cured sample (4 days aged and 2 hours UV exposed) of CuO results in 98% increase in drive current. Table of comparison among three metal incorporations under AC stress is presented in Table 4.7.

Table 4.7

Comparison of drain current increment under NBTI effect and AC stress

Incorporation Type	**Drain Current Increment Under NBTI Effect**
ZnO incorporation	No increment in drain current
TiO_2 incorporation	65%
CuO incorporation	98%

In Table 4.6 and 4.7, there is no increment in drain current for ZnO incorporation since under ZnO incorporation onto SiO_2, passivation of hydrogen induced traps are least (Shi et al., 2004) & (Shi et al., 2005). On the other hand, CuO incorporation causes maximum passivation of hydrogen induced traps and produces highest drain current increment among the three types of metal incorporation as per (Kim et al., 2003). This is also true for the case of TiO_2 incorporation (Göpel et al., 1983).

4.9 Summary

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This chapter projects the results obtained from the experiments. From the obtained experimental results, the compatible samples were chosen for RC delay and NBTI mitigation. For this, a statistical analysis is conducted by taking the whole set of population (data) into account. The verification of the compatible samples is performed using surface morphological analysis. In order to mitigate NBTI effect NBTI compatible sample is evaluated using a predictive model which complies with experimental data. Based on three different metal oxide incorporations, NBTI effect is evaluated and compared with Si-SiO_2 dielectric. The significant percentage decrement

in threshold voltage is reported and analysed for different types of metal oxide incorporation under DC and AC stress. Since, conventional R-D framework is unable to explain the correlation between NBTI and frequency, it is not possible to relate NBTI degradation with frequency in device level. Therefore, the device level R-D models cannot explain the compatible frequency range for lesser NBTI degradation. In this research, a circuit level technique is developed to find out the compatible frequency range under NBTI effect. In order to develop it, the device level data from the experiments are used into the targeted sample of CMOS circuit. As a whole, the mitigation results for NBTI and RC delay is shown here and a CMOS circuit level technique is developed to predict the compatible frequency range under NBTI effect.

CHAPTER 5 FUNCTIONAL IMPOSITION OF REDUCED NBTI & RC EFFECT IN CIRCUIT AND DEVICE

5.1 Introduction

After mitigating NBTI & RC effect and analyzing NBTI in circuit, this chapter will impose the obtained device and circuit level results to improve the accuracy of existing NBTI lifetime prediction models, RC circuit topologies and NBTI circuit level mitigation methods. The aim is to validate the compatibility of the obtained data by imposing it on other NBTI and RC based works. Having done the validation, an assessment will be shown between this research and other related works.

5.2 Compatibility Validation of the Results in RC Circuit Topology

Several research works have been employed so far to improve circuit level performance by mitigating delay as mentioned by (Krambeck, Lee, & Law, 1982), (Murabayashi et al., 1996), (Chu & Pulfrey, 1987), (Pfennings, Mol, Bastiaens, & Van Dijk, 1985) and (Belluomini et al., 2006). Fast circuit topologies are of utmost necessity in deep submicron technologies since the technology nodes are decreasing as feature size decreases. In circuit level, the delay is determined by the transition between high to low and low to high digital nodes. This transition can take place in both PMOS and NMOS transistors. According to (Akl, 2008), PMOS transistors are slower than that of NMOS. As a result the circuit techniques mentioned above concentrates more on PMOS in circuit level. Moreover, this thesis also takes PMOS into account in device level.

Circuit delay is dependent on many important factors. According to (Tsai, 2007), the following factors mainly contribute to the delay,

- Supply voltage

- Operating temperature
- Coupling of interconnected signals
- Circuit switching patterns

(Begur, 2011) has found difficulty in controlling supply voltage and temperature in CMOS circuit. Coupling of interconnected signals can be one of the ways but in a big CMOS system (e.g Microprocessor) this option cannot be effective due to repetitive parallel capacitance values. Circuit switching pattern can be changed through different ways but again its incompatibility with a large circuit (microprocessor) still persists as per (Begur, 2011).

CMOS circuit simulators such as HSPICE (Users' Manual, 1990) and Eldospice (Karam, Fikry, Haddara, & Ragai, 2001) have been in practice to analyze delay. However, the computation time for these simulators is long. Therefore, to analyze delay, existing literatures use model based approaches. One of the existing works by (Hashimoto, Yamaguchi, & ONODERA, 2008) & (Pant & Blaauw, 2005) suggested to control supply voltage in a specific range of time which would result in an equivalent voltage and would be employed to bias the circuitry. This means an external circuitry needs to be employed to control the time delay. But, this method can only be applicable in a low frequency system as per (Tsai, 2007). For GHz ranged radio frequency, transistor level capacitance must be reduced in order to make the system faster. And this research can solve this issue by mitigating delay.

There is another type of circuit level technique which replaces coupling capacitances with an equivalent ground capacitance as per (Alpert, Devgan, & Kashyap, 2001). However, according to (Vittal, Hui Chen, Marek-Sadowska, Wang, & Yang,

1999) this method is inaccurate in nanometer nodes due to high oxide capacitance of device. But, if the oxide capacitance can be reduced as per the proposed thesis, this method can play an extra role in mitigating delay.

If the device level delay is reduced then the circuit level delay will be reduced. For a targeted sample, the circuit technique obtained by (Begur, 2011) results in a reduced delay up to 4ps exploiting Si-SiO_2 interface. In terms of percentage calculation, (Tsai, 2007) showed a circuit delay which can be reduced up to 2.02% with respect to the normal case. Both of these cases and the other circuit level delay mitigation techniques mentioned earlier in this thesis can employ the mitigated device level data in order to further subside the delay. In these circuit topologies, pure SiO_2 is considered as the dielectric material where the dielectric constant happens to be 3.9. Under a reduced dynamic dielectric constant, the delay in circuit is supposed to be lesser than what mentioned in the previous circuit level delay mitigation techniques. Hence, the delay reduction in percentage in circuit level will be as per Equation 5.1:

$$\%, Delay\ Reduction\ in\ Circuit = 1 - \frac{Dielectric\ constant\ of\ the\ cured\ sample}{Dielectric\ constant\ used\ in\ circuit\ technique} X100 \quad (5.1)$$

The above equation (Equation 5.1) has been derived considering the ratio of the dielectric constant of the cured sample and the dielectric constant of SiO_2 which is used by the most circuit techniques. Based on the above calculation, the following table (Table 5.1) shows the comparison on delay reduction in circuit considering different types of cured devices

Table 5.1

Comparison of prior RC mitigation works considering percentile change in circuit

	Results for Different Device Level Works		
	Work	***Method***	***Reduction in delay***
Comparison of prior works	(Hong et al., 1997)	Surface modification with Trimethylchlorosilane	59%
	(Almaral-Sanchez et al., 2005)	Incorporating organic materials	53%
	(Cheong & Jasni, 2007)	Sampling based on precursor ageing	56%
	(Joshi & Mahajan, 2010)	Incorporating Methylmethacrylate (MMA)	56%
	(Joshi et al., 2010)	Incorporating carbon in the film due to MMA monomer	57%
	(Mhaisagar & Mahajan, 2012)	Incorporating Tween 80	63%
	This Work	UV exposure in precursor aged samples	69% with ZnO incorporation 73% with TiO_2 incorporation 99% with CuO incorporation

5.3 Compatibility Validation of the Device Level Results in R-D Based NBTI Predictive Models

The advantage of using R-D framework has been mentioned in **Chapter 2**. Due to its benefits, this research work is evaluated using an updated form of R-D framework. The updated R-D framework by (Kumar et al., 2009a) considered SiO_2 while developing NBTI predictive models. The dielectric constant of the transistor dielectric does not remain the same after incorporating high-K metal oxides. And this is one of the factors to be taken care in implementing predictive NBTI models. Employing pure SiO_2 does not justify full extent of accuracy of NBTI model since in sub-nanometer nodes high-K oxides are incorporated. Therefore, to ensure higher accuracy it is important to employ the accurate values of dielectric constant in the NBTI models. This research finds out a way to obtain an appropriate dielectric constant which can contribute to predict NBTI behaviour with higher accuracy. In this research, having incorporated cured samples of ZnO, TiO_2 and CuO onto SiO_2 dielectric, it is observed that the dielectric constant is changed for all samples. While predicting degradation due to NBTI through predictive NBTI models, the obtained values of dielectric constant can be used in order to accurately predict the degradation behaviour. Table 5.2 shows the difference in threshold voltage considering SiO_2 and considering high-K dielectric constant.

Table 5.2

Compatibility & accuracy of high-K in R-D framework

	V_{th} shift (10 years) without high-K incorporation according to (Kumar et al., 2009a)	**V_{th} shift (10 years) with ZnO incorporation according to this research**	**V_{th} shift (10 years) with TiO_2 incorporation according to this research**	**V_{th} shift (10 years) with CuO incorporation according to this research**
R-D Framework	0.11V for DC; 6.81mV for AC	0.25V for DC; 0.016V for AC	0.03V for DC; 2mV for AC	1.98 mV for DC; 0.12mV for AC

5.4 Compatibility Validation of the Device Level Results in Circuit Level Mitigation of NBTI

5.4.1 Case Study of Voltage Division Circuit Technique

As stated earlier, NBTI affects device performance and lifetime. In order to get rid of NBTI in circuit level, different mitigation techniques have been developed. Considering NBTI effect, circuit level methods have been implemented by (X. Chen et al., 2009). (X. Chen et al., 2009) used a lower supply voltage in early lifetime of the transistors. The technique implemented by (X. Chen et al., 2009) can mitigate 52.98% threshold voltage. It is useful in the early lifetime of the circuit, but degradation soon converges to long time framework as per (Chan et al., 2011). In order to get rid of NBTI induced degradation the work in this thesis can play an important role by mitigating the threshold voltage in device level.

5.4.2 Case Study of Adaptive Body Bias and Forward Body Bias Circuit Technique

NBTI causes incremental shift in threshold voltage which affects the performance of transistors in the circuit. Forward body bias (FBB) is employed to reduce threshold voltage as per (Narendra, Keshavarzi, Bloechel, Borkar, & De, 2003). Adaptive body bias (ABB) is a technique used to overcome the effect of NBTI by selectively using FBB. By adapting source voltage with ABB technique, (Tschanz, Narendra, Nair, & De, 2003) implemented a comparatively effective technique. By eliminating the leakage power, this technique reduces threshold voltage. This technique requires measuring supply voltage, threshold voltage, leakage power and delay calculation in circuit level. In order to reduce threshold voltage the proposed work in this research deals with less computations compared to the combined ABB and FBB technique. But, the decrement of threshold voltage is up to 14% only.

5.4.3 Validating Device Level Data with Circuit Techniques

Having mentioned about the above techniques, the following table (Table 5.3) shows the comparison of the NBTI data obtained from this work with the circuit techniques.

Table 5.3

Comparison of this research with NBTI circuit level works

Techniques	**V_{th} reduction level**
Voltage Division Circuit Technique	52.98%
ABB & FBB	14%
This Work	65%~70% for TiO_2 incorporation & 98% for CuO incorporation

5.5 Compatibility Validation of the Circuit Level Algorithm

The circuit algorithm depicted in **Chapter 3** is tested using MATLAB. Having tested the ageing of the circuit, the outcomes will be portrayed in this section. For simulation an oscillator circuit by (Razavi, 2011) was selected [APPENDIX K]. The selected oscillator is compatible up to frequency as high as 300GHz. The simulation was performed using HSPICE circuit simulator and Predictive Technology Model [APPENDIX H]. The simulation conditions are given in Table 5.4.

Table 5.4

Simulation conditions

Simulation Parameter	**Values**
Threshold voltage	As obtained from section 4.8.
Stress Type	Dynamic Stress at 0.7V
Maximum operable frequency	300 GHz
Technology Node	16nm
Oxide Thickness	$9.5X10^{-10}$ (m)

Here, oscillator is selected as a sample since it is widely used as a performance metric in digital circuit according to (W. Wang et al., 2007). (W. Wang et al., 2007) also showed that over time the frequency characteristics and gain shift due to NBTI get hampered. And that is why, this research takes oscillator as a sample. Though, the proposed circuit technique can be employed to any CMOS circuit.

After obtaining the change (due to ageing) in gain per frequency, frequency versus gain change was plotted for 10 years, 15 years and 20 years as per Fig. 5.1. Fig. 5.1 refers to a smaller microwave bandwidth (0~10GHz). From Fig. 5.1 a tabular datasheet was formed in Table 5.5 indicating the maximum and minimum gain change for different microwave frequency range and for different ageing time (e.g. 10years, 15 years and 20 years). As per this algorithm, from this tabular data the mean of the maximum and minimum values are calculated for 10 years, 15 years and 20 years respectively. Therefore, the summation of the maximum mean and minimum mean values under each frequency range are obtained. The highest value among all the summations refers to the most compatible frequency range for a circuit under NBTI effect since it refers to higher drain current. A similar approach is done for TiO_2 and CuO in Fig. 5.2 and Fig. 5.3 respectively, since the cured samples in device level result in higher drain current hence higher gain. From Fig. 5.1, Fig. 5.2 and Fig. 5.3; tabular datasheets are formed in Table 5.5, 5.6 and 5.7 indicating the maximum and minimum gain change for different microwave frequency range and for different ageing time (e.g. 10years, 15 years and 20 years). Cured sample of ZnO does not exhibit higher drain current compared to Si-SiO_2 dielectric as per the previous findings in this research. And that is why, ZnO is not taken into account for circuit level NBTI forecasting. However, this technique only forecasts the behaviour of gain change due to NBTI in any circuit so that designers can choose a NBTI compatible frequency range.

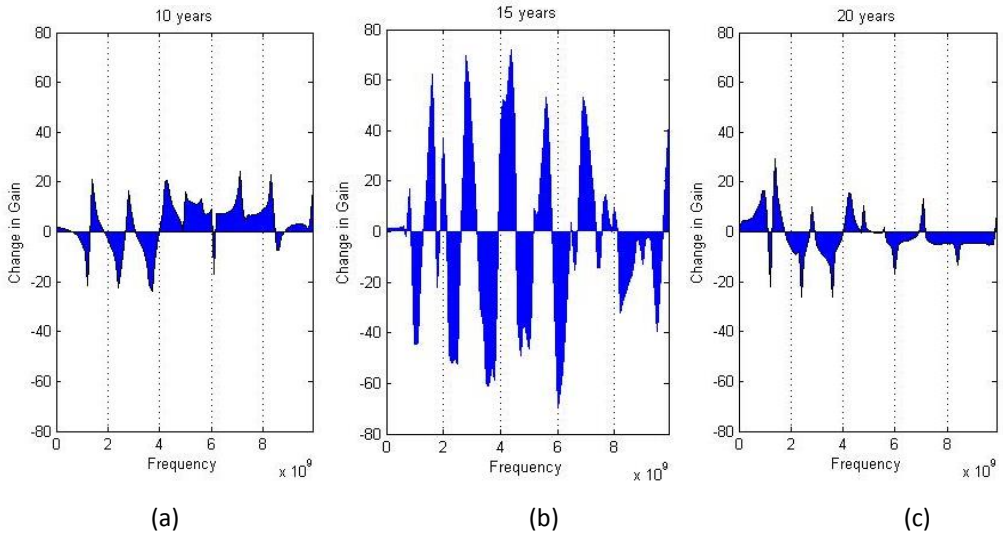

Fig. 5.1. Area plot for frequency vs. change in gain due to NBTI after (a)10 years (b)15 years (c) 20 years under 0~10GHz bandwidth for pure Si-SiO_2 interface

Table 5.5

Average shift in gain in Si-SiO2 based circuit

Frequency (GHz)	**10Years**	**15 Years**	**20 Years**	**Mean**
0 to 2	Max21.3	Max62.4	Max29.1	37.64
	Min 0.09	Min1.34	Min0.96	0.80
2> to 4	Max23.7	Max69.7	Max26.0	39.87
	Min0.58	Min0.65	Min0.82	0.68
4> to 6	Max20.7	Max71.9	Max16.7	36.47
	Min0.56	Min2.8	Min0.08	1.17
6> to 8	Max24.2	Max62.5	Max13.3	33.37
	Min4.73	Min0.33	Min0.57	1.88
8> to 10	Max22.9	Max44	Max13	26.8
	Min0.16	Min0.2	Min4.4	1.61

In device level, cured TiO_2 shows a high increment in drain current. Taking the drain current and threshold voltage for cured TiO_2 into account; frequency versus gain

change was plotted in Fig. 5.2, where lower microwave frequency (0~10GHz) bandwidth for 10, 15 and 20 years of ageing is observed. This plotting shows the case of oscillator circuit and depending on the circuit configuration the gain characteristics happen to be different since, transistor mapping exhibits different levels of drain current at different nodes. From Table 5.6, it is observed that 2 to 4 GHz frequency spectrum is the most compatible zone considering NBTI effect. This data complies with the previously obtained data from Si-SiO2 based circuit.

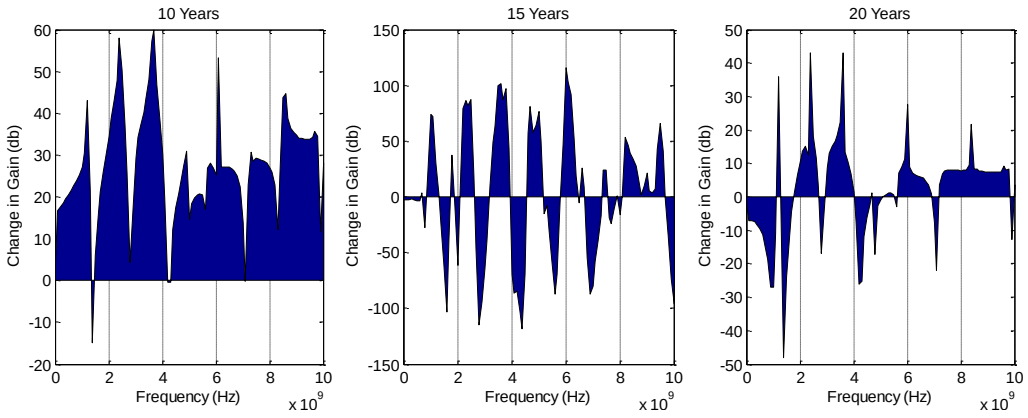

Fig. 5.2. Area plot for frequency vs. change in gain due to NBTI after (a)10 years (b)15 years (c) 20 years under 0~10GHz bandwidth for Si-SiO2-Cured TiO_2 interface

Table 5.6

Average shift in gain in Si-SiO2-Cured TiO_2 based transistors employed in circuit

Frequency (GHz)	**10Years**	**15 Years**	**20 Years**	**Mean**
0 to 2	Max43.0	Max103.0	Max48.0	64.67
	Min 4.1	Min2.2	Min1.6	2.63
2> to 4	Max59.9	Max115.2	Max43.0	72.7
	Min4.2	Min1.1	Min1.4	2.23
4> to 6	Max31.0	Max118.7	Max27.6	59.1
	Min0.38	Min4.8	Min0.13	1.77
6> to 8	Max53.3	Max103.1	Max22.0	59.47
	Min0.07	Min0.55	Min0.94	0.52
8> to 10	Max44.6	Max96.0	Max21.8	54.13
	Min11.8	Min0.33	Min3.4	5.18

In device level, cured sample of CuO showed a high increment in drain current. Due to high drain current, the gain is supposed to be high. Taking the drain current and threshold voltage for cured CuO; frequency versus gain change was plotted in Fig.5.3 for the targeted oscillator circuit (Razavi, 2011) [APPENDIX K]. Here, lower microwave frequency (0~10GHz) bandwidth for 10, 15 and 20 years of ageing is observed. This plotting shows the case of oscillator circuit and depending on the circuit configuration the gain characteristics happen to be different since, transistor mapping exhibits different levels of drain current at different nodes. From Table 5.7, it is observed that 2 to 4 GHz frequency spectrum is the most compatible zone considering

NBTI effect. This data complies with the previously obtained data from Si-SiO_2 based circuit and Si-SiO_2-Cured TiO_2 based circuit.

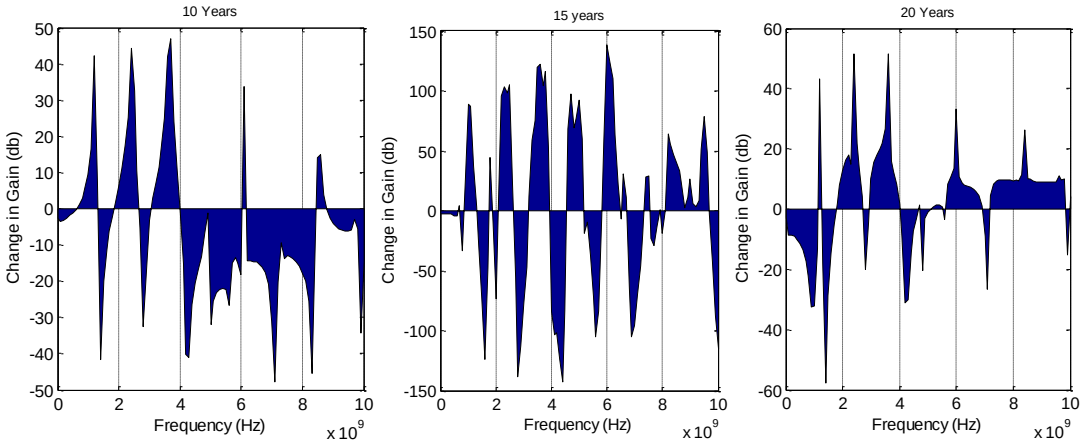

Fig. 5.3. Area plot for frequency vs. change in gain due to NBTI after (a)10 years (b)15 years (c) 20 years under 0~10GHz bandwidth for pure Si-SiO2-Cured CuO interface

Table 5.7

Average shift in gain in Si-SiO2-Cured CuO based transistors employed in circuit

Frequency (GHz)	**10Years**	**15 Years**	**20 Years**	**Mean**
0 to 2	Max42.2	Max88.5	Max43.2	57.96
	Min1.13	Min3.2	Min1.8	2.04
2> to 4	Max47.0	Max122.0	Max51.5	73.5
	Min2.9	Min21.4	Min8.3	10.86
4> to 6	Max0	Max138.7	Max33.1	57.3
	Min0	Min56.6	Min0.15	19.0
6> to 8	Max33.7	Max123.7	Max10.7	56.03
	Min0.	Min22.3	Min4.3	8.9
8> to 10	Max14.9	Max79	Max26.1	40.0
	Min14.1	Min2.4	Min4.1	6.87

The above mentioned technique has significance in order to corelate NBTI induced degradation and frequency, since device level R-D models (Jeppson & Svensson, 1977), (Alam et al., 2007) and (Kumar et al., 2009a) fail to interprete frequency with NBTI. Therefore, for understanding the frequency corelation with NBTI a new technique is developed in this research which finds out the compatible range of frequency band for a particular CMOS circuit.

5.6 Benchmarking for RC Results

The previous works related to reduction of dielectric constant mainly considered pure SiO_2 as the dielectric material. But in order to get rid of other types of defects like leakage current and boron penetration many high-K dielectric metal oxides are widely being used. The significance of using high-K has been described in this research. While exploiting high-K in a CMOS based system it is important to pay attention to the time delay since dielectric constant is directly proportional to time delay and high-K metal oxides manifests high dynamic dielectric constant. As per (Cheong & Jasni, 2007), dynamic dielectric constant is directly proportional to refractive index. To reduce the dynamic dielectric constant, refractive index was mitigated by ageing the precursors, exposing the samples under UV light for hours and by re-exposing the samples over a wide range of wavelength of UV light using PerkinElmer Filmetrics system. Hence, it can be said that in order to get the minimum RC delay, we must expose and age the dielectric samples. For delay reduction, other methods mainly considered low-K dielectrics. The method of (Hong et al., 1997) mainly focused on surface modification of low-K dielectrics. The other researchers incorporated organic materials, Methylmethacrylate, Carbon and Tween 80 (Almaral-Sanchez et al., 2005), (Joshi & Mahajan, 2010), (Joshi et al., 2010) & (Mhaisagar & Mahajan, 2012). In this work, UV process and precursor ageing has been combined with the sampling technique of

(Cheong & Jasni, 2007). (Cheong & Jasni, 2007) showed, different precursor ageing changes the refractive index and this fact was exploited in this thesis. But, as said earlier, for other reliability issues like reducing boron penetration and reducing leakage current, researchers now use high-K based materials inside the dielectric. By taking this factor into account ZnO, TiO_2 and CuO are incorporated onto the dielectric. The research was started with the preparation of sol-gel. Sol-gel was used so that ageing can be carried out for different time spans and this played a key role in lowering refractive index. One important point to be noted is that, sol-gel precursors are not aged for a prolonged period since surface roughness will be high as mentioned (Kucharczyk & Shigorin, 1989). The technique followed here is a combination of precursor ageing for 3 different days and UV exposure for 3 different hours. This technique of precursor sampling and UV exposure of the samples severely reduced the refractive index and permittivity compared to the previous works as per Table 5.8.

Table 5.8

Comparison of the Prior RC Mitigation Works

	Results for Different Works		
	Work	***Method***	***Refractive Index***
Comparison of prior works	(Hong et al., 1997)	Surface modification with Trimethylchlorosilane	1.59 in low-K
	(Almaral-Sanchez et al., 2005)	Incorporating organic materials	1.85 in low-K
	(Cheong & Jasni, 2007)	Sampling based on precursor ageing	1.72 in low-K
	(Joshi & Mahajan, 2010)	Incorporating Methylmethacrylate (MMA)	1.71 in low-K
	(Joshi et al., 2010)	Incorporating carbon in the film due to MMA monomer	1.7 in low-K

Comparison of prior works	Results for Different Works		
	Work	***Method***	***Refractive Index***
	(Mhaisagar & Mahajan, 2012)	Incorporating Tween 80	1.42 in low-K
	This Work	UV exposure in precursor aged samples	1.1924 with ZnO incorporation 1.0294 with TiO_2 incorporation 4e-08 with CuO incorporation

5.7 Benchmarking for NBTI Results

While mitigating NBTI degradation, circuit level mitigation techniques have already been discussed, but those techniques mostly depend on device level mitigation. Hence, it is more important to compare the device level mitigation data of this work only with the contemporary p-MOSFET device level data. (Yao Wang et al., 2012) demonstrated a FinFET based technique to mitigate NBTI. The authors used a separate gate to control threshold voltage. Employing an additional gate takes an extra area while implementing the overall circuit. In order to mitigate NBTI induced parameter degradation, (J. B. Yang et al., 2010) increased the drive current by 19%. (C.-H. Chen et al., 2004) increased the drive current up to 15% and for (H. S. Yang et al., 2004) it was 32%.

While exploiting the maximum refractive index for NBTI significant improvements in TiO_2 and CuO was noticed. In this case the evaluation was performed under both DC and AC stress for 10 years of ageing. Under DC stress, exploiting cured sample (4 days

aged and 3 hours UV exposed) of TiO2 results in a 70% increase in drive current and exploiting cured sample (4 days aged and 2 hours UV exposed) of CuO results in 98% increase in drive current. Under AC or dynamic bias stress, exploiting cured sample (4 days aged and 3 hours UV exposed) of TiO2 results in a 65% increase in drive current and exploiting cured sample (4 days aged and 2 hours UV exposed) of CuO results in 98% increase in drive current.

A predictive circuit methodology for NBTI is implemented in this thesis (Karim, Manzoor, & Soin, 2013). To implement this technique, the authors selected an RF oscillator on which ageing simulations were performed for 10, 15 and 20 years. Having performed ageing simulation by employing an updated form of reaction-diffusion (RD) framework inside Virtuoso Rel Xpert and HSPICE simulator, it is observed that the p-MOSFETs had shift in gain with respect to different radio frequencies. The algorithm is based on the device level data obtained from this research. Previous circuit level techniques did not consider gain transformation and radio frequency behavior into account. Moreover, unlike previous techniques this technique considers the incorporation of high-K dielectric.

5.8 Summary

The different possible aspects of the proposed research have been delineated in this chapter. The RC mitigation technique can be employed in different circuit level techniques. At the same time the dielectric properties obtained from NBTI mitigation method can be used in RD framework to accurately predict the device behaviour after certain period of device lifetime. In contrast to these, the dielectric property can be employed in circuit level techniques to further improve the reliability of CMOS systems.

Moreover, compared to the recent works, the proposed RC delay shows better performance despite of the incorporation of high-K metal oxides. Similarly compared to the major contemporary device level works, the proposed NBTI mitigation technique shows significant improvement which comprise of both DC and AC biasing mode.

CHAPTER 6 CONCLUSIONS & FUTURE WORKS

6.1 Conclusions

In order to subside RC delay, the dielectric constant in CMOS is subsided considering the incorporation of different types of high-K metal oxides. For ZnO, results show that the smallest obtainable dynamic dielectric constant is 1.1925. For TiO_2, Results show that the smallest obtainable dynamic dielectric constant is 1.0294. And, for CuO, Results show that the smallest obtainable dynamic dielectric constant is 4e-8. These obtained results on RC delay are validated over previous literatures. The percentile change in delay is extracted for the contemporary works on RC delay and hence, the results from this thesis are validated over the previous data.

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In order to minimize NBTI effect, highest dynamic dielectric constant was exploited from the samples to obtain a low threshold voltage and high drain current. While exploiting the maximum refractive index for NBTI significant improvements were found in TiO_2 and CuO. Under DC stress, TiO_2 results in 70% increase in drive current and CuO results in 98% increase in drive current. Under AC or dynamic bias stress, TiO_2 results in a 65% increase in drive current and CuO results in 98% increase in drive current. The NBTI results are validated over the contemporary device level works. Along with device level, the obtained data are validated over different circuit techniques under NBTI effect.

The reduced threshold voltage under NBTI effect is exploited to develop a circuit level technique. The developed technique predicts the most compatible frequency range for CMOS circuit under NBTI effect. Having developed the circuit level technique, the

technique is validated with different metal incorporations and without metal incorporation (with pure SiO_2). The validated technique is able to track the compatible frequency range for targeted CMOS circuit. An oscillator is selected as a target circuit to elaborate the NBTI circuit level algorithm. The result shows that 2~4 GHz frequency spectrum as the most compatible frequency range for the oscillator circuit under NBTI effect since this range obtains highest gain for pure SiO_2, TiO_2 incorporated SiO_2 and CuO incorporated SiO_2. TiO_2 incorporation shows 45% increment in gain over pure SiO_2. And CuO incorporation shows 46% increment in gain over pure SiO_2. This frequency range was found by employing refractive index yielded dielectric constant into the developed algorithm.

6.2 Future works on NBTI & RC Mitigation

6.2.1 Examining Other High-K Materials

In this research, ZnO, TiO_2 and CuO have been examined. HfO_2 and ZrO_2 are two of those high-K metal oxides which are widely incorporated onto transistor's dielectric (S Zafar et al., 2006) & (Cho, Kaczer, Kauerauf, Ragnarsson, & Groeseneken, 2013). It can be a research question- "how ageing and UV exposing affect NBTI and delay through the incorporation of HfO_2 and ZrO_2?"

6.2.2 Examining the Incorporation of Nitrogen Yielded Species

The use of nitrogen driven species helps to get rid of leakage current (Guo & Ma, 1998). But these materials enhance NBTI. It is yet to be examined whether aged nitrogen precursor can improve the condition of NBTI and RC delay.

6.2.3 Mitigation of HCI & PBTI Using Similar Method

Since HCI is dependent on threshold voltage (Takeda, Shimizu, et al., 1983), this research can be employed to mitigate HCI effect. Similarly, PBTI is a threshold voltage dependent defect (Zhang & Eccleston, 1998) and incorporation of aged high-K metal oxide can minimize this issue.

6.2.4 Use of Ferroelectric Materials

Ferroelectric materials are recently proposed for using in CMOS architecture by (Salahuddin & Datta, 2008). As per (Salahuddin & Datta, 2008), incorporating ferroelectric materials improve the subthreshold properties of transistors by reducing the sub-threshold slope. The aim can be- to analyze whether aged precursors of ferroelectric materials can improve reliability or not.

6.2.5 Analysis on FinFET

Due to the growing demand of FinFET, its reliability is a concern for the researchers (Yao Wang et al., 2012). The implemented mitigation results can be utilized in a FinFET NBTI model to minimize NBTI effect over time.

6.2.6 Exploring Atomic Layer Deposition

Apart from spin coating there are other methods of depositing metal oxides onto Si-SiO_2 surface. Atomic layer deposition (ALD) is one of these methods. ALD is a

method of applying films onto substrate with atomic precision. The biggest constraints one may find are slowness and high expense.

6.2.7 Investigating Si<100> and Si<111>

The orientation of atoms in Si<100> and Si<111> are different than Si<110>. These exhibit a different amount of transconductance degradation due to NBTI (Momose et al., 2003). As a result the drain current and threshold voltage will be different than Si<110>. And supposedly, the degradation in Si<100> and Si<111> is lesser than Si<110> as stated earlier. Hence, hypothetically it is assumed Si<100> and Si<111> will exhibit better result from the context of NBTI. In order to test this hypothesis, this research can be re-experimented with Si<100> and Si<111>.

6.2.8 Investigating Quantum Tunneling

The NBTI predictive models by (Jeppson & Svensson, 1977), (Alam et al., 2007) and (Kumar et al., 2009a) do not consider the following issues:

- Quantum mechanical tunneling of holes from gate to bulk
- Quantum mechanical tunneling of holes from the source to drain, and from drain to the bulk.
- Control of the density and location of dopant atoms in the MOSFET channel

Having taken the above points into account a model needs to be implemented so that NBTI can be evaluated more precisely in lower technology nodes.

6.3 Epilogue

This PhD research was initiated to mitigate NBTI effect and RC delay. Now a days, defect analysis and speed involve many evolving theories. These contribute to the development of power electronics, RF devices, and renewable energy sources. While making these developments, accurate treatment of materials is of utmost necessity in order to attain the best possible result. The method of this research significantly increases the operational speed by obtaining a low value of dielectric constant. At the same time it shows a method to obtain a high drain current to minimize NBTI effect. CMOS defect mitigation and speed enhancement using high-K metal oxides play an important role in this research. Hopefully, the use of other high-K metal oxide would enable one to analyze NBTI, HCI and PBTI in future.

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APPENDIX A: LIST OF PUBLICATIONS

Journals

[1] **N. M. Karim**, Sadia Manzoor, Norhayati Soin: *Statistical forecasting algorithm on circuit level gain transformation due to negative bias temperature instability for the microwave frequency spectrum*. Journal of Computational Electronics, Springer 08/2013; 12(2). **(Cited: Once) (Journal Impact Factor: 1.372)**

[2] **Nissar Mohammad Karim**, Sadia Manzoor, Norhayati Soin: *Unification of Contemporary Negative Bias Temperature Instability Models for p-MOSFET Energy Degradation*. Renewable and Sustainable Energy Reviews, Elsevier 10/2013; 26:776-780. **(Journal Impact Factor: 5.510)**

[3] **Nissar Mohammad Karim**, Norhayati Soin, Fatema Banitorfian, Sadia Manzoor: *Analysis from the Perspective of Gate Material under the Effect of Negative Bias Temperature Instability*. Informacije Midem -Ljubljana- 01/2012; 42(2):95-97. **(Cited: Once) (Journal Impact Factor: 0.369)**

[4] **Nissar Mohammad Karim**, Norhayati Soin, Sadia Manzoor, Soon Foo Yew, Mohamed Mounir: *Prediction of energy change due to hot carrier injection in nano-structured CMOS system: Perspective of an envelope detector*. Microelectronic Engineering, Elsevier 11/2013; 111:256-260. **(Cited: Once) (Journal Impact Factor: 1.338)**

[5] Siti Amaniah Mohd Chachuli, Puteri Nor Aznie Fasyar, Norhayati Soin, **Nissar Mohammad Karim**, Norbayah Yusop, Pareto ANOVA analysis for CMOS 0.18µm two-stage Op-amp, Materials Science in Semiconductor Processing, Elsevier, Volume 24, August 2014, Pages 9-14. **(Journal Impact Factor: 1.761)**

[6] Sadia Manzoor, **Nissar Mohammad Karim**, Norhayati Soin: *Analyzing p-MOSFET Lifetime by Employing R-D Model & MOS Device Theory*. Applied Mechanics and Materials 11/2012;

[7] H. Hussin, N. Soin, **N. M. Karim**, S. F. Wan Muhamad Hatta: *On the effects of NBTI degradation in p-MOSFET devices*. Physica B: Condensed Matter, Elsevier 08/2012**. (Cited: 2 times) (Journal Impact Factor: 1.276)**

[8] Nissar Mohammad Karim, Norhayati Soin, Christopher Fearday, Uda Hashim, and MohamadAzman Bin Abu Hassan : *The Effect of UV Treatment Time and Sol-Gel Aging on Delay Mitigation in a TiO_2 Incorporated CMOS Gate Dielectric*. The Scientific World Journal**. (In Pipeline) (Journal Impact Factor: 1.133)**

[9] Nissar Mohammad Karim, Norhayati Soin : *Mitigation of threshold voltage increment due to negative bias temperature instability by exploiting sol-gel derived TiO2 incorporation*. IET Circuits, Devices & Systems**. (In Pipeline) (Journal Impact Factor: 0.912)**

Conferences

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[2] **Nissar Mohammad Karim**, Norhayati Soin, Characterizing of CuO Incorporated CMOS Dielectric for Fast Switching System, 2015 International Conference on Advanced Materials (ICAM), Accepted and presented on January 2015 in Jeddah, Saudi Arabia.

APPENDIX B: MAGNETIC STIRRER

The following figure shows a magnetic stirrer with nobs to control stirring speed, temperature. A magnetic bar is immersed into the liquid to spin the motion of the liquid.

APPENDIX C: OXIDATION FURNACE

The following figure shows a thermal oxidation furnace. Thermal oxidation furnace is a reactive growth processor to grow silicon oxide on silicon surface. This system is comprised of three-zone atmosphere pressure furnace tube. The furnace has three modules- wafers input module, furnace/process tube module, and gas control module. Oxidation furnace tube has its own microprocessor to display panel and keypad are located on the front side of the wafer load/unload module.

APPENDIX D: SPIN COATER

The following figure shows WS-400-6NPPB Laurell spin coater. It contains a plane to keep the sample. Once the vacuum connected with it is turned on the sample gets fixed with the plane. The control panel attached with the system receives command on the basis of speed.

APPENDIX E: UV EXPOSURE CABINET

The following figure shows UV laminar cabinet for adhesive UV exposure. It is protected with polypropylene so that the UV ray cannot harm the user. While placing the samples inside it fluorescent light is turned on. Having turned the samples in, user needs to turn on the UV light by covering the cabinet with polypropylene glass.

APPENDIX F: REFRACTOMETER

The following figure shows Perkin Elmer Lambda 35 refractometer. It can measure the refractive index, transmittance, absorbance of reflectance of liquid and solid samples. The measurement is done in a closed chamber so that light from any other source cannot interfere. The measurement result is shown in the Computer connected with it. The hardware needs a software (WinLab) to process and show the measured data.

APPENDIX G: MATLAB CODE FOR NBTI MODEL

DC Bias Coding:

```
clear all

clc

% CONSTANTS

dox=0.1*(10^-8); % Oxide thickness in (cm)

Dox= 4^-17; % Diffusion coefficient in the oxide. (cm2.s-1)

Dp=0.25*Dox; % Diffusion coefficient in the poly. (cm2.s-1)

kf=4.66;          % Forward rate constant, Si–H bond-breaking rate.(s-1)

N0=5*10^12; % Si–H bonds Maximum density, initial bond density before stress. (cm-2)

kH=1.4*10^-3; % Reverse rate constant, Si–H bond-annealing rate.(cm3.s-1)

kr=4.48*10^-9; % Reverse rate constant, Si–H bond-annealing rate.(cm3.s-1)

e0=8.854*10^-14; % vacuum permittivity. ( F/cm)

cox= 3.9*e0/dox; % Oxide capacitance (F)

q= 1.602*10^-19; % Elementary  charge

kit=( kf * N0 * (sqrt(kH)) / kr )^(2/3);

t = 3*(10^8):  (10^4)  : 3.1*(10^8); %3.000*10^8; % Time frame

t1= ( ((dox)^2)/ (2*Dox)); % Time required for hydrogen to diffuse to oxygen/poly interface

len = length(t);

%

for a= 1:len

 f(a)= (( Dox*sqrt(2*Dp*(t(a)-t1)) )/( Dox*sqrt(2*Dp*(t(a)- t1))+Dp*dox ) );

  if ( t(a) <= t1)

 Nit(a)= kit *( (2*Dox*t(a))^(1/6)) ; % Density of interface traps. (cm-2)

else

Nit(a) = kit * ( (dox*(1+f(a))) + ( sqrt(2*Dp*(t(a)-t1)) *f(a) ) )^(1/3);
```

```
end;
end;
vth= q * Nit/cox;
figure(1)
plot(t, Nit) % printing the Nit in Figure 1
figure(2)
plot(t, vth) % printing the Vth wave in Figure 2
```

Dynamic Bias Coding:

```
clear all
clc
dox=0.016*(10^-7);
Dox= 4^-17;
Dp=0.25*Dox;
kf=4.66;
N0=5*10^12;
kH=1.4*10^-3;
kr=4.48*10^-9;
e0=8.854*10^-14;
cox= 223.80*e0/dox;
q= 3.9*10^-19;
kit=( kf * N0 * (sqrt(kH)) / kr )^(2/3);
tx=1000;
T=10^5;
t = 0:  (10^1)  : (tx);
tt =  0:  (10^1)  : (T);
lent = length(t);
lentt = length(tt);
```

```
t= t(1:lent-1);
tt= tt(1:lentt-1);
t1= ( ((dox)^2)/ (2*Dox));
t2= 0.6351*( (tx)^0.6439 )* ( (dox*(10^7))^1.6641 );
%
NitT=0;
NT=0;
for n= 1 : 2 : (T/tx)
 waitbar(n/(T/tx));
 a=1;
 b=1;
%stress
%
for a= 1:lent-1
 %  waitbar(a/(lent-1));
 if ( t(a) <= t1)
 Nit(a)= kit *( (NitT/kit)^6 + (2*Dox*t(a)))^(1/6) ;
else
 Nit(a)= kit * ( sqrt((NitT/kit)^6+ (2*dox)^2)  + sqrt(2*Dp*(t(a)-t1)) )^(1/3) ;
 end;
NT= cat(2,NT,Nit(a));
end;
NitT=Nit(a);
%
%relax
for b= 1:lent-1
%  waitbar(b/(lent-1));
if ( t(b) <= t2)
```

```
 z1=(0.5843*(t(b)/tx))^0.0897;

 h1(b)= ( sqrt(z1*2*Dox*t(b))  ) / ( 2*dox - sqrt(2*Dox*t(b)) + sqrt(2*Dp*(t(b)+n*tx))
);

 Nit(b)= NitT/ (1+h1(b));

 NitTs=Nit(b);

else

 h2(b)= sqrt((0.125*(t(b)-t2))/(t(b)+(n*tx)));

 Nit(b)= NitTs *(1-h2(b));

 end;

NT= cat(2,NT,Nit(b));

end;

NitT=Nit(b);

%

end;

lenx= length(NT);

NT = NT(2:lenx);

vth= q * NT/cox;

figure(1)

plot(tt,NT) % printing the sine wave in Figure 1

figure(2)

plot(tt,vth) % printing the sine wave in Figure 1
```

APPENDIX H: SPICE CODE

```
* PTM High Performance 16nm Metal Gate / High-K / Strained-Si
* nominal Vdd = 0.7V

.model  nmos  nmos  level = 54

+version = 4.0            binunit = 1             paramchk= 1
mobmod  = 0
+capmod  = 2              igcmod  = 1             igbmod  = 1
geomod  = 1
+diomod  = 1              rdsmod  = 0             rbodymod= 1
rgatemod= 1
+permod  = 1              acnqsmod= 0             trnqsmod= 0

+tnom    = 27             toxe    = 9.5e-010      toxp    = 7e-010
toxm    = 9.5e-010
+dtox    = 2.5e-010       epsrox  = 3.9           wint    = 5e-009
lint    = 1.45e-009
+ll      = 0              wl      = 0             lln     = 1
wln     = 1
+lw      = 0              ww      = 0             lwn     = 1
wwn     = 1
+lwl     = 0              wwl     = 0             xpart   = 0
toxref  = 9.5e-010
+xl       = -6.5e-9

+vth0    = 0.47965        k1      = 0.4           k2      = 0
k3      = 0
+k3b     = 0              w0      = 2.5e-006      dvt0    = 1
dvt1    = 2
+dvt2    = 0              dvt0w   = 0             dvt1w   = 0
dvt2w   = 0
+dsub    = 0.1            minv    = 0.05          voffl   = 0
dvtp0   = 1e-011
+dvtp1   = 0.1            lpe0    = 0             lpeb    = 0
xj      = 5e-009
+ngate   = 1e+023         ndep    = 7e+018        nsd     = 2e+020
phin    = 0
+cdsc    = 0              cdscb   = 0             cdscd   = 0
cit     = 0
+voff    = -0.13          nfactor = 2.3           eta0    = 0.0032
etab    = 0
+vfb     = -0.55          u0      = 0.03          ua      = 6e-010
ub      = 1.2e-018
+uc      = 0              vsat    = 290000        a0      = 1
ags     = 0
+a1      = 0              a2      = 1             b0      = 0
b1      = 0
+keta    = 0.04           dwg     = 0             dwb     = 0
pclm    = 0.02
+pdiblc1 = 0.001          pdiblc2 = 0.001         pdiblcb = -0.005
drout   = 0.5
+pvag    = 1e-020         delta   = 0.01          pscbe1  =
8.14e+008       pscbe2  = 1e-007
+fprout  = 0.2            pdits   = 0.01          pditsd  = 0.23
pditsl  = 2300000
+rsh     = 5              rdsw    = 140           rsw     = 75
rdw     = 75
+rdswmin = 0              rdwmin  = 0             rswmin  = 0
prwg    = 0
+prwb    = 0              wr      = 1             alpha0  = 0.074
alpha1  = 0.005
```

```
+beta0   = 30              agidl   = 0.0002          bgidl   =
2.1e+009        cgidl   = 0.0002
+egidl   = 0.8             aigbacc = 0.012           bigbacc = 0.0028
cigbacc = 0.002
+nigbacc = 1               aigbinv = 0.014           bigbinv = 0.004
cigbinv = 0.004
+eigbinv = 1.1             nigbinv = 3               aigc    = 0.0213
bigc    = 0.0025889
+cigc    = 0.002           aigsd   = 0.0213          bigsd   =
0.0025889       cigsd   = 0.002
+nigc    = 1               poxedge = 1               pigcd   = 1
ntox    = 1
+xrcrg1  = 12              xrcrg2  = 5

+cgso    = 5e-011          cgdo    = 5e-011          cgbo    = 2.56e-
011       cgdl    = 2.653e-010
+cgsl    = 2.653e-010      ckappas = 0.03            ckappad = 0.03
acde    = 1
+moin    = 15              noff    = 0.9             voffcv  = 0.02

+kt1     = -0.11           kt1l    = 0               kt2     = 0.022
ute     = -1.5
+ua1     = 4.31e-009       ub1     = 7.61e-018       uc1     = -5.6e-
011       prt     = 0
+at      = 33000

+fnoimod = 1               tnoimod = 0

+jss     = 0.0001          jsws    = 1e-011          jswgs   = 1e-010
njs     = 1
+ijthsfwd= 0.01            ijthsrev= 0.001           bvs     = 10
xjbvs   = 1
+jsd     = 0.0001          jswd    = 1e-011          jswgd   = 1e-010
njd     = 1
+ijthdfwd= 0.01            ijthdrev= 0.001           bvd     = 10
xjbvd   = 1
+pbs     = 1               cjs     = 0.0005          mjs     = 0.5
pbsws   = 1
+cjsws   = 5e-010          mjsws   = 0.33            pbswgs  = 1
cjswgs  = 3e-010
+mjswgs  = 0.33            pbd     = 1               cjd     = 0.0005
mjd     = 0.5
+pbswd   = 1               cjswd   = 5e-010          mjswd   = 0.33
pbswgd  = 1
+cjswgd  = 5e-010          mjswgd  = 0.33            tpb     = 0.005
tcj     = 0.001
+tpbsw   = 0.005           tcjsw   = 0.001           tpbswg  = 0.005
tcjswg  = 0.001
+xtis    = 3               xtid    = 3

+dmcg    = 0               dmci    = 0               dmdg    = 0
dmcgt   = 0
+dwj     = 0               xgw     = 0               xgl     = 0

+rshg    = 0.4             gbmin   = 1e-010          rbpb    = 5
rbpd    = 15
+rbps    = 15              rbdb    = 15              rbsb    = 15
ngcon   = 1


.model  pmos  pmos  level = 54

+version = 4.0             binunit = 1               paramchk= 1
mobmod  = 0
```

```
+capmod  = 2               igcmod  = 1               igbmod  = 1
geomod  = 1
+diomod  = 1               rdsmod  = 0               rbodymod= 1
rgatemod= 1
+permod  = 1               acnqsmod= 0               trnqsmod= 0

+tnom    = 27              toxe    = 1e-009          toxp    = 7e-010
toxm    = 1e-009
+dtox    = 3e-010          epsrox  = 3.9             wint    = 5e-009
lint    = 1.45e-009
+ll      = 0               wl      = 0               lln     = 1
wln     = 1
+lw      = 0               ww      = 0               lwn     = 1
wwn     = 1
+lwl     = 0               wwl     = 0               xpart   = 0
toxref  = 1e-009
+xl        = -6.5e-9

+vth0    = -0.43121        k1      = 0.4             k2      = -0.01
k3      = 0
+k3b     = 0               w0      = 2.5e-006        dvt0    = 1
dvt1    = 2
+dvt2    = -0.032          dvt0w   = 0               dvt1w   = 0
dvt2w   = 0
+dsub    = 0.1             minv    = 0.05            voffl   = 0
dvtp0   = 1e-011
+dvtp1   = 0.05            lpe0    = 0               lpeb    = 0
xj      = 5e-009
+ngate   = 1e+023          ndep    = 5.5e+018        nsd     = 2e+020
phin    = 0
+cdsc    = 0               cdscb   = 0               cdscd   = 0
cit     = 0
+voff    = -0.126          nfactor = 2.1             eta0    = 0.0032
etab    = 0
+vfb     = 0.55            u0      = 0.006           ua      = 2e-009
ub      = 5e-019
+uc      = 0               vsat    = 250000          a0      = 1
ags     = 1e-020
+a1      = 0               a2      = 1               b0      = 0
b1      = 0
+keta    = -0.047          dwg     = 0               dwb     = 0
pclm    = 0.12
+pdiblc1 = 0.001           pdiblc2 = 0.001           pdiblcb = 3.4e-
008        drout   = 0.56
+pvag    = 1e-020          delta   = 0.01            pscbe1  =
1.2e+009        pscbe2  = 8.0472e-007
+fprout  = 0.2             pdits   = 0.08            pditsd  = 0.23
pditsl  = 2300000
+rsh     = 5               rdsw    = 140             rsw     = 70
rdw     = 70
+rdswmin = 0               rdwmin  = 0               rswmin  = 0
prwg    = 0
+prwb    = 0               wr      = 1               alpha0  = 0.074
alpha1  = 0.005
+beta0   = 30              agidl   = 0.0002          bgidl   =
2.1e+009        cgidl   = 0.0002
+egidl   = 0.8             aigbacc = 0.012           bigbacc = 0.0028
cigbacc = 0.002
+nigbacc = 1               aigbinv = 0.014           bigbinv = 0.004
cigbinv = 0.004
+eigbinv = 1.1             nigbinv = 3               aigc    = 0.0213
bigc    = 0.0025889
+cigc    = 0.002           aigsd   = 0.0213          bigsd   =
0.0025889       cigsd   = 0.002
```

```
+nigc    = 1              poxedge = 1              pigcd   = 1
ntox    = 1
+xrcrg1  = 12             xrcrg2  = 5

+cgso    = 5e-011         cgdo    = 5e-011         cgbo    = 2.56e-
011       cgdl    = 2.653e-010
+cgsl    = 2.653e-010     ckappas = 0.03           ckappad = 0.03
acde    = 1
+moin    = 15             noff    = 0.9            voffcv  = 0.02

+kt1     = -0.11          kt1l    = 0              kt2     = 0.022
ute     = -1.5
+ua1     = 4.31e-009      ub1     = 7.61e-018      uc1     = -5.6e-
011       prt     = 0
+at      = 33000

+fnoimod = 1              tnoimod = 0

+jss     = 0.0001         jsws    = 1e-011         jswgs   = 1e-010
njs     = 1
+ijthsfwd= 0.01           ijthsrev= 0.001          bvs     = 10
xjbvs   = 1
+jsd     = 0.0001         jswd    = 1e-011         jswgd   = 1e-010
njd     = 1
+ijthdfwd= 0.01           ijthdrev= 0.001          bvd     = 10
xjbvd   = 1
+pbs     = 1              cjs     = 0.0005         mjs     = 0.5
pbsws   = 1
+cjsws   = 5e-010         mjsws   = 0.33           pbswgs  = 1
cjswgs  = 3e-010
+mjswgs  = 0.33           pbd     = 1              cjd     = 0.0005
mjd     = 0.5
+pbswd   = 1              cjswd   = 5e-010         mjswd   = 0.33
pbswgd  = 1
+cjswgd  = 5e-010         mjswgd  = 0.33           tpb     = 0.005
tcj     = 0.001
+tpbsw   = 0.005          tcjsw   = 0.001          tpbswg  = 0.005
tcjswg  = 0.001
+xtis    = 3              xtid    = 3

+dmcg    = 0              dmci    = 0              dmdg    = 0
dmcgt   = 0
+dwj     = 0              xgw     = 0              xgl     = 0

+rshg    = 0.4            gbmin   = 1e-010         rbpb    = 5
rbpd    = 15
+rbps    = 15             rbdb    = 15             rbsb    = 15
ngcon   = 1
```

APPENDIX I: SCANNING ELECTRON MICROSCOPY

Scanning Electron Microscopy (SEM) used in this project is by FEI and modelled as Verios; which is the second generation, extreme high resolution SEM. It provides sub-nanometer resolution from 1 to 30 kV and enhanced contrast needed for precise measurements on MEMS, Microfabrication and materials science applications.

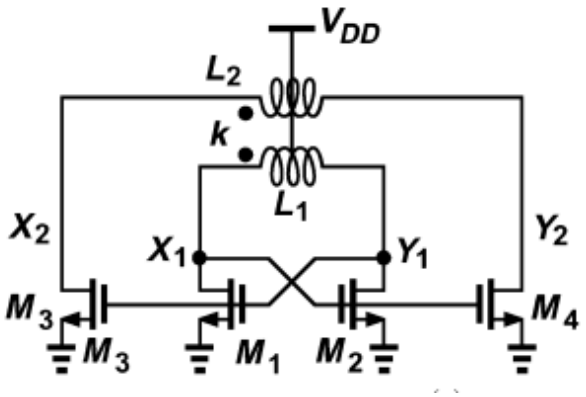
APPENDIX J: EDXMA

EDXMA or EDS is a technique to do elemental analysis. X-Max Silicon Drift EDS Detector is used in this project which offers over TEN times the solid angle of conventional EDS detectors. It has the following features.

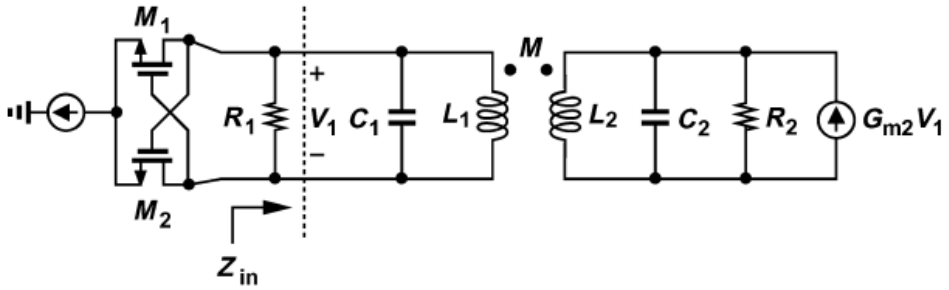
- Up to 80mm^2 active area
- Count rates > 500,000 cps
- Throughput > 200,000 cps
- Standard tube diameter (no larger than that of a 10mm^2 SDD detector)

APPENDIX K: CMOS SCHEMATIC

Schematic (a) shows the circuit diagram for an oscillator used by(Razavi, 2011). (b) shows the equivalent simplified model of the circuit.



(a)



(b)