DESIGN AND IMPLEMENTATION OF A NEW MULTILEVEL INVERTER TOPOLOGY WITH SHARED POWER SWITCHES

JAFFERI BIN JAMALUDIN

FACULTY OF ENGINEERING
UNIVERSITY OF MALAYA
KUALA LUMPUR

2014

DESIGN AND IMPLEMENTATION OF A NEW MULTILEVEL INVERTER TOPOLOGY WITH SHARED POWER SWITCHES

JAFFERI BIN JAMALUDIN

THESIS SUBMITTED IN FULFILLMENT OF THE REQUIREMENT FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

FACULTY OF ENGINEERING
UNIVERSITY OF MALAYA
KUALA LUMPUR

2014

UNIVERSITI MALAYA

ORIGINAL LITERARY WORK DECLARATION

Name of Candidate: **Jafferi bin Jamaludin** (I.C/Passport No: [redacted])

Registration/Matric No: **KHA090053**

Name of Degree: **PhD**

Title of Project Paper/Research Report/Dissertation/Thesis ("this Work"):

Design and implementation of a new multilevel inverter topology with shared power switches

Field of Study:

I do solemnly and sincerely declare that:

(1) I am the sole author/writer of this Work;
(2) This Work is original;
(3) Any use of any work in which copyright exists was done by way of fair dealing and for permitted purposes and any excerpt or extract from, or reference to or reproduction of any copyright work has been disclosed expressly and sufficiently and the title of the Work and its authorship have been acknowledged in this Work;
(4) I do not have any actual knowledge nor do I ought reasonably to know that the making of this work constitutes an infringement of any copyright work;
(5) I hereby assign all and every rights in the copyright to this Work to the University of Malaya ("UM"), who henceforth shall be owner of the copyright in this Work and that any reproduction or use in any form or by any means whatsoever is prohibited without the written consent of UM having been first had and obtained;
(6) I am fully aware that if in the course of making this Work I have infringed any copyright whether intentionally or otherwise, I may be subject to legal action or any other action as may be determined by UM.

[redacted]

Candidate's Signature

Date 8 DECEMBER 2014

Subscribed and solemnly declared before,

[redacted]

Witness's Signature

Date 8/12/14

Name: Dr. Siti Rohani Sheikh Raihan
Designation: Lecturer
UMPEDAC, University of Malaya

ABSTRACT

The increasing attention drawn on multilevel inverters particularly in medium and high power applications has led to the enhanced efforts and initiatives to improve the features and competitiveness of multilevel inverters. This research is part of such efforts and initiatives, with the intended improvement is targeted at reducing circuit complexity and cost. For this purpose, a new three-phase multilevel inverter topology based on switch-sharing approach has been proposed in this research. The topology is made up of three modules. Combination of Module 1 and Module 2 produces an arrangement of the conventional full-bridge circuit with three bidirectional switches. Module 3 comprises a string of bidirectional switches connected to DC sources. Here, the switches operate in the optimized mode. In this way, the operation of each switch is divided among the three phases. By adding one bidirectional switch in Module 3 of *m*-level structure, the (*m* + 1)-level structure is formed. A new modulation scheme based on space vector concept with virtual vectors utilization has been developed for this topology. By using the virtual vectors, the difficulty in decomposing the reference vector in certain zones as a result of the elimination of several voltage vectors, can be effectively overcome. A proportional integral (PI) controller equipped with a new automatic tuning has been developed to deal with varying load conditions. A detailed study of the proposed four-level and five-level inverters has been described. The performance of the proposed inverter is analyzed through MATLAB/SIMULINK simulation. The hardware prototype of the proposed multilevel inverter using digital signal processors (DSPs) in implementing the proposed modulation and current control algorithms has been developed for validation.

ABSTRAK

Perhatian yang semakin meningkat terhadap penyongsang bertingkat terutamanya dalam aplikasi sederhana dan kuasa yang tinggi telah membawa kepada usaha-usaha and inisiatif dipertingkatkan untuk menambah baik ciri-ciri dan daya saing penyongsang pelbagai peringkat. Kajian ini adalah sebahagian daripada usaha dan inisiatif itu, dengan penambahbaikan yang dirancang disasarkan kepada mengurangkan kerumitan litar dan kos. Bagi tujuan ini, topologi baru tiga fasa penyongsang bertingkat berdasarkan pendekatan perkongsian suis telah dicadangkan dalam kajian ini. Topologi ini terdiri daripada tiga modul. Gabungan Modul 1 dan Modul 2 menghasilkan satu susunan litar konvensional sepenuh jambatan dengan tiga suis dwiarah. Modul 3 yang terdiri daripada rentetan suis dwiarah disambungkan kepada sumber DC, mempunyai suis-suis tersebut untuk beroperasi dalam mod dioptimumkan. Dengan cara ini, pengendalian setiap suis dibahagikan di antara tiga fasa. Melalui penambahan satu suis dwiarah dalam Modul 3 sahaja, struktur dengan tahap yang lebih tinggi seterusnya terbentuk. Satu skim modulasi novel berdasarkan ruang konsep vektor dengan penggunaan vektor maya juga telah dibangunkan untuk topologi ini. Dengan menggunakan vektor maya, kesukaran untuk menguraikan vektor rujukan dalam zon tertentu akibat penghapusan beberapa vektor voltan, boleh diatasi dengan berkesan. Pengawal berkadar kamiran (PI) dilengkapi dengan modul penalaan automatik baru juga telah direka untuk menangani keadaan beban yang berbeza-beza. Kajian terperinci penyongsang yang dicadangkan diterangkan melalui contoh dari empat dan lima tahap struktur. Prestasi penyongsang yang dicadangkan dianalisis melalui simulasi MATLAB/SIMULINK. Pengesahan selanjutnya dilakukan melalui ujian praktikal dijalankan ke atas prototaip makmal dengan pemproses isyarat digital (DSP) digunakan untuk melaksanakan modulasi yang dicadangkan dan algoritma kawalan arus.

ACKNOWLEDGMENTS

First and foremost, my fullest praise and gratitude to Allah S.W.T. for giving me the will, strength and patience to complete this study despite the difficulties and challenges encountered.

My sincere thanks go to both of my thesis supervisors; Professor Dr. Nasrudin Abd. Rahim and Professor Dr. Hew Wooi Ping, for their continuous support, guidance and advices in making this study a successful journey. I am very fortunate to be given the opportunity to carry out the work independently under their supervision in the exploration for the possible solutions to the various problems faced. They have been very understanding, caring and cooperative indeed and I admire them for the good qualities that they have.

I would also like to express my special appreciation to all of my teachers and colleagues, namely Dr. Wijono, Dr. Mohamed N Abdul Kadir, Dr. Krismadinata, Mr. Syarkawi Syamsuddin, Mr. Fauzan Ismail, Mr. Muhammad Abdul Rahman, Mr. Messikh Tarek and Mr. Zulkarnain @ Khayree Faisal Ishak for their generous helps, useful suggestions, valuable ideas and kind willingness to exchange knowledge.

I am also thankful to the Ministry of Higher Education, Malaysia and the University of Malaya for providing me financial assistance to support my study. I am also appreciative of the role played by the UM Power Energy Dedicated Advanced Center (UMPEDAC) and the Institute of Research Management and Consultancy (IPPP) in allocating some funds for this research.

Last but not least, I would like to extend my deepest thanks to my parents and siblings for their endless love, priceless encouragement, strong inspiration and sincere pray. Without them, I will not be properly nurtured to achieve the accomplishments that I have attained.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS

$\alpha_1, \alpha_2, \alpha_3$ …..	Switching angles
$\Delta i_A, \Delta i_B, \Delta i_C$	Current errors
$\Delta i_d, \Delta i_q$	Current errors in synchronous rotating frame
$\Delta p, \Delta q$	Power errors
$\Delta v_d, \Delta v_q$	Outputs of the PI controllers
η	Efficiency
θ_{ref}	Reference voltage vector angle
φ	Phase angle
ω	Angular frequency
$\cos \gamma$	Power factor
$\frac{di(t)}{dt}$	Forward current rate
$\frac{di_d}{dt}, \frac{di_q}{dt}$	Synchronous rotating frame DC current derivatives
$\frac{di_A}{dt}, \frac{di_B}{dt}, \frac{di_C}{dt}$	Output current derivatives
$\frac{di_\alpha}{dt}, \frac{di_\beta}{dt}$	Stationary frame AC current derivatives
A, B, C, D, F, G	Constants used in the automatic tuning algorithm
$e(n)$	Error signal in discrete-time domain
$e(t)$	Error signal in continuous-time domain
$E_{sw,Diode}$	Diode switching energy loss
E_{TS}	IGBT switching energy loss
f	Fundamental frequency
h	Sampling period

H_n	Amplitude for harmonic n
i_A, i_B, i_C	Instantaneous output currents
$i_{A,ref}$, $i_{B,ref}$, $i_{C,ref}$	Reference output currents
i_d, i_q	Synchronous rotating frame DC currents
$i_{d,ref}$, $i_{q,ref}$	Synchronous rotating frame reference DC currents
I_{rms}	rms value of the load current
I_{RRM}	Reverse recovery current
i_α, i_β	Stationary frame AC currents
k_i	Integral gain
$k_{i,n}$	Integral gain in discrete-time domain
$k_{i,t}$	Integral gain in continuous-time domain
k_p	Proportional gain
$k_{p,n}$	Proportional gain in discrete-time domain
$k_{p,t}$	Proportional gain in continuous-time domain
L_f	Filtering inductor
n	Discrete-time index
N_s	Number of subintervals
p	Instantaneous real power
$P_{cond,Diode}$	Diode conduction loss
$P_{cond,IGBT}$	IGBT conduction loss
P_{loss}	Total power loss
P_{out}	Output power
p_{ref}	Reference real power
$P_{sw,Diode}$	Diode switching power loss
$P_{sw,IGBT}$	IGBT switching power loss
q	Instantaneous reactive power
Q_{K1}-Q_{K2}	Switches in Module 1 (K = A, B, C)

Q_{K3}	Switches in Module 2 (K = A, B, C)
q_{ref}	Reference reactive power
Q_{S1}-Q_{S3}	Switches in Module 3
S_A, S_B, S_C	Switching states
sum(n)	Summation
t	Time
t_1, t_2	Time increment
T_1, T_2, T_3	On-state time of nearest vectors
$T_{1,g}$, $T_{2,g}$	On-state time of nearest vectors solved using values in g-axis
$T_{1,h}$, $T_{2,h}$	On-state time of nearest vectors solved using values in h-axis
t_a	Time required for the diode reverse current to increase from zero to its peak negative value
t_b	Time required for the diode reverse current to fall from its peak negative value to zero
T_p	Period for one cycle
t_{rr}	Reverse recovery time
T_s	Sampling time
u(n)	Output of a general PI controller in discrete-time domain
u(t)	Output of a general PI controller in continuous-time domain
U_{high}	Top bound of the controller's output anti-windup module
$u_i(n)$	Output of the integral term of a general PI controller in discrete-time domain
$U_{i,high}$	Top bound of the integral anti-windup module
$U_{i,low}$	Bottom bound of the integral anti-windup module
U_{low}	Bottom bound of the controller's output anti-windup module
V_1, V_2, V_3	Nearest voltage vectors
$V_{1,g}$, $V_{2,g}$, $V_{3,g}$	Nearest voltage vectors components in g-axis

$V_{1,gn}$,	Normalized first nearest voltage vector component in *g*-axis
$V_{1,h}$, $V_{2,h}$, $V_{3,h}$	Nearest voltage vectors components in *h*-axis
$V_{1,hn}$,	Normalized first nearest voltage vector component in *h*-axis
v_{ab}, v_{bc}, v_{ca}	Instantaneous line-to-line load voltages
v_{AB}, v_{BC}, v_{CA}	Instantaneous line-to-line output voltages of the inverter
V_{AB}, V_{BC}, V_{CA}	Inverter's line-to-line output voltages
V_{aim}	Desired reference voltage vector amplitude
v_{aN}, v_{bN}, v_{cN}	Instantaneous phase load voltages
v_{AN}, v_{BN}, v_{CN}	Instantaneous phase output voltages of the inverter
V_{AN}, V_{BN}, V_{CN}	Inverter's phase output voltages
V_{AO}, V_{BO}, V_{BO}	Voltages across phase node (*A, B* or *C*) and node *O*
$v_{c,A}$, $v_{c,B}$, $v_{c,C}$	Control signals
V_{CE}	Collector-to-emitter voltage
v_d, v_q	Synchronous rotating frame DC load voltages
v_d, v_q, v_p	Control signals from the controller
V_{DC}	DC voltage
V_F	Forward voltage drop
V_g	Voltage vector component in *g*-axis
V_h	Voltage vector component in *h*-axis
V_{NO}	Voltage across node *N* and node *O*
V_p	Peak voltage amplitude
V_R	Reverse voltage drop
V_{ref}	Reference voltage vector
$V_{ref,g}$	Reference voltage vector component in *g*-axis
$V_{ref,gn}$	Normalized reference voltage vector component in *g*-axis
$V_{ref,h}$	Reference voltage vector component in *h*-axis
$V_{ref,hn}$	Normalized reference voltage vector component in *h*-axis

V_{rms}	rms value of the load phase voltage
V_s	Step voltage
$v_{s,d}$, $v_{s,q}$	Synchronous rotating frame DC output voltages of the inverter
$v_{s,\alpha}$, $v_{s,\beta}$	Stationary frame AC output voltages of the inverter
$V_{V1} - V_{V6}$	Virtual vectors of magnitude $\sqrt{3}V_{dc}$ for the proposed four-level inverter
V_{vec}	Voltage vector
$V_{X1} - V_{X6}$	Virtual vectors of magnitude $\sqrt{3}V_{dc}$ for the proposed five-level inverter
$V_{Y1} - V_{Y12}$	Virtual vectors of magnitude $\sqrt{7}V_{dc}$ for the proposed five-level inverter
V_α	Voltage vector component in α-axis
v_α, v_β	Stationary frame AC load voltages
V_β	Voltage vector component in β-axis

LIST OF ABBREVIATIONS

1DM	One-dimensional space vector modulation
3D-SVM	Three-dimensional space vector modulation
AC	Alternating current
APOD	Alternative phase opposition disposition
ASD	Adjustable speed drive
CO_2	Carbon dioxide
DC	Direct current
DPC	Direct power control
DPC-SVM	Direct power control with space vector modulation
DSP	Digital signal processor
DTC	Direct torque control
EMI	Electromagnetic interference
FOC	Field-oriented control
GPIO	General purpose input/output
HVDC	High voltage DC
IEA	International Energy Agency
IPPP	Institute of Research Management and Consultancy
ISR	Interrupt service routine
MMC or M2C	Modular multilevel converter
Mt	Megatonnes
NPC	Neutral-point-clamped
OVSS	Optimum vector selection scheme
PD	Phase disposition
P-DPC	Predictive direct power control

PI	Proportional integral
PLL	Phase-locked loop
POD	Phase opposition disposition
PWM	Pulse width modulation
REGS	Renewable energy generation system
rms	Root mean square
SFO-PWM	Switching frequency optimal PWM
SHE	Selective harmonic elimination
SHM	Selective harmonic mitigation
SVM	Space vector modulation
SVPWM	Space vector PWM
THD	Total harmonic distortion
TPES	Total Primary Energy Supply
UMPEDAC	University of Malaya Power Energy Dedicated Advanced Center
VAR	Volt Ampere Reactive
VOC	Voltage-oriented control

CHAPTER 1

INTRODUCTION

1.1 Introduction

This chapter provides a general idea about the work reported in this thesis. First, the importance of energy sustainability and how it initiates the motivation to carry out this research work is presented. Next, the objectives and methodology of the research work are explained. In the last section, overview of the chapters in this thesis is then described.

1.2 Study Motivation

Energy sustainability has become one major issue in the world today. It poses a great challenge in finding a balanced solution to the need of having energy resources for the benefits of mankind but without bringing serious harmful effects to the environment which needs to be conserved for the sake of future generations. According to the 2012 Key World Energy Statistics from the International Energy Agency (IEA), around 81% of the Total Primary Energy Supply (TPES) for the year of 2010 came from the fossil fuels. Although the use of fossil fuels offers a large amount of energy produced per unit weight with a fairly low production cost, they are not long-lasting. Fossil fuel reserves are depleting from time to time. As fossil fuels are categorized as non-renewable energy resources, there will be a time where fossil fuel supply can no longer meet energy demand. A serious energy crisis will occur if such a situation does take place in the future.

Another big concern regarding the use of fossil fuels is the increasing level of carbon dioxide (CO_2) emissions as a result of the burning activity of the fossil fuels. The

excessive release of this gas into the atmosphere contributes to the greenhouse effect which causes global warming and climate change. Based on the executive summary of World Energy Outlook 2013 published by IEA, two-thirds of global greenhouse-gas emissions are contributed from the energy sector. From the 2012 Key World Energy Statistics, 30,326 megatonnes (Mt) of CO_2 were released as of 2010, which is about double the emission level in the year of 1973. As energy demand is expected to increase in the future, the abovementioned executive summary projected that the energy-related CO_2 emissions will also rise by 20% to the year of 2035. This will result in an increase in the world's average temperature of 3.6 °C, which is higher than the 2 °C target.

To achieve energy sustainability, a two-pronged strategy has been implemented. The first prong is to increase the contributions of renewable energy to the world's TPES. Renewable energy that can be extracted from the sun, wind, tide, biomass and geothermal sources provides a good alternative to reduce the dependence on the fossil fuels as the main energy resources. Renewable energy can be supplied endlessly, thus makes it suitable to overcome the fossil fuel depletion issue. Besides, the most important fact about renewable energy that can make energy sustainability a triumphal policy is that it is environmentally friendly. No CO_2 emissions take place, thus this helps in tackling the global warming and climate change phenomena. No pollution of any sort is produced as well and this can make the world a safer place to live in not only for the current generation but also for the next generations to come. Nonetheless, there is still a barrier to the spread of the supply of renewable energy since the cost of development of renewable energy generation systems (REGSs) is not competitive at the present time. Therefore, the approach to enhance the deployment of renewable energy is more to a long-term measure.

The second prong that is suitable in the short and medium run seeks to improve energy efficiency by reducing the amount of energy consumed to power a specific application. Reduced energy consumption can be accomplished by minimizing energy wastage. In this respect, power electronic converters can play an important role. In adjustable speed drives (ASDs) which can be found in many applications such as pumps, fans, compressors, conveyors, etc a considerable level of energy saving can be acquired since ASDs ensure that the electric machine only consumes a sufficient amount of energy to carry out a particular task (Mohan, 2003). For an ASD to properly function, a power electronic converter known as the inverter is required. The converter is the heart of the variable-speed property of the drive since it is the one that regulates the power delivered to the machine (Kouro, Rodriguez, Bin, Bernet, & Perez, 2012). The same goes to REGSs such as those exploiting wind and solar photovoltaics as the main sources. The inverter converts the DC power into the AC power to be fed to the distribution grid. It is preferable for the inverter to perform the task with high efficiency.

Multilevel inverters have become more attractive for the ASDs and REGSs. As compared to the classical two-level inverters, multilevel inverters are able to produce voltage waveforms with better harmonic profile and lower total harmonic distortion (THD) as the many levels that exist in the waveform leads to a closer approximation to a pure sinusoid. This significant attribute paves the way for more advantages such as high voltage capacity, low voltage derivatives (*dv/dt*), few filter requirements, near sinusoidal currents and improved efficiency (Franquelo et al., 2008; Palanivel & Dash, 2011; Rodriguez et al., 2009). In addition to these beneficial characteristics, the original reason for the introduction of multilevel inverters is the ability of the inverters to achieve high voltage rating that is way beyond the maximum voltage rating of the existing semiconductor power switches. This special trait leads to the preference to

utilize multilevel inverters for medium and high power applications which the ASDs and REGSs are moving to. This preference emerges as a result of the economic and technical difficulties encountered in designing auxiliary circuits consisting of precise resistive and capacitive components to ensure equal voltage sharing among series-connected power switches, when the two-level inverter is to be used. Here, series connection of power switches is inevitable in order to achieve high voltages since the existing maximum voltage rating of the switches is limited to a certain value which is way too low for a high power application in particular.

Despite the fact that multilevel inverters are basically meant for medium and high power applications, the potential and tendency for them to be utilized in low power applications have also been explored especially when the issue of energy sustainability has become imperative nowadays. In line with the concerted efforts to enhance the deployment of renewable energy, innovative concepts have been proposed such as microgrids and building-integrated photovoltaics (BIPV). Microgrids are small-scale distributed power generation systems that are capable to perform self-generation of electric power for buildings. They offer the integration of different forms of renewable energy sources such as photovoltaic (PV) panels, fuel cells and microturbines into a small-capacity power generation network that can also be connected to the utility grid. They improves generation systems reliability in case of utility grid interruption that is caused by islanding phenomenon. In BIPV systems, the PV modules are used to replace certain parts of a building such as roof, skylight and façade. In this way, the building itself becomes a large PV structure for energy generation that can be useful not only to satisfy the building's energy demand but also to deliver surplus power to the grid.

In both microgrids and BIPV systems, investigations on the use of multilevel inverters have already been initiated. Although the two-level inverters are normally sufficient to accommodate low power applications, there are instances in which multilevel inverters can be useful. One such instance is observed in PV generation systems whereby multilevel inverters are proposed to overcome the problem of partial shading of individual PV modules which are connected in series (Abdalla, Corda & Zhang, 2013; Wang, Tan & Yi, 2011; Lee, Bae & Cho, 2009). Partial shading occurs when the PV modules are exposed to non-uniform irradiation, which then contributes to a significant reduction in output power. Another instance involves the use of multilevel inverters to reduce conversion losses so as to improve efficiency in microgrids (Liao & Lai, 2011; Shen, Jou, Wu & Wu, 2013).

Another low power application which has been reported to be of good potential for the use multilevel inverters is the aircraft system (De, Benerjee, Sivakumar, Gopakumar, Ramchand & Patel, 2010). As modern aircrafts are moving towards the electric-based architecture, inverters appear to be widely applied in compressors, hydraulic pumps, fuel metering, electric brake and starter for engine. However, several strict guidelines have to be fulfilled by the inverters. One such requirement is the weight restriction. The two-level inverters require the use of heavy differential mode and common mode filters. The only way to reduce the size of these filters is by increasing the switching frequency. However, this approach results in high heat dissipation which then contributes to the increased weight in the cooling system. Hence, multilevel inverters have been proposed as an attractive solution to the problems encountered with the two-level inverters.

In spite of the superior characteristics, multilevel inverters also suffer from one main dilemma. They require a high number of power switches as the number of levels increases (Gupta & Jain, 2013). This in turn contributes to a complex control problem and an increase in cost. As a result, careful considerations have to be made to ensure that a balanced compromise can be achieved, namely the inverters can still produce good quality outputs with high efficiency without deteriorating the circuit complexity issue and the implementation cost.

As an attempt to search for that balanced compromise, this study is then conducted. The study can be divided into two sections. The first section presents the design and implementation of the proposed multilevel inverter in the open-loop system. Conceptual design of the inverter with a novel pulse width modulation (PWM) scheme is explained. A laboratory prototype is constructed and tested with a digital signal processor (DSP) that is used to implement the PWM algorithm. The second section provides the development details of the current controller that is employed with a feedback path to form a closed-loop system. A DSP-based current controller is built to carry out the hardware testing for a closed loop system. Thorough analysis of the overall results obtained from simulation and experiment is subsequently conducted to appropriately assess the performance of the proposed multilevel inverter.

1.3 Research Objectives

The general aim of this research is to design a new multilevel inverter topology and to develop a control strategy that satisfies the needs to improve power quality and energy efficiency. The emphasis given in the design of the inverter is more on the reduction in the increase in the number of circuit's components as the number of voltage levels increases. The control strategy is developed with the main idea to find a good

tradeoff between harmonic contents and power losses. The specific objectives of this research as seen from three different perspectives are listed as follows:

1. Topology:

   To develop a three-phase multilevel voltage source inverter topology with the increase in the number of voltage levels only results in a minimum addition in the number of circuit's components.

2. Modulation technique:

   To design a novel PWM scheme that is able to accommodate the unique features reflected in the proposed multilevel inverter for the achievement of improved efficiency rating as well as low harmonic content and low total harmonic distortion in the inverter output.

3. Controller:

   To build an adaptive controller for current control with a new tuning algorithm in order to maintain a good quality of the output currents for varying load conditions.

1.4 Methodology

The design stage of this research begins with the introduction of the proposed multilevel inverter topology. The proposed topology is selected based on its ability to share several power switches among the three phases as a way to minimize the increase in the number of semiconductor components as the number of levels grows. In the preliminary analysis, the operational principles of the proposed topology for the case of the four-level and five-level structures at low switching frequency are investigated using the analytical approach. Then, for high switching frequency operation, space vector PWM (SVPWM) method is employed. To suit the uniqueness of the proposed topology, some modifications are made to the conventional SVPWM by utilizing virtual vectors. The four-level and five-level structures are studied to illustrate the proposed SVPWM.

A complete algorithm to calculate the on-state times of the nearest vectors based on the modified SVPWM is developed. To deal with changing load variations, an adaptive PI controller is proposed. The adaptive feature is realized through an automatic tuning algorithm that is developed for the anti-windup module.

As a way to verify the theoretical analysis, computer simulation using MATLAB/SIMULINK software is used. This software is widely employed in various engineering fields. First, simulation is carried out for open-loop system which requires no feedback path. The proposed four-level and five-level inverters are simulated for both low and high switching frequency operations. The proposed SVPWM is evaluated based on the simulation results obtained at various reference voltage amplitudes. Analysis on the waveform pattern, harmonic content, THD and voltage magnitude is conducted for the evaluation. Power loss investigation is also included. Next, for the closed-loop system that has a feedback path, simulation is performed to investigate the performance of the adaptive PI controller in varying load conditions. The simulation results are analyzed to assess the step responses and the output current quality.

To validate the simulation results, hardware implementation and experimental investigations are performed. A prototype of the proposed multilevel inverter is constructed to conduct laboratory testing. To execute the SVPWM and the control algorithms, DSP is used. Both open-loop and closed-loop testing are carried out. Experimental results are analyzed in detail to complete this research work.

1.5 Chapter Overview

This thesis comprises six chapters. The subsequent chapters are briefly described as the following:

Chapter 2 presents a general overview of three-phase multilevel inverters. It begins with a description about the fundamentals of multilevel inverters. A comprehensive review on multilevel inverter topologies including those categorized as classical and new ones is presented. Modulation techniques and current control methods suitable for multilevel inverters are also covered in this chapter.

Chapter 3 focuses on the design of the proposed multilevel inverter topology. A generalized structure of the proposed topology is given before the operational principles are described with the help of four-level and five-level structures. The details of the PWM strategy and controller's design are also discussed towards the end of this chapter.

Chapter 4 discusses the simulation results for the proposed multilevel inverter based on the four-level and five-level structure. The results include those when the inverter is operating at low switching frequency and at high switching frequency with the novel PWM scheme. Power loss analysis and dynamic performance assessment are also provided. Some comparative analysis against certain benchmarks is also included in this chapter.

Chapter 5 covers the details of the hardware implementation of the proposed multilevel inverter. The construction of a laboratory prototype of the inverter for four-level and five-level structures is described in this chapter. Information about the program codes to execute the control algorithms is also provided. The relevant experimental results and analysis are presented and discussed here.

Chapter 6 provides the concluding remarks drawn from this study. It also presents the contributions of the study and the recommendations for future work.

1.6 Summary

The increasing attention on energy sustainability nowadays has reinforced the efforts to push for the deployment of renewable energy and the improvement in energy efficiency. Multilevel inverters as one group in power electronic converters family can play a significant role in this respect. However, they are not in a position to have no flaws. Hence, this study is conducted to offer a solution in dealing with the weaknesses of multilevel inverters. The research objectives and methodology have been identified. The way this study is organized and reported in this thesis has also been presented.

CHAPTER 2

MULTILEVEL INVERTERS:

REVIEW OF TOPOLOGY, MODULATION TECHNIQUES AND CONTROL

2.1 Introduction

Power electronic converters facilitate the flow of power between the source and the load. This is done by converting the voltage and current from one form to another through the utilization of power semiconductor switches in the power circuit that are controlled by a control unit. There are four categories of power electronic converters: rectifiers converting AC to DC, inverters converting DC to AC, choppers or a switch-mode power supplies converting DC to another DC, and AC regulators converting AC to another AC. This chapter is devoted to provide a review of literature on a particular class of inverters known as the multilevel inverters. The chapter begins with a description on the fundamental concept of multilevel inverters including their advantages and drawbacks. Next, traditional multilevel inverter topologies are discussed before emerging topologies are presented. The various modulation techniques employed for these inverters are also provided before the current control techniques are explained.

2.2 Fundamentals of Multilevel Inverters

2.2.1 Basic Concept

Classical three-phase two-level inverters are able to generate output line-to-line voltage waveform with two levels namely 0 and $\pm V_{DC}$. The shape of the waveform is considered as quasi-square and far from a pure sinusoid. To improve the waveform's approximation to the ideal sinusoidal waveform, more levels are preferred and this gives birth to the concept of multilevel inverters. The general idea of multilevel inverters is to generate a multi-step voltage waveform that is synthesized by selecting several voltage

levels via the proper switching of power semiconductor switches. Theoretically, the number of steps can reach infinity. The higher the number of levels, the more steps are added in the waveform, thus the closer the waveform to imitate a perfect sine wave and the lower the harmonic distortion (Rodriguez, Jih-Sheng, & Fang Zheng, 2002).

To illustrate the multilevel concept, Figure 2.1 is presented. Consider one phase leg in the figure. The input DC voltage is divided into multiple sections either by using capacitor voltage dividers or by using battery cells. Through the use of multiple-input, single-output switch, the terminal of each section of the input DC voltage can be alternately connected to the load. If the switch has m inputs, then m possible voltage levels can be formed. As a result, the output line-to-line voltage waveform comprises $(2m - 1)$ steps. Figure 2.2 shows the corresponding waveforms for two-level and five-level inverters. It can be observed that the five-level inverter waveform has better approximation to the ideal sine wave.

To derive the line-to-line voltage equations, consider the voltage across nodes A and O, V_{AO} in Figure 2.1. This voltage is determined by the state of switch S_A. If S_A has m-inputs, then the possible states range from 0 to $m - 1$. Hence, V_{AO} can be expressed as the following:

$$V_{AO} = \frac{V_{DC}}{m-1} S_A \tag{2.1}$$

The same applies for voltages V_{BO} and V_{CO} whereby S_B and S_C are used respectively. Therefore,

$$V_{BO} = \frac{V_{DC}}{m-1} S_B \tag{2.2}$$

$$V_{CO} = \frac{V_{DC}}{m-1} S_C \tag{2.3}$$

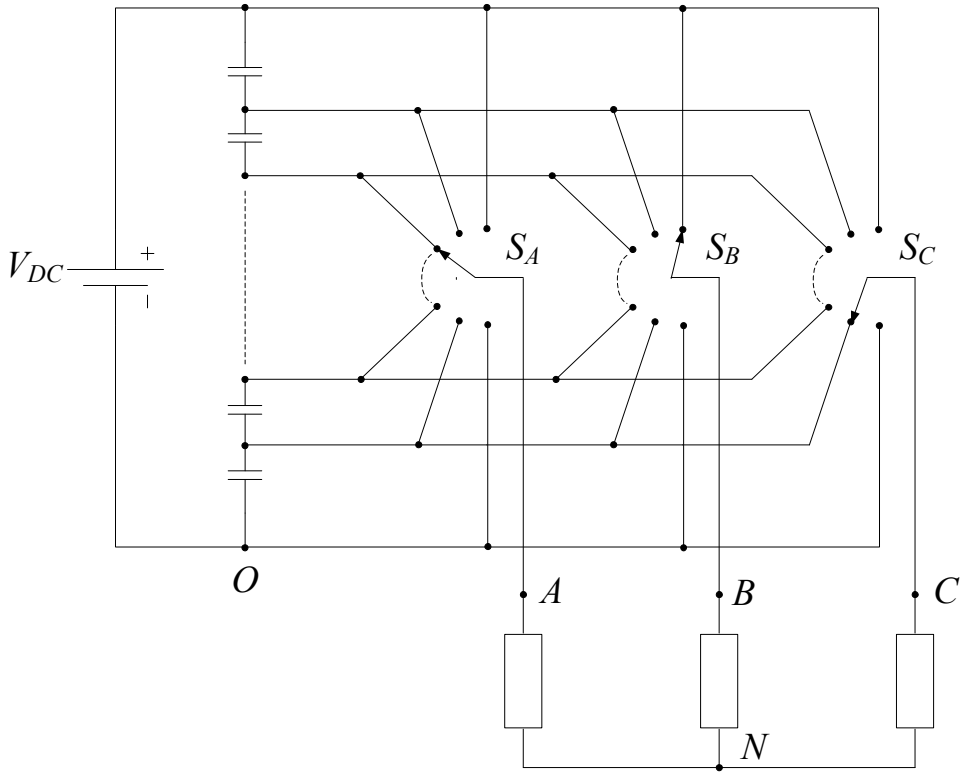
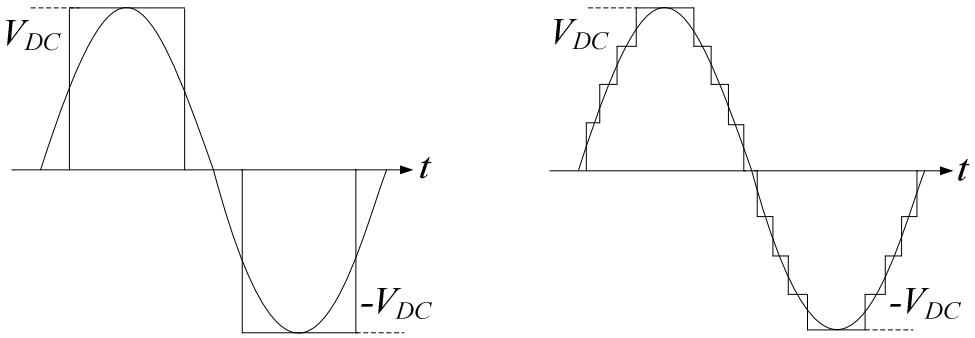


Figure 2.1: Generalized structure of an ideal multilevel inverter model.



(a) Two-level waveform (b) Five-level waveform

Figure 2.2: Comparison of the output line-to-line voltage waveforms in approximating a sinusoidal reference between two-level and five-level inverters.

To obtain the expressions for the line-to-line voltages, the following applies:

$$\begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix} = \begin{bmatrix} V_{AO} - V_{BO} \\ V_{BO} - V_{CO} \\ V_{CO} - V_{AO} \end{bmatrix} = \frac{V_{DC}}{m-1} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} S_A \\ S_B \\ S_C \end{bmatrix} \tag{2.4}$$

In equation (2.4), the coefficient $\frac{V_{DC}}{m-1}$ represents the voltage in between the steps. From equations (2.4), it can be calculated that the peaks of the line-to-line voltages have values of $\pm V_{DC}$.

2.2.2 Comparison with Two-Level Inverters

The obvious limitation of the three-phase two-level inverter is that the output line-to-line voltage only consists of three voltage steps. As a result, the quality of the output voltage and current waveforms has been compromised with a high amount of ripple content. To avoid this problem, the inverter requires high frequency PWM switching (Rashid, 2004). However, high frequency switching can lead to high switching losses and increased common-mode voltages. The common-mode voltage issue can further cause fault activation of current detection circuits, undesirable electromagnetic interference (EMI) to the surrounding equipment and damage to motor bearings (Yen-Shin & Fu-San, 2004). If the inverter is utilized in high-power and high-voltage applications, the power semiconductor devices suffer from high *dv/dt* stress, thus the need for high power semiconductors is critical. Unfortunately, since the high power semiconductor technology is still not mature (Franquelo, Rodriguez, Leon, Kouro, Portillo, & Prats, 2008), the use of two-level inverter for these applications is rather limited indeed.

Multilevel inverter's strength lies in the fact that the output voltage waveforms contain more than three voltage steps. As the number of voltage steps increases, the

THD reduces further and the harmonic content decreases significantly (Rashid, 2004). The presence of many voltage steps also implies a reduction in *dv/dt* stress, thus making the inverter suitable for high-power and high-voltage applications. Besides, reduced *dv/dt* stress also allows the inverter to be capable of reaching high voltages without increasing the ratings of the individual power semiconductors (Serpa, 2007). In addition, lower common-mode voltages can also be obtained which further minimizes the EMI effects. In fact, with appropriate modulation methods, common mode voltages can be eliminated altogether (Rodriguez, Jih-Sheng, & Fang Zheng, 2002). Less filter requirement is sufficient for the inverter, owing to the improved quality of the output waveforms (Rodriguez, Franquelo, Kouro, Leon, Portillo, Prats, & Perez, 2009).

Despite the advantages offered, multilevel inverter has one obvious weakness as compared to the two-level inverter. It requires a high number of circuit's components. This increases the likelihood of the inverter to fail or malfunction, thus reliability becomes a concern (Babaei & Hosseini, 2009; K. K. Gupta & Jain, 2013). A high number of components particularly the power semiconductor switches also poses an issue of additional control complexity. Computational burden of the control unit increases and this may result in the need for more powerful processors. A significant increase in the total cost of implementation is also inevitable. For the case of capacitor usage to divide the input DC voltage, a sort of voltage balancing method has to be adopted as well (Jih-Sheng & Fang Zheng, 1996).

2.3 Topologies of Multilevel Inverters

The realization of multilevel inverter circuits can be traced back to the late 1960s when the cascaded H-bridge converter and the low-power flying capacitor topology were introduced (Kouro, Malinowski, Gopakumar, Pou, Franquelo, Bin,

Rodriguez, Perez, & Leon, 2010). About a decade later, the diode-clamped multilevel inverter was developed. When it was first used in a three-level structure for medium voltage applications, the diode-clamped inverter was also known as the neutral-point-clamped (NPC) inverter since the mid-voltage level was marked as the neutral point (Nabae, Takahashi, & Akagi, 1981). Up to the 1990s, these three inverter topologies have become the subject of in-depth investigations before other topologies emerged. Since those topologies were already in existence for the last three decades or so, they can now be considered as classic or traditional multilevel inverter topologies. Other topologies that came later are categorized as new or emerging topologies.

2.3.1 Classic Topologies

Diode-clamped, flying-capacitor and cascaded H-bridge inverters have provided the fundamental circuit configurations to implement a multilevel structure. They have become the benchmarks for other topologies to rely on for comparison in terms of performance and characteristics. Therefore, it is imperative to know about these classic topologies before further study on multilevel inverters can be conducted.

2.3.1.1 Diode-Clamped Inverter

The diode-clamped inverter (Ozdemir, Ozdemir, & Tolbert, 2009; Renge & Suryawanshi, 2008; Rodriguez, Bernet, Steimer, & Lizama, 2010) is noticeably characterized by the presence of clamping diodes. For a three-phase m-level structure, the inverter generates line-to-line voltage waveforms with $(2m - 1)$ steps. The inverter is typically supplied by one DC voltage supply V_{DC} which is then split by $(m - 1)$ series-connected capacitors. The voltage across each capacitor, which is defined as $\frac{V_{DC}}{m-1}$, can be tapped and connected to the inverter arm via power switches or clamping diodes. A

total of 6(m – 1) power switches and 3(m – 1)(m – 2) clamping diodes are required to construct the power circuit.

To explain the principle of operation of the diode-clamped inverter, a three-phase five-level structure is taken as an example. Figure 2.3 shows the three-phase five-level diode-clamped inverter. The voltage across each capacitor is $\frac{V_{DC}}{4}$. Consider only one arm, phase A for instance, and take neutral point N as the reference point to define the voltage across nodes A and N, V_{AN}. Five values of V_{AN} can be obtained through the following switch combinations:

1. Switches S_{A1}, S_{A2}, S_{A3} and S_{A4} are turned on while others are turned off to obtain $V_{AN} = \frac{V_{DC}}{2}$.
2. Switches S_{A2}, S_{A3}, S_{A4} and S_{A1}' are turned on while others are turned off to obtain $V_{AN} = \frac{V_{DC}}{4}$.
3. Switches S_{A3}, S_{A4}, S_{A1}' and S_{A2}' are turned on while others are turned off to obtain $V_{AN} = 0$.
4. Switches S_{A4}, S_{A1}', S_{A2}' and S_{A3}' are turned on while others are turned off to obtain $V_{AN} = -\frac{V_{DC}}{4}$.
5. Switches S_{A1}', S_{A2}', S_{A3}' and S_{A4}' are turned on while others are turned off to obtain $V_{AN} = -\frac{V_{DC}}{2}$.

It can be seen that for each value of V_{AN}, four switches must be turned on while the remaining four are turned off. In addition, switches S_{A1} and $S_{A1'}$ work in complementary manner. The same is true for switch pairs (S_{A2},S_{A2}'), (S_{A3},S_{A3}') and (S_{A4},S_{A4}'). Another

point worth mentioning is that three middle values of V_{AN} namely 0, $\frac{V_{DC}}{4}$ and $-\frac{V_{DC}}{4}$ cannot be generated without the role played by the clamping diodes. For example, to obtain $V_{AN} = 0$, either diodes D_{A2} or D_{A2}' become active, depending on the direction of the load current. If the current flows to the load, then D_{A2} becomes active. D_{A2}' only conducts when the current flows from the load.

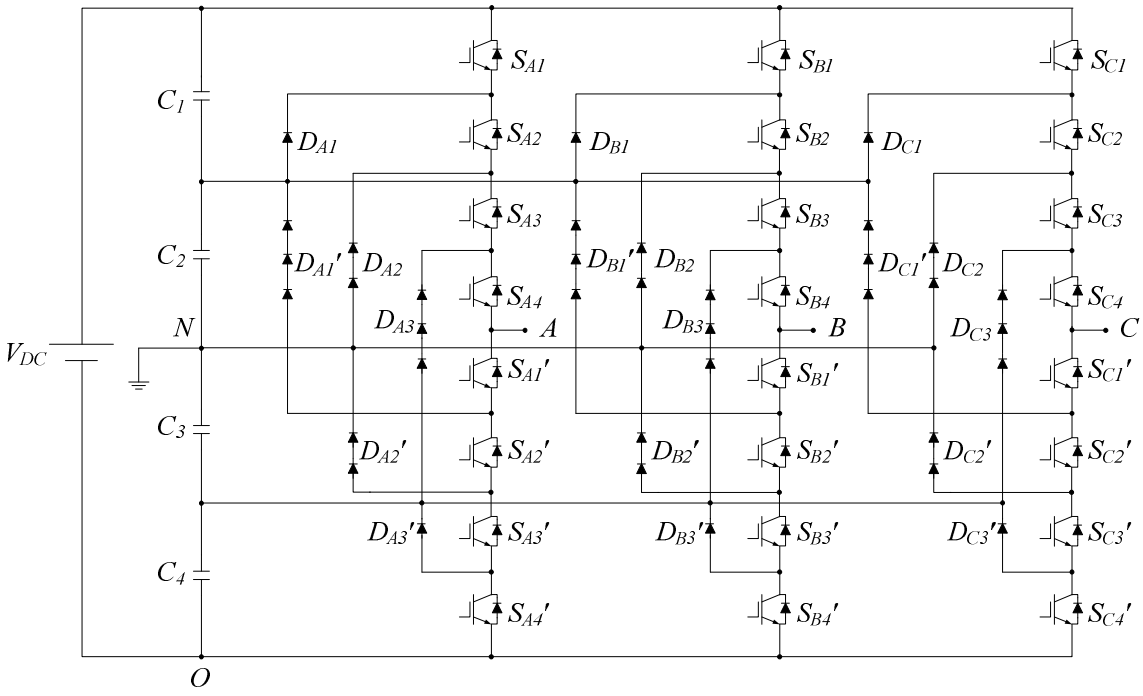


Figure 2.3: Three-phase five-level diode-clamped inverter.

One advantageous fact about the diode-clamped inverter is that each power switch only blocks a voltage step of $\frac{V_{DC}}{m-1}$, or $\frac{V_{DC}}{4}$ in the case of the five-level structure. Hence, no switches have to experience a voltage level higher than that, thus minimizing the possibility of a switch failure if the voltage level exceeds the voltage rating of the switch. However, the case is different for the clamping diodes. Depending on the position, each clamping diode has to have different voltage ratings to block the reverse voltage. As an illustration, consider a condition whereby S_{A2}', S_{A3}' and S_{A4}' in

Figure 2.3 are turned on. Diode D_{A1}' has to block three capacitor voltages of a total of $\frac{3V_{DC}}{4}$. The same is experienced by D_{A3} while D_{A2} and D_{A2}' need to block $\frac{V_{DC}}{2}$. If all clamping diodes have similar ratings as the power switches, then some diodes have to experience excessive voltage. To avoid this limitation, series connection of diodes is applied, but at the expense of increasing the number of clamping diodes in a quadratic manner. For a five-level structure, the number of clamping diodes required is 36. As the number of levels increases, more clamping diodes are needed, thus deteriorating the complexity faced for practical implementation.

Another issue with the diode-clamped inverter is the unequal loss distribution among the semiconductor devices. Several switches conduct longer than the others. As a result, these switches become hot earlier than the others. Therefore, for these switches, higher current rating and different cooling system are needed. Capacitor voltage balancing problem also poses a great challenge (Du Toit Mouton, 2002; Marchesoni & Tenca, 2002). Additional circuit may have to be included to properly balance the voltage across each capacitor.

2.3.1.2 Flying-Capacitor Inverter

Unlike diode-clamped inverter, the flying-capacitor inverter (Escalante, Vannier, & Arzande, 2002; H. Jing & Corzine, 2006; Kang, Lee, & Hyun, 2004) is well recognized through the use of auxiliary capacitors known as flying capacitors in addition to the DC link capacitors. For a three-phase m-level structure, the line-to-line voltage waveforms consist of $(2m - 1)$ steps. The number of DC link capacitors required to divide the DC input voltage V_{DC} is $(m - 1)$. Flying capacitors are used to clamp the switch voltage to one capacitor voltage level which is given by $\frac{V_{DC}}{m-1}$. A total of $6(m -$

1) power switches and $\frac{3}{2}(m-1)(m-2)$ flying capacitors are required to construct the power circuit.

The operational principle of the flying-capacitor inverter can be described with the aid of a five-level structure as displayed in Figure 2.4. By considering one phase, say phase A, five voltage levels can be generated across nodes *A* and *N*. Table 2.1 provides the switch combinations to obtain all the five levels. It can be noticed that for voltage levels 0, $\frac{V_{DC}}{4}$ and $-\frac{V_{DC}}{4}$, more than one switch combinations can be employed. This allows flexibility in selecting the appropriate switch combinations to balance the charging and discharging of capacitors. However, this flexibility is unavailable for $\frac{V_{DC}}{2}$ and $-\frac{V_{DC}}{2}$ voltage levels since these levels do not involve the use of the capacitors. Despite the flexibility offered, the selection process of the appropriate switch combinations may not be that straightforward. In fact, it can become very complicated and tedious indeed.

The flying-capacitor inverter does not require isolated DC sources and clamping diodes. Nevertheless, these properties may be limited by flying capacitors' voltage unbalancing problem although the extra redundant switch combinations created by the flying capacitors can be exploited to tackle the unbalancing problem. Another issue is that the flying capacitors are exposed to different voltage levels, similar to the blocking requirements of the clamping diodes. Therefore, several capacitors must be connected in series to divide equally the voltage stress across each capacitor. As a result, a large number of flying capacitors are needed.

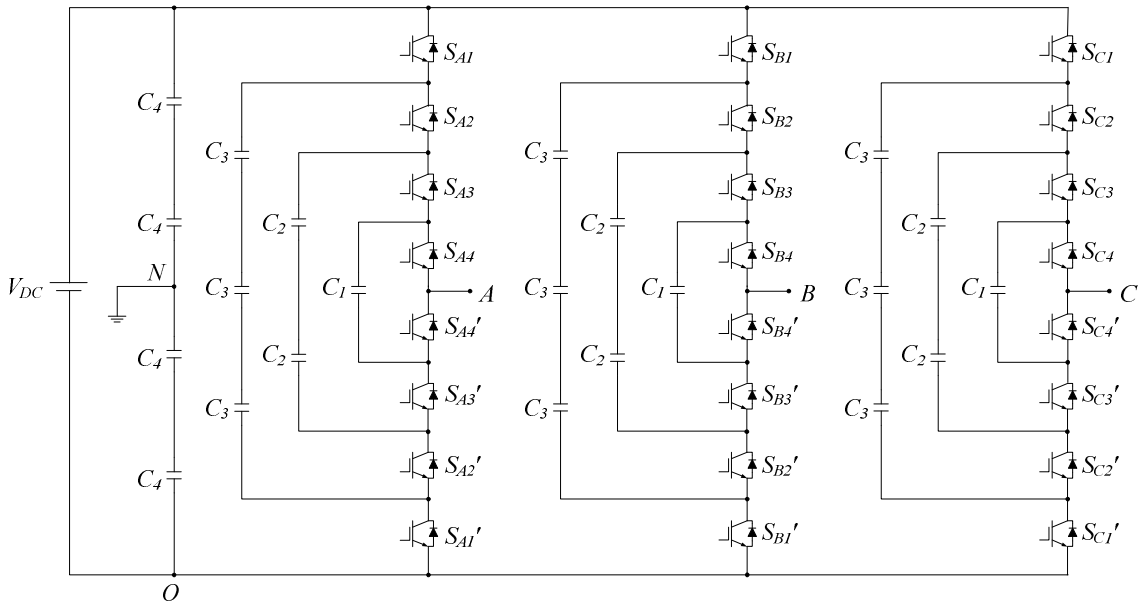


Figure 2.4: Three-phase five-level flying-capacitor inverter.

Table 2.1: Voltages and switch states for phase A of five-level flying-capacitor inverter.

V_{AN}	Switch states							
	S_{A1}	S_{A2}	S_{A3}	S_{A4}	S_{A1}'	S_{A2}'	S_{A3}'	S_{A4}'
$\frac{V_{DC}}{2}$	**On**	**On**	**On**	**On**	Off	Off	Off	Off
$\frac{V_{DC}}{4}$	**On**	**On**	**On**	Off	Off	Off	Off	**On**
	On	**On**	Off	**On**	Off	Off	**On**	Off
	On	Off	**On**	**On**	Off	**On**	Off	Off
	Off	**On**	**On**	**On**	**On**	Off	Off	Off
0	**On**	**On**	Off	Off	Off	Off	**On**	**On**
	On	Off	**On**	Off	Off	**On**	Off	**On**
	Off	**On**	**On**	Off	**On**	Off	Off	**On**
	On	Off	Off	**On**	Off	**On**	**On**	Off
	Off	**On**	Off	**On**	**On**	Off	**On**	Off
	Off	Off	**On**	**On**	**On**	**On**	Off	Off
$-\frac{V_{DC}}{4}$	**On**	Off	Off	Off	Off	**On**	**On**	**On**
	Off	**On**	Off	Off	**On**	Off	**On**	**On**
	Off	Off	**On**	Off	**On**	**On**	Off	**On**
	Off	Off	Off	**On**	**On**	**On**	**On**	Off
$-\frac{V_{DC}}{2}$	Off	Off	Off	Off	**On**	**On**	**On**	**On**

2.3.1.3 Cascaded H-Bridge Inverter

The cascaded H-bridge inverter (Alonso, Sanchis, Gubia, & Marroyo, 2003; Malinowski, Gopakumar, Rodriguez, & Perez, 2010; Villanueva, Correa, Rodriguez, & Pacas, 2009) is formed from a series connection of single-phase H-bridge inverter cells with each cell has its own separated DC voltage supply. For a three-phase *m*-level structure, the line-to-line voltage waveforms comprise (2*m* – 1) steps. The number of DC link capacitors or separated DC sources required is $\frac{3}{2}(m-1)$. A total of 6(*m* – 1) power switches are required to construct the power circuit without any use of clamping diodes or flying capacitors.

Figure 2.5 which portrays the five-level cascaded H-bridge inverter, is used to explain the operational principle of the inverter. To simplify the explanation, one phase is considered. Here, take phase A as the phase of interest. Five voltage levels can be generated across nodes *A* and *N*. These voltage levels are achieved by adding the individual cell voltages. Taking Cell 1 as an illustration, the individual cell has the following voltage outputs:

1. Switches S_{A1} and S_{A4} are turned on while others are turned off to obtain V_{DC}.
2. Switches S_{A1} and S_{A2} (or S_{A3} and S_{A4}) are turned on while others are turned off to 0.
3. Switches S_{A2} and S_{A3} are turned on while others are turned off to obtain $-V_{DC}$.

Table 2.2 lists the switch combinations to obtain all the five levels. Similar to flying-capacitor inverter, the middle voltage levels namely 0, V_{DC} and $-V_{DC}$ have more than one switch combinations. This provides options in selecting the optimum switch combinations to satisfy certain criteria such minimizing switching actions or balancing switch's current.

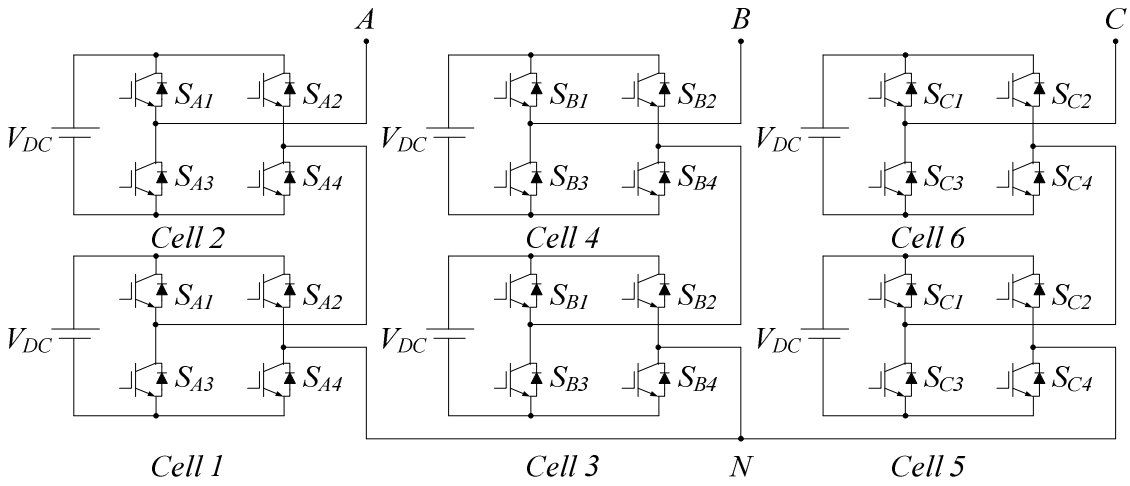


Figure 2.5: Three-phase five-level cascaded H-bridge inverter.

Table 2.2: Voltages and switch states for phase A of five-level cascaded H-bridge inverter.

V_{AN}	Switch states							
	Cell 1				Cell 2			
	S_{A1}	S_{A2}	S_{A3}	S_{A4}	S_{A1}	S_{A2}	S_{A3}	S_{A4}
$2V_{DC}$	**On**	Off	Off	**On**	**On**	Off	Off	**On**
V_{DC}	**On**	Off	Off	**On**	**On**	**On**	Off	Off
	On	Off	Off	**On**	Off	Off	**On**	**On**
	On	**On**	Off	Off	**On**	Off	Off	**On**
	Off	Off	**On**	**On**	**On**	Off	Off	**On**
0	**On**	Off	Off	**On**	Off	**On**	**On**	Off
	On	**On**	Off	Off	**On**	**On**	Off	Off
	On	**On**	Off	Off	Off	Off	**On**	**On**
	Off	Off	**On**	**On**	Off	Off	**On**	**On**
	Off	Off	**On**	**On**	**On**	**On**	Off	Off
	Off	**On**	**On**	Off	**On**	Off	Off	**On**
$-V_{DC}$	**On**	**On**	Off	Off	Off	**On**	**On**	Off
	Off	Off	**On**	**On**	Off	**On**	**On**	Off
	Off	**On**	**On**	Off	**On**	**On**	Off	Off
	Off	**On**	**On**	Off	Off	Off	**On**	**On**
$-2V_{DC}$	Off	**On**	**On**	Off	Off	**On**	**On**	Off

When compared with the diode-clamped and flying-capacitor inverters, the cascaded H-bridge inverter offers the least number of components to produce the same number of voltage levels. Since the H-bridge cells are identical, the cascaded H-bridge inverter circuit can be easily modified by simply adding or removing the cells to achieve

the desired number of levels. This is a preferable design feature as the circuit does not have to go through a major redesign process when the desired number of levels is changed. Despite the advantages mentioned, this inverter requires multiple separated DC supplies and thus its application is somewhat limited. Although one transformer with multiple isolated DC secondaries have been suggested to replace the separated DC supplies, it appears that this solution rather makes the circuit more complicated.

2.3.2 Emerging Topologies

Some of the concerns arising from the fact that the three classic multilevel inverters are lacking in certain areas, have contributed to the advent of new multilevel inverter topologies. Each of these new topologies was introduced to iron out some specific issues viewed from the perspective of the circuit's size and weight, overall cost, output quality, switching frequency, power loss, efficiency, reliability, device utilization, fault-tolerance capability and many more. Most of these topologies were derived from classic multilevel inverters with some modifications. This section presents several topologies under this category which are also known as emerging topologies.

2.3.2.1 Active Neutral-Point-Clamped Inverter

One of the main issues involving the diode-clamped or the NPC inverter is the unequal loss distribution among the power semiconductors in each inverter leg (Bruckner & Bemet, 2001). It was observed that the outer switches in the three-level neutral-point-clamped inverter conduct longer than the inner switches during a fundamental cycle. This requires the use of different heat sinks and cooling systems for switches that produce high and low losses. Besides, the maximum power rate, output current and switching frequency have to be limited to a certain range (Kouro, Malinowski, Gopakumar, Pou, Franquelo, Bin, Rodriguez, Perez, & Leon, 2010). A solution was

proposed with the introduction of active NPC inverter (Bruckner & Bemet, 2001; Bruckner, Bernet, & Guldner, 2005). This inverter uses clamping switches to replace the clamping diodes in the conventional NPC inverter. Figure 2.6 shows the active NPC inverter for a three-level structure.

The clamping switches provide an additional path for the neutral current. Taking phase A in Figure 2.6 as an example, there are two paths for the neutral current to flow to generate zero voltage level. If the current flows to the load, then the first path is through D_{A3} and S_{A2}, and the second path is through S_{A3}' and the antiparallel diode of S_{A1}'. Two paths can also be used if the current flows from the load. By forcing the current to flow in the two paths in the alternate manner through the appropriate control of S_{A2} and S_{A3}', then the power loss distribution among the semiconductor devices can be properly adjusted. The NPC inverter obviously lacks of this behavior since there is only one path for the neutral current to flow.

Based on the three-level active NPC concept, a five-level structure has been derived by combining the three-level active NPC leg and the three-level flying-capacitor cell (Barbosa, Steimer, Steinke, Meysenc, Winkelnkemper, & Celanovic, 2005). By having this combination, the strength of the NPC and the flying-capacitor inverters can be integrated in one superior topology. Figure 2.7 shows one leg of the five-level active NPC inverter. Despite the superiority shown in the active NPC topology in some aspects, the fact that the increase in the number of switches used may lead to a more complex control strategy. The use of flying-capacitor cells also presents a challenge to balance the capacitor voltages.

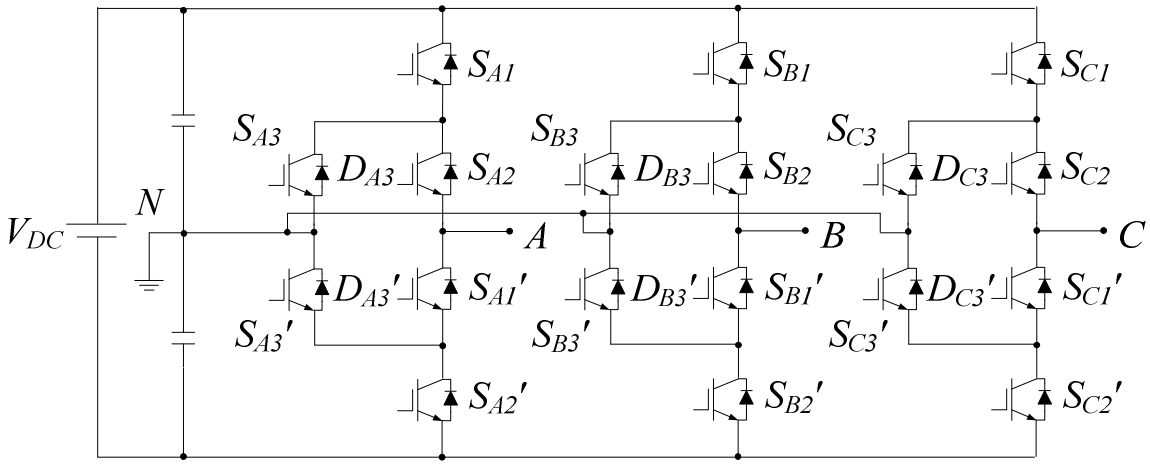


Figure 2.6: Three-phase three-level active neutral-point-clamped inverter.

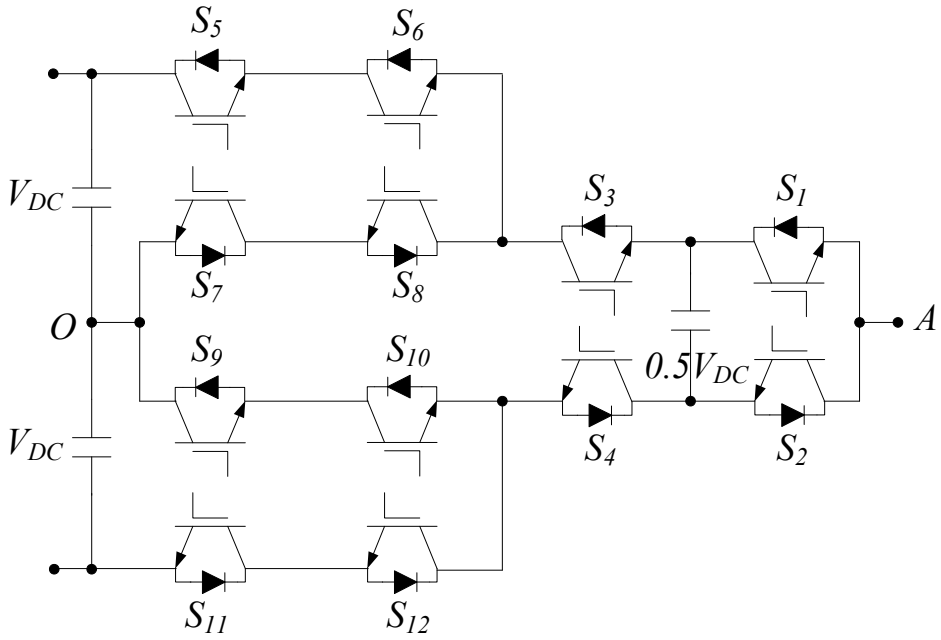


Figure 2.7: One leg of five-level active neutral-point-clamped inverter.

2.3.2.2 Modular Multilevel Converter

Modular multilevel converter (MMC or M2C) is one of the next-generation multilevel converters intended for high- or medium-voltage power conversion without transformers (Hagiwara & Akagi, 2009). This converter has attracted a lot of attention in recent years especially in the field of high voltage DC or HVDC transmission

(Marquardt, 2010). Figure 2.8 displays the structure of the three-phase MMC. This converter combines the elements of both the series-connected H-bridge converter and the flying-capacitor converter (Rohner, Bernet, Hiller, & Sommer, 2010). The converter consists of six arms in which every two of them forms one phase leg. Each arm is composed of a number of identical cells or submodules which are connected in series and an inductor. Half-bridge cells are typically used but full-bridge and clamp-double cells have also been proposed (Marquardt, 2010). The inductor provides protection that limits the AC current in case of a short circuit at the DC side.

For a half-bridge cell, two switching states can be generated. On state occurs when the upper switch is turned on and the lower switch is turn off which then lead to the cell output voltage to be equal to the capacitor voltage. Off state happens when the opposite takes place which results in a zero cell output voltage. With a suitable number of cells connected in series, controlled by an appropriate switching scheme for the cells in the two arms per phase leg, a multilevel voltage waveform can be generated. As for the arm currents, they flow continuously and are not chopped (Marquardt, 2010).

The MMC topology attractive features include the modular design and the simple voltage scaling through the series connection of cells. With many cells included in the topology, the stepped voltage waveform can approximate very closely to an ideal sinusoid with a very low harmonic distortion, thus a filterless configuration is possible. A reduction in the device average switching frequency can also be accomplished without compromising power quality. However, the increase in the number of cells implies the use of many semiconductor devices. In addition, for floating capacitors, a proper voltage balancing control is essential (Lesnicar & Marquardt, 2003).

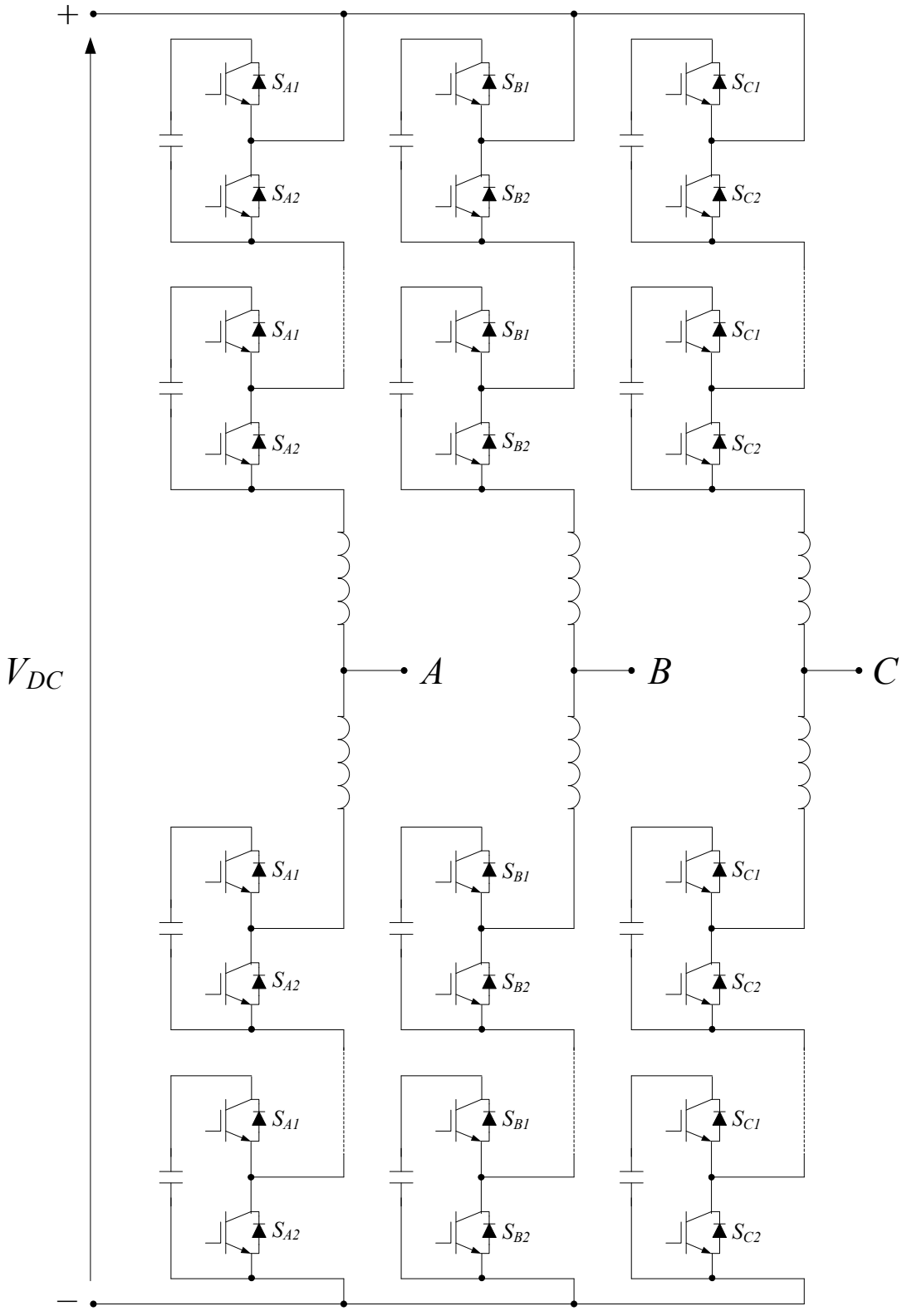


Figure 2.8: Modular multilevel converter.

2.3.2.3 Asymmetric Cascaded H-Bridge Inverter

An approach to increase the number of levels in the output voltages generated from a cascaded H-bridge inverter is suggested by employing unequal DC voltage sources (Mueller & Park, 1994). This type of inverter is known as the asymmetric cascaded H-bridge inverter. Figure 2.9 depicts an example of the inverter circuit. Considering only one phase, say phase A, cell 1 and cell 2 are supplied by two different DC voltage supplies, namely $2V_{DC}$ and V_{DC}. By implementing this, seven output voltage levels can be generated across nodes *A* and *O* as compared to five levels which are produced when both cells are supplied by equal DC voltage inputs.

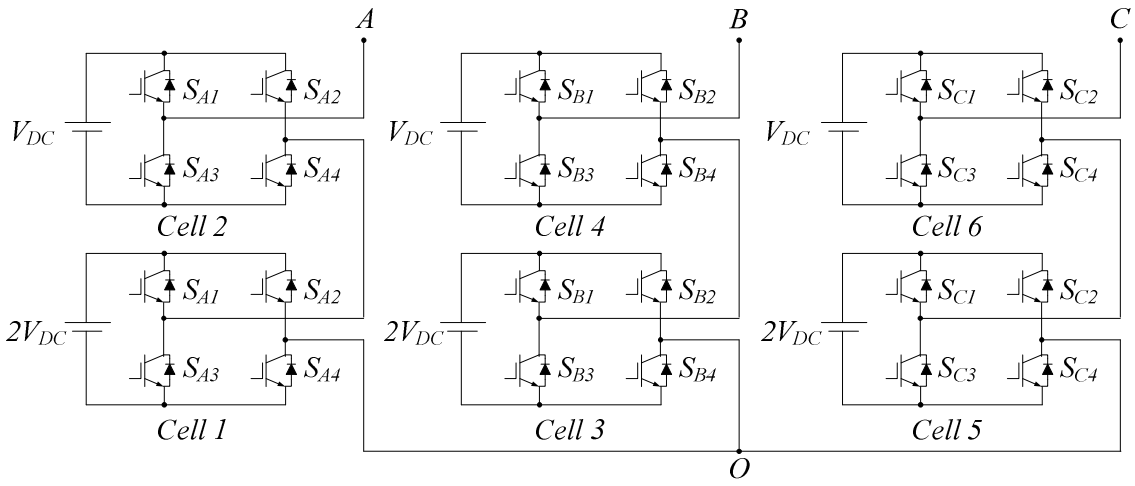


Figure 2.9: Three-phase asymmetric cascaded H-bridge inverter.

To further maximize the number of voltage levels, voltage ratios in powers of three were proposed (Dixon, Breton, Rios, Rodriguez, Pontt, & Perez, 2007; Yu & Fang-Lin, 2008). With this configuration, for inverter having *m* cells per phase leg, 3^m voltage levels can be generated (Kadir & Hussien, 2005). Besides, another approach proposed the use of capacitors in several cells to reduce the number of separated DC sources (Zhong, Tolbert, Chiasson, & Ozpineci, 2006). For a single-phase structure, only one DC source is used in the first cell while the other cells use capacitors.

However, this approach requires a complex control strategy since an additional criterion, namely capacitor voltage balancing has to be met.

Besides increasing the number of levels in exponential manner, asymmetric cascaded H-bridge inverter allows the high power cells to operate at low switching frequency, thus reducing switching losses. However, the utilization of different switching frequencies between the high and low power cells results in uneven power distribution among the cells. Different switching device categories with different thermal designs are necessary to satisfy the unequal characteristics of the cells. As a result, the modularity advantage of the cascaded H-bridge inverter is lost since the cells are no longer identical. In addition, the use of separated DC sources is still considered a major disadvantage for this inverter.

2.3.2.4 Mixed-Level Cascaded H-Bridge Inverter

Mixed-level cascaded H-bridge inverter is basically constructed from the combination of the cascaded H-bridge inverter with the other two classic multilevel inverters. This is realized by replacing the H-bridge cells with diode-clamped converter cells or flying-capacitor converter cells (Hill & Harbourt, 1999). By doing so, the number of separated DC sources can be reduced. Figure 2.10 displays the nine-level mixed-level cascaded H-bridge inverter using the flying-capacitor converter cells. By having this arrangement, only six separated DC sources are needed as compared to 12 if the H-bridge cells are used. This accounts for a considerable reduction of 50% in the number of DC supplies. This saving is made possible since the flying-capacitor converter cells are of a five-level structure in contrast to the H-bridge cells of the three-level structure. Nevertheless, the use of the five-level cells worsens the control

complexity. For the case of capacitor usage in the cells, voltage balancing issue needs to be resolved.

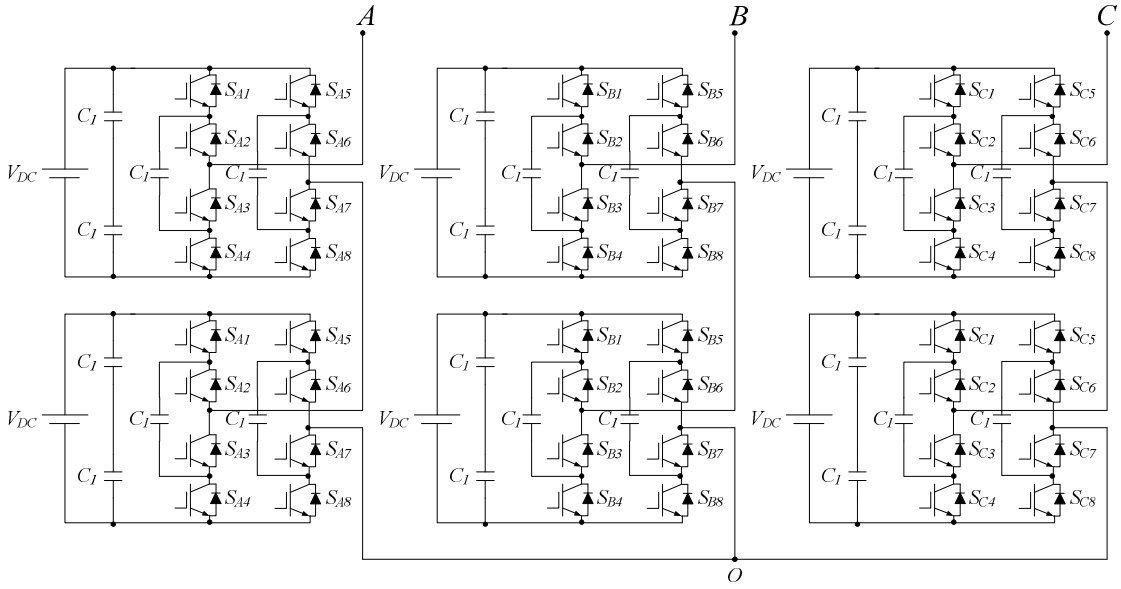


Figure 2.10: Three-phase mixed-level cascaded H-bridge inverter.

2.3.2.5 Hybrid Multilevel Inverter

Like the asymmetric and mixed-level cascaded H-bridge inverter, hybrid multilevel inverter is also introduced to basically reduce the number of separated DC supplies in the cascaded H-bridge inverter. Hybrid inverter integrates two different topologies into one that is expected to offer better characteristics and performance. By this definition, in the literature, some considered asymmetric and mixed-level cascaded H-bridge inverter as part of the hybrid inverter family. Another form of hybrid inverter is shown in Figure 2.11 whereby two stages of different topologies are combined (Mariethoz & Rufer, 2004). Through series connection, this inverter connects the three-phase full-bridge circuit as the first stage to a single-phase H-bridge cell per phase leg, as the second stage. By doing so, one DC supply is sufficient to replace three separated DC sources in the first stage.

The second stage functions as an active filter that contributes to the enhancement of power quality and the reduction of common mode voltages (Kouro, Malinowski, Gopakumar, Pou, Franquelo, Bin, Rodriguez, Perez, & Leon, 2010). To attain the desired number of voltage levels, the ratio of DC voltage of the first stage to that of the second stage is adjusted. Besides, unlike the symmetric or asymmetric cascaded H-bridge inverter that can only generate odd number of voltage levels, the hybrid inverter can also produce even number of voltage levels that may be necessary in some applications to achieve optimum device utilization (Serpa, 2007).

In replacement of the six-switch full-bridge circuit, the NPC inverter has also been employed in the first stage (Veenstra & Rufer, 2005). The DC voltage sources for the H-bridge inverter in the second stage are replaced with capacitors. The use of capacitors further reduces the number of DC sources in the hybrid inverter. However, the inverter becomes more difficult to control and its operation is highly nonlinear. Special control of the floating capacitors is essential.

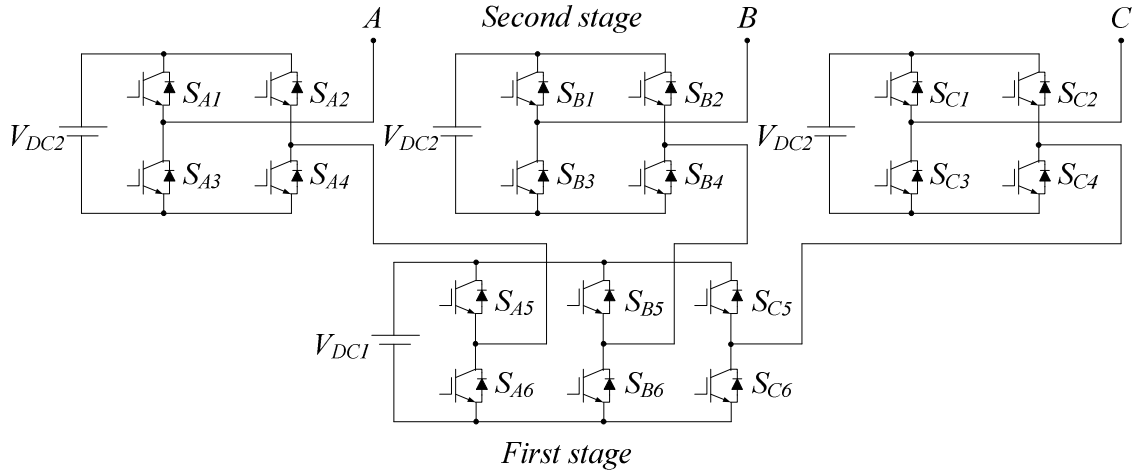


Figure 2.11: Hybrid inverter constructed from the series connection of the six-switch full-bridge inverter and the H-bridge inverters.

2.3.2.6 Multilevel DC Link Inverter

With the motivation to reduce the number of switches, clamping diodes or capacitors, multilevel inverter based on a multilevel DC link and a H-bridge inverter in each phase leg is introduced (Gui-Jia, 2005). The multilevel DC link can be formed by connecting a number of half-bridge cells in series as shown in Figure 2.12. Each cell consists of two switches that operate in complementary manner. The DC voltage of each cell is added or bypassed by turning on one switch and turning off the other switch simultaneously. The DC link voltage across nodes *M* and *O* is obtained by adding the voltages across each cell. To get a DC link voltage with the shape of the staircase across the two nodes, the switches in each cell must conduct according to different duty cycles at twice the frequency of the output voltage.

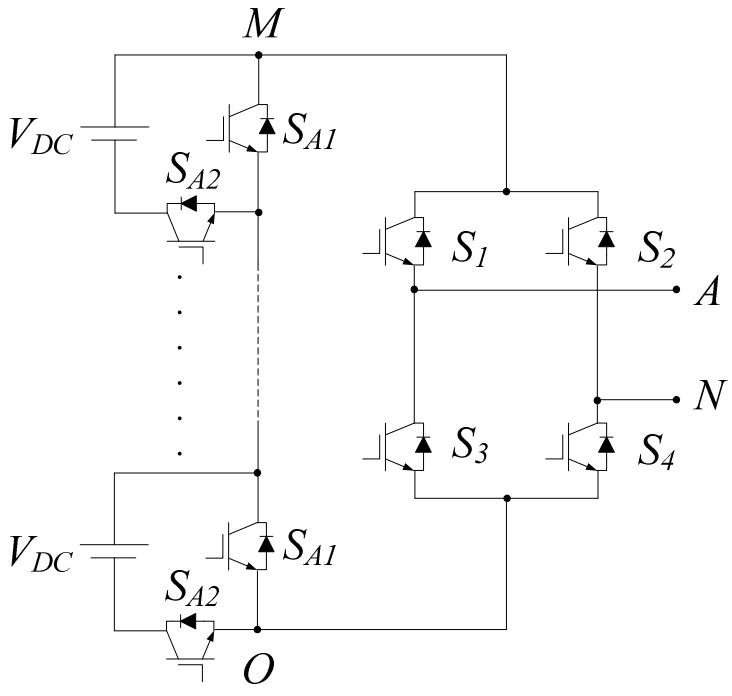
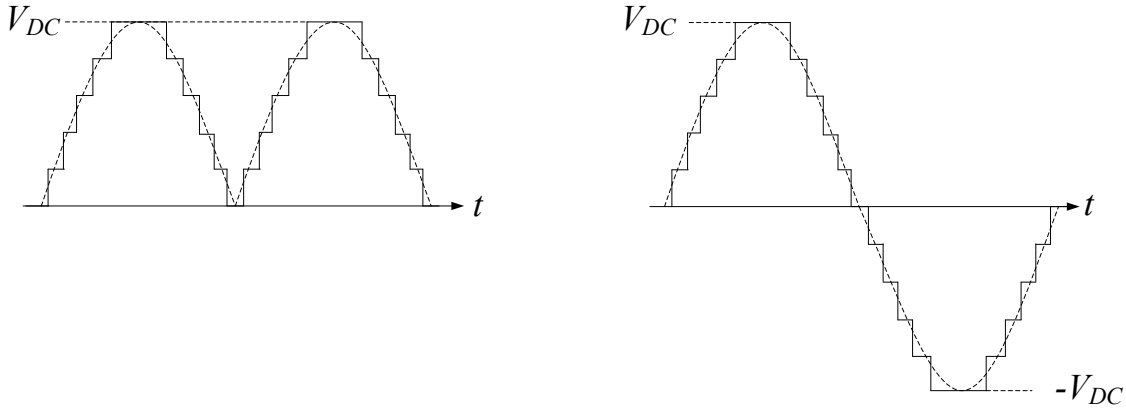


Figure 2.12: One phase leg of multilevel DC link inverter based on cascaded half-bridge cells.

The staircase voltage waveform of the DC link does approximate the rectified waveform of a commanded sinusoidal wave. To convert into an AC voltage, the H-bridge inverter is used to alternately change the polarity of the DC link staircase waveform at a frequency equals the frequency of the output voltage. Figure 2.13 presents the waveforms of the DC link, V_{MO} and the multilevel DC link inverter's output, V_{AN}. As the number of voltage levels m increases, the number of active switches also grows according to $m + 3$ per phase leg for the multilevel DC link inverter as compared to $2(m - 1)$ for the classic multilevel inverters.

Besides the series-connected half-bridge cells, the diode-clamped and flying-capacitor phase leg can also be utilized to provide the staircase DC link voltage. As an example, Figure 2.14 shows the multilevel DC link inverter based on the diode-clamped phase leg that is able to generate eleven voltage levels across nodes A and N. In addition, multilevel DC link inverter can also be employed using unequal voltage sources (Ramkumar, Kamaraj, Thamizharasan, & Jeevananthan, 2012). Despite the advantage of reducing the number of switches, the inverter also requires many separated DC sources. Capacitor voltage balancing is another issue to be tackled if the diode-clamped or the flying-capacitor phase leg is used.



(a) DC link voltage waveform, V_{MO} (b) Output voltage waveform, V_{AN}

Figure 2.13: The voltage waveforms of the DC link and inverter's output.

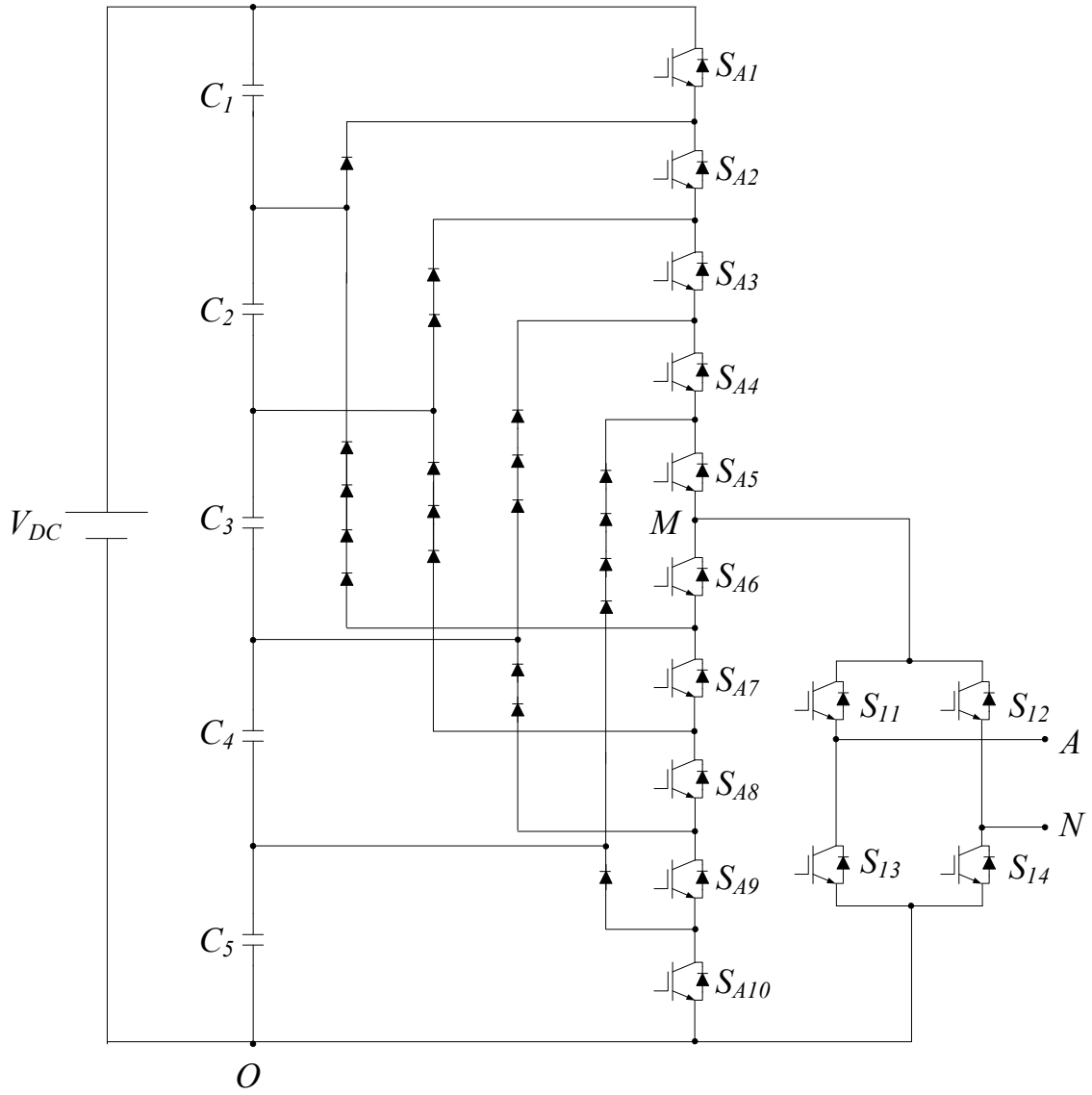


Figure 2.14: One phase leg of the diode-clamped-phase-leg-based multilevel DC link inverter.

2.3.2.7 Transistor-Clamped Multilevel Inverter

Transistor-clamped multilevel inverter is derived from the diode-clamped converter concept. Bidirectional switches are used to clamp the connection points between the main switches and capacitors in the transistor-clamped inverter, thus eliminating the use of clamping diodes. One type of the bidirectional switches used is given in Figure 2.15 (Dixon & Moran, 2006). The bidirectional switch is composed of

one transistor and four diodes. By adding one bidirectional switch of this sort to a single-phase H-bridge inverter in the arrangement shown in Figure 2.16, five voltage levels can be generated at the output (Ceglia, Guzman, Sanchez, Ibanez, Walter, & Gimenez, 2006; Sung-Jun, Feel-Soon, Man Hyung, & Cheul, 2003). The inverter has been further studied for photovoltaic applications (Selvaraj & Rahim, 2009). Further modification on the inverter produces a seven-level output voltage waveform by just adding another bidirectional switch (Rahim, Chaniago, & Selvaraj, 2011).

A three-phase version of the three-level transistor-clamped inverter is shown in Figure 2.17 (Guennegues, Gollentz, Meibody-Tabar, Rael, & Leclere, 2009). For this inverter, a different form of bidirectional switch is used. The switch comprises two transistors and two diodes. The structure of the inverter is similar to that of the equivalent NPC inverter. While the NPC inverter suffers from the unequal loss distribution among the devices, the transistor-clamped inverter is able to share the losses among the devices in a more balanced manner. This allows the inverter to operate at high switching frequency, thus makes it suitable for variable high-speed applications. However, more switches are required, which then lead to a significant rise in cost.

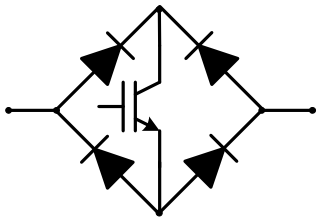


Figure 2.15: One type of a bidirectional switch.

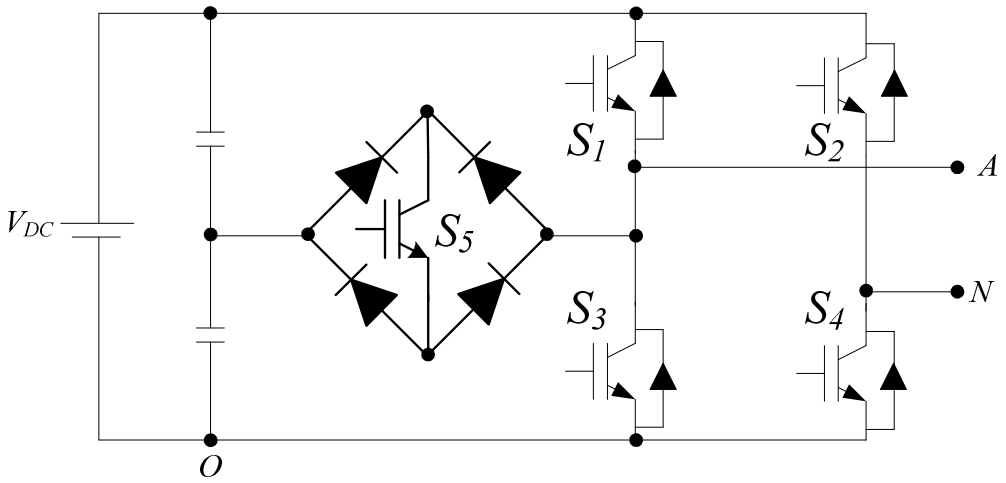


Figure 2.16: A single-phase transistor-clamped H-bridge inverter.

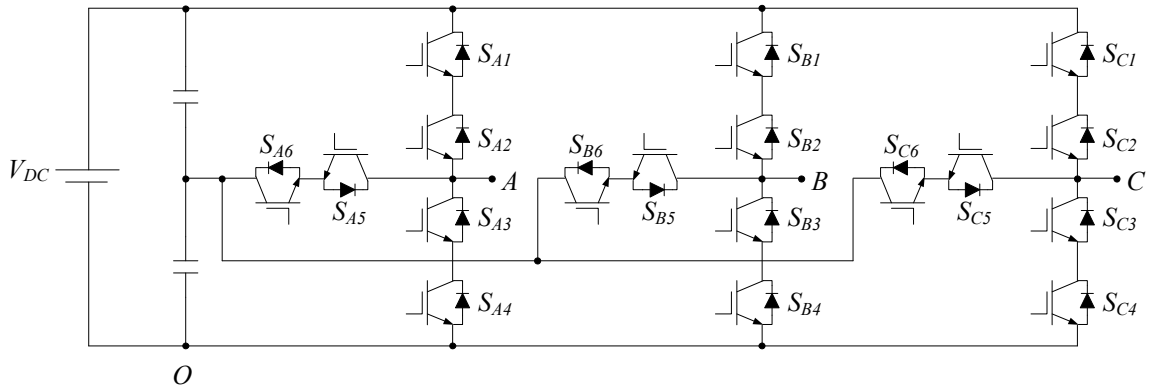


Figure 2.17: A three-phase three-level transistor-clamped inverter.

Recently, a cascaded multilevel inverter that uses transistor-clamped H-bridge cells has been proposed for medium voltage drive applications (Rahim, Elias, & Wooi Ping, 2013). The inverter has the advantage of producing less power loss as compared to the equivalent cascaded NPC inverter and the conventional nine-level cascaded H-bridge inverter when similar modulation method is applied. In spite of this advantage, the use of a complicated voltage balancing method is unavoidable.

2.4 Modulation Techniques

With the rapid development of multilevel inverter topologies in recent years, studies on modulation techniques have also intensified. As multilevel inverters experience an increasing number of devices when the number of voltage levels grows, the level of complexity of modulation techniques also increases since more devices are needed to be controlled. Despite the complexity faced, the extra switching states generated provide flexibility in developing the modulation technique in order to achieve not only one particular target but also many desired criteria such as low harmonic contents, low switching loss, voltage-balancing capability and so on.

Most modulation techniques for multilevel inverters are adapted from the traditional methods employed for the conventional two-level inverters. There are several ways to classify these techniques. One way of classification is by looking at the domain the modulation algorithms operate: the state-space vector domain that is based on the voltage vector generation, and the time domain that is based on the voltage level generation over a time frame (Franquelo, Rodriguez, Leon, Kouro, Portillo, & Prats, 2008). Another way of classification is by basing on the reference voltage type: the sampled reference, in which only the instantaneous reference amplitude is provided to the modulator, and the full-cycle reference, in which a sinusoidal output voltage is usually assumed, thus the amplitude, frequency and in some cases, the phase angle are provided to the modulator (Kadir, 2010). Besides the two ways of classification, the most common way mostly presented in the literature is the classification according to the switching frequency. 1-kHz boundary is usually used to differentiate between low and high switching frequency. Owing to the simplicity presented in defining the switching frequencies for easy understanding, this thesis describes the various modulation techniques based on their average operating switching frequency.

2.4.1 Low Switching Frequency Methods

Low switching frequency is generally defined to be below 1 kHz. It is commonly observed that the range of the low switching frequency employed is up to few multiples of the fundamental frequency. Low switching frequency methods are generally preferred for high power applications, owing to the switching loss reduction offered. The methods are also effective in cases in which a sufficiently high number of voltage levels are involved (Yu & Fang-Lin, 2008). In this thesis, three low switching frequency methods mostly discussed in the literature are presented.

2.4.1.1 Selective Harmonic Elimination

Selective harmonic elimination (SHE) method is basically designed to eliminate undesired low order harmonics through the appropriate choice of the switching angles (Holtz, 1994). The process in determining the desired switching angles normally involves Fourier series analysis. For a stepped voltage waveform comprising s number of steps with each step voltage equals V_s, the amplitude of any odd harmonics can be expressed as the following:

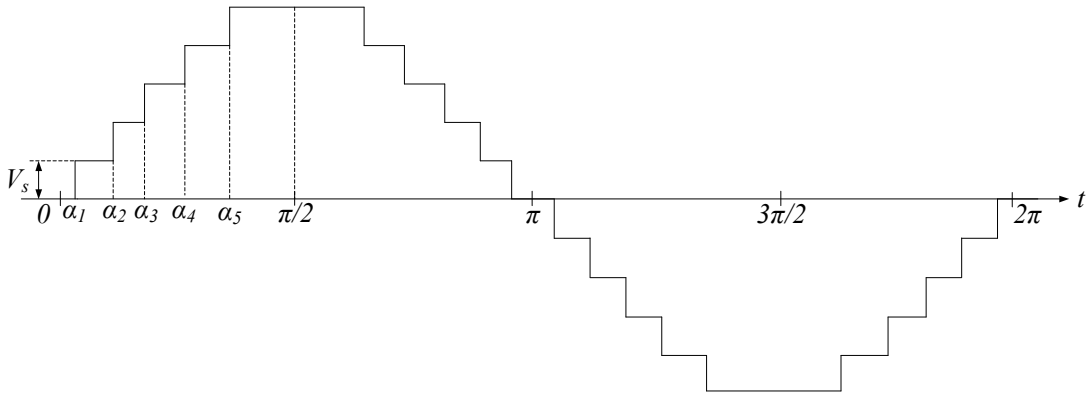


Figure 2.18: An 11-level stepped-voltage waveform.

$$H_n = \frac{4V_s}{n\pi}\left[\cos(n\alpha_1) + \cos(n\alpha_2) + ... + \cos(n\alpha_s)\right] \quad (2.5)$$

where H_n is the amplitude for harmonic n and the switching angles satisfy $\alpha_1 < \alpha_2 <$ ……. $< \frac{\pi}{2}$. By using equation (2.5), the harmonics that need to be eliminated can be set to zero. Usually, low order harmonics are chosen since they are the most significant ones that contribute more to THD. With the adequate number of equations, the desired or the optimum switching angles can be calculated.

Figure 2.18 shows a stepped waveform with eleven steps. For this waveform, four harmonics can be eliminated, namely the 5th, 7th, 11th and 13th. The 3rd harmonic and its multiples are not included since they are naturally canceled by the three-phase connection. The first harmonic refers to the fundamental component and is set to the desired modulation index, *M*. By applying equation (2.5), the following are obtained:

$$\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) + \cos(\alpha_4) + \cos(\alpha_5) = \frac{\pi}{4} \cdot M \quad (2.6)$$

$$\cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) + \cos(5\alpha_4) + \cos(5\alpha_5) = 0 \quad (2.7)$$

$$\cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) + \cos(7\alpha_4) + \cos(7\alpha_5) = 0 \quad (2.8)$$

$$\cos(11\alpha_1) + \cos(11\alpha_2) + \cos(11\alpha_3) + \cos(11\alpha_4) + \cos(11\alpha_5) = 0 \quad (2.9)$$

$$\cos(13\alpha_1) + \cos(13\alpha_2) + \cos(13\alpha_3) + \cos(13\alpha_4) + \cos(13\alpha_5) = 0 \quad (2.10)$$

The above set of equations is normally solved offline. Since these equations are nonlinear and transcendental, numerical methods such as Newton-Raphson method is used (Tolbert, Fang Zheng, & Habetler, 1999). Other methods have also been proposed such as those using genetic algorithms (Dahidah & Agelidis, 2005; El-Naggar & Abdelhamid, 2008; Ozpineci, Tolbert, & Chiasson, 2004) and theory of symmetric

polynomials and resultants (Chiasson, Tolbert, McKenzie, & Zhong, 2005). Particle swarm optimization has also been applied to eliminate harmonics in a cascaded multilevel inverter with unequal DC sources (Taghizadeh & Hagh, 2010). The results obtained from solving the equations provide the optimum switching angles needed to eliminate the abovementioned harmonics. For practical implementation, the switching angles are usually precalculated and then stored in a look-up table. Since online calculation of switching angles are preferable in any real-time applications, an algorithm to carry out real-time calculation with any look-up table has been proposed (Yu, Hoon, & Huang, 2009). For the case of varying DC sources with respect to time, artificial neural networks are employed to determine the switching angles that changes according to the variation in the real-time values of the DC sources (Filho, Maia, Mateus, Ozpineci, Tolbert, & Pinto, 2013).

Besides the great difficulty encountered in solving the transcendental equations, another drawback of SHE method is the fact that it only provides a narrow range of modulation index. To widen the modulation index range with low THD, a method known as optimized harmonic stepped waveform technique was proposed (Sirisukprasert, Jih-Sheng, & Tian-Hua, 2002). This method is an extension of the conventional SHE. The range of modulation index is divided into a number of levels. By introducing the modulation index levels, wide modulation index with low switching frequency and minimized harmonic distortion in the output waveform can be achieved. This technique has also been used with genetic algorithms to further improve the THD in a cascaded multilevel inverter with adjustable DC supplies (Yousefpoor, Fathi, Farokhnia, & Sadeghi, 2009).

2.4.1.2 Selective Harmonic Mitigation

Selective harmonic elimination technique is effective enough to fully remove a number of dominant low order harmonics that can significantly contribute to high harmonic distortion. However, the action of eliminating these harmonics somehow creates some side effects. It is reported that the elimination of the low order harmonics causes the harmonic energy to move to higher frequencies which results in the corresponding harmonic amplitudes to increase (Kouro, Malinowski, Gopakumar, Pou, Franquelo, Bin, Rodriguez, Perez, & Leon, 2010). This is not acceptable in some applications such as the grid-connected system. The increased awareness in the power quality of the grid has led to the introduction of more stringent grid codes that limit the amplitudes of the harmonics up to the 50th order. Although passive filters can be used to reduce the harmonic distortion into the grid, they are usually bulky and expensive.

It is more convenient to use an efficient modulation method to obtain output waveforms that can meet the grid regulations. A method known as selective harmonic mitigation (SHM) was proposed (Franquelo, Napoles, Guisado, Leon, & Aguirre, 2007). Instead of completely eliminating specific harmonics, this technique reduces the harmonic amplitudes so as to pass the grid code limits. Franquelo et al (2007) reported that it is possible to satisfy the grid code requirements of CIGRE WG 36-05 and EN 50160 by using SHM technique at a switching frequency of 750 Hz without any additional filtering system employed. Harmonics were successfully mitigated up to the 49th order. SHM technique has also been implemented for cascaded H-bridge converters with unequal DC voltages with ten switching angles per quarter cycle are used (Napoles, Leon, Franquelo, Portillo, & Aguirre, 2009). In another study (Napoles, Watson, Padilla, Leon, Franquelo, Wheeler, & Aguirre, 2013), SHM method based on the interpolation of different sets of angles obtained for specific imbalanced situations

of the DC link voltages in a cascaded H-bridge multilevel converter was presented. An optimal selective harmonic mitigation method applied to a single-phase seven-level cascaded H-bridge inverter with a switching frequency of 150 Hz was also investigated (Marzoughi, Imaneini, & Moeini, 2013). The method distributes the required number of switching angles between different voltage levels, which then reduces the switching frequency to the least possible. With this method, it is claimed that the requirements of grid codes EN 50160, CIGRE JWG C4.07 and IEC 61000-3-6 are able to be achieved.

To investigate the dynamic performance for a closed loop operation, a predictive control based SHM method was proposed (Aggrawal, Leon, Franquelo, Kouro, Garg, & Rodriguez, 2011). The control objectives of this method are to follow voltage reference, to control the low order harmonic distortion and to reduce the switching losses. Using the sliding discrete Fourier transform algorithm, the objectives are successfully achieved with very low switching frequency. Since the technique is computed online, an improvement in the dynamic performance is also accomplished. Another technique which is similar to the SHM known as the optimal minimization of THD is also proposed. The main objective of this technique is to minimize the waveform THD with the proper selection of switching angles by reducing most of the harmonics without eliminating them completely (Hosseini Aghdam, Fathi, & Gharehpetian, 2007). In one study (Yousefpoor, Fathi, Farokhnia, & Abyaneh, 2012), the THD minimization process uses genetic algorithms to improve the output voltages with less THD.

2.4.1.3 Voltage Vector Approximation

Voltage vector approximation or nearest vector control (Rodriguez, Franquelo, Kouro, Leon, Portillo, Prats, & Perez, 2009) is a low switching frequency method suitable for multilevel inverter that has a very high number of levels, usually above

seven. This method is based on the space vector theory. The space vector diagram generated in the $\alpha\beta$ plane is used to approximate a given reference vector to the closest voltage vector. In one study (Rodriguez, Correa, & Moran, 2001), voltage vector approximation is applied to an eleven-level inverter. The criterion used to select the approximated voltage vector is the space error or the distance between the closest vectors and the reference vector must be the minimum possible. This is to ensure that only the voltage vector that has the greatest proximity to the reference is always selected.

The presence of a large number of levels provides options for the voltage vector approximation method to reduce common mode voltage (Rodriguez, Pontt, Correa, Cortes, & Silva, 2004). Voltage vectors that can provide zero common mode voltage are only used for selection to approximate the reference vector. Rodriguez et al (2004) has developed a simple algorithm to select the most appropriate vector with zero common mode voltage that can imitate the reference vector. This method has then been adapted for a multilevel inverter that is able to produce 81 voltage levels with zero common mode voltage (Yu & Fang-Lin, 2008). Another method which is quite similar to the voltage vector approximation known as voltage level approximation or nearest level control has also been proposed (Perez, Rodriguez, Pontt, & Kouro, 2007). Instead of the nearest voltage vector, this method selects the nearest voltage levels to approximate the desired output voltage reference. Like the voltage vector approximation, the voltage level approximation method is only effective if a sufficiently high number of levels exist.

The main advantage of the voltage vector approximation method is the implementation simplicity and the high efficiency offered. However, it is only suitable

when the number of levels is high enough which then provides a high density of voltage vector availability. When such a condition is achieved, better approximation can be attained with smaller error between the nearest vector and the reference. From the perspective of harmonic minimization, the method is not designed to serve such a purpose. No low order harmonics are eliminated or reduced, thus their harmful effects remain.

2.4.2 High Switching Frequency Methods

For high power applications, high switching frequency is considered to begin from 1 kHz. Modulation methods that employ high switching frequency are suitable for multilevel inverters with low number of voltage levels. In the presence of high number of levels, these methods can also be applied but at the expense of increased complexity. Generally, the better output power quality and the higher bandwidth offered make the high switching frequency methods attractive for high dynamic range applications (Franquelo, Rodriguez, Leon, Kouro, Portillo, & Prats, 2008). There are a number of methods that use high switching frequency in which some of the popular ones are explained in the following subsections.

2.4.2.1 Multicarrier PWM

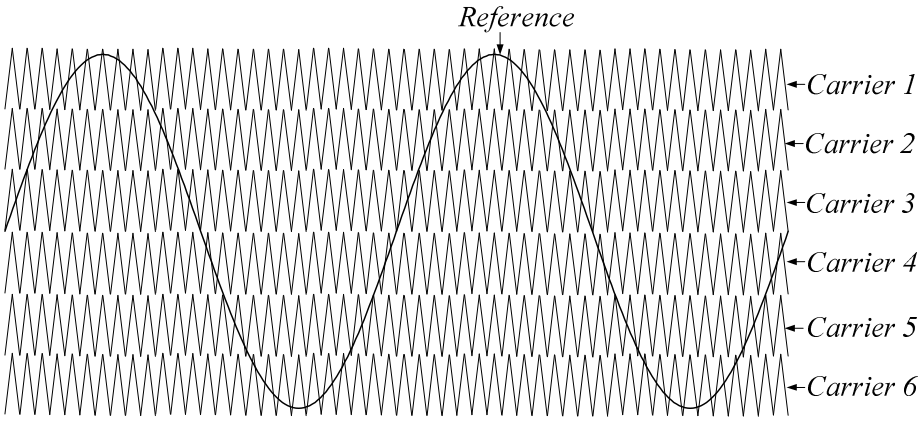
Multicarrier PWM method is basically derived from the classical sinusoidal PWM method. In this method, high frequency multicarrier signals are used and compared with a low frequency sinusoidal reference signal to generate the switching signals for the power switches. There are two categories of multicarrier PWM that are characterized by the way the carriers are arranged. For a vertical arrangement of carriers in which each carrier is set in between two voltage levels, the category is known as

level-shifted PWM. Another category known as phase-shifted PWM arranges the carriers horizontally in which a phase shift is introduced between two carriers.

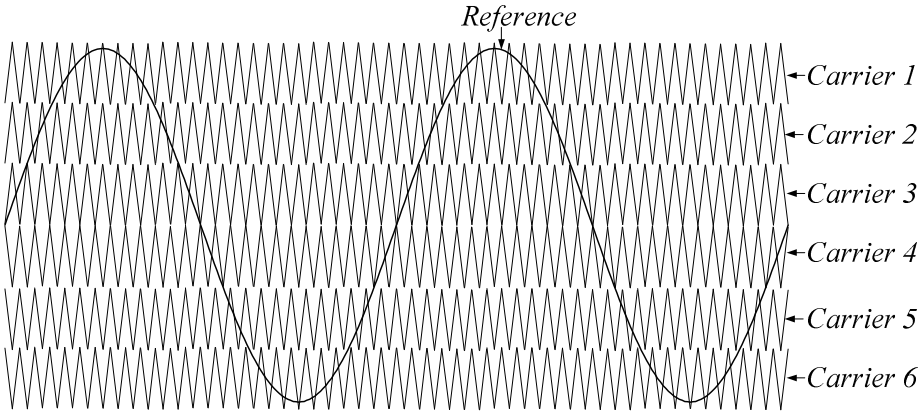
Level-shifted PWM method is particularly suitable for diode-clamped inverter since each carrier signal can be easily related to each power switch (Franquelo, Rodriguez, Leon, Kouro, Portillo, & Prats, 2008). For *m*-level diode-clamped inverter, $m - 1$ triangular carriers of the same frequency and amplitude are required to completely occupy the peak-to-peak amplitude of the reference signal which is generally a sinusoidal waveform. The reference and carrier signals are continuously compared with each other. When the reference is greater than the carrier, then the power switch associated with this carrier is turned on. If the opposite takes place, then the power switch corresponding to the carrier is turned off. The disposition of the carrier can be divided into three (Carrara, Gardella, Marchesoni, Salutari, & Sciutto, 1992; McGrath & Holmes, 2002), namely:

1. Phase disposition (PD) where all carriers are in phase.
2. Phase opposition disposition (POD) where the carriers above the sinusoidal reference zero point are 180° out of phase with those below the zero point.
3. Alternative phase opposition disposition (APOD) where each carrier is phase-shifted by 180° from its adjacent carrier.

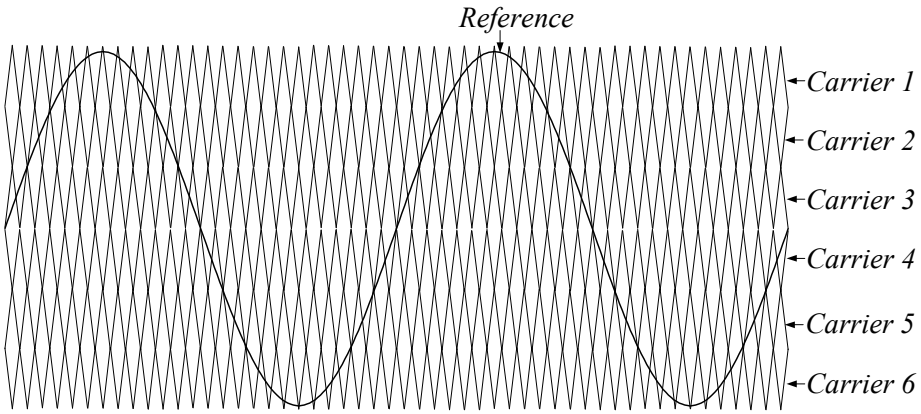
Figure 2.19(a) – (c) show the three carrier dispositions for a seven-level inverter. A comparative analysis has been done and the results showed that for POD and APOD, no harmonics exist at the carrier frequency but odd order harmonics exist at each sideband. For PD, harmonics exist at the carrier frequency and odd multiples of it (Carrara, Gardella, Marchesoni, Salutari, & Sciutto, 1992). Using analytical approach through double Fourier analysis, it has been identified that PD modulation has a better



(a) Phase disposition (PD).

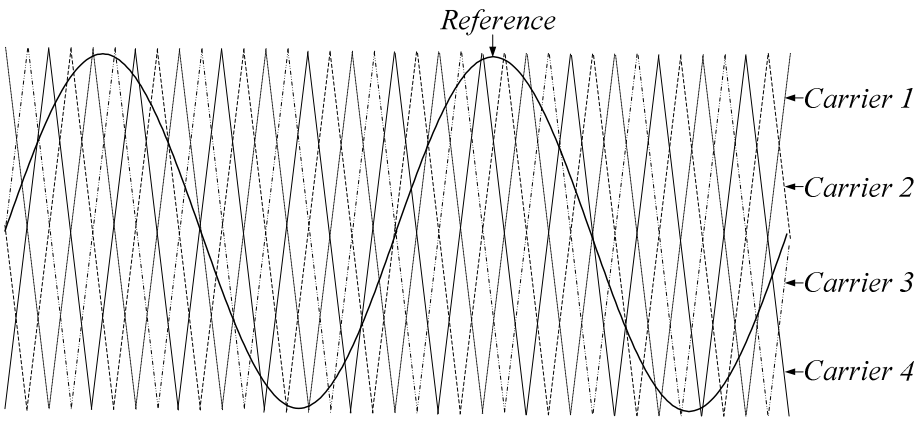


(b) Phase opposition disposition (POD).



(c) Alternative opposition disposition (APOD).

Figure 2.19: Carrier arrangements of level-shifted and phase-shifted PWM.



(d) Phase-shifted PWM.

Figure 2.19, continued: Carrier arrangements of level-shifted and phase-shifted PWM.

line-to-line harmonic performance compared to APOD modulation (McGrath & Holmes, 2002). Owing to this superiority, PD modulation has been applied to flying-capacitor inverters (McGrath, Meynard, Gateau, & Holmes, 2007). In another study, the strength of the POD modulation in terms of the differential mode of phase currents has also been integrated into the PD strategy and has been investigated with parallel multilevel inverters (Cougo, Gateau, Meynard, Bobrowska-Rafal, & Cousineau, 2012). Based on the improvement of PD modulation, higher and lower carrier cells alternative phase opposition PWM has been proposed for hybrid-clamped multilevel inverters (Z. Jing, Xiangning, & Zhao, 2010). This method is able to reduce the switching losses and lower harmonic amplitudes quite remarkably.

Modification done on the reference signal with the addition of zero-sequence, triplen harmonic voltage introduces a method known as switching frequency optimal PWM (SFO-PWM) (Menzies, Steimer, & Steinke, 1994). This method increases the maximum output voltage by 15% before overmodulation occurs. To balance the switching speed among all the switches in a NPC inverter, the frequency of several

carriers are made to be different, viz, the top and bottom carrier bands have lower frequency as compared to the others (Tolbert & Habetler, 1999).

While level-shifted PWM is more suitable for diode-clamped inverter, the phase-shifted PWM is specially conceived for flying-capacitor and cascaded H-bridge inverters (Rodriguez, Franquelo, Kouro, Leon, Portillo, Prats, & Perez, 2009; Yiqiao & Nwankpa, 1998). Figure 2.19(d) displays the carrier arrangement for phase-shifted PWM method for a five-level inverter. Using this method, for an inverter with *m* cells, a carrier phase shift of $\frac{180°}{m}$ for the cascaded H-bridge topology and of $\frac{360°}{m}$ for the flying-capacitor topology is introduced across the cells to generate stepped output waveform with the lowest distortion (Franquelo, Rodriguez, Leon, Kouro, Portillo, & Prats, 2008). The advantage of this method is power distribution among the cells is evenly distributed. This provides a way to reduce input current harmonics in the cascaded H-bridge inverter through the use of multipulse diode rectifiers. For the case of flying-capacitor inverter, this avoids voltage unbalance since natural balancing is possible (Wilkinson, Meynard, & Du Toit Mouton, 2006). As compared to the PD method, the phase-shifted PWM contributes to more distorted line voltages (McGrath & Holmes, 2002). Nonetheless, the differences between the two methods are too small for high frequency harmonic orders which are normally filtered by the load (Kouro, Malinowski, Gopakumar, Pou, Franquelo, Bin, Rodriguez, Perez, & Leon, 2010).

2.4.2.2 Space Vector PWM

Space vector PWM (SVPWM) method originates from the concept of describing the switching states of the inverter using vector representations known as voltage vectors or state vectors. Since each switching state provides information about discrete output voltages, a relationship can then be established between the voltage vectors and

the output voltages. This relationship is given as follows (Rodriguez, Franquelo, Kouro, Leon, Portillo, Prats, & Perez, 2009):

$$V_{vec} = \frac{2}{3}\left[V_{AN} + aV_{BN} + a^2 V_{CN}\right] \tag{2.11}$$

where $a = -\left(\frac{1}{2}\right) + \left(j\frac{\sqrt{3}}{2}\right)$ (2.12)

V_{vec} is the voltage vector and V_{AN}, V_{BN} and V_{CN} are the phase output voltages. By using equation (2.11), the values of the three phase variables from the *ABC*-plane can be mapped to a unique voltage vector in the *αβ*-plane. For a three-phase three-level inverter, three switching states can be derived for each phase. Therefore, this results in 3^3 = 27 switching state combinations. Using equation (2.11), the 27 switching state combinations are reduced to 19 voltage vectors in which several vectors represent more than one switching state combinations. Basically, these vectors can be grouped into four categories, depending on the amplitude as shown in Figure 2.20. It can seen that zero vector has three switching state combinations, small-magnitude vectors represent two combinations each, while medium- and large-magnitude vectors correspond to one combination each. Fig. 2.21 portrays the overall space vector diagram. The vectors with more than one combination are said to have redundant switching states which can be useful to achieve a certain target.

To implement the PWM switching, a reference voltage vector of a particular length is used to rotate on the *αβ*-plane. The speed of rotation determines the inverter output frequency while the vector length affects the number of voltage levels produced. In a conventional SVPWM algorithm, at least three steps are involved. The first step is to identify a set of voltage vectors that can represent the reference vector at a particular point in the *αβ*-plane. In general, three nearest vectors to the reference are selected so as

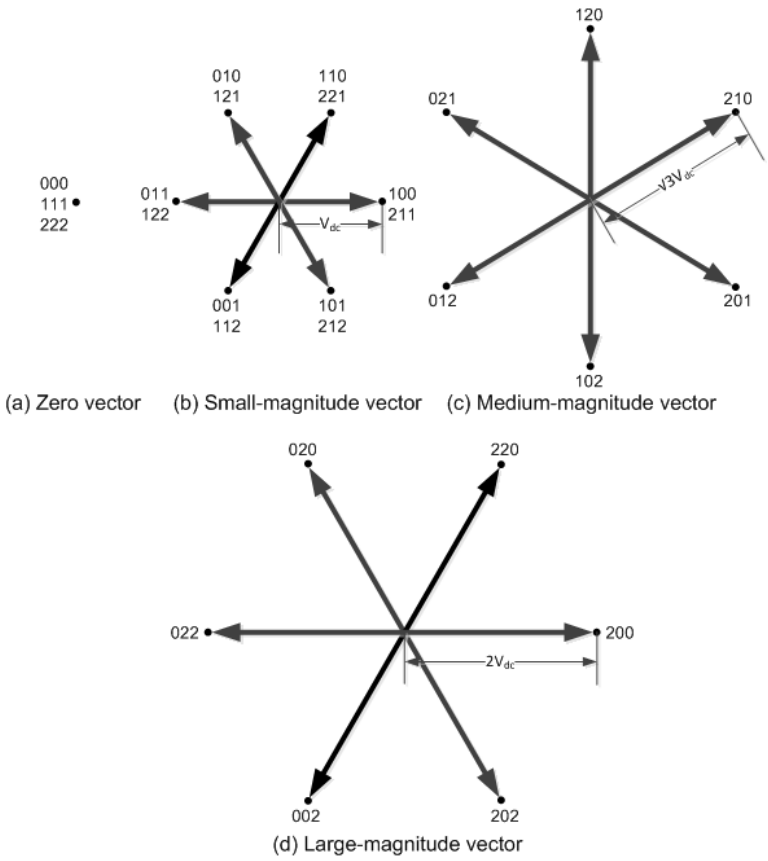


Figure 2.20: Four space vector categories for a three-phase three-level inverter (V_{dc} is the voltage across each DC link capacitor).

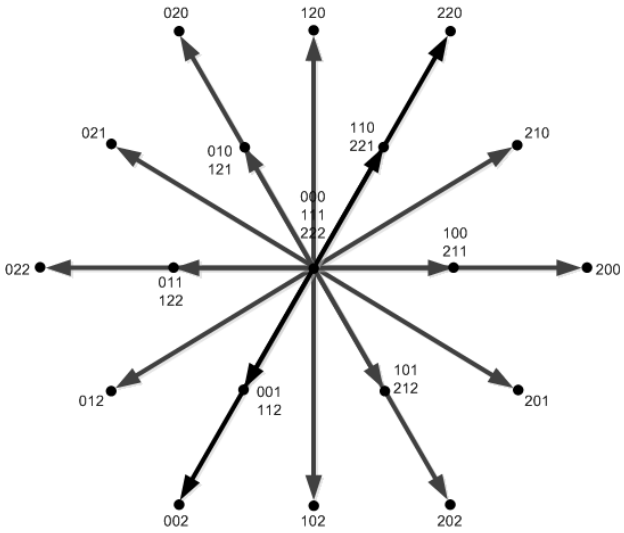


Figure 2.21: All voltage vectors on a common $\alpha\beta$-plane for a three-phase three-level inverter.

to minimize the harmonic components of the output line-to-line voltages (Liu, Choi, & Cho, 1991). Figure 2.22 illustrates the three nearest vectors. The second step is to compute the on-state time of each nearest vector to obtain the reference vector over a sampling period. If the V_1, V_2 and V_3 are the three nearest vectors for the reference vector V_{ref}, and the sampling period is given by T_s, then the corresponding on-state time of the nearest vectors which are denoted by T_1, T_2 and T_3 respectively can be determined by solving the following equations:

$$V_{1,\alpha}T_1 + V_{2,\alpha}T_2 + V_{3,\alpha}T_3 = V_{ref,\alpha}T_s \tag{2.13}$$

$$V_{1,\beta}T_1 + V_{2,\beta}T_2 + V_{3,\beta}T_3 = V_{ref,\beta}T_s \tag{2.14}$$

$$T_1 + T_2 + T_3 = T_s \tag{2.15}$$

The subscripts α and β in equations (2.13) and (2.14) refer to vector component in α-axis and β-axis respectively. The third step is to select the appropriate switching state sequence in which the vectors are generated. In most cases, the center-distributed or symmetric sequences are employed owing to the synchronous digital sampling of the current (Kouro, Malinowski, Gopakumar, Pou, Franquelo, Bin, Rodriguez, Perez, & Leon, 2010).

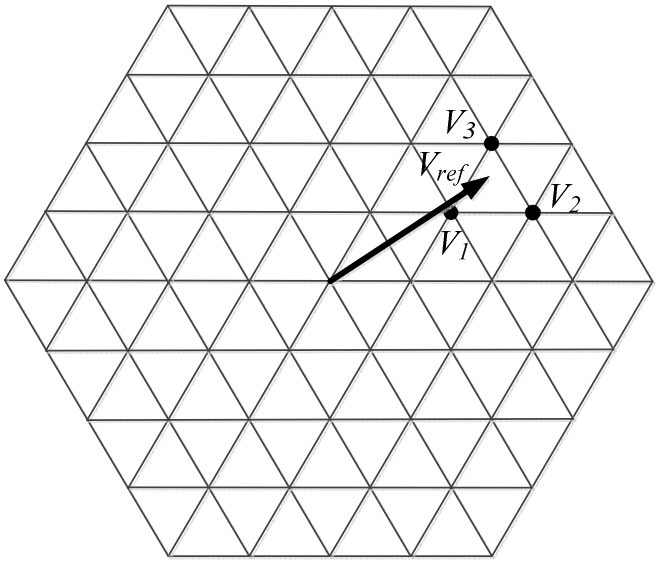


Figure 2.22: Three nearest vectors.

Many studies have been conducted on the SVPWM methods with many different goals to achieve. One of those goals is the reduction in implementation complexity. In one study (Sanmin, Bin, Fahai, & Congwei, 2003), a 60° coordinate transformation or *gh* coordinate system is proposed to simplify the computation of the on-state time of the nearest vectors. This coordinate system has two axes in which one of them is in horizontal position (*g*-axis), while the other (*h*-axis) is inclined at an angle of 60° from the horizontal axis. Through the *gh* transformation, all voltage vector coordinates are converted into fixed-point values which are critical to reduce the time spent to do computation in real time. Another study proposes a fast and simple method based on simple geometrical considerations to provide online computation of the nearest vectors as well as their on-state durations without trigonometric functions calculations, look-up tables or coordinate systems transformation (Prats, Portillo, Carrasco, & Franquelo, 2002). A general computationally-efficient space vector algorithm that is independent of the number of voltage levels has also been reported (Celanovic & Boroyevich, 2001). The computational efficiency offered makes this algorithm attractive for execution in real time using any commercially available DSP. Another method that attempts to ease the implementation complexity, uses two-level modulation to calculate the on-state times and applies simple mapping for implementation in a multilevel inverter (A. K. Gupta & Khambadkone, 2006).

Besides the attempts to simplify the implementation of SVPWM, there are also studies conducted to utilize the redundant switching state combinations for capacitor voltage balancing. One of those studies proposes a closed loop control scheme based on the switching state redundancy that has the capability of maintaining the capacitor voltage balance through certain corrective actions initiated during different dynamic operating conditions of an induction motor drive (Tekwani, Kanchan, & Gopakumar, 2007a).

Another study presents an analytical-based generalized space vector algorithm that also demonstrates the use of redundant paths for capacitor balancing (Massoud, Finney, & Williams, 2008). Redundant switching states are also used to optimize switch utilization as reported in another study (Dae-Wook, Yo-Han, Bum-Seok, Chang-Ho, & Dong-Seok, 2003). A carrier-based SVPWM scheme is proposed to make use the voltage redundancies for redistribution of triangular carrier waves in order to achieve even utilization of switches. The concept of carrier-based SVPWM is mooted from the idea that the conventional space vector modulation scheme can be equivalently realized by the carrier-based PWM scheme with a proper common mode injection is added to the sinusoidal reference (Fei, 2002; Keliang & Danwei, 2002). By using this method, the need to determine the nearest vectors, duty ratios and switching state sequence as in the conventional space vector scheme can be avoided. At the same time, the superiority of the conventional SVPWM in providing higher DC voltage utilization and lower switching losses as compared to the carrier-based PWM is maintained in the method.

For a single-phase multilevel inverter, one-dimensional space vector modulation method known as 1DM that is based on the generation of the reference phase voltage as an average of two nearest voltage levels has been reported (Leon, Portillo, Vazquez, Padilla, Franquelo, & Carrasco, 2008). By using simple geometrical properties and calculations, the search for the two nearest switching states which in fact represent the two nearest voltage levels, and the determination of the switching sequence and the corresponding duty cycles are carried out with much ease, independent of the number of levels of the inverter. Owing to the simple calculations performed, the computational burden is then very low. Such a method has been applied to a three-phase inverter and it has been shown that this method is equivalent to the conventional space vector modulation, but with low computational complexity (Leon, Vazquez, Sanchez, Portillo,

Franquelo, Carrasco, & Dominguez, 2010). The success of this demonstration may make way for the use of this method for inverters with any number of phases and levels since the extension of this single-phase modulator can be easily done.

Among the various studies conducted on the SVPWM which are mostly concentrated on hexagonal structures, there are also investigations done on non-hexagonal space vector structures. In one study, 12-sided polygonal voltage vectors can be realized with an open-end induction motor drive whose both ends of the three-phase windings are fed by two separate inverters of the DC link voltages follow 1 : 0.366 ratio (Mohapatra, Gopakumar, Somasekhar, & Umanand, 2003). Using the 12-sided polygonal SVPWM method, the elimination of $6n \pm 1$ ($n = 1, 3, 5, \ldots$) harmonics, together with the suppression of the 11th and 13th order harmonics are possible. Further improvements have been made in the following study with the achievement of the additional boost in the fundamental phase voltage through the use of three two-level inverters in a cascaded arrangement with asymmetric DC links (Lakshminarayanan, Kanchan, Tekwani, & Gopakumar, 2006). The use of the 12-sided polygonal space vector modulation has then been further deepened in the subsequent studies to achieve various goals such as reduction in switching frequency, device ratings and *dv/dt* stress (Das, Sivakumar, Ramchand, Patel, & Gopakumar, 2009b), common mode voltage elimination (Lakshminarayanan, Mondal, Tekwani, Mohapatra, & Gopakumar, 2007), improved motor current harmonic profile to minimize the torque ripple (Das, Sivakumar, Ramchand, Patel, & Gopakumar, 2009a) and improved current THD (Mathew, Mathew, Azeez, Rajeevan, & Gopakumar, 2013).

Non-hexagonal space vector structure can also be formed when multiphase inverters are employed. For a five-phase two-level inverter, $2^5 = 32$ voltage vectors are generated in which two of them are zero vectors. These vectors are generated using $\alpha\beta$

transformation with five quantities (De Silva, Fletcher, & Williams, 2004). The transformation results in the formation of two vector spaces: the main space produces the fundamental component of the voltage and the auxiliary space creates third harmonic voltages embedded in the fundamental. Each vector space has three 10-sided polygons or decagons of different sizes that are formed by the voltage vectors. The presence of the auxiliary vector space that causes harmonic distortion in the five-phase system, leads to the difficulty in generating sinusoidal output voltages. The solution to this problem is proposed by combining the utilization of large and medium length neighboring space vectors in an appropriate manner to cancel the vectors in the auxiliary vector domain so that sinusoidal output voltages can be produced (De Silva, Fletcher, & Williams, 2004). To enable full utilization of DC voltage, some modifications have been made to the abovementioned solution in the subsequent study (Iqbal & Levi, 2005). Different methods have also been applied for multiphase inverter such as multilevel multiphase space vector algorithm based on two-level multiphase modulator (Lopez, Alvarez, Doval-Gandoy, & Freijedo, 2008) and multi-dimensional SVPWM which avoids vector space decomposition process (Duran & Levi, 2006; Lopez, Alvarez, Doval-Gandoy, & Freijedo, 2009).

For systems whereby zero sequence components of currents and voltages exist, three-dimensional space vector modulation methods (3D-SVM) are then proposed (Prats, Franquelo, Portillo, Leon, Galvan, & Carrasco, 2003). In addition to the α- and β-axes, γ-axis is also introduced to form the three dimensional space vectors. In this method, the cube and subcube where the reference vector lies, is identified. Since each subcube is divided into six tetrahedrons, then the corresponding tetrahedron that contains the reference vector is determined. The four vertexes of the tetrahedron are then considered as the four nearest vectors. Further calculations are then carried out to determine the duty

cycles and switching sequence. 3D-SVM is basically useful for unbalanced systems with or without neutral, with unbalanced load and with triplen harmonics (Rodriguez, Franquelo, Kouro, Leon, Portillo, Prats, & Perez, 2009). An example of such a system can be seen in the multilevel four-leg four-wire inverters which are applied to active power filters to compensate for harmonics and zero sequence components. The use of 3D-SVM with low computational cost for such inverters has been reported (Franquelo, Prats, Portillo, Galvan, Perales, Carrasco, Diez, & Jimenez, 2006). Despite the advantage of providing information on zero sequence components, 3D-SVM increases complexity to the modulation algorithm.

2.4.3 Hybrid Modulation Methods

Hybrid modulation methods basically involve mixed-switching frequencies. The methods were originally introduced for cascaded H-bridge inverters with unequal DC sources (Manjrekar & Lipo, 1998). Since each cell in a cascaded H-bridge inverter is not identical, the power rate of each cell differs from one to another. Hence, it is possible to use different switching frequencies among the cells. For high-power cells, low switching frequency is employed so that square waveform patterns are generated. PWM switching which occurs at much higher frequency is only utilized for low-power cells. In this way, switching losses of the inverter can be reduced, thus improving overall efficiency.

The basic principle of the hybrid modulation method can be explained with the aid of the control block diagram portrayed in Figure 2.23. Three stages of modulation are introduced. The first-stage control cell of high power compares a sinusoidal reference V_{ref} with specific maximum and minimum voltage levels at fundamental switching frequency to generate a square waveform V_{A1}. The difference between V_{ref} and

V_{A1} that represents the unmodulated part from the first stage, $V_{ref,2}$ is then used as the input for the second stage. Further comparison is done at the second-stage control cell of lower power at low switching frequency to produce the second-stage square waveform V_{A2}. The last unmodulated part from the second stage, $V_{ref,3}$ is then fed to the third-stage PWM cell of the lowest power which involves high switching frequency to generate the PWM waveform, V_{A3}. Summation of V_{A1}, V_{A2} and V_{A3} leads to the generation of the total output voltage, V_{AN}.

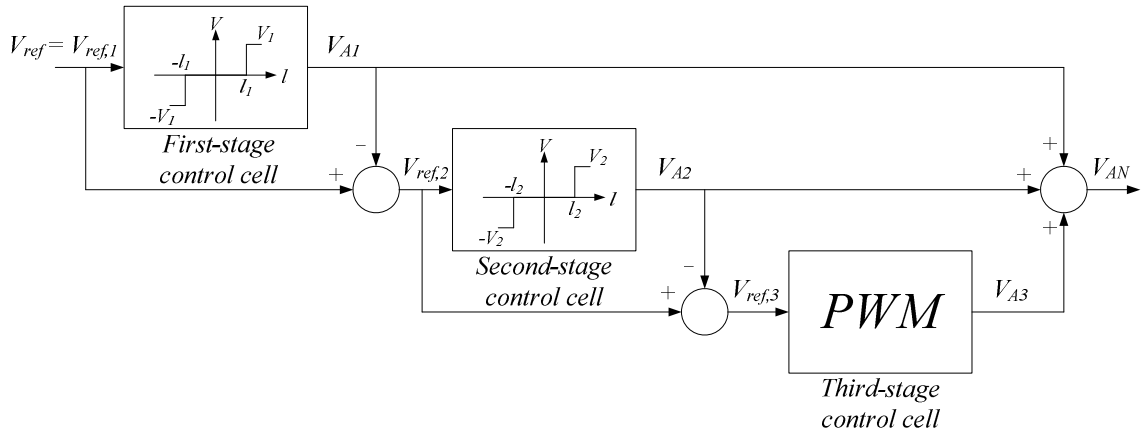


Figure 2.23: Hybrid modulation method.

For a cascaded H-bridge inverter with unequal DC sources, to achieve a maximum number of output levels, it is proposed that the optimal symmetry that should be employed for a three-cell inverter is $V_{DC1} : V_{DC2} : V_{DC3} = 1 : 2 : 6$ (Rodriguez, Bernet, Bin, Pontt, & Kouro, 2007). Further investigations have been conducted on several hybrid topologies with various number of cells and several design considerations have been proposed including those related to hybrid modulation (Rech & Pinheiro, 2007a). A detail analysis of the impact of the hybrid multilevel modulation strategy on the harmonic content of the input currents and output voltages have also been carried out (Rech & Pinheiro, 2007b). Modifications have been proposed to improve the input harmonic performance of adjustable speed drives by eliminating undesirable low

frequency harmonics from input currents in all operating ranges. Another study investigates a situation when the load consumes active power which causes some power cells to operate in regeneration mode (Espinosa, Espinoza, Melin, Ramirez, Villarroel, Munoz, & Moran, 2013). To overcome this problem, a new hybrid modulation technique has been proposed for a 13-level asymmetric inverter that ensures unidirectional power flow in every power cell. In one hybrid modulation method, selective harmonic elimination is applied for high-power cells and level-shifted multilevel PWM is employed for low-power cells (Adam, Abdelsalam, Finney, Holliday, Williams, & Fletcher, 2013). Triplen harmonic injection is also exploited to reduce semiconductor losses by minimizing the number of H-bridge cells and to enhance the cell capacitor voltage balancing.

2.5 Current Control Techniques

Current control techniques play an important role in determining the level of performance of an inverter system. A system is considered to perform well if it is able to meet certain desired criteria such as low harmonic distortion of the output current, high dynamic response, good DC voltage utilization, small current ripple and limited or constant switching frequency to ensure safe operation of the power devices (Kazmierkowski & Malesani, 1998). In some cases, the ability to provide bidirectional power flow is also an advantage to the system (Serpa, 2007). The main task of a current control scheme is to direct the actual currents to be as close as possible to the reference currents. In the ideal case, the actual and reference currents are desired to be similar in terms of phase and amplitude without any difference. Nonetheless, in the real world, the difference always exists and is usually noted as the current error.

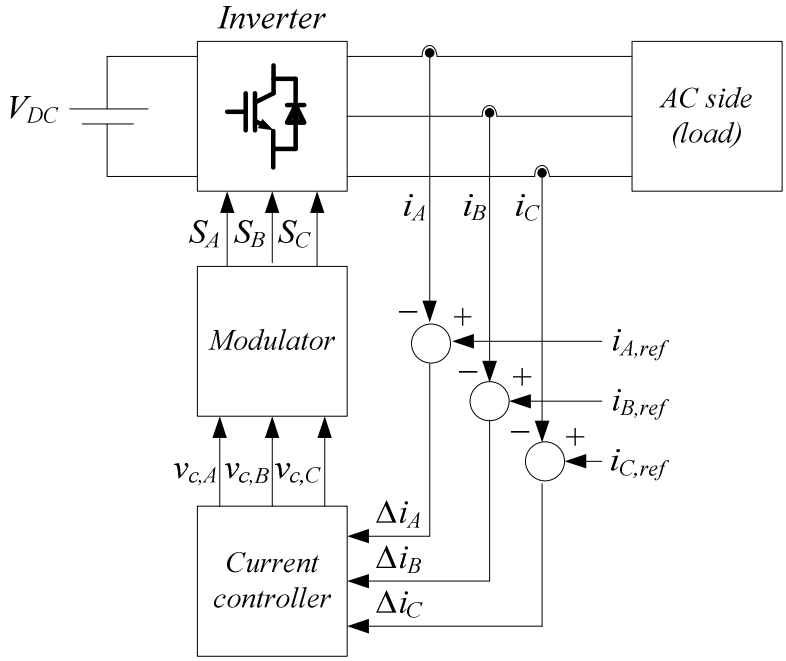


Figure 2.24: General current control scheme.

Figure 2.24 portrays the block diagram of a general current control scheme. The feedback path in the figure provides the measured output currents i_A, i_B and i_C for comparison with the desired output currents, $i_{A,ref}$, $i_{B,ref}$ and $i_{C,ref}$ respectively. The difference between the measured and desired currents which denotes the current errors Δi_A, Δi_B and Δi_C, are then sent to the current controller for processing to generate control signals $v_{c,A}$, $v_{c,B}$ and $v_{c,C}$. Next, the modulator uses the control signals to produce the switching states S_A, S_B and S_C for the power switches of the inverter. Based on the switching states, the inverter operates in such a way that the output currents always try to follow their references closely so that the current errors are always within the allowable limits. These limits are preferably to be near to zero. There are many current control schemes reported in the literature in which some of the major ones are briefly discussed in this section.

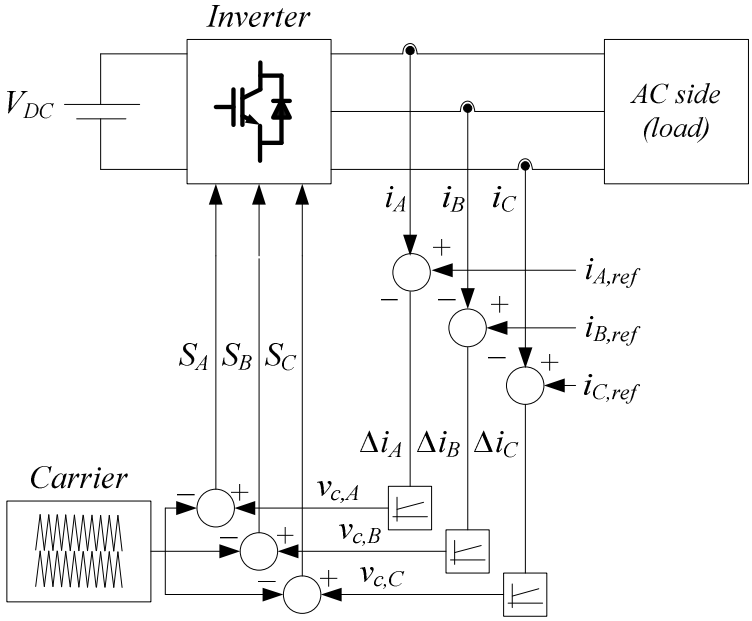


Figure 2.25: Ramp-comparison current control scheme.

2.5.1 Ramp-Comparison Control

Ramp-comparison control scheme basically employs carrier-based modulation to generate the switching states. Figure 2.25 shows the ramp-comparison control scheme. In this control scheme, proportional-integral (PI) controllers are used to receive the current errors Δi_A, Δi_B and Δi_C and then to generate the control signals $v_{c,A}$, $v_{c,B}$ and $v_{c,C}$. These control signals act as modulating signals which are next used for comparison with triangular carrier signals. The results of the comparison provide the switching signals S_A, S_B and S_C for the inverter switches. The switches are activated to produce positive output voltages when the modulating signals are higher than the carrier signals. On the other hand, when the modulating signals are lower than the carrier signals, then the switches are activated to generate negative output voltages instead.

The PI controller plays a crucial role in minimizing errors through the integral part and in controlling the amount of ripple via the proportional gain and zero placement (Kazmierkowski & Malesani, 1998). Therefore, the design of the PI controller has to be

carried out with several considerations have to be taken into account. The gain has to be properly limited so that the slope of the modulating signals does not exceed the triangular signal slope. This is to avoid multiple crossings that can contribute to an increase in the switching frequency and switching losses. At the same time, the gain cannot be too low so that the tracking error does not become too big.

The switching frequency of the inverter follows that of the carrier signal, thus it is constant. The produced harmonics are then defined at a fixed frequency. Proper selection of the carrier frequency is crucial as inappropriate frequency can also lead to multiple crossing problem. An analytical approach to select a proper carrier frequency has been described in one study (Srikanthan & Mishra, 2008). In addition, there is also inherent amplitude and phase error since the PI controller has to process AC signals (Serpa, 2007). This leads to a transmission delay in the system. Moreover, the system response is also influenced by the feedback path which is highly dependent on load parameters. There is also a zero voltage vector applied to the load which causes the load to be disconnected at several instants over the fundamental period of the output voltage (Azizur Rahman, Radwan, Osheiba, & Lashine, 1997). Nonetheless, a solution has been proposed with the use of three 120° phase-shifted triangular carriers. The implementation of ramp-comparison has been described in various studies. In one study, a digital PI controller has been implemented on a DSP to realize a ramp-comparison control scheme for grid-connected applications (Chaniago, Selvaraj, & Rahim, 2008).

2.5.2 Hysteresis Control

Unlike ramp-comparison control, hysteresis current control scheme is independent of load parameter changes (Kazmierkowski & Malesani, 1998). In this scheme, hysteresis comparators are used to process the current errors and then directly

generate the switching signals of the power switches, as depicted in Figure 2.26. Each hysteresis comparator has a predefined tolerance boundary around the reference current known as the hysteresis band which is used to guide the measured current to be always within the range specified by the band. Since the switching signals are produced from direct comparisons in the hysteresis comparators that can lead to fast responses, the dynamic performance is then excellent. The fact that this scheme is based on a simple concept makes it easy to implement practically. The scheme is also robust and lack of tracking errors as well (Kazmierkowski & Malesani, 1998).

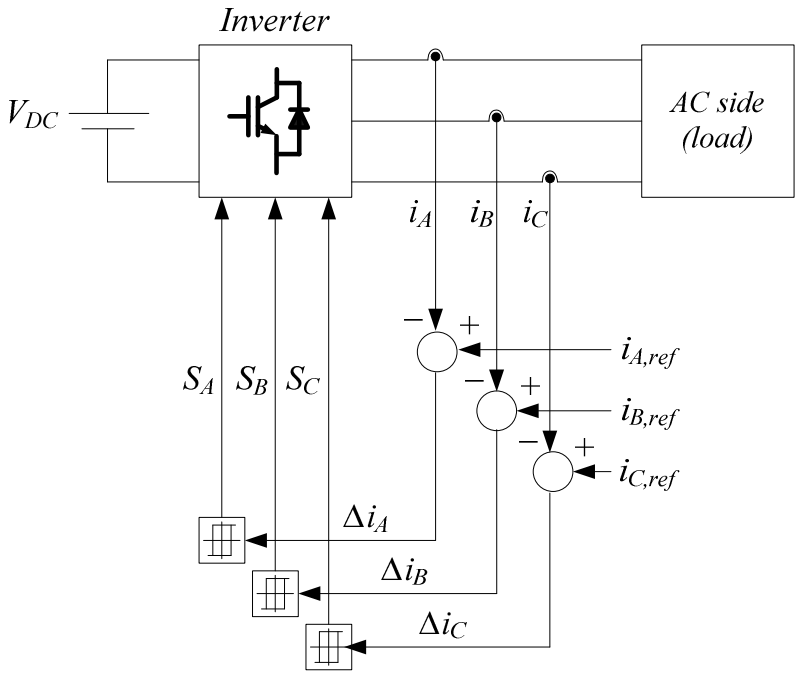


Figure 2.26: Hysteresis current control scheme.

Despite the advantages offered, hysteresis control scheme is basically characterized by the variable switching frequency of the inverter during a fundamental period. (Brod & Novotny, 1985). This results in occasional irregular operations of the inverter which then contributes to the increase in the switching losses (Azizur Rahman, Radwan, Osheiba, & Lashine, 1997). In addition, for a grid-connected inverter system, undesirable spread of ripple current harmonics can also occur which then complicates

the design of the output filter and generates unwanted resonances to the grid (Serpa, 2007). For a system without a neutral connection, the current error can reach double the value of the hysteresis band (Kazmierkowski & Malesani, 1998). Since variable switching frequency is caused by the interaction between three independent hysteresis comparators that makes the phase current in one phase to be also affected by the voltages of the other phases, then a solution is proposed to employ three dependent hysteresis comparators with the application of zero voltage vector (Brod & Novotny, 1985) in compensating the interaction effect. Further improvements have been made with the introduction of space-vector-based hysteresis current controller (Bong-Hwan, Tae-Woo, & Jang-Hyoun, 1998).

To avoid the undesirable effects of variable switching frequency altogether, constant switching frequency hysteresis controllers have been proposed. In one study, an adaptive hysteresis controller is proposed by varying the hysteresis band according to the variations in motor speed, load current and neutral-point voltage in order to hold the switching frequency constant at any operating conditions (Tae-Won & Meong-Kyu, 1996). Another study proposes the concept of parabolic hysteresis band for a space-vector-based hysteresis controller to achieve a nearly-constant switching frequency for a two-level inverter-fed drive (Tekwani, Kanchan, & Gopakumar, 2007b). Time-based hysteresis controller has also been introduced by considering the derivative of the current error for selecting the voltage level so that the current error can be forced to zero (Bode, Zmood, Loh, & Holmes, 2001). The concept of multiband hysteresis has also been studied to improve the transient response (Loh, Bode, Holmes, & Lipo, 2002) and to stabilize the switching frequency (Zare, Zabihi, & Ledwich, 2007). Recently, a new space-vector-based hysteresis current controller for multilevel inverter-fed induction motor drive has been reported (Dey, Rajeevan, Ramchand, Mathew, & Gopakumar,

2013). The control scheme uses varying parabolic hysteresis band to control the switching frequency variation and employs a certain voltage vector selection procedure to ensure optimal switching of the inverter.

2.5.3 Voltage-Oriented Control

Voltage-oriented control (VOC) scheme is based on the coordinate transformation between the stationary $\alpha\beta$ and synchronous rotating dq reference frames. The coordinate transformation converts the AC phase quantities into DC components which allow the synchronous controller to control the DC components with zero steady-state error (Cichowlas & Kamierkowski, 2002; Liserre, Dell'Aquila, & Blaabjerg, 2003; Zmood & Holmes, 2003). Figure 2.27 illustrates the basic principle of the VOC scheme. The measured output currents i_A, i_B and i_C are first transformed into stationary frame AC current i_α and i_β. Next, second transformation takes place to produce synchronous rotating frame DC quantities i_d and i_q. These DC quantities are compared with their respective references and the errors generated Δi_d and Δi_q are used as inputs to the PI synchronous controllers. The PI controllers act to compensate for these errors by producing appropriate control signals v_d and v_q. To generate the switching signals of the power devices for the execution of the command signals, v_d and v_q have to be transformed back to the stationary frame and then to the phase quantities before they are used by the modulator.

VOC scheme is considered as a control technique of indirect active and reactive power control. The DC quantities i_d and i_q determine the active and reactive power flow respectively. To achieve unity power factor, it is desirable that i_q is set to zero. Therefore, the reference command for the q-component, $i_{q,ref}$ is fixed at zero value. Since i_d and i_q are two different quantities, it appears that active and reactive powers can

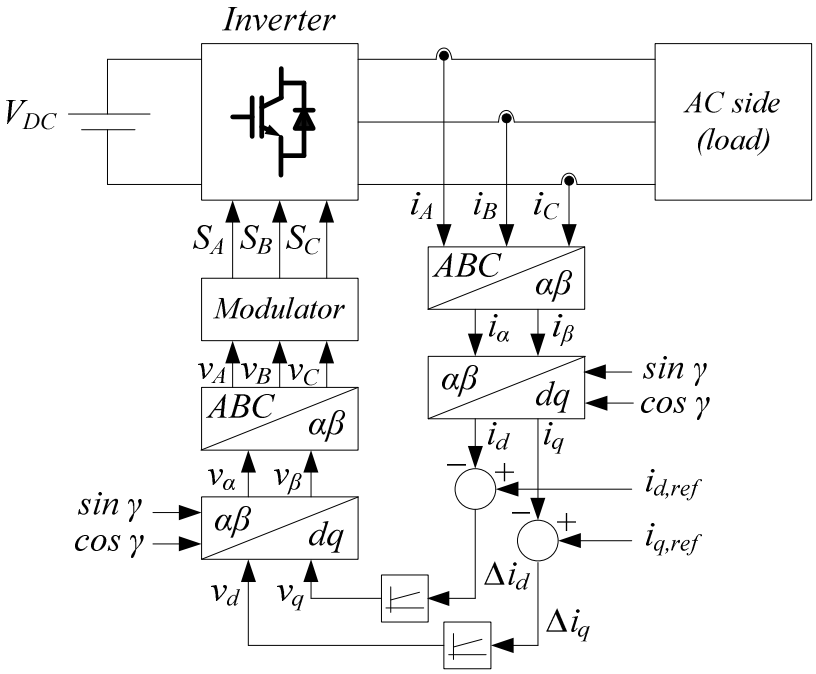


Figure 2.27: Voltage-oriented current control scheme.

be controlled independently. However, PI controllers cannot work well to provide satisfactory tracing performance as a result of the presence of cross-coupling components in the rotating frame voltage equations (Bong-Hwan, Jang-Hyoun, & Jee-Woo, 1999). To remove the cross-coupling effect so that the controllers are independent of each other to control i_d and i_q, a feedforward decoupling network is used. This solution allows the PI controllers to function as desired with accurate current tracking performance (Malinowski, 2001). Further improvement has been reported with the application of virtual flux concept. In a grid-connected system employing VOC scheme, the angle of the line voltage vector in the stationary frame is used to perform coordinate transformation to the synchronous rotating frame. The accuracy of the angle calculated is very much influenced by the disturbances in the line voltages (Malinowski, 2001). To minimize this effect, the angle of virtual flux vector is used instead to achieve a more accurate coordinate transformation since virtual flux is less sensitive to the abovementioned disturbances. Furthermore, with this approach, the implementation of phase-locked loop (PLL) is not necessary to achieve robustness in the VOC scheme.

VOC scheme generally leads to good transient response and acceptable steady-state operation (Larrinaga, Vidal, Oyarbide, & Apraiz, 2007). It can also operate at a fixed switching frequency (Kazmierkowski, Jasinski, & Wrona, 2011). VOC scheme is normally employed for grid-connected applications. In one study, a dynamic Volt Ampere Reactive (VAR) compensator based on VOC scheme has been reported for grid-connected wind energy conversion system (Amin & Mohammed, 2010). To achieve low switching frequency operation which is usually seen in high power applications without deteriorating the amount of harmonic distortion, LCL filters have been used to replace the series inductor filter to provide the interface between the inverter and the grid (Liserre, Blaabjerg, & Hansen, 2005). Nonetheless, one concern about LCL filter is that it requires resonance damping. Therefore, the performance of PI controllers in the VOC scheme that employs LCL filters has been investigated (Dannehl, Wessels, & Fuchs, 2009). Based on VOC scheme as well, an improved maximum power point tracker has been proposed to solve the changing irradiation problem (Kadri, Gaubert, & Champenois, 2011).

The equivalent of VOC scheme in motor drive applications is known as field-oriented control (FOC) scheme (Kouro, Malinowski, Gopakumar, Pou, Franquelo, Bin, Rodriguez, Perez, & Leon, 2010). In a basic FOC scheme (Jasinski, 2005), the stator currents are used for comparison in the *dq* frame before they are fed to the PI controllers to generate the commanded stator voltage of *d*-axis and *q*-axis components. These commanded voltage components are transformed back to the stationary frame from the rotating frame for further used by the space vector modulator to produce the switching signals for the power switches. In this scheme, a speed controller is also utilized to provide the reference stator current for the *q*-axis component. As for the *d*-axis component, rotor flux linkage is used to derive the reference stator current. Many

studies have been conducted to further improve the scheme so that its application can be expanded to include various types of machines such as bearingless (Zhu, Hao, Zhang, Pan, & Liu, 2008) and five-phase (Ben Echikh, Trabelsi, Mirnouni, & M'Sahli, 2013) induction motors.

2.5.4 Direct Power Control

Direct power control (DPC) scheme is a control scheme that regulates the phase currents by directly controlling the instantaneous active and reactive powers (Noguchi, Tomiki, Kondo, & Takahashi, 1998). Unlike VOC that is characterized by the inner current control loops with coordinate transformation, DPC applies power control loops without any synchronous rotating coordinate transformation. Figure 2.28 presents the block diagram of the DPC scheme. The three-phase currents and voltages are used to estimate the instantaneous active power p and reactive power q by the voltage and power estimation block. The estimated p and q are then compared with their respective references p_{ref} and q_{ref}. p_{ref} can be determined using a voltage controller while q_{ref} is normally set at zero to achieve unity power factor. The power errors Δp and Δq are next fed to the hysteresis controllers to produce digitized signals v_p and v_q which are used together with the output of the voltage position detector θ to select the appropriate voltage vector according to the switching table. The selection is done in a manner that restricts the power errors within the hysteresis band. The switching table is prepared offline and stores the switching states of the inverter according to the operating conditions.

Similar to the VOC scheme, the DPC scheme can also be further improved using virtual flux concept. The estimation of instantaneous powers requires many voltage and current sensors which then lead to an increase in cost and a reliability issue. As a result,

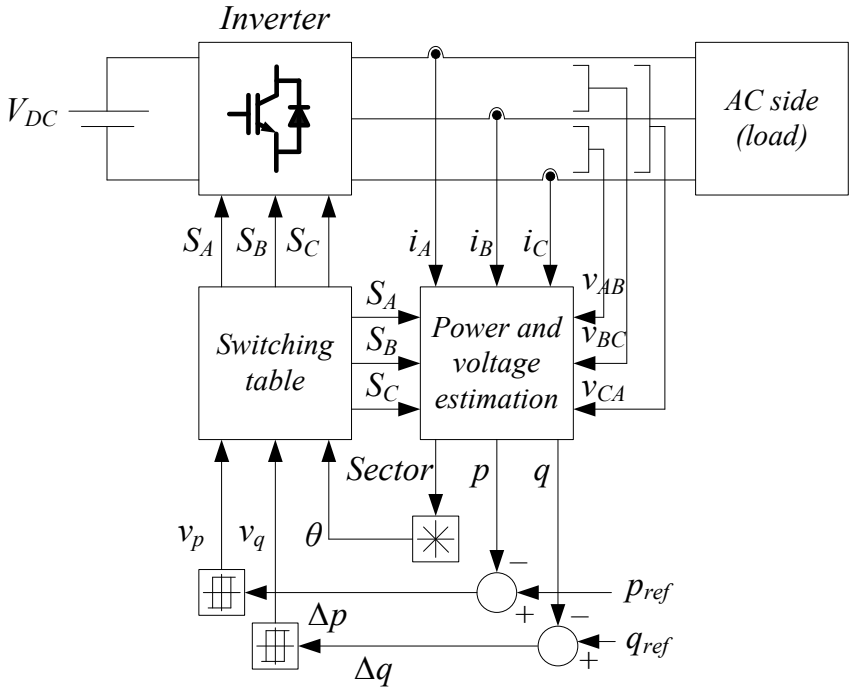


Figure 2.28: Direct power control scheme.

voltage estimation method is proposed to reduce the number of sensors used (Noguchi, Tomiki, Kondo, & Takahashi, 1998). However, since the computation of the instantaneous powers involves time derivatives of the measured currents, practical implementation has become an issue. Besides, the derivatives can also amplify the noise which then causes an increase in the level of distortion. To overcome this problem, virtual flux concept has been applied (Malinowski, Kazmierkowski, Hansen, Blaabjerg, & Marques, 2001). Instead of using voltages, virtual flux is used to estimate the instantaneous powers. Power estimation can be done in both the *dq* and *αβ* frame. In most cases, estimation using *αβ* quantities is preferable since *dq* transformation can be avoided.

The main advantage of the DPC scheme is that it can provide fast and robust dynamic response (Serpa, Round, & Kolar, 2007). This is owing to the absence of synchronous rotating frame transformation which typically demands high computational

efforts. Implementation of DPC scheme can be made easier especially with the use of virtual flux for power estimation. Further improvements on the DPC have been reported in various studies. In one study, a third-order LCL output filter is used with the DPC scheme in order to achieve a reduced level of harmonic distortion for the inverter that operates with a low switching frequency (Serpa, Ponnaluri, Barbosa, & Kolar, 2007). Since LCL filter resonances can cause the steady-state and transient distortion of the output current, a modified virtual flux DPC scheme has been proposed with the introduction of power-based active damping and individual harmonic control loops. Another modified virtual flux DPC scheme that is applied to a five-level active NPC inverter includes an additional block to balance the voltage across the DC link and floating capacitors (Serpa, Barbosa, Steimer, & Kolar, 2008).

The fact that the DPC employs hysteresis controllers contributes to the variation of the switching frequency. Besides, high sampling frequency is also needed for digital implementation of the hysteresis controllers (Malinowski, Jasinski, & Kazmierkowski, 2004). To overcome this problem, modification is made to the normal DPC scheme by replacing the hysteresis controllers and the switching table with PI controllers and space vector modulator. This gives birth to a modified DPC scheme known as direct power control with space vector modulation (DPC-SVM) (Malinowski, Jasinski, & Kazmierkowski, 2004). Figure 2.29 illustrates the DPC-SVM scheme. The PI controllers receive the power errors to generate the control signals which have to be transformed from the dq frame to the $\alpha\beta$ frame. The $\alpha\beta$ quantities of the control signals are then used by the space vector modulator to generate the switching signals. Further improvements have been made to the DPC-SVM scheme for grid-connected applications with the addition of higher harmonic and voltage dips compensation

modules (Kazmierkowski, Jasinski, & Wrona, 2011). The modified DPC-SVM algorithm has also been implemented in a single chip floating-point microcontroller.

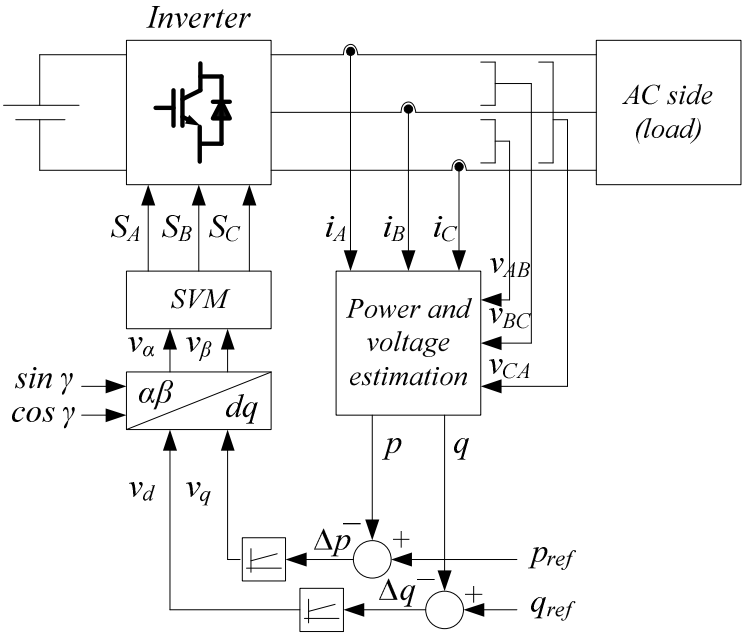


Figure 2.29: Direct power control with space vector modulation scheme.

DPC scheme is basically derived from a vector control of AC machines known direct torque control (DTC) (Larrinaga, Vidal, Oyarbide, & Apraiz, 2007). As DPC is normally employed for grid-connected applications, the DTC is popularly used in motor drive applications. Instead of active and reactive powers, the DTC corresponds to torque and stator flux control. A lot of studies have been conducted on the DTC owing to the advantages offered which include simple control structure, no coordinate transformation and excellent dynamic performance of the torque control loop (Jasinski, 2005). Despite these advantages, DTC also suffers from several drawbacks such as torque pulsation and high and variable switching frequency, which requires further studies for improvement. Example of the studies include those that attempt to minimize torque pulsation (Rekioua & Rekioua, 2005), to reduce torque and flux ripples (Lixin, Limin,

Rahman, & Yuwen, 2004) and to improve the estimation of the reference torque and the reference flux (Inoue, Morimoto, & Sanada, 2012).

2.5.5 Predictive Control

Predictive current control scheme is based on the idea that current behaviour can be predicted using load and inverter models based on certain predefined criteria (Rodriguez, Pontt, Silva, Correa, Lezana, Cortes, & Ammann, 2007). From a number of possible control actions generated from the models, one that satisfies the specified criteria based on the prediction done is then selected and applied to the inverter. The predefined criteria are usually described as a quality function that is used for the evaluation of the predicted values of the output currents in the future. Figure 2.30 displays the block diagram of the predictive current control scheme. The measured output currents are first received by the predictive model block. The predictive model block provides all possible voltage vectors generated by the inverter and the discrete-time form of the output currents in the next sampling instant namely $i(k+1)$. For each voltage vector, the value of the output current in the next sampling interval is predicted and then sent to the next block that evaluates the value of the quality function. The most common quality function assesses the current error between the predicted current and its reference to attain good tracking performance. Additional term can also be included in the quality function to achieve extra criteria such as minimum switching frequency and voltage balancing (Vargas, Cortes, Ammann, Rodriguez, & Pontt, 2007). The voltage vector that corresponds to the minimum value of the quality function is then selected and applied to the inverter.

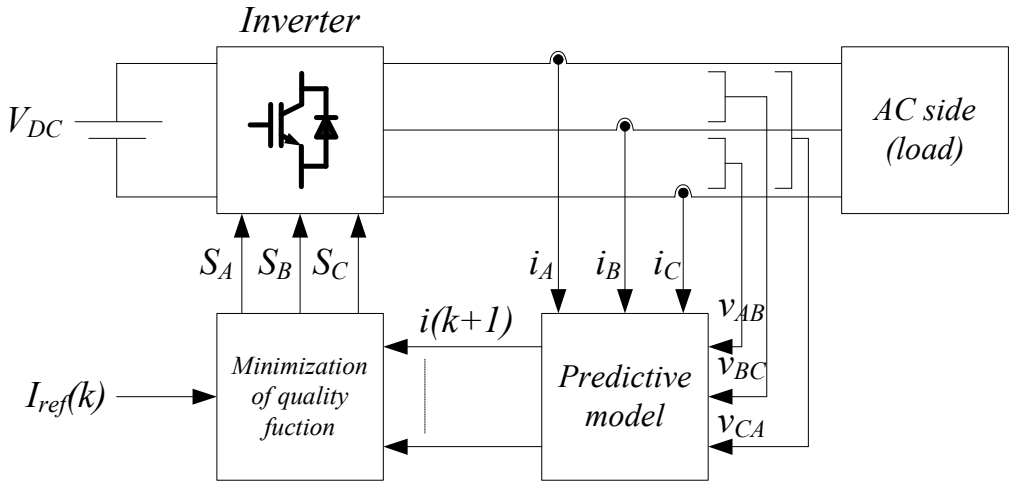


Figure 2.30: Predictive current control scheme.

Predictive current control scheme offers the advantage of having the possibility to include nonlinearities of the system in the predictive model (Rodriguez, Pontt, Silva, Correa, Lezana, Cortes, & Ammann, 2007). Several criteria can also be met by adding the terms that corresponds to the criteria in the quality function. These advantages have attracted the interest to apply the predictive element of this control scheme to compensate for the weakness of another current control approaches. For example, in one study, to overcome the variable switching frequency issue of the DPC scheme, predictive element has been added to modify the DPC scheme by computing the application times of the voltage vectors in a way that forces the predicted active and reactive powers to converge towards their respective reference values along a fixed predefined switching period (Larrinaga, Vidal, Oyarbide, & Apraiz, 2007). This so-called predictive DPC (P-DPC) scheme can be illustrated using the block diagram shown in Figure 2.31. The predictive module which consists of the power predictive model block and the quality function minimization block, selects the appropriate voltage vector sequence that can provide minimum line current ripple and computes the application times in a manner that reduces the final tracking errors.

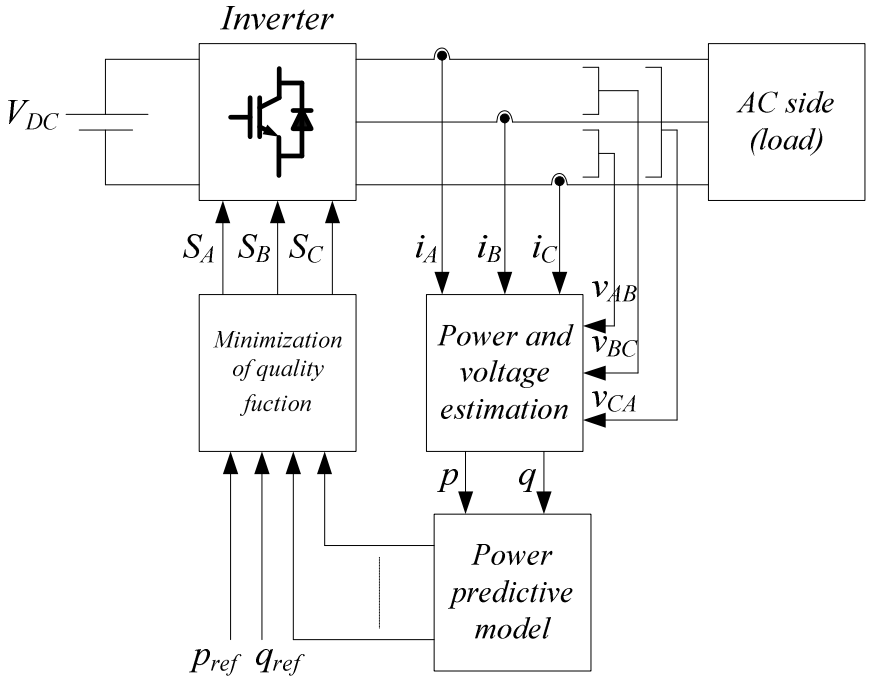


Figure 2.31: Predictive direct power control scheme.

Further improvement on the P-DPC has also been reported. An improved optimum vector selection scheme (OVSS) algorithm is proposed by using a closed-form formula to compute the voltage vector required to obtain the minimum value of the quality function (Restrepo, Aller, Viola, Bueno, & Habetler, 2009). A standard space vector modulator is used to synthesize the computed vector. This algorithm is claimed to be able to provide instantaneous corrections of the active and reactive powers, reduce current harmonic content, minimize power and current ripple and ease computational burden of the processor for practical implementation. In another study of P-DPC, a predictive control algorithm based on deadbeat control principle is proposed to compute the required average voltage vector for the cancellation of active and reactive power tracking errors simultaneously (Bouafia, Gaubert, & Krim, 2010). Space vector modulator is also used to generate the switching state sequence that corresponds to the voltage vector. A study on the application of predictive control for multilevel inverters has also been reported. In one study, an optimized method of model predictive current control is proposed to reduce the amount of calculations needed for the selection of

optimal voltage vectors for the case of a five-level cascaded H-bridge inverter (Cortes, Wilson, Kouro, Rodriguez, & Abu-Rub, 2010). Reduction in the computation time is critical as multilevel inverters generate many voltage vectors for evaluation which then contribute to high complexity in the implementation of the predictive control scheme.

2.6 Summary

This chapter has provided a discussion about multilevel inverters in general. The basic concept of multilevel inverters has been described. The fact that the inverters are able to generate output voltages higher than the ratings of the individual semiconductor devices with reduced THD and harmonic contents make them a strong competitor to the traditional two-level inverters especially in the high voltage and high power applications. Three classic multilevel circuit topologies namely diode-clamped, flying-capacitor and cascaded H-bridge inverters have been detailed. They have become the basis for the development of new multilevel topologies with improved characteristics and performance as well as less complexity to ease practical implementation.

In tandem with the growth of multilevel inverter topologies, modulation methods for multilevel inverters have also witnessed a rapid progress. Many modulation methods of low and high switching frequency have been developed with various targets to achieve such as low harmonic contents, low switching loss, voltage-balancing capability, simplified implementation and so on. Current control techniques suitable for multilevel inverters have also been briefly explained. These techniques are basically an extension of the existing techniques employed for two-level inverters with some have to undergo a certain level of modifications to suit the multilevel characteristics.

CHAPTER 3

DESIGN OF THE PROPOSED MULTILEVEL INVERTER TOPOLOGY

3.1 Introduction

Traditional multilevel inverters in the form of diode-clamped, flying-capacitor and cascaded H-bridge topologies have been widely studied over decades. An important fact reached from these studies is that the number of circuit's components dramatically increases when the number of voltage levels increases. For example, for a three-phase m-level inverter, diode-clamped topology requires $3(m-1)(m-2)$ clamping diodes, flying-capacitor topology needs $1.5(m-1)(m-2)$ flying capacitors and cascaded H-bridge topology uses $1.5(m-1)$ isolated DC sources. As a result, with increasing number of voltage levels, the circuit complexity becomes very high, the implementation cost is getting far from economical and the inverter's reliability issue raises the stake to emerge as a major concern.

As a solution to overcome the abovementioned drawbacks, a number of methods have been proposed which then pave the way for the emergence of new multilevel inverter topologies. Based on close scrutiny, it can be observed that most of these topologies are very much related to cascaded H-bridge topology. This is mostly due to the modularity feature reflected in the topology, although for asymmetric configuration, modularity is lost as the cells are not identical anymore. Another reason is that cascaded H-bridge topology uses the fewest number of devices as compared to diode-clamped and flying-capacitor topologies. Despite the fact that many studies have been conducted based on cascaded H-bridge topology, the diode-clamped inverter particularly the three-level structure is still the one widely used in all types of industrial applications as the implementation cost is the most competitive (Rodriguez, Bernet, Bin, Pontt, & Kouro,

2007; Zambra, Rech, & Pinheiro, 2010). Besides, although cascaded H-bridge topology offers attractive features, the fact that it requires multiple separated DC supplies makes its application to be somewhat limited.

It has been reported that one of the factors that hinders the use of diode-clamped inverter of higher number of levels (more than three levels) is the high number of clamping diodes employed which then contributes to a significant increase in conduction losses (Kouro, Malinowski, Gopakumar, Pou, Franquelo, Bin, Rodriguez, Perez, & Leon, 2010). Although active NPC multilevel inverter has been proposed to eliminate the use of clamping diodes, it comes at the expense of the use of more power switches instead (Barbosa, Steimer, Steinke, Meysenc, Winkelnkemper, & Celanovic, 2005). As power switches are more expensive that diodes, the implementation cost may consequently increase. The same is also experienced with the transistor-clamped multilevel inverter. The use of bidirectional switches in which each consists of two semiconductor power switches, increases the total number of switches used (Guennegues, Gollentz, Meibody-Tabar, Rael, & Leclere, 2009).

In this study, a different approach is taken to remove the clamping diodes without increasing the number of power switches. The suggested solution employs a switch-sharing approach that not only eliminates the use of clamping diodes, but also significantly reduces the number of power switches. The proposed multilevel inverter topology is derived from the transistor-clamped multilevel inverter and carries some similarities to the diode-clamped inverter in the sense that both do not need isolated DC sources. The voltage balancing methods for the DC link capacitors that are used for the diode-clamped inverter can also be applied to the proposed inverter. Furthermore, in both inverters, the top outer and the bottom outer switches in each leg are responsible

for the maximum and minimum voltage levels. Only the way that the other voltage levels are generated makes the proposed inverter different from the diode-clamped counterpart. The next section provides the general structure of the proposed inverter before four-level and five-level inverters are illustrated. The operating principles of the inverters at low switching frequency are explained. A novel PWM scheme based on modified space vector principles is proposed. Current control of the proposed inverter based on VOC and DPC-SVM schemes are discussed. To improve the tracking performance and the quality of the output current after a load change, one of the PI controllers is equipped with a novel tuning algorithm to make it adaptive.

3.2 Generalized Structure

Figure 3.1 shows the generalized structure of the proposed topology. The structure is made up of three modules. Module 1 is the conventional full-bridge circuit whose switches are utilized to generate the maximum and minimum voltage steps in the line-to-line waveforms. Module 2 is composed of three bidirectional switches in which each of them represents each phase. In other words, each bidirectional switch functions in the normal mode in the sense that it is exclusively employed for a particular phase. Module 3 comprises a string of bidirectional switches which are connected to DC sources. The bidirectional switches are made to operate in the optimized mode in a way that the operation of each switch is divided among the three phases. This means that the bidirectional switches are shared among the three phases instead of exclusively reserved to a certain phase. Here, only one switch is allowed to be active while others are turned off at a particular time as to avoid a short circuit across the DC sources. For m-level structure, the inverter requires $(m - 2)$ bidirectional switches in Module 3. The appropriate interaction between Module 2 and Module 3 produces the non-zero voltage steps in between the maximum and the minimum.

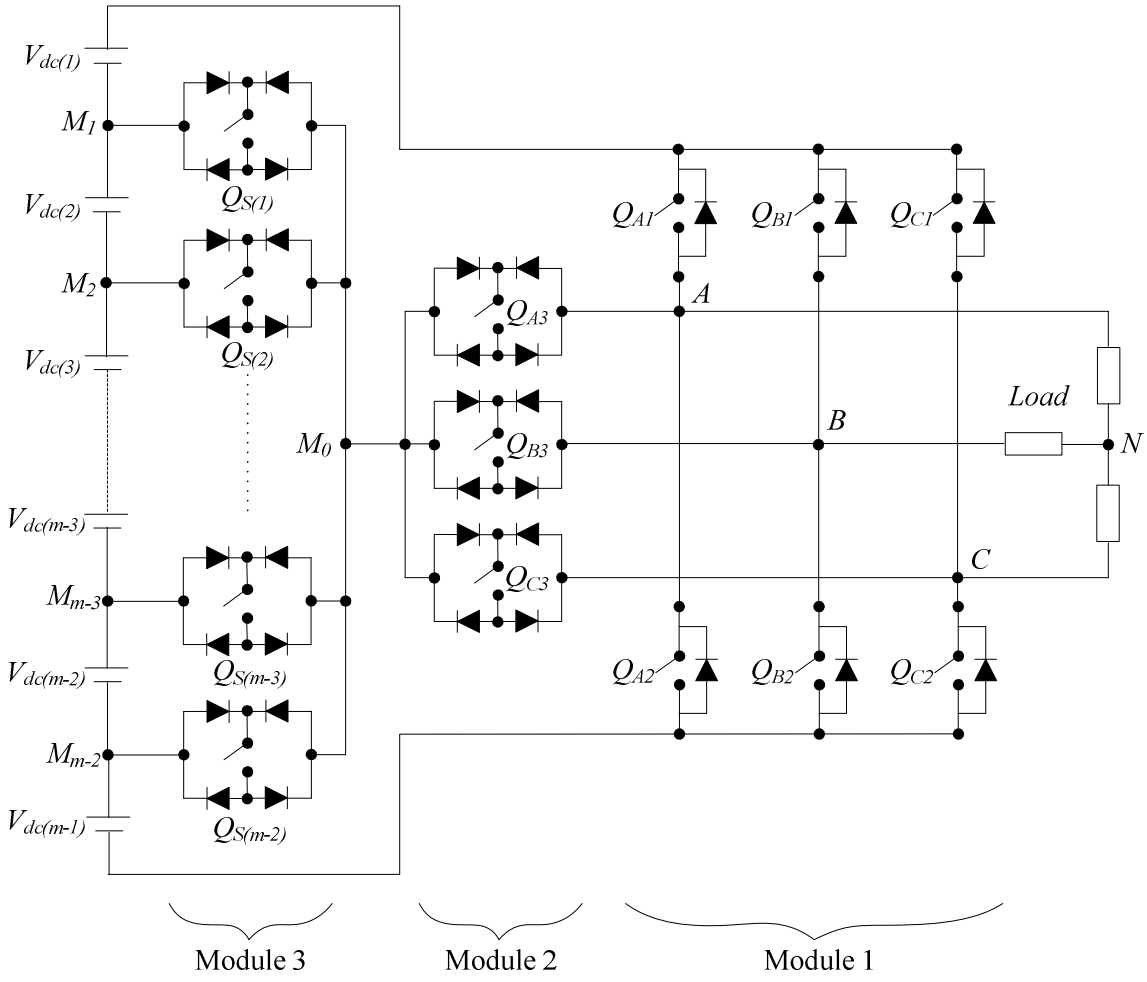


Figure 3.1: Generalized structure of the proposed topology.

The combination of Module 1 and Module 2 is actually equivalent to a three-phase three-level transistor-clamped inverter proposed by Guennegues et al (2009) as shown in Figure 2.17. In the proposed topology, a different type of bidirectional switch is used. Unlike the transistor-clamped inverter shown in Figure 2.17 that uses bidirectional switches comprising two transistors and two diodes in every switch, the proposed topology employs one-transistor, four-diodes bidirectional switches instead as displayed in Figure 2.15. By using these switches, the total number of power switches used in the proposed topology can be reduced, thus simplifying the three-level transistor-clamped inverter circuit. In fact, such a simplified three-phase transistor-clamped inverter has been derived from the single-phase transistor-clamped H-bridge

inverter (Mahrous, Rahim, & Hew, 2007). To implement the switch-sharing approach, Module 3 is added to give birth to the proposed topology.

Table 3.1 Comparison of component requirements between the proposed topology and the three classic topologies

Components	Number of levels	Topology			
		Diode-clamped topology	Flying-capacitor topology	Cascaded H-bridge topology	Proposed topology
Number of main switches	5	24	24	24	12
	m	$6(m-1)$	$6(m-1)$	$6(m-1)$	$m+7$
Number of anti-parallel diodes	5	24	24	24	6
	m	$6(m-1)$	$6(m-1)$	$6(m-1)$	6
Number of diodes for bidirectional switches	5	0	0	0	24
	m	0	0	0	$4(m+1)$
Number of clamping diodes	5	36	0	0	0
	m	$3(m-1)\times(m-2)$	0	0	0
Number of flying capacitors	5	0	18	0	0
	m	0	$3(m-1)\times(m-2)/2$	0	0
Number of DC link capacitors	5	4	4	0	4
	m	$m-1$	$m-1$	0	$m-1$
Number of isolated DC sources	5	1	1	6	1
	m	1	1	$3(m-1)/2$	1
Total number of components	5	89	71	54	47

Table 3.1 summarizes the component requirements of the proposed topology and the three classical topologies. The table provides the number of components for both the generalized case of m-level structure and the specific case of a five-level configuration. It can be implied from the table that the proposed topology offers the lowest number of components compared to other topologies particularly when the number of levels becomes bigger. As seen from the table, for a five-level inverter, the proposed topology only requires a total of 47 components which is less than that of other topologies namely 89, 71 and 54 for diode-clamped, flying-capacitor and cascaded H-bridge

topologies respectively. Although the total number of diodes used (excluding the clamping diodes) appears to be higher for the proposed topology with five-level structure, this is no longer the case when the number of levels increases. For example, for eleven-level inverter, the proposed topology needs a total of 54 diodes which is less than 60 required by other topologies. In addition, a significant reduction is observed in the number of main switches. 50% reduction is acquired with the proposed topology of five-level structure, thus makes it more cost-effective.

3.3 Operational Principles

To illustrate the operation of the proposed topology, four-level and five-level configurations are presented. The two configurations are obtained by only modifying the number of bidirectional switches in Module 3. Module 1 and Module 2 requires no modifications for any level of the proposed topology.

3.3.1 Four-Level Structure

Figure 3.2 depicts the four-level inverter of the proposed topology. The inverter has 11 switches in which two bidirectional switches are used in Module 3 to produce seven voltage steps in the line-to-line voltage waveform of the following amplitudes: $-3V_{dc}$, $-2V_{dc}$, $-V_{dc}$, V_{dc}, $2V_{dc}$, $3V_{dc}$ and 0. In order to explain the basic operation of the inverter at low switching frequency for the generation of the line-to-line stepped voltage waveforms, 18 modes of operation are defined and they are described as follows:

1. Mode 1 ($V_{AB} = 0$, $V_{BC} = -3V_{dc}$, $V_{CA} = 3V_{dc}$): Q_{A2} is on, linking node A to ground; Q_{B2} is on, linking node B to ground; and Q_{C1} is on, linking node C to $3V_{dc}$. All other switches are off. Figure 3.3(a) shows the current path during this mode.

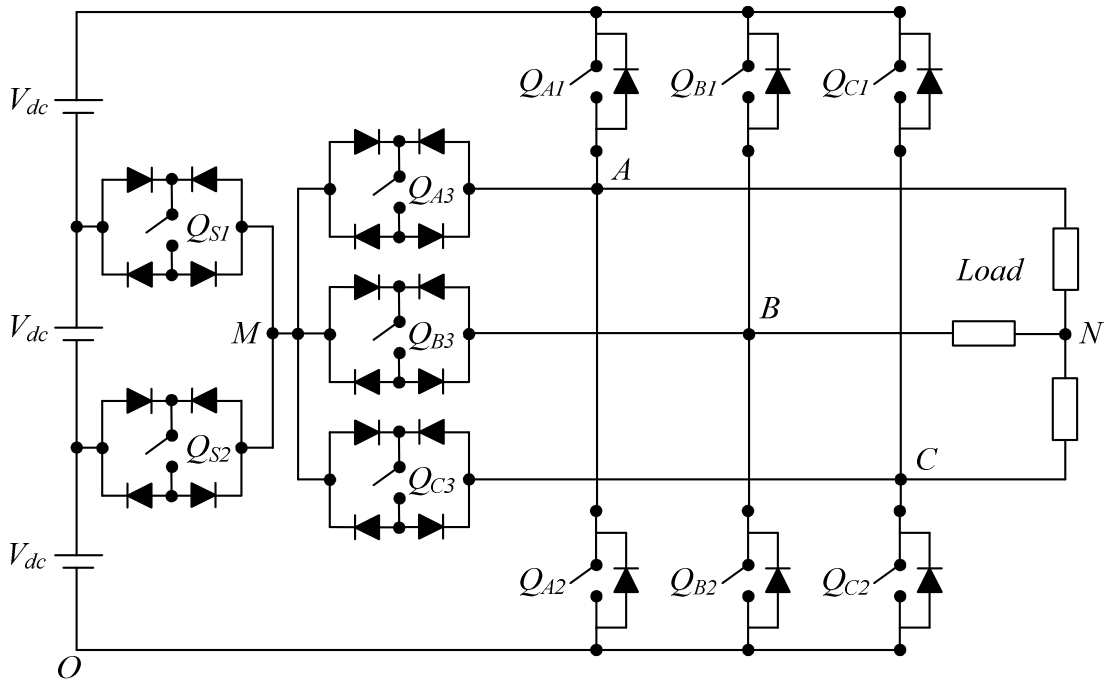


Figure 3.2: Four-level inverter of the proposed topology.

2. Mode 2 ($V_{AB} = V_{dc}$, $V_{BC} = -3V_{dc}$, $V_{CA} = 2V_{dc}$): Q_{A3} and Q_{S2} are on, linking node *A* to V_{dc}; Q_{B2} is on, linking node *B* to ground; and Q_{C1} is on, linking node *C* to $3V_{dc}$. All other switches are off. Figure 3.3(b) shows the current path during this mode.

3. Mode 3 ($V_{AB} = 2V_{dc}$, $V_{BC} = -3V_{dc}$, $V_{CA} = V_{dc}$): Q_{A3} and Q_{S1} are on, linking node *A* to $2V_{dc}$; Q_{B2} is on, linking node *B* to ground; and Q_{C1} is on, linking node *C* to $3V_{dc}$. All other switches are off. Figure 3.3(c) shows the current path during this mode.

4. Mode 4 ($V_{AB} = 3V_{dc}$, $V_{BC} = -3V_{dc}$, $V_{CA} = 0$): Q_{A1} is on, linking node *A* to $3V_{dc}$; Q_{B2} is on, linking node *B* to ground; and Q_{C1} is on, linking node *C* to $3V_{dc}$. All other switches are off. Figure 3.3 (d) shows the current path during this mode.

5. Mode 5 ($V_{AB} = 3V_{dc}$, $V_{BC} = -2V_{dc}$, $V_{CA} = -V_{dc}$): Q_{A1} is on, linking node *A* to $3V_{dc}$; Q_{B2} is on, linking node *B* to ground; and Q_{C3} and Q_{S1} are on, linking node *C* to $2V_{dc}$. All other switches are off. Figure 3.3(e) shows the current path during this

mode.

6. Mode 6 ($V_{AB} = 3V_{dc}$, $V_{BC} = -V_{dc}$, $V_{CA} = -2V_{dc}$): Q_{A1} is on, linking node A to $3V_{dc}$; Q_{B2} is on, linking node B to ground; and Q_{C3} and Q_{S2} are on, linking node C to V_{dc}. All other switches are off. Figure 3.3(f) shows the current path during this mode.

7. Mode 7 ($V_{AB} = 3V_{dc}$, $V_{BC} = 0$, $V_{CA} = -3V_{dc}$): Q_{A1} is on, linking node A to $3V_{dc}$; Q_{B2} is on, linking node B to ground; and Q_{C2} is on, linking node C to ground. All other switches are off. Figure 3.3(g) shows the current path during this mode.

8. Mode 8 ($V_{AB} = 2V_{dc}$, $V_{BC} = V_{dc}$, $V_{CA} = -3V_{dc}$): Q_{A1} is on, linking node A to $3V_{dc}$; Q_{B3} and Q_{S2} are on, linking node B to V_{dc}; and Q_{C2} is on, linking node C to ground. All other switches are off. Figure 3.3(h) shows the current path during this mode.

9. Mode 9 ($V_{AB} = V_{dc}$, $V_{BC} = 2V_{dc}$, $V_{CA} = -3V_{dc}$): Q_{A1} is on, linking node A to $3V_{dc}$; Q_{B3} and Q_{S1} are on, linking node B to $2V_{dc}$; and Q_{C2} is on, linking node C to ground. All other switches are off. Figure 3.3(i) shows the current path during this mode.

10. Mode 10 ($V_{AB} = 0$, $V_{BC} = 3V_{dc}$, $V_{CA} = -3V_{dc}$): Q_{A1} is on, linking node A to $3V_{dc}$; Q_{B1} is on, linking node B to $3V_{dc}$; and Q_{C2} is on, linking node C to ground. All other switches are off. Figure 3.3(j) shows the current path during this mode.

11. Mode 11 ($V_{AB} = -V_{dc}$, $V_{BC} = 3V_{dc}$, $V_{CA} = -2V_{dc}$): Q_{A3} and Q_{S1} are on, linking node A to $2V_{dc}$; Q_{B1} is on, linking node B to $3V_{dc}$; and Q_{C2} is on, linking node C to ground. All other switches are off. Figure 3.3(k) shows the current path during this mode.

12. Mode 12 ($V_{AB} = -2V_{dc}$, $V_{BC} = 3V_{dc}$, $V_{CA} = -V_{dc}$): Q_{A3} and Q_{S2} are on, linking node A to V_{dc}; Q_{B1} is on, linking node B to $3V_{dc}$; and Q_{C2} is on, linking node C to ground. All other switches are off. Figure 3.3(l) shows the current path during

this mode.

13. Mode 13 (V_{AB} = -3V_{dc}, V_{BC} = 3V_{dc}, V_{CA} = 0): Q_{A2} is on, linking node *A* to ground; Q_{B1} is on, linking node *B* to 3V_{dc}; and Q_{C2} is on, linking node *C* to ground. All other switches are off. Figure 3.3(m) shows the current path during this mode.

14. Mode 14 (V_{AB} = -3V_{dc}, V_{BC} = 2V_{dc}, V_{CA} = V_{dc}): Q_{A2} is on, linking node *A* to ground; Q_{B1} is on, linking node *B* to 3V_{dc}; and Q_{C3} and Q_{S2} are on, linking node *C* to V_{dc}. All other switches are off. Figure 3.3(n) shows the current path during this mode.

15. Mode 15 (V_{AB} = -3V_{dc}, V_{BC} = V_{dc}, V_{CA} = 2V_{dc}): Q_{A2} is on, linking node *A* to ground; Q_{B1} is on, linking node *B* to 3V_{dc}; and Q_{C3} and Q_{S1} are on, linking node *C* to 2V_{dc}. All other switches are off. Figure 3.3(o) shows the current path during this mode.

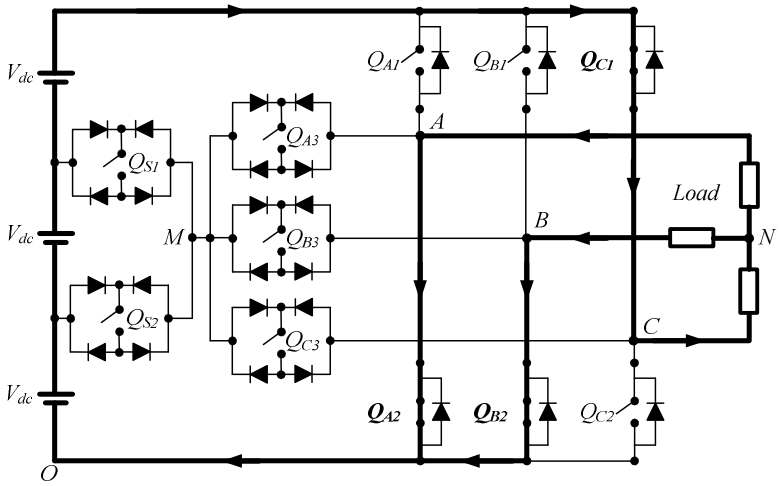
16. Mode 16 (V_{AB} = -3V_{dc}, V_{BC} = 0, V_{CA} = 3V_{dc}): Q_{A2} is on, linking node *A* to ground; Q_{B1} is on, linking node *B* to 3V_{dc}; and Q_{C1} is on, linking node *C* to 3V_{dc}. All other switches are off. Figure 3.3(p) shows the current path during this mode.

17. Mode 17 (V_{AB} = -2V_{dc}, V_{BC} = -V_{dc}, V_{CA} = 3V_{dc}): Q_{A2} is on, linking node *A* to ground; Q_{B3} and Q_{S1} are on, linking node *B* to 2V_{dc}; and Q_{C1} is on, linking node *C* to 3V_{dc}. All other switches are off. Figure 3.3(q) shows the current path during this mode.

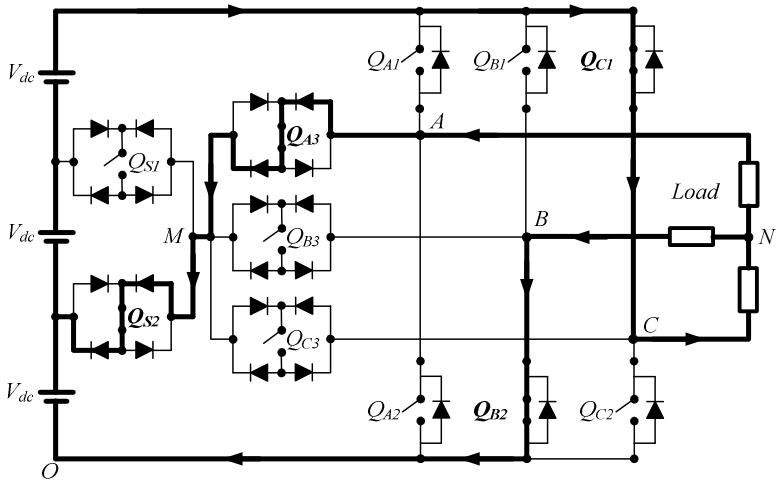
18. Mode 18 (V_{AB} = -V_{dc}, V_{BC} = -2V_{dc}, V_{CA} = 3V_{dc}): Q_{A2} is on, linking node *A* to ground; Q_{B3} and Q_{S2} are on, linking node *B* to V_{dc}; and Q_{C1} is on, linking node *C* to 3V_{dc}. All other switches are off. Figure 3.3(r) shows the current path during this mode.

Figure 3.4 shows the switching signals for the generation of the seven voltage steps in the line-to-line output voltage waveforms. It can be observed that if the output

voltages operate at frequency f, then Q_{A1}, Q_{A2}, Q_{B1}, Q_{B2}, Q_{C1} and Q_{C2} also operate at frequency f; Q_{A3}, Q_{B3} and Q_{C3} operate at frequency $2f$, and Q_{S1} and Q_{S2} operate at frequency $3f$. Out of the 18 modes of operation, six require three switches in Module 1 to be active while other switches are turned off. These modes lead to the maximum, the minimum and zero voltage steps in the three phases. For the remaining 12 modes, four switches are made to be active: two active switches in Module 1, one active switch in Module 2 and one active switch in Module 3, while the others are off. These modes generate all voltage steps other than zero.

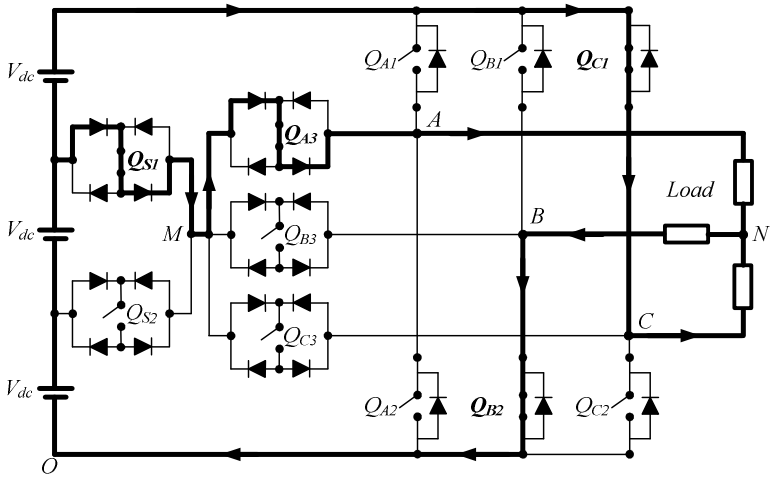


(a) Mode 1 ($V_{AB} = 0$, $V_{BC} = -3V_{dc}$, $V_{CA} = 3V_{dc}$).

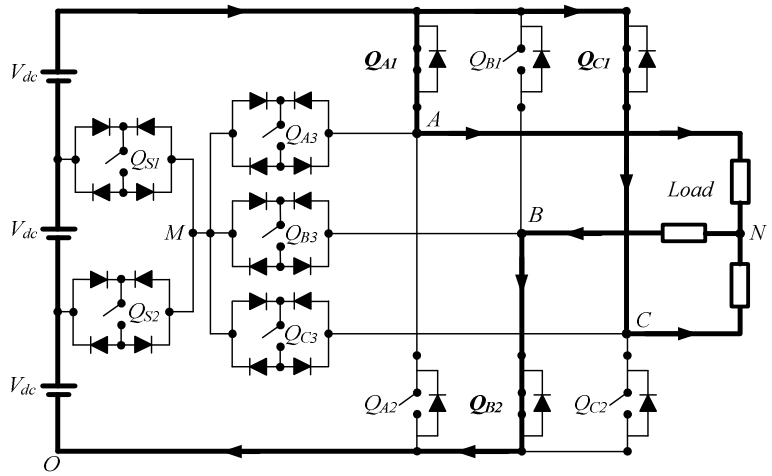


(b) Mode 2 ($V_{AB} = V_{dc}$, $V_{BC} = -3V_{dc}$, $V_{CA} = 2V_{dc}$).

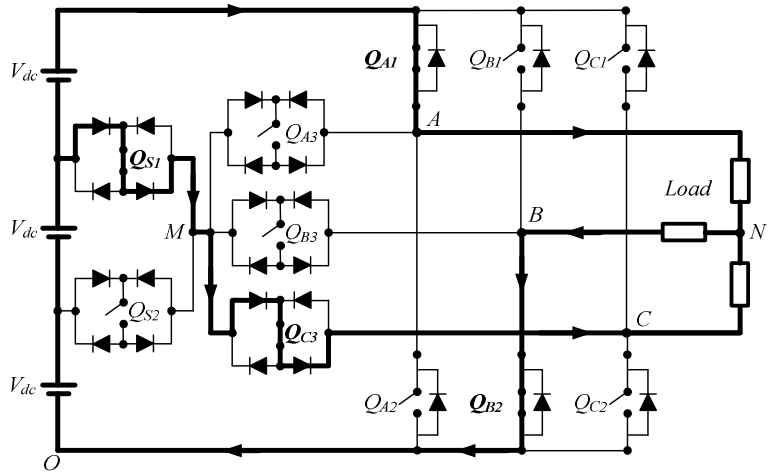
Figure 3.3: Modes of operation of the proposed four-level inverter.



(c) Mode 3 ($V_{AB} = 2V_{dc}$, $V_{BC} = -3V_{dc}$, $V_{CA} = V_{dc}$).

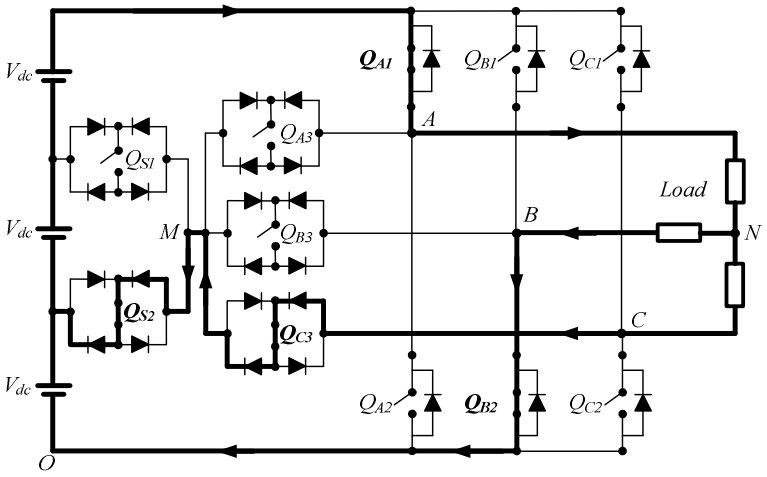


(d) Mode 4 ($V_{AB} = 3V_{dc}$, $V_{BC} = -3V_{dc}$, $V_{CA} = 0$).

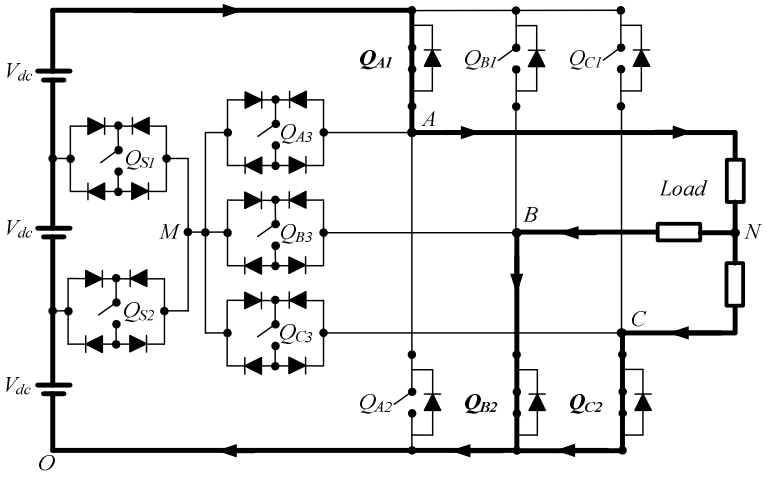


(e) Mode 5 ($V_{AB} = 3V_{dc}$, $V_{BC} = -2V_{dc}$, $V_{CA} = -V_{dc}$).

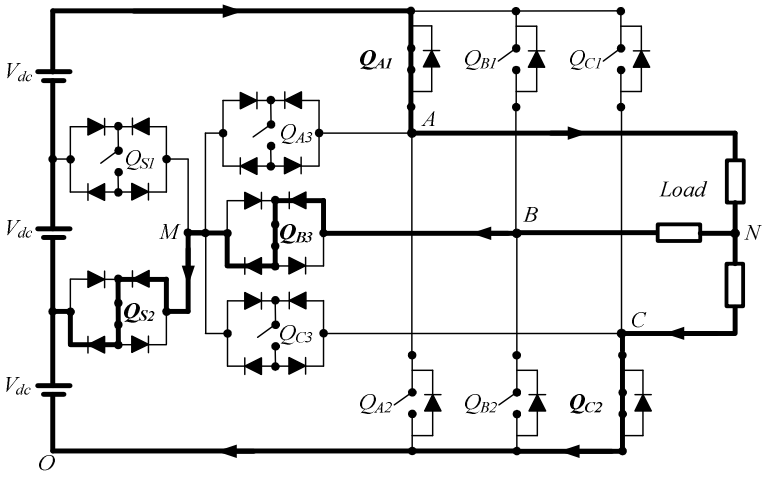
Figure 3.3, continued: Modes of operation of the proposed four-level inverter.



(f) Mode 6 ($V_{AB} = 3V_{dc}$, $V_{BC} = -V_{dc}$, $V_{CA} = -2V_{dc}$).

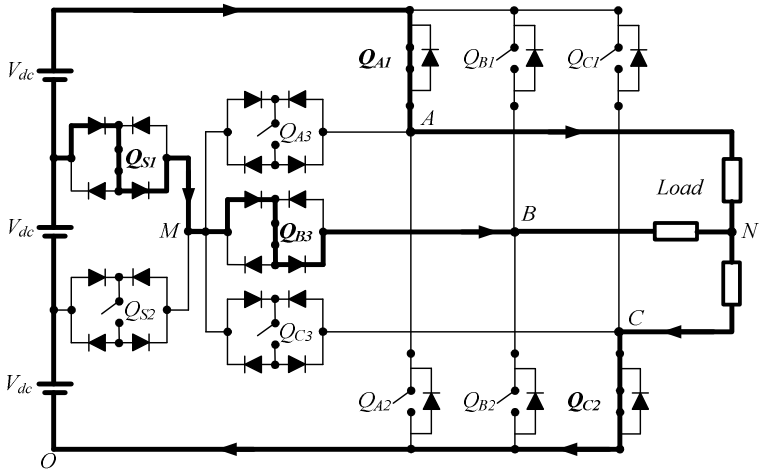


(g) Mode 7 ($V_{AB} = 3V_{dc}$, $V_{BC} = 0$, $V_{CA} = -3V_{dc}$).

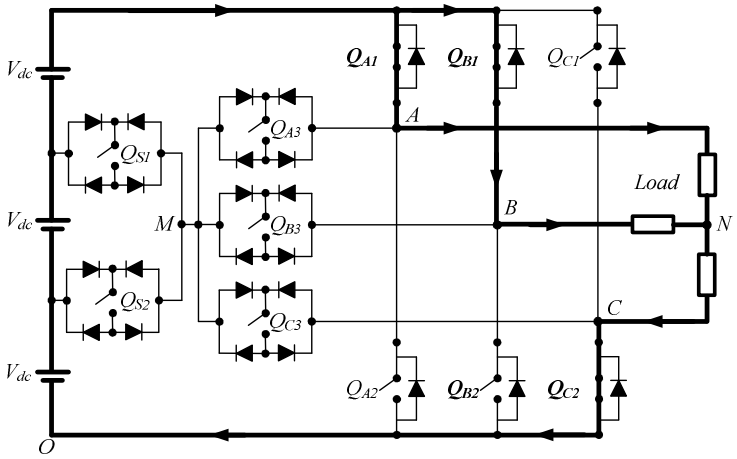


(h) Mode 8 ($V_{AB} = 2V_{dc}$, $V_{BC} = V_{dc}$, $V_{CA} = -3V_{dc}$).

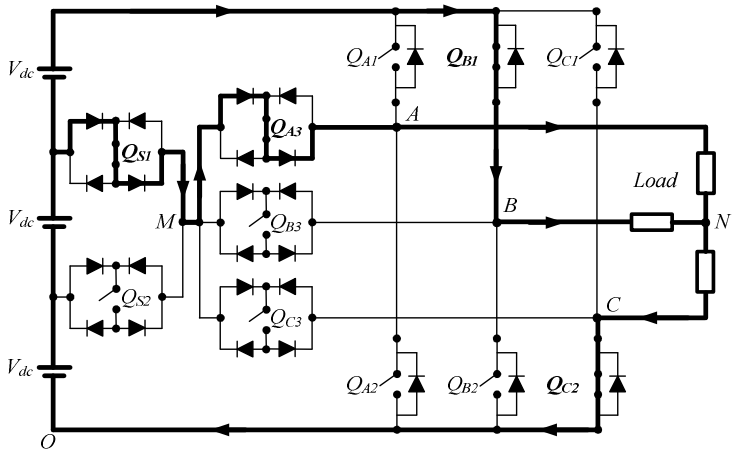
Figure 3.3, continued: Modes of operation of the proposed four-level inverter.



(i) Mode 9 ($V_{AB} = V_{dc}$, $V_{BC} = 2V_{dc}$, $V_{CA} = -3V_{dc}$).

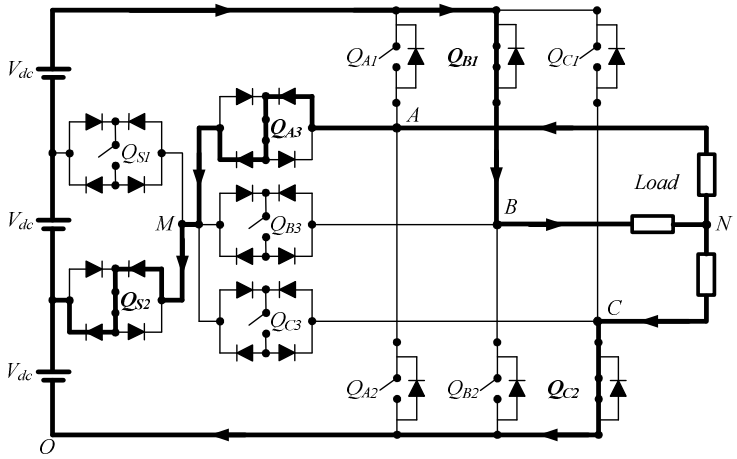


(j) Mode 10 ($V_{AB} = 0$, $V_{BC} = 3V_{dc}$, $V_{CA} = -3V_{dc}$).

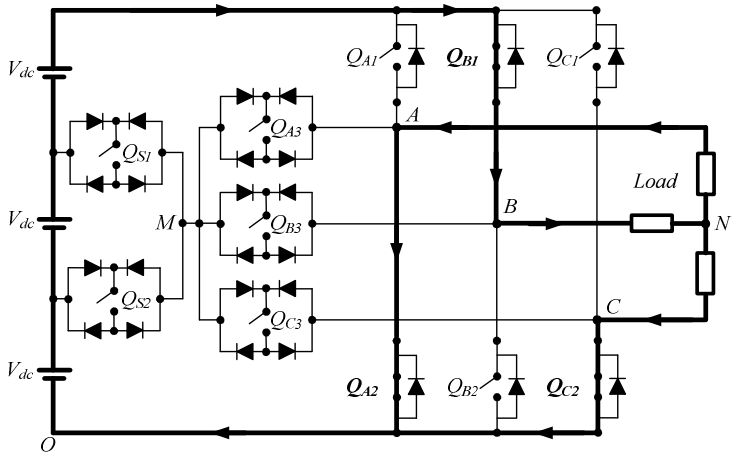


(k) Mode 11 ($V_{AB} = -V_{dc}$, $V_{BC} = 3V_{dc}$, $V_{CA} = -2V_{dc}$).

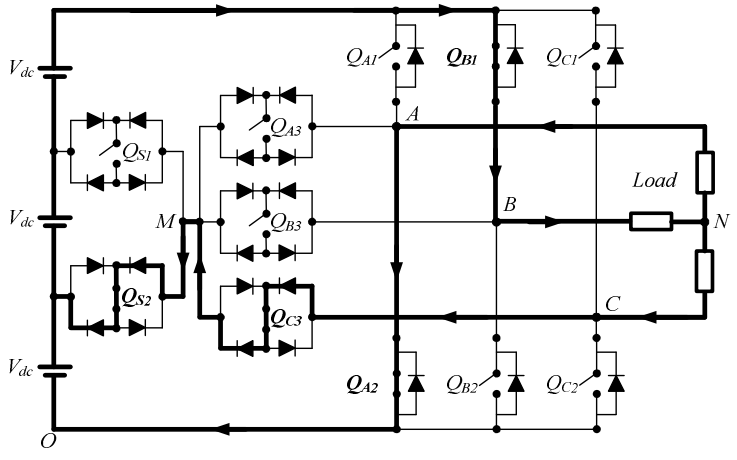
Figure 3.3, continued: Modes of operation of the proposed four-level inverter.



(l) Mode 12 (V_{AB} = -2V_{dc}, V_{BC} = 3V_{dc}, V_{CA} = -V_{dc}).

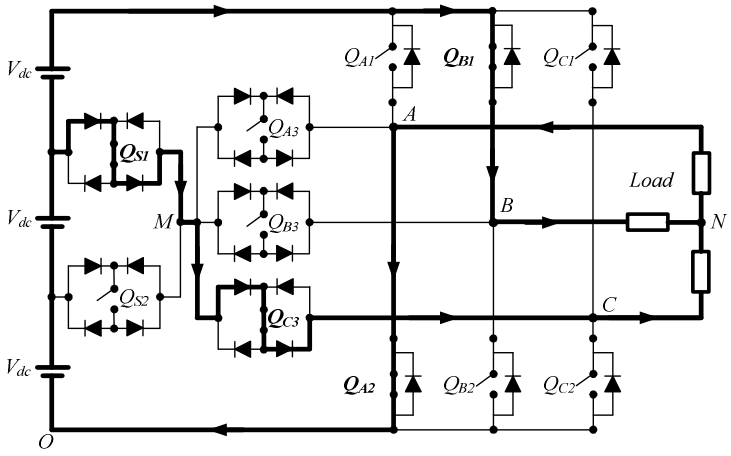


(m) Mode 13 (V_{AB} = -3V_{dc}, V_{BC} = 3V_{dc}, V_{CA} = 0).

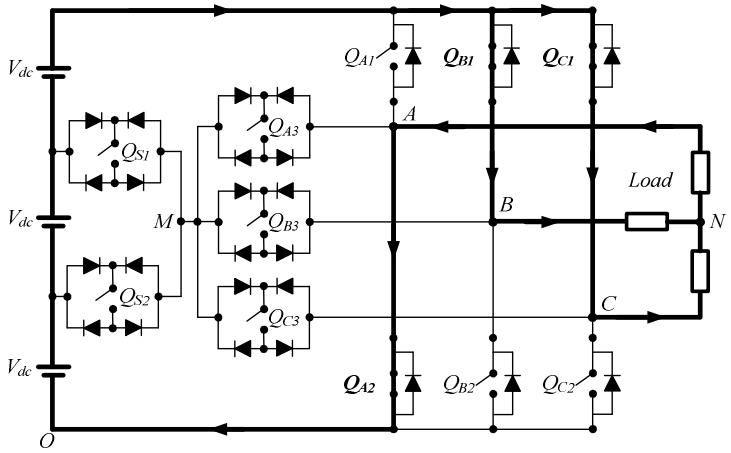


(n) Mode 14 (V_{AB} = -3V_{dc}, V_{BC} = 2V_{dc}, V_{CA} = V_{dc}).

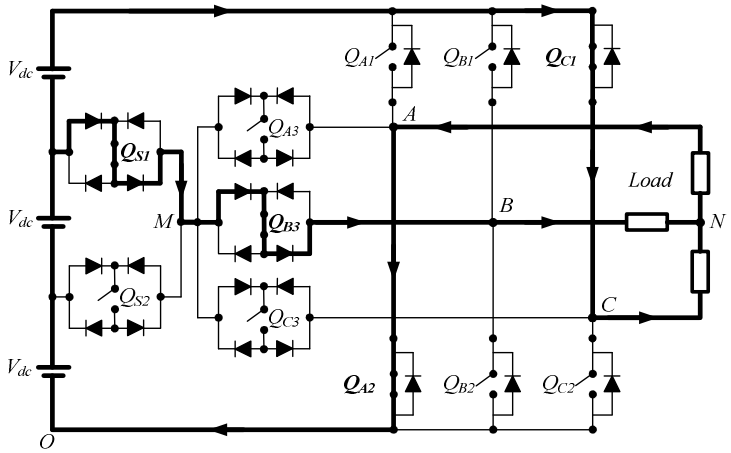
Figure 3.3, continued: Modes of operation of the proposed four-level inverter.



(o) Mode 15 (V_{AB} = -3V_{dc}, V_{BC} = V_{dc}, V_{CA} = 2V_{dc}).

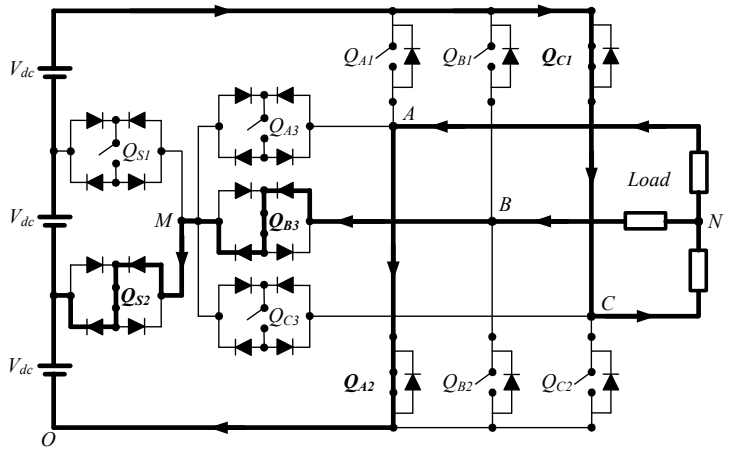


(p) Mode 16 (V_{AB} = -3V_{dc}, V_{BC} = 0, V_{CA} = 3V_{dc}).



(q) Mode 17 (V_{AB} = -2V_{dc}, V_{BC} = -V_{dc}, V_{CA} = 3V_{dc}).

Figure 3.3, continued: Modes of operation of the proposed four-level inverter.



(r) Mode 18 (V_{AB} = -V_{dc}, V_{BC} = -2V_{dc}, V_{CA} = 3V_{dc}).

Figure 3.3, continued: Modes of operation of the proposed four-level inverter.

3.3.2 Five-Level Structure

To obtain a five-level structure from the four-level configuration of the proposed topology, only one additional bidirectional switch is included in Module 3 while Module 1 and Module 2 remain. Hence, the total number of switches required is 12. The circuit configuration is portrayed in Figure 3.5. The inverter is able to produce nine voltage steps in the line-to-line output voltage waveforms of the following amplitudes: -4V_{dc}, -3V_{dc}, -2V_{dc}, -V_{dc}, V_{dc}, 2V_{dc}, 3V_{dc}, 4V_{dc} and 0. The basic operation of the inverter at a fundamental switching frequency can be described by the following 24 modes of operation below:

1. Mode 1 (V_{AB} = 0, V_{BC} = -4V_{dc}, V_{CA} = 4V_{dc}): Q_{A2} is on, linking node *A* to ground, Q_{B2} is on, linking node *B* to ground and Q_{C1} is on, linking node *C* to 4V_{dc}. All other switches are off. Figure 3.6(a) shows the current path during this mode.
2. Mode 2 (V_{AB} = V_{dc}, V_{BC} = -4V_{dc}, V_{CA} = 3V_{dc}): Q_{A3} and Q_{S3} are on, linking node *A* to V_{dc}, Q_{B2} is on, linking node *B* to ground and Q_{C1} is on, linking node *C* to 4V_{dc}. All other switches are off. Figure 3.6(b) shows the current path during this mode.

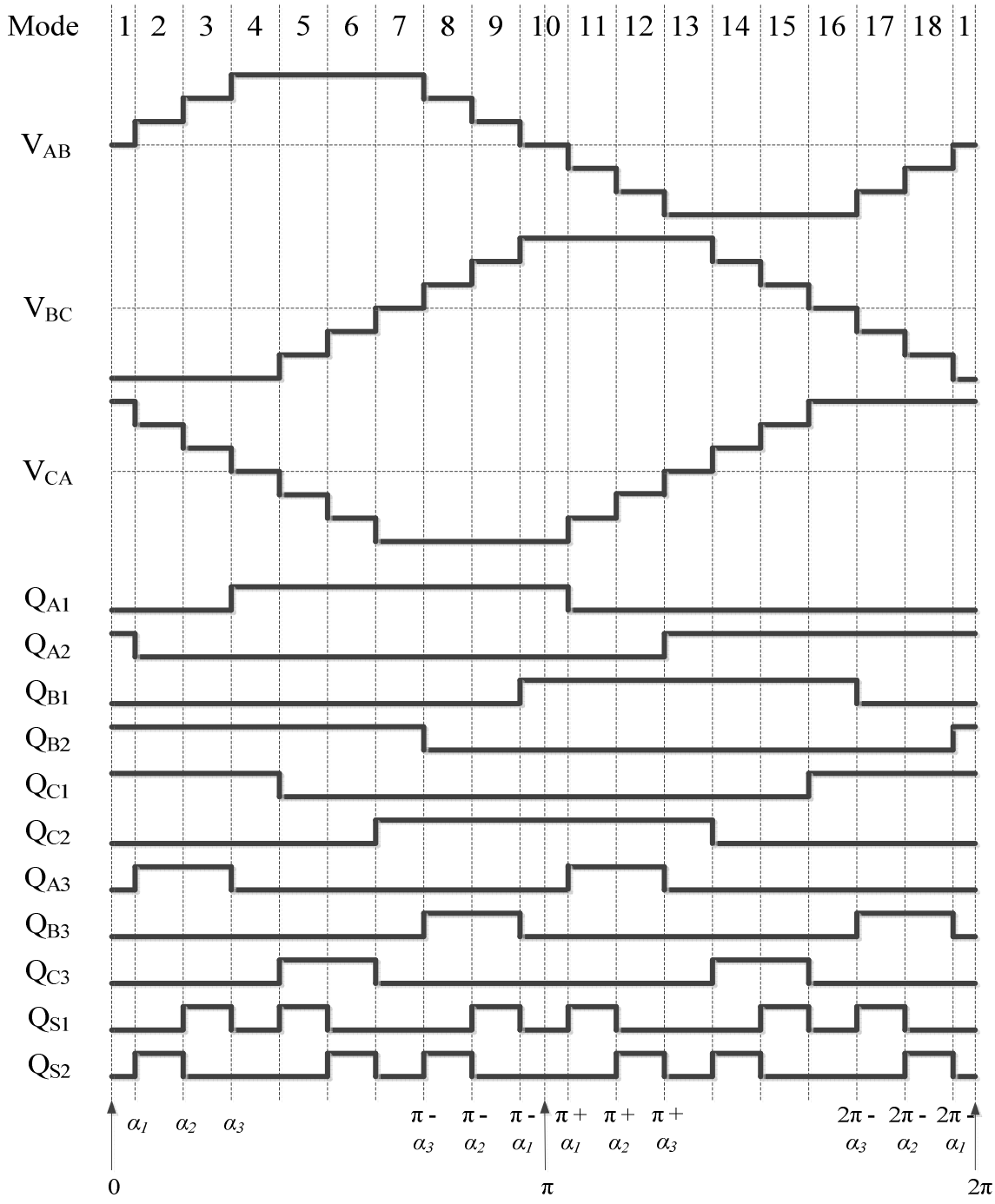


Figure 3.4: Switching signals to generate output voltages with seven voltage steps.

3. Mode 3 ($V_{AB} = 2V_{dc}$, $V_{BC} = -4V_{dc}$, $V_{CA} = 2V_{dc}$): Q_{A3} and Q_{S2} are on, linking node *A* to $2V_{dc}$, Q_{B2} is on, linking node *B* to ground and Q_{C1} is on, linking node *C* to $4V_{dc}$. All other switches are off. Figure 3.6(c) shows the current path during this mode.

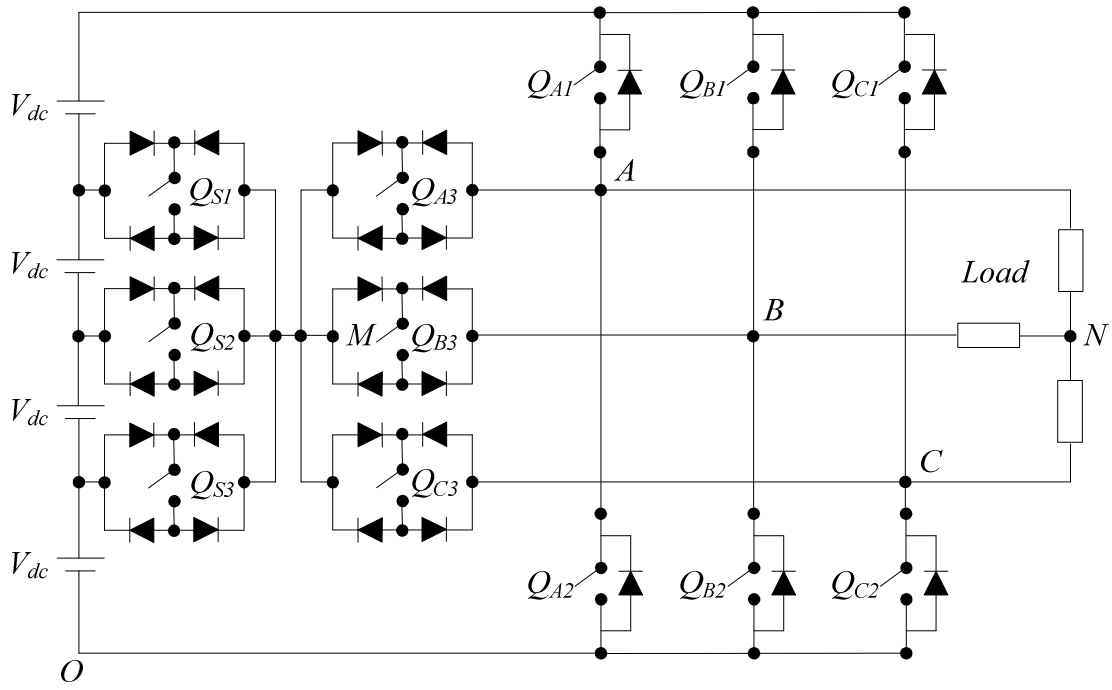


Figure 3.5: Five-level inverter of the proposed topology.

4. Mode 4 ($V_{AB} = 3V_{dc}$, $V_{BC} = -4V_{dc}$, $V_{CA} = V_{dc}$): Q_{A3} and Q_{S1} are on, linking node A to $3V_{dc}$, Q_{B2} is on, linking node B to ground and Q_{C1} is on, linking node C to $4V_{dc}$. All other switches are off. Figure 3.6(d) shows the current path during this mode.

5. Mode 5 ($V_{AB} = 4V_{dc}$, $V_{BC} = -4V_{dc}$, $V_{CA} = 0$): Q_{A1} is on, linking node A to $4V_{dc}$, Q_{B2} is on, linking node B to ground and Q_{C1} is on, linking node C to $4V_{dc}$. All other switches are off. Figure 3.6(e) shows the current path during this mode.

6. Mode 6 ($V_{AB} = 4V_{dc}$, $V_{BC} = -3V_{dc}$, $V_{CA} = -V_{dc}$): Q_{A1} is on, linking node A to $4V_{dc}$, Q_{B2} is on, linking node B to ground and Q_{C3} and Q_{S1} are on, linking node C to $3V_{dc}$. All other switches are off. Figure 3.6(f) shows the current path during this mode.

7. Mode 7 ($V_{AB} = 4V_{dc}$, $V_{BC} = -2V_{dc}$, $V_{CA} = -2V_{dc}$): Q_{A1} is on, linking node A to $4V_{dc}$, Q_{B2} is on, linking node B to ground and Q_{C3} and Q_{S2} are on, linking node C to

$2V_{dc}$. All other switches are off. Figure 3.6(g) shows the current path during this mode.

8. Mode 8 ($V_{AB} = 4V_{dc}$, $V_{BC} = -V_{dc}$, $V_{CA} = -3V_{dc}$): Q_{A1} is on, linking node A to $4V_{dc}$, Q_{B2} is on, linking node B to ground and Q_{C3} and Q_{S3} are on, linking node C to V_{dc}. All other switches are off. Figure 3.6(h) shows the current path during this mode.

9. Mode 9 ($V_{AB} = 4V_{dc}$, $V_{BC} = 0$, $V_{CA} = -4V_{dc}$): Q_{A1} is on, linking node A to $4V_{dc}$, Q_{B2} is on, linking node B to ground and Q_{C2} is on, linking node C to ground. All other switches are off. Figure 3.6(i) shows the current path during this mode.

10. Mode 10 ($V_{AB} = 3V_{dc}$, $V_{BC} = V_{dc}$, $V_{CA} = -4V_{dc}$): Q_{A1} is on, linking node A to $4V_{dc}$, Q_{B3} and Q_{S3} are on, linking node B to V_{dc} and Q_{C2} is on, linking node C to ground. All other switches are off. Figure 3.6(j) shows the current path during this mode.

11. Mode 11 ($V_{AB} = 2V_{dc}$, $V_{BC} = 2V_{dc}$, $V_{CA} = -4V_{dc}$): Q_{A1} is on, linking node A to $4V_{dc}$, Q_{B3} and Q_{S2} are on, linking node B to $2V_{dc}$ and Q_{C2} is on, linking node C to ground. All other switches are off. Figure 3.6(k) shows the current path during this mode.

12. Mode 12 ($V_{AB} = V_{dc}$, $V_{BC} = 3V_{dc}$, $V_{CA} = -4V_{dc}$): Q_{A1} is on, linking node A to $4V_{dc}$, Q_{B3} and Q_{S1} are on, linking node B to $3V_{dc}$ and Q_{C2} is on, linking node C to ground. All other switches are off. Figure 3.6(l) shows the current path during this mode.

13. Mode 13 ($V_{AB} = 0$, $V_{BC} = 4V_{dc}$, $V_{CA} = -4V_{dc}$): Q_{A1} is on, linking node A to $4V_{dc}$, Q_{B1} is on, linking node B to $4V_{dc}$ and Q_{C2} is on, linking node C to ground. All other switches are off. Figure 3.6(m) shows the current path during this mode.

14. Mode 14 ($V_{AB} = -V_{dc}$, $V_{BC} = 4V_{dc}$, $V_{CA} = -3V_{dc}$): Q_{A3} and Q_{S1} are on, linking node A to $3V_{dc}$, Q_{B1} is on, linking node B to $4V_{dc}$ and Q_{C2} is on, linking node C to

ground. All other switches are off. Figure 3.6(n) shows the current path during this mode.

15. Mode 15 ($V_{AB} = -2V_{dc}$, $V_{BC} = 4V_{dc}$, $V_{CA} = -2V_{dc}$): Q_{A3} and Q_{S2} are on, linking node A to $2V_{dc}$, Q_{B1} is on, linking node B to $4V_{dc}$ and Q_{C2} is on, linking node C to ground. All other switches are off. Figure 3.6(o) shows the current path during this mode.

16. Mode 16 ($V_{AB} = -3V_{dc}$, $V_{BC} = 4V_{dc}$, $V_{CA} = -V_{dc}$): Q_{A3} and Q_{S3} are on, linking node A to V_{dc}, Q_{B1} is on, linking node B to $4V_{dc}$ and Q_{C2} is on, linking node C to ground. All other switches are off. Figure 3.6(p) shows the current path during this mode.

17. Mode 17 ($V_{AB} = -4V_{dc}$, $V_{BC} = 4V_{dc}$, $V_{CA} = 0$): Q_{A2} is on, linking node A to ground, Q_{B1} is on, linking node B to $4V_{dc}$ and Q_{C2} is on, linking node C to ground. All other switches are off. Figure 3.6(q) shows the current path during this mode.

18. Mode 18 ($V_{AB} = -4V_{dc}$, $V_{BC} = 3V_{dc}$, $V_{CA} = V_{dc}$): Q_{A2} is on, linking node A to ground, Q_{B1} is on, linking node B to $4V_{dc}$ and Q_{C3} and Q_{S3} are on, linking node C to V_{dc}. All other switches are off. Figure 3.6(r) shows the current path during this mode.

19. Mode 19 ($V_{AB} = -4V_{dc}$, $V_{BC} = 2V_{dc}$, $V_{CA} = 2V_{dc}$): Q_{A2} is on, linking node A to ground, Q_{B1} is on, linking node B to $4V_{dc}$ and Q_{C3} and Q_{S2} are on, linking node C to $2V_{dc}$. All other switches are off. Figure 3.6(s) shows the current path during this mode.

20. Mode 20 ($V_{AB} = -4V_{dc}$, $V_{BC} = V_{dc}$, $V_{CA} = 3V_{dc}$): Q_{A2} is on, linking node A to ground, Q_{B1} is on, linking node B to $4V_{dc}$ and Q_{C3} and Q_{S1} are on, linking node C to $3V_{dc}$. All other switches are off. Figure 3.6(t) shows the current path during this mode.

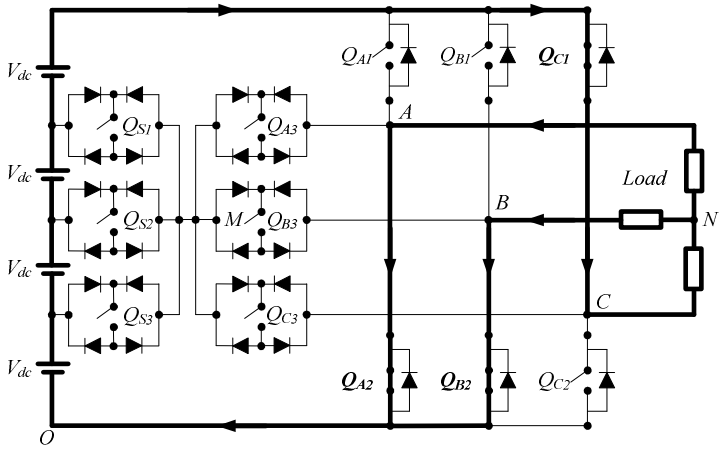
21. Mode 21 (V_{AB} = -4V_{dc}, V_{BC} = 0, V_{CA} = 4V_{dc}): Q_{A2} is on, linking node *A* to ground, Q_{B1} is on, linking node *B* to 4V_{dc} and Q_{C1} is on, linking node *C* to 4V_{dc}. All other switches are off. Figure 3.6(u) shows the current path during this mode.

22. Mode 22 (V_{AB} = -3V_{dc}, V_{BC} = -V_{dc}, V_{CA} = 4V_{dc}): Q_{A2} is on, linking node *A* to ground, Q_{B3} and Q_{S1} are on, linking node *B* to 3V_{dc} and Q_{C1} is on, linking node *C* to 4V_{dc}. All other switches are off. Figure 3.6(v) shows the current path during this mode.

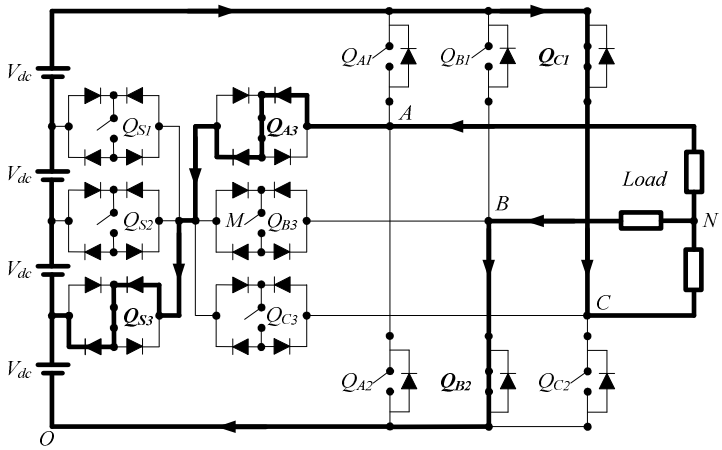
23. Mode 23 (V_{AB} = -2V_{dc}, V_{BC} = -2V_{dc}, V_{CA} = 4V_{dc}): Q_{A2} is on, linking node *A* to ground, Q_{B3} and Q_{S2} are on, linking node *B* to 2V_{dc} and Q_{C1} is on, linking node *C* to 4V_{dc}. All other switches are off. Figure 3.6(w) shows the current path during this mode.

24. Mode 24 (V_{AB} = -V_{dc}, V_{BC} = -3V_{dc}, V_{CA} = 4V_{dc}): Q_{A2} is on, linking node *A* to ground, Q_{B3} and Q_{S3} are on, linking node *B* to V_{dc} and Q_{C1} is on, linking node *C* to 4V_{dc}. All other switches are off. Figure 3.6(x) shows the current path during this mode.

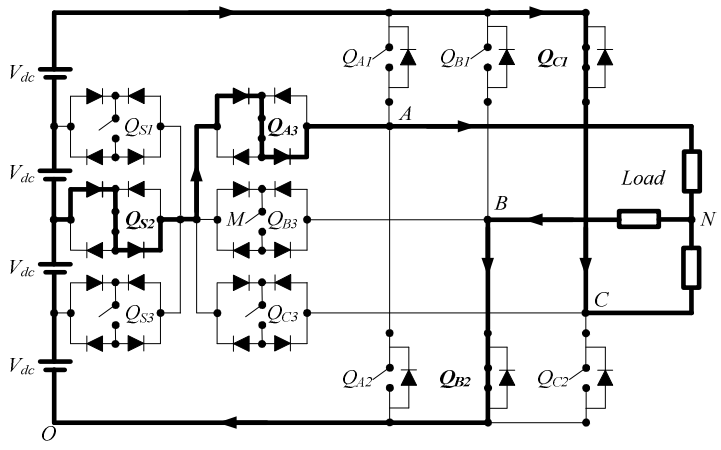
Figure 3.7 shows the switching signals generated to produce line-to-line output voltage waveforms with nine voltage steps. Similar to the four-level inverter, the switches in Module 2 and Module 3 operate at frequencies of respectively double and triple that of Module 1. Six modes of operation only have active switches in Module 1 while those of Module 2 and Module 3 are turned off to generate the maximum, the minimum and zero voltage steps. Other modes of operation have active switches in all modules to produce non-zero voltage steps.



(a) Mode 1 ($V_{AB} = 0$, $V_{BC} = -4V_{dc}$, $V_{CA} = 4V_{dc}$).

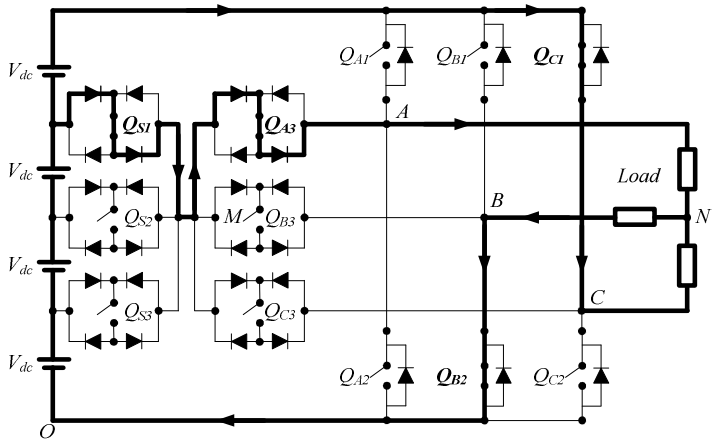


(b) Mode 2 ($V_{AB} = V_{dc}$, $V_{BC} = -4V_{dc}$, $V_{CA} = 3V_{dc}$).

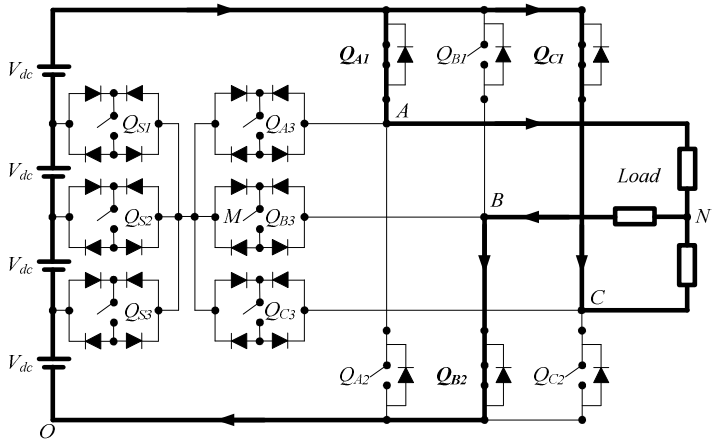


(c) Mode 3 ($V_{AB} = 2V_{dc}$, $V_{BC} = -4V_{dc}$, $V_{CA} = 2V_{dc}$).

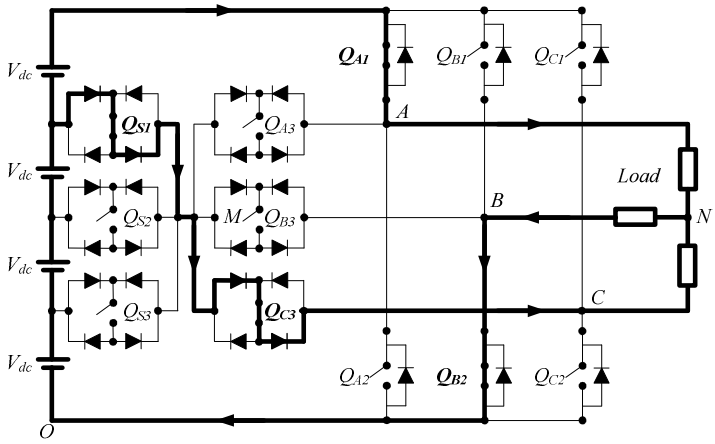
Figure 3.6: Modes of operation of the proposed five-level inverter.



(d) Mode 4 ($V_{AB} = 3V_{dc}$, $V_{BC} = -4V_{dc}$, $V_{CA} = V_{dc}$).

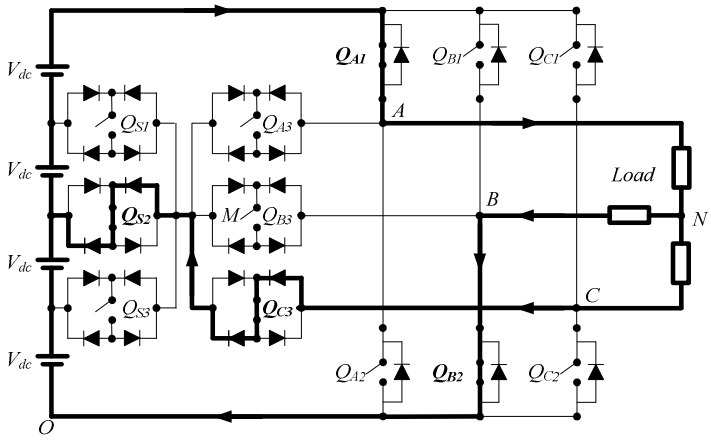


(e) Mode 5 ($V_{AB} = 4V_{dc}$, $V_{BC} = -4V_{dc}$, $V_{CA} = 0$).

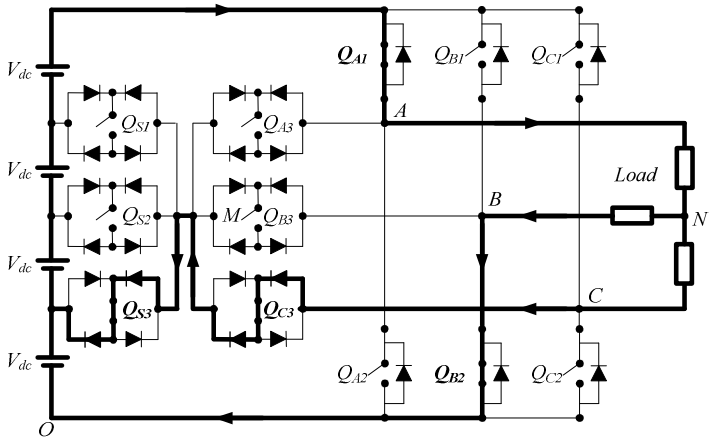


(f) Mode 6 ($V_{AB} = 4V_{dc}$, $V_{BC} = -3V_{dc}$, $V_{CA} = -V_{dc}$).

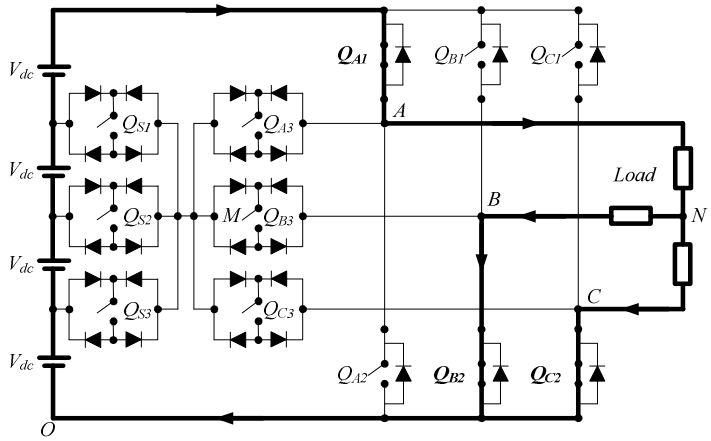
Figure 3.6, continued: Modes of operation of the proposed five-level inverter.



(g) Mode 7 ($V_{AB} = 4V_{dc}$, $V_{BC} = -2V_{dc}$, $V_{CA} = -2V_{dc}$).

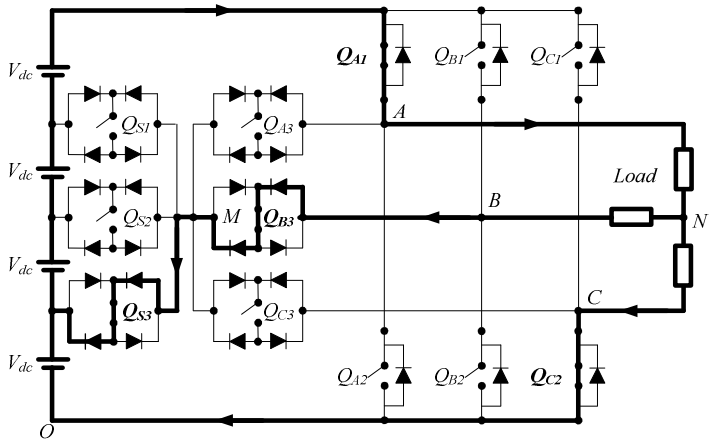


(h) Mode 8 ($V_{AB} = 4V_{dc}$, $V_{BC} = -V_{dc}$, $V_{CA} = -3V_{dc}$).

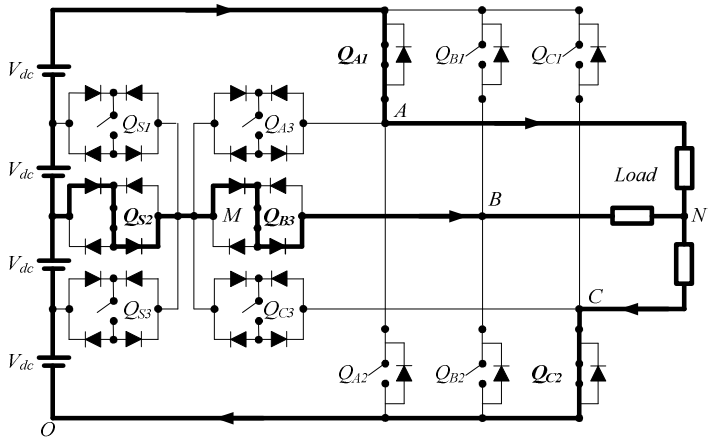


(i) Mode 9 ($V_{AB} = 4V_{dc}$, $V_{BC} = 0$, $V_{CA} = -4V_{dc}$).

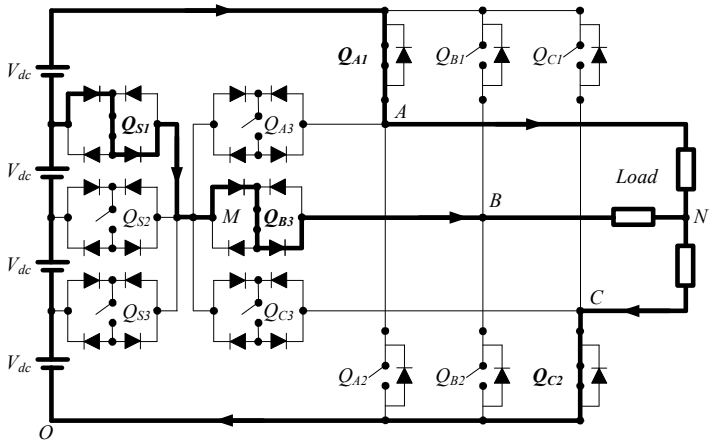
Figure 3.6, continued: Modes of operation of the proposed five-level inverter.



(j) Mode 10 ($V_{AB} = 3V_{dc}$, $V_{BC} = V_{dc}$, $V_{CA} = -4V_{dc}$).

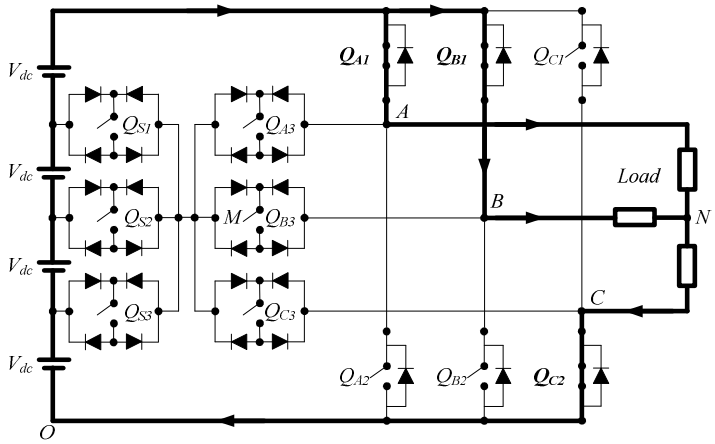


(k) Mode 11 ($V_{AB} = 2V_{dc}$, $V_{BC} = 2V_{dc}$, $V_{CA} = -4V_{dc}$).

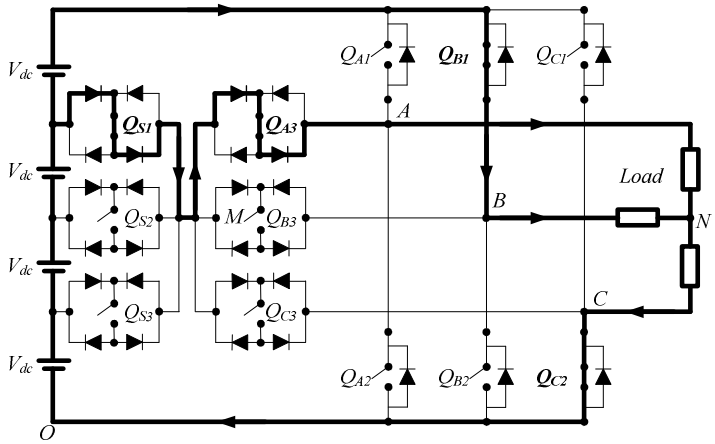


(l) Mode 12 ($V_{AB} = V_{dc}$, $V_{BC} = 3V_{dc}$, $V_{CA} = -4V_{dc}$).

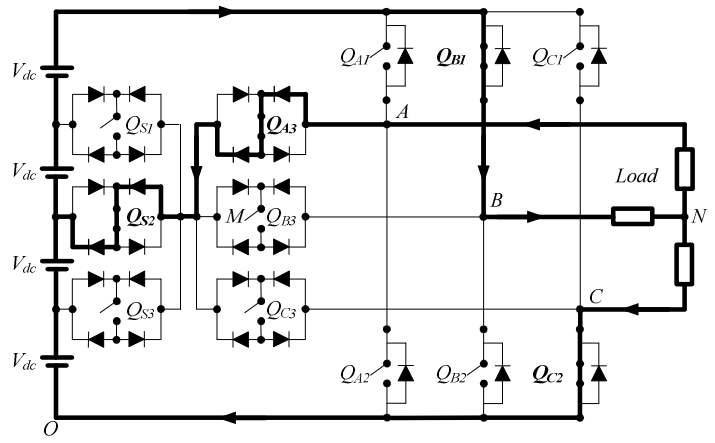
Figure 3.6, continued: Modes of operation of the proposed five-level inverter.



(m) Mode 13 ($V_{AB} = 0$, $V_{BC} = 4V_{dc}$, $V_{CA} = -4V_{dc}$).

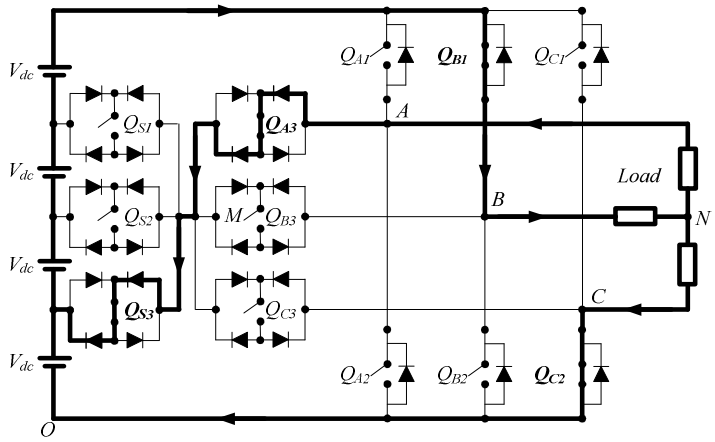


(n) Mode 14 ($V_{AB} = -V_{dc}$, $V_{BC} = 4V_{dc}$, $V_{CA} = -3V_{dc}$).

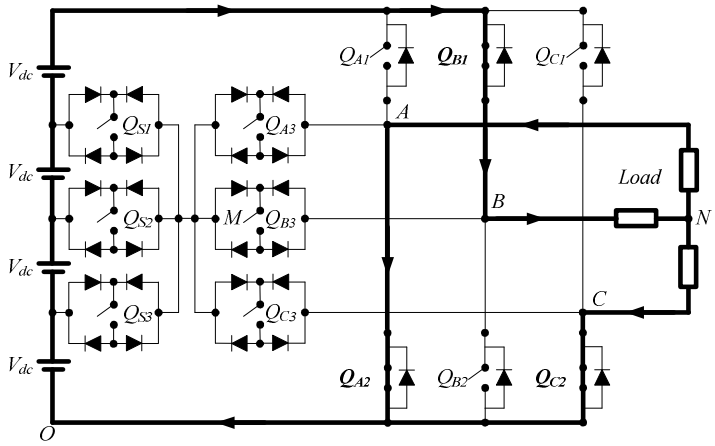


(o) Mode 15 ($V_{AB} = -2V_{dc}$, $V_{BC} = 4V_{dc}$, $V_{CA} = -2V_{dc}$).

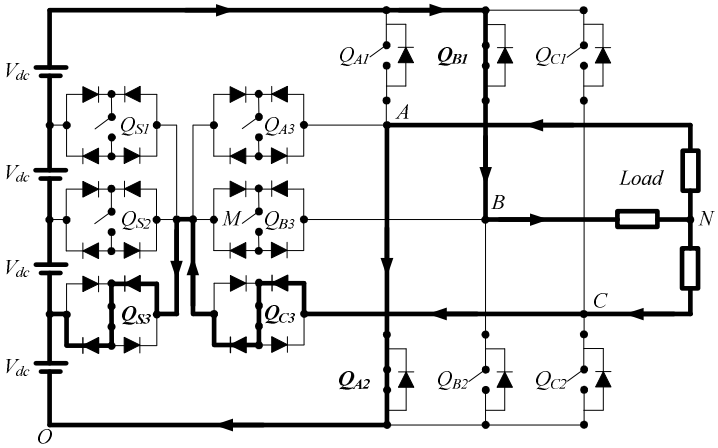
Figure 3.6, continued: Modes of operation of the proposed five-level inverter.



(p) Mode 16 (V_{AB} = -3V_{dc}, V_{BC} = 4V_{dc}, V_{CA} = -V_{dc}).

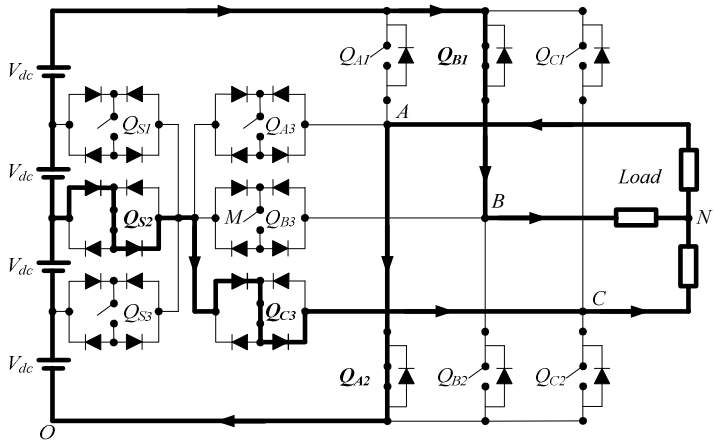


(q) Mode 17 (V_{AB} = -4V_{dc}, V_{BC} = 4V_{dc}, V_{CA} = 0).

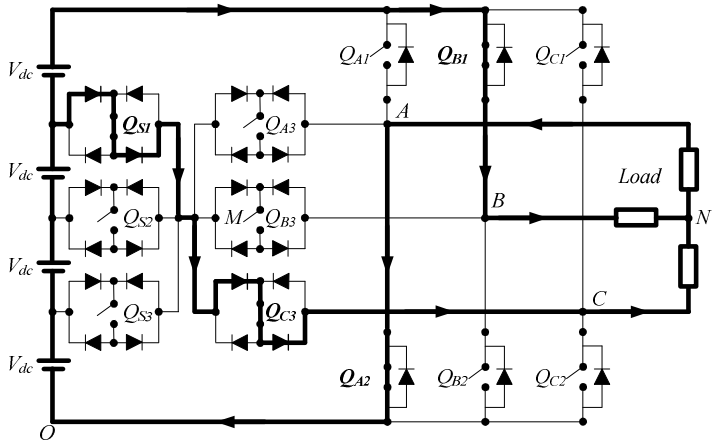


(r) Mode 18 (V_{AB} = -4V_{dc}, V_{BC} = 3V_{dc}, V_{CA} = V_{dc}).

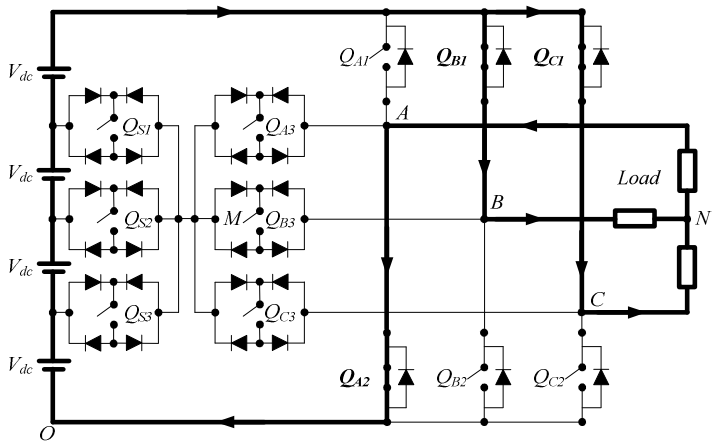
Figure 3.6, continued: Modes of operation of the proposed five-level inverter.



(s) Mode 19 (V_{AB} = -4V_{dc}, V_{BC} = 2V_{dc}, V_{CA} = 2V_{dc}).

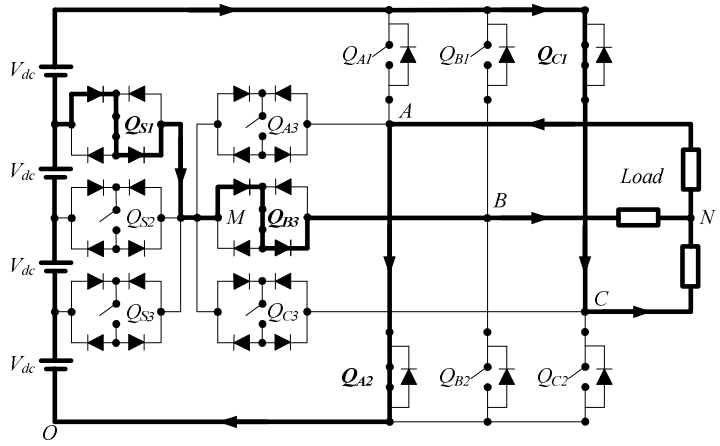


(t) Mode 20 (V_{AB} = -4V_{dc}, V_{BC} = V_{dc}, V_{CA} = 3V_{dc}).

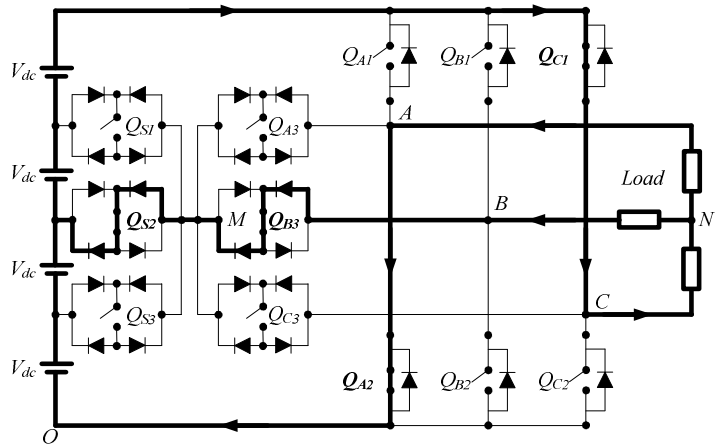


(u) Mode 21 (V_{AB} = -4V_{dc}, V_{BC} = 0, V_{CA} = 4V_{dc}).

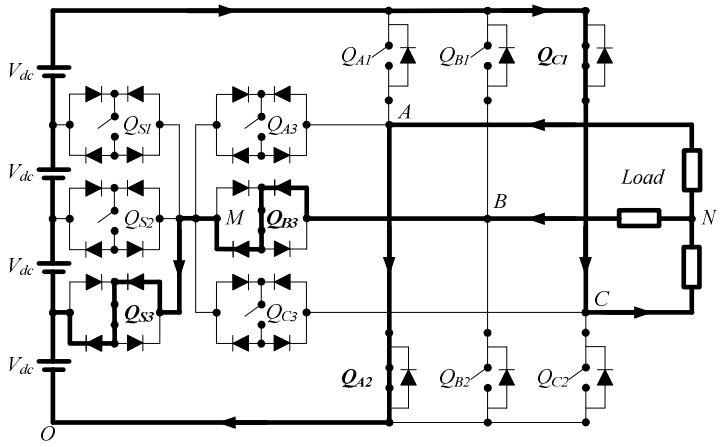
Figure 3.6, continued: Modes of operation of the proposed five-level inverter.



(v) Mode 22 (V_{AB} = -3V_{dc}, V_{BC} = -V_{dc}, V_{CA} = 4V_{dc}).



(w) Mode 23 (V_{AB} = -2V_{dc}, V_{BC} = -2V_{dc}, V_{CA} = 4V_{dc}).



(x) Mode 24 (V_{AB} = -V_{dc}, V_{BC} = -3V_{dc}, V_{CA} = 4V_{dc}).

Figure 3.6, continued: Modes of operation of the proposed five-level inverter.

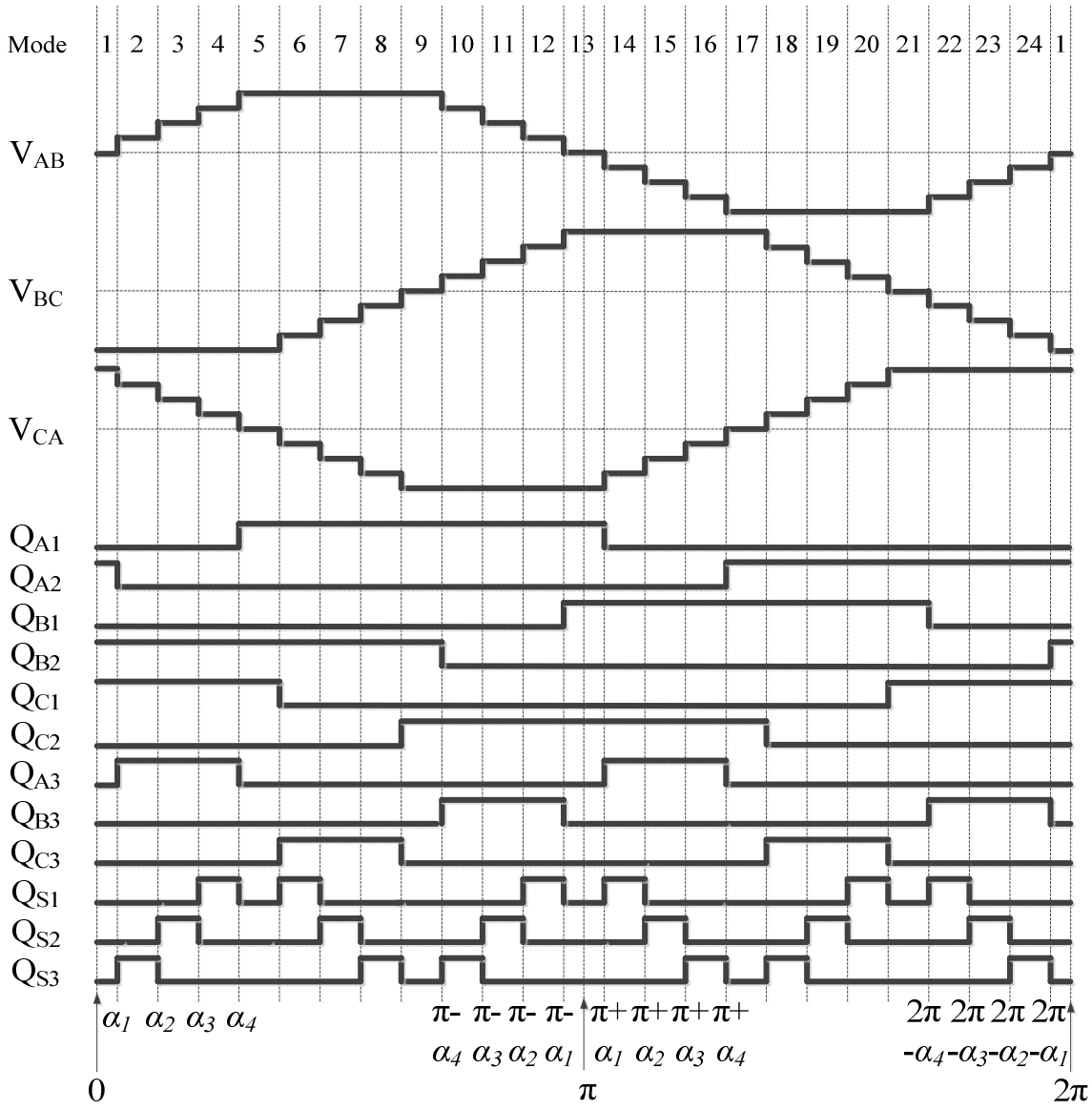


Figure 3.7: Switching signals to generate output voltages with nine voltage steps.

3.4 Novel SVPWM for the Proposed Topology

Since four-level and five-level inverters of the proposed topology are considered as multilevel inverters with low number of voltage levels, a high switching frequency method is therefore adopted. SVPWM is selected in this work. This section provides the steps to implement SVPWM for the proposed topology with the focus on four-level and five-level configurations.

3.4.1 Switching States

To define the switching states of the four-level inverter, Figure 3.2 is used as the reference. Consider one phase, say phase A. The switches involved with this phase are Q_{A1} and Q_{A2} from Module 1 and Q_{A3} from Module 2. The switches from Module 3 namely Q_{S1}, and Q_{S2} are made for common use for the three phases as to optimize their usage. Here, V_{AO} is also used as the reference parameter to define the switching states. Let denote switching state for phase A as S_A. Through appropriate switching, the following are obtained:

1. When Q_{A1} is switched on while others are switched off, V_{AO} becomes $3V_{dc}$.
2. When Q_{A2} is switched on while others are switched off, V_{AO} becomes 0.
3. When Q_{A3} and Q_{S1} are switched on while others are switched off, V_{AO} becomes $2V_{dc}$.
4. When Q_{A3} and Q_{S2} are switched on while others are switched off, V_{AO} becomes V_{dc}.

By applying equation (3.1) below, four switching states are defined.

$$S_A = \frac{V_{AO}}{V_{dc}} \tag{3.1}$$

The same can be applied for phase B and phase C as well. By using subscript K to represent A, B and C, a generalized definition of switching states can be made. Table 3.1 details the derived switching states.

The same steps can be repeated to define the switching states of the five-level inverter with the aid of Figure 3.5. In reference to phase A, the following can be described:

1. When Q_{A1} is switched on while others are switched off, V_{AO} becomes $4V_{dc}$.
2. When Q_{A2} is switched on while others are switched off, V_{AO} becomes 0.

3. When Q_{A3} and Q_{S1} are switched on while others are switched off, V_{AO} becomes $3V_{dc}$.

4. When Q_{A3} and Q_{S2} are switched on while others are switched off, V_{AO} becomes $2V_{dc}$.

5. When Q_{A3} and Q_{S3} are switched on while others are switched off, V_{AO} becomes V_{dc}.

Using equation (3.1), five switching states can be derived for the five-level inverter as listed in Table 3.2.

Table 3.2 Switching states for the proposed four-level inverter

(with respect to Figure 3.2).

Switching states (S_K)	Active switches			Voltage level (V_{KO})
	Module 1	Module 2	Module 3	
0	Q_{K2}			0
1		Q_{K3}	Q_{S2}	V_{dc}
2		Q_{K3}	Q_{S1}	$2V_{dc}$
3	Q_{K1}			$3V_{dc}$

Table 3.3 Switching states for the proposed five-level inverter

(with respect to Figure 3.5).

Switching states (S_K)	Active switches			Voltage level (V_{KO})
	Module 1	Module 2	Module 3	
0	Q_{K2}			0
1		Q_{K3}	Q_{S3}	V_{dc}
2		Q_{K3}	Q_{S2}	$2V_{dc}$
3		Q_{K3}	Q_{S1}	$3V_{dc}$
4	Q_{K1}			$4V_{dc}$

3.4.2 Voltage Vectors

Switching state combinations in the form of $S_AS_BS_C$ can be generated by combining all the switching states of the three phases. To obtain all allowable combinations, a condition must be fulfilled. The fact that each bidirectional switch in Module 3 operates in optimized mode dictates that only one switch is turned on at any

particular time as to avoid a short circuit across the DC sources. In the optimized mode, the operation of the switch that is turned on, is divided among phase A, phase B and phase C. Consequently, switching states 1, 2 and 3 cannot exist at the same time. Therefore, several switching state combinations are not allowed. For example, combination 210 is invalid because $S_A = 2$ and $S_B = 1$ occur simultaneously. This is not permitted since two bidirectional switches in Module 3 are both active. By taking this condition into account, the total allowable combinations for the four-level and five-level inverters are 46 and 65 respectively. To obtain the line-to-line and phase output voltages from given switching states, the following are derived:

From equation (3.1),

$$V_{AO} = S_A V_{dc} \tag{3.2}$$

Similarly,

$$V_{BO} = S_B V_{dc} \tag{3.3}$$

and

$$V_{CO} = S_C V_{dc} \tag{3.4}$$

From Figures 3.2 and 3.5, line-to-line voltages can be expressed as follows:

$$\begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix} = \begin{bmatrix} V_{AO} - V_{BO} \\ V_{BO} - V_{CO} \\ V_{CO} - V_{AO} \end{bmatrix} \tag{3.5}$$

Substituting equations (3.2), (3.3) and (3.4) into equation (3.5), the line-to-line output voltages can be expressed in terms of the switching states as given below:

$$\begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix} = V_{dc} \begin{bmatrix} S_A - S_B \\ S_B - S_C \\ S_C - S_A \end{bmatrix} \tag{3.6}$$

Also, from Figures (3.2) and (3.5),

$$\begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} = \begin{bmatrix} V_{AO} - V_{NO} \\ V_{BO} - V_{NO} \\ V_{CO} - V_{NO} \end{bmatrix} \tag{3.7}$$

and,

$$V_{AN} + V_{BN} + V_{CN} = 0 \tag{3.8}$$

Substituting equation (3.7) into equation (3.8), then

$$V_{NO} = \frac{1}{3}\left(V_{AO} + V_{BO} + V_{CO}\right) \tag{3.9}$$

Using equations (3.2), (3.3) and (3.4), equation (3.9) becomes

$$V_{NO} = \frac{V_{dc}}{3}\left(S_A + S_B + S_C\right) \tag{3.10}$$

Substituting equations (3.2), (3.3), (3.4) and (3.10) into equation (3.7), the phase output voltages can be expressed in terms of the switching states as the following:

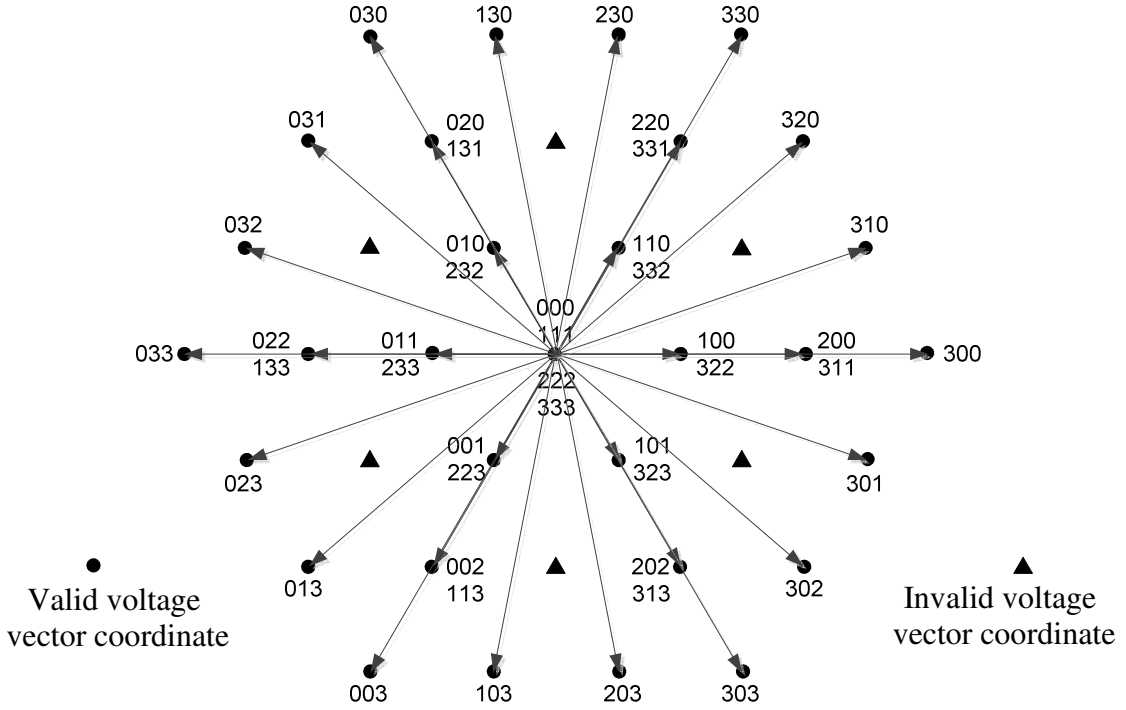
$$\begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2S_A - S_B - S_C \\ 2S_B - S_C - S_A \\ 2S_C - S_A - S_B \end{bmatrix} \tag{3.11}$$

To transform the voltage values in the *ABC* frame into those of the *αβ* frame, Park's transformation (Massoud, Finney, & Williams, 2008) below is applied:

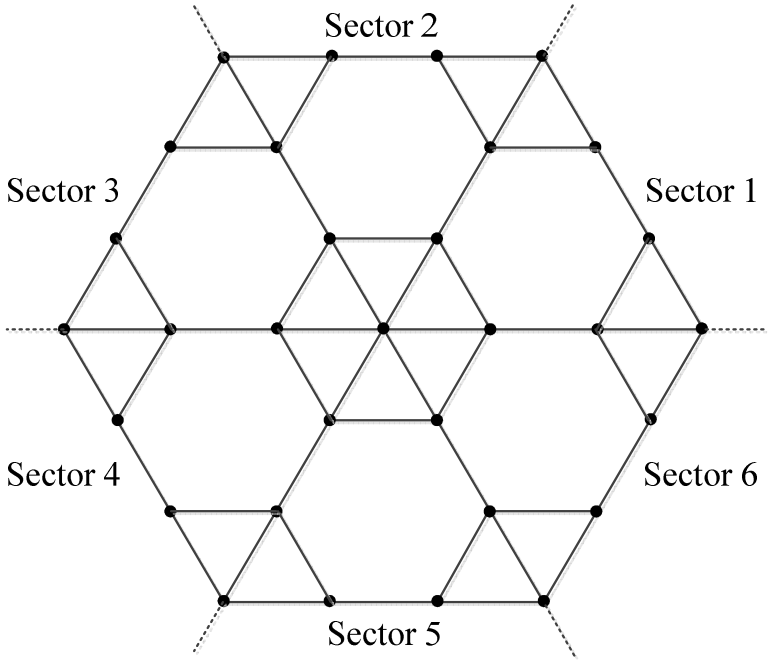
$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} \tag{3.12}$$

The transformation results in the generation of 31 and 43 voltage vectors for the four-level and five-level inverters respectively. Figure 3.8 portrays the overall voltage vectors on *αβ* frame and the resulting vector hexagon respectively for the four-level inverter. Those are also displayed for the case of five-level inverter in Figure 3.9. It can

be observed that the vector hexagons obtained are different from the conventional four-level and five-level hexagons depicted in Figure 3.10.

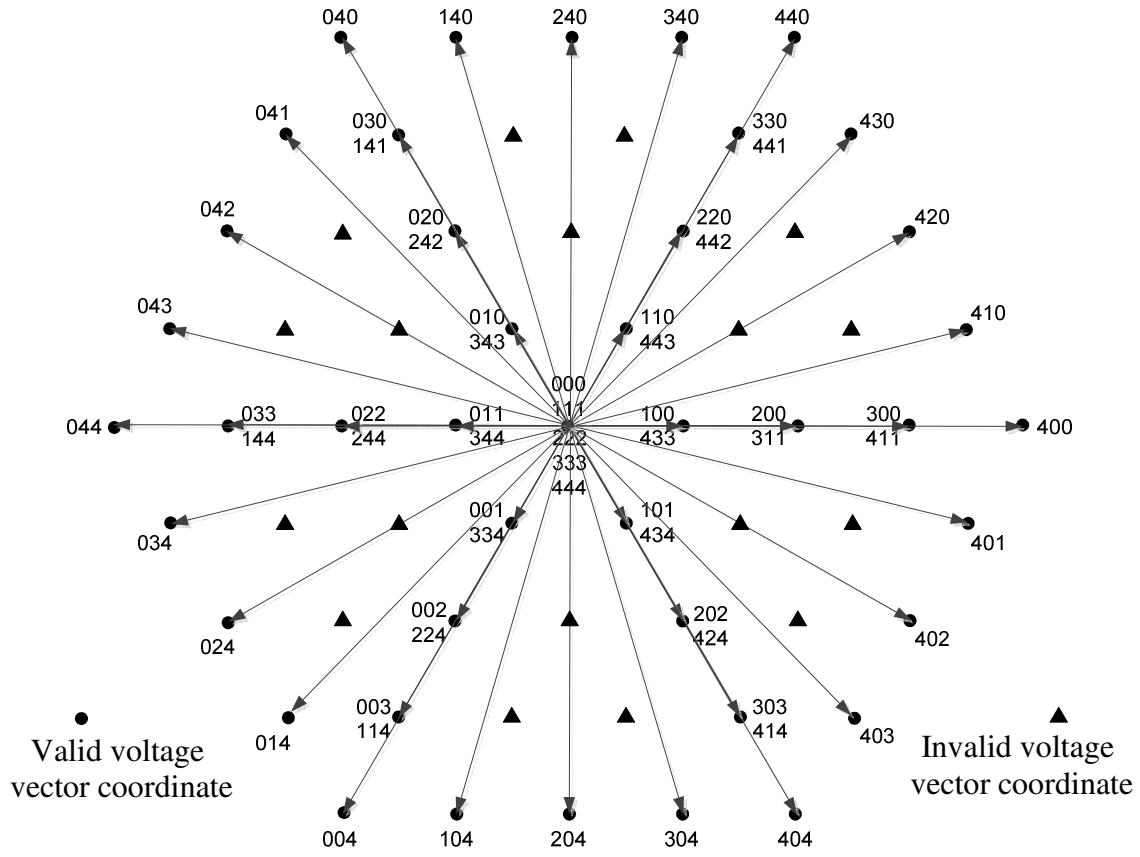


(a) Voltage vectors on $\alpha\beta$-plane.

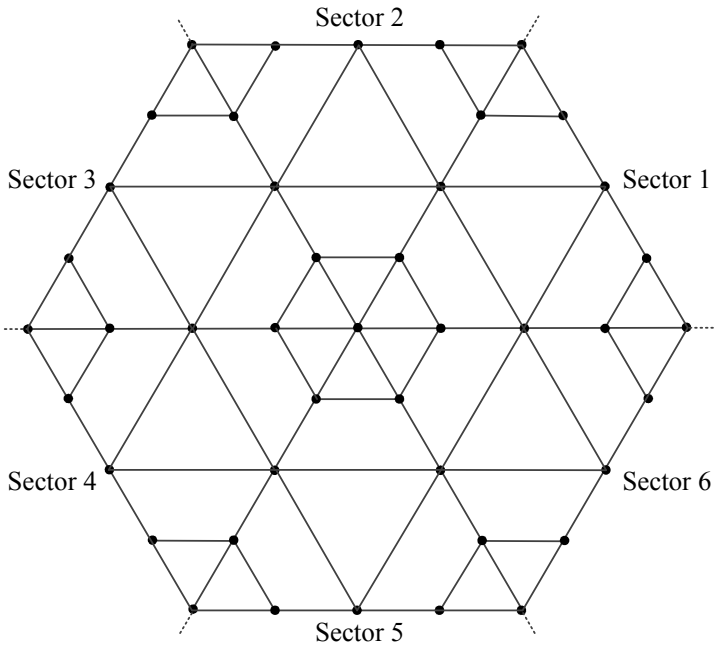


(b) Vector hexagon.

Figure 3.8: Voltage vectors and the resulting vector hexagon for the proposed four-level inverter.

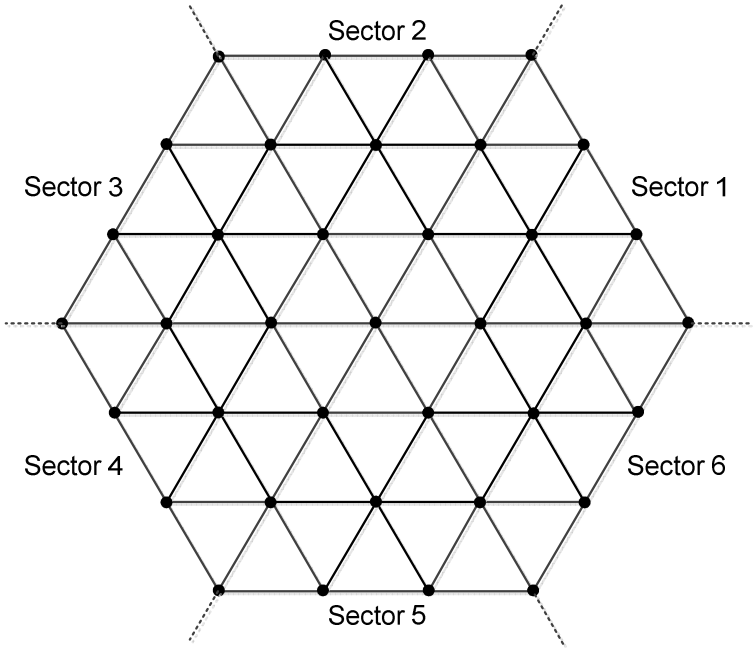


(a) Voltage vectors on $\alpha\beta$-plane.

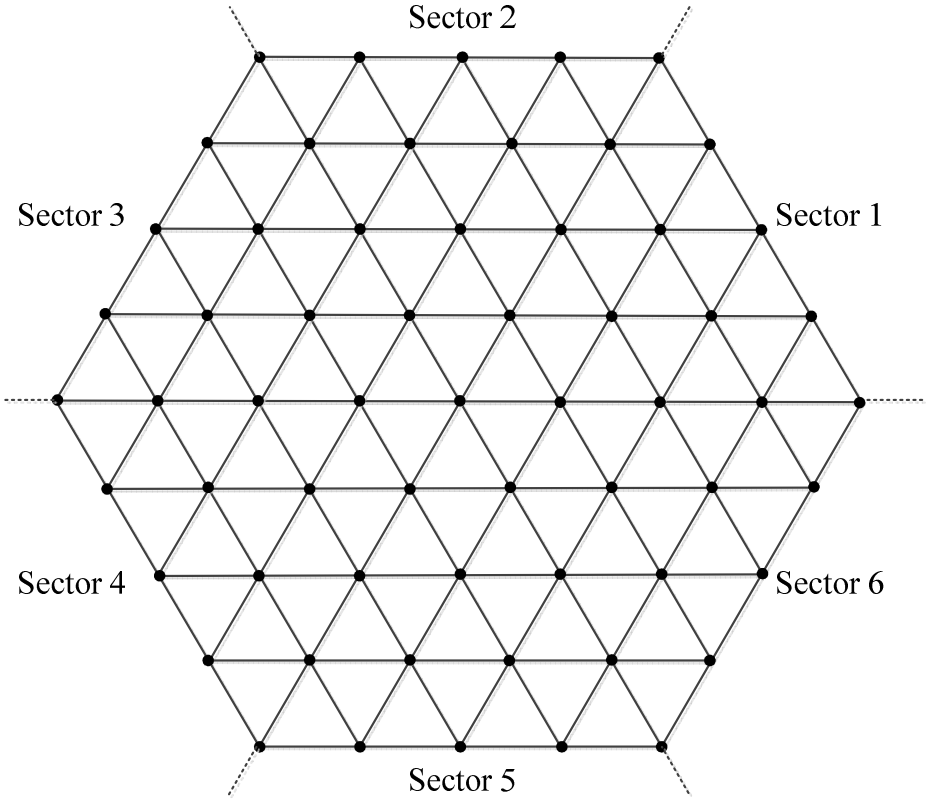


(b) Vector hexagon.

Figure 3.9: Voltage vectors and the resulting vector hexagon for the proposed five-level inverter.



(a) Conventional four-level vector hexagon.



(b) Conventional five-level vector hexagon.

Figure 3.10: Conventional vector hexagons.

3.4.3 Virtual Voltage Vectors

The introduction of Module 3 in the proposed topology leads to the fact that several switching state combinations are invalid and must not be used. This causes the elimination of some voltage vectors as seen in Figure 3.8(a) and Figure 3.9(a). Since the voltage hexagons of the proposed topology are different from the ordinary ones, the conventional space vector concept cannot be directly applied. Therefore, certain modifications are made to adapt to the changes reflected in the vector hexagons.

3.4.3.1 Four-Level Inverter

The condition imposed in producing the voltage vectors as mentioned above causes the elimination of six vectors of magnitude $\sqrt{3}V_{dc}$. As a result, each sector comprises a hexagon and 3 equilateral triangles as opposed to 9 triangles in a normal sector. A problem arises when decomposing the reference vector in the hexagon within the sector. Six nearest vectors that form the hexagon have to be considered in order to represent the reference vector. This contributes to complication in computing the on-state time of each of the six vectors. To avoid this difficulty, a novel method is developed in which six virtual vectors are introduced as shown in Figure 3.11. Each of the virtual vectors (V_{V1}, V_{V2}, V_{V3}, V_{V4}, V_{V5} and V_{V6}) in the figure has a magnitude of $\sqrt{3}V_{dc}$ and is positioned at the center of each hexagon.

To describe the method in more detail, consider sector 1 of the vector hexagon as shown in Figure 3.12. Virtual vector V_{V1} of magnitude of $\sqrt{3}V_{dc}$ is introduced so that three virtual boundaries can be drawn. Each virtual boundary connects two opposite voltage vectors and it has to pass through the virtual vector's location to obtain a straight-line boundary. With the virtual boundaries, nine triangles can be formed in which six of them have two virtual sides each. Any voltage reference vector that falls in triangles 1, 5

and 9 in Figure 3.12 can be represented by a sum of different portions of the three nearest vectors that form the triangles. In other words, the conventional space vector concept applies. However, if the reference vector lies in any of the other triangles namely triangles 2,3,4,6,7 and 8, two nearest vectors are only considered to represent the reference vector. The same applies to the remaining sectors. Figure 3.13 portrays the modified vector hexagon with the virtual boundaries.

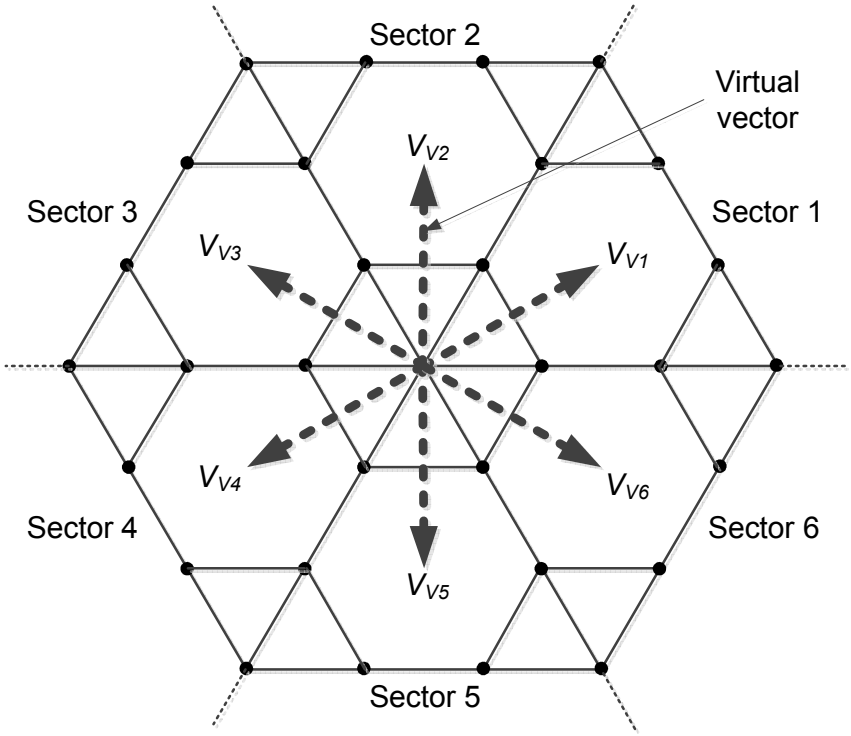


Figure 3.11: Location of the introduced virtual vectors in the proposed four-level vector hexagon.

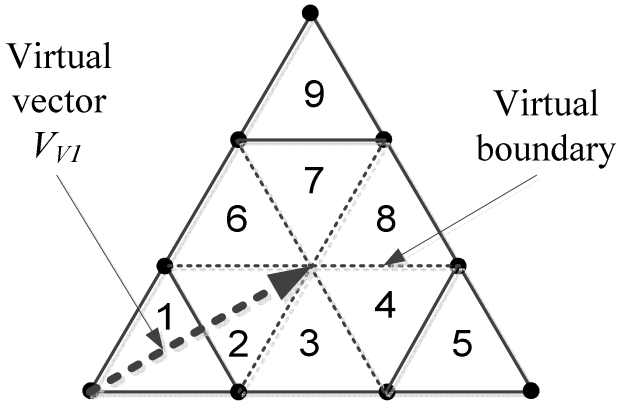


Figure 3.12: The formation of nine triangles in sector 1 as a result of the presence of virtual vector V_{V1}.

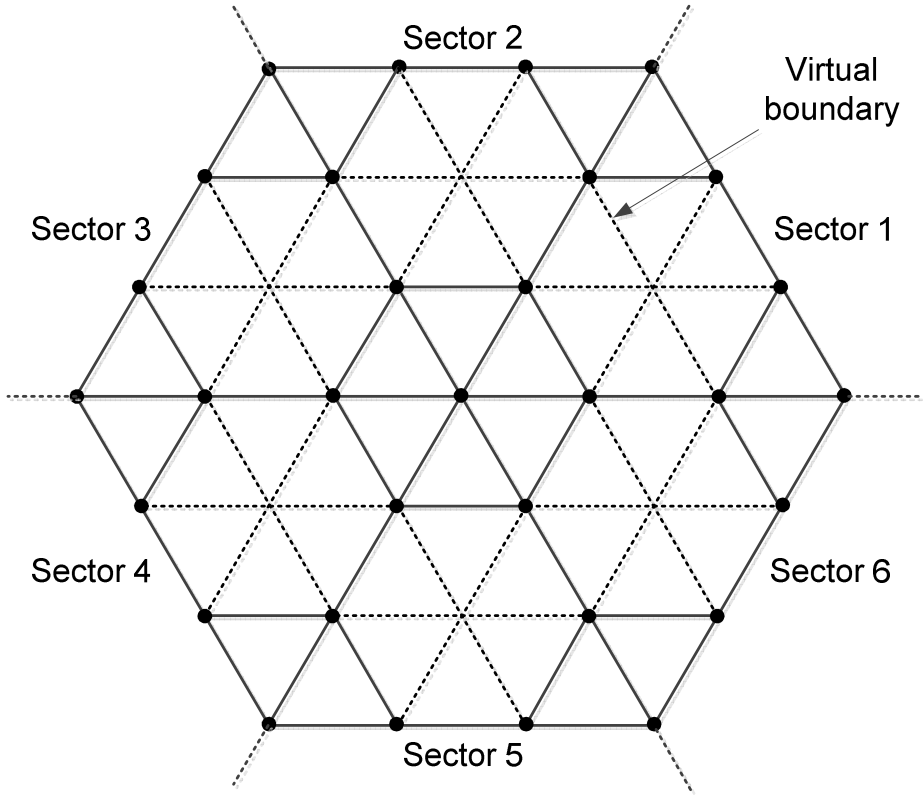


Figure 3.13: The modified vector hexagon with virtual boundaries for the proposed four-level inverter.

3.4.3.2 Five-Level Inverter

For the proposed five-level inverter, the removal of invalid switching state combinations leads to the elimination of 6 voltage vectors of magnitude $\sqrt{3}V_{dc}$ and 12 voltage vectors of magnitude $\sqrt{7}V_{dc}$. As a result, every sector consists of a large triangle in the middle and three small triangles at the three vertices which are separated between them by three trapeziums, as depicted in Figure 3.9(b). A problem arises when a given reference vector falls in the trapezium. Here, four nearest vectors have to be considered and this complicates the reference vector decomposition process. To provide a solution to this problem, virtual vectors are utilized. Six virtual vectors of magnitude $\sqrt{3}V_{dc}$ (V_{X1}, V_{X2}, V_{X3}, V_{X4}, V_{X5} and V_{X6}) and 12 additional virtual vectors of magnitude $\sqrt{7}V_{dc}$ (V_{Y1}, V_{Y2}, V_{Y3}, V_{Y4}, V_{Y5}, V_{Y6}, V_{Y7}, V_{Y8}, V_{Y9}, V_{Y10}, V_{Y11} and V_{Y12}) are introduced and positioned at the coordinates shown in Figure 3.14.

To illustrate the role of the virtual vectors in simplifying reference voltage decomposition, sector 1 is considered. As displayed in Figure 3.15, three virtual vectors V_{X1} (amplitude of $\sqrt{3}V_{dc}$), V_{Y1} (amplitude of $\sqrt{7}V_{dc}$) and V_{Y2} (amplitude of $\sqrt{7}V_{dc}$) are introduced. The idea behind these virtual vectors is to break each trapezium in the sector into three triangles. This is done by joining the virtual vectors to the opposite voltage vectors via virtual boundaries. By adopting this method, one large triangle in the middle and 12 small triangles can be formed including those created with one or two virtual sides. Any reference vector that falls in triangles 1, 6, 12 and 13 can be represented by a sum of different portions of the three nearest vectors that form the triangles. For the case when the reference vector lies in any of the other triangles namely triangles 2,3,4,5,7,8,9,10 and 11, two nearest vectors are only considered to represent the reference vector instead. The same is true for all of the other sectors. Figure 3.16 shows the modified vector hexagon with the virtual boundaries.

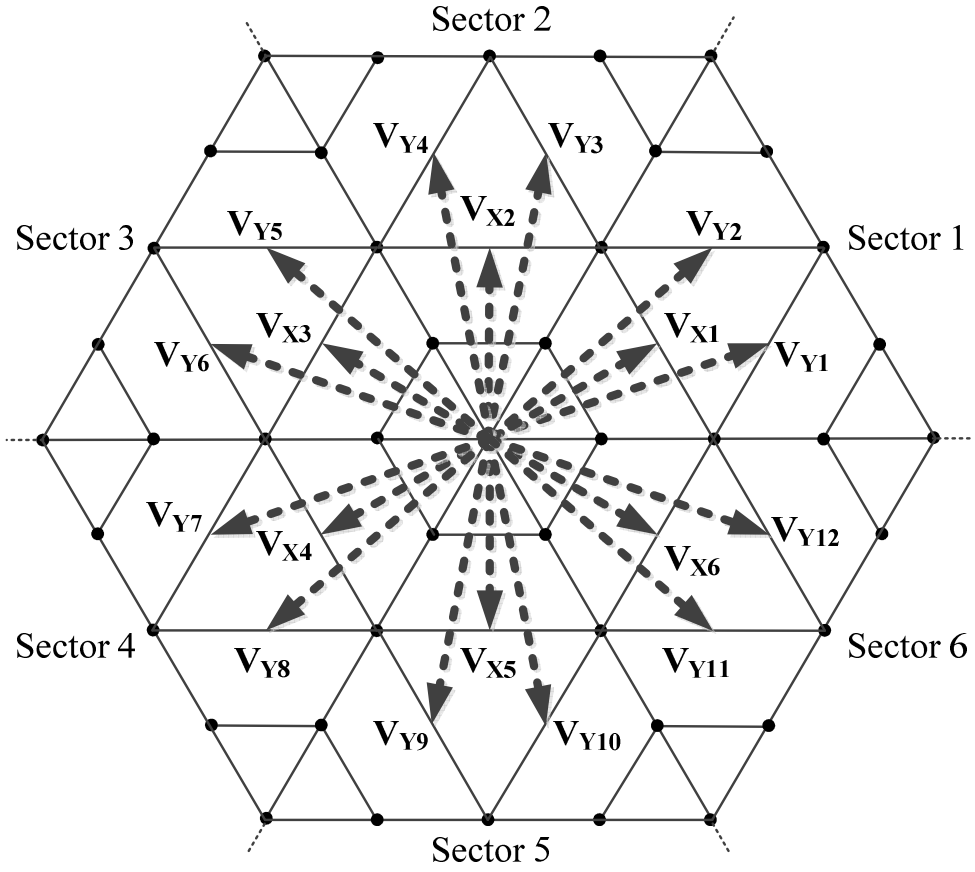


Figure 3.14: Location of the introduced virtual vectors in the proposed five-level vector hexagon.

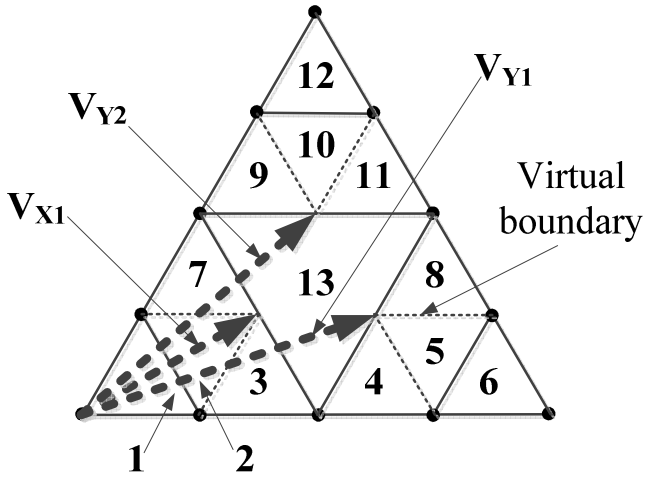


Figure 3.15: The formation of 13 triangles in sector 1 as a result of the presence of virtual vectors V_{X1}, V_{Y1} and V_{Y2}.

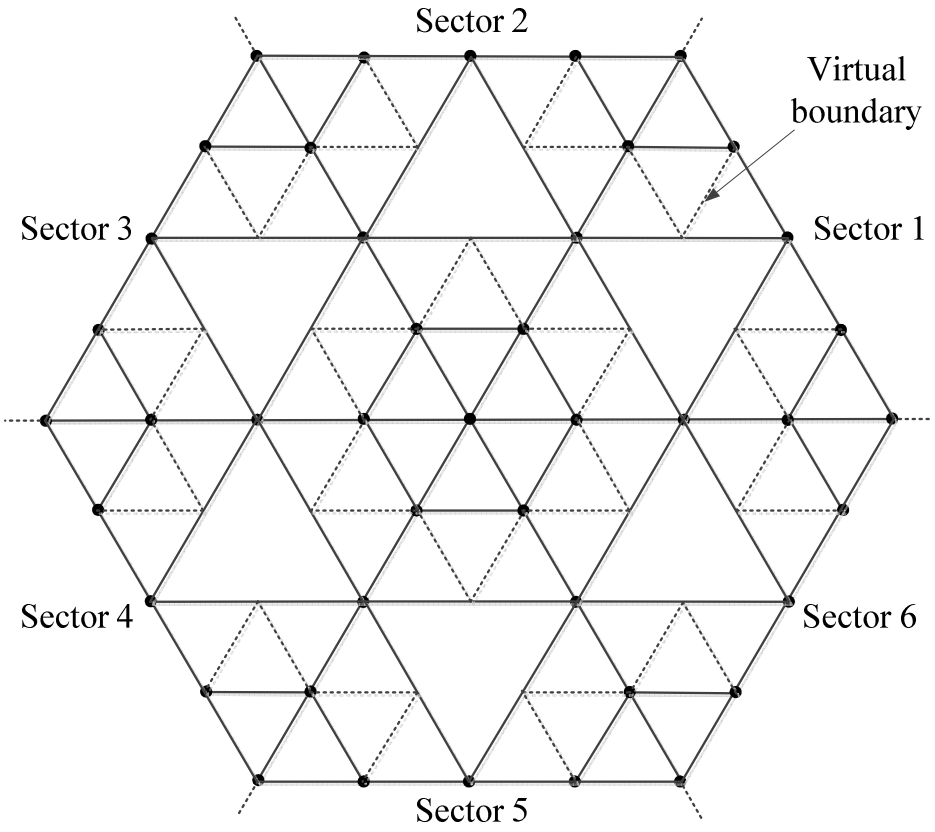


Figure 3.16: The modified vector hexagon with virtual boundaries for the proposed five-level inverter.

3.4.4 Conversion to 60° *gh*-plane Coordinate System

The $\alpha\beta$ coordinate system has two axes which are perpendicular to each other namely horizontal or α-axis and vertical or β-axis. The transformation into the $\alpha\beta$-plane introduces an obvious drawback. V_α and V_β calculated from equation (3.12) result in floating-point values. For example, for switching state combination 430, the corresponding V_α and V_β values are $\frac{5}{2}V_{dc}$ and $\frac{3\sqrt{3}}{2}V_{dc}$ respectively. The use of floating-point values in the subsequent calculation of on-state times for the power switches will lead to complexity and a time-consuming process. This may also pose a serious problem in terms of practical implementation using low-cost processors which

mostly deal with fixed-point values. Due to these challenges, it is imperative to get the values of the voltage vector coordinates in fixed-point or integer form.

To obtain the desired voltage vector coordinates, the 60° coordinate system is employed (Sanmin, Bin, Fahai, & Congwei, 2003). This coordinate system has two axes in which one of them is in horizontal position (*g*-axis), while the other (*h*-axis) is inclined at an angle of 60° from the horizontal axis as shown in Figure 3.17. To convert the space vector coordinates from *αβ*-plane to *gh*-plane, the following apply:

$$V_g = V_{ref}\left(\cos\theta_{ref} - \frac{\sin\theta_{ref}}{\sqrt{3}}\right) \tag{3.13}$$

$$V_h = V_{ref}\left(\frac{2\sin\theta_{ref}}{\sqrt{3}}\right) \tag{3.14}$$

where

$$V_{ref} = \sqrt{V_\alpha{}^2 + V_\beta{}^2} \tag{3.15}$$

and $$\theta_{ref} = \tan^{-1}\left(\frac{V_\beta}{V_\alpha}\right) \tag{3.16}$$

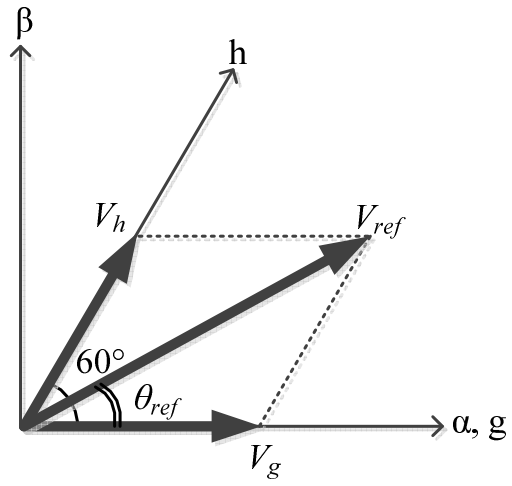


Figure 3.17: The 60° *gh*-plane coordinate system.

By this conversion, all values of V_g and V_h are expressed in integer form. For instance, referring back to switching state combination 430, the corresponding V_g and V_h values are V_{dc} and $3V_{dc}$ respectively.

3.4.5 On-State Time of the Nearest Vectors

In the proposed SVPWM technique, the reference voltage vector is decomposed using one of the two ways, depending on the location of the reference vector on the $\alpha\beta$ or gh plane. If the reference vector is located in a real triangle, then the vector is decomposed using three nearest vectors. If it lies in a virtual triangle, two nearest vectors are used to represent it. A virtual triangle is the triangular zone in the vector hexagon that has at least one virtual side. A real triangle has none virtual side. Depending on the decomposition method employed, the on-state times of the nearest vectors are then calculated accordingly.

If three nearest vectors are used to represent the reference voltage vector, then equations (2.13), (2.14) and (2.15) are employed to determine the on-state times of the three nearest vectors. To calculate the on-state times using gh values, equations (2.13) and (2.14) become the following:

$$V_{1,g}T_1 + V_{2,g}T_2 + V_{3,g}T_3 = V_{ref,g}T_s \tag{3.17}$$

$$V_{1,h}T_1 + V_{2,h}T_2 + V_{3,h}T_3 = V_{ref,h}T_s \tag{3.18}$$

$V_{1,g}$, $V_{2,g}$ and $V_{3,g}$ are the three vectors' components in g-axis while $V_{1,h}$, $V_{2,h}$ and $V_{3,h}$ refer to those in h-axis.

On the other hand, if two nearest vectors are utilized instead, then the following steps are taken to derive the equations for the on-state times T_1 and T_2:

1. From equations (3.17), (3.18) and (2.15), by removing the terms related to the third nearest voltage vector, the following are obtained:

$$V_{1,g}T_1 + V_{2,g}T_2 = V_{ref,g}T_s \tag{3.19}$$

$$V_{1,h}T_1 + V_{2,h}T_2 = V_{ref,h}T_s \tag{3.20}$$

$$T_1 + T_2 = T_s \tag{3.21}$$

2. From equations (3.19), (3.20) and (3.21), T_1 and T_2 can be solved by either using the values in *g*-axis only or the values in *h*-axis only as described below:

Solution 1 (using values in *g*-axis only):

For this solution, equations (3.19) and (3.21) are used. T_1 and T_2 in the equations are rewritten as $T_{1,g}$ and $T_{2,g}$ respectively based on the fact that the on-state times are calculated using the values in *g*-axis only.

By rearranging equation (3.21), the following is obtained:

$$T_{2,g} = T_s - T_{1,g} \tag{3.22}$$

By substituting equation (3.22) into equation (3.19), $T_{1,g}$ can be determined and the result is the following:

$$T_{1,g} = \frac{V_{ref,g} - V_{2,g}}{V_{1,g} - V_{2,g}} T_s \tag{3.23}$$

By substituting equation (3.23) into equation (3.22), $T_{2,g}$ can be expressed as follows:

$$T_{2,g} = \left[1 - \frac{V_{ref,g} - V_{2,g}}{V_{1,g} - V_{2,g}}\right] T_s \tag{3.24}$$

Solution 2 (using values in *h*-axis only):

For this solution, equations (3.20) and (3.21) are used. T_1 and T_2 in the equations are rewritten as $T_{1,h}$ and $T_{2,h}$ respectively to reflect the use of the values in *h*-axis only to calculate the on-state times.

By rearranging equation (3.21), the following is obtained:

$$T_{1,h} = T_s - T_{2,h} \tag{3.25}$$

By substituting equation (3.25) into equation (3.20), $T_{2,h}$ can be determined and the result is the following:

$$T_{2,h} = \frac{V_{ref,h} - V_{1,h}}{V_{2,h} - V_{1,h}} T_s \tag{3.26}$$

By substituting equation (3.26) into equation (3.25), $T_{1,h}$ can be expressed as follows:

$$T_{1,h} = \left[1 - \frac{V_{ref,h} - V_{1,h}}{V_{2,h} - V_{1,h}}\right] T_s \tag{3.27}$$

3. To take into account the results of both Solution 1 and Solution 2, the average of the two is calculated to obtain T_1 and T_2 as expressed below:

$$T_1 = \frac{T_{1,g} + T_{1,h}}{2} \tag{3.29}$$

$$T_2 = \frac{T_{2,g} + T_{2,h}}{2} \tag{3.30}$$

4. Equations (3.23) and (3.26) may lead to infinity if the denominator equals zero. Therefore, to avoid that, the following conditions are imposed to ensure that $T_{1,g}$ and $T_{2,h}$ do not become infinity.

$$V_{1,g} - V_{2,g} \neq 0 \tag{3.31}$$

$$V_{2,h} - V_{1,h} \neq 0 \tag{3.32}$$

If equation (3.31) is not satisfied, then the result of Solution 1 is ignored. Therefore, equations (3.29) and (3.30) do not apply. As a result, $T_1 = T_{1,h}$ and $T_2 = T_{2,h}$.

Similarly, if equation (3.32) is violated, then the result of Solution 2 is no longer counted. Therefore, equations (3.29) and (3.30) do not apply. As a result, $T_1 = T_{1,g}$ and $T_2 = T_{2,g}$.

Figure 3.18 presents the flowchart that shows the processes involved according to the steps described above in order to determine the on-state times of the nearest voltage vectors.

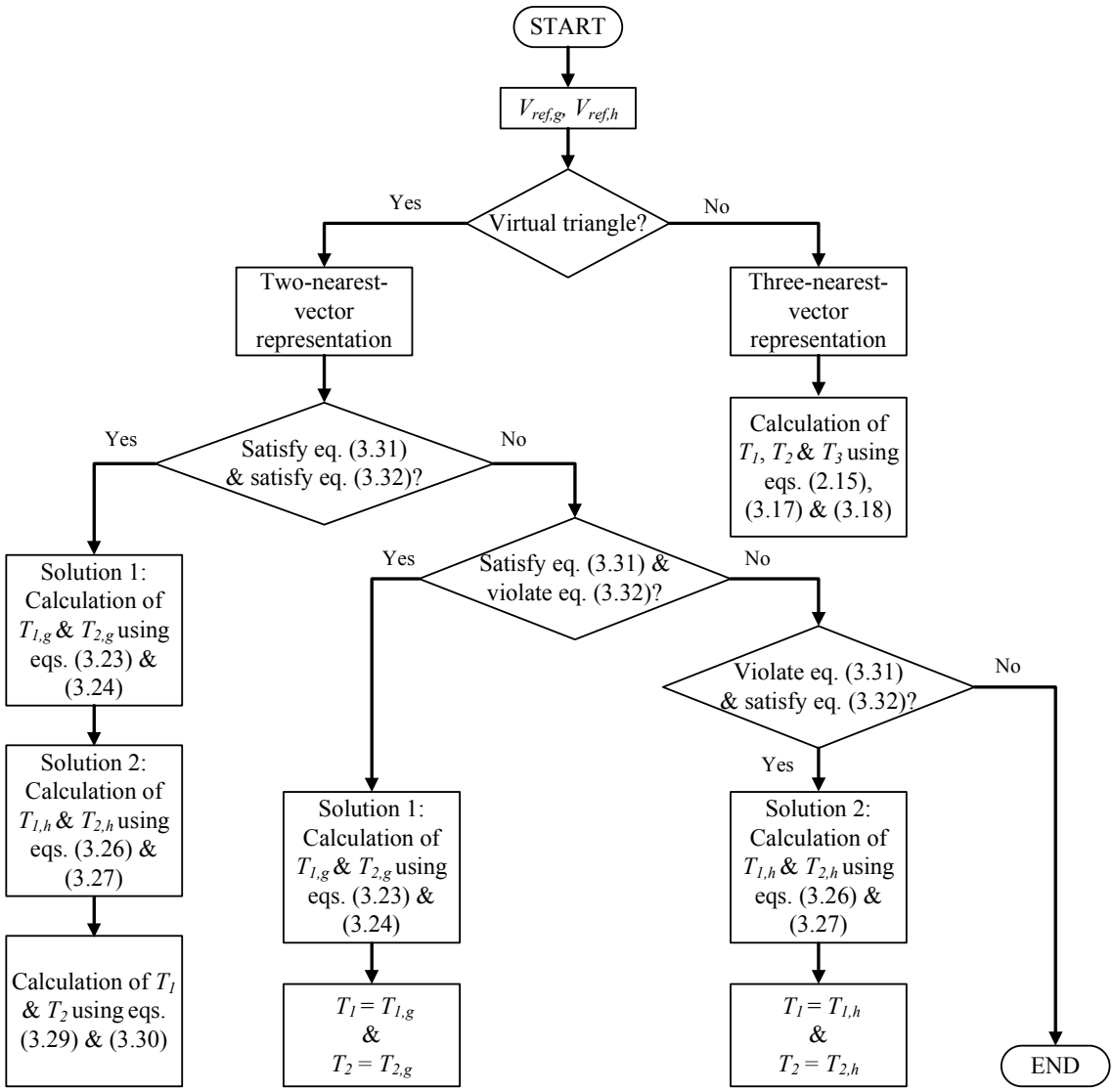
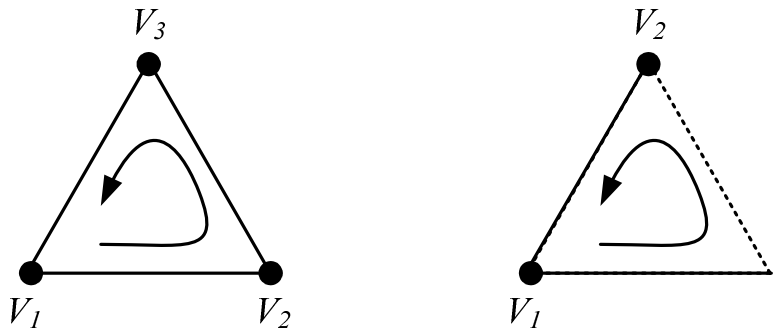


Figure 3.18: Flowchart to determine the on-state times of the nearest voltage vectors.

3.4.6 Switching State Sequence

In this work, symmetric switching state sequences are employed. For three nearest vectors, the sequence begins from V_1, followed by V_2 and then V_3 before returning to V_1 again during the first sampling time duration. To achieve symmetry, the sequence starts again from V_1 to V_3 and next, to V_2 before coming back to V_1 during the second sampling time interval. In short, the sequence can be generally written as V_1-V_2-V_3-V_1-V_1-V_3-V_2-V_1. The same applies for two nearest vectors in which the general sequence V_1-V_2-V_1-V_1-V_2-V_1 is used. Figure 3.19 illustrates the general sequences. Figures 3.20 and 3.21 show the sequences used for all triangular zones in the proposed four-level and five-level inverters respectively. A number is given to each triangular zone to simplify identification.



(a) V_1-V_2-V_3-V_1-V_1-V_3-V_2-V_1 (b) V_1-V_2-V_1-V_1-V_2-V_1

Figure 3.19: Generalized switching state sequences for three and two voltage vectors.

The use of *gh*-plane coordinate system ensures that each voltage vector has coordinates with integer values. For example, Triangular Zone 1 in Figures 3.20 and 3.21 has three voltage vectors of the following coordinates: V_1 (0,0), V_2 (V_{dc},0) and V_3 (0,V_{dc}). To further simplify calculation of the on-state times, normalized coordinates can be used by taking V_{dc} as the base value. Hence, the normalized coordinates for the vectors of Zone 1 are V_1 (0,0), V_2 (1,0) and V_3 (0,1). Referring to Figure 3.20, it can be seen that other zones with three vectors that use a similar sequence to that of Zone 1 are

Zones 5 and 9. The normalized coordinates of the vectors for Zone 5 are V_1 (2,0), V_2 (3,0) and V_3 (2,1) while those for Zone 9 are V_1 (0,2), V_2 (1,2) and V_3 (0,3). From these coordinates, a generalized formula can be derived. If the normalized coordinate of the first vector V_1 is given by ($V_{1,gn}$,$V_{1,hn}$), then the second and third vectors V_2 and V_3 can then be generalized as ($V_{1,gn}$ +1, $V_{1,hn}$) and ($V_{1,gn}$, $V_{1,hn}$ +1) respectively. In this way, by knowing the coordinate of the first vector V_1 only, it is sufficient to calculate the on-state times for a given reference vector and a given switching state sequence. For example, referring to Zones 1, 5 and 9 of Figure 3.20 again, by using the generalized coordinates of V_1, V_2 and V_3 above to solve for the on-state times T_1, T_2 and T_3 in equations (2.15), (3.17) and (3.18), the following are obtained:

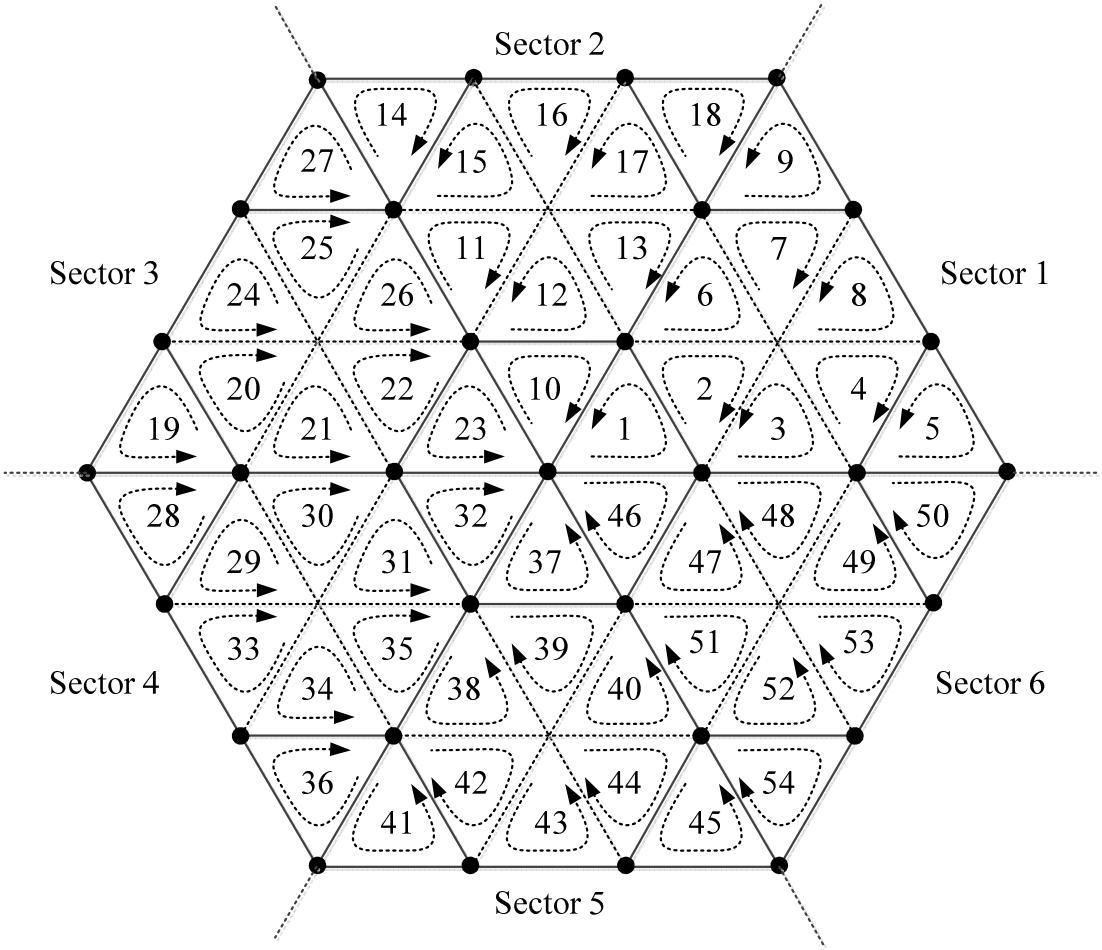


Figure 3.20: Switching state sequences adopted for the proposed four-level inverter.

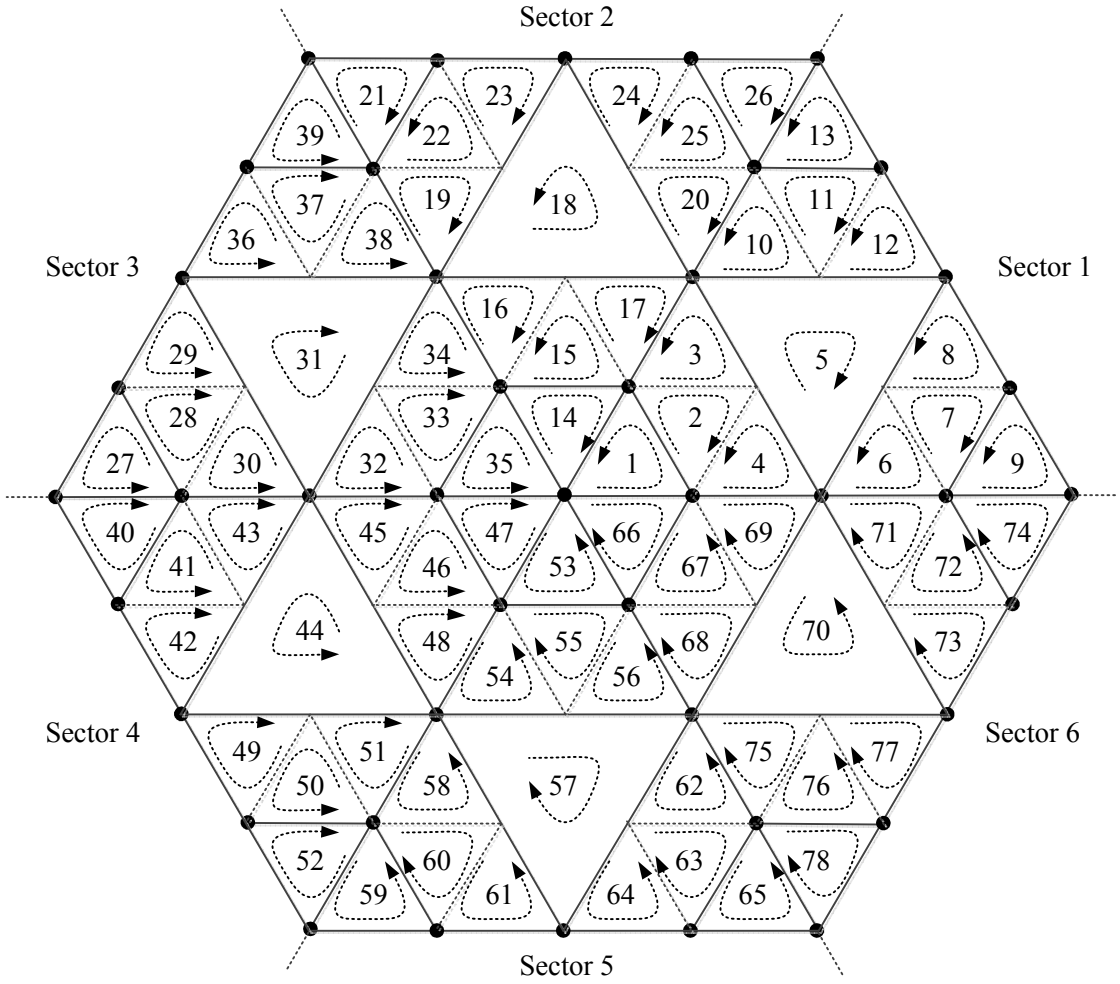


Figure 3.21: Switching state sequences adopted for the proposed five-level inverter.

$$T_1 = \left(V_{1,gn} + V_{1,hn} - V_{ref,gn} - V_{ref,hn} + 1\right)T_s \tag{3.33}$$

$$T_2 = \left(V_{ref,gn} - V_{1,gn}\right)T_s \tag{3.34}$$

$$T_3 = \left(V_{ref,hn} - V_{1,hn}\right)T_s \tag{3.35}$$

The generalization applies to all other zones as well. By having the generalized formulas for the normalized coordinates and the on-state times, computational burden can be reduced to achieve a simplified implementation of the algorithm.

3.5 Current Control Scheme

In this work, two current control schemes are employed namely VOC and DPC-SVM schemes. Both schemes utilize the PI controllers. Coordinate transformation is necessary to obtain the DC quantities of currents and the active and reactive powers. In VOC scheme, the PI controllers use current errors to generate the appropriate control signals for the modulator. In DPC-SVM scheme, the power errors are utilized as inputs to the PI controllers to produce commands for the modulator. To further improve the performance of the PI controllers, a tuning algorithm is developed. This section details the VOC and DPC-SVM schemes for the proposed inverter with the proposed PI controller.

3.5.1 VOC Scheme

The block diagram of the VOC scheme is shown in Figure 3.22. In this work, the proposed four-level inverter is used for illustration. In each phase, an inductance L_f which acts a filter is mounted between the inverter and the load. Assuming that the internal resistance of the inverter is so small that it can be neglected, the voltage equations in the *ABC* frame can then be written as follows:

$$\begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \end{bmatrix} = \begin{bmatrix} v_{AN} \\ v_{BN} \\ v_{CN} \end{bmatrix} - L_f \frac{d}{dt} \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} \tag{3.36}$$

where v_{aN}, v_{bN} and v_{cN} are the voltages across the load, i_A, i_B and i_C are the load currents and v_{AN}, v_{BN} and v_{CN} are the output voltages of the inverter. To obtain the voltage equations in the stationary $\alpha\beta$ frame, the following applies:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \end{bmatrix} \tag{3.37}$$

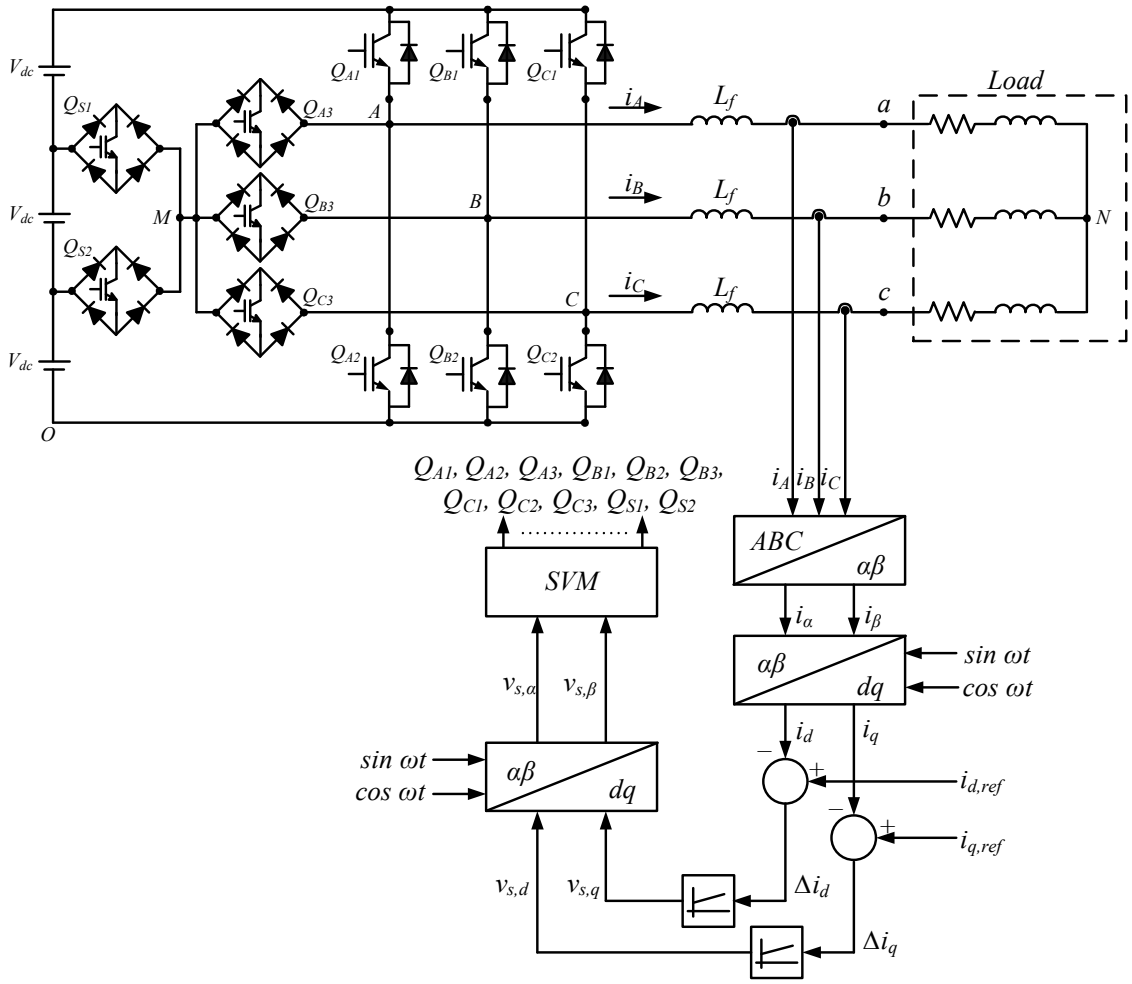


Figure 3.22: VOC scheme with the proposed four-level inverter.

Substituting equation (3.36) into equation (3.37), the result is given as the following:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{AN} - L_f \dfrac{di_A}{dt} \\ v_{BN} - L_f \dfrac{di_B}{dt} \\ v_{CN} - L_f \dfrac{di_C}{dt} \end{bmatrix} \tag{3.38}$$

Hence,

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} v_{s,\alpha} - L_f \dfrac{di_\alpha}{dt} \\ v_{s,\beta} - L_f \dfrac{di_\beta}{dt} \end{bmatrix} \tag{3.39}$$

Transformation from the stationary $\alpha\beta$ frame to the synchronous dq frame that is rotating with angular frequency ω is obtained using equation (3.40) below:

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{3.40}$$

Substituting equation (3.39) into equation (3.40), the following is obtained:

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} v_{s,\alpha} - L_f \dfrac{di_\alpha}{dt} \\ v_{s,\beta} - L_f \dfrac{di_\beta}{dt} \end{bmatrix} \tag{3.41}$$

Hence (Bong-Hwan, Jang-Hyoun, & Jee-Woo, 1999),

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} v_{s,d} \\ v_{s,q} \end{bmatrix} - \left(L_f \frac{d}{dt} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \omega L_f \begin{bmatrix} -i_q \\ i_d \end{bmatrix} \right) \tag{3.42}$$

For the load voltages whose expressions in the *ABC* frame are given in equation (3.43), the resulting expressions in $\alpha\beta$ and dq frames are therefore presented in equation (3.44) and (3.45) respectively.

$$\begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \end{bmatrix} = V_p \begin{bmatrix} \cos(\omega t) \\ \cos(\omega t - \frac{2}{3}\pi) \\ \cos(\omega t - \frac{4}{3}\pi) \end{bmatrix} \tag{3.43}$$

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{3}{2}} V_p \begin{bmatrix} \cos(\omega t) \\ \sin(\omega t) \end{bmatrix} \tag{3.44}$$

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{3}{2}} V_p \\ 0 \end{bmatrix} \tag{3.45}$$

Using equation (3.45), equation (3.42) becomes:

$$\begin{bmatrix} \sqrt{\frac{3}{2}} V_p \\ 0 \end{bmatrix} = \begin{bmatrix} v_{s,d} \\ v_{s,q} \end{bmatrix} - \left(L_f \frac{d}{dt} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \omega L_f \begin{bmatrix} -i_q \\ i_d \end{bmatrix} \right) \tag{3.46}$$

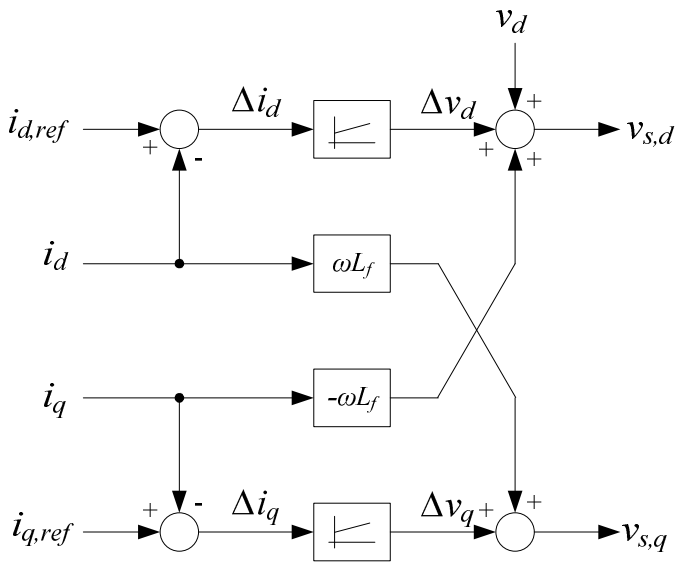


Figure 3.23: *dq* decoupling network.

From equation (3.46), it can be noticed that the control of i_d and i_q cannot be carried out completely independent due to the cross-coupling terms $\omega L_f i_q$ and $\omega L_f i_d$. As a result, the PI controllers used to control the currents cannot work well to provide satisfactory tracking performance. To overcome this problem, a decoupling network as shown in Figure 3.23 is used (Bong-Hwan, Jang-Hyoun, & Jee-Woo, 1999).

Hence,

$$v_{s,d} = v_d - \omega L_f i_q + \Delta v_d \tag{3.47}$$

$$v_{s,q} = \omega L_f i_d + \Delta v_q \tag{3.48}$$

where Δv_d and Δv_q are the output signals of the PI controllers which are defined as follows:

$$\Delta v_d = k_p \Delta i_d + k_i \int \Delta i_d dt \tag{3.49}$$

$$\Delta v_q = k_p \Delta i_q + k_i \int \Delta i_q dt \tag{3.50}$$

k_p and k_i are the proportional and integral gains of the PI controllers respectively.

Once $v_{s,d}$ and $v_{s,q}$ are obtained, a transformation to $\alpha\beta$ frame has to be performed using equation (3.51) below. The results are then used by the SVM modulator to generate the switching signals of the inverter.

$$\begin{bmatrix} v_{s,\alpha} \\ v_{s,\beta} \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) \\ \sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} v_{s,d} \\ v_{s,q} \end{bmatrix} \tag{3.51}$$

To achieve unity power factor in all conditions, the q-axis reference current $i_{q,ref}$ is then set to zero so that no q-axis current i_q can be produced.

3.5.2 DPC-SVM Scheme

The block diagram of the DPC-SVM scheme with the proposed four-level inverter is shown in Figure 3.24. An inductance L_f is used to limit the magnitude of the current ripple in each phase. The power estimation block calculates the instantaneous active and reactive powers using current and voltage values. There are two ways to estimate the instantaneous powers. The first approach is by using the *ABC* quantities, while the second method utilizes the $\alpha\beta$ quantities.

Instantaneous active power p has been defined as the scalar product between the three-phase voltages and currents while the instantaneous reactive power q is the vector product between them (Noguchi, Tomiki, Kondo, & Takahashi, 1998). By using the *ABC* quantities, the following equations are used to calculate p and q:

$$p = \bar{v}_{(ABC)} \cdot \bar{i}_{(ABC)} = v_{aN} i_A + v_{bN} i_B + v_{cN} i_C \tag{3.52}$$

$$q = \bar{v}_{(ABC)} \times \bar{i}_{(ABC)} = \frac{1}{\sqrt{3}} \left[(v_{bN} - v_{cN}) i_A + (v_{cN} - v_{aN}) i_B + (v_{aN} - v_{bN}) i_C \right] \tag{3.53}$$

The definitions of p and q have also been described using the $\alpha\beta$ quantities as given below (Akagi, Kanazawa, & Nabae, 1984; Kazmierkowski, Jasinski, & Wrona, 2011):

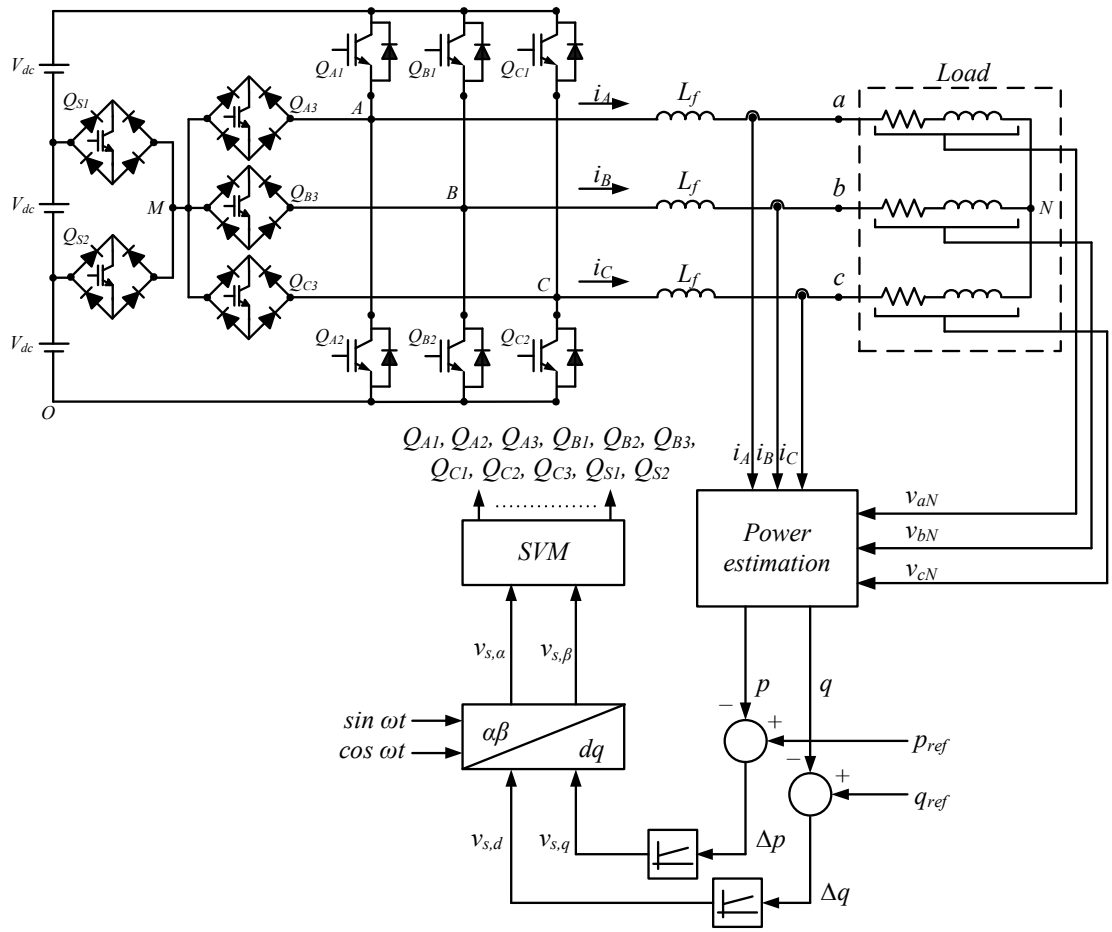


Figure 3.24: DPC scheme with the proposed four-level inverter.

$$p = v_\alpha i_\alpha + v_\beta i_\beta \tag{3.54}$$

$$q = v_\alpha i_\beta - v_\beta i_\alpha \tag{3.55}$$

In DPC-SVM scheme, two PI controllers are used to generate the control signals based on the power errors received. To achieve unity power factor operation condition, the reference reactive power q_{ref} is set to zero. To ensure that the two PI controllers work independently, a decoupling network as described in equations (3.47), (3.48), (3.49) and (3.50) is applied. Since the command voltage $v_{s,d}$ and $v_{s,q}$ are expressed in synchronous rotating frame, a transformation to $\alpha\beta$ frame has to be performed using equation (3.51). Based on the transformed command voltages $v_{s,\alpha}$ and $v_{s,\beta}$, the SVM block generates the appropriate signals for inverter control.

3.5.3 Digital PI Controllers

In both VOC and DPC-SVM schemes, the PI controllers are developed for use with digital circuitry which can be realized by using a microcontroller or a DSP. Digital control is preferred as this can avoid the use of analog components such as resistors and capacitors which are associated with component variation as a result of the components allowable tolerances. Besides, in digital control, realization of the controller is done in software, thus making the tuning process to be easily and accurately carried out.

To build a digital PI controller model, a conversion from the continuous-time domain to the discrete-time domain is necessary. Equation (3.56) presents the general equation for a PI controller in the continuous-time domain:

$$u(t) = k_{p,t}e(t) + k_{i,t}\int_{\tau=0}^{t} e(\tau)d\tau \tag{3.56}$$

with *u(t)* as the output of the controller, *e(t)* as the error signal, *t* as the time variable, $k_{p,t}$ as the proportional mode gain and $k_{i,t}$ as the integral mode gain. The conversion to the discrete-time domain can be done by using several techniques. One of the techniques is the trapezoidal sum approximation technique which results in the following equation in the discrete-time domain:

$$u(n) = k_{p,n}e(n) + k_{i,n}\sum_{i=0}^{n}\left[e(i) + e(i-1)\right] \tag{3.57}$$

with

$$k_{p,n} = k_{p,t} \tag{3.58}$$

$$k_{i,n} = k_{i,t}\frac{h}{2} \tag{3.59}$$

$$t = n * h \tag{3.60}$$

where *n* is the discrete-time index and *h* is the sampling period.

The second term in the right hand side of equation (3.57) denotes the full summation starting from the point when the controller begins to run until the present time when the calculation involving the current error takes place. To avoid high computational burden which continuously increases as time goes by in calculating the full summation at each time step, the abovementioned term is then treated as a continuous summation, instead of a full summation. Hence, equation (3.57) can be simplified as the following:

$$u(n) = k_{p,n}e(n) + k_{i,n}sum(n) \tag{3.61}$$

with

$$sum(n) = sum(n-1) + \left[\left(e(n) + e(n-1)\right)\right] \tag{3.62}$$

3.5.4 Anti-Windup Module

The performance of the PI controllers is very much influenced by the load parameters especially the *d*-component current controller in VOC scheme and the active power controller in the DPC-SVM scheme. At a certain load condition, the PI controller in each scheme can only receives its respective input within an allowable range, beyond which the input becomes constant as it reaches its saturation level. This is so since the controller's input is actually derived from the output of a closed-loop system whose values are restricted by the load parameters. Therefore, when the controller's input has reached saturation, this means that the system's output has arrived at its maximum or minimum restricted value. Although saturation has been reached, the integral part of the controller continues to increase or decrease which causes increases or decreases in the controller's output. At this stage, the change in the controller's output has no more effects on the system's output since the maximum or minimum restricted value has already been achieved. If the integral component of the controller keeps integrating, this causes the controller to experience integral windup effect. As a consequence, the

controller may take a long time to achieve the steady-state condition and system's instability can even occur.

To avoid the windup effect, the PI controller is equipped with two anti-windup modules. One module is to limit the output of the integrator and the other is to set proper bounds for the controller's output. With the addition of the anti-windup modules, then integral term $u_i(n)$ in equation (3.61) is governed by the following conditions:

$$u_i(n) = k_{i,n} sum(n) \text{ if } U_{i,low} < u_i(n) < U_{i,high} \tag{3.63}$$

$$u_i(n) = U_{i,low} \text{ if } u_i(n) < U_{i,low} \tag{3.64}$$

$$u_i(n) = U_{i,high} \text{ if } u_i(n) > U_{i,high} \tag{3.65}$$

As for the controller's output $u(n)$, the following conditions apply:

$$u(n) = k_{p,n} e(n) + k_{i,n} sum(n) \text{ if } U_{low} < u(n) < U_{high} \tag{3.66}$$

$$u(n) = U_{low} \text{ if } u(n) < U_{low} \tag{3.67}$$

$$u(n) = U_{high} \text{ if } u(n) > U_{high} \tag{3.68}$$

$U_{i,low}$ and $U_{i,high}$ are the minimum and maximum limits of the integral anti-windup module and U_{low} and U_{high} are the bottom and top bounds of the controller's output anti-windup module. Figure 3.25 shows the generalized structure of the conventional PI controller with anti-windup modules included. With suitable values of $U_{i,low}$, $U_{i,high}$, U_{low} and U_{high}, the controller's performance can be further improved since it is in a better position to run at its optimum operating point for a particular load condition.

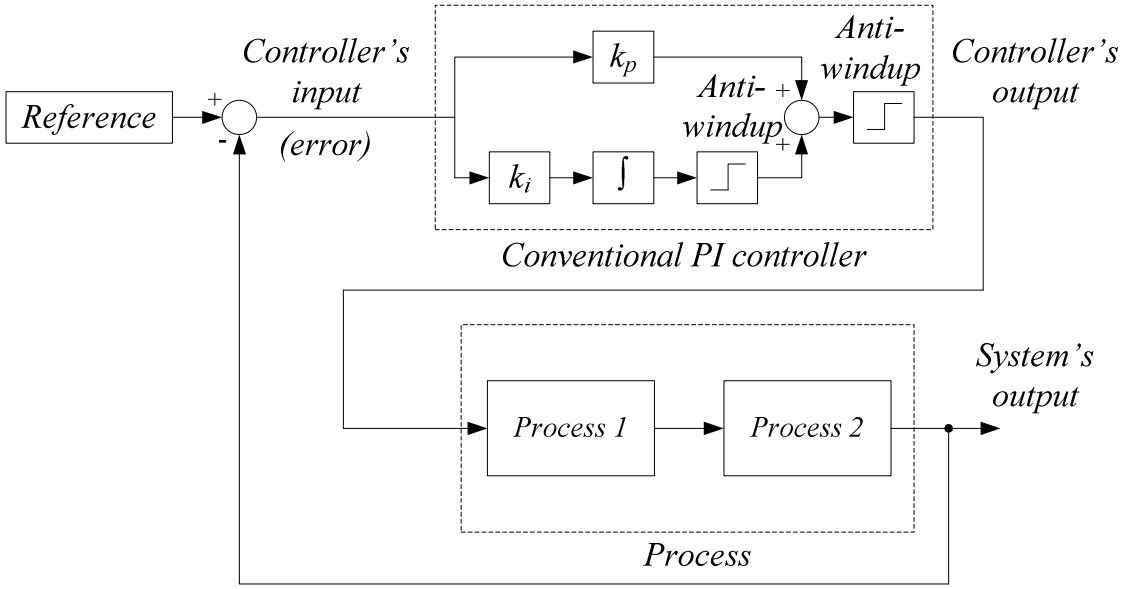


Figure 3.25: The generalized structure of the conventional PI controller with anti-windup modules.

3.5.5 Proposed Tuning Algorithm

It is commonly observed that the performance of the PI controller is somehow compromised when there is a change in the load condition. The degree of the performance drop depends on the amount of the load change. If the load change is small enough, the controller's good performance can still be maintained. However, when the amount of load change is significant, the controller may not be able to run at its optimum operating point anymore and as a result, its performance considerably deteriorates. Hence, parameter tuning is normally carried out to make the controller adaptive so that proper adjustment can be made by the controller to suit itself to different load conditions. To avoid the time-consuming manual tuning, automatic tuning has been introduced and in most cases, the tuning is concentrated more on the proportional and integral gain. In this work, a different perspective is viewed in which the anti-windup parameters are the ones focused for tuning.

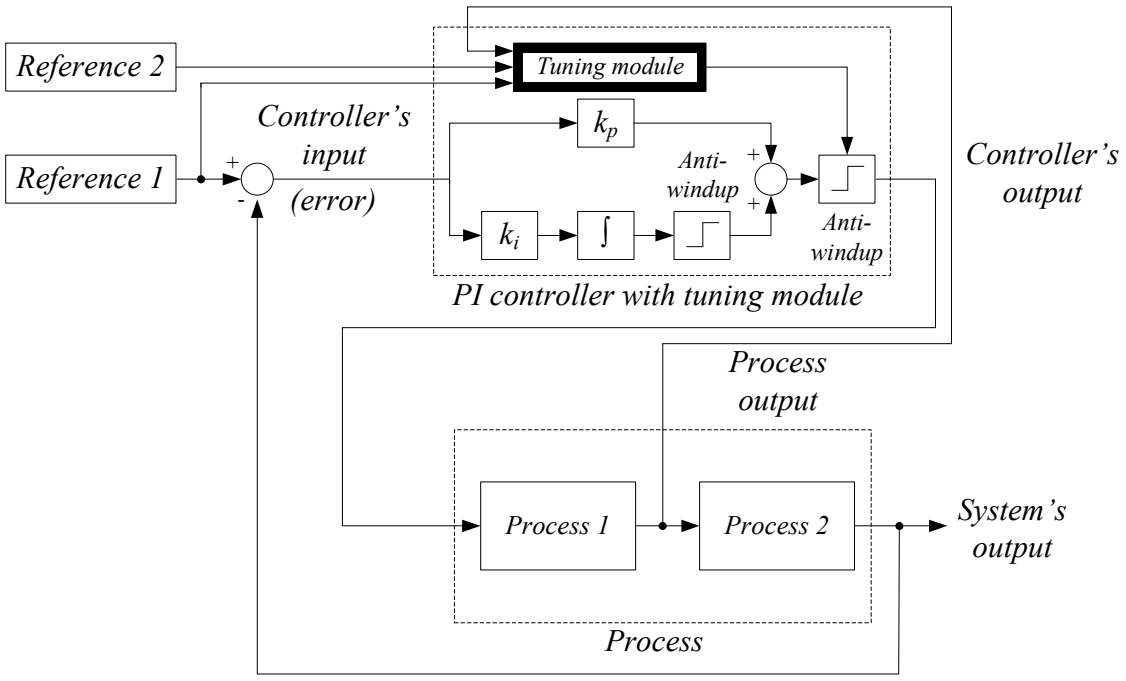


Figure 3.26: The generalized structure of the proposed PI controller with tuning module.

Figure 3.26 portrays the generalized structure of the proposed PI controller with the automatic tuning module. For the tuning module to work, it requires two reference signals and a feedback signal from the output of one of the processes involved in the system. To specifically design the controller for current control purpose, Figure 3.27 and 3.28 are given to illustrate the VOC and DPC-SVM schemes respectively. The two reference signals required are the reference *d*-component current $i_{d,ref}$ in VOC, or the reference active power p_{ref} in DPC-SVM, and the desired reference voltage vector amplitude, V_{aim}. The feedback signal is the actual reference voltage vector amplitude, V_{ref}. It should be noted that the tuning module is not included in the PI controller for the *q*-component current or the reactive power since the reference signal for the controller is always zero.

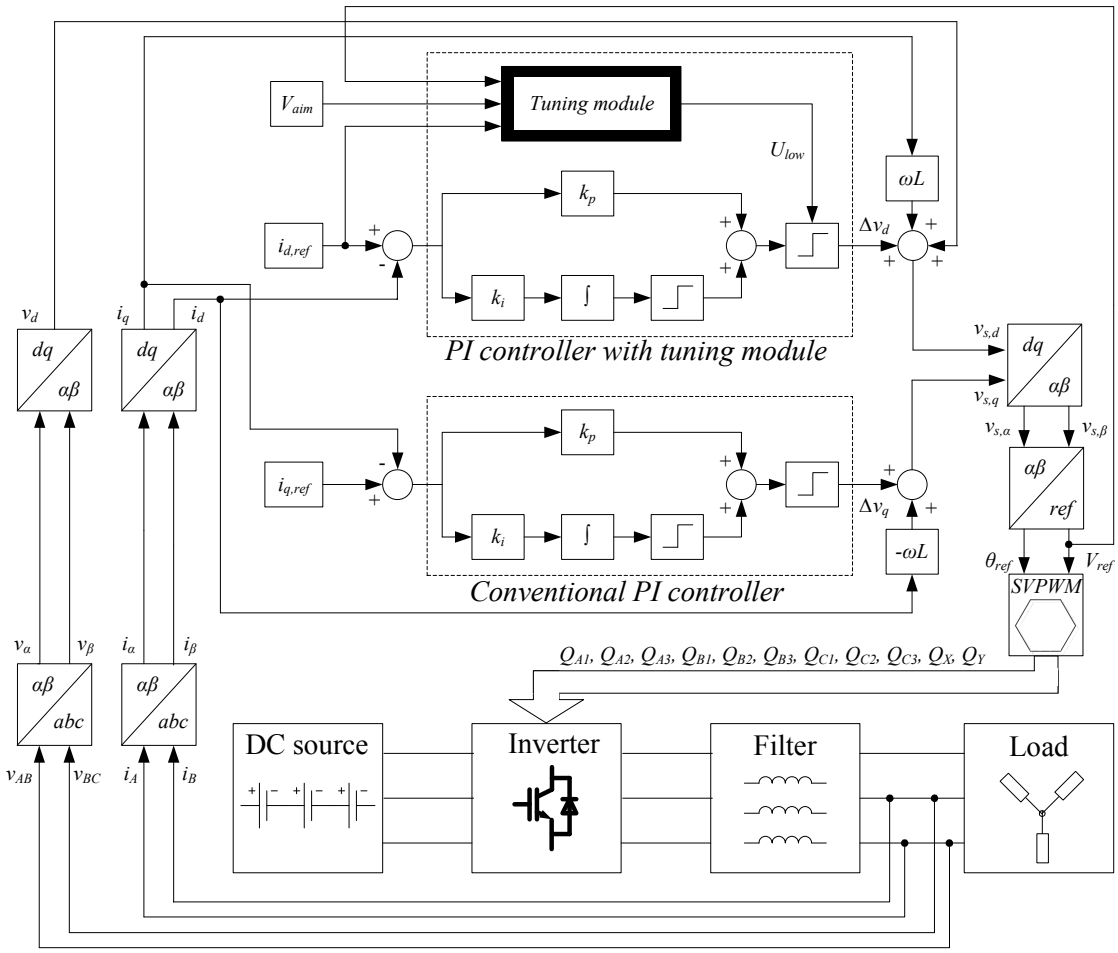


Figure 3.27: VOC scheme with the proposed PI controller with a tuning module.

The purpose of the tuning module is to maintain or even improve the quality of the output current after a change in the load condition. This is realized by applying an additional criterion for the controller to achieve namely V_{aim}. V_{aim} is chosen based on certain preferred characteristics such as low voltage THD or good voltage harmonic spectrum. The selection of V_{aim} can be done within a range between 0 and 100% in which 100% means the highest reference voltage vector amplitude allowed before overmodulation occurs. It is normally observed that a reference voltage vector of amplitude 70% and higher produces good THD and harmonic spectrum. Therefore, V_{aim} should be selected within this range and must stay constant for any load conditions. The tuning algorithm is then designed to direct the actual reference voltage vector V_{ref} to be

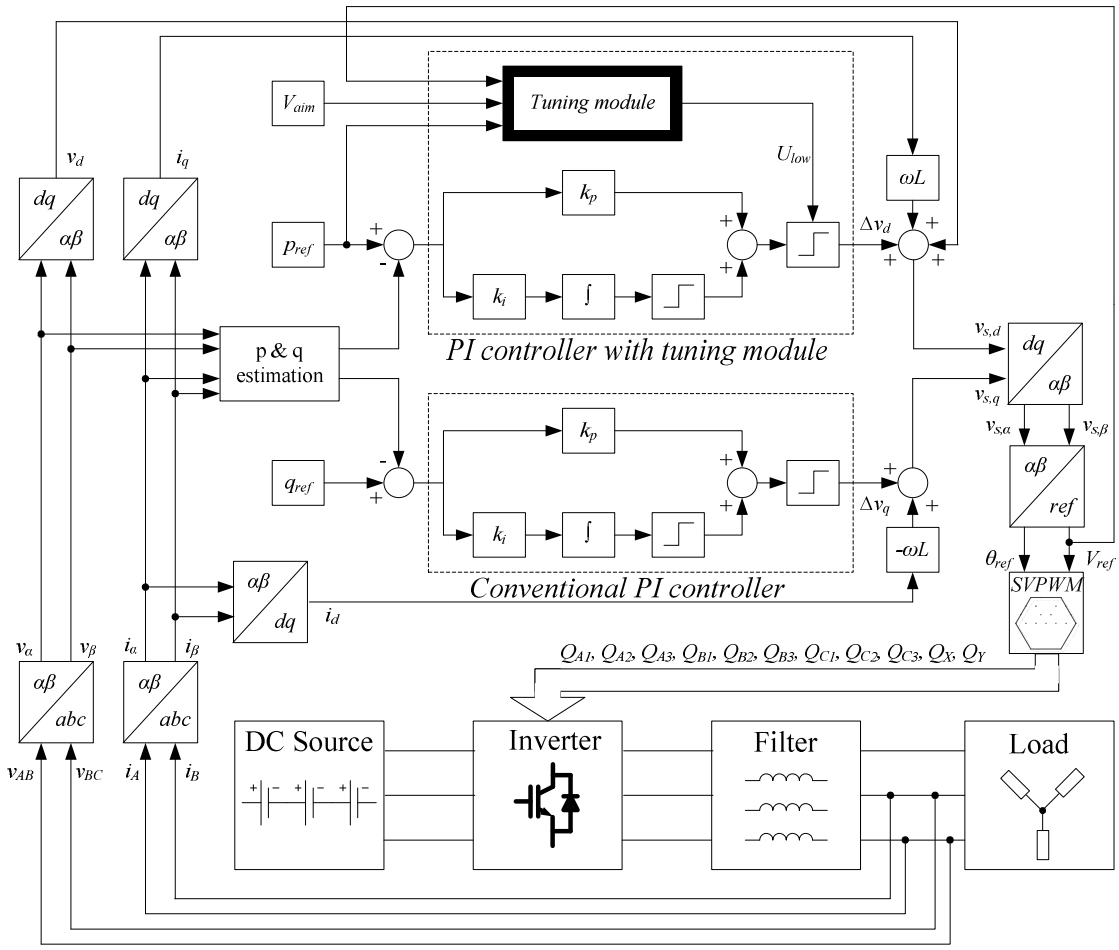


Figure 3.28: DPC-SVM scheme with the proposed PI controller with a tuning module.

as close as possible to V_{aim} by adjusting U_{low} only in the controller's output anti-windup module without modifying other controller's parameters including the proportional or integral gains. By doing so, the controller's ability to reduce the current error in VOC and the power error in DPC-SVM can be enhanced. This is true as the tuning module acts a fine-tuner for the controller to always operate at its optimum operating point in order to attain excellent tracking performance especially after a load change.

The process flow of the tuning mechanism for VOC scheme as displayed Figure 3.29 is explained as follows:

1. $i_{d,ref}$ is first checked whether its present value (stored in i_1) is similar to its most recent value recorded previously (stored in i_2).
2. If the present value is different from the previous value, then i_2 is updated to store the present value. New U_{low} ($U_{low,new}$) is calculated using the following equation:

$$U_{low,new} = Ae^{Bi_2} + Ce^{Di_2} \tag{3.69}$$

A, B, C and D are constants. They are pre-determined from preliminary tests carried out to establish the relationship between $i_{d,ref}$ and U_{low} for several bands of $i_{d,ref}$. The $i_{d,ref}$ bands represent the different load conditions. The data collected from the tests are analyzed using Matlab curve-fitting tool in order to create an exponential equation in the form shown in equation (3.69) that can approximately reflect the relationship between $i_{d,ref}$ and U_{low}. From this analysis, suitable values of A, B, C and D are obtained for a specific $i_{d,ref}$ band.

3. If the present value is the same as the previous value, then V_{ref} is determined whether it is within the allowable V_{aim} band. V_{aim} band is defined by the following limits with F is a fixed value:

Maximum limit: $V_{aim} + F$:

Minimum limit: $V_{aim} - F$:

4. If V_{ref} is higher than the maximum limit of the V_{aim} band, then $U_{low.new}$ is calculated by reducing the previous U_{low} ($U_{low,old}$) by a fixed value G as follows:

$$U_{low,new} = U_{low,old} - G \tag{3.70}$$

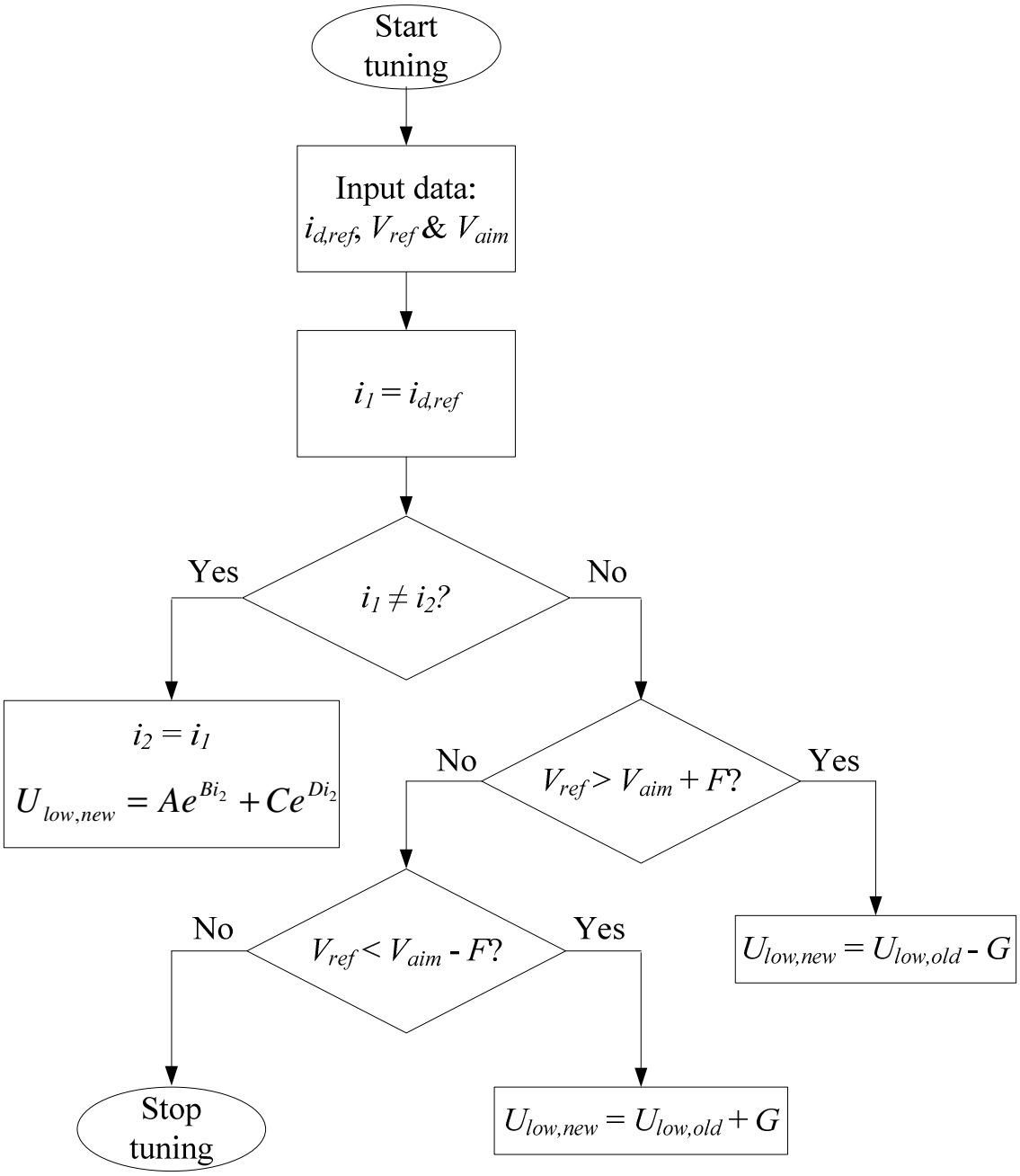


Figure 3.29: Process flow for automatic tuning in VOC scheme.

5. If V_{ref} is lower than the minimum limit of the V_{aim} band, then $U_{low,new}$ is calculated by increasing the $U_{low.old}$ by a fixed value G as follows:

$$U_{low,new} = U_{low,old} + G \tag{3.71}$$

6. Steps 1 to 5 are repeated in the following iterations until V_{ref} lies within the V_{aim} band.

The same procedure is carried out for DPC-SVM scheme as well. The only difference is the use of p_{ref} instead of $i_{d,ref}$.

3.6 Summary

In this chapter, a new multilevel inverter topology has been discussed. With the motivation to reduce the number of components used in the diode-clamped multilevel inverter, the proposed topology is derived from the transistor-clamped configuration with a switching-sharing strategy. The design and operating principle of the four-level and five-level structure of the proposed topology have been described. A novel SVPWM technique based on the application of virtual vectors have also been explained in detail. VOC and DPC-SVM current control schemes have been employed with the proposed topology. To ensure that the output current is maintained at a good quality after a change in the load condition, a new automatic tuning algorithm is proposed to adjust the bottom limit of the anti-windup module for the PI controller's output.

CHAPTER 4

SIMULATION RESULTS AND ANALYSIS

4.1 Introduction

Verification of the theoretical analysis of the proposed multilevel inverter topology can be done in two ways: testing on the simulated systems and testing on the real systems. This chapter is devoted to the former. This testing phase is critical as it provides a convenient platform to test unproven control algorithms without causing too many risks in terms of the costs spent and the losses brought to the system in case of algorithm failure. Furthermore, various parameters can be simply adjusted and optimized, hence speeding up the simulation process towards achieving the desired results.

In this chapter, MATLAB/SIMULINK software is used to conduct simulation work. Simulation model of the proposed multilevel inverter topology is built for the cases of four-level and five-level structures. Simulation is done according to the following system environment: open loop and closed loop. Closed-loop system has a feedback path while the open-loop system has none. In the open-loop system, the focus of simulation is to verify that the proposed multilevel inverter works as expected with the modulation methods employed. First, simulation is performed for operation at low switching frequency. The next stage is to run simulations of the constructed model at high switching frequency with the proposed SVPWM technique. For this high switching frequency operation, power loss analysis based on simulation is also conducted. To have a meaningful evaluation of the inverter's performance, comparisons are performed with the diode-clamped multilevel inverter.

For the closed-loop system, the objective of the simulation is to prove that the current controllers employed function as desired to produce good responses to changes in the load conditions. Special attention is given to the quality of the output current after the load changes. Two current control schemes are simulated for this purpose, namely the VOC and DPC-SVM schemes with the proposed multilevel inverter and the suggested SVPWM technique. The performance of the PI current controllers with and without the automatic tuning algorithm is also analyzed and compared in detail.

4.2 Simulation for Low Switching Frequency Modulation

To prove that the proposed multilevel inverter does operate according to the operating principles as described in Section 3.3, simulation is conducted for low switching frequency modulation. This section provides the related simulation details and results for the case of four-level and five-level configurations of the proposed topology.

4.2.1 Four-Level Inverter

Figure 4.1 shows the circuit configuration of the proposed four-level inverter developed with MATLAB/SIMULINK platform. Three DC sources of 50 V each are used. The AC load consists of three resistors of 30.5 Ω each. The switching pulses of the power switches are generated using “pulse generator” blocks. Some of the signals obtained from the blocks are manipulated by adding or subtracting them together with a constant. Hence, “add” and “constant” blocks are used for this purpose. Figure 4.2 portrays the schematic diagram for pulse generation.

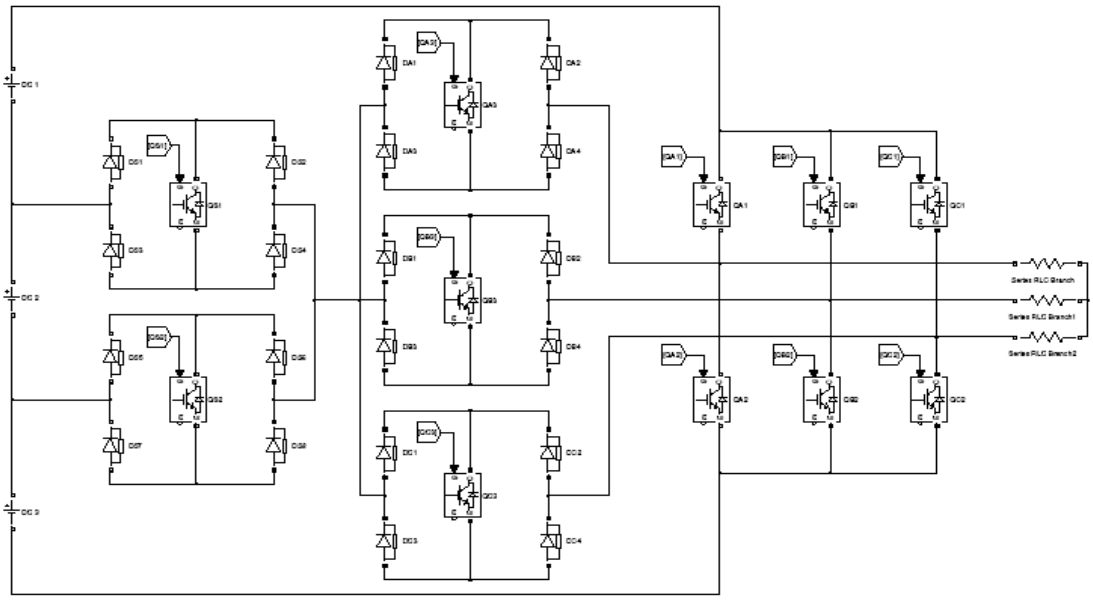


Figure 4.1: Circuit configuration of the proposed four-level inverter developed with MATLAB/SIMULINK.

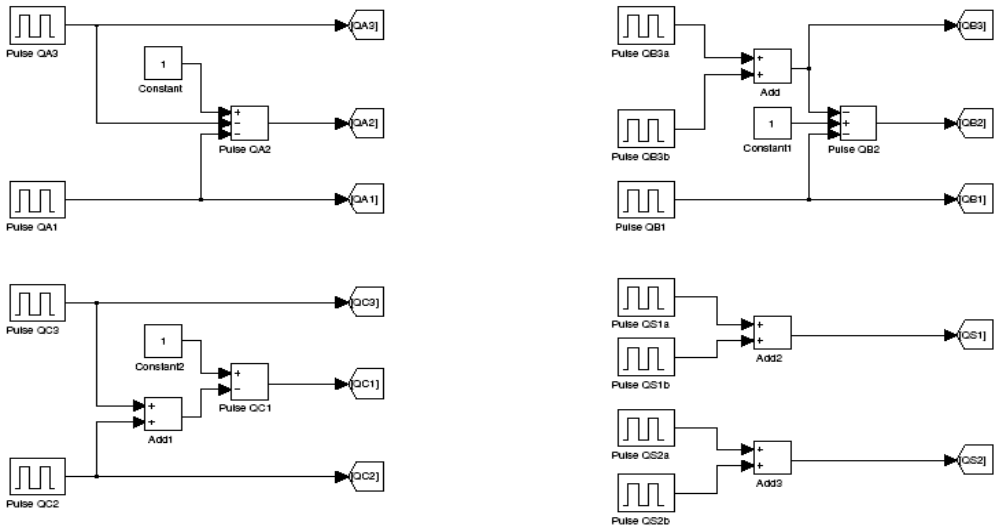
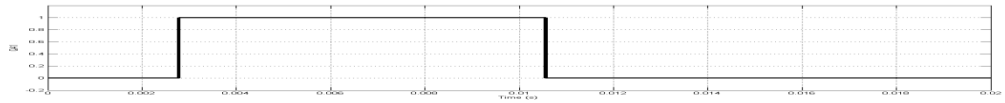


Figure 4.2: Pulse generation for the proposed four-level inverter.

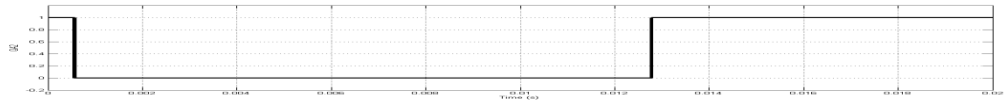
The switching pulses of all power switches are given in Figure 4.3. The resulting line-to-line and phase output voltage waveforms are displayed in Figures 4.4 and 4.5 respectively. It can be confirmed that the line-to-line output voltage waveforms comprises seven voltage steps. This is comparable to the one shown in Figure 3.4. For the phase voltage waveforms, ten voltage steps are produced. It should be noticed that simulation is carried out with equal time interval for each mode of operation. With reference to Figure 3.4, the switching angles are then given as follows: α_1 = 10°, α_2 = 30°, α_3 = 50°. In this thesis, optimum switching angles are not determined as this is beyond the scope of the work conducted.

4.2.2 Five-Level Inverter

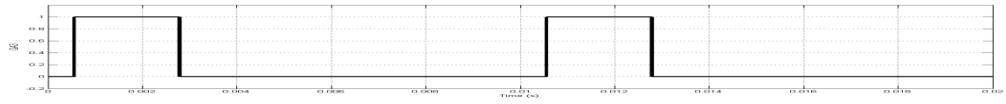
Simulation details for the proposed five-level inverter is similar to those of the four-level inverter as described earlier. The schematic circuit as shown in Figure 4.1 is altered to include one additional 50-V DC source and one extra bidirectional switch in Module 3 of the proposed topology to obtain an arrangement as depicted in Figure 3.5. An additional "pulse generator" block is used to generate the switching pulse for the extra bidirectional switch. Figures 4.6, 4.7 and 4.8 present the switching pulses, the line-to-line voltages and the phase voltages obtained from simulation. Nine and thirteen voltage steps are observed in the line-to-line and phase voltage waveforms respectively. In this simulation, each mode of operation is allocated with equal time interval. Therefore, the switching angles as defined in Figure 3.7 are set as the following: α_1 = 7.5°, α_2 = 22.5°, α_3 = 37.5°, α_4 = 52.5°. As mentioned earlier, optimum switching angles determination is not included in this work.



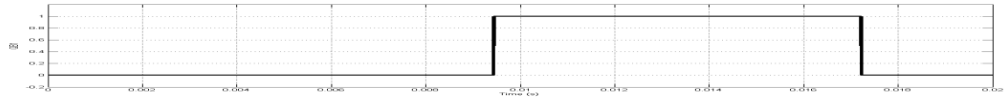
(a) Q_{A1}



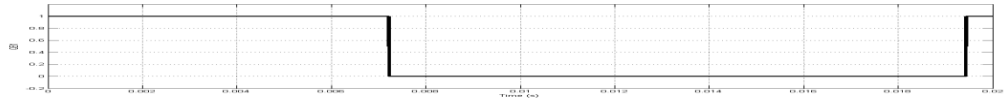
(b) Q_{A2}



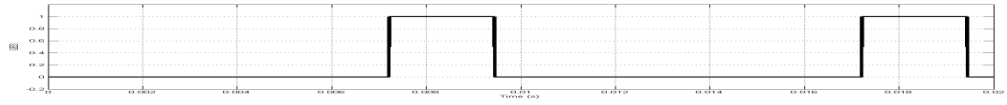
(c) Q_{A3}



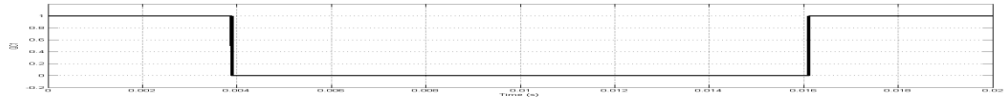
(d) Q_{B1}



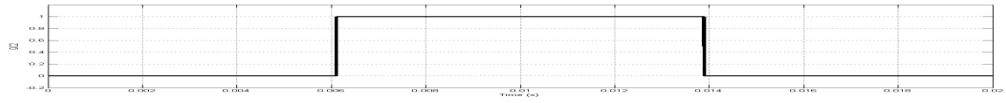
(e) Q_{B2}



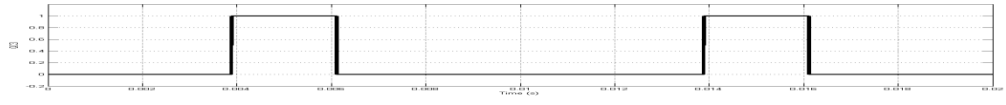
(e) Q_{B3}



(f) Q_{C1}

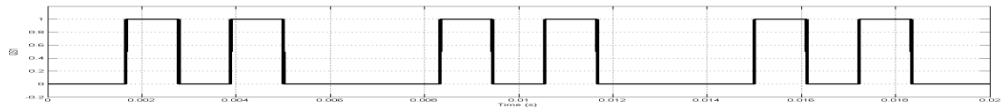


(g) Q_{C2}

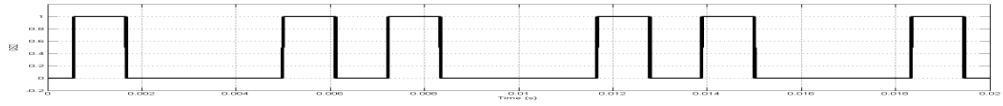


(h) Q_{C3}

Figure 4.3: Switching pulses for the proposed four-level inverter.

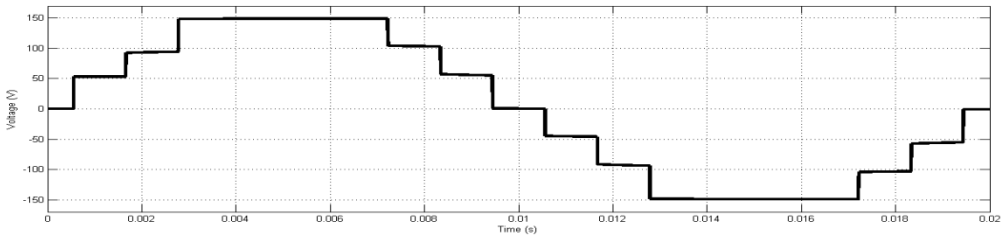


(i) Q_{S1}

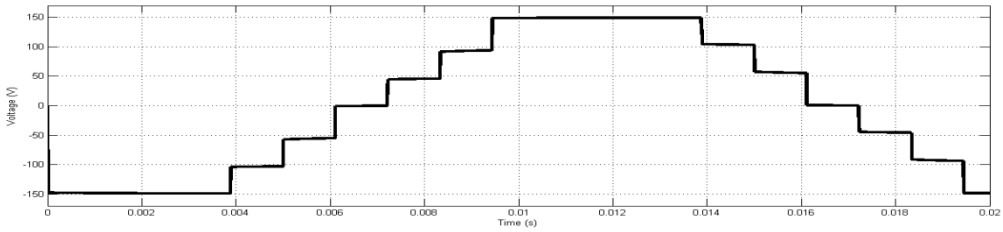


(j) Q_{S2}

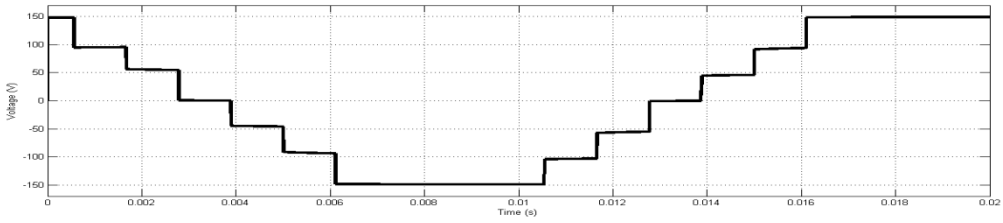
Figure 4.3, continued: Switching pulses for the proposed four-level inverter.



(a) V_{AB}

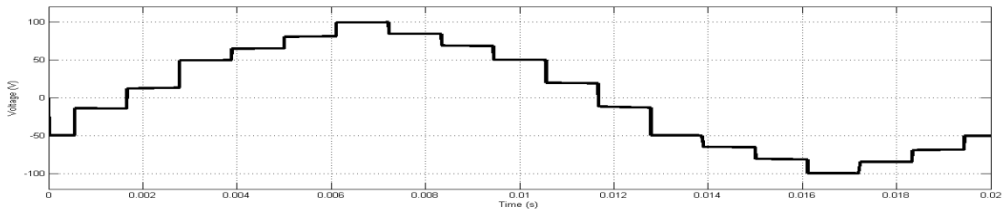


(b) V_{BC}

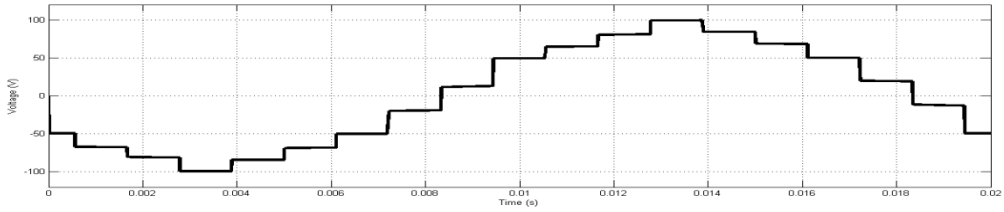


(c) V_{CA}

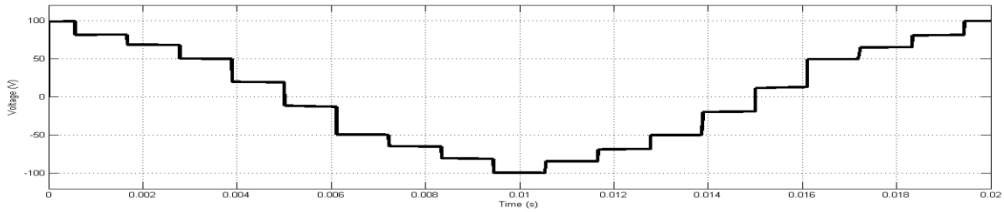
Figure 4.4: Line-to-line voltage waveforms of the proposed four-level inverter.



(a) V_{AN}

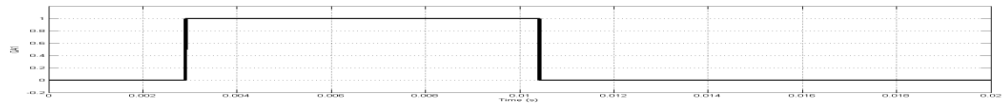


(b) V_{BN}

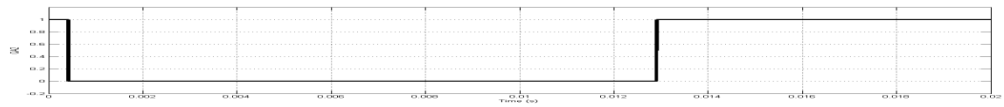


(c) V_{CN}

Figure 4.5: Phase voltage waveforms of the proposed four-level inverter.

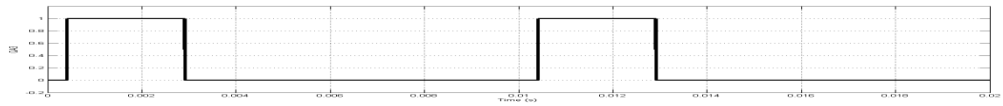


(a) Q_{A1}

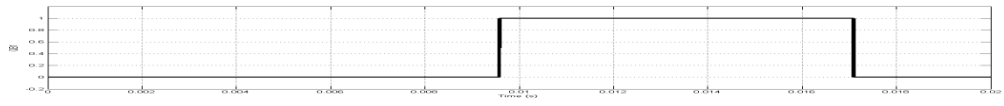


(b) Q_{A2}

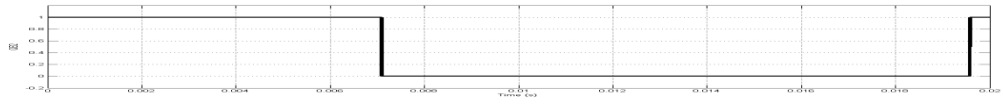
Figure 4.6: Switching pulses for the proposed five-level inverter.



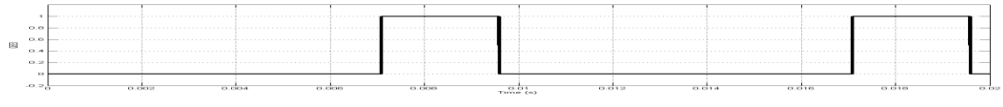
(c) Q_{A3}



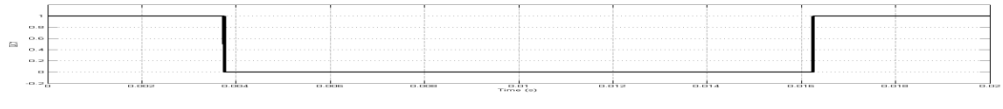
(d) Q_{B1}



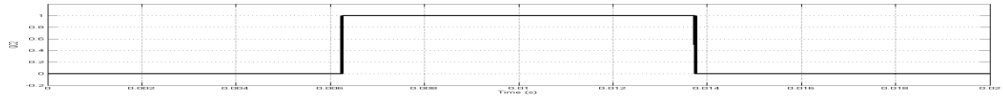
(e) Q_{B2}



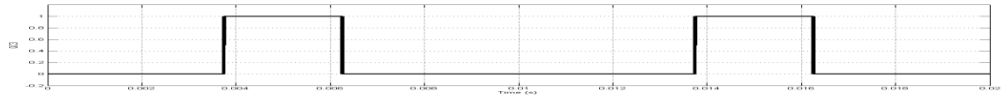
(f) Q_{B3}



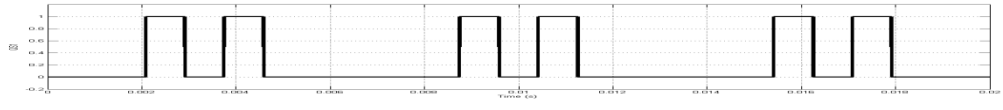
(g) Q_{C1}



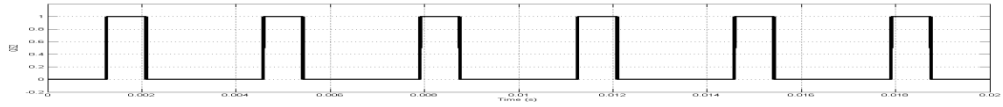
(h) Q_{C2}



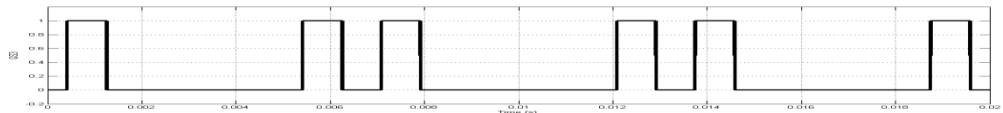
(i) Q_{C3}



(j) Q_{S1}

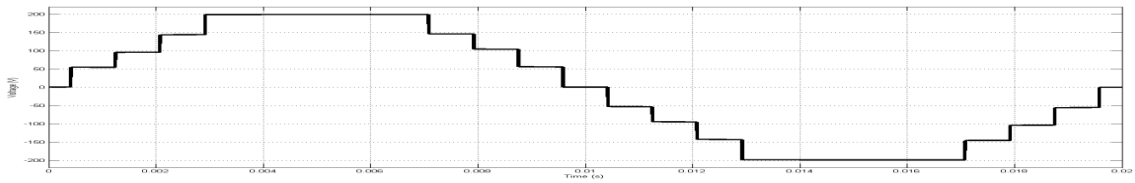


(k) Q_{S2}

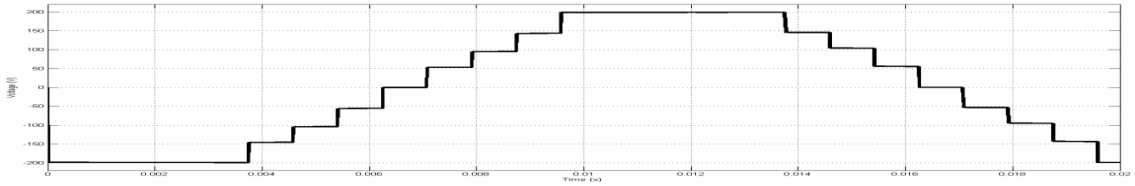


(l) Q_{S3}

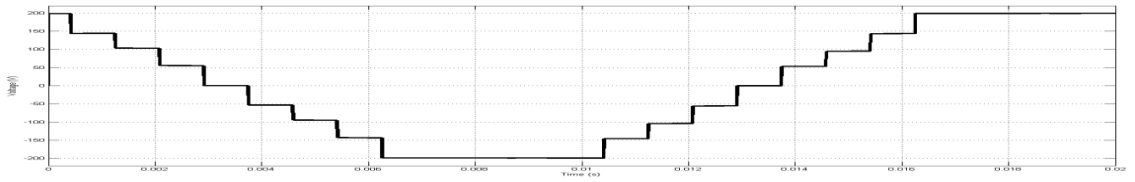
Figure 4.6, continued: Switching pulses for the proposed five-level inverter.



(a) V_{AB}

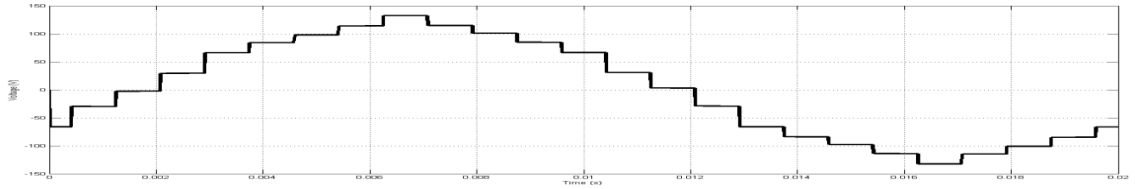


(b) V_{BC}

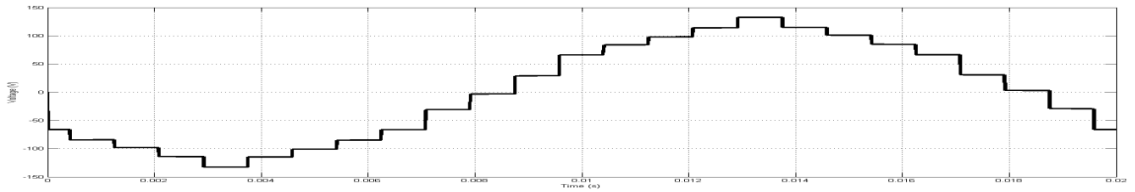


(c) V_{CA}

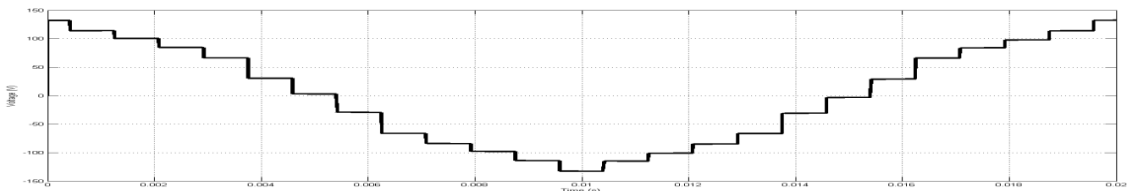
Figure 4.7: Line-to-line voltage waveforms of the proposed five-level inverter.



(a) V_{AN}



(b) V_{BN}



(c) V_{CN}

Figure 4.8: Phase voltage waveforms of the proposed five-level inverter.

4.3 Simulation for the Novel SVPWM

To investigate the effectiveness of the novel SVPWM method, simulation is carried out for four-level and five-level structures of the proposed topology. In this simulation study, the amplitude of the reference voltage vector is set to vary between 0% and 100%. 100% amplitude is defined as the radius of largest circle that can be formed within the vector hexagon. The impact of the amplitude variation on the voltage and current waveforms and harmonic spectra are analyzed.

4.3.1 Four-Level Inverter

The circuit configuration as shown in Figure 4.1 is used for simulation using MATLAB/SIMULINK. Three input DC sources are set to generate 150 V and a three-phase Y-connected load of 30.5 Ω and 68 mH per phase is used. The novel SVPWM is employed with a sampling frequency of 4.6 kHz to generate the PWM switching signals. 4.6 kHz is chosen so as to follow the sampling frequency used for practical implementation. Further explanation about the sampling frequency can be found under Section 5.5.1. By having similar sampling frequency between simulation and experiment, proper comparison can be made. To run the SVPWM in MATLAB/SIMULINK environment, “embedded MATLAB function” block is utilized. By using this block, a MATLAB program code is prepared. Figure 4.9 shows how the block uses the inputs obtained from two “repeating sequence stair” blocks to generate the PWM signals. The “repeating sequence stair” blocks act as the time counters. One of the blocks counts every sampling period up to 0.02 s (for fundamental frequency of 50 Hz) before the counter returns to zero and repeats counting again. The sampling period is further divided into ten subintervals. The other block uses the subinterval to count from zero up to the sampling period and this is continuously repeated.

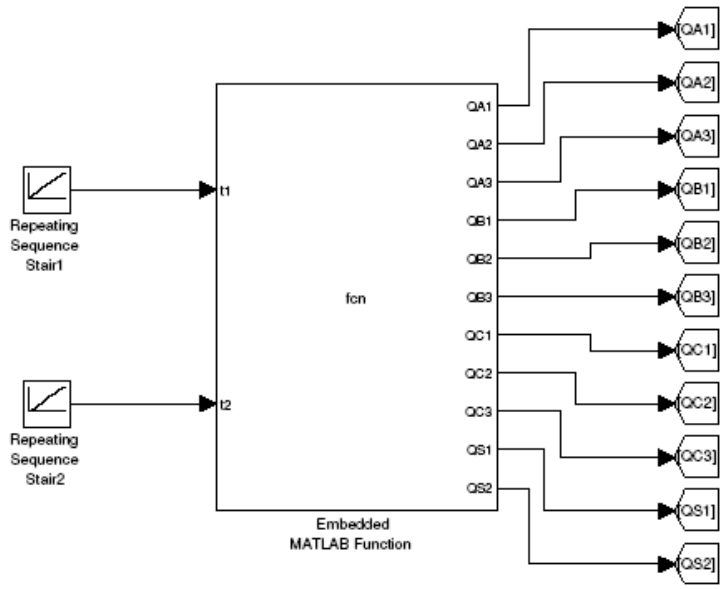


Figure 4.9: PWM signal generation for the proposed four-level inverter.

To describe how the program functions, a flowchart is provided in Figure 4.10. The input t_1 is used to initiate the calculation of the phase angle φ using the following equation:

$$\varphi = 2\pi f t_1 \tag{4.1}$$

f is the fundamental frequency which equals 50 Hz. The time increment in t_1 equals the sampling period. The phase voltages are next determined as follows:

$$V_{AN} = V_p \sin(\varphi) \tag{4.2}$$

$$V_{BN} = V_p \sin\left(\varphi - \frac{2}{3}\pi\right) \tag{4.3}$$

$$V_{CN} = V_p \sin\left(\varphi - \frac{4}{3}\pi\right) \tag{4.4}$$

V_p is the peak voltage that can be varied to obtain the desired reference voltage vector. Transformation to $\alpha\beta$ frame and then to gh frame take place using equations (3.12) to (3.16). The next stage involves identification of the sector and zone in which the

reference voltage vector lies. The nearest vectors are determined and the on-state times are accordingly computed as explained in Section 3.4.5.

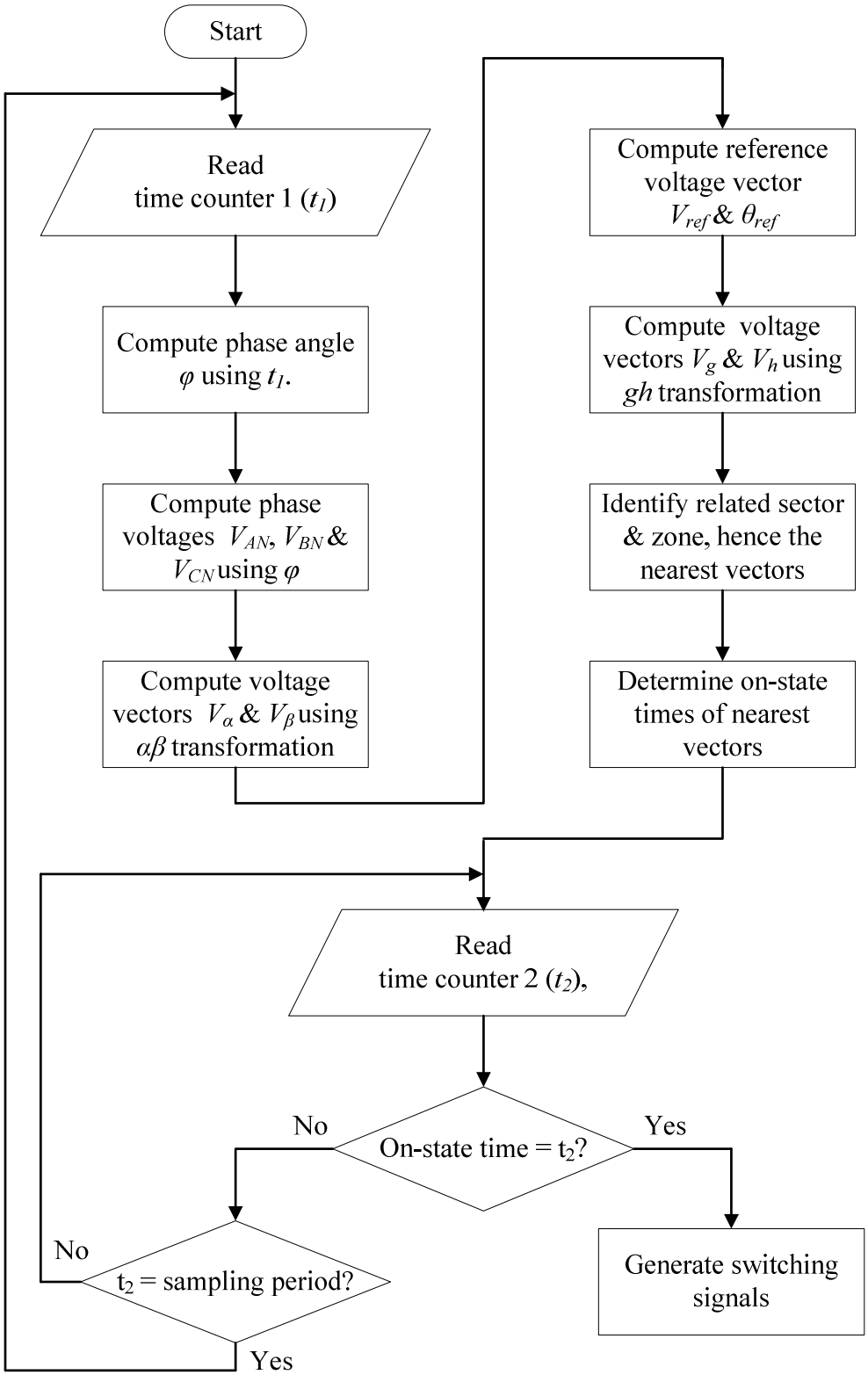


Figure 4.10: Flowchart of the MATLAB program code.

To generate the PWM signals, input t_2 is used to compare with the computed on-state times. The time increment t_2 equals the subinterval stated earlier. Switching signals are generated when t_2 and the on-state times are the same. If otherwise, the next value of t_2 is then waited and once it is received, the comparison process takes place again until t_2 equals the sampling period. A new iteration begins once the switching signal generation loop is exited.

Figure 4.11 presents the simulation result that shows the impact of varying the reference voltage vector amplitude on the number of voltage steps produced in the line-to-line output voltage waveforms. As the reference voltage amplitude increases, the number of voltage steps also increases from three to five and finally to seven. Figure 4.12 shows the representations of line-to-line output voltage waveforms with three, five and seven voltage steps that are obtained at 20%, 50% and 80% reference voltage amplitudes respectively. It can be seen from Figure 4.13 that the voltage THD reduces from 83.16% at 20% amplitude to 37.41% at 50% amplitude. Further reduction is achieved at 80% amplitude with 18.93% THD.

Despite the reduction seen in the THD, the harmonic spectra present different scenes. It can be observed that from the three harmonic spectra as shown in Figure 4.13, the one at 50% amplitude shows higher magnitudes for most harmonics while that at 80% amplitude records the lowest magnitudes for all harmonics. As an illustration, consider the fifth harmonic which happens to be the most significant one. Its magnitude jumps from 4.11% at 20% amplitude to 22.36% at 50% amplitude before reduces to 1.67% at 80% amplitude. The reason for this phenomenon is due to the elimination of the six voltage vectors of magnitude $\sqrt{3}V_{dc}$ that significantly contributes to the magnitude increase in the low order harmonics particularly at reference voltage

amplitudes around 50% mark. This effect can also be seen in the THD profiles of the line-to-line voltage as shown in Figures 4.14. THD slightly increases at 50% amplitude (37.41% THD) as compared to that of the 40% amplitude (37% THD) before it starts to drop. Nevertheless, this phenomenon does not influence the output voltage magnitude. As can be observed from Figure 4.15, the rms line-to-line fundamental voltage shows an upward trend as the reference voltage amplitude increases.

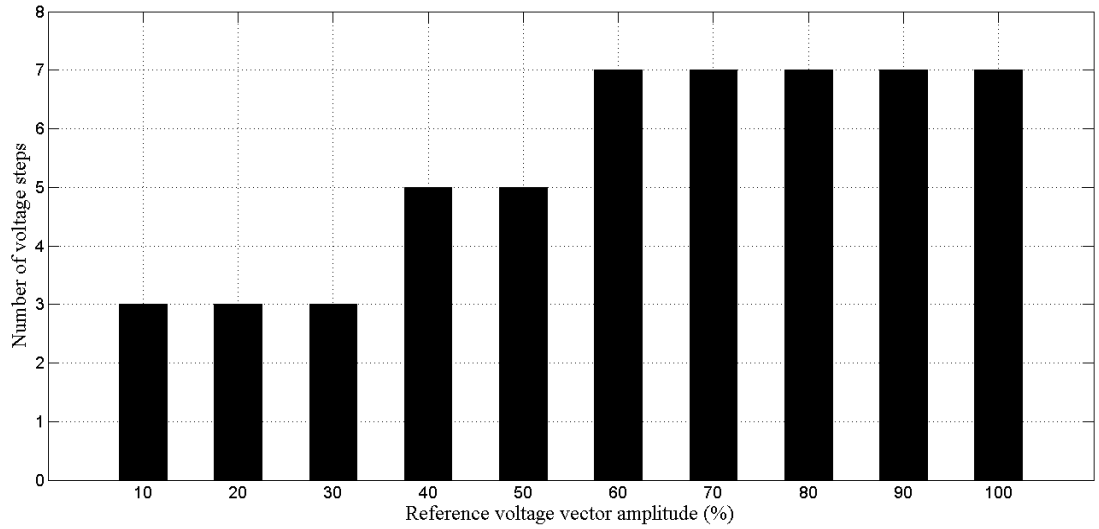
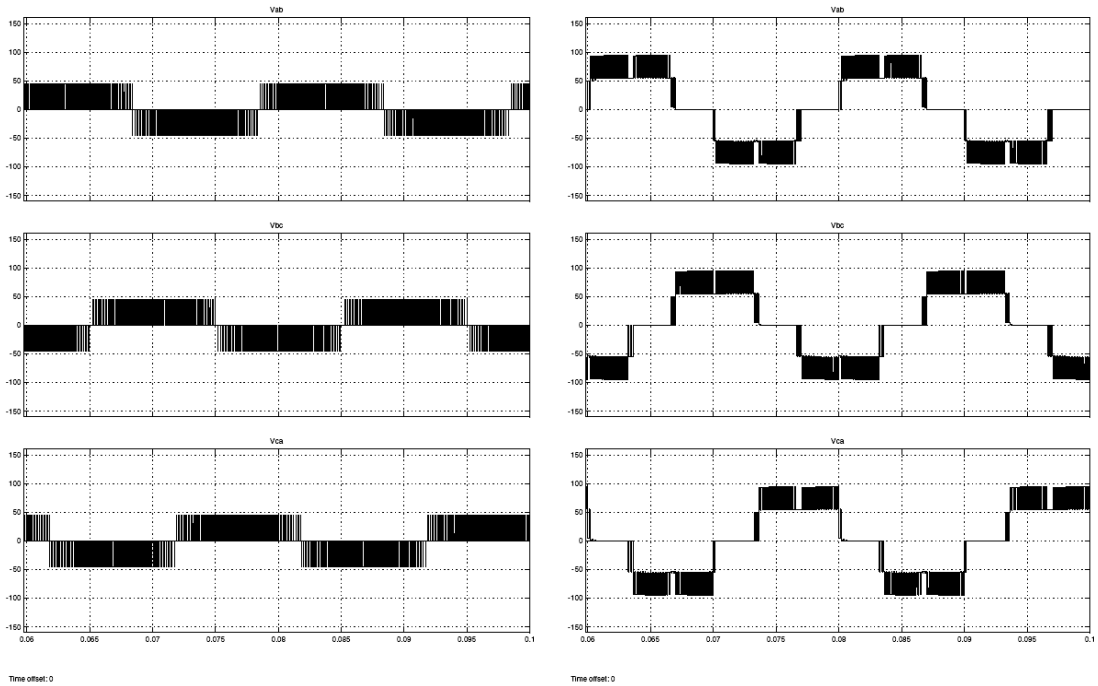
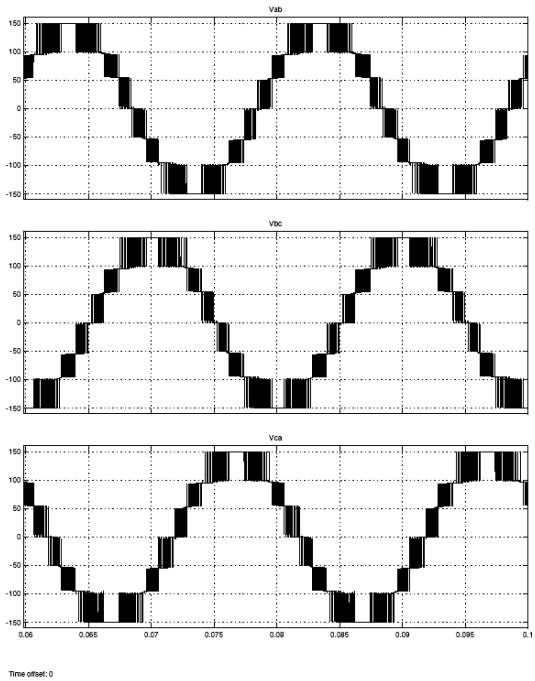


Figure 4.11: Number of voltage steps in the line-to-line output voltage waveforms of the proposed four-level inverter as the reference voltage amplitude varies.



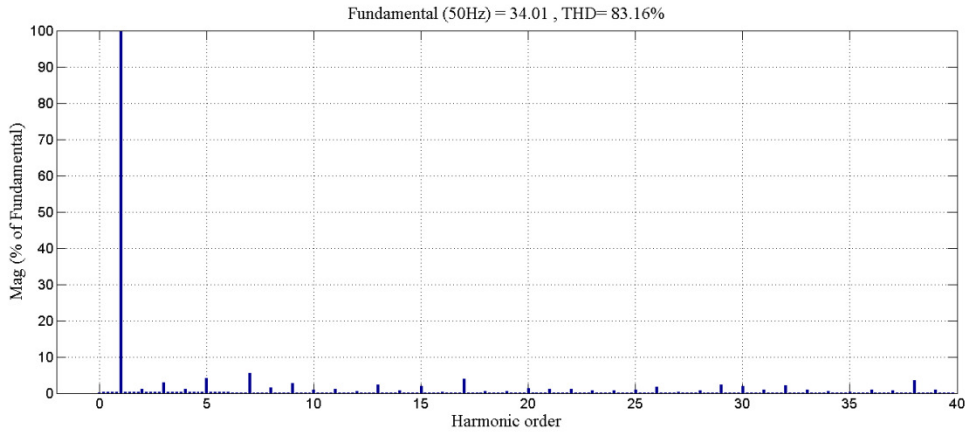
(a) 20% reference voltage amplitude

(b) 50% reference voltage amplitude

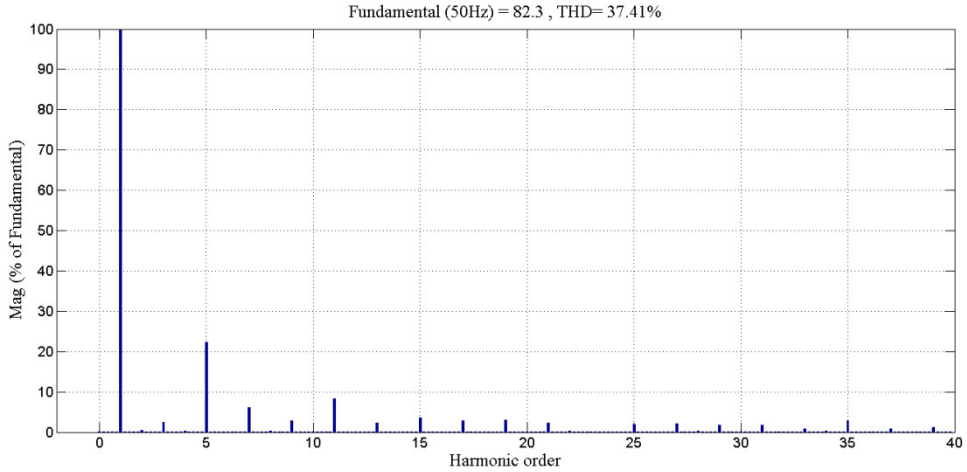


(c) 80% reference voltage amplitude

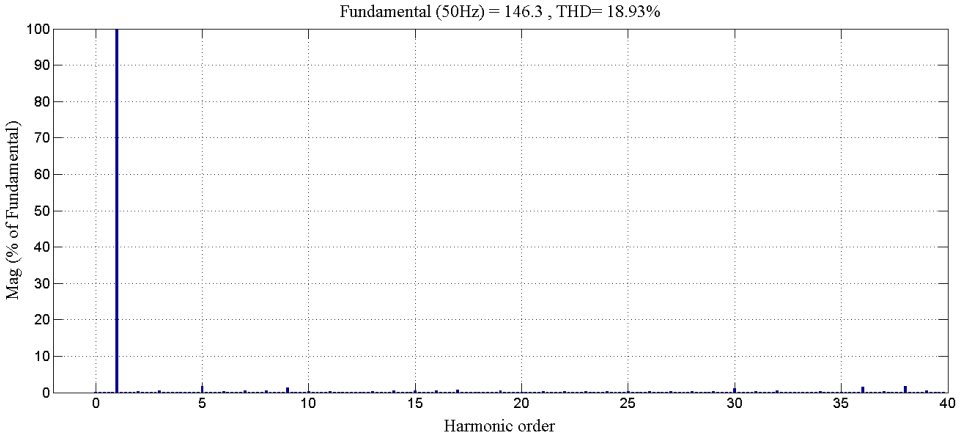
Figure 4.12: Line-to-line output voltage waveforms at different reference voltage amplitudes for the proposed four-level inverter.



(a) 20% reference voltage amplitude



(b) 50% reference voltage amplitude



(c) 80% reference voltage amplitude

Figure 4.13: Harmonic spectra at different reference voltage amplitudes for the proposed four-level inverter.

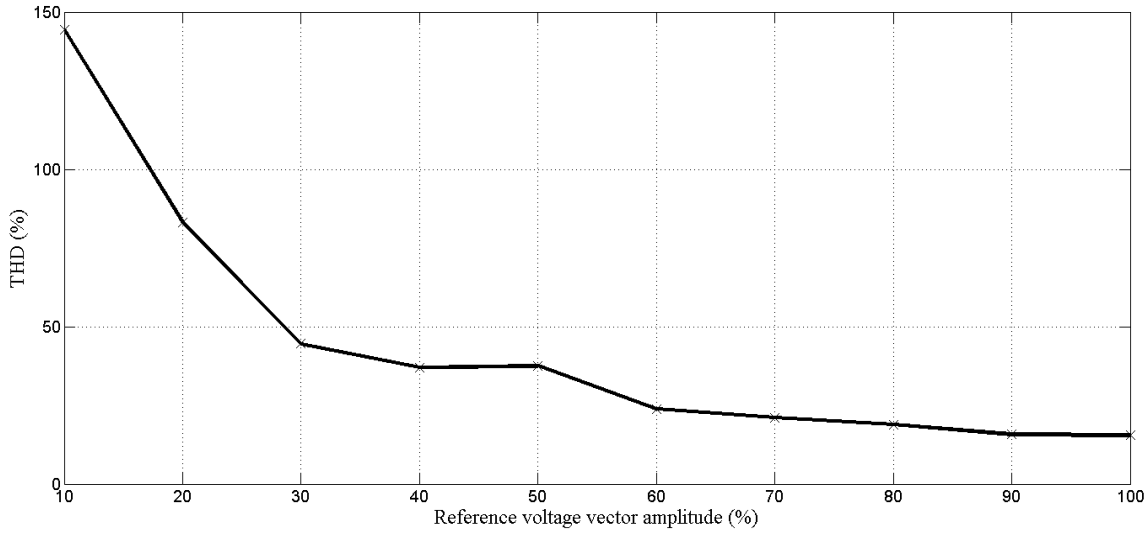


Figure 4.14: Line-to-line voltage THD performance of the proposed four-level inverter.

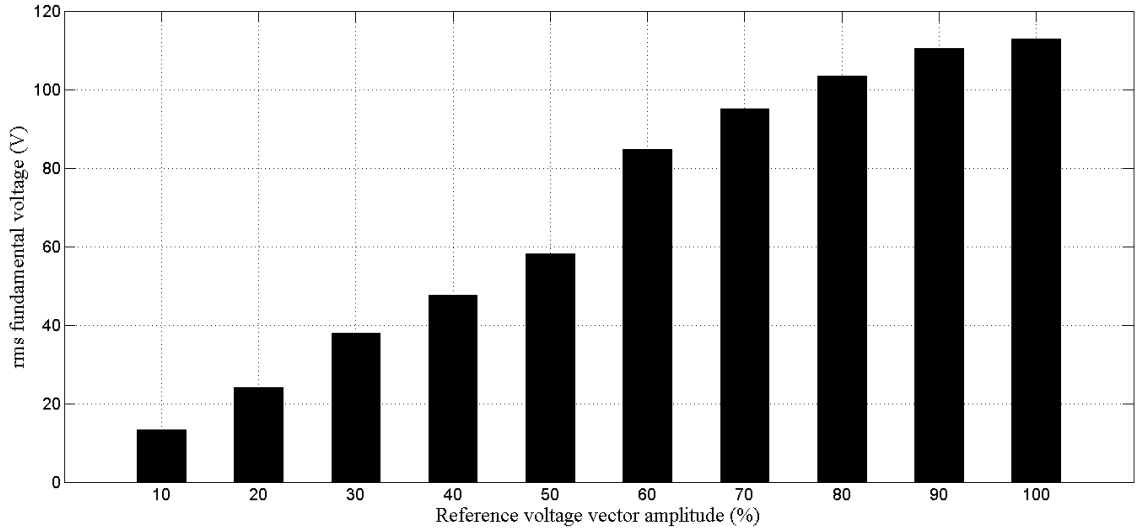


Figure 4.15: rms line-to-line fundamental voltage performance of the proposed four-level inverter.

4.3.2 Five-Level Inverter

The schematic circuit used for simulation is similar to the one described in Section 4.2.2. The difference is that the following simulation details are adopted: the proposed SVPWM applies a sampling frequency of 3.3 kHz and a Y-connected RL load is considered with R = 30.5 Ω per phase and L = 68 mH per phase. 3.3 kHz is selected

because this is the sampling frequency used for laboratory testing (refer to Section 5.5.1 for the details about the sampling frequency). Comparison of results between simulation and experiment can only be meaningful when the sampling frequencies used in both are the same. A MATLAB program code is prepared to carry out SVPWM in simulation based on the method explained in Section 4.3.1. Results from the simulation are provided in Figures 4.16 to 4.20.

From Figure 4.16, it can be noted that the number of voltage steps in the line-to-line output voltage waveform changes from three to five to seven and then to nine as the reference voltage amplitude approaches the 100% value. Figure 4.17 displays the four groups of waveform patterns which are taken at 10%, 40%, 60% and 90% amplitudes. Their corresponding harmonic spectra are given in Figure 4.18. As expected, THD performance improves as reference voltage amplitude becomes bigger. The following THD values are obtained: 137.78% (10% amplitude), 35.77% (40% amplitude), 32.83% (60% amplitude) and 13.04% (90% amplitude).

In terms of the harmonic performance, it can be noticed that significant low order harmonics appear in the harmonic spectrum taken at 40% amplitude as compared to the other harmonic spectra portrayed in Figure 4.18. As the most dominant harmonic, the fifth harmonic is considered as an example for investigation. From 10% to 40% amplitudes, the fifth harmonic magnitude rises from 7.2% to 19.27%. The harmonic magnitude then plummets to 4.54% at 60% amplitude. The magnitude is the lowest at 90% amplitude with a reading of 1.03%. Such a change exists for low order harmonics especially the fifth one is mainly contributed from the absence of $\sqrt{3}V_{dc}$ and $\sqrt{7}V_{dc}$ voltage vectors as explained in Section 3.4.3.2. The elimination of those vectors also affects THD performance of the line-to-line voltages as depicted in Figure 4.19. For the

range between 40% and 50% amplitudes, the THD records a rise from 35.77% to 42.27%. After the peak has been reached at 50% amplitude, a reduction in THD starts to appear. The effect of the abovementioned vector elimination seems to be the most significant between 40% and 60% amplitudes. Despite the noticeable change in THD in the range of amplitudes mentioned, it appears that the rms line-to-line fundamental voltage performance is not much affected. Figure 4.20 displays the fundamental voltage performance. The voltage increases almost linearly with the reference voltage amplitudes.

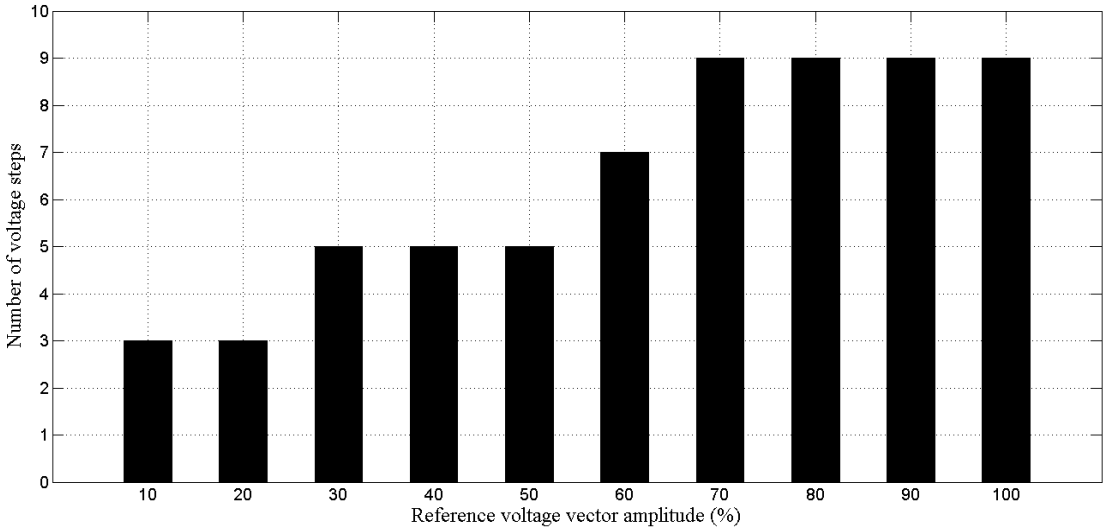
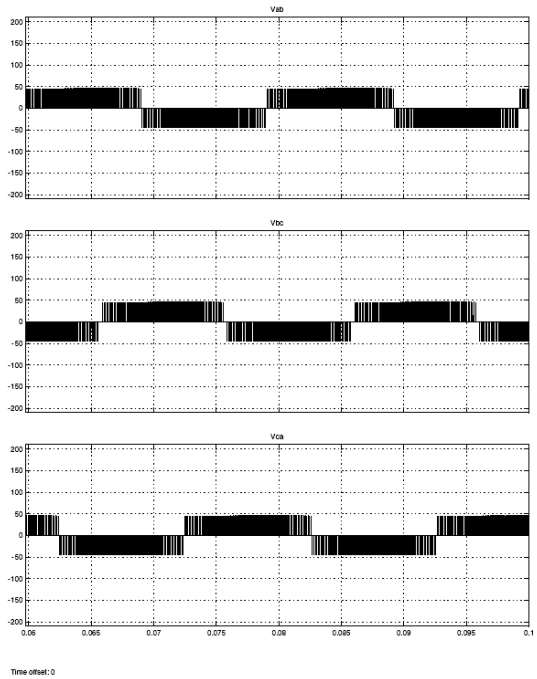
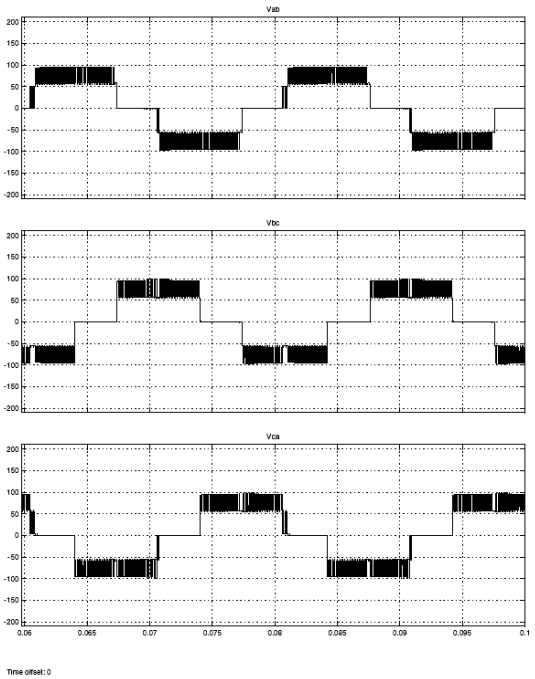


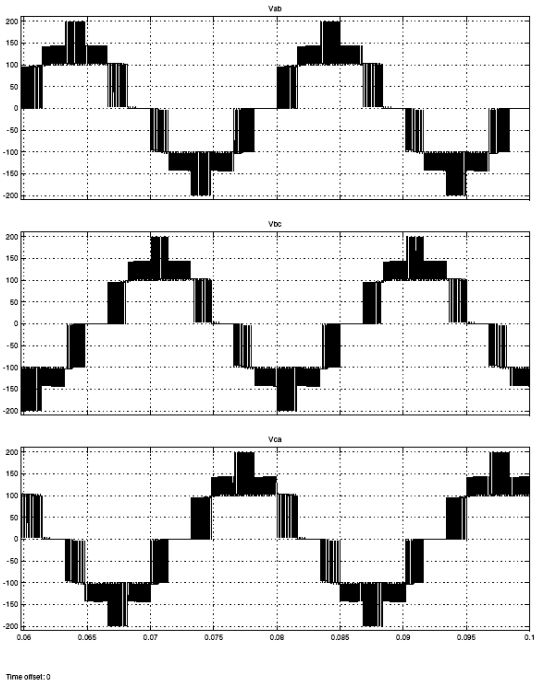
Figure 4.16: Number of voltage steps in the line-to-line output voltage waveforms of the proposed five-level inverter for various reference voltage amplitudes.



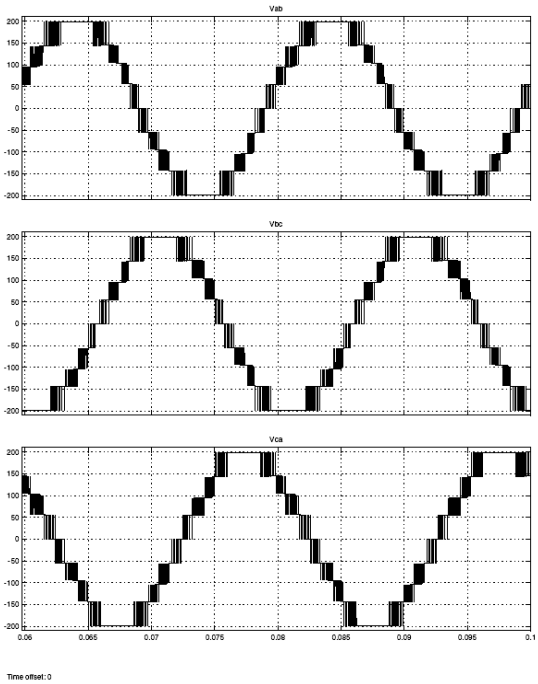
(a) 10% reference voltage amplitude



(b) 40% reference voltage amplitude

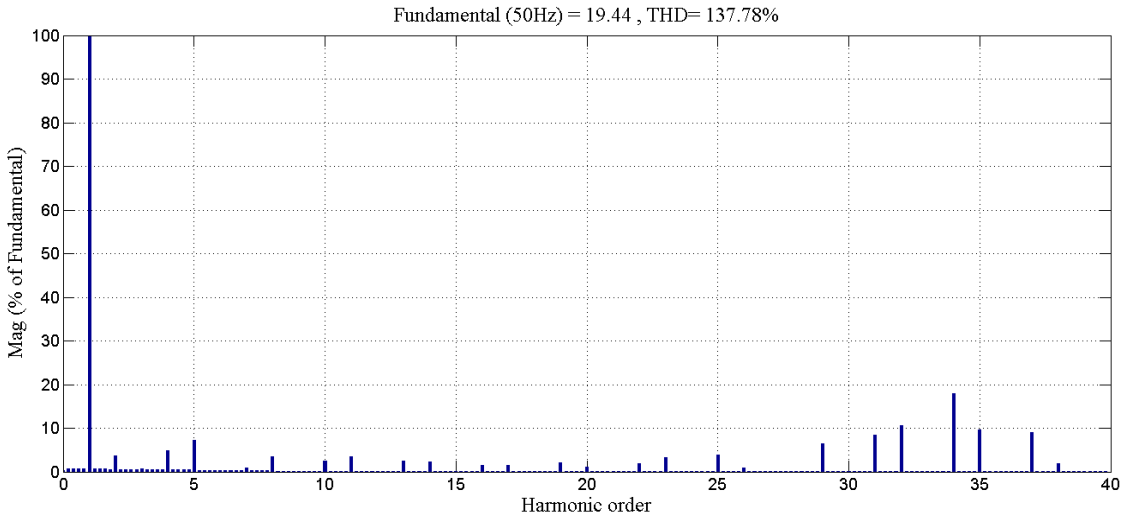


(c) 60% reference voltage amplitude

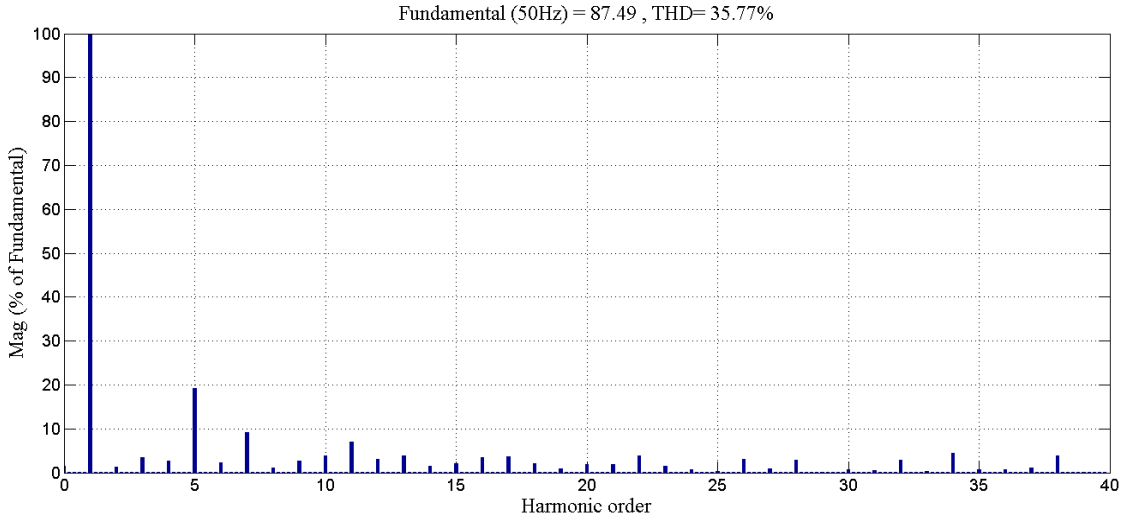


(d) 90% reference voltage amplitude

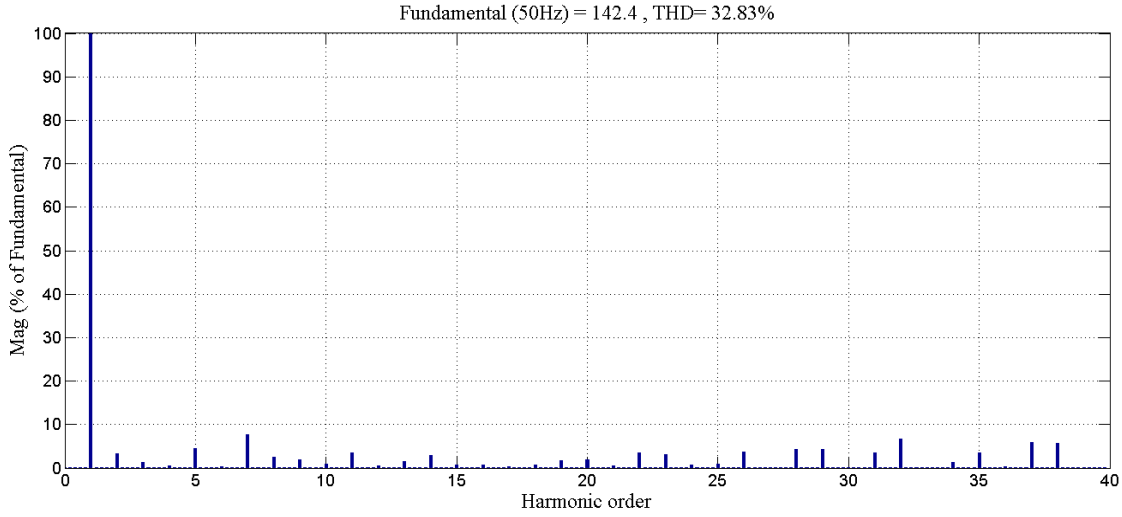
Figure 4.17: Line-to-line output voltage waveforms at different reference voltage amplitudes for the proposed five-level inverter.



(a) 10% reference voltage amplitude

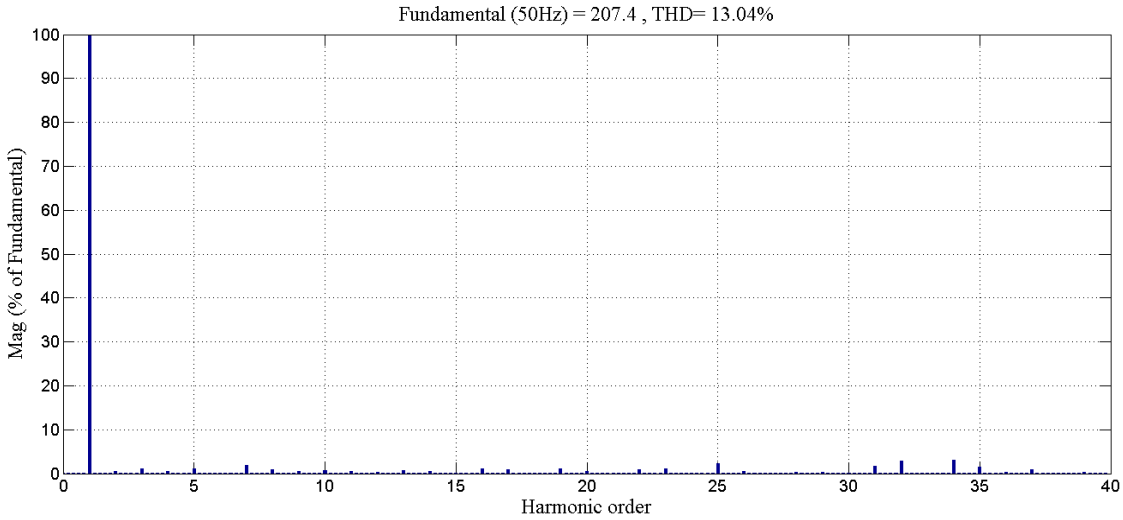


(b) 40% reference voltage amplitude



(c) 60% reference voltage amplitude

Figure 4.18: Harmonic spectra at different reference voltage amplitudes for the proposed five-level inverter.



(d) 90% reference voltage amplitude

Figure 4.18, continued: Harmonic spectra at different reference voltage amplitudes for the proposed five-level inverter.

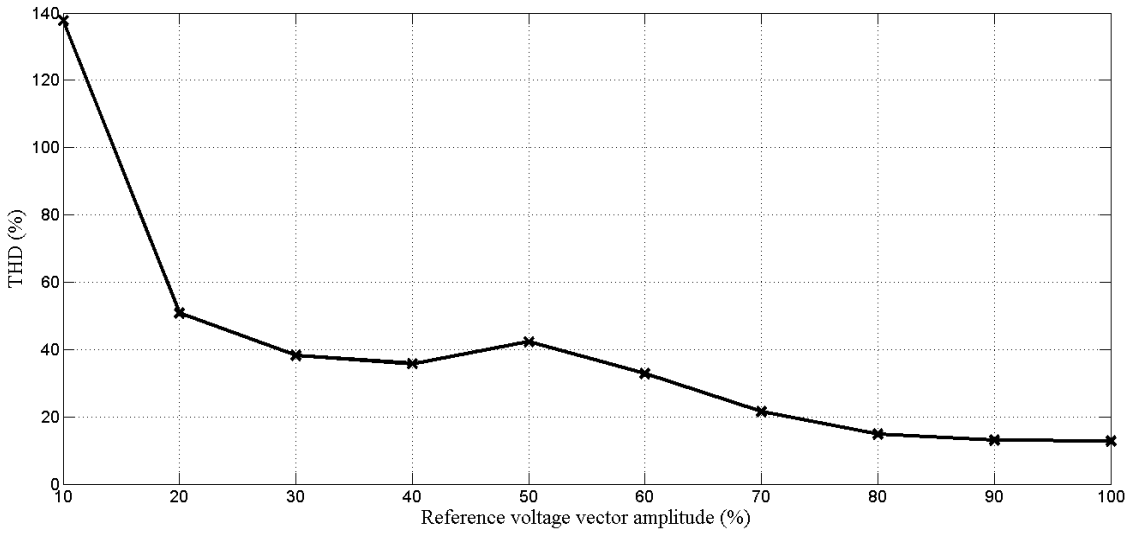


Figure 4.19: Line-to-line voltage THD performance the proposed five-level inverter.

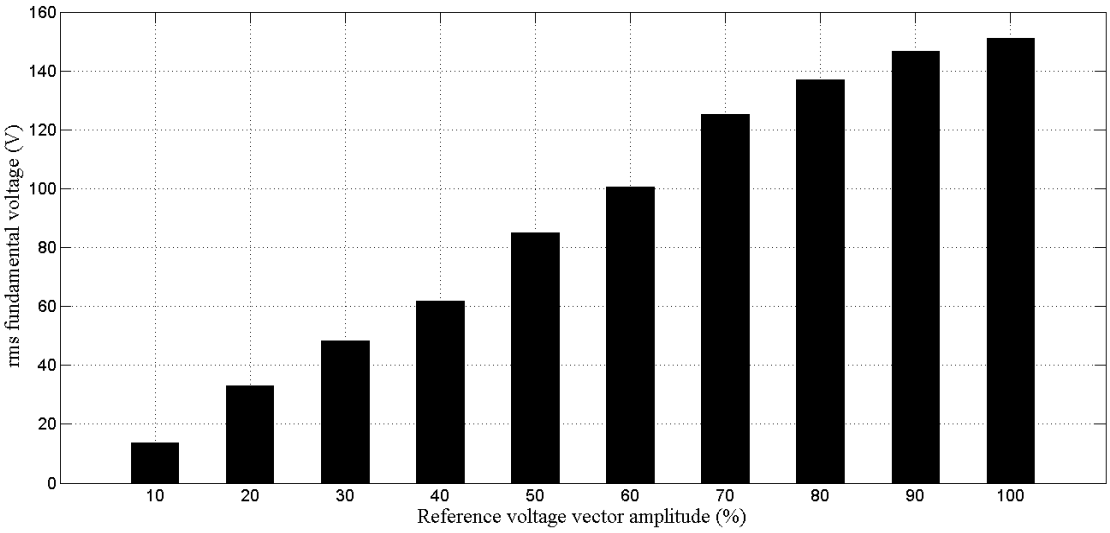


Figure 4.20: rms line-to-line fundamental voltage performance of the proposed five-level inverter.

4.4 Simulation for Power Loss

Estimation of the power losses can be made by basing the analysis on the characteristic curves which are usually found in the datasheet of the individual power device. In this study, only conduction and switching losses are considered as the off-state loss is so small that it can be neglected (Ebrahimi, Babaei, & Gharehpetian, 2012; Tae-Jin, Dae-Wook, Yo-Han, & Dong-Seok, 2001). From the relevant characteristic curves presented in the datasheet, mathematical equations that reflect the curves can be derived (Govindaraju & Baskaran, 2011). Equation that relates the forward voltage drop across the device and the conducted current is used to calculate the conduction loss. For the switching loss of the power switching device which is due to the turn-on and turn-off commutation as well as the reverse recovery of the freewheeling diode, it is estimated from the energy loss curve with respect to current. As for the diodes in the bidirectional switches, the switching loss due to reverse recovery process can be approximated from the reverse recovery time t_{rr} and reverse recovery current I_{RRM} curves.

In this analysis, the power switching devices selected are the IGBT modules IRG4PC40UDPbF from International Rectifier. The diodes used to construct the bidirectional switches are assumed to have the same characteristics as the freewheeling diodes in the IGBT modules. By using the datasheet of the IGBT modules (refer to the appendix), the curves which are relevant for the calculation of conduction and switching losses are obtained from the points extracted from the datasheet. Mathematical models that represent these curves are derived using MATLAB curve-fitting tool. The mathematical models are given as follows:

$$V_{CE} = 3.141e^{0.003496i(t)} - 2.296e^{-0.01392i(t)} \tag{4.5}$$

$$V_F = 1.396e^{0.009157i(t)} - 0.5844e^{-0.1733i(t)} \tag{4.6}$$

$$E_{TS} = 15.62(e^{0.009769i(t)} - e^{0.009764i(t)}) \tag{4.7}$$

$$t_{rr} = (82.33e^{0.001376i(t)} - 35.89e^{-0.08029i(t)}) \times 10^{-9} \tag{4.8}$$

$$I_{RRM} = 6.367e^{0.003473i(t)} - 0.713e^{-0.07622i(t)} \tag{4.9}$$

Here, V_{CE} is the collector-to-emitter voltage, V_F is the forward voltage drop and E_{TS} is the total switching energy loss of the IGBT module. To calculate the conduction loss, the following are used:

$$P_{cond,IGBT} = \frac{1}{T_p}\int V_{CE} i(t) dt \tag{4.10}$$

$$P_{cond,Diode} = \frac{1}{T_p}\int V_F i(t) dt \tag{4.11}$$

$P_{cond,IGBT}$ and $P_{cond,Diode}$ are the conduction losses of IGBT and diodes respectively and T_p is the period for one cycle. The total switching power loss of IGBT, $P_{sw,IGBT}$ is calculated using equation (4.12) below:

$$P_{sw,IGBT} = \frac{1}{T_p}\sum E_{TS} \tag{4.12}$$

The switching energy loss of the diodes in the bidirectional switches, $E_{sw,Diode}$, is due to the reverse recovery process. It is approximated by using equation (4.13) below (Khersonsky, Robinson & Gutierrez, 1992):

$$E_{sw,Diode} = \frac{V_R I_{RRM} t_b}{4} \tag{4.13}$$

where

$$t_b = t_{rr} - t_a \tag{4.14}$$

and

$$t_a = \frac{I_{RRM}}{\frac{di(t)}{dt}} \tag{4.15}$$

V_R is the reverse voltage drop and $\frac{di(t)}{dt}$ is the forward current rate. Both are constants which are specified in the datasheet. t_a is the time required for the diode reverse current to increase from zero to its peak negative value and t_b is the time required for the same current to fall from its peak negative value to zero (Khersonsky, Robinson & Gutierrez, 1992). The final result of $E_{sw,Diode}$ is as follows:

$$E_{sw,Diode} = (16.2e^{0.003252i(t)} - 10.4e^{-0.076497i(t)} - 1.815e^{-0.076441i(t)} + 1.166e^{-0.1562i(t)}) \times 10^{-6} \tag{4.16}$$

Therefore, the total switching power loss of diode, $P_{sw,Diode}$ is calculated as follows:

$$P_{sw,Diode} = \frac{1}{T_p} \sum E_{sw,Diode} \tag{4.17}$$

The total power loss, P_{loss} is the sum of all conduction and switching losses as represented in equation (4.18).

$$P_{loss} = P_{cond,IGBT} + P_{cond,Diode} + P_{sw,IGBT} + P_{sw,Diode} \tag{4.18}$$

If the output power is denoted by P_{out}, as given in equation (4.19), then efficiency η can be approximated using equation (4.20).

$$P_{out} = 3V_{rms}I_{rms}\cos\gamma \tag{4.19}$$

$$\eta = (1 - \frac{P_{loss}}{P_{out} + P_{loss}}) \times 100\% \tag{4.20}$$

V_{rms} represents the root mean square (rms) value of the load phase voltage, I_{rms} is the rms value of the load current and cos γ denotes the power factor.

4.4.1 Four-Level Inverter

The power loss analysis for the proposed four-level inverter is conducted at a sampling frequency of 4.6 kHz using MATLAB/SIMULINK software. The inverter is supplied with a total DC voltage of 150 V. The simulation results of the power loss analysis are given in Figures 4.21 to 4.24. Figures 4.21 and 4.22 are obtained at an 80% reference voltage vector. It can be observed that with the increase in power factor, total power loss and efficiency also reflect an upward trend. This is possible since the output power also grows as the power factor approaches the maximum value, namely 1. The increase in output power outweighs the increase in power loss which in turn contributes to the rise in efficiency. The highest total power loss is 17.84 W, recorded at unity power factor. At 0.94 power factor, the best efficiency is achieved at 95.5%.

To obtain the variation in efficiency from low reference voltage vector to the maximum amplitude, Figure 4.23 is presented. Here, the data is collected at 0.82 power factor. Starting from 60% mark of the reference voltage vector, efficiency begins to go beyond 90%. The highest efficiency is 96.23% which is observed at the maximum reference voltage vector amplitude. Figure 4.24 shows the power loss distribution among the semiconductor devices which are obtained at 0.82 power factor and 80%

reference voltage vector. The power loss for each power switch accounts for the conduction and switching losses of the IGBT and the diodes related to the power switch. All switches record almost equal power loss except those in Module 3 namely Q_{S1} and Q_{S2}. This is expected since the two switches operate for the three phases, instead of specifically used for a certain phase as in the case of the other switches.

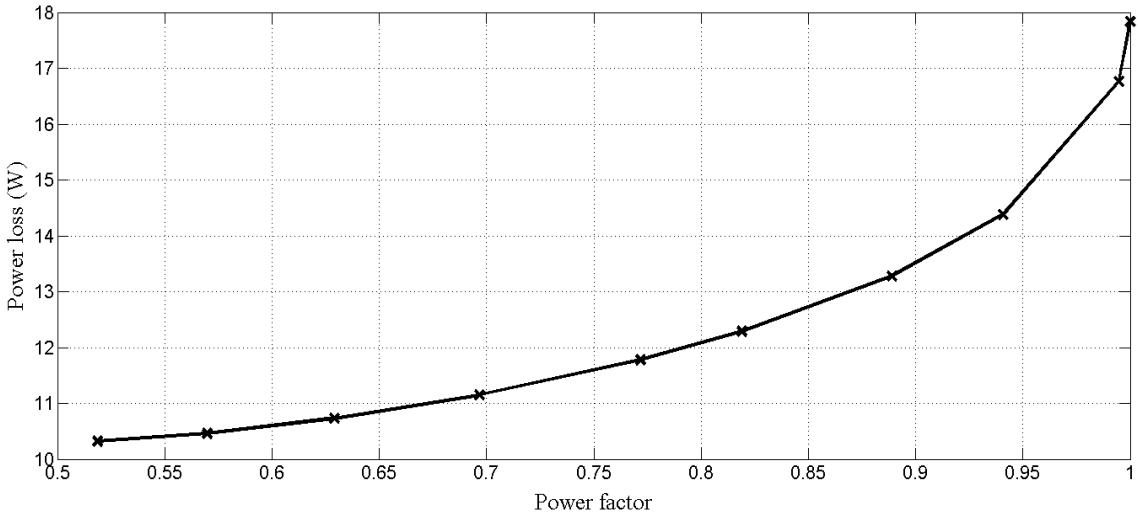


Figure 4.21: Total power loss variation with respect to power factor for the proposed four-level inverter (at 80% reference voltage vector).

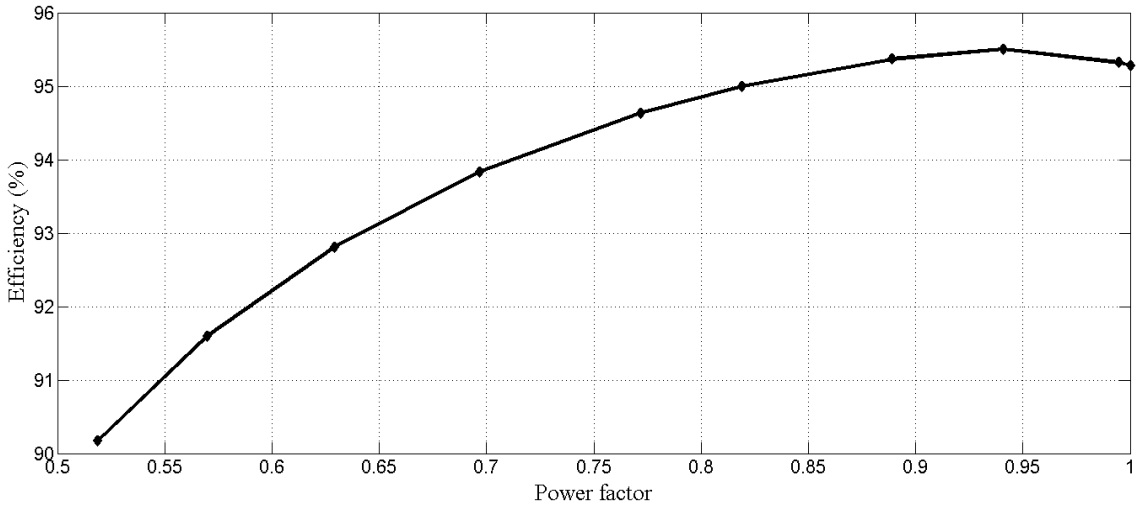


Figure 4.22: Variation in efficiency with respect to power factor for the proposed four-level inverter (at 80% reference voltage vector).

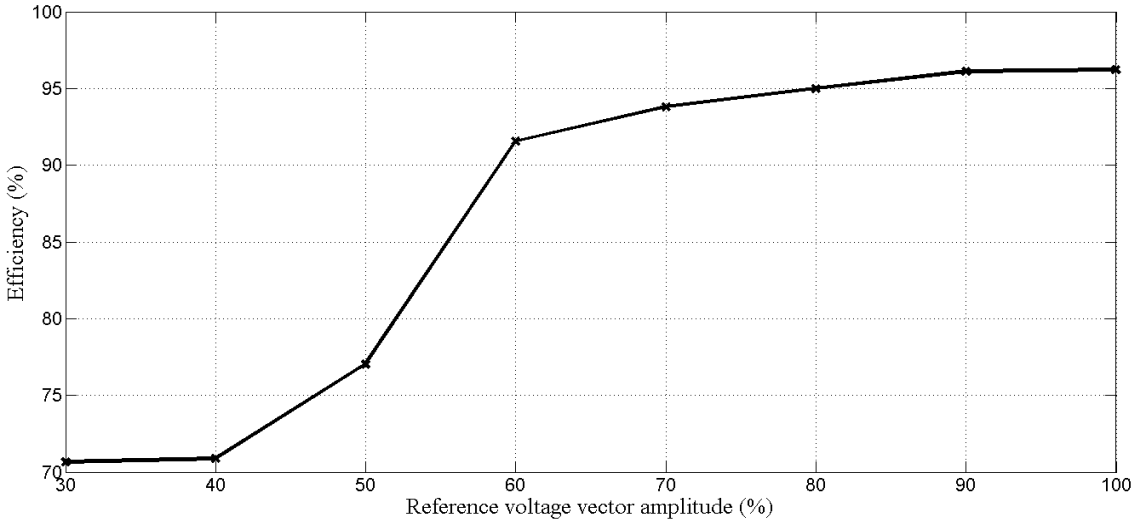


Figure 4.23: Variation in efficiency with respect to reference voltage amplitude for the proposed four-level inverter (at 0.82 power factor).

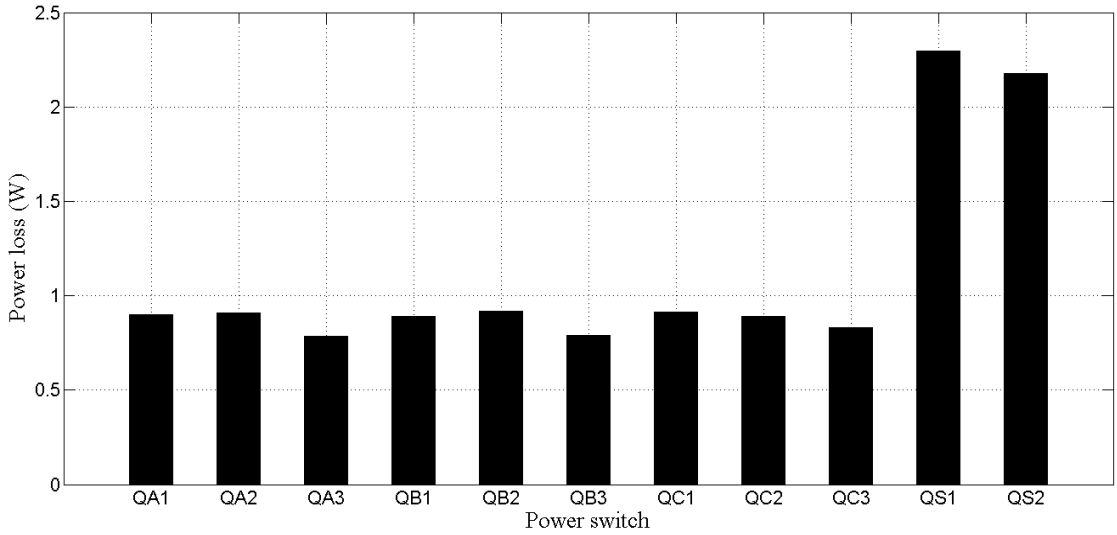


Figure 4.24: Power loss distribution among the power switches for the proposed four-level inverter (at 0.82 power factor and 80% reference voltage vector).

4.4.2 Five-Level Inverter

In the power loss study for the proposed five-level inverter, the sampling frequency is set at 3.3 kHz and the total input DC voltage applied to the inverter is 200 V. Figures 4.25 to 4.28 presents the simulation results obtained. The power loss and efficiency variations with respect to power factor as shown in Figure 4.25 and 4.26 respectively are taken at 90% reference voltage vector. As power factor increases, both power loss and efficiency also increases in an exponential manner. The increase in efficiency is realized since the output power growth exceeds the increase in power loss as the power factor rises to the maximum. For the power loss curve, the peak value is 26.34 W which occurs at unity power factor. As for efficiency, the peak value viz 96.62%, is recorded at a slightly lower power factor namely 0.94.

In Figure 4.27, the efficiency curve is obtained by varying the amplitude of the reference voltage vector while maintaining the power factor at 0.82. Efficiency starts to exceed 90% when the reference vector amplitude is 50% or more. The highest efficiency is 96.63% that happens when a 100% reference voltage vector is applied. From the power loss distribution analysis as summarized in Figure 4.28, it can be observed that the power loss is more or less uniformly distributed among ten power switches with an average loss of 1.19 W. For the remaining two switches namely the top and bottom outer switches of Module 3 (Q_{S1} and Q_{S3}), the power loss is about double as compared to the others.

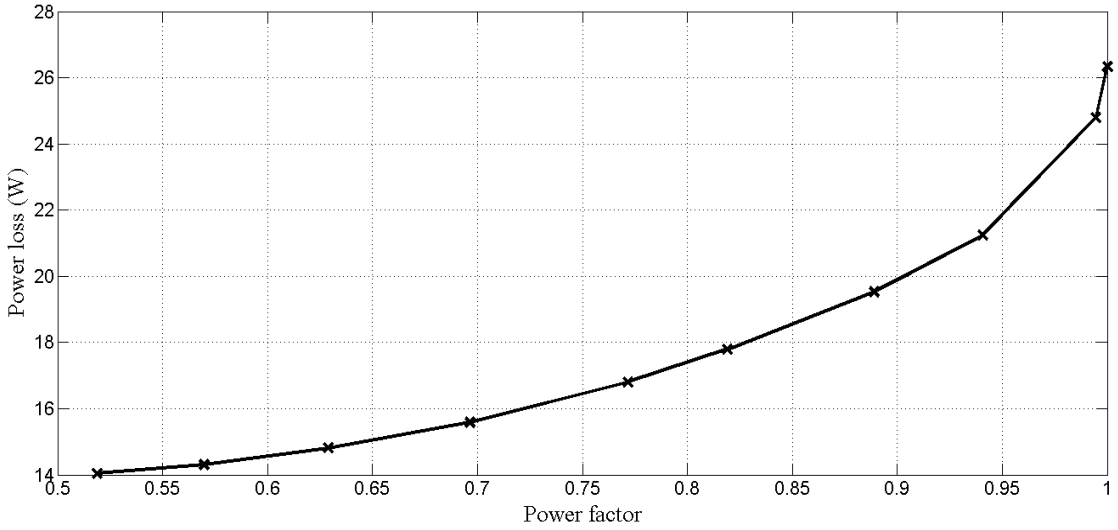


Figure 4.25: Total power loss variation with respect to power factor for the proposed five-level inverter (at 90% reference voltage vector).

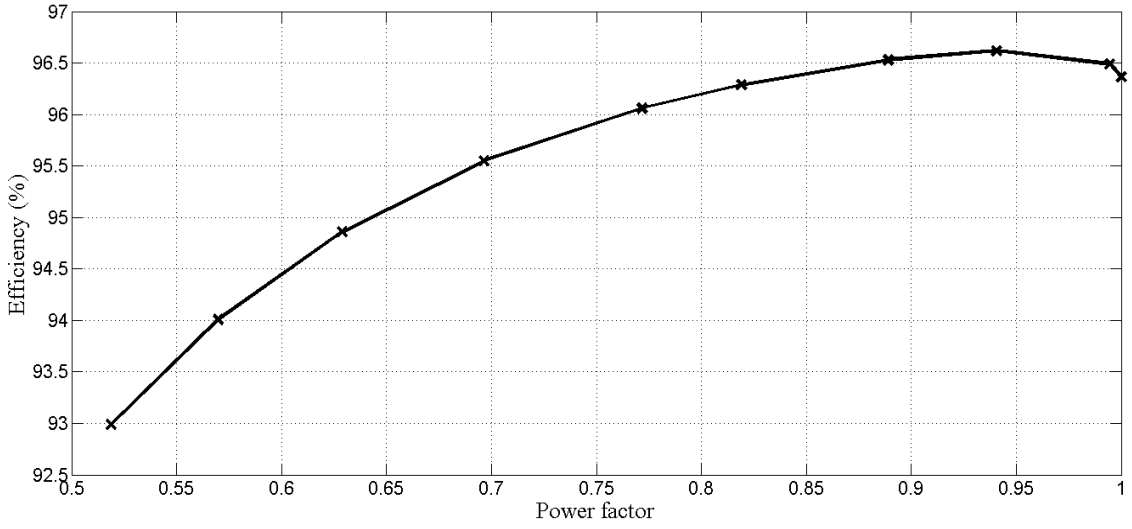


Figure 4.26: Variation in efficiency with respect to power factor for the proposed five-level inverter (at 90% reference voltage vector).

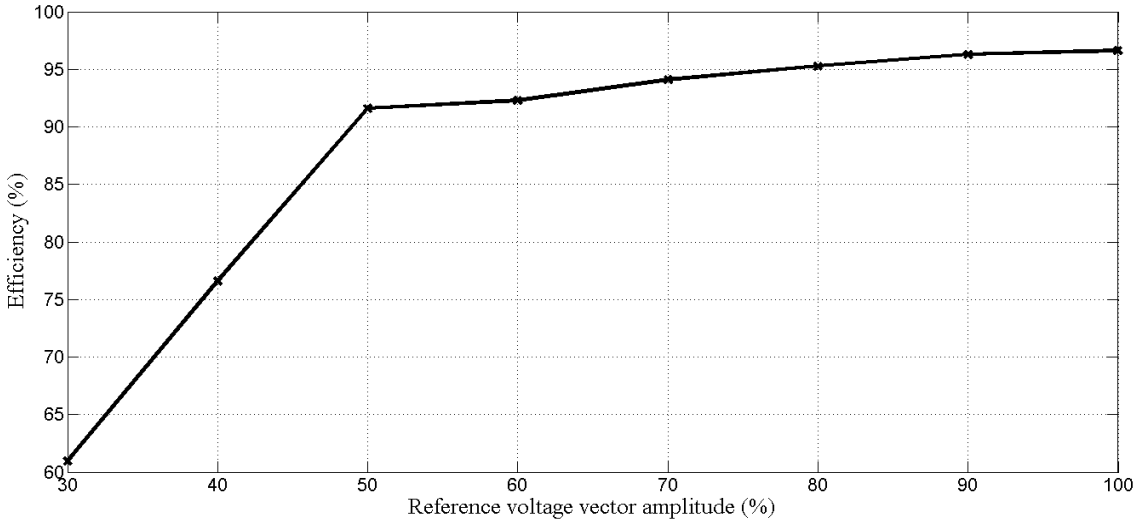


Figure 4.27: Variation in efficiency with respect to reference voltage amplitude for the proposed five-level inverter (at 0.82 power factor).

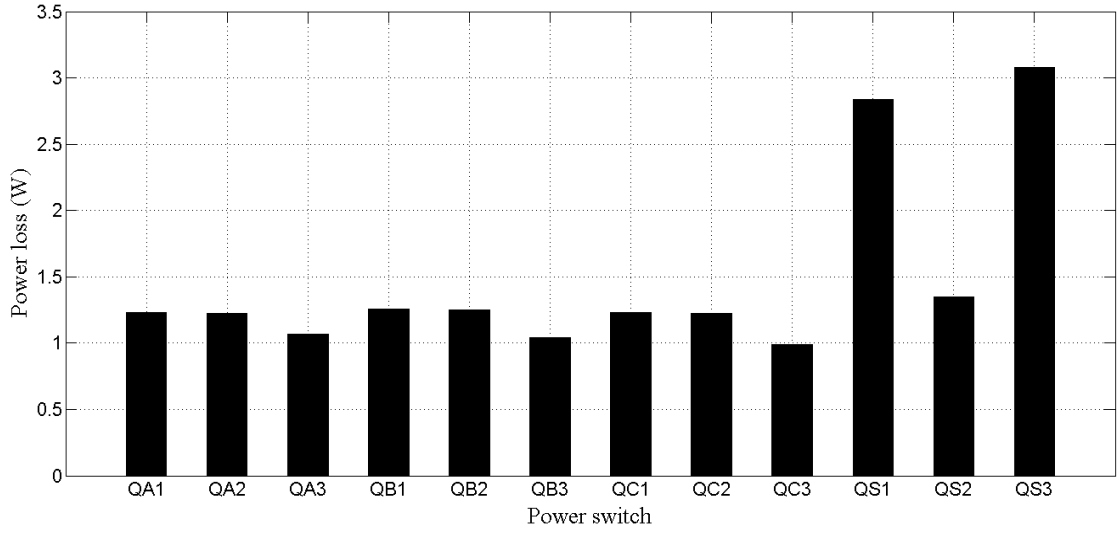


Figure 4.28: Power loss distribution among the power switches for the proposed five-level inverter (at 0.82 power factor and 90% reference voltage vector).

4.5 Comparison with Diode-Clamped Topology

In order to have a meaningful assessment of the characteristics and performance of the proposed multilevel inverter, a comparison is made with other topologies. The three classical topologies are the most appropriate since they are the most deeply studied and the most widely used in the industry. Therefore, the comparative analysis will not be complete without having any of these topologies as the benchmark. In this study, the comparative investigation is conducted with the diode-clamped topology is chosen as the best reference for comparison. Such a selection is made due to the fact that the diode-clamped topology carries the most resemblance to the proposed topology, as pointed out in Section 3.1.

To have a sound comparison, the proposed and the diode-clamped topologies are investigated under the same simulation conditions as provided in Table 4.1. The load is a Y-connected type. While the proposed topology employs the novel SVPWM method, the diode-clamped topology adopts the conventional SVPWM technique. Table 4.2 summarizes the characteristics comparison between the two topologies for the four-level and five-level structures. It can be observed that the proposed topology offers lower number of semiconductor devices. It also has higher level-to-switch ratio which increases as the number of levels rises. This is opposite to the diode-clamped topology whereby the ratio reduces when the number of levels increases. The proposed topology also has a fixed number of active switches per switching state per phase regardless of the number of levels. On the contrary, the diode-clamped topology adds an extra active switch per switching state per phase every time the number of levels increases by one.

Table 4.1: Simulation conditions for the four-level and five-level structures of the comparative analysis.

Simulation conditions		Inverter's structure	
		Four-level	Five-level
Total input DC voltage (V)		150	200
Sampling frequency (kHz)		4.6	3.3
Load	R (Ω per phase)	30.5	30.5
	L (mH per phase)	68.0	68.0

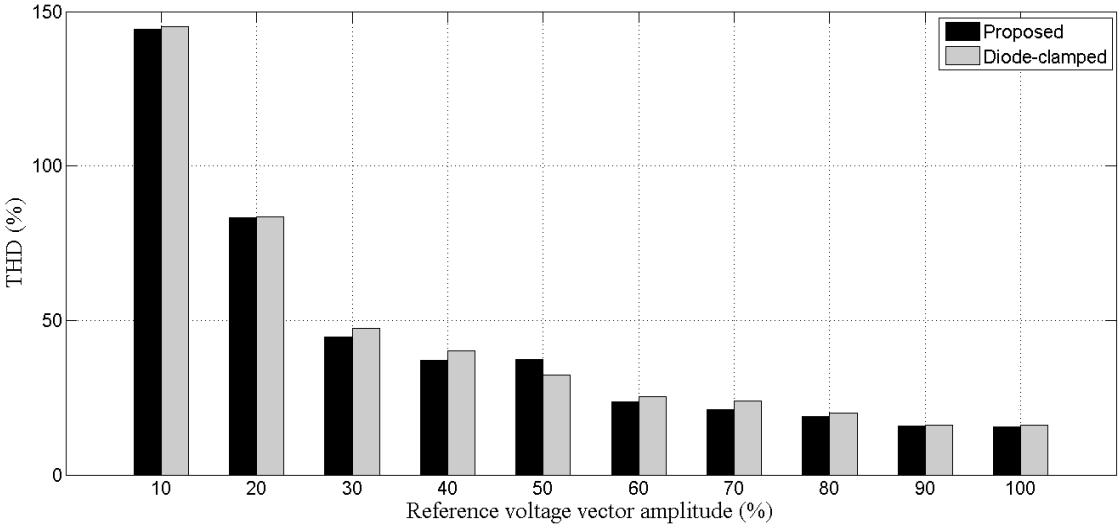
Table 4.2: Characteristics comparison between the proposed and the diode-clamped topologies for the four-level and five-level structures.

Characteristics	Topology			
	Four-level		Five-level	
	Proposed	Diode-clamped	Proposed	Diode-clamped
Number of main switches	11	18	12	24
Number of diodes other than clamping diodes	26	18	30	24
Number of clamping diodes	0	18	0	36
Level-to-switch ratio	0.3636	0.2222	0.4167	0.2083
Number of active switches per switching state per phase	1 for minimum and maximum states, 2 for other states	3 for every state	1 for minimum and maximum states, 2 for other states	4 for every state

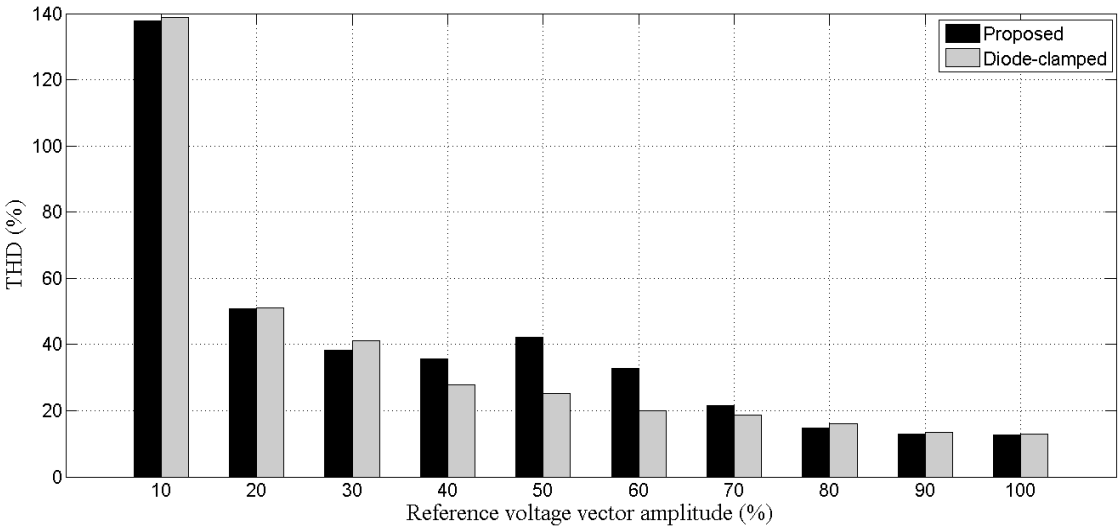
The line-to-line voltage THD comparisons between the two topologies for the four-level and five-level structures are given in Figure 4.29. From the THD results, it reflects a close agreement between the two topologies for all reference voltage amplitudes except at a certain amplitude range. For the four-level structure, the absence of the six voltage vectors causes the proposed topology to record an increase in THD by

15.86% at 50% reference voltage amplitude as compared to the diode-clamped counterpart. The five-level proposed inverter also shows higher THD within 40% and 60% amplitude range with the highest is recorded at 42.27%. This is also due to elimination of 18 voltage vectors in the proposed five-level structure. However, in terms of the fundamental voltage amplitude, it appears that both topologies portray an upward trend as the reference voltage amplitude increases. Figure 4.30 provides the fundamental voltage comparison between the two topologies.

Power loss comparative analysis is also conducted between the two topologies. The reference voltage amplitudes are set at 80% and 90% for the four-level and five-level structures respectively. The simulation results are displayed in Figure 4.31. It can be seen that the switching loss between the two topologies are almost similar especially for the five-level structure. Only the diode switching loss for the four-level structure shows a slight difference. On the other hand, the conduction loss provides a different picture. The proposed topology records higher diode conduction loss as compared to that of the diode-clamped topology. However, this is compensated by the lower conduction loss generated by the IGBTs in the proposed topology. In terms of the overall power loss produced, the proposed topology dissipates lower power loss. If these losses are only considered for efficiency calculation, then, the proposed topology offers 95.0% and 96.29% for the four-level and five-level structures respectively as compared to 94.14% and 94.89% for the respective equivalent diode-clamped inverters.

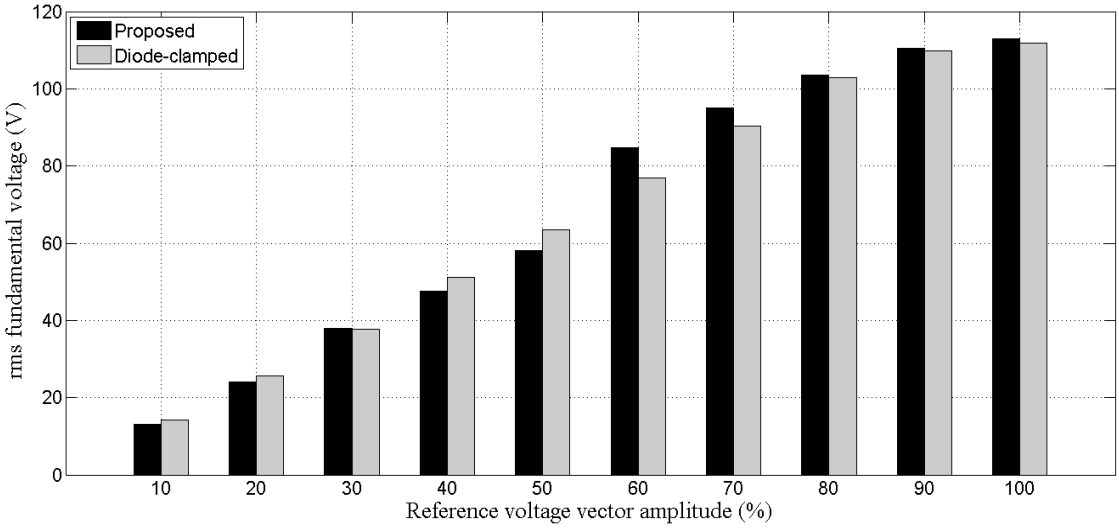


(a) Comparison for four-level structure

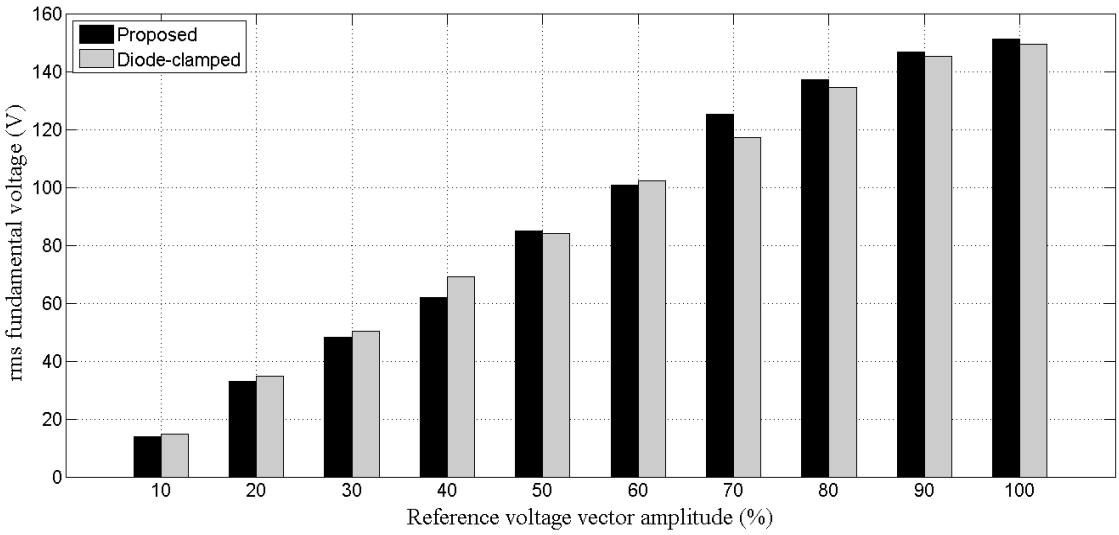


(b) Comparison for five-level structure

Figure 4.29: Line-to-line voltage THD comparison between the proposed and diode-clamped topologies.

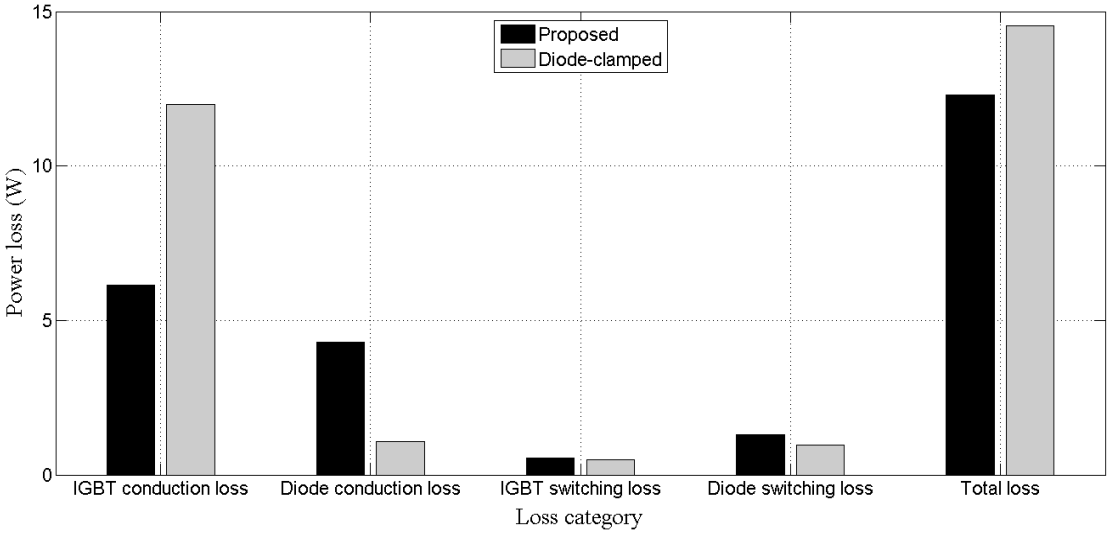


(a) Comparison for four-level structure

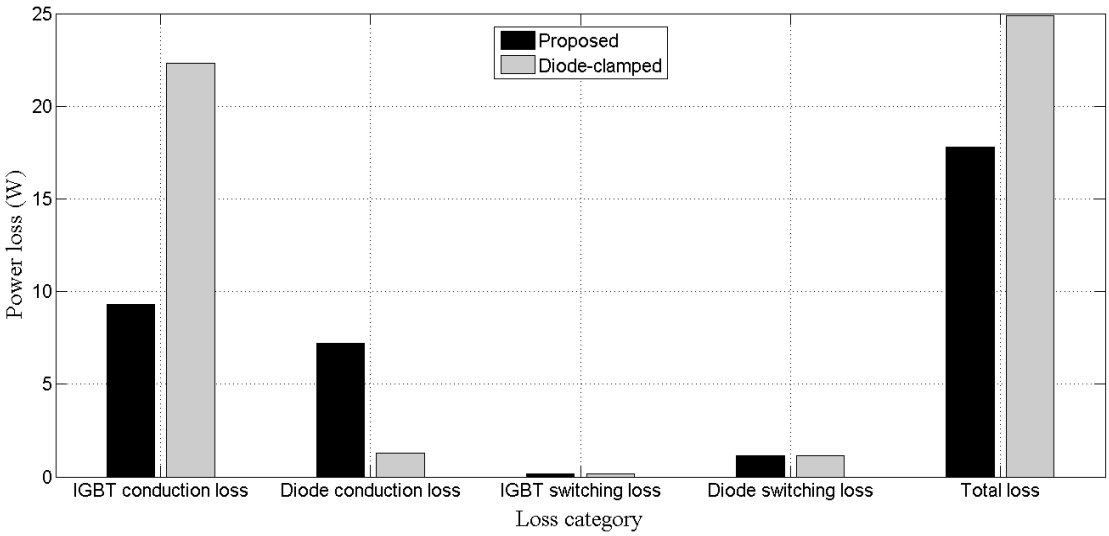


(b) Comparison for five-level structure

Figure 4.30: Fundamental voltage comparison between the proposed and diode-clamped topologies.



(a) Comparison for four-level structure



(b) Comparison for five-level structure

Figure 4.31: Power loss comparison between the proposed and diode-clamped topologies.

4.6 Simulation for Current Control Scheme

In order to investigate the effectiveness of the PI controller with the proposed tuning algorithm by simulation, an additional MATLAB program code is prepared using a new "embedded MATLAB function" block. The program executes parameter transformation and calculation and PI controllers' operation to generate the reference voltage vector and its position before feeding to the other "embedded MATLAB function" block that runs the proposed SVPWM algorithm. For this simulation, the VOC and DPC-SVM current control schemes are employed with the proposed four-level inverter. Three inductive filters of 10mH per phase are placed between the inverter and the load. The inverter is supplied with a total DC voltage of 150 V and the sampling frequency of the SVPWM is set at 4.6 kHz. To set suitable values for the proportional and integral gains of the controller, trial-and-error method is adopted for fine-tuning for a chosen load parameter. In this simulation, the gains are determined at 30.5 Ω load value. These gains are then used for other load values as well so that they are kept as constants regardless of any load changes. By doing so, the automatic tuning performance can be appropriately evaluated. Step responses which are resulted from load changes, are investigated in this simulation study with the focus more on the quality of the output current.

4.6.1 Step Response with VOC Scheme

For simulation of the VOC scheme, two PI controllers are used for the *d*- and *q*-component currents. All parameters of the controllers are made constant regardless of the load value except for the bottom bound U_{low} of the anti-windup module of the PI controller for the *d*-component current. U_{low} is adjusted according to the automatic tuning algorithm described in Section 3.5.5. The acceptable value of U_{low} is achieved as long as V_{ref} is within the V_{aim} band. The value of V_{aim} selected is the 80% amplitude of

the reference voltage vector since at this amplitude, the inverter voltage THD is acceptably low as compared to other amplitudes and the corresponding harmonic spectrum is good as displayed in Figure 4.13(c). V_{aim} is fixed for any given load so that V_{ref} derived from the PI controllers is always maintained to be close to V_{aim}, which is realized through the adjustment of U_{low}.

Figure 4.32 shows the simulation results reflecting the step response as a result of a load change from 30.5 Ω to 12.0 Ω. With the change in load, $i_{d,ref}$ also changes, which then causes the PI controllers to react. With the aid of the automatic tuning, i_d is able to track its reference satisfactorily. The line-to-line voltage waveforms at the inverter output and the load are similar before and after the load change. In the figure, only the waveforms for phase A are shown. Variation of V_{ref} with respect to V_{aim} is small and this influences the quality of the output current produced. The THDs of the output current are 3.28% and 1.74% before and after the load change respectively. Figure 4.33 presents the output current waveforms of the three phases. The automatic tuning algorithm employed in this simulation leads to the increase of U_{low} from an average value of -7.0 before the load change, to 3.0 after the change occurs.

To evaluate the improvement made by the PI controller with the tuning algorithm in improving the THD of the output currents, simulation is also conducted for the PI controller without the tuning module. Simulation conditions are set to be the same as the one when the PI controller with the tuning capability is utilized to ensure a fair comparison. U_{low} is made constant at a value of -7.0. The simulation results are portrayed in Figure 4.34. It can be observed that the reference tracking performance and the voltage and current waveforms are almost similar to those depicted in Figure 4.32 except the V_{ref} variation which shows significant fluctuations after the load change. As a

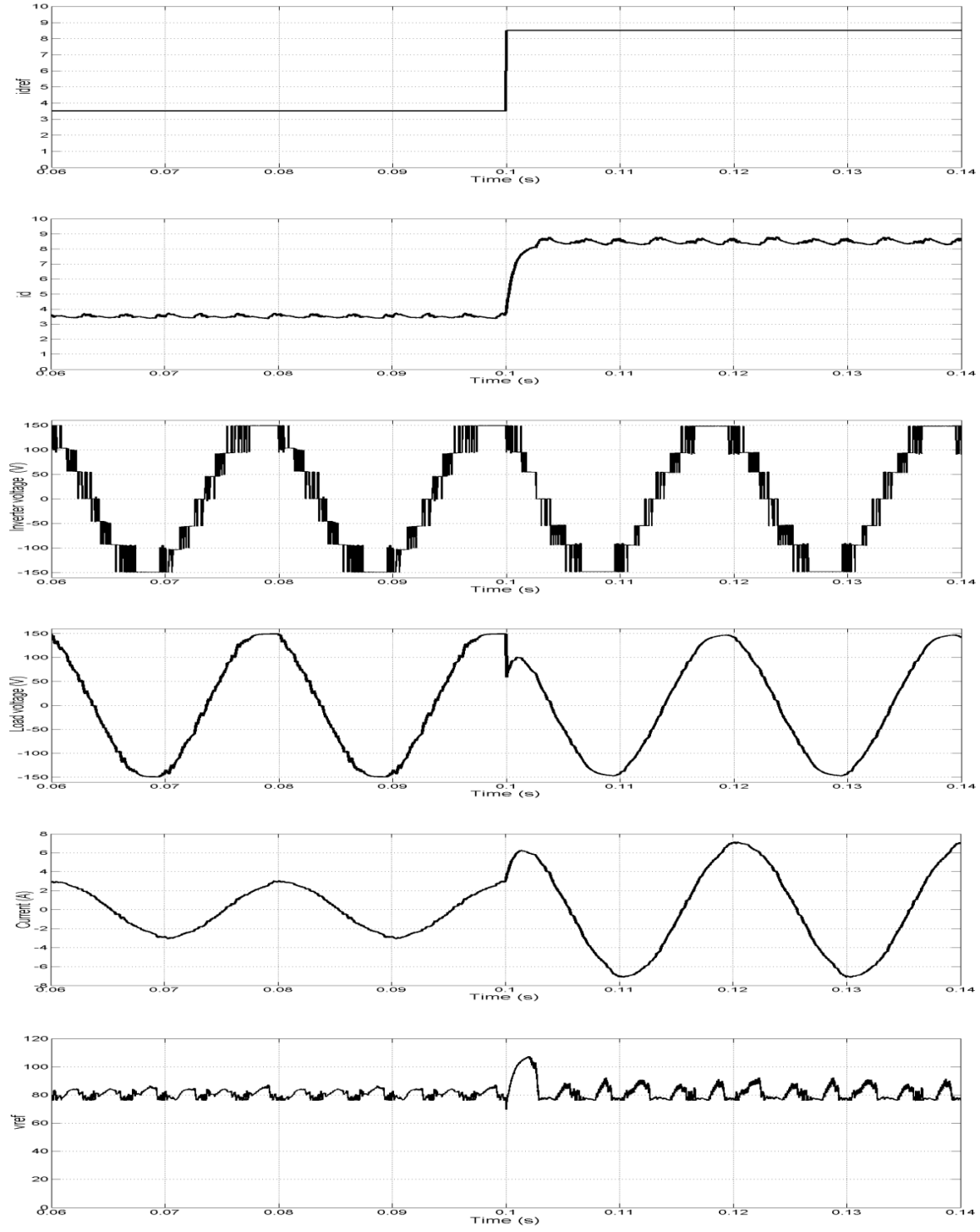


Figure 4.32: Step response as a result of a load change from 30.5 Ω to 12.0 Ω for VOC scheme with automatic tuning algorithm, from top to bottom: $i_{d,ref}$, i_d, v_{AB} (inverter side), v_{ab} (load side), i_A and V_{ref}.

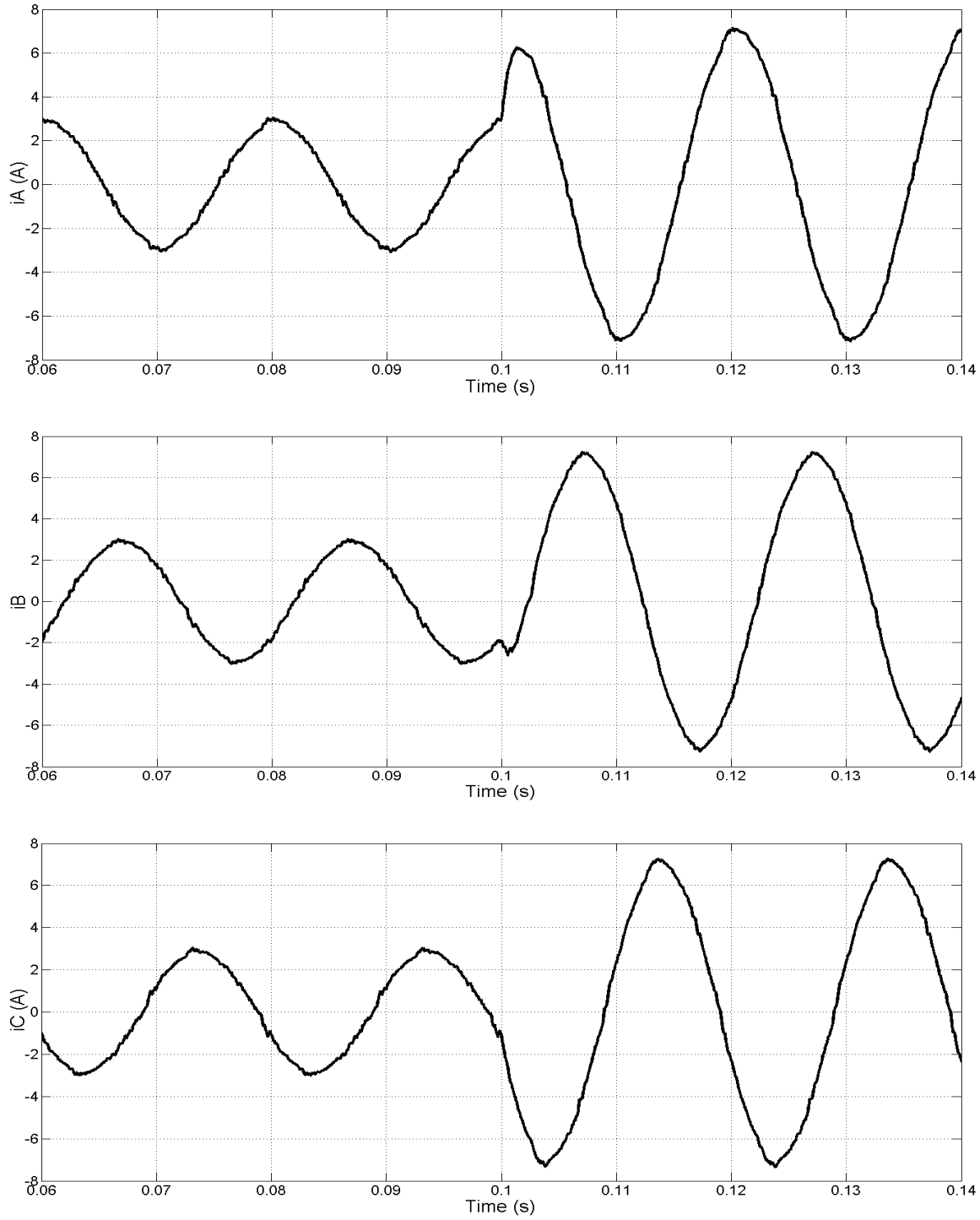


Figure 4.33: Step response as a result of a load change from 30.5 Ω to 12.0 Ω for VOC scheme with automatic tuning algorithm, from top to bottom: i_A, i_B and i_C.

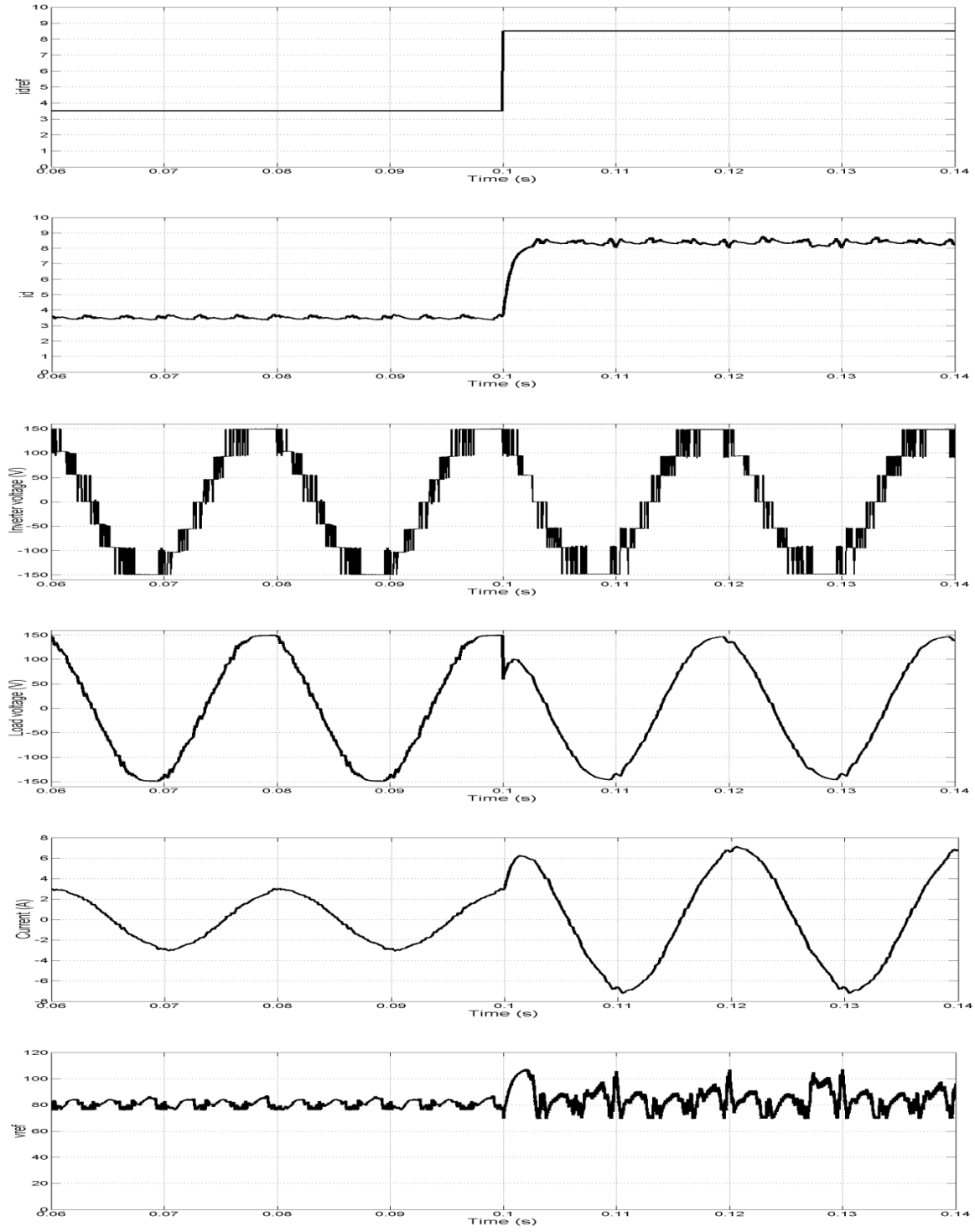


Figure 4.34: Step response as a result of a load change from 30.5 Ω to 12.0 Ω for VOC scheme without automatic tuning algorithm, from top to bottom: $i_{d,ref}$, i_d, v_{AB} (inverter side), v_{ab} (load side), i_A and V_{ref}.

consequence, output current THD after the load change is recorded at 2.38%, higher than that when the tuning algorithm is applied. This proves that the tuning algorithm provides a beneficial mechanism to improve the THD of the output currents in changing load conditions.

4.6.2 Step Response with DPC-SVM Scheme

In DPC-SVM scheme, power PI controllers for p and q are used in the simulation instead of the current controllers. All simulation details are similar to those for the simulation with the VOC scheme. Simulation is carried out with and without the automatic tuning algorithm so that comparison can be made between the two. For DPC-SVM scheme, the tuning algorithm attempts to adjust U_{low} of the anti-windup module of the PI controller for the real power so that V_{ref} is directed towards achieving V_{aim}. Here, V_{aim} is set at 80% amplitude of the reference voltage vector. Figure 4.35 presents the step response of the PI controller with the tuning algorithm when the load changes from 30.5 Ω to 12.0 Ω. i_d manages to track $i_{d,ref}$ satisfactorily. The load change appears not to heavily affect the line-to-line voltage waveforms as a close imitation is seen before and after the load change. V_{ref} is able to follow V_{aim} closely even after the load change, as a result of U_{low} adjustment from an average value of 2.0 to 22.0. As expected, the rms magnitude of the output current increases from 2.014 A to 4.959 A. The current THD also improves from 3.28% to 1.87%. Figure 4.36 shows the three-phase currents.

The simulation results for the case without the tuning algorithm are provided in Figure 4.37. For this simulation, U_{low} is kept at a fixed value, namely 2.0. i_d and V_{ref} fluctuations are noticeable after the load change. As a consequence, both parameters are not able to show good tracking performance. The quality of the line-to-line voltage and output current waveforms is heavily affected as well. The load voltage THD deteriorates

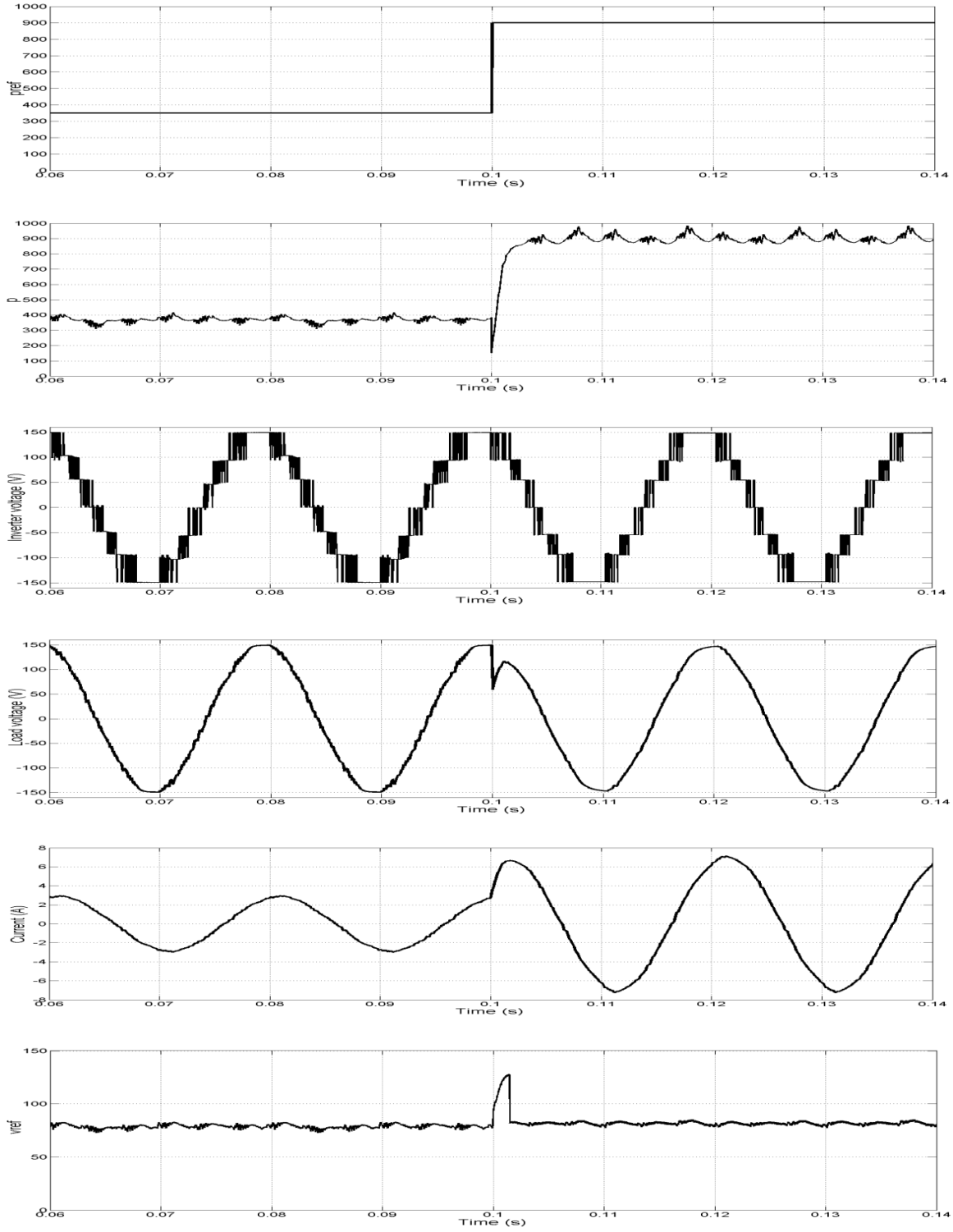


Figure 4.35: Step response as a result of a load change from 30.5 Ω to 12.0 Ω for DPC-SVM scheme with tuning algorithm, from top to bottom: p_{ref}, p, v_{AB} (inverter side), v_{ab} (load side), i_A and V_{ref}.

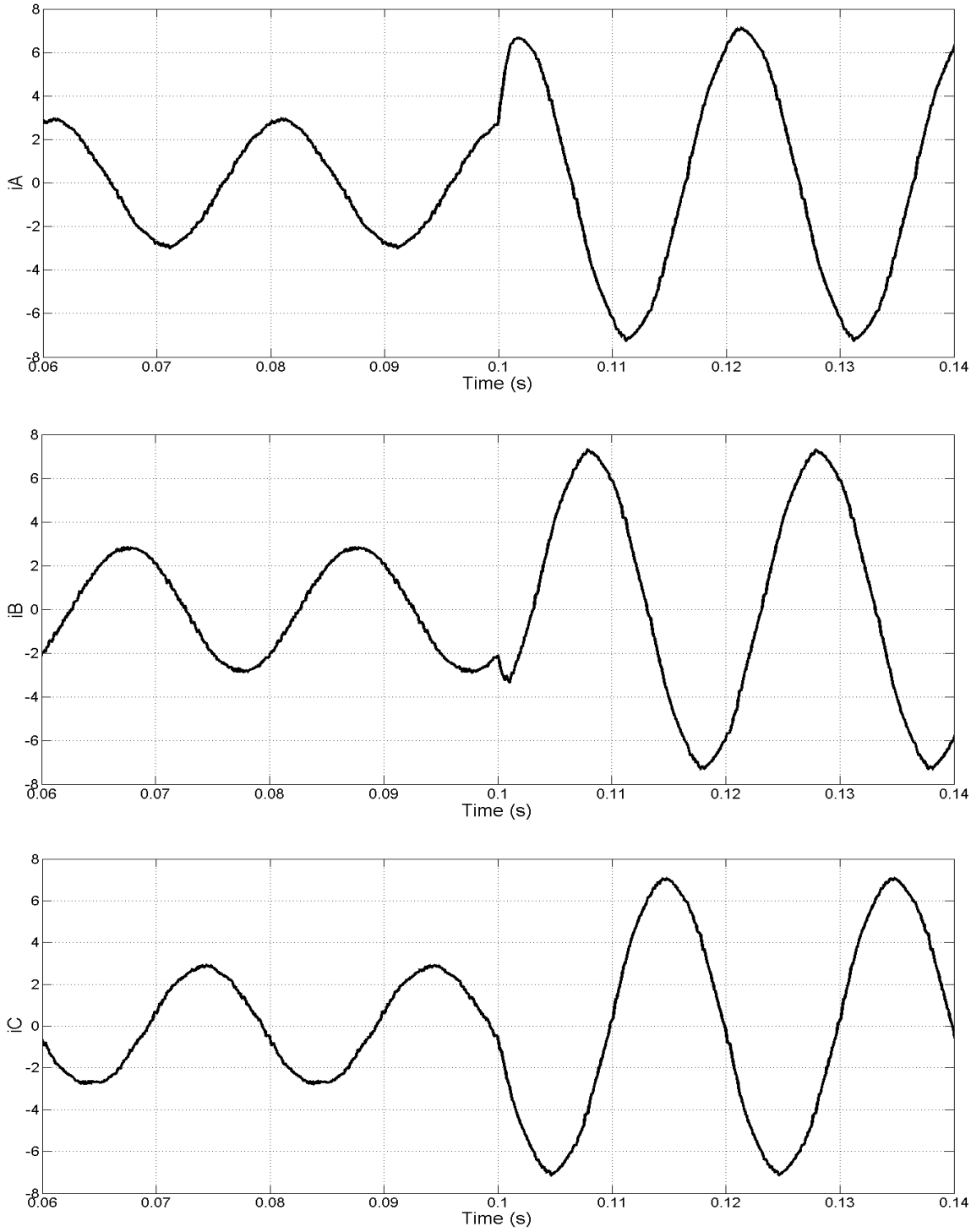


Figure 4.36: Step response as a result of a load change from 30.5 Ω to 12.0 Ω for DPC-SVM scheme with tuning algorithm, from top to bottom: i_A, i_B and i_C.

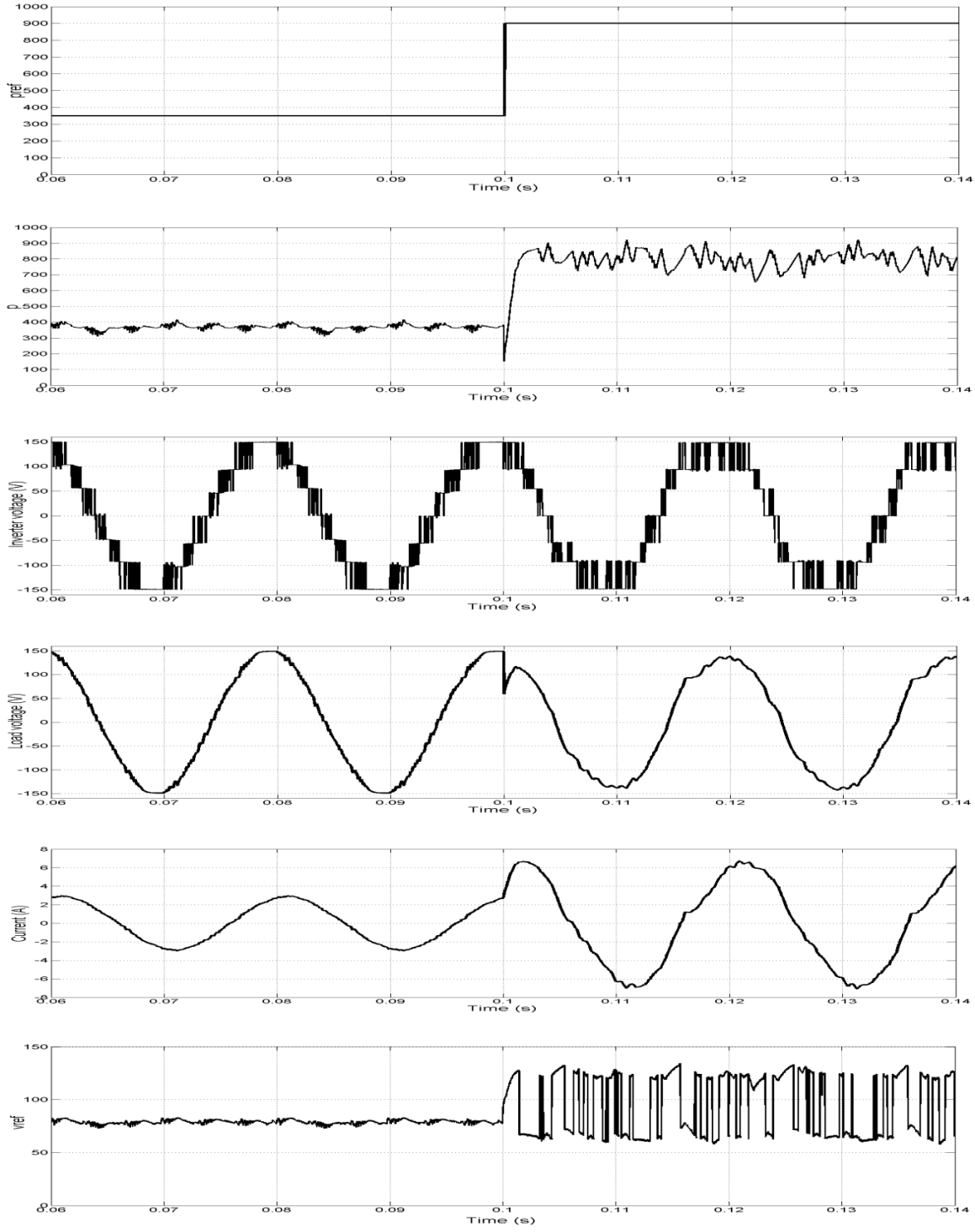


Figure 4.37: Step response as a result of a load change from 30.5 Ω to 12.0 Ω for DPC-SVM scheme without tuning algorithm, from top to bottom: p_{ref}, p, v_{AB} (inverter side), v_{ab} (load side), i_A and V_{ref}.

from 2.78% before the load change to 7.40% after the change takes place. The current THD also worsens to a value of 8.00% from the prior THD value recorded at 3.28% before the load change occurs. It can be seen that the simulation results verify the significance of the tuning algorithm in enhancing the quality of the output voltages and currents.

4.7 Summary

This chapter covers the simulation results and analysis of the proposed multilevel inverter topology with the focus on the four-level and five-level structures. MATLAB/SIMULINK has been used to carry out all simulations. The inverter's operation at low switching frequency modulation has been investigated. Further study has been conducted at high switching frequency with the proposed SVPWM method. The line-to-line output voltage waveforms and the corresponding harmonic spectra have been examined for various amplitudes of reference voltage vector. The THD and fundamental voltage performance have also been analyzed.

Power loss and efficiency analysis have also been carried out for various power factors and reference voltage vector amplitudes. Distribution of power dissipation among the semiconductor devices has been detailed. Comparison with the diode-clamped topology has been comprehensively made to have a meaningful assessment of performance and characteristics of the proposed topology. The results show that the performance of the proposed topology is comparable with that of the diode-clamped topology. In terms of power loss, the proposed topology records better performance which then leads to higher efficiency as compared to the diode-clamped topology. In addition, current control schemes based on VOC and DPC-SVM strategies with the

proposed tuning algorithm for the PI controllers have been scrutinized as well. Step response as a result of a load change has been provided with relevant comparative analysis. The tuning algorithm has been verified to be able to reduce the output current THD and for the case of the DPC-SVM scheme, it also improves the reference tracking performance.

CHAPTER 5

HARDWARE IMPLEMENTATION AND EXPERIMENTAL INVESTIGATIONS

5.1 Introduction

Testing on simulated systems does not guarantee that a complete practical implementation of the systems can be a straightforward one. In most occasions, it is always observed that the results obtained from simulated testing differ in some degree from the results of the real testing. The reason for these differences is mainly due to the ideal conditions adopted in carrying out simulations. Despite the fact that the software tool has been upgraded from time to time to include some new features that may be able to mimic the real situation in the best possible way, it is still an approximation that can never be with perfect precision and accuracy. Therefore, simulated testing is not sufficient to correctly judge that the systems can perform in the same manner as in the real environment. Simulated testing can only be regarded as the first step necessary to provide preliminary evidences in verifying unproven algorithms before it can be confidently concluded that successful actual implementation is possible.

To compensate for the weakness of the simulated testing, testing on real systems is then conducted. By doing so, the simulation results are further validated. In this work, a laboratory prototype of the proposed multilevel inverter is constructed. To implement the modulation and control algorithms, a DSP controller board eZdsp F2812 is used. The 32 bit, 150 MHz, fixed-point TMS320F2812 processor executes the algorithms to generate the relevant switching signals. Texas Instrument's Code Composer Studio (CCStudio v3.1) is used as the platform to prepare the C program codes of the algorithms.

Hardware testing is carried out for both open-loop and closed-loop systems. Testing in the open-loop system involves the implementation of the proposed multilevel inverter with the low switching frequency modulation and the proposed SVPWM. Both four-level and five-level structures are experimentally investigated. For the closed-loop system, testing is conducted for both the VOC and DPC-SVM schemes. Experimental results are obtained and analyzed for both cases of PI controller with and without the automatic tuning algorithm for each current control scheme. Comparative analysis is also done to complete the investigation. To understand how the algorithms are executed in the DSP, relevant flowcharts are provided as well.

It should be noted that power loss measurement of IGBTs and diodes is not included in this experimental work. This is because of the difficulty encountered in achieving accurate measurement of voltage, current and time spent during turn-on, turn-off and conduction duration within a sampling period. On top of that, it is an equally great challenge to correctly determine the maximum diode reverse recovery current and the time required for the current to change to zero as this happens in the range of nanosecond. Hence, to avoid from presenting incorrect results, the idea to conduct experimental tests for power loss investigation cannot be realized.

5.2 Overall Hardware Configuration

In order to test the proposed inverter experimentally, a workable hardware set-up is then prepared. It basically consists of the DC input source, the inverter prototype and the load bank. Figure 5.1 displays the complete hardware set-up used in this work. The DC sources are provided by NiMH batteries. Each battery is of 48 V, 13 Ah capacity. Depending on the number of levels of the proposed inverter, the number of batteries needed varies. For example, three batteries are required in a four-level structure while

the five-level structure uses four batteries. The use of these batteries may make the proposed multilevel inverter topology appropriate for battery-powered applications such as electric vehicles. In addition, the DC sources can also be obtained from photovoltaic modules or strings in renewable energy systems. Thus, the proposed multilevel inverter can also be useful in functioning as an interface between the renewable energy sources and the grid, for instance. The load is a variable three-phase AC load bank of RL type. The inverter prototype is constructed from two main parts namely the power circuit and the control unit. The details of the prototype are described in the next section.

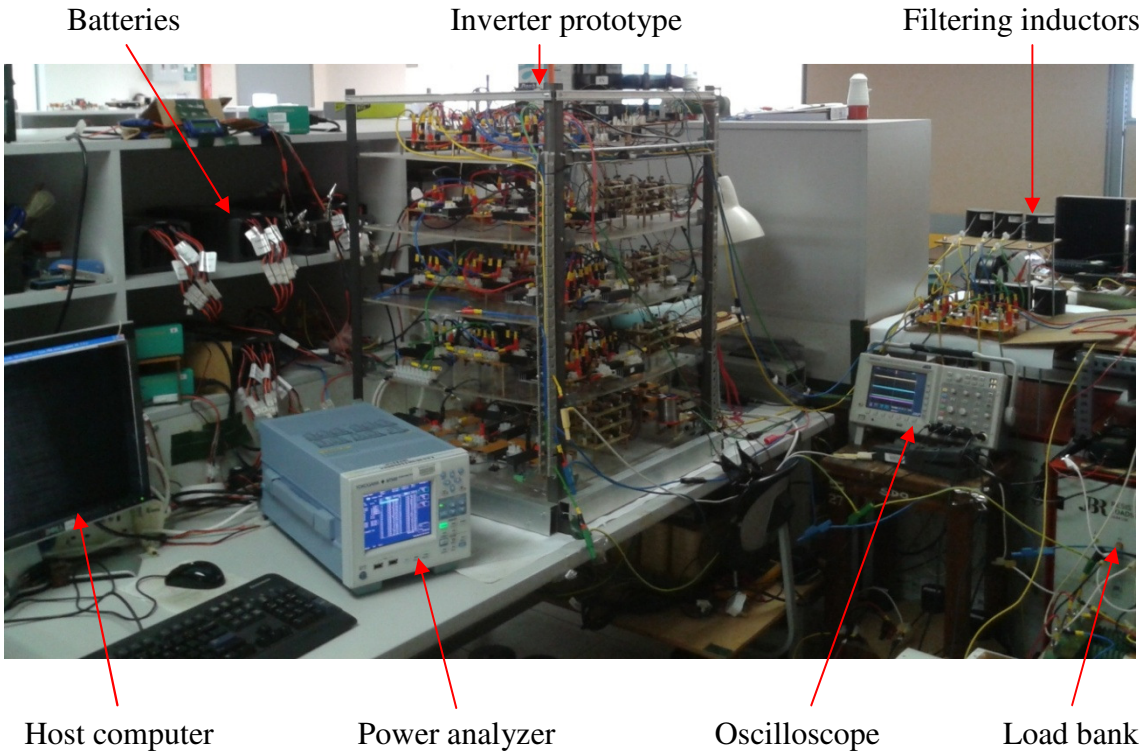


Figure 5.1: Experimental set-up for hardware implementation.

In addition to the three components that make up the hardware set-up, measuring equipment is also equally important. Tektronix TDS3054C oscilloscope is used for waveform capturing. Voltage differential probe from Tektronix of mode P5205 is used for voltage measurement. For current measurement, Fluke 80i-110s AC/DC current

probe is utilized. For THD and harmonic amplitude measurement, Yokogawa power analyzer of model WT500 is used.

5.3 Inverter Prototype

Development of the proposed inverter prototype involves two main areas namely the hardware and software parts. The hardware part is related to the construction of the power circuit of the inverter. The control of the inverter is done by the software module.

5.3.1 Power Circuit

The power circuit is built using semiconductor devices. IGBTs of model IRG4PC40UDPbF from International Rectifier with rating up to 600 V are used as the power switches. To construct a bidirectional switch, four hyperfast diodes RHRP30120 of 30 A, 1200 V rating from Fairchild Semiconductor are used with the IGBT. RC snubber is also connected across each IGBT to prevent voltage surges during turning off and to reduce electromagnetic interference. Besides the semiconductor devices, auxiliary circuits in the form of the gate drives and the dead band generators are also added to complete the power circuit. The gate drives provide isolation between the power circuit and the control unit for protection purposes, and also increase the voltage level of the switching signals to +15 V for the IGBTs to operate. The dead band generators produce the blanking time of 1 μs to ensure that the power switches are not turned on at the same time, thus avoiding a short circuit across the DC sources. To measure the voltages and currents for the control unit to use as inputs, voltage and current sensors of models LV25P and LA25-NP from LEM are used.

5.3.2 Control Unit

The control unit is represented by the controller board eZdsp^{TM} F2812 from Spectrum Digital that is based on the TMS320F2812 DSP. The DSP is a high performance 32-bit fixed-point processor from Texas Instruments with 150 MIPS operating speed. Besides the processor, the controller board is also equipped with specialized features which are suitable to develop control algorithms for real-time applications. Among those features which are useful in this work include general purpose input/output (GPIO) ports, analog-to-digital conversion (ADC) module and event manager timers.

The controller board comprises six GPIO ports known as ports A, B, D, E, F and G that can be set to function as digital inputs/outputs by clearing certain bits in the respective multiplex registers. Another register known as the direction register decides whether the GPIO pin is set to receive or transmit signals. In this work, the GPIO ports are used for three purposes. Firstly, port A is set to transmit PWM signals for the IGBTs. Secondly, ports D, E, F and G are employed to perform data transfer between two controller boards using flag signals, in which the details are provided in Section 5.6.1.3. Thirdly, port B is used to carry out digital-to-analog conversion (DAC) with the use of external low-pass filter.

ADC module is used to provide an interface between the controller board and the real signals which are analog in nature. In this work, the signals required for measurement are the three-phase voltages and currents. Using voltage and current sensors, these signals are converted into smaller electrical voltages whose magnitudes are proportional to the original signals for the ADC module to safely receive. For signal filtering to suppress undesirable noise, external low-pass filter and internal filtering

program are employed. Through the ADC module, a digital number that represents the analog signal at a particular instant is generated for use in arithmetic operation.

The DSP comprises one hardware module known as the Event Manager. It is used to deal with time-based procedures. There are two Event Managers available in which each of them has two 16-bit timers. In this work, two timers, called Timer 1 and Timer 2 of Event Manager A are utilized. Timer 1 is set to cause an interrupt service routine (ISR) for the modulation algorithm to update the PWM outputs. Timer 2 is used to initiate an ISR for the ADC module to receive and evaluate the analog signals according to the desired sampling time. An ISR is basically called when the counter value of the each timer equals a specific register value. In this work, compare and period registers are used for Timer 1 and Timer 2 respectively. The value of each register represents the time interval needed for the interrupt to occur.

For the purpose of building and debugging the program code in C language platform, a software package known as Code Composer Studio is provided. The software is supported with header files and peripheral example libraries from Texas Instruments which are useful to enable and utilize the peripherals required by setting certain bits in the related registers. To optimize the program code involving mathematical operations of floating-point numbers, IQmath library is provided. By using the functions in this library, execution speed can be shortened and high-precision calculation can be maintained. To develop the program code in the Code Composer Studio, a host computer is used. To execute the control algorithm in real time, the program code is then uploaded onto the DSP via the parallel port from the host computer.

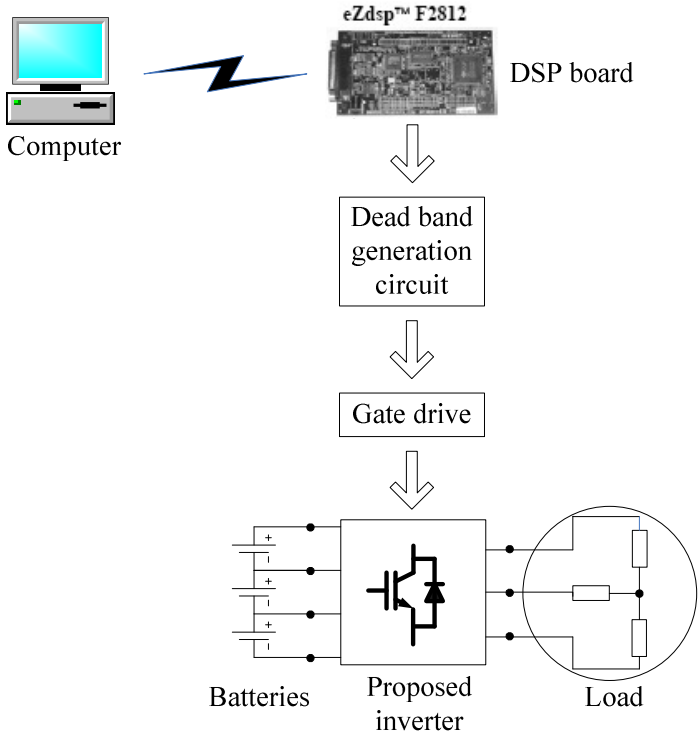


Figure 5.2: Block diagram of the experimental set-up without feedback path.

5.4 Implementation for Low Switching Frequency Modulation

To conduct experimental tests for low switching frequency modulation as to prove that the proposed inverter does operate according to the principles described in Section 3.3, the inverter prototype is tested with a three-phase, Y-connected resistive load of 30.5 Ω per phase. Both four-level and five-level structures are investigated. Figure 5.2 shows the block diagram of the experimental set-up. The four-level and five-level inverters use three and four batteries respectively as the input DC source.

5.4.1 Main Program and ISR

The program code to implement the low switching frequency modulation can be described by the flowchart shown Figure 5.3. The program is composed of two parts namely the main program and the ISR. In the main program, there are two sections called the initialization section and the infinite loop. The ISR contains the instruction set to generate the switching pulses for the IGBTs to operate.

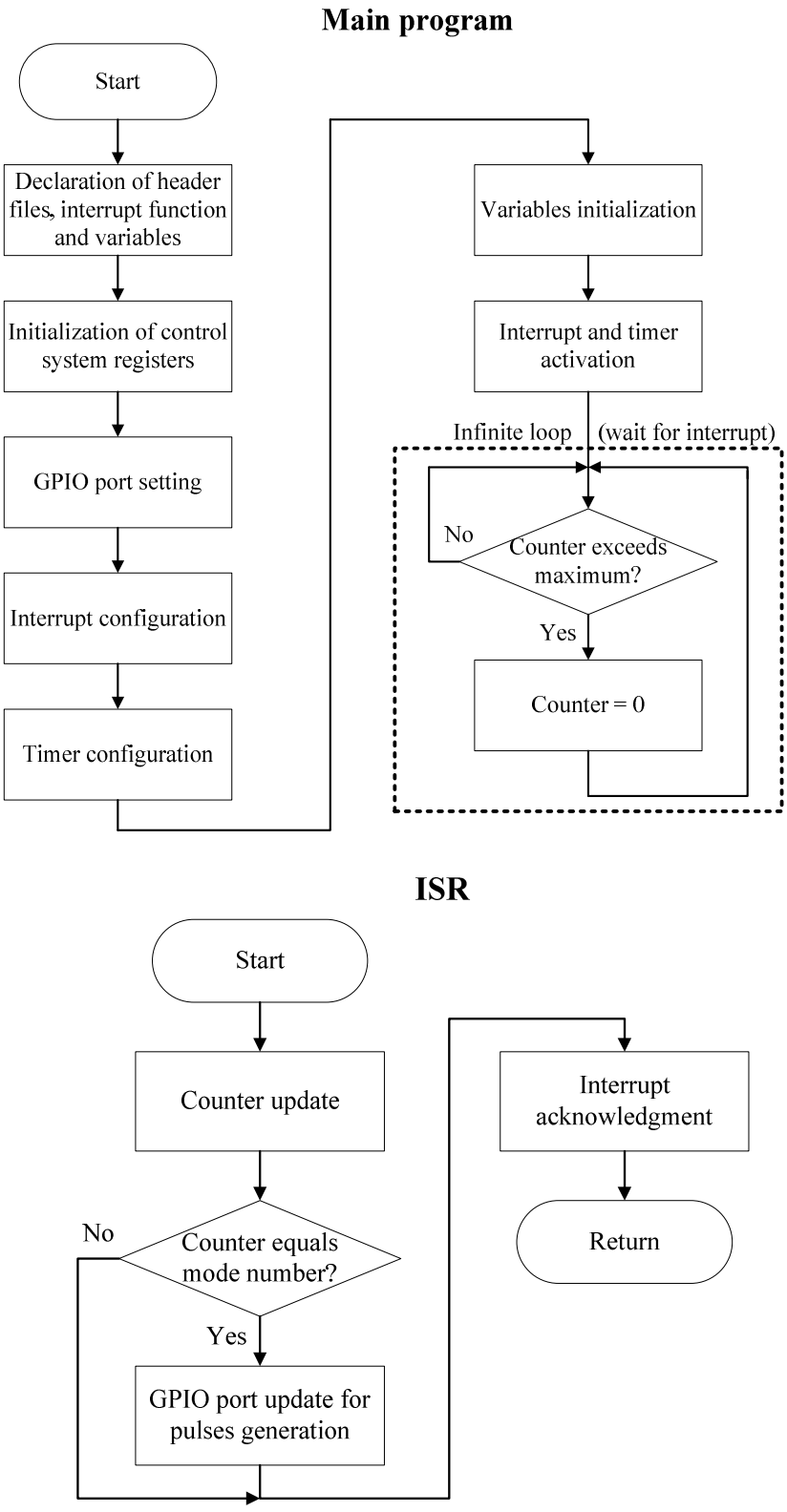


Figure 5.3: Flowchart of the program code for low switching frequency modulation.

Initialization section of the main program is meant to set the required peripherals to be ready for use. First, certain header files and libraries required to run the peripherals, the ISR function, the relevant variables needed for storing parameter values and the constants used for calculation are declared. Then, the system control registers are initialized so that the watchdog timer, the system clock and the peripheral clock are set to the proper state. GPIO port is programmed to function as digital outputs. For this implementation, bits GPIOA0 up to GPIOA11 of port A are used to generate the switching pulses for the IGBTs. Configuration for ISR trigger is based on Timer 1 of Event Manager A. Compare register is used for this purpose. The timer is set to cause an interrupt every 1.11 ms and 0.833 ms for the four-level and five-level inverters respectively. Some variables which are required to have initial values to avoid errors in computation once the program runs in real time, are also defined. The last instruction before the main program enters the infinite loop is to enable the interrupt and the corresponding timer. Besides waiting for the interrupt to occur, the infinite loop also monitors a variable known as counter. Once the counter reaches the maximum number, the counter is reset to 0. To obtain 50-Hz output waveforms from the inverter, the maximum number is defined as 18 and 24 for the four-level and five-level structures respectively.

The ISR starts by increasing the counter value by one. The counter is then compared with the mode number. The four-level inverter has mode numbers ranging from 1 to 18 since it runs with 18 modes of operation. As for the five-level inverter that consists of 24 modes of operation, the mode numbers are limited between 1 and 24. When the counter value equals a particular mode number, on-state pulses are generated for IGBTs which are supposed to be switched on during the corresponding operational mode. Before the ISR ends, interrupt acknowledgment is required as a condition

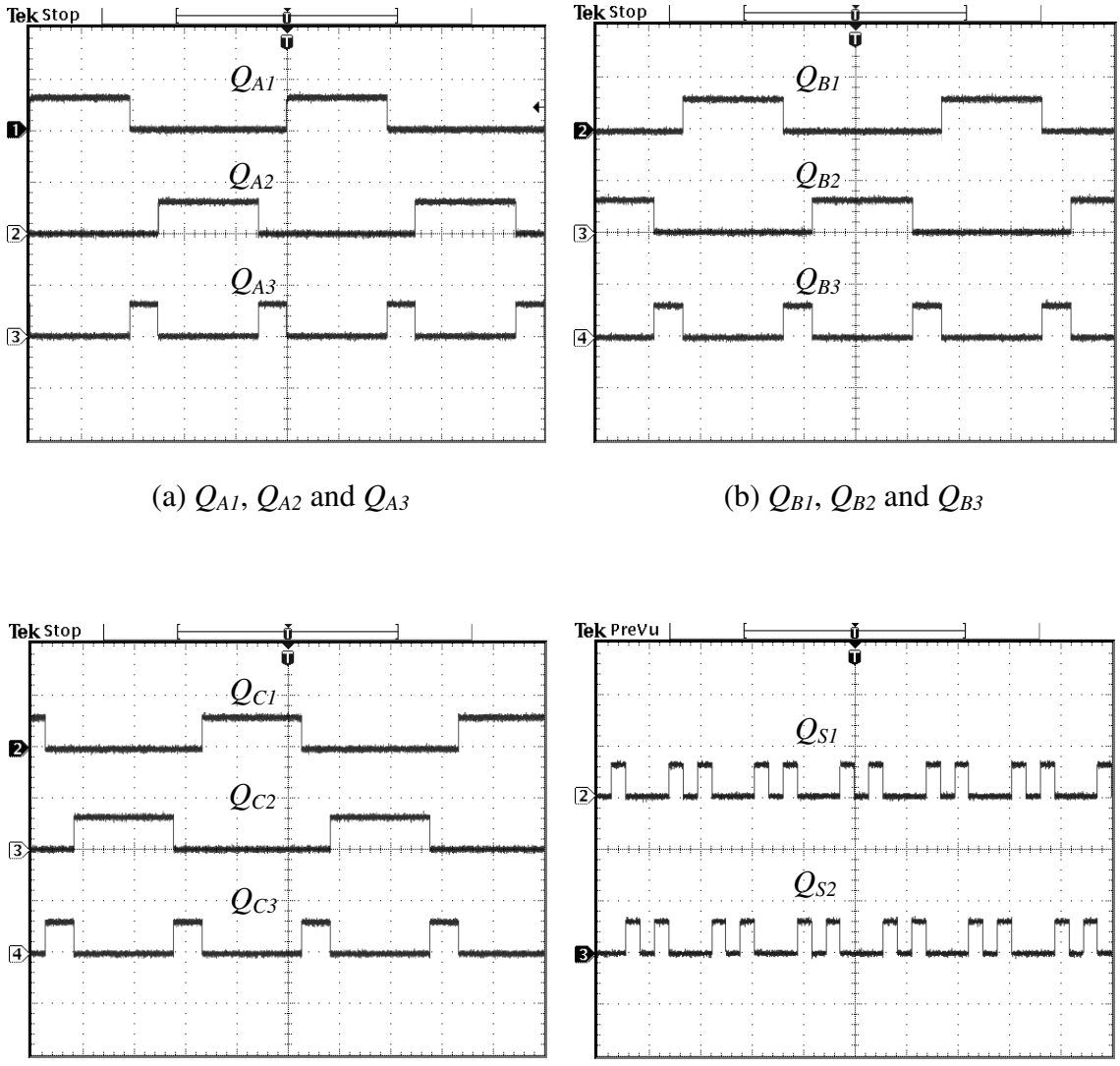
necessary for the same ISR to be called again. Once the acknowledgment is made, the execution is then transferred to the infinite loop of the main program.

5.4.2 Experimental Results for Four-Level Inverter

Figure 5.4 shows the switching pulses generated for the IGBTs. The resulting line-to-line and phase output voltage waveforms are displayed in Figures 5.5 and 5.6 respectively. It can be validated that similar to the simulation results presented in Figures 4.3, 4.4 and 4.5, the line-to-line output voltage waveforms comprises seven voltage steps. For the phase voltage waveforms, ten voltage steps are produced. The switching angles are set according to equation (4.1). Determination of optimum switching angles is not carried out as this is not considered in the scope of the work conducted.

5.4.3 Experimental Results for Five-Level Inverter

Figures 5.7, 5.8 and 5.9 portray the switching pulses, the line-to-line voltages and the phase voltages obtained from the experiment. The switching angles are defined according to equation (4.2). Nine and thirteen voltage steps are observed in the line-to-line and phase voltage waveforms respectively. These results are in line with those achieved by simulation as portrayed in Figures 4.6, 4.7 and 4.8. As mentioned earlier, optimum switching angles determination is not included in this work.



(a) Q_{A1}, Q_{A2} and Q_{A3}

(b) Q_{B1}, Q_{B2} and Q_{B3}

(c) Q_{C1}, Q_{C2} and Q_{C3}

(d) Q_{S1} and Q_{S2}

Figure 5.4: Experimental results of the switching pulses for the proposed four-level inverter

(scale: 5 V per division, 4 ms per division).

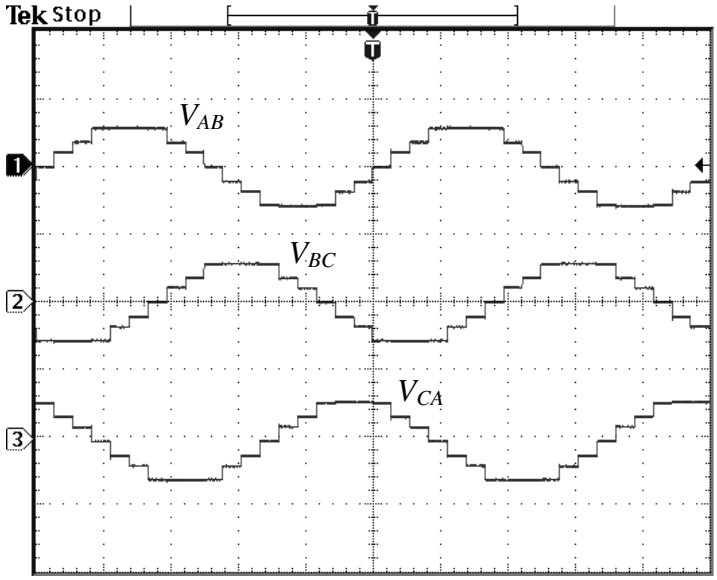


Figure 5.5: Experimental result of the line-to-line voltage waveforms for the proposed four-level inverter

(scale: 250 V per division, 4 ms per division).

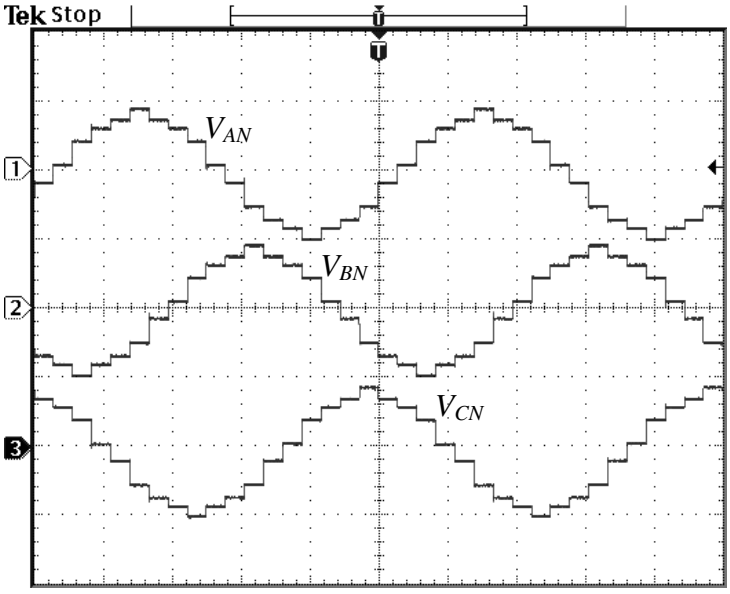
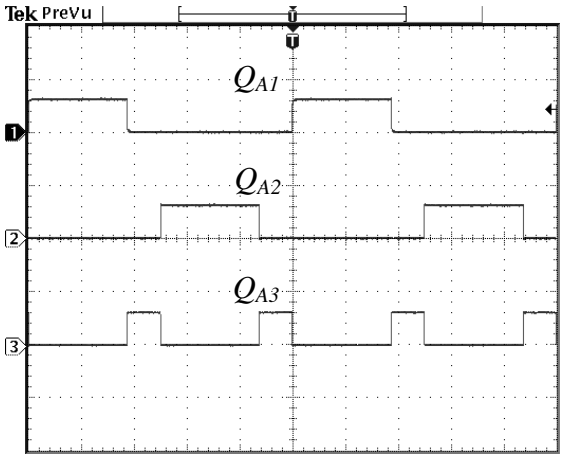
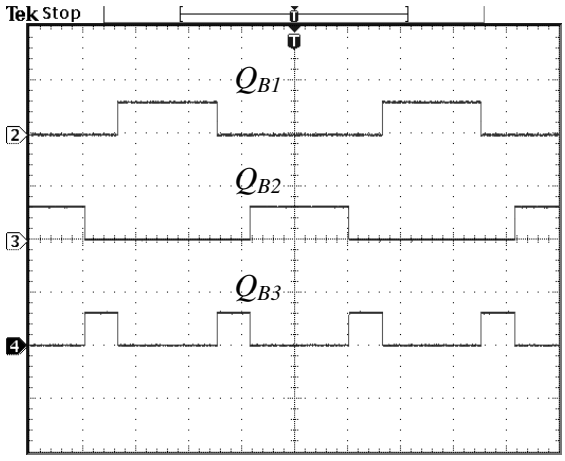


Figure 5.6: Experimental result of the phase voltage waveforms for the proposed four-level inverter

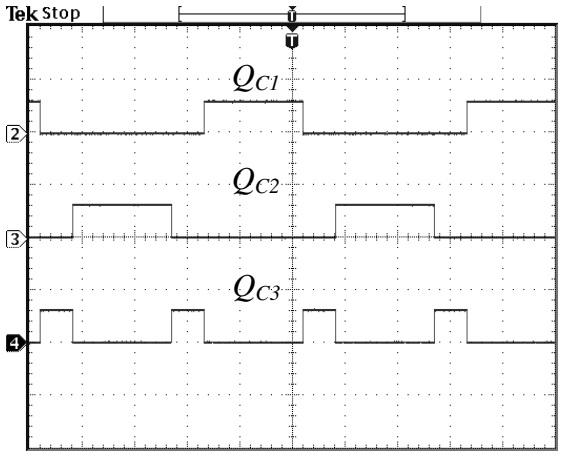
(scale: 100 V per division, 4 ms per division).



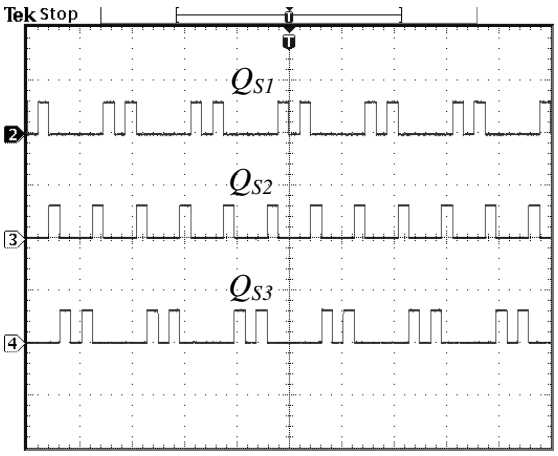
(a) Q_{A1}, Q_{A2} and Q_{A3}



(b) Q_{B1}, Q_{B2} and Q_{B3}



(c) Q_{C1}, Q_{C2} and Q_{C3}



(d) Q_{S1}, Q_{S2} and Q_{S3}

Figure 5.7: Experimental results of the switching pulses for the proposed five-level inverter

(scale: 5 V per division, 4 ms per division).

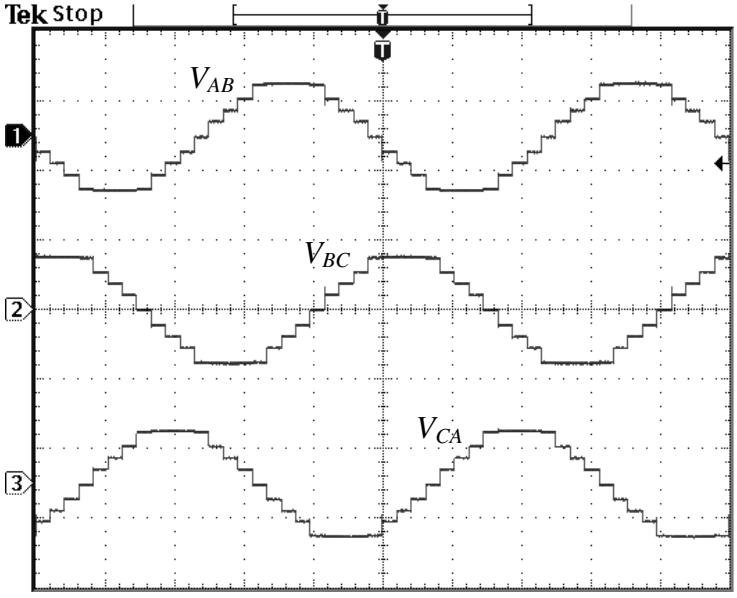


Figure 5.8: Experimental result of the line-to-line voltage waveforms for the proposed five-level inverter

(scale: 250 V per division, 4 ms per division).

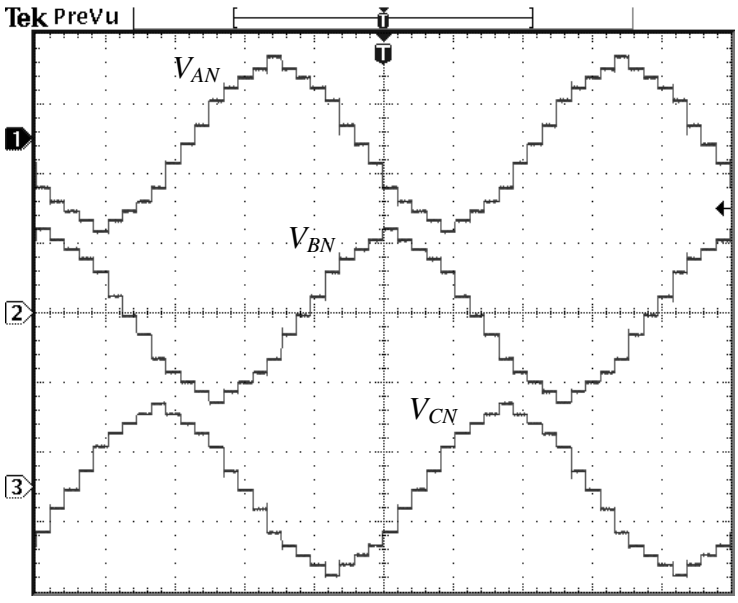


Figure 5.9: Experimental result of the phase voltage waveforms for the proposed five-level inverter

(scale: 100 V per division, 4 ms per division).

5.5. Implementation for the Novel SVPWM

Block diagram of hardware implementation of the novel SVPWM is similar to the one displayed in Figure 5.2. The inverter prototype is tested with a three-phase, Y-connected RL load of the following values: 30.5 Ω and 68 mH per phase.

5.5.1 Main Program and ISR

Similar to the program code for the low switching frequency modulation, the program code for SVPWM implementation also comprises two parts, viz, the main program and the ISR. Figure 5.10 presents the flowchart of the main program. It can be noticed that the structure of the main program is almost the same as the one previously explained. Only one additional procedure is included, namely memory allocation setting. Extra memory space is required as the on-chip memory capacity is insufficient to accommodate the entire program code. Therefore, some of the on-board memory is allocated for several program functions and the IQmath library. Proper setting of the on-board memory sections is necessary to serve for this purpose.

For this implementation, 12 bits of port A, starting from GPIOA0 until GPIOA11 are programmed to act as digital outputs. Timer 1 of Event Manager A is set to trigger the ISR every 21.74 μs for the four-level inverter and every 30.3 μs for the five-level inverter. The infinite loop monitors two counters. Counter1 is used to update the phase angle so that the computation of the on-state times of the nearest vectors can be carried out accordingly. As for Counter2, it signals the update event for PWM signals generation through port A. Counter1 has a maximum value of 46 and 33 for the four-level and five-level inverters respectively while Counter2 sets 20 as its maximum value for both inverter structures. Both counters are reset to 0 once their respective maximum value has been reached.

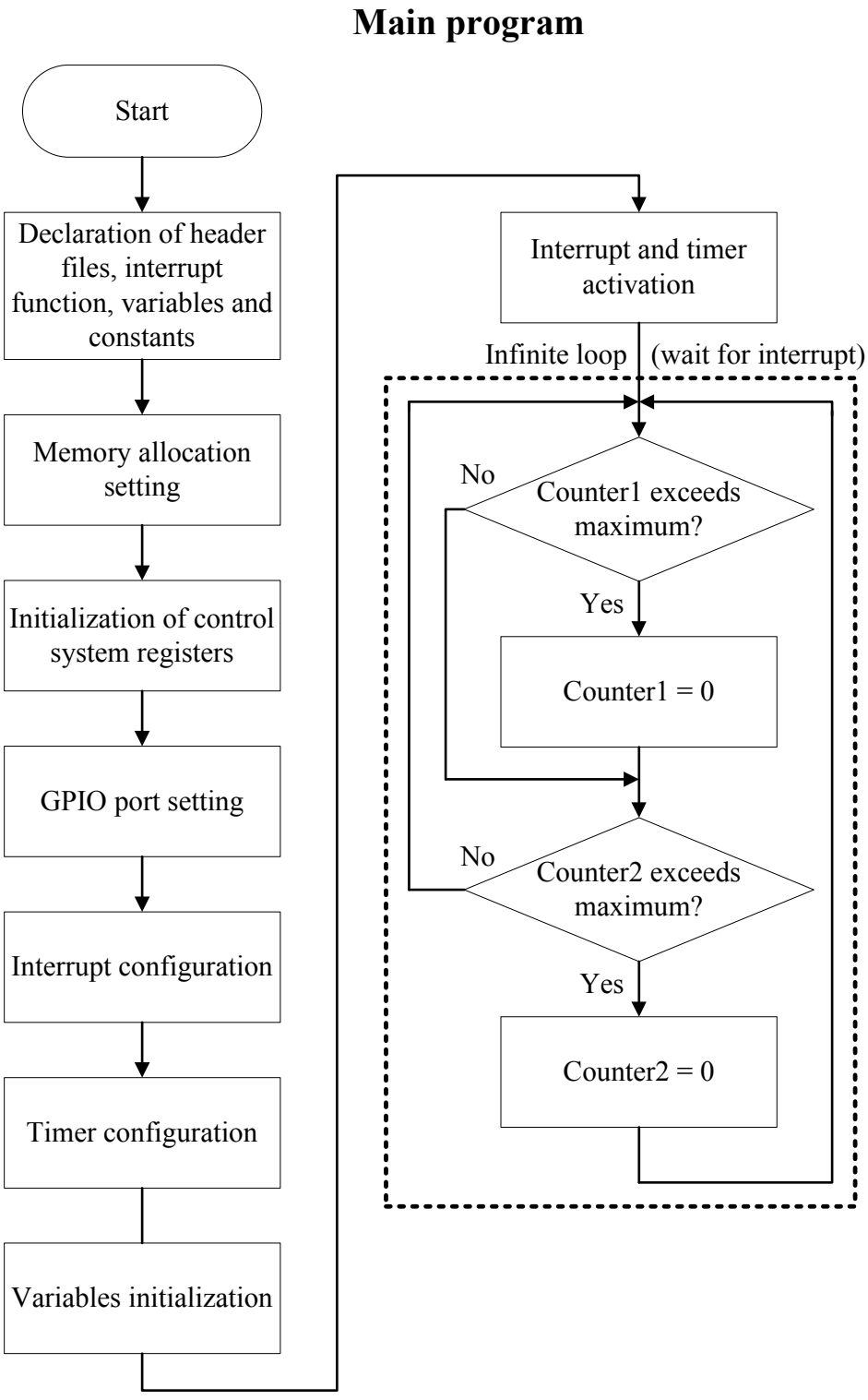


Figure 5.10: Main program for the SVPWM implementation.

The sampling frequencies for the four-level and five-level inverters are fixed at 4.6 kHz and 3.3 kHz respectively. These frequencies are chosen since they are the maximum frequencies that can be implemented by the DSP to ensure distortion-free PWM signals. Beyond these maximum frequencies, the DSP program is not able to be completely executed within the sampling period. As a result, modulation is not complete and the signals generated are distorted. For the selected sampling frequencies, each sampling period is further divided by 10 subintervals. To obtain 50-Hz output waveforms from the inverter, the number of subintervals, N_s required for the four-level and five-level inverters are given in equations (5.1) and (5.2) respectively:

$$N_{s(4-level)} = \frac{4600}{50} \times 10 = 920 \tag{5.1}$$

$$N_{s(5-level)} = \frac{3300}{50} \times 10 = 660 \tag{5.2}$$

The subinterval represents the fixed time duration for the ISR to be called periodically. In other words, N_s also reflects the number of ISR occurrence within a period of the inverter output waveforms. Therefore, the subinterval is equivalent to 21.74 μs and 30.3 μs for the four-level and five-level respectively. In respect of the counter updates, Counter1 requires 20 subintervals for an update while Counter2 is updated every subinterval. Within the subinterval, the ISR is able to complete execution nicely before it can be requested again. It can be noticed too that the subinterval for the four-level inverter is shorter than that for the five-level inverter. This is logical since the five-level inverter has more sectors and zones to consider before the correct identification is accomplished.

Figure 5.11 displays the flowchart of the ISR. The ISR starts by updating Counter2. Counter2 checking is then made to note whether its value equals 1. If Counter2 value is 1, then Counter1 is updated. Further computation is carried out to

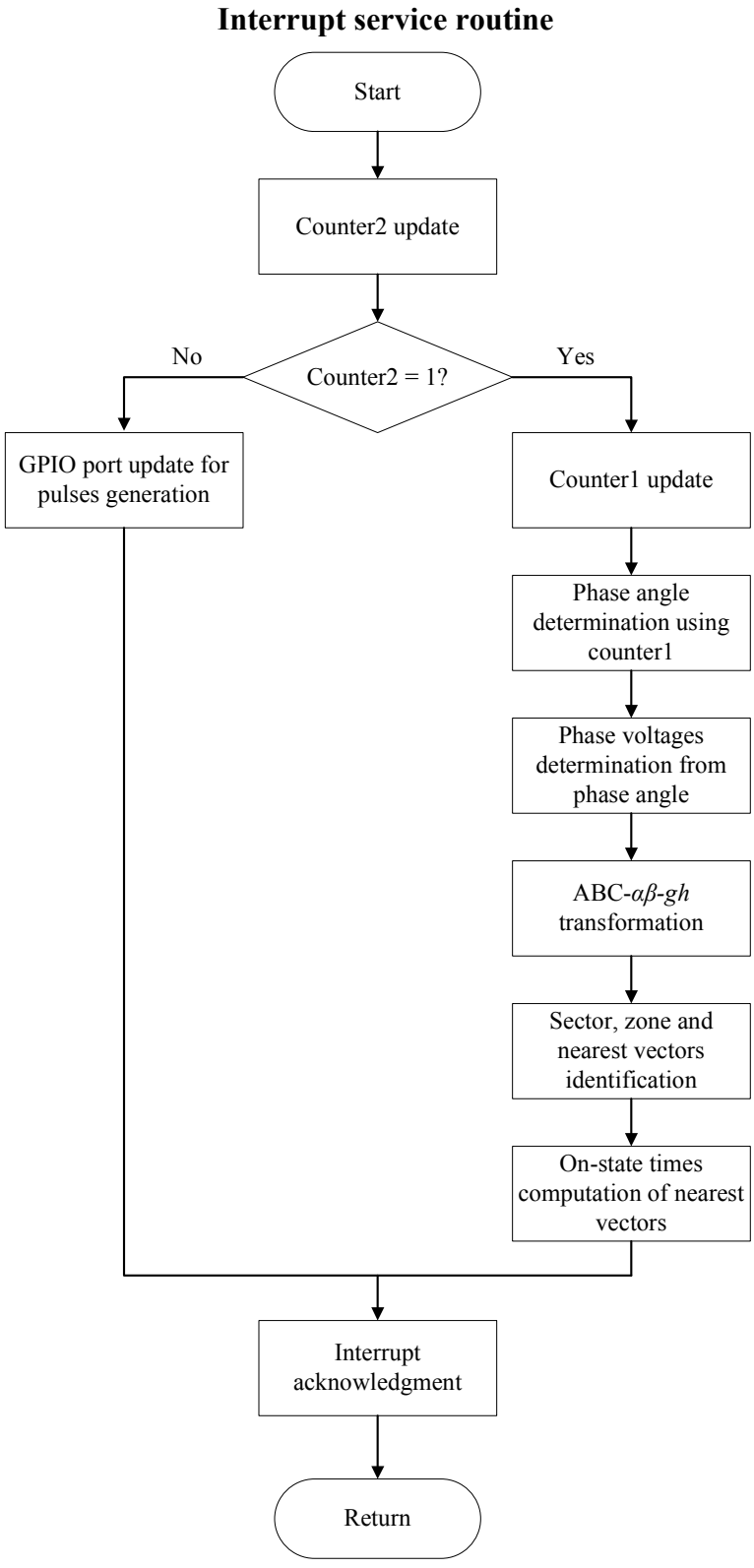


Figure 5.11: ISR for the SVPWM implementation.

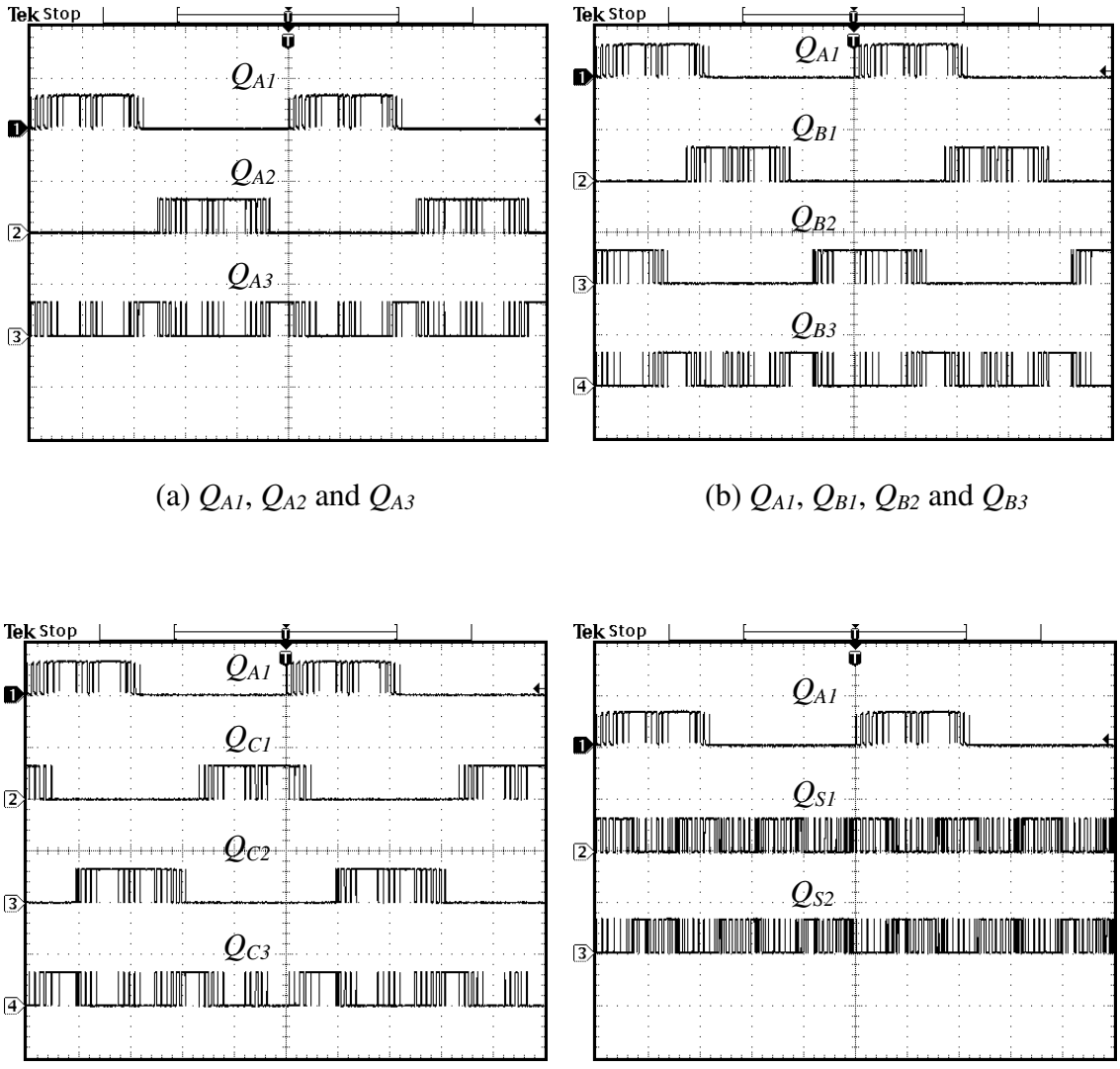
update the phase angle and subsequently, the phase voltages using equations (4.1) to (4.4). In the equations, t_1 is obtained from Counter1 value. Coordinate transformations from ABC to $\alpha\beta$ to gh frames take place using equations (3.12) and (3.16). The next processes involve identification of the sector and zone in which the reference voltage vector lies. The nearest vectors are determined and the on-state times are accordingly computed as explained in Section 3.4.5. With proper conversion, the on-state times are transformed into integer numbers between 0 and 10 as the sampling time requires 10 subintervals. Since symmetric switching state sequence is adopted in this work, two sampling times are needed to complete the sequence. Therefore, in the second sampling time, the integer numbers that represent the on-state times are set between 11 and 20.

When Counter2 has values other than 1, the integer-numbered on-state times previously determined in the most recent update, are compared with Counter2 value every time the ISR is called. Port A is updated every ISR event to produce the switching signals for the IGBTs. The patterns of the switching signals are determined by the time length of the on-state times measured using Counter2. The ISR is ended with interrupt acknowledgment before the main program takes the execution control until the ISR is called again in the next subinterval.

5.5.2 Experimental Results and Analysis for Four-Level Inverter

Figure 5.12 displays the PWM signals generated at 80% reference voltage amplitude whereby the inverter is able to generate seven voltage steps in the line-to-line voltage waveforms. To investigate the impact of variation of the reference voltage amplitude on the inverter's output voltage magnitude and quality, Figure 5.13 is then presented. It can be seen that as the reference voltage amplitude increases, the number of line-to-line voltage levels also rises. Figure 5.13(a) shows the representation of the

three-step waveforms which are obtained at 20% amplitude. The five-step waveforms displayed in Figure 5.13(b) are measured at 50% amplitude. For the seven-step waveforms that are captured at 20% amplitude, Figure 5.13(c) is presented.



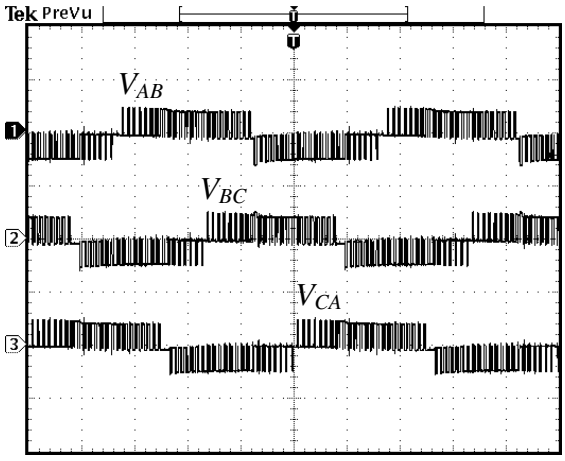
(a) Q_{A1}, Q_{A2} and Q_{A3}

(b) Q_{A1}, Q_{B1}, Q_{B2} and Q_{B3}

(c) Q_{A1}, Q_{C1}, Q_{C2} and Q_{C3}

(d) Q_{A1}, Q_{S1} and Q_{S2}

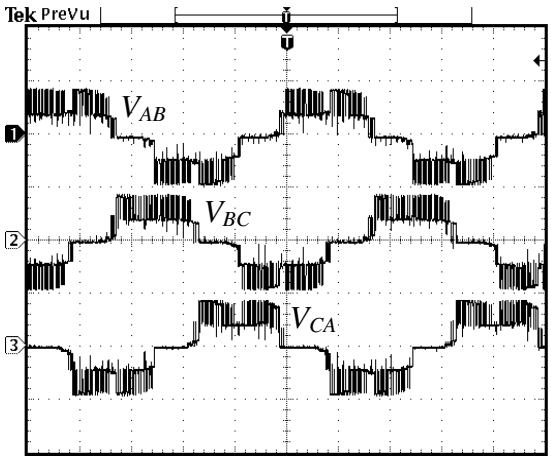
Figure 5.12: Experimental results of the PWM pulses for the proposed four-level inverter at 80% reference voltage amplitude
(scale: 5 V per division, 4 ms per division).



(a) 20% reference voltage amplitude

(scale: 100 V per division,

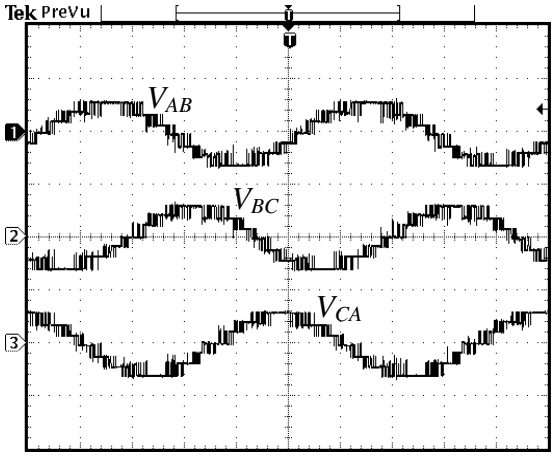
4 ms per division)



(b) 50% reference voltage amplitude

(scale: 100 V per division,

4 ms per division)



(c) 80% reference voltage amplitude

(scale: 250 V per division, 4 ms per division)

Figure 5.13: Experimental results of the line-to-line output voltage waveforms for the proposed four-level inverter.

Harmonics analysis is performed to study the effect on the THD and harmonic magnitude for the three-step, five-step and seven-step waveforms. Figure 5.14 provides the harmonic spectra of the respective line-to-line voltage waveforms. As expected, better THD performance is achieved as reference voltage amplitude increases. THD reduces from 46.86% at 20% amplitude to 33.20% at 50% amplitude. Further reduction is seen at 80% amplitude with a measurement of 10.19% THD. At 20% amplitude, low order harmonics display significant magnitudes with the highest is recorded at 14.99%. The same is observed for the 50% amplitude. The fifth harmonic in particular, records a magnitude as high as 24.13%. For 80% amplitude, all harmonic components are of magnitudes below 5% with the highest is 2.94% at the second harmonic.

The line-to-line voltage THD profile is shown in Figure 5.15. It can be seen that the profile is almost similar to its simulation counterpart portrayed in Figure 4.14. Higher THD is observed at 50% amplitude as compared to those of the 40% and 60% amplitudes, as a result of the absence of six voltage vectors of magnitude $\sqrt{3}V_{dc}$. It should be noted that the 50% amplitude reference vector has a magnitude very close to $\sqrt{3}V_{dc}$. Since the nearest vector to this reference vector has been eliminated as mentioned above and the other two nearest vectors are positioned quite far from the reference vector, the representation of the reference vector is consequently lacking in accuracy. Hence, due to this inaccurate reference vector representation, the THD at 50% amplitude records higher value. While THD indicates a significant fluctuation within a range between 40% and 60% amplitudes, the rms voltage magnitude consistently rises as the reference voltage amplitude grows to the maximum. Figure 5.16 presents the rms line-to-line voltage variation with respect to the reference voltage amplitude. The rms voltage magnitude growth pattern is observed to be comparable with the related simulation result portrayed in Figure 4.15.

PLL	I1	Or.	U1 [V]	hdf[%]	Or.	U1 [V]	hdf[%]
Freq	49.986 Hz	Tot.	26.75		dc		
		1	24.21	100.000	2	3.63	14.993
Urms1	32.46 V	3	0.15	0.618	4	2.16	8.901
Irms1	0.3431 A	5	0.98	4.065	6	0.32	1.338
P1	0.0033kW	7	1.48	6.096	8	0.57	2.359
S1	0.0111kVA	9	0.61	2.522	10	0.62	2.551
Q1	0.0106kvar	11	0.68	2.828	12	0.37	1.524
λ1	0.2960	13	0.76	3.131	14	0.50	2.072
ϕ1	G72.78 °	15	0.53	2.185	16	0.78	3.220
		17	0.56	2.301	18	0.46	1.899
Uthd1	46.863 %	19	0.65	2.693	20	0.11	0.459
Ithd1	10.677 %	21	0.38	1.585	22	0.38	1.578
Pthd1	3.257 %	23	0.23	0.954	24	0.53	2.197
		25	0.44	1.800	26	0.15	0.628
		27	0.33	1.361	28	0.22	0.892
△PAGE▽	1/5	29	0.16	0.662	30	0.58	2.396
		31	0.21	0.855	32	0.37	1.521
		33	0.84	3.484	34	0.22	0.910
		35	0.54	2.219	36	0.89	3.695
		37	0.78	3.242	38	0.67	2.750
		39	1.11	4.595	40	0.64	2.650

(a) 20% reference voltage amplitude

PLL	I1	Or.	U1 [V]	hdf[%]	Or.	U1 [V]	hdf[%]
Freq	50.030 Hz	Tot.	52.96		dc		
		1	50.25	100.000	2	1.15	2.296
Urms1	56.02 V	3	4.12	8.196	4	2.41	4.797
Irms1	0.6864 A	5	12.13	24.134	6	1.90	3.786
P1	0.0141kW	7	3.30	6.568	8	0.96	1.908
S1	0.0385kVA	9	2.25	4.469	10	1.85	3.677
Q1	0.0358kvar	11	3.60	7.157	12	1.07	2.132
λ1	0.3660	13	2.35	4.686	14	0.89	1.780
ϕ1	G68.53 °	15	0.36	0.713	16	2.04	4.054
		17	2.23	4.433	18	1.07	2.136
Uthd1	33.195 %	19	0.67	1.334	20	0.81	1.602
Ithd1	12.734 %	21	1.19	2.369	22	1.53	3.047
Pthd1	4.688 %	23	0.38	0.761	24	0.38	0.754
		25	0.57	1.139	26	0.86	1.716
		27	0.22	0.431	28	1.33	2.642
△PAGE▽	1/5	29	0.42	0.841	30	0.77	1.533
		31	0.37	0.736	32	0.58	1.158
		33	0.41	0.811	34	0.43	0.859
		35	0.99	1.967	36	0.70	1.395
		37	1.56	3.110	38	1.05	2.092
		39	1.27	2.529	40	0.83	1.642

(b) 50% reference voltage amplitude

PLL	I1	Or.	U1 [V]	hdf[%]	Or.	U1 [V]	hdf[%]
Freq	50.022 Hz	Tot.	103.38		dc		
		1	102.84	100.000	2	3.03	2.945
Urms1	105.56 V	3	2.25	2.187	4	0.16	0.160
Irms1	1.3912 A	5	2.26	2.202	6	0.85	0.824
P1	0.0527kW	7	1.81	1.763	8	1.65	1.602
S1	0.1468kVA	9	0.98	0.950	10	1.57	1.527
Q1	0.1371kvar	11	1.95	1.895	12	0.98	0.952
λ1	0.3587	13	0.43	0.418	14	1.39	1.355
ϕ1	G68.98 °	15	0.38	0.367	16	1.98	1.926
		17	1.73	1.680	18	0.28	0.269
Uthd1	10.189 %	19	1.44	1.398	20	1.01	0.983
Ithd1	2.048 %	21	0.53	0.518	22	1.12	1.087
Pthd1	0.112 %	23	1.43	1.392	24	1.05	1.025
		25	0.95	0.924	26	0.40	0.388
		27	0.93	0.908	28	0.67	0.648
△PAGE▽	1/5	29	0.35	0.341	30	1.75	1.703
		31	1.82	1.767	32	1.23	1.197
		33	0.88	0.858	34	0.33	0.322
		35	0.60	0.584	36	1.29	1.259
		37	1.14	1.112	38	1.27	1.230
		39	2.23	2.166	40	0.38	0.373

(c) 80% reference voltage amplitude

Figure 5.14: Experimental results of the line-to-line voltage harmonic spectra for the proposed four-level inverter.

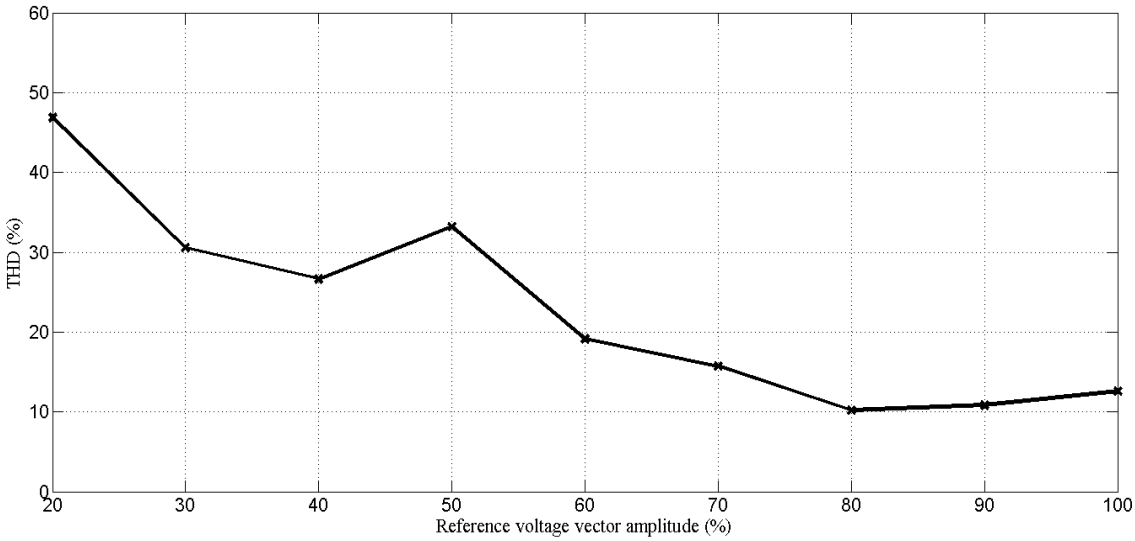


Figure 5.15: Experimental result of the line-to-line voltage THD performance of the proposed four-level inverter.

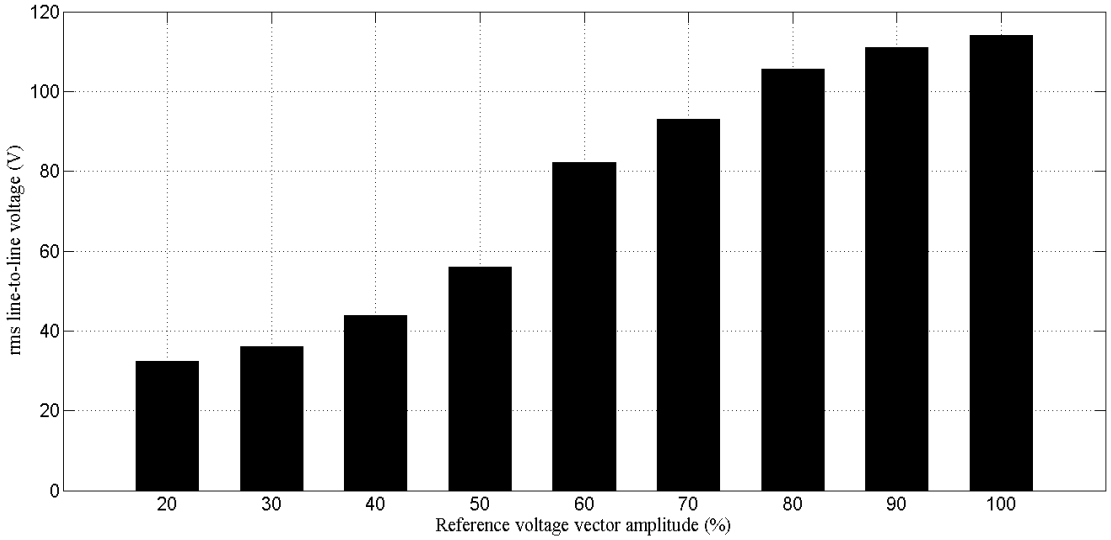
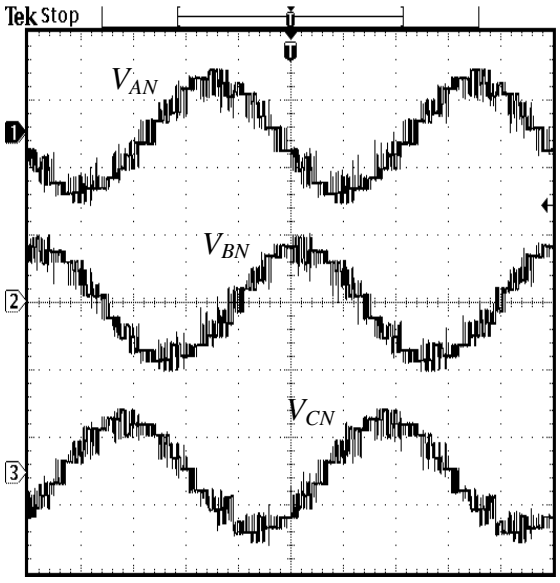


Figure 5.16: Experimental result of the rms line-to-line voltage performance of the proposed four-level inverter.

From the experimental results obtained, it is preferable to operate the four-level inverter with high reference voltage amplitude. In the analysis described previously, 80% amplitude falls in the desired amplitude range. Further investigation is then carried out to study the phase voltage and the load current characteristics at 80% amplitude. Figures 5.17 and 5.18 show the phase voltage and load current waveforms respectively. Their corresponding harmonic spectra are also portrayed in the figures. The phase voltage THD is recorded at 10.04%. Its harmonic amplitudes are all below 5%. The current THD is very low, namely 2.06%. With the exception of the 5th harmonics that show amplitude of 1%, the other current harmonics are all lower than 1%.

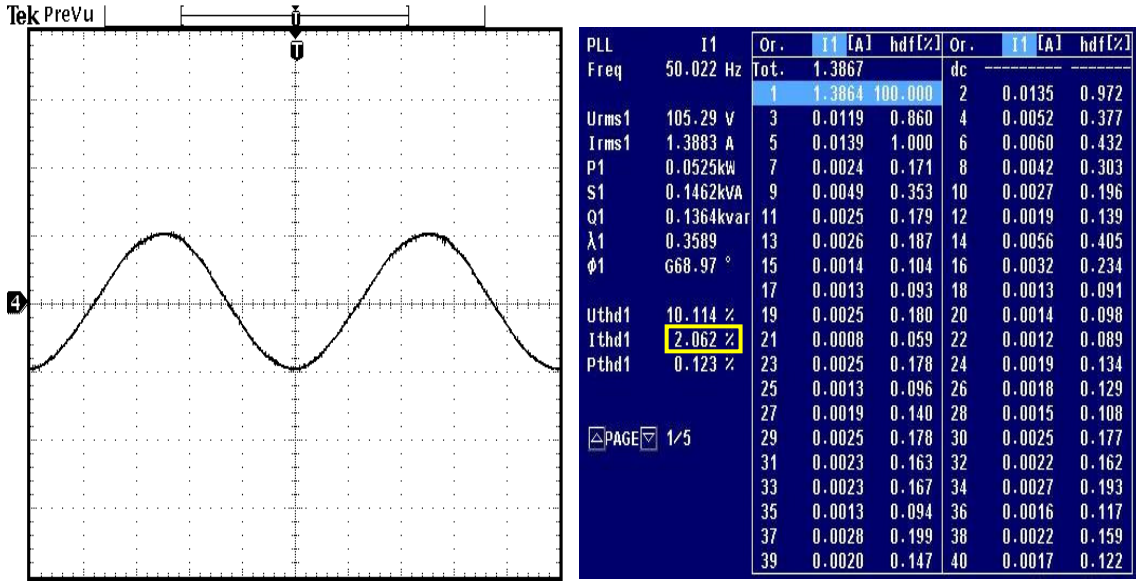


PLL	I1	Or.	U1 [V]	hdf[%]	Or.	U1 [V]	hdf[%]
Freq	50.022 Hz	Tot.	59.08		dc		
		1	58.78	100.000	2	0.76	1.286
Urms1	60.41 V	3	0.93	1.581	4	0.52	0.879
Irms1	1.3851 A	5	1.60	2.721	6	0.85	1.453
P1	0.0636kW	7	0.55	0.930	8	1.01	1.725
S1	0.0837kVA	9	1.04	1.768	10	0.85	1.448
Q1	0.0544kvar	11	0.68	1.154	12	0.57	0.971
λ1	0.7596	13	0.52	0.889	14	1.58	2.684
ϕ1	G40.57 °	15	0.27	0.459	16	1.16	1.974
		17	0.12	0.202	18	0.13	0.228
Uthd1	10.038 %	19	1.16	1.969	20	0.33	0.561
Ithd1	2.036 %	21	0.36	0.609	22	0.21	0.349
Pthd1	0.040 %	23	0.31	0.525	24	0.47	0.795
		25	0.45	0.759	26	0.41	0.695
		27	0.49	0.839	28	0.51	0.868
PAGE	1/5	29	0.60	1.019	30	1.25	2.133
		31	0.65	1.108	32	0.87	1.472
		33	0.44	0.750	34	0.29	0.497
		35	0.74	1.267	36	0.32	0.544
		37	0.43	0.732	38	0.35	0.589
		39	1.32	2.252	40	0.61	1.035

(a) Phase voltage waveforms (b) Phase voltage harmonic spectrum

(scale: 100 V per division, 4 ms per division)

Figure 5.17: Experimental results of the phase voltage waveforms and the corresponding harmonic spectrum at 80% reference voltage vector amplitude.



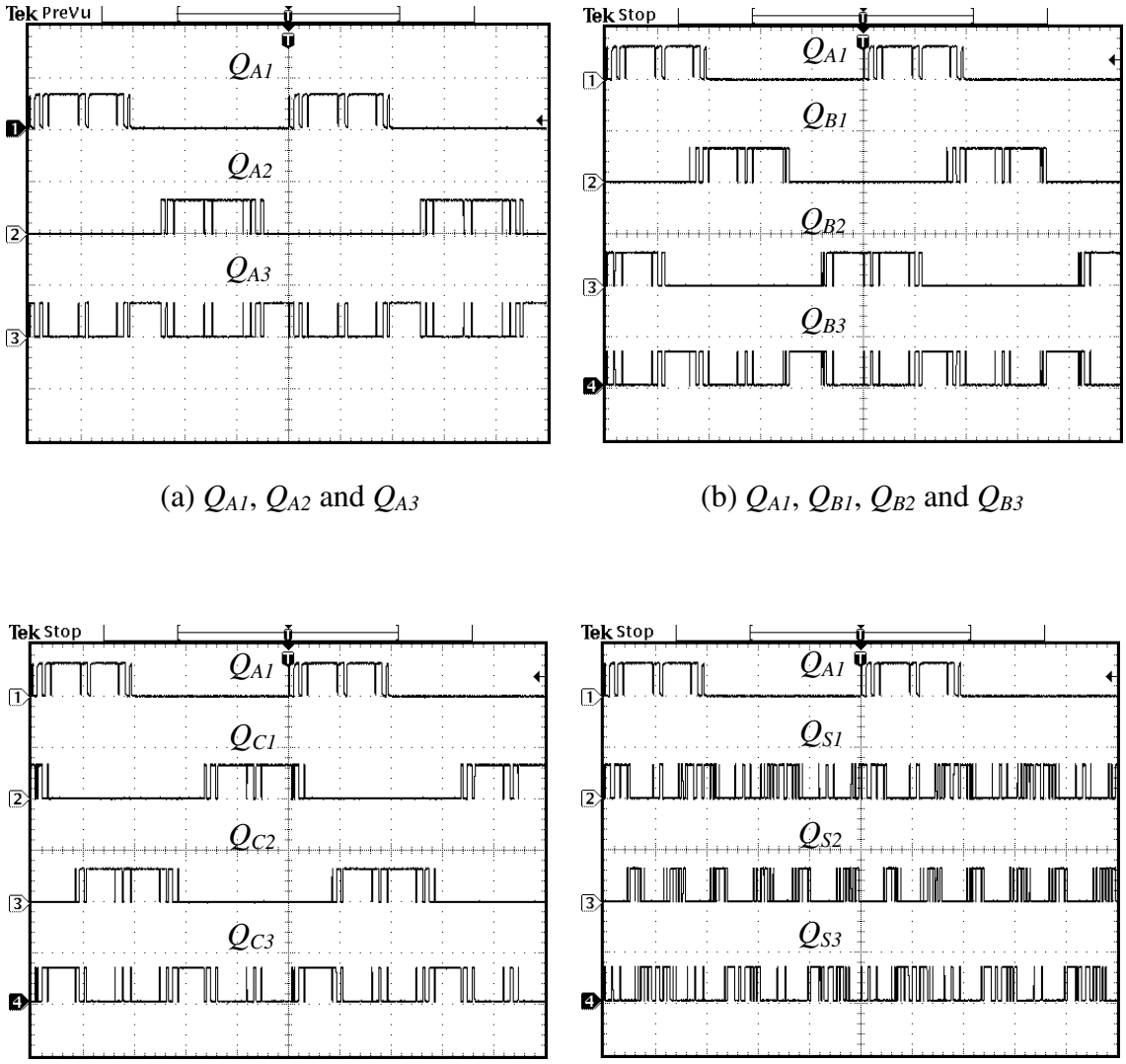
(a) Current waveform of one phase (b) Current harmonic spectrum

(scale: 2 A per division, 4 ms per division)

Figure 5.18: Experimental results of the load current waveform and the corresponding harmonic spectrum at 80% reference voltage vector amplitude.

5.5.3 Experimental Results and Analysis for Five-Level Inverter

The five-level inverter is able to generate up to nine voltage steps in the line-to-line voltage waveforms. At 90% amplitude of the reference voltage vector, the nine voltage steps can be generated with the PWM signals displayed in Figure 5.19. Besides nine-step waveforms, the inverter can also produce seven-step, five-step and three-step waveforms. Figure 5.20 displays the four waveform categories. The three-step waveforms are obtained at 20% amplitude while the five-step waveforms are measured at 40% amplitude. The seven-step and nine-step waveforms are captured at 60% and 90% amplitudes respectively.



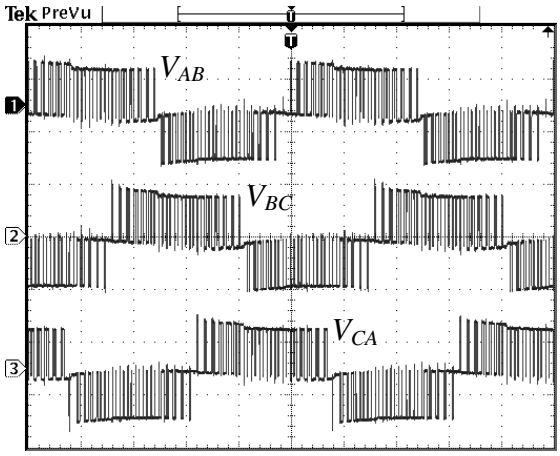
(a) Q_{A1}, Q_{A2} and Q_{A3}

(b) Q_{A1}, Q_{B1}, Q_{B2} and Q_{B3}

(c) Q_{A1}, Q_{C1}, Q_{C2} and Q_{C3}

(d) Q_{A1}, Q_{S1}, Q_{S2} and Q_{S3}

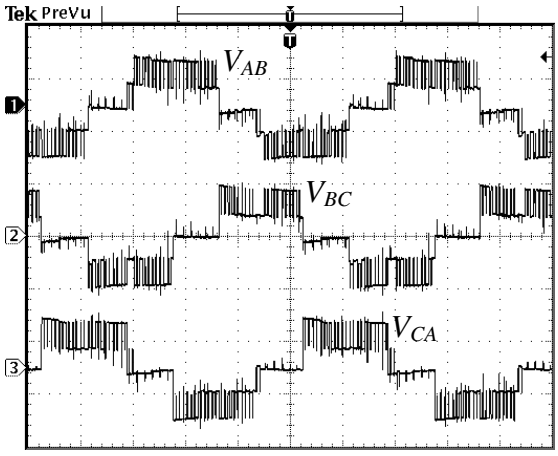
Figure 5.19: Experimental results of the PWM pulses for the proposed five-level inverter at 90% reference voltage amplitude (scale: 5 V per division, 4 ms per division).



(a) 20% reference voltage amplitude

(scale: 50 V per division,

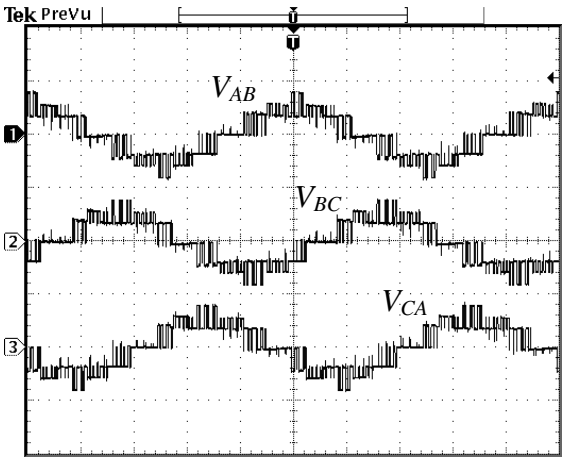
4 ms per division)



(b) 40% reference voltage amplitude

(scale: 100 V per division,

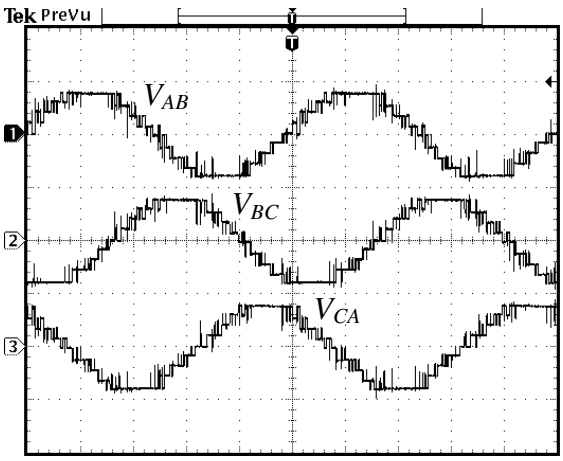
4 ms per division)



(c) 60% reference voltage amplitude

(scale: 250 V per division,

4 ms per division)



(d) 90% reference voltage amplitude

(scale: 250 V per division,

4 ms per division)

Figure 5.20: Experimental results of the line-to-line output voltage waveforms for the proposed five-level inverter.

Using power analyzer, harmonic spectra of the three-step, five-step, seven-step and nine-step waveforms are captured to carry out THD and harmonic analysis. The results are given in Figure 5.21. THD improvement is achieved as the number of steps increases. The lowest THD is 8.61% recorded for the nine-step waveforms at 90% amplitude while the highest THD indicates a value of 39.92% for the 20% amplitude that generates the three-step waveforms. In terms of harmonic magnitude, the 20% and 60% amplitudes show a significant number of harmonics of magnitude higher than 5%, namely eight and seven respectively. The highest harmonic magnitude for the case of 20% amplitude is 19.80% at 32nd harmonic. For the 60% amplitude, the 33rd harmonic records the highest value viz 10.86%. Although the 40% amplitude records four harmonics with magnitude higher than 5%, the fact that the fifth harmonic is the one with the highest magnitude (18.30%) contributes to the higher THD value as compared to the 60% amplitude. For the case of the 90% amplitude, none of the harmonics are of higher than 5% magnitude.

Line-to-line voltage THD and rms voltage magnitude profiles are also studied for a range between 20% and 100% amplitude. The results are displayed in Figures 5.22 and 5.23. It can be observed that the experimental results are comparable with the results obtained from simulation as presented in Figure 4.19 and 4.20. Noticeable fluctuation in the line-to-line voltage THD profile is seen between 40% and 60% amplitudes due to the elimination of several voltage vectors of magnitude $\sqrt{3}V_{dc}$ and $\sqrt{7}V_{dc}$. It can be noted that during this range of amplitudes, the reference vector mostly lies in the large triangle in every sector of the vector hexagon shown in Figure 3.16. As a result, the approximation of the reference vector within the large triangle is somewhat compromised with a loss of a degree of accuracy. A direct effect of this accuracy loss is the high THD observed around

the 50% amplitude of the reference vector. As for the rms voltage magnitude, the voltage rise appears to be almost linearly with respect to the reference voltage amplitude.

PLL	I1	Or.	U1 [V]	hdf[%]	Or.	U1 [V]	hdf[%]
Freq	50.029 Hz	Tot.	29.89		dc		
		1	27.75	100.000	2	1.30	4.702
Urms1	33.81 V	3	0.22	0.803	4	1.20	4.324
Irms1	0.3918 A	5	0.92	3.298	6	0.15	0.531
P1	0.0043kW	7	1.25	4.509	8	0.24	0.874
S1	0.0132kVA	9	0.34	1.224	10	1.12	4.024
Q1	-0.0125kvar	11	0.21	0.751	12	0.19	0.685
λ1	0.3253	13	0.59	2.131	14	0.71	2.546
φ1	D71.01 °	15	0.26	0.928	16	0.44	1.600
		17	0.42	1.509	18	0.31	1.118
Uthd1	39.916 %	19	0.20	0.733	20	0.39	1.414
Ithd1	4.867 %	21	0.61	2.197	22	0.23	0.829
Pthd1	0.729 %	23	0.44	1.581	24	0.74	2.659
		25	0.45	1.629	26	0.47	1.708
		27	1.03	3.697	28	0.78	2.816
PAGE	1/5	29	1.33	4.778	30	3.61	13.018
		31	1.66	5.984	32	5.49	19.800
		33	1.93	6.952	34	1.04	3.735
		35	3.06	11.033	36	4.82	17.368
		37	1.67	6.000	38	4.49	16.174
		39	0.79	2.852	40	0.33	1.174

(a) 20% reference voltage amplitude

PLL	I1	Or.	U1 [V]	hdf[%]	Or.	U1 [V]	hdf[%]
Freq	50.014 Hz	Tot.	58.69		dc		
		1	56.71	100.000	2	0.44	0.770
Urms1	61.63 V	3	4.23	7.453	4	0.35	0.611
Irms1	0.7612 A	5	10.38	18.297	6	0.28	0.491
P1	0.0191kW	7	4.54	8.011	8	0.40	0.703
S1	0.0469kVA	9	2.67	4.705	10	0.23	0.408
Q1	-0.0428kvar	11	2.43	4.286	12	0.27	0.474
λ1	0.4074	13	2.62	4.613	14	0.47	0.838
φ1	D65.96 °	15	2.84	5.009	16	0.54	0.956
		17	2.07	3.642	18	0.51	0.901
Uthd1	26.566 %	19	1.52	2.680	20	0.33	0.586
Ithd1	10.083 %	21	1.00	1.767	22	0.25	0.444
Pthd1	3.066 %	23	1.13	1.999	24	0.18	0.317
		25	1.88	3.313	26	0.30	0.530
		27	3.60	6.342	28	0.44	0.770
PAGE	1/5	29	1.06	1.871	30	0.40	0.708
		31	0.35	0.616	32	0.34	0.605
		33	2.10	3.696	34	0.34	0.592
		35	2.69	4.742	36	0.55	0.962
		37	0.84	1.484	38	0.35	0.617
		39	1.42	2.509	40	0.30	0.532

(b) 40% reference voltage amplitude

PLL	I1	Or.	U1 [V]	hdf[%]	Or.	U1 [V]	hdf[%]
Freq	50.002 Hz	Tot.	93.16		dc		
		1	90.56	100.000	2	0.40	0.441
Urms1	98.01 V	3	3.68	4.069	4	1.04	1.147
Irms1	1.2410 A	5	5.26	5.806	6	0.98	1.083
P1	0.0405kW	7	4.07	4.498	8	1.28	1.409
S1	0.1216kVA	9	2.37	2.622	10	0.45	0.497
Q1	-0.1147kvar	11	6.40	7.072	12	0.78	0.866
λ1	0.3328	13	1.20	1.321	14	2.86	3.160
φ1	D70.56 °	15	1.57	1.739	16	0.98	1.082
		17	0.45	0.502	18	1.97	2.173
Uthd1	24.068 %	19	1.19	1.313	20	1.71	1.887
Ithd1	4.464 %	21	2.03	2.241	22	1.78	1.963
Pthd1	0.543 %	23	5.15	5.686	24	2.80	3.094
		25	1.09	1.209	26	0.78	0.858
		27	3.07	3.385	28	1.54	1.697
PAGE	1/5	29	5.48	6.053	30	3.89	4.294
		31	1.52	1.680	32	1.84	2.030
		33	9.84	10.862	34	1.60	1.767
		35	6.03	6.654	36	4.16	4.596
		37	1.63	1.802	38	2.36	2.606
		39	6.63	7.316	40	1.62	1.793

(c) 60% reference voltage amplitude

PLL	I1	Or.	U1 [V]	hdf[%]	Or.	U1 [V]	hdf[%]
Freq	50.029 Hz	Tot.	142.86		dc		
		1	142.33	100.000	2	2.13	1.498
Urms1	144.43 V	3	1.31	0.922	4	0.73	0.516
Irms1	1.9039 A	5	4.71	3.312	6	0.70	0.492
P1	0.0963kW	7	2.24	1.576	8	1.83	1.285
S1	0.2750kVA	9	0.79	0.552	10	1.07	0.751
Q1	0.2576kvar	11	0.82	0.578	12	1.96	1.378
λ1	0.3501	13	0.66	0.464	14	1.65	1.161
φ1	G69.51 °	15	0.78	0.551	16	1.82	1.282
		17	0.90	0.636	18	0.83	0.584
Uthd1	8.612 %	19	0.49	0.342	20	0.85	0.596
Ithd1	1.878 %	21	0.58	0.407	22	2.04	1.433
Pthd1	0.109 %	23	0.21	0.146	24	1.30	0.916
		25	0.65	0.454	26	2.84	1.997
		27	1.34	0.941	28	0.76	0.532
PAGE	1/5	29	0.38	0.266	30	1.31	0.918
		31	0.21	0.147	32	3.69	2.592
		33	3.73	2.620	34	1.72	1.208
		35	4.92	3.458	36	1.80	1.268
		37	1.39	0.976	38	1.38	0.972
		39	0.81	0.572	40	0.21	0.148

(d) 90% reference voltage amplitude

Figure 5.21: Experimental results of the line-to-line voltage harmonic spectra for the proposed five-level inverter.

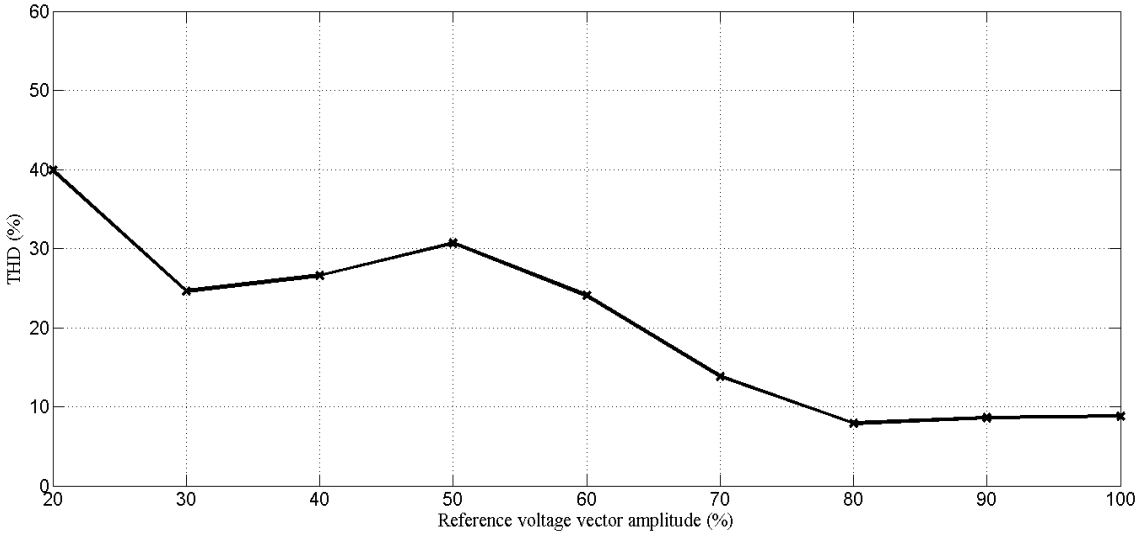


Figure 5.22: Experimental result of the line-to-line voltage THD performance of the proposed five-level inverter.

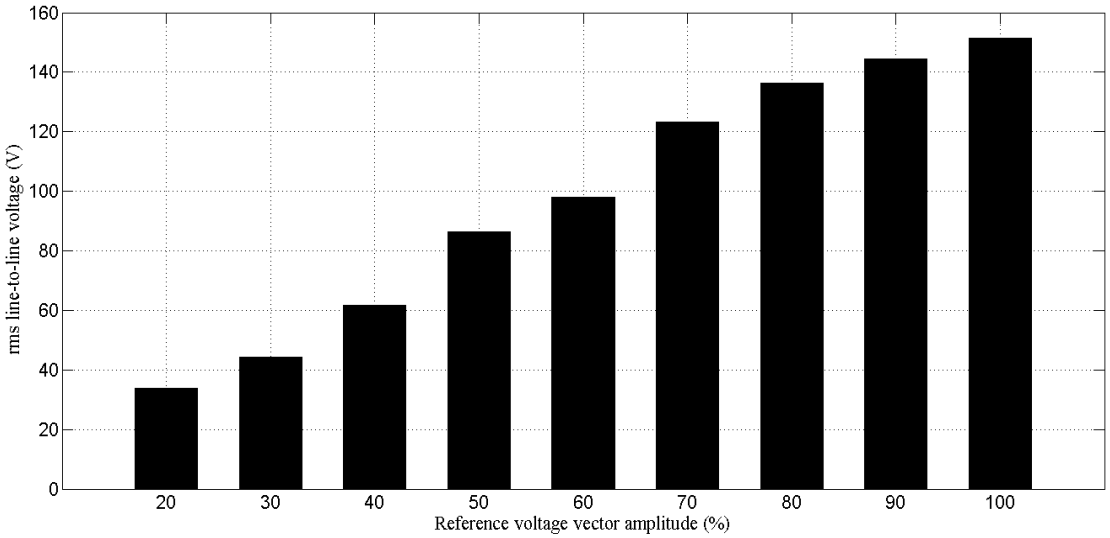
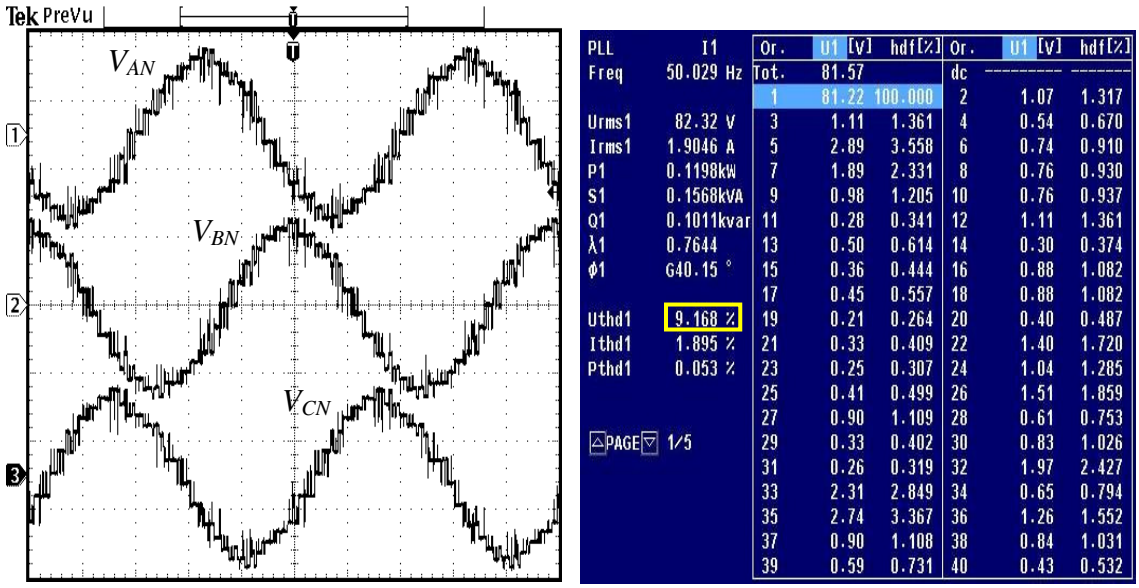


Figure 5.23: Experimental result of the rms line-to-line voltage performance of the proposed five-level inverter.

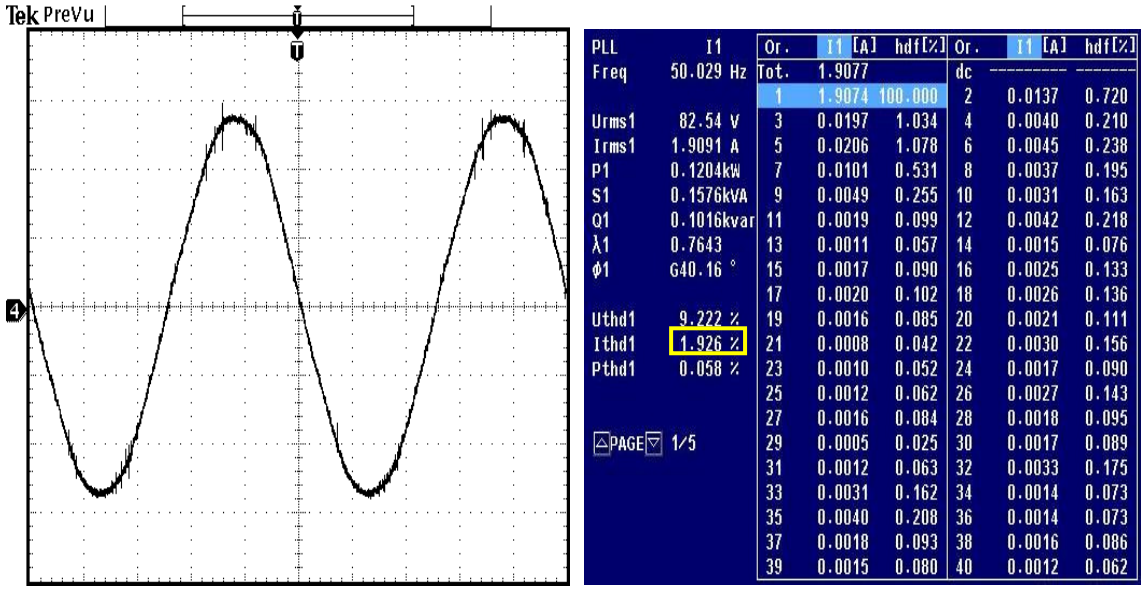
Considering line-to-line voltage THD and harmonic performance, it is obvious that the optimum operating point of the inverter can be achieved when it runs at high reference voltage amplitude such as 90% amplitude. Besides the line-to-line voltages, characteristics of the phase voltages and the load currents at such amplitude are also of interest. The phase voltage waveforms and the corresponding harmonic spectrum are shown in Figure 5.24. Figure 5.25 displays those for the load currents. The phase voltage THD indicates a value of 9.17%. The harmonic amplitudes are all below 5%. The current THD is recorded at 1.93%. With the exception of 3rd and 5th harmonics that show amplitudes of around 1%, the other current harmonics are all very low, namely below 1%.



(a) Phase voltage waveforms (b) Phase voltage harmonic spectrum

(scale: 100 V per division, 4 ms per division)

Figure 5.24: Experimental results of the phase voltage waveforms and the corresponding harmonic spectrum at 90% reference voltage vector amplitude.



(a) Current waveform of one phase (scale: 1 A per division, 4 ms per division)

(b) Current harmonic spectrum

Figure 5.25: Experimental results of the load current waveform and the corresponding harmonic spectrum at 90% reference voltage vector amplitude.

5.6 Implementation for Current Control Scheme

The block diagram of the experimental set-up is portrayed in Figure 5.26. The experimental test is conducted on the four-level inverter of the proposed topology. A three-phase, Y-connected variable RL load is used. Filtering inductors of 10 mH per phase are also placed between the inverter prototype and the load. The use of voltage and current sensors reflect the feedback path in the system. The control unit consists of two DSP boards which act as the modulator and the controller. The reason to use two DSP boards is to separate the program code for the SVPWM algorithm from the code that executes ADC results reading, parameter transformation between $\alpha\beta$ and dq frames and PI controller functions. By doing so, long program code that leads to the reduction of the program execution speed, thus causes slow responses, can be avoided if one DSP

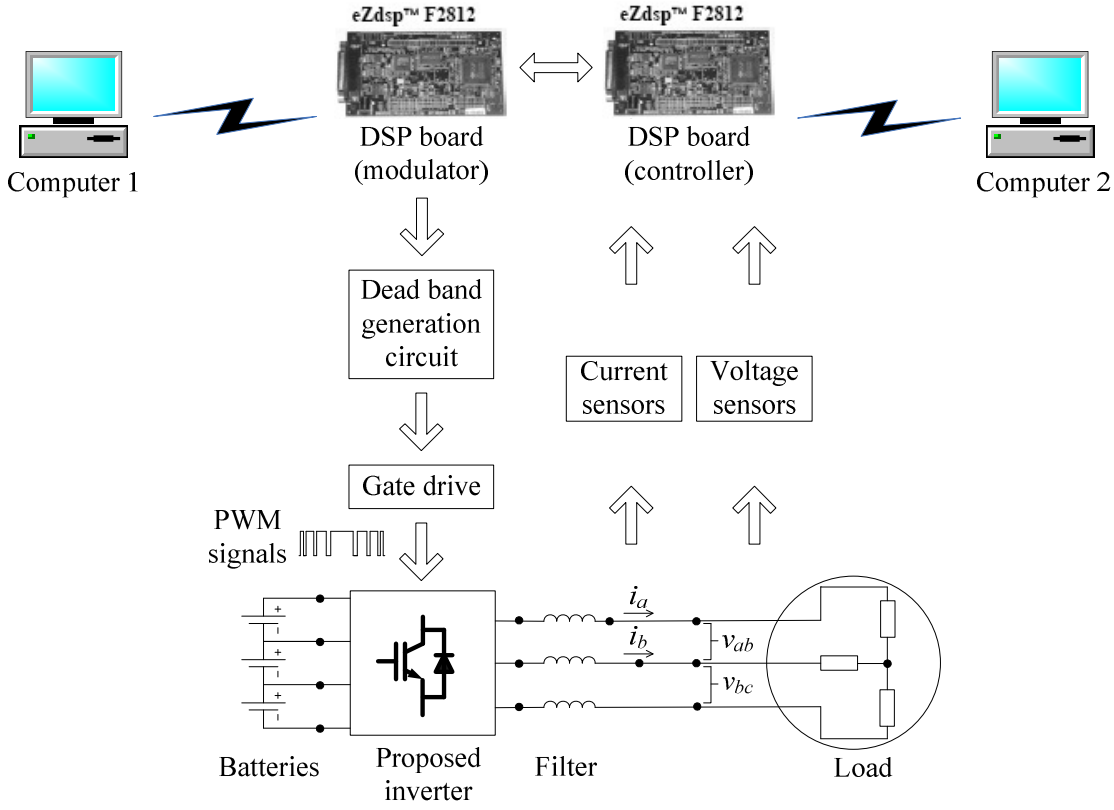


Figure 5.26: Block diagram of the experimental set-up with feedback path.

board is to be used. To facilitate the programming for the two boards, two host computers are then used.

5.6.1 Main Program and ISR

Two program codes are prepared for the DSP-based modulator and controller. Each program uses ISR. The modulator's ISR basically updates the PWM pulses generation while the controller's ISR periodically reads ADC results and provides inputs to the modulator. A simple data communication interface is developed between the modulator and the controller based on flag signalling approach.

5.6.1.1 Modulator

The program code of the modulator consists of the main program and the ISR. The flowchart describing the main program is provided in Figure 5.27. Initialization section of the main program is quite similar to the one explained for the SVPWM implementation in Section 5.5.1 except in some areas whereby certain modifications are needed to accommodate data transfer between the modulator and the controller. Five GPIO ports are used in this implementation. Bits GPIOA0 to GPIOA10 of port A are configured as digital outputs for IGBTs' control signals generation. Port F, starting from bits GPIOF0 to GPIOF14, is set to receive data from the controller. Two bits of port G, namely GPIOG4 and GPIOG5 are also set as digital inputs for data reception. Other two bits from port E, namely GPIOE0 and GPIOE1 are programmed to receive flag signals while bits GPIOD0 and GPIOD1 of port D are used to transmit flag signals. Timer 1 of Event Manager A is also utilized to initiate ISR every 20.41 μs.

As for the infinite loop, instead of monitoring counters as in the previous implementation, it is used to monitor the data received from the controller. There are three data involved in the transfer namely V_{ref}, θ_{ref} and an update signal. Recall that V_{ref} and θ_{ref} are defined according to equations (3.15) and (3.16) respectively. The transfer of data is basically done through the use of flag signals in which the details are provided in Section 5.6.1.3. Once the data are received, they are then stored in three different variables which can be accessed by the ISR.

Figure 5.28 portrays the flowchart of the ISR. When the ISR is requested, the first instruction executed is to update the counter. The counter has a maximum value of 20. If this maximum value is exceeded, the counter is then reset to 0. In order to reach the maximum value, the counter requires two sampling time. Since the counter is

updated every 20.41 μs, the sampling time is then set at 204.1 μs which next leads to a sampling frequency of 4.9 kHz. Every time the counter value becomes 1, the update signal is checked whether new data of V_{ref} and θ_{ref} are available. If no new data present, the existing value of V_{ref} is used to compute the on-state times. θ_{ref} continues to change from its previous value at a rate of 0.12823 rad every time the counter value turns to 1. Once θ_{ref} exceeds π rad, the value is immediately switched to -π rad. If new data are

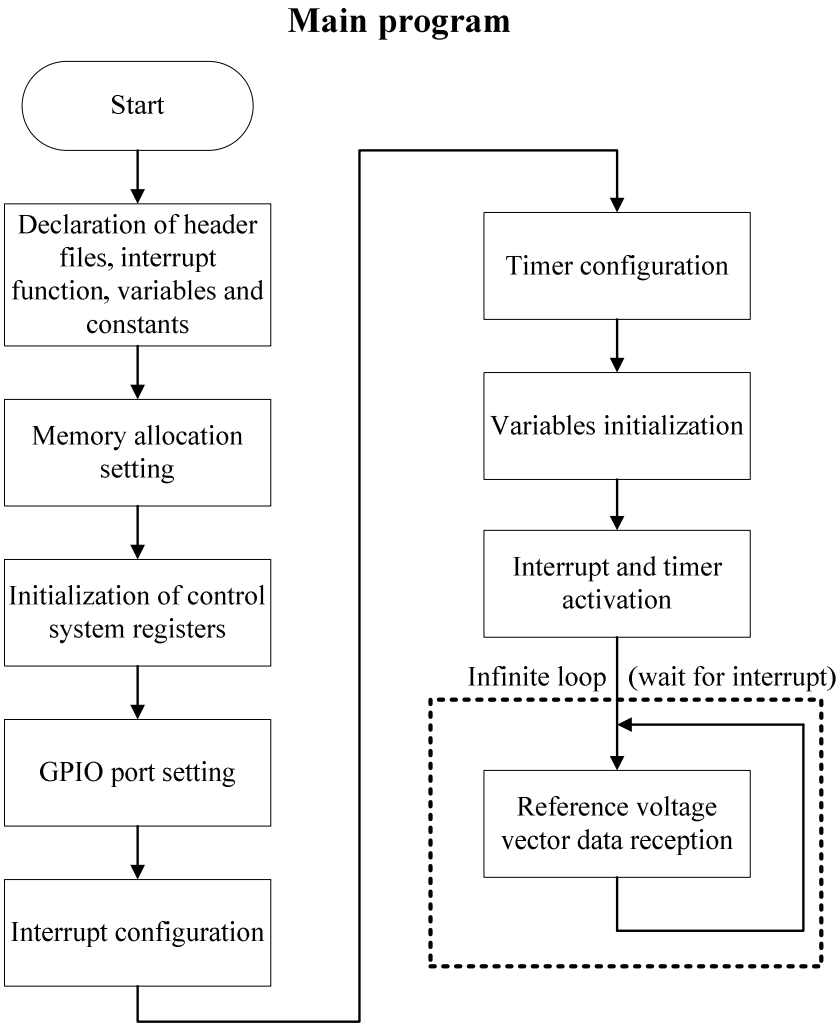


Figure 5.27: Main program for the modulator implementation.

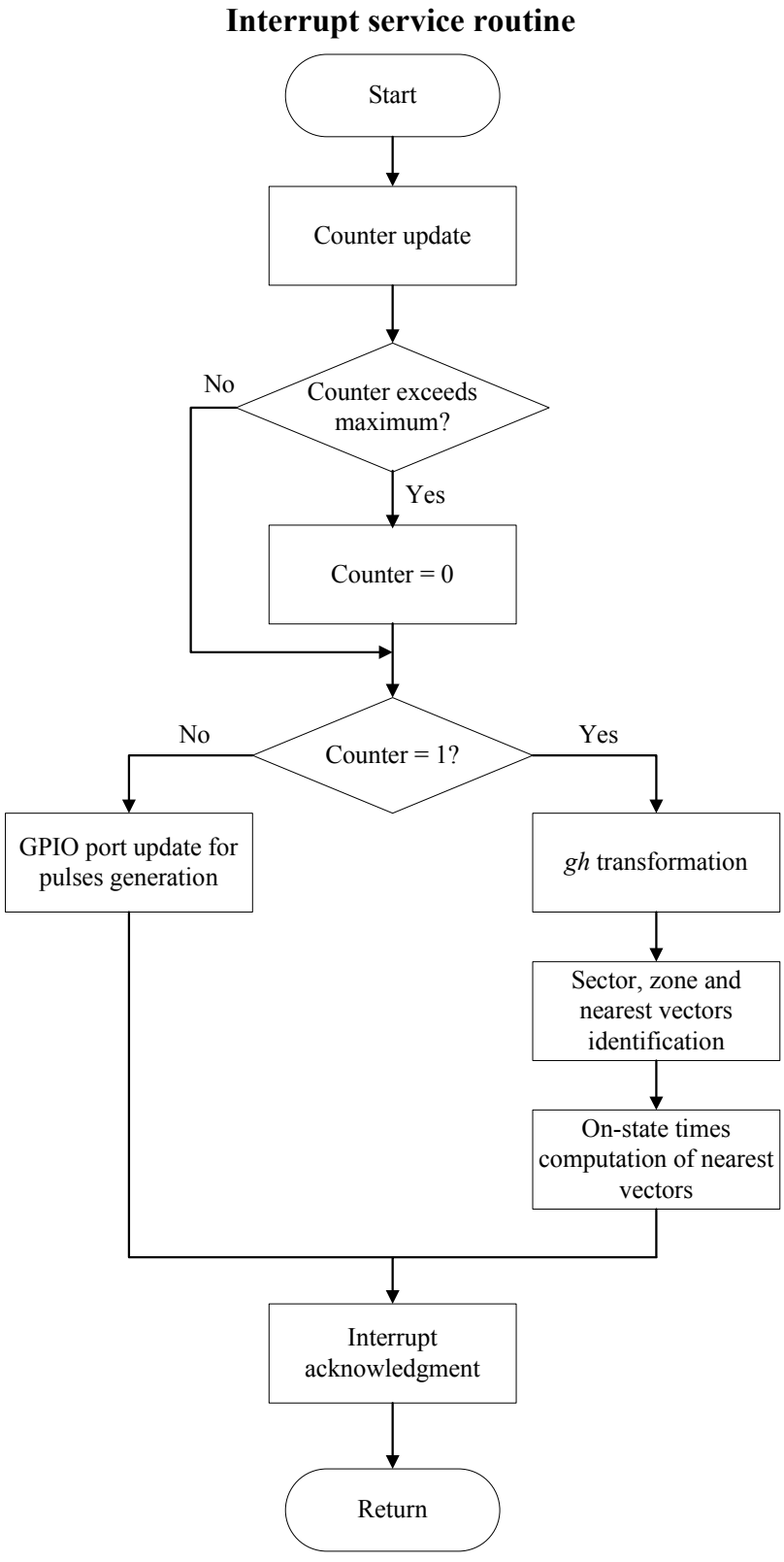


Figure 5.28: ISR for the modulator implementation.

available, V_{ref} and θ_{ref} are accordingly updated with the new values. In the next on-state time computation, θ_{ref} increment starts from the newly-changed value which is previously updated. For sector and zone identification, V_{ref} and θ_{ref} are transformed into gh coordinate system before computation of the on-state times can be carried out. Interrupt acknowledgment follows before the ISR ends.

5.6.1.2 Controller

The main program of the controller's program code is similar to that of the modulator. The corresponding flowchart is given in Figure 5.29. Similar bits of port D, E, F and G as those utilized by the modulator, are also used by the controller for the purpose of data transfer. The difference is the direction of those bits. The related bits of port D are configured as digital inputs. Other bits concerned of port E, F and G are set as digital outputs. Bits GPIOB0, GPIOB2 and GPIOB4 of port B are also programmed for use with the DAC function. With external low-pass filters, the DAC module can convert the values of variables of interest into signals that can be viewed using an oscilloscope. In addition, bit GPIOA0 is used as an input to indicate a load change event. ADC port through bits ADCA0, ADCA1, ADCA2 and ADCA6 are also employed to receive the signals from the voltage and current sensors for two phases. The signals for the third phase are determined by calculation. For example, the current in the third phase equals the summation of the currents in the first and second phases with a negative sign. Timer 2 of Event Manager A is also programmed to initiate an ISR for the ADC module every 204 μs. As for the infinite loop, data transmission involving V_{ref}, θ_{ref} and an update signal is monitored.

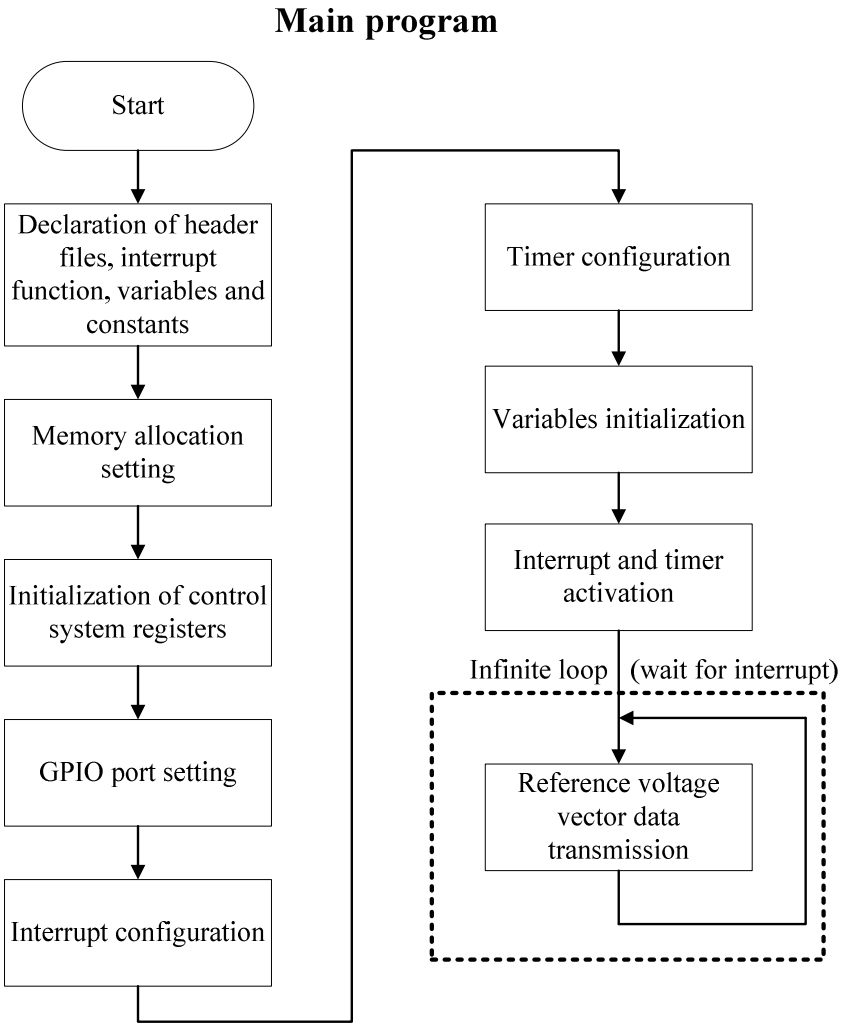


Figure 5.29: Main program for the controller implementation.

The process flow of the ISR can be described by the flowchart shown in Figure 5.30. The execution of the ISR begins by reading the ADC port. Through proper conversion, the original signal values which represent the measured voltage and current fed to the sensors, are obtained and then stored in dedicated variables for further use in the computation. A counter which has a maximum value of 98 is checked. If the counter value is not equal to 98, then the value increases by 1. Besides, summations of values of several parameters of interest are also carried out for the purpose of calculating the average and rms values within a period of 0.02 ms. These average and rms values are determined once the counter value equals 98. The reason to calculate the average and

rms values is to verify that the conversion done on the ADC values in obtaining the original signal data collected by the sensors is correct.

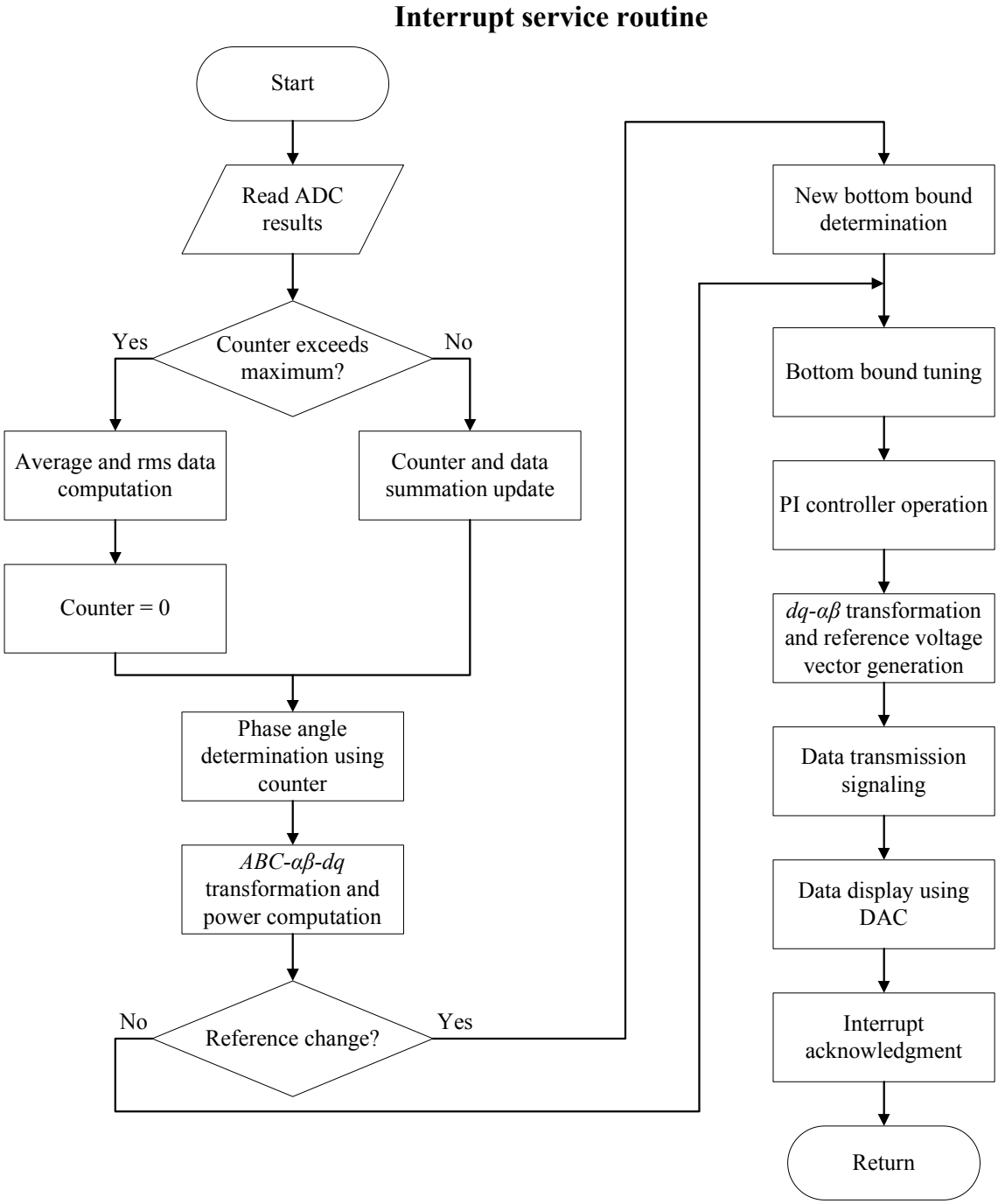


Figure 5.30: ISR for the controller implementation.

For example, the rms values of output current calculated by the DSP and measured by a multimeter are compared. If the two values are similar or almost similar with small error, then it is safe to use the converted ADC values for further computation. Another reason is that average value is more stable as compared to instantaneous value which fluctuates constantly. Therefore, to have a smooth data transfer, the average value of V_{ref} is used.

By using the counter, the phase angle is computed. After obtaining the voltage and current values in the stationary $\alpha\beta$ frame via ABC-$\alpha\beta$ transformation, further transformation to synchronous rotating dq frame is conducted using cosine and sine of the phase angle, as expressed in equation (3.40). Power computation is also conducted for the case of DPC-SVM scheme. The next process involves the checking of bit GPIOA0 which highlights a change in $i_{d,ref}$. The change occurs as a result of a load change. The proposed tuning algorithm as explained in Section 3.5.5 is then carried out before the PI controllers operation takes place. The control signals generated by the PI controllers are converted into V_{ref} and θ_{ref} after dq-$\alpha\beta$ transformation using equations (3.51), (3.15) and (3.16). A signal is then sent to the infinite loop to start a data transfer. For the purpose of displaying and monitoring the values of some variables in the form of real-time signals on the oscilloscope, the DAC module is employed. Before the ISR completes its execution, interrupt acknowledgment is declared at the end of the program.

5.6.1.3 Modulator-Controller Communication Interface

Communication between the modulator and the controller for the purpose of data transfer is carried out using GPIO ports. Four ports are configured for this purpose, namely ports D, E, F and G. Figure 5.31 shows all ports used by the modulator and the controller including those programmed for data transfer activity. There are three signals involved to implement the communication interface. 17-bit data signal is sent from the controller to the modulator, 2-bit control signal designated as Flag 1, is sent from the controller to the modulator and another 2-bit control signal labelled as Flag 2, is sent from the modulator to the controller.

Three data are involved in the data transfer namely V_{ref}, θ_{ref} and an update signal. To complete the transfer of the three data, three cycles of Flag 1-Flag 2 signal exchanges has to be executed. Figure 5.32 portrays the three cycles of the flag signal exchanges. During cycle 1, the modulator requests for a data transfer by sending bits 01 through Flag 2 to the controller. Once the controller receives the request, it then transmits bits 01 through Flag 1 to the modulator as an acknowledgement. The acknowledgment signal indicates that both controller and modulator are ready for the data transfer. A 16-bit data of V_{ref} is first transmitted. An additional bit is also transmitted using GPIOG5 to indicate the positive or negative sign of V_{ref}. All data bits are transmitted simultaneously during the cycle. After cycle 1 ends, cycle 2 starts and the same procedure as previously mentioned is repeated. In cycle 2, θ_{ref} is transferred while in cycle 3, an update signal is sent. Once cycle 3 finishes, the modulator checks the update signal whether the data received are new updates. If the data are new, they are then used to overwrite the old data. Otherwise, the old data maintain.

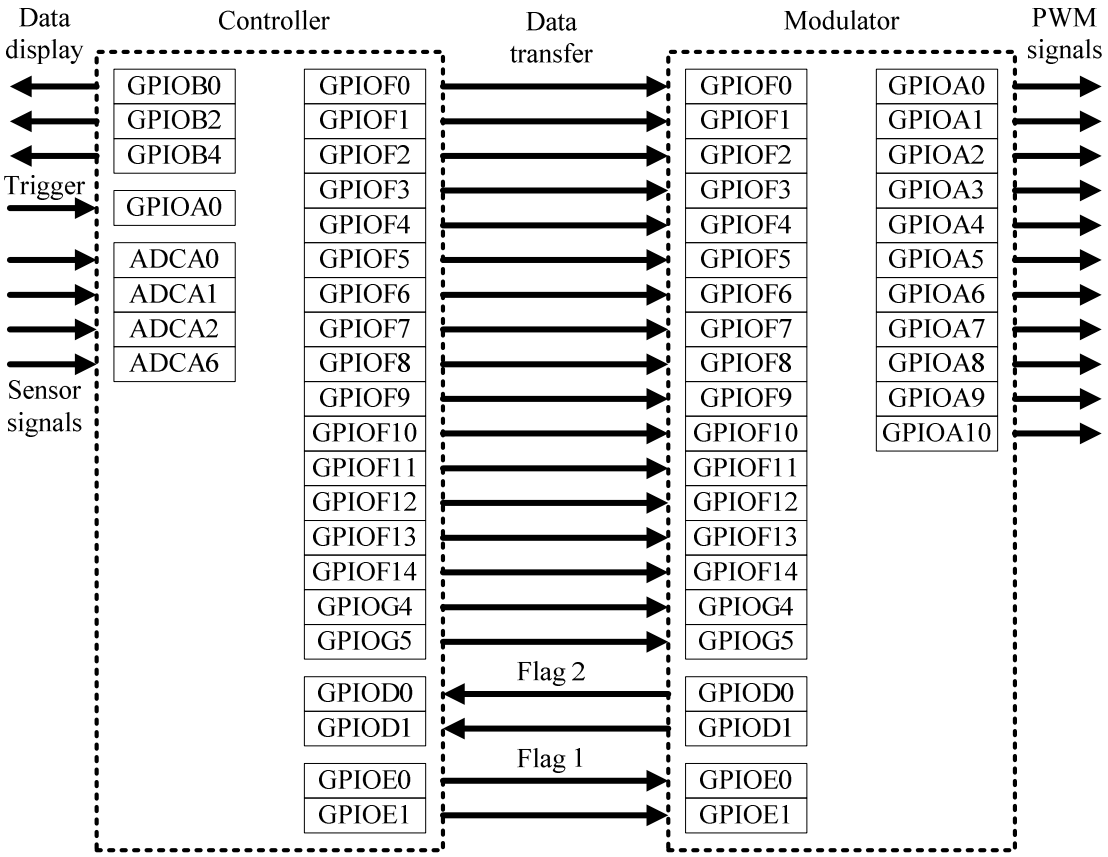


Figure 5.31: GPIO ports used by the modulator and controller.

When the controller transmits the data, the data type must be set as integer type. Since the data sent are of small decimal-point numbers, a conversion to bigger numbers is done via multiplication with a proper scaling factor as long as the converted number is not bigger than 2^{16}. The conversion also helps in maintaining the accuracy of the decimal-point numbers at an acceptable level. Once the data reach the modulator, they are stored in variables of float type. The same scaling factor used in the previous conversion, is now utilized to convert the transferred big numbers to the original small decimal-point numbers. This is done by dividing the big numbers with the scaling factor. Through these conversions, the data sent are correctly transferred without sacrificing the accuracy.

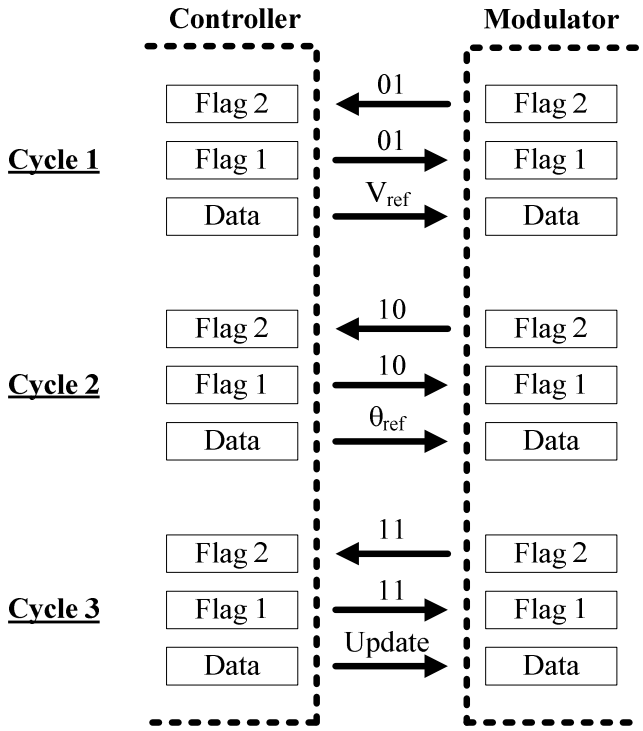


Figure 5.32: Data transfer mechanism.

The data transfer is basically done in binary form through the use of GPIO ports. To transfer a value, say 6.432, a conversion is carried out by multiplying the number with 1000 so that it becomes 6432. In binary form, 6432 is represented by 0001 1001 0010 0000_2. This binary number is sent to the ports concerned for transfer. As seen from Figure 5.31, two ports are used namely ports F and G. For the first 15 least significant bits, port F is directly used starting from GPIOF0 to GPIOF14. The most significant bit has to be transferred using GPIOG4 since all GPIO bits of port F have been utilized. To implement this, bit shifting has to be performed. Before the transfer takes place, the most significant bit is separated from other bits so that it can be transferred using GPIOG4 by shifting the bit 11 places to the right. Once the transfer is completed, the most significant bit is combined again with the other bits in a common variable by shifting 11 places to the left. To get the original decimal-point number, 6432 is then divided by 1000. Through this bit manipulation, the data transfer can be done with much ease.

5.6.2 Experimental Results and Analysis for VOC Scheme

Experiments are conducted for two conditions. The first condition involves the use of the automatic tuning algorithm for U_{low} adjustment of the PI current controller. In the second condition, the algorithm is not applied. The experimental results from both conditions are then compared to assess the effectiveness of the tuning algorithm. For the tuning algorithm to function as desired, preliminary tests are carried out to establish the relationship between U_{low} and $i_{d,ref}$ so that a specific equation based on the general equation (3.70) can be defined. By varying the resistive element of the load while keeping the inductive element at 10 mH, the experimental data shown in Figure 5.33 is obtained. By using MATLAB curve-fitting tool, the following equation is established to approximate the

U_{low}-$i_{d,ref}$ relationship as illustrated in Figure 5.34.

$$U_{low} = 4.836e^{0.3382 i_{d,ref}} \tag{5.3}$$

Figure 5.35 shows the experimental results reflecting the step response as a result of a load change. The step response displayed in Figure 5.35(a) is captured when the load changes from 62.0 Ω to 15.6 Ω. When the load change is reversed, Figure 5.35(b) is the result. The automatic tuning algorithm employed in obtaining those results leads to the increase of U_{low} from an average value of 7.4 to 28.0 when the load increases. The opposite is observed when the load decreases. A comparison between the two abovementioned conditions is illustrated in Figures 5.36 and 5.37. The results exhibited in Figure 5.36 are captured when the automatic tuning is employed while those displayed in Figure 5.37 are taken without the automatic tuning.

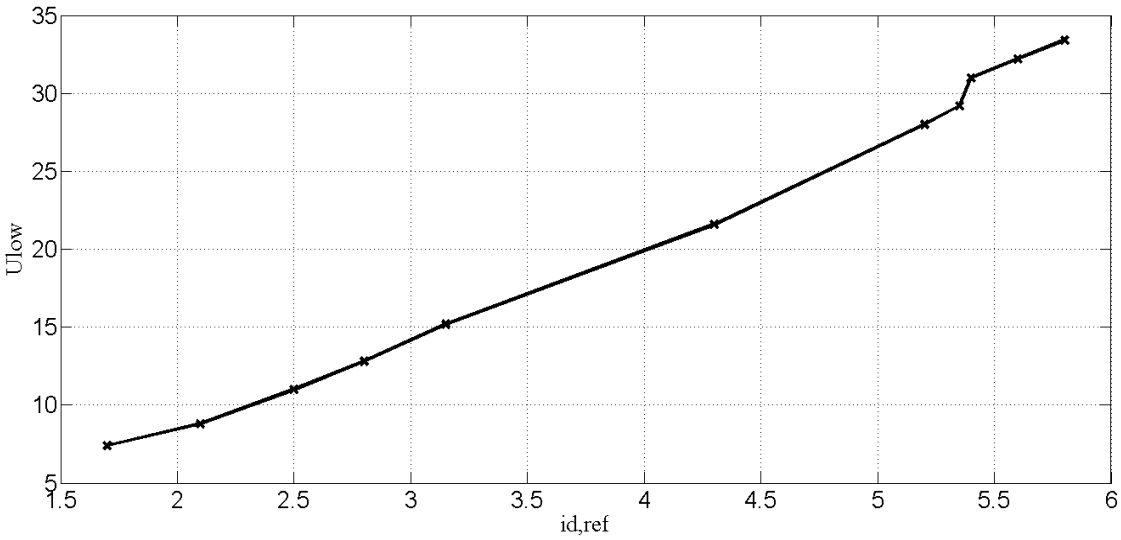


Figure 5.33: Experimental result showing the relationship between U_{low} and $i_{d,ref}$ as a result of load variations.

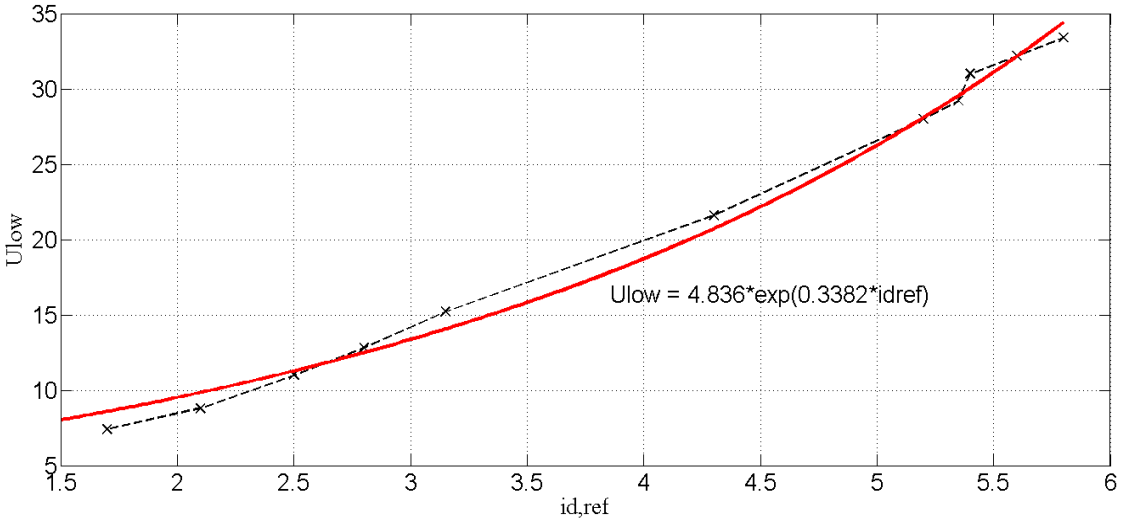
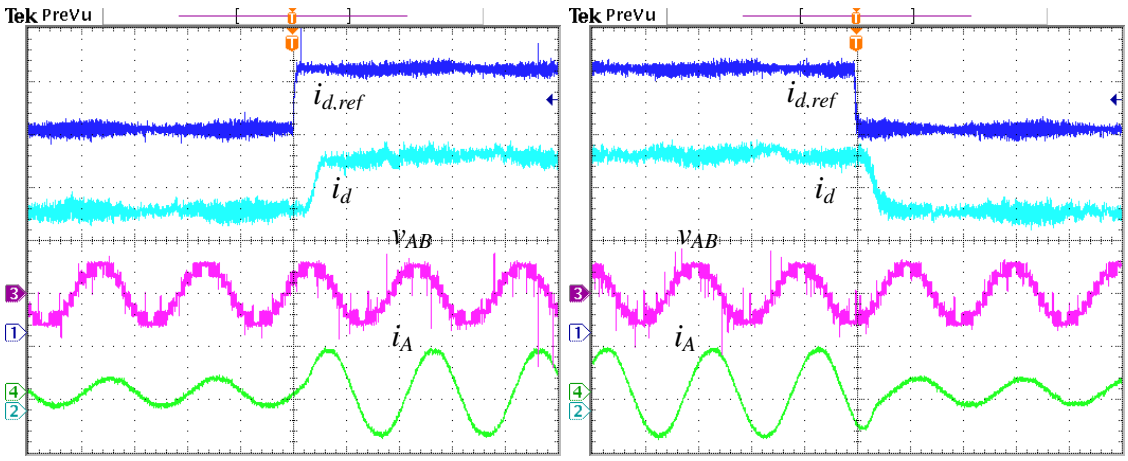


Figure 5.34: Approximation of U_{low}-$i_{d,ref}$ relationship using MATLAB curve-fitting tool.

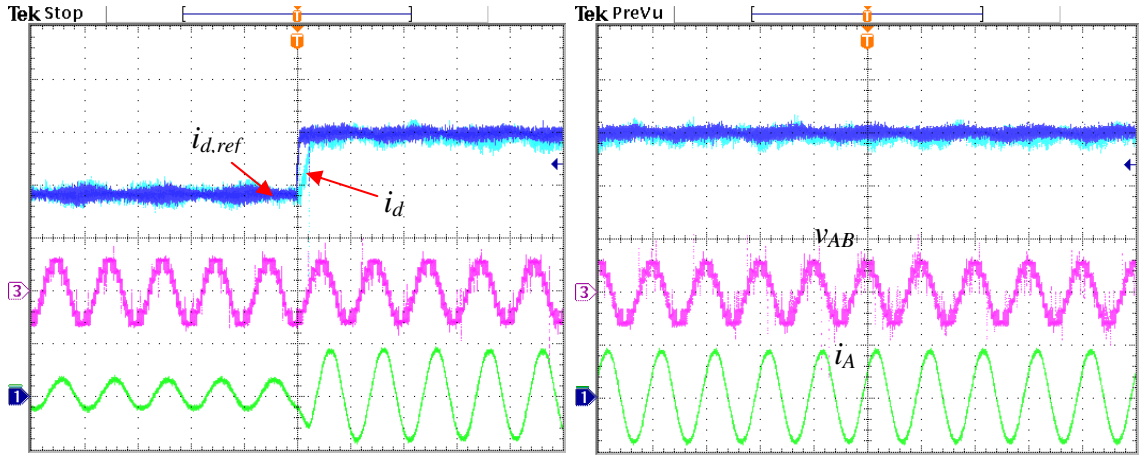


(a) Step response due to a load change from 62.0 Ω to 15.6 Ω

(b) Step response due to a load change from 15.6 Ω to 62.0 Ω

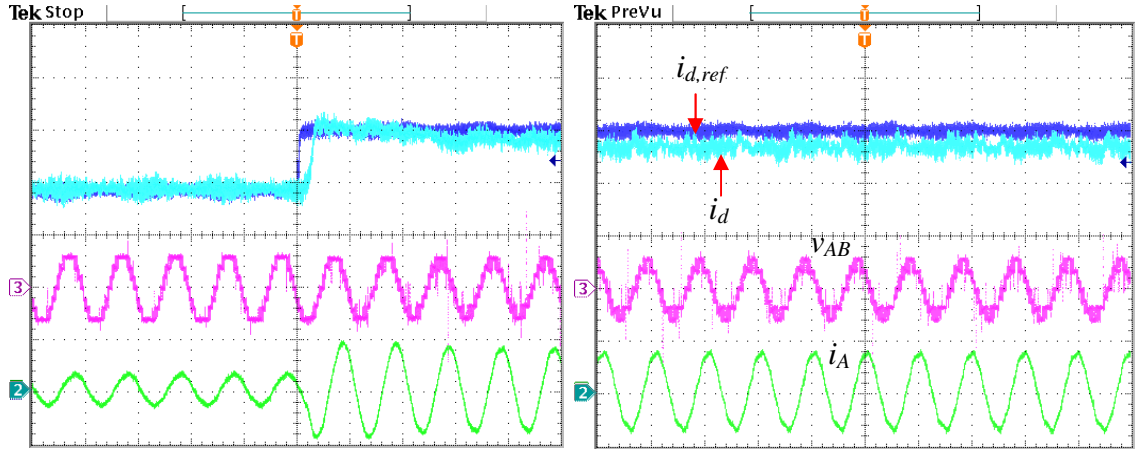
Figure 5.35: Experimental results of the step responses as a result of load changes for VOC scheme.

The results shown in Figures 5.36 and 5.37 are obtained when the load is made to change from 62.0 Ω to 15.6 Ω. For the implementation without automatic tuning, U_{low} is kept constant at value of 22.0. In both figures, two events are investigated, namely during the transient situation when the step response occurs and during the steady-state situation after the step response takes place. For the case with automatic tuning, it can be noticed that i_d is able to follow $i_{d,ref}$ satisfactorily. The inverter voltage v_{AB} appears to be similar before and after the load change. The quality of the load current i_A remains intact with a THD of 1.96% after the load change. However, when the tuning module in not included in the control scheme, i_d is no longer able to track $i_{d,ref}$ correctly. v_{AB} is observed to vary after the load change. The quality of i_A is also compromised with the THD during steady state is recorded at 3.43%.



(a) During the load change (b) After the load change

Figure 5.36: Experimental results of the step response with automatic tuning for VOC scheme.



(a) During the load change (b) After the load change

Figure 5.37: Experimental results of the step response without automatic tuning for VOC scheme.

5.6.3 Experimental Results and Analysis for DPC-SVM Scheme

The experimental procedure is similar to the one previously described for the VOC scheme. Instead of the current controllers, power controllers are employed in DPC-SVM scheme. Preliminary tests are performed to define the relationship between

U_{low} and p_{ref} according to the general equation (3.70). The result of the preliminary test is presented graphically in Figure 5.38. The readings are collected by varying the resistance of the load and maintaining the inductance at 10 mH. The following equation is derived with the aid of the MATLAB curve-fitting tool.

$$U_{low} = 1.062 \times 10^{-11} e^{0.06087\, p_{ref}} + 4.442 e^{0.00426\, p_{ref}} \tag{5.4}$$

The first term in equation (5.4) is ignored since it is very small. Hence, the equation is simplified as follows:

$$U_{low} = 4.442 e^{0.00426\, p_{ref}} \tag{5.5}$$

Figure 5.39 shows the curve of equation (5.5) to approximate U_{low}-p_{ref} relationship.

Figure 5.40 presents the step responses as a result of load changes between the values of 62.0 Ω and15.6 Ω. The automatic tuning module employed in the control scheme results in the rise of U_{low} from 8.6 to 28.6 during the load increase. The opposite is also true when the load reduces as U_{low} drops by 20 from 29. Using the same amount of load change, a study is also conducted without the use of automatic tuning. For this purpose, U_{low} is fixed at value of 20.0. The experimental results with and without automatic tuning during transient and steady-state situations are provided in Figures 5.41 and 5.42 respectively. For the case with automatic tuning, the tracking performance is satisfactory and the load current quality is maintained with the THD after the load change is recorded at 1.99%. On the other hand, the results without automatic tuning indicate poor tracking performance. The load current also records higher THD after the load change, viz 5.18% as compared to that when the automatic tuning is executed.

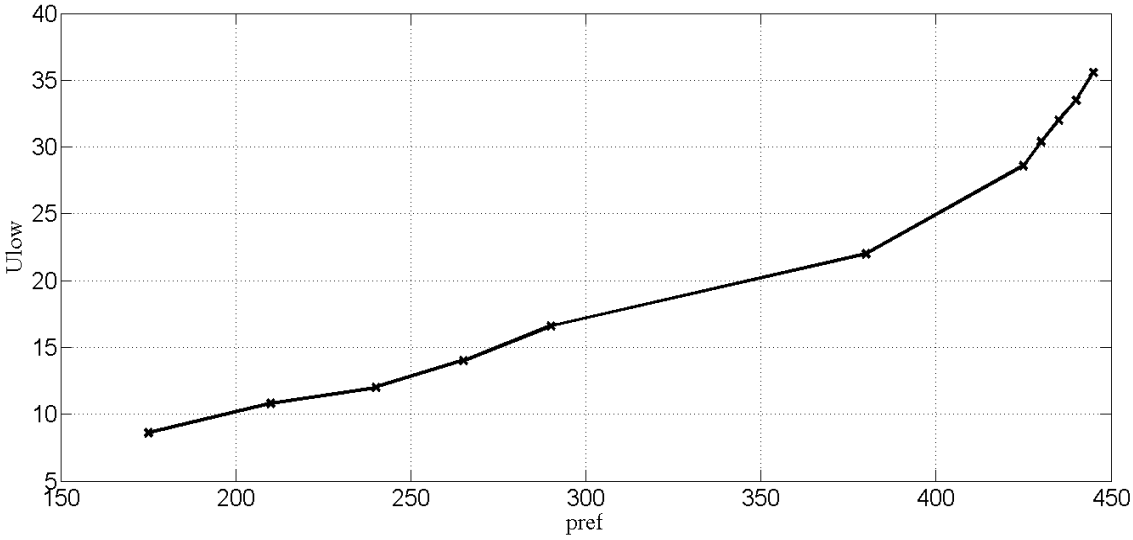


Figure 5.38: Experimental result showing the relationship between U_{low} and p_{ref} as a result of load variations.

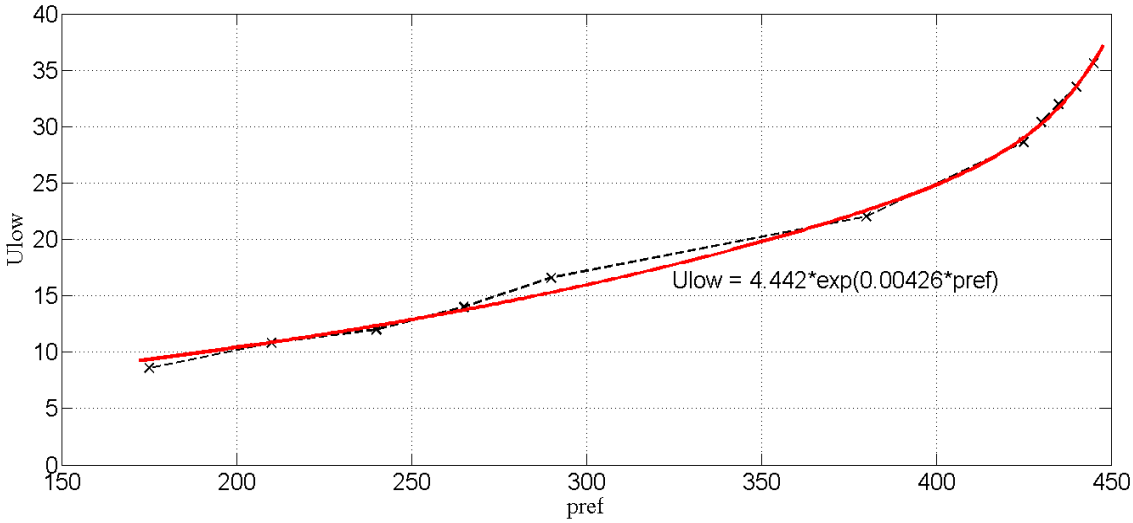
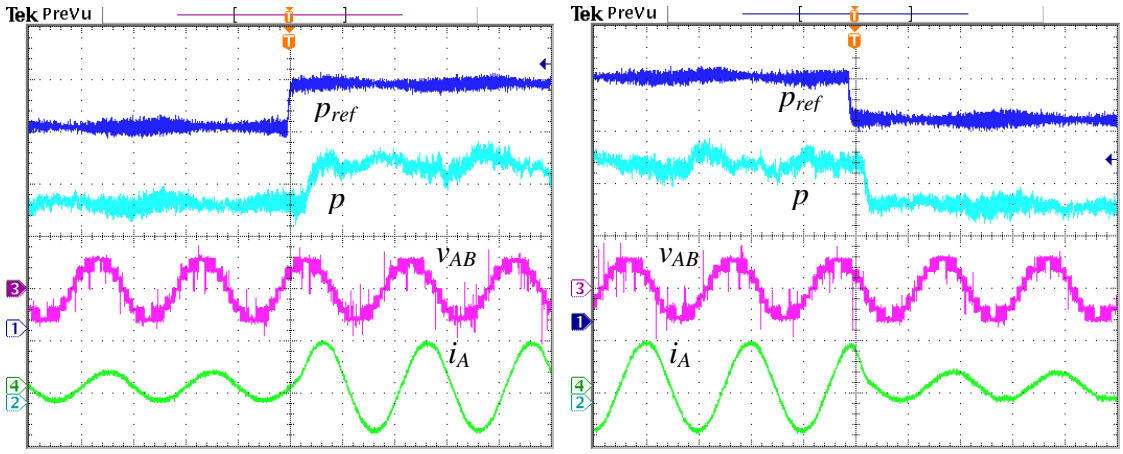


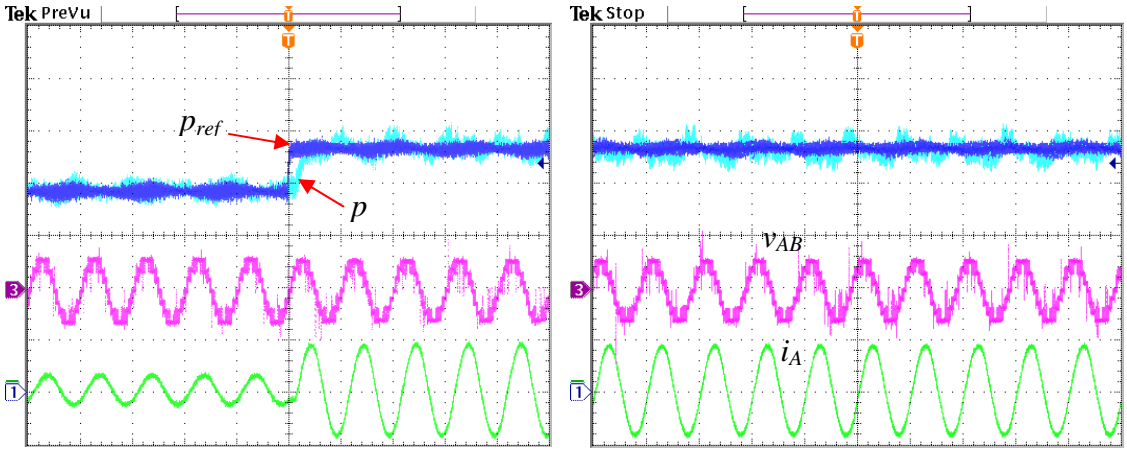
Figure 5.39: Approximation of U_{low}-p_{ref} relationship using MATLAB curve-fitting tool.



(a) Step response due to a load change from 62.0 Ω to 15.6 Ω

(b) Step response due to a load change from 15.6 Ω to 62.0 Ω

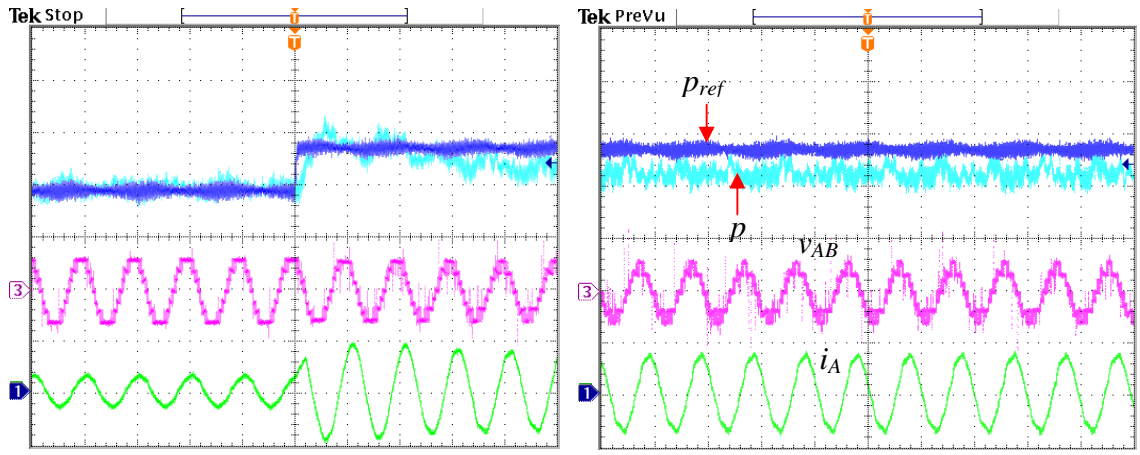
Figure 5.40: Experimental results of the step responses as a result of load changes for DPC-SVM scheme.



(a) During the load change

(b) After the load change

Figure 5.41: Experimental results of the step response with automatic tuning for DPC-SVM scheme.



(a) During the load change (b) After the load change

Figure 5.42: Experimental results of the step response without automatic tuning for DPC-SVM scheme.

5.7 Summary

In this chapter, the hardware implementation of the proposed inverter topology has been discussed. The prototype of the proposed inverter has been constructed for the four-level and five-level structures. DSP controller boards eZdsp^{TM} F2812 have been used to execute the programs designed for the implementation of the low switching frequency modulation, the proposed SVPWM and the current control schemes. The related program codes have been clearly described with the aid of relevant flowcharts.

Experiments have been conducted to capture the switching signals and the waveforms of interest. For the proposed SVPWM, the output voltage waveforms and the corresponding harmonic spectra have been analyzed for various reference voltage vector amplitudes. Harmonic analysis has been carried out and THD and voltage magnitude profiles have also been examined. To complete the experimental investigations, the control scheme performance with and without the proposed automatic tuning has been investigated. The tuning algorithm has been validated to improve the PI controller's performance.

CHAPTER 6

CONCLUSIONS

6.1 Concluding Remarks

As a way to promote energy sustainability, efficient power electronic converters are highly desired. Multilevel inverter is a converter that is able to offer that. However, like any other inventions, it also poses its own challenges. This work is conducted to get more insights into multilevel inverter's design and implementation issues and to propose viable solutions to the problems encountered.

One critical criterion that is always considered to justify the implementation of multilevel inverters for commercial use is the added cost incurred. In most cases, economical considerations are usually placed at the top among all other factors considered. Hence, it is no surprise when high performance, high efficient multilevel inverters are not entertained for a particular application when the added cost is not justified by the performance offered. In this work, the added cost is limited to the minimum possible by reducing the increase in the number of components used as the number of levels grows. This is realized by the new multilevel inverter topology proposed in this study.

The proposed multilevel inverter topology is composed of three modules. Module 1 is the conventional full-bridge six-switch circuit while Module 2 is represented by three bidirectional switches in which each of them represents each phase. Module 3 comprises a string of bidirectional switches which are connected to DC sources. To change the structure of the inverter from one level to the next nearest higher level, only one additional bidirectional switch is added in Module 3, while the number

of components in other modules is always the same regardless of the number of levels in the structure. Another important characteristic of the proposed topology is that the bidirectional switches in Module 3 are made to operate in the optimized mode in a way that the operation of each switch is divided among the three phases. In other words, the bidirectional switches are shared among the three phases instead of exclusively used for a certain phase.

To investigate the specific characteristics of a particular inverter structure of the proposed topology, the study is then concentrated on the four-level and five-level configurations. A novel SVPWM technique is developed to accommodate the uniqueness reflected in the proposed topology. As a result of the switch-sharing approach adopted for Module 3 which contributes to the elimination of several voltage vectors, virtual vectors are therefore introduced to replace the eliminated voltage vectors. This results in the presence of virtual boundaries that modify the voltage vector hexagon. Decomposition of the reference vector can be realized by using either three or two nearest vectors, depending on the fact whether the corresponding identified triangular zone has virtual sides or otherwise. A new method is also developed to determine the on-state times for the case when two nearest vectors are used to represent the reference vector.

Current control strategies based on VOC and DPC-SVM schemes have also become the subject of interest in this work. Since the performance of the PI controller is very much influenced by the load parameters, a new automatic tuning algorithm has been proposed to direct the controller to operate at the optimum operating point at any load conditions. The tuning algorithm is characterized by the adjustment initiated to modify only one parameter of the anti-windup module at the controller's output. The

significant impact of the tuning algorithm includes the ability of the controller to enhance or at least, maintain the good quality of the load current after a change in the load conditions occur.

Simulation has been performed as the first step to verify the theoretical design and analysis of the proposed multilevel inverter topology. For further validation, a hardware implementation has been conducted. A laboratory prototype has been constructed and a DSP has been used to implement the SVPWM algorithm in real time. An additional DSP has also been employed to execute the current control schemes. A simple DSP-to-DSP interfacing has also been established to link the SVPWM module and the current control module. The experimental results reveal the close agreement with those from simulation.

6.2 Author's Contributions

The contribution of the work conducted can be viewed from three different aspects namely, multilevel inverter topology, modulation method and automatic tuning module for the PI controller. These are summarized as below:

1. The proposed multilevel inverter topology is a novel topology that exploits the ability of the power switching devices for sharing among the three phases. By doing so, the number of components employed can be significantly reduced. As an example, the five-level structure of the proposed topology requires only 47 components as compared to 89 for the diode-clamped topology, 71 for the flying-capacitor topology and 60 for cascaded H-bridge topology (refer to Table 3.1). This implies a considerable reduction in cost, improved reliability and less complexity for implementation. At the same time, the proposed topology is also able to offer the same performance as other topologies in certain aspects. In fact,

in some areas such as efficiency, the proposed topology outperforms the diode-clamped topology, for instance.

2. A novel SVPWM method has been developed with the application of virtual vectors. This method provides the solution to the reference vector decomposition problem in certain zones that require more than three nearest vectors to represent the reference vector. In this method, a reference vector can be decomposed into either three or two nearest vectors. A step-by-step procedure to calculate the on-state times particularly for the two nearest vectors has also been established.
3. A new automatic tuning module is included into the PI controller structure to make the controller adaptive. The tuning module prompts one of the anti-windup module parameters of the controller's output to vary until an appropriate value is achieved. This tuning signals a change of the controller's optimum operating point in handling different load conditions.

6.3 Recommendations for Further Work

Although the study objectives have been achieved as highlighted in the work contributions, several issues are worthwhile for further investigations. The proposed multilevel inverter has one shortcoming. The voltage stress that each switch in Module 1 has to withstand is equal to the total DC input voltage. As a result, the voltage rating of the inverter cannot be increased without increasing the voltage rating of the individual switches in Module 1. Since the existing switches can only achieve a voltage rating of up to a few kilovolt, the inverter is therefore not able to be used for medium and high power applications. Although the approach to replace each switch in Module 1 with a series connection of a number of switches, can be attempted, there is no guarantee that the voltage stress that the switches have to bear is equally divided. The fact that solid-state switches are grown from crystals, leads to uneven properties of the

switches. Hence, auxiliary circuits based on precise values of resistive, capacitive and inductive elements have to be designed to ensure equal voltage stress sharing among the series-connected switches in both transient and steady-state operations. Unfortunately, since the design of such circuits amounts to expensive investment in research and development, most industrial players abandon the pursuit to develop the required expertise. Therefore, different approaches can be further explored to give focus on Module 1 by means of modifying the structure or the like.

Despite the fact that the proposed multilevel inverter has a flaw that prevents it from being used in medium and high power applications, its prospect for being employed in low power applications is not as dim as one might expects. Although the competition against the classical two-level inverter is fierce, there are areas where the proposed multilevel inverter may have the edge. With the increasing interest in microgrids in recent years, the emphasis on efficiency improvement may pave the way for the possible application of the proposed inverter. In addition, the proposed inverter may well be utilized to overcome the partial shading issue to improve the output power in small-capacity PV generation systems. Another aspect involves the stringent requirements in the aviation industry to reduce the weight of the parts installed in a modern aircraft. As modern aircrafts are evolving to be of electric-based, the heavy filters used with the two-level inverters in compressors, hydraulic pumps and electric brakes for instance, can be a non-compliance to the regulations. This may provide an opportunity for the expanded application of the proposed inverter.

Considering the fact that the proposed multilevel inverter can be useful in some low power applications, further work can be carried out to iron out several issues that require better solutions. In this work, to implement the closed loop system, two DSPs

have been used to implement the SVPWM algorithm and the current control strategy. Program code optimization can be performed to simplify the SVPWM implementation in particular. Improved algorithm can be suggested so that the entire program that combines both SVPWM and the current control algorithm can be implemented on a single DSP. Although this is challenging as the number of levels grows, it is definitely an added advantage to use one DSP as this reduces the implementation cost further.

In this work, batteries are used as the DC sources. Instead of using batteries, a power supply and voltage dividing capacitors can also be used. Further investigations can be carried out to study the capacitor voltage balancing issue for the proposed topology. Besides, implementation of the proposed topology for low-powered REGS such as PV applications can also be considered for further work. In addition, the performance of the PI controller with the automatic tuning module has not been studied in this work for variable DC source conditions. Some modifications are needed to the tuning algorithm and this worth further investigations as well.

Other modulation methods based on carrier-based modulation or SHE techniques can be investigated for the proposed multilevel inverter. The tuning algorithm can also be equipped with AI-based techniques such as neural networks and genetic algorithms. Other controllers such as fuzzy logic controllers, hysteresis controllers, predictive controllers and emotional controllers are also possible for further study to replace the adaptive PI controller.

REFERENCES

Abdalla, I., Corda, J., & Zhang, L. (2013). Multilevel DC-link inverter and control algorithm to overcome the PV partial shading. *IEEE Transactions on Power Electronics*, 28(1), 14-18.
doi: 10.1109/TPEL.2012.2209460

Adam, G. P., Abdelsalam, I., Finney, S. J., Holliday, D., Williams, B. W., & Fletcher, J. (2013). Comparison of two advanced modulation strategies for a hybrid cascaded converter. *Proceedings of the IEEE ECCE Asia Downunder (ECCE Asia)*, 1334-1340.
doi: 10.1109/ECCE-Asia.2013.6579283

Aggrawal, H., Leon, J. I., Franquelo, L. G., Kouro, S., Garg, P., & Rodriguez, J. (2011). Model predictive control based selective harmonic mitigation technique for multilevel cascaded H-bridge converters. *Proceedings of the 37th Annual Conference on IEEE Industrial Electronics Society (IECON 2011)*, 4427-4432.
doi: 10.1109/IECON.2011.6120037

Akagi, H., Kanazawa, Y., & Nabae, A. (1984). Instantaneous reactive power compensators comprising switching devices without energy storage components. *IEEE Transactions on Industry Applications*, IA-20(3), 625-630.
doi: 10.1109/TIA.1984.4504460

Alonso, O., Sanchis, P., Gubia, E., & Marroyo, L. (2003). Cascaded H-bridge multilevel converter for grid connected photovoltaic generators with independent maximum power point tracking of each solar array. *Proceedings of the IEEE 34th Annual Power Electronics Specialist Conference (PESC '03)*, 2, 731-735.
doi: 10.1109/PESC.2003.1218146

Amin, M. M. N., & Mohammed, O. A. (2010). Vector oriented control of voltage source PWM inverter as a dynamic VAR compensator for wind energy conversion system connected to utility grid. *Proceedings of the 25th Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 1640-1650.
doi: 10.1109/APEC.2010.5433452

Azizur Rahman, M., Radwan, T. S., Osheiba, A. M., & Lashine, A. E. (1997). Analysis of current controllers for voltage-source inverter. *IEEE Transactions on Industrial Electronics*, 44(4), 477-485.
doi: 10.1109/41.605621

Babaei, E., & Hosseini, S. H. (2009). New cascaded multilevel inverter topology with minimum number of switches. *Energy Conversion and Management*, 50(11), 2761-2767.
doi: http://dx.doi.org/10.1016/j.enconman.2009.06.032

Barbosa, P., Steimer, P., Steinke, J., Meysenc, L., Winkelnkemper, M., & Celanovic, N. (2005). Active neutral-point-clamped multilevel converters. *Proceedings of the IEEE 36th Power Electronics Specialists Conference (PESC '05)*, 2296-2301.
doi: 10.1109/PESC.2005.1581952

Ben Echikh, H., Trabelsi, R., Mirnouni, M. F., & M'Sahli, F. (2013). 5-Phase AC induction motor rotor flux oriented control with space vector modulation technique. *Proceedings of the International Conference on Electrical Engineering and Software Applications (ICEESA)*, 1-12.
doi: 10.1109/ICEESA.2013.6578487

Bode, G. H., Zmood, D. N., Loh, P. C., & Holmes, D. G. (2001). A novel hysteresis current controller for multilevel single phase voltage source inverters. *Proceedings of the IEEE 32nd Annual Power Electronics Specialists Conference (PESC 2001)*, 4, 1845-1850.
doi: 10.1109/PESC.2001.954390

Bong-Hwan, K., Jang-Hyoun, Y., & Jee-Woo, L. (1999). A line-voltage-sensorless synchronous rectifier. *IEEE Transactions on Power Electronics*, 14(5), 966-972.
doi: 10.1109/63.788502

Bong-Hwan, K., Tae-Woo, K., & Jang-Hyoun, Y. (1998). A novel SVM-based hysteresis current controller. *IEEE Transactions on Power Electronics*, 13(2), 297-307.
doi: 10.1109/63.662844

Bouafia, A., Gaubert, J. P., & Krim, F. (2010). Predictive direct power control of three-phase pulsewidth modulation (PWM) rectifier using space-vector modulation (SVM). *IEEE Transactions on Power Electronics*, 25(1), 228-236.
doi: 10.1109/TPEL.2009.2028731

Brod, D. M., & Novotny, D. W. (1985). Current control of VSI-PWM inverters. *IEEE Transactions on Industry Applications*, IA-21(3), 562-570.
doi: 10.1109/TIA.1985.349711

Bruckner, T., & Bemet, S. (2001). Loss balancing in three-level voltage source inverters applying active NPC switches. *Proceedings of the IEEE 32nd Annual Power Electronics Specialists Conference (PESC 2001)*, 2, 1135-1140.
doi: 10.1109/PESC.2001.954272

Bruckner, T., Bernet, S., & Guldner, H. (2005). The active NPC converter and its loss-balancing control. *IEEE Transactions on Industrial Electronics*, 52(3), 855-868. doi: 10.1109/TIE.2005.847586

Carrara, G., Gardella, S., Marchesoni, M., Salutari, R., & Sciutto, G. (1992). A new multilevel PWM method: a theoretical analysis. *IEEE Transactions on Power Electronics*, 7(3), 497-505. doi: 10.1109/63.145137

Ceglia, G., Guzman, V., Sanchez, C., Ibanez, F., Walter, J., & Gimenez, M. I. (2006). A new simplified multilevel inverter topology for DC-AC conversion. *IEEE Transactions on Power Electronics*, 21(5), 1311-1319. doi: 10.1109/TPEL.2006.880303

Celanovic, N., & Boroyevich, D. (2001). A fast space-vector modulation algorithm for multilevel three-phase converters. *IEEE Transactions on Industry Applications*, 37(2), 637-641.

Chaniago, K., Selvaraj, J., & Rahim, N. A. (2008). Implementation of single-phase grid connected inverter using TMS320F2812. *Proceedings of the 3rd IEEE Conference on Industrial Electronics and Applications (ICIEA 2008)*, 1498-1502. doi: 10.1109/ICIEA.2008.4582768

Chiasson, J. N., Tolbert, L. M., McKenzie, K. J., & Zhong, D. (2005). Elimination of harmonics in a multilevel converter using the theory of symmetric polynomials and resultants. *IEEE Transactions on Control Systems Technology*, 13(2), 216-223. doi: 10.1109/TCST.2004.839556

Cichowlas, M., & Kamierkowski, M. P. (2002). Comparison of current control techniques for PWM rectifiers. *Proceedings of the 2002 IEEE International Symposium on Industrial Electronics (ISIE 2002)*, 4, 1259-1263. doi: 10.1109/ISIE.2002.1025970

Cortes, P., Wilson, A., Kouro, S., Rodriguez, J., & Abu-Rub, H. (2010). Model predictive control of multilevel cascaded H-bridge inverters. *IEEE Transactions on Industrial Electronics*, 57(8), 2691-2699. doi: 10.1109/TIE.2010.2041733

Cougo, B., Gateau, G., Meynard, T., Bobrowska-Rafal, M., & Cousineau, M. (2012). PD modulation scheme for three-phase parallel multilevel inverters. *IEEE Transactions on Industrial Electronics*, 59(2), 690-700. doi: 10.1109/TIE.2011.2158773

Dae-Wook, K., Yo-Han, L., Bum-Seok, S., Chang-Ho, C., & Dong-Seok, H. (2003). An improved carrier-based SVPWM method using leg voltage redundancies in generalized cascaded multilevel inverter topology. *IEEE Transactions on Power Electronics*, 18(1), 180-187. doi: 10.1109/TPEL.2002.807187

Dahidah, M. A., & Agelidis, V. G. (2005). A hybrid genetic algorithm for selective harmonic elimination control of a multilevel inverter with non-equal DC sources. *Proceedings of the International Conference on Power Electronics and Drives Systems (PEDS 2005)*, 2, 1205-1210. doi: 10.1109/PEDS.2005.1619871

Dannehl, J., Wessels, C., & Fuchs, F. W. (2009). Limitations of voltage-oriented PI current control of grid-connected PWM rectifiers with LCL filters. *IEEE Transactions on Industrial Electronics*, 56(2), 380-388. doi: 10.1109/TIE.2008.2008774

Das, A., Sivakumar, K., Ramchand, R., Patel, C., & Gopakumar, K. (2009a). A combination of hexagonal and 12-Sided polygonal voltage space vector PWM control for IM drives using cascaded two-level inverters. *IEEE Transactions on Industrial Electronics*, 56(5), 1657-1664. doi: 10.1109/TIE.2009.2013751

Das, A., Sivakumar, K., Ramchand, R., Patel, C., & Gopakumar, K. (2009b). A pulsewidth modulated control of induction motor drive using multilevel 12-sided polygonal voltage space vectors. *IEEE Transactions on Industrial Electronics*, 56(7), 2441-2449. doi: 10.1109/TIE.2009.2020075

De, S., Banerjee, D., Siva Kumar, K., Gopakumar, K., Ramchand, R., & Patel, C. (2011). Multilevel inverters for low-power application. *IET Power Electronics*, 4(4), 384-392. doi: 10.1049/iet-pel.2010.0027

De Silva, P. S. N., Fletcher, J. E., & Williams, B. W. (2004). Development of space vector modulation strategies for five phase voltage source inverters. *Proceedings of the 2nd International Conference on Power Electronics, Machines and Drives (PEMD 2004)*, 2, 650-655. doi: 10.1049/cp:20040365

Dey, A., Rajeevan, P. P., Ramchand, R., Mathew, K., & Gopakumar, K. (2013). A space-vector-based hysteresis current controller for a general n-level inverter-fed drive with nearly constant switching frequency control. *IEEE Transactions on Industrial Electronics*, 60(5), 1989-1998.
doi: 10.1109/TIE.2012.2200217

Dixon, J., Breton, A. A., Rios, F. E., Rodriguez, J., Pontt, J., & Perez, M. A. (2007). High-power machine drive, using nonredundant 27-level inverters and active front end rectifiers. *IEEE Transactions on Power Electronics,* 22(6), 2527-2533.
doi: 10.1109/TPEL.2007.909276

Dixon, J., & Moran, L. (2006). High-level multistep inverter optimization using a minimum number of power transistors. *IEEE Transactions on Power Electronics*, 21(2), 330-337.
doi: 10.1109/TPEL.2005.869745

Du Toit Mouton, H. (2002). Natural balancing of three-level neutral-point-clamped PWM inverters. *IEEE Transactions on Industrial Electronics*, 49(5), 1017-1025.
doi: 10.1109/TIE.2002.803205

Duran, M. J., & Levi, E. (2006). Multi-dimensional approach to multi-phase space vector pulse width modulation. *Proceedings of the 32nd Annual Conference on IEEE Industrial Electronics (IECON 2006)*, 2103-2108.
doi: 10.1109/IECON.2006.347436

Ebrahimi, J., Babaei, E., & Gharehpetian, G. B. (2012). A new multilevel converter topology with reduced number of power electronic components. *IEEE Transactions on Industrial Electronics*, 59(2), 655-667.
doi: 10.1109/TIE.2011.2151813

El-Naggar, K., & Abdelhamid, T. H. (2008). Selective harmonic elimination of new family of multilevel inverters using genetic algorithms. *Energy Conversion and Management*, 49(1), 89-95.
doi: http://dx.doi.org/10.1016/j.enconman.2007.05.014

Escalante, M. F., Vannier, J. C., Arzande, A. (2002). Flying capacitor multilevel inverters and DTC motor drive applications. *IEEE Transactions on Industrial Electronics*, 49(4), 809-815.
doi: 10.1109/TIE.2002.801231

Espinosa, E., Espinoza, J., Melin, P., Ramirez, R., Villarroel, F., Munoz, J., & Moran, L. (2014). A new modulation method for a 13-level asymmetric inverter towards minimum THD. *IEEE Transactions on Industry Applications*, 50(3), 1924-1933.
doi: 10.1109/TIA.2013.2282494

Fei, W. (2002). Sine-triangle versus space-vector modulation for three-level PWM voltage-source inverters. *IEEE Transactions on Industry Applications*, 38(2), 500-506.
doi: 10.1109/28.993172

Filho, F., Maia, H. Z., Mateus, T. H. A., Ozpineci, B., Tolbert, L. M., & Pinto, J. O. P. (2013). Adaptive selective harmonic minimization based on ANNs for cascade multilevel inverters with varying DC sources. *IEEE Transactions on Industrial Electronics*, 60(5), 1955-1962.
doi: 10.1109/TIE.2012.2224072

Franquelo, L. G., Napoles, J., Guisado, R. C. P., Leon, J. I., & Aguirre, M. A. (2007). A flexible selective harmonic mitigation technique to meet grid codes in three-level PWM converters. *IEEE Transactions on Industrial Electronics*, 54(6), 3022-3029.
doi: 10.1109/TIE.2007.907045

Franquelo, L. G., Prats, M. A. M., Portillo, R. C., Galvan, J. I. L., Perales, M. A., Carrasco, J. M., Diez, E. G., Jimenez, J. L. M. (2006). Three-dimensional space-vector modulation algorithm for four-leg multilevel converters using abc coordinates. *IEEE Transactions on Industrial Electronics*, 53(2), 458-466.
doi: 10.1109/TIE.2006.870884

Franquelo, L. G., Rodriguez, J., Leon, J. I., Kouro, S., Portillo, R., & Prats, M. A. M. (2008). The age of multilevel converters arrives. *IEEE Industrial Electronics Magazine*, 2(2), 28-39.
doi: 10.1109/MIE.2008.923519

Govindaraju, C., & Baskaran, K. (2011). Efficient sequential switching hybrid-modulation techniques for cascaded multilevel inverters. *IEEE Transactions on Power Electronics*, 26(6), 1639-1648.
doi: 10.1109/TPEL.2010.2089064

Guennegues, V., Gollentz, B., Meibody-Tabar, F., Rael, S., & Leclere, L. (2009). A converter topology for high speed motor drive applications. *Proceedings of the 13th European Conference on Power Electronics and Applications (EPE '09)*, 1-8.

Gui-Jia, S. (2005). Multilevel DC-link inverter. *IEEE Transactions on Industry Applications*, 41(3), 848-854.
doi: 10.1109/TIA.2005.847306

Gupta, A. K., & Khambadkone, A. M. (2006). A space vector PWM scheme for multilevel inverters based on two-level space vector PWM. *IEEE Transactions on Industrial Electronics*, 53(5), 1631-1639. doi: 10.1109/TIE.2006.881989

Gupta, K. K., & Jain, S. (2013). A multilevel voltage source inverter (VSI) to maximize the number of levels in output waveform. *International Journal of Electrical Power & Energy Systems*, 44(1), 25-36. doi: http://dx.doi.org/10.1016/j.ijepes.2012.07.008

Hagiwara, M., & Akagi, H. (2009). Control and experiment of pulsewidth-modulated modular multilevel converters. *IEEE Transactions on Power Electronics*, 24(7), 1737-1746. doi: 10.1109/TPEL.2009.2014236

Hill, W. A., & Harbourt, C. D. (1999). Performance of medium voltage multi-level inverters. *Proceedings of the 34th IEEE IAS Annual Meeting Industry Applications Conference*, 2, 1186-1192. doi: 10.1109/IAS.1999.801654

Holtz, J. (1994). Pulsewidth modulation for electronic power conversion. *Proceedings of the IEEE,* 82(8), 1194-1214. doi: 10.1109/5.301684

Hosseini Aghdam, M. G., Fathi, S. H., & Gharehpetian, G. B. (2007). Comparison of OMTHD and OHSW harmonic optimization techniques in multi-level voltage-source inverter with non-equal DC sources. *Proceedings of the 7th International Conference on Power Electronics (ICPE '07)*, 587-581. doi: 10.1109/ICPE.2007.4692456

Inoue, Y., Morimoto, S., & Sanada, M. (2012). Control method suitable for direct-torque-control-based motor drive system satisfying voltage and current limitations. *IEEE Transactions on Industry Applications*, 48(3), 970-976. doi: 10.1109/TIA.2012.2191170

International Energy Agency. (2012). *2012 Key world energy statistics*. Paris.

International Energy Agency. (2013). *Executive summary world energy outlook 2013*. Paris.

Iqbal, A., & Levi, E. (2005). Space vector modulation schemes for a five-phase voltage source inverter. *Proceedings of the European Conference on Power Electronics and Applications*, 1-12.

doi: 10.1109/EPE.2005.219194

Jasinski, M. (2005). Direct power and torque control of AC/DC/AC converter-fed induction motor drives. (Doctoral dissertation, Warsaw University of Technology). Retrieved from http://www.isep.pw.edu.pl/icg/pdf/phd/marek_jasinski.pdf

Jia-Min, S., Hurng-Liahng, J., Jinn-Chang, W., & Kuen-Der, W. (2013). Five-level inverter for renewable power generation system. *IEEE Transactions on Energy Conversion*, 28(2), 257-266.
doi: 10.1109/TEC.2013.2252352

Jih-Sheng, L., & Fang Zheng, P. (1996). Multilevel converters-a new breed of power converters. *IEEE Transactions on Industry Applications*, 32(3), 509-517.
doi: 10.1109/28.502161

Jing, H., & Corzine, K. A. (2006). Extended operation of flying capacitor multilevel inverters. *IEEE Transactions on Power Electronics*, 21(1), 140-147.
doi: 10.1109/TPEL.2005.861108

Jing, Z., Xiangning, H., & Zhao, R. (2010). A novel PWM control method for hybrid-clamped multilevel inverters. *IEEE Transactions on Industrial Electronics*, 57(7), 2365-2373.
doi: 10.1109/TIE.2009.2027915

Kadir, M. N. A. (2010). Design and control of hybrid multistage inverter for AC drives. (Unpublished doctoral dissertation). University of Malaya, Kuala Lumpur.

Kadir, M. N. A., & Hussien, Z. F. (2005). Asymmetrical multilevel inverter: maximum resolution for H-bridge topology. *Proceedings of the International Conference on Power Electronics and Drives Systems (PEDS 2005)*, 2, 1068-1071.
doi: 10.1109/PEDS.2005.1619846

Kadri, R., Gaubert, J. P., & Champenois, G. (2011). An improved maximum power point tracking for photovoltaic grid-connected inverter based on voltage-oriented control. *IEEE Transactions on Industrial Electronics*, 58(1), 66-75.
doi: 10.1109/TIE.2010.2044733

Kang, D. W., Lee, W. K., & Hyun, D. S. (2004). Carrier-rotation strategy for voltage balancing in flying capacitor multilevel inverter. *IEE Proceedings Electric Power Applications*, 151(2), 239-248.
doi: 10.1049/ip-epa:20040220

Kazmierkowski, M. P., Jasinski, M., & Wrona, G. (2011). DSP-based control of grid-connected power converters operating under grid distortions. *IEEE Transactions on Industrial Informatics*, 7(2), 204-211.
doi: 10.1109/TII.2011.2134856

Kazmierkowski, M. P., & Malesani, L. (1998). Current control techniques for three-phase voltage-source PWM converters: a survey. *IEEE Transactions on Industrial Electronics*, 45(5), 691-703.
doi: 10.1109/41.720325

Keliang, Z., & Danwei, W. (2002). Relationship between space-vector modulation and three-phase carrier-based PWM: a comprehensive analysis. *IEEE Transactions on Industrial Electronics*, 49(1), 186-196.
doi: 10.1109/41.982262

Khersonsky, Y., Robinson, M., & Gutierrez, D. (1992). The HEXFRED^{TM} Ultrafast Diode in Power Switching Circuits. International Rectifier Application Note AN-989.

Kouro, S., Malinowski, M., Gopakumar, K., Pou, J., Franquelo, L. G., Bin, W., Rodriguez, J., Perez, M. A., Leon, J. I. (2010). Recent advances and industrial applications of multilevel converters. *IEEE Transactions on Industrial Electronics*, 57(8), 2553-2580.
doi: 10.1109/TIE.2010.2049719

Kouro, S., Rodriguez, J., Bin, W., Bernet, S., & Perez, M. (2012). Powering the future of industry: high-power adjustable speed drive topologies. *IEEE Industry Applications Magazine*, 18(4), 26-39.
doi: 10.1109/MIAS.2012.2192231

Lakshminarayanan, S., Kanchan, R. S., Tekwani, P. N., & Gopakumar, K. (2006). Multilevel inverter with 12-sided polygonal voltage space vector locations for induction motor drive. *IEE Proceedings Electric Power Applications*, 153(3), 411-419.
doi: 10.1049/ip-epa:20050444

Lakshminarayanan, S., Mondal, G., Tekwani, P. N., Mohapatra, K. K., & Gopakumar, K. (2007). Twelve-sided polygonal voltage space vector based multilevel inverter for an induction motor drive with common-mode voltage elimination. *IEEE Transactions on Industrial Electronics*, 54(5), 2761-2768.
doi: 10.1109/TIE.2007.899929

Larrinaga, S. A., Vidal, M. A. R., Oyarbide, E., & Apraiz, J. R. T. (2007). Predictive control strategy for DC/AC converters based on direct power control. *IEEE Transactions on Industrial Electronics*, 54(3), 1261-1271.
doi: 10.1109/TIE.2007.893162

Lee, S. J., Bae, H. S., & Cho, B. H. (2009). Modeling and control of the single-phase photovoltaic grid-connected cascaded H-bridge multilevel inverter. *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE 2009)*, 43-47.
doi: 10.1109/ECCE.2009.5316126

Leon, J. I., Portillo, R., Vazquez, S., Padilla, J. J., Franquelo, L. G., & Carrasco, J. M. (2008). Simple unified approach to develop a time-domain modulation strategy for single-phase multilevel converters. *IEEE Transactions on Industrial Electronics*, 55(9), 3239-3248.
doi: 10.1109/TIE.2008.928141

Leon, J. I., Vazquez, S., Sanchez, J. A., Portillo, R., Franquelo, L. G., Carrasco, J. M., & Dominguez, E. (2010). Conventional space-vector modulation techniques versus the single-phase modulator for multilevel converters. *IEEE Transactions on Industrial Electronics*, 57(7), 2473-2482.
doi: 10.1109/TIE.2009.2034674

Lesnicar, A., & Marquardt, R. (2003). An innovative modular multilevel converter topology suitable for a wide power range. *Proceedings of the IEEE Bologna Power Tech Conference*, 3, 1-6.
doi: 10.1109/PTC.2003.1304403

Liserre, M., Blaabjerg, F., & Hansen, S. (2005). Design and control of an LCL-filter-based three-phase active rectifier. *IEEE Transactions on Industry Applications*, 41(5), 1281-1291.
doi: 10.1109/TIA.2005.853373

Liserre, M., Dell'Aquila, A., & Blaabjerg, F. (2003). An overview of three-phase voltage source active rectifiers interfacing the utility. *Proceedings of the IEEE Bologna Power Tech Conference*, 3, 1-8.
doi: 10.1109/PTC.2003.1304405

Liu, H. L., Choi, N. S., & Cho, G. H. (1991). DSP based space vector PWM for three-level inverter with DC-link voltage balancing. *Proceedings of the International Conference on Industrial Electronics, Control and Instrumentation (IECON '91)*, 1, 197-203.
doi: 10.1109/IECON.1991.239306

Lixin, T., Limin, Z., Rahman, M. F., & Yuwen, H. (2004). A novel direct torque controlled interior permanent magnet synchronous machine drive with low ripple in flux and torque and fixed switching frequency. *IEEE Transactions on Power Electronics*, 19(2), 346-354.
doi: 10.1109/TPEL.2003.823170

Loh, P. C., Bode, G. H., Holmes, D. G., & Lipo, T. A. (2002). A time-based double band hysteresis current regulation strategy for single-phase multilevel inverters. *Proceedings of the 37th IAS Annual Meeting Industry Applications Conference*, 3, 1994-2001.
doi: 10.1109/IAS.2002.1043806

Lopez, O., Alvarez, J., Doval-Gandoy, J., & Freijedo, F. D. (2008). Multilevel multiphase space vector PWM algorithm. *IEEE Transactions on Industrial Electronics*, 55(5), 1933-1942.
doi: 10.1109/TIE.2008.918466

Lopez, O., Alvarez, J., Doval-Gandoy, J., & Freijedo, F. D. (2009). Multilevel multiphase space vector PWM algorithm with switching state redundancy. *IEEE Transactions on Industrial Electronics*, 56(3), 792-804.
doi: 10.1109/TIE.2008.2004390

Mahrous, E. A., Rahim, N. A., & Hew, W. P. (2007). Three-phase three-level voltage source inverter with low switching frequency based on the two-level inverter topology. *IET Electric Power Applications,* 1(4), 637-641.
doi: 10.1049/iet-epa:20060280

Malinowski, M. (2001). Sensorless control strategies for three-phase PWM rectifiers. (Doctoral dissertation, Warsaw University of Technology). Retrieved from http://www.isep.pw.edu.pl/icg/pdf/phd/mariusz_malinowski.pdf

Malinowski, M., Gopakumar, K., Rodriguez, J., Perez, M. A. (2010). A survey on cascaded multilevel inverters. *IEEE Transactions on Industrial Electronics*, 57(7), 2197-2206.
doi: 10.1109/TIE.2009.2030767

Malinowski, M., Jasinski, M., & Kazmierkowski, M. P. (2004). Simple direct power control of three-phase PWM rectifier using space-vector modulation (DPC-SVM). *IEEE Transactions on Industrial Electronics*, 51(2), 447-454.
doi: 10.1109/TIE.2004.825278

Malinowski, M., Kazmierkowski, M. P., Hansen, S., Blaabjerg, F., & Marques, G. D. (2001). Virtual-flux-based direct power control of three-phase PWM rectifiers. *IEEE Transactions on Industry Applications*, 37(4), 1019-1027.

doi: 10.1109/28.936392

Manjrekar, M. D., & Lipo, T. A. (1998). A hybrid multilevel inverter topology for drive applications. *Proceedings of the 13th Annual Applied Power Electronics Conference and Exposition, (APEC '98)*, 2, 523-529.
doi: 10.1109/APEC.1998.653825

Marchesoni, M., & Tenca, P. (2002). Diode-clamped multilevel converters: a practicable way to balance DC-link voltages. *IEEE Transactions on Industrial Electronics*, 49(4), 752-765.
doi: 10.1109/TIE.2002.801237

Mariethoz, S., & Rufer, A. (2004). New configurations for the three-phase asymmetrical multilevel inverter. *Proceeding of the 39th IEEE IAS Annual Meeting Industry Applications Conference*, 2, 828-835.
doi: 10.1109/IAS.2004.1348509

Marquardt, R. (2010). Modular multilevel converter: an universal concept for HVDC-networks and extended DC-bus-applications. *Proceedings of the International Power Electronics Conference (IPEC)*, 502-507.
doi: 10.1109/IPEC.2010.5544594

Marzoughi, A., Imaneini, H., & Moeini, A. (2013). An optimal selective harmonic mitigation technique for high power converters. *International Journal of Electrical Power & Energy Systems*, 49, 34-39.
doi: http://dx.doi.org/10.1016/j.ijepes.2012.12.007

Massoud, A. M., Finney, S. J., & Williams, B. W. (2008). Systematic analytical-based generalised algorithm for multilevel space vector modulation with a fixed execution time. *IET Power Electronics*, 1(2), 175-193.
doi: 10.1049/iet-pel:20060445

Mathew, J., Mathew, K., Azeez, N. A., Rajeevan, P. P., & Gopakumar, K. (2013). A hybrid multilevel inverter system based on dodecagonal space vectors for medium voltage IM drives. *IEEE Transactions on Power Electronics*, 28(8), 3723-3732.
doi: 10.1109/TPEL.2012.2227978

McGrath, B. P., & Holmes, D. G. (2002). Multicarrier PWM strategies for multilevel inverters. *IEEE Transactions on Industrial Electronics*, 49(4), 858-867.
doi: 10.1109/TIE.2002.801073

McGrath, B. P., Meynard, T., Gateau, G., & Holmes, D. G. (2007). Optimal modulation of flying capacitor and stacked multicell converters using a state machine decoder. *IEEE Transactions on Power Electronics*, 22(2), 508-516. doi: 10.1109/TPEL.2006.889932

Menzies, R. W., Steimer, P., & Steinke, J. K. (1994). Five-level GTO inverters for large induction motor drives. *IEEE Transactions on Industry Applications*, 30(4), 938-944. doi: 10.1109/28.297910

Mohan, N. (2003). *First course on power electronics and drives*. Minneapolis, MN: MNPERE.

Mohapatra, K. K., Gopakumar, K., Somasekhar, V. T., & Umanand, L. (2003). A harmonic elimination and suppression scheme for an open-end winding induction motor drive. *IEEE Transactions on Industrial Electronics*, 50(6), 1187-1198. doi: 10.1109/TIE.2003.819670

Mueller, O. M., & Park, J. N. (1994). Quasi-linear IGBT inverter topologies. Proceedings of the 9th Annual Applied Power Electronics Conference and Exposition (APEC '94), 1, 253-259. doi: 10.1109/APEC.1994.316391

Nabae, A., Takahashi, I., & Akagi, H. (1981). A new neutral-point-clamped PWM inverter. *IEEE Transactions on Industry Application*s, IA-17(5), 518-523. doi: 10.1109/TIA.1981.4503992

Napoles, J., Leon, J. I., Franquelo, L. G., Portillo, R., & Aguirre, M. A. (2009). Selective harmonic mitigation technique for multilevel cascaded H-bridge converters. *Proceedings of the 35th Annual Conference of IEEE Industrial Electronics (IECON '09)*, 806-811. doi: 10.1109/IECON.2009.5415023

Napoles, J., Watson, A. J., Padilla, J. J., Leon, J. I., Franquelo, L. G., Wheeler, P. W., & Aguirre, M. A. (2013). Selective harmonic mitigation technique for cascaded H-bridge converters with nonequal DC link voltages. *IEEE Transactions on Industrial Electronics*, 60(5), 1963-1971. doi: 10.1109/TIE.2012.2192896

Noguchi, T., Tomiki, H., Kondo, S., & Takahashi, I. (1998). Direct power control of PWM converter without power-source voltage sensors. *IEEE Transactions on Industry Applications*, 34(3), 473-479. doi: 10.1109/28.673716

Ozdemir, E., Ozdemir, S., & Tolbert, L. M. (2009). Fundamental-frequency-modulated six-level diode-clamped multilevel inverter for three-phase stand-alone photovoltaic system. *IEEE Transactions on Industrial Electronics*, 56(11), 4407-4415.
doi: 10.1109/TIE.2008.928096

Ozpineci, B., Tolbert, L. M., & Chiasson, J. N. (2004). Harmonic optimization of multilevel converters using genetic algorithms. *Proceedings of the IEEE 35th Annual Power Electronics Specialists Conference*, 5, 3911-3916.
doi: 10.1109/PESC.2004.1355167

Palanivel, P., & Dash, S. S. (2011). Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques. *IET Power Electronics*, 4(8), 951-958.
doi: 10.1049/iet-pel.2010.0332

Perez, M., Rodriguez, J., Pontt, J., & Kouro, S. (2007). Power distribution in hybrid multi-cell converter with nearest level modulation. *Proceedings of the IEEE International Symposium on Industrial Electronics (ISIE 2007)*, 736-741.
doi: 10.1109/ISIE.2007.4374688

Prats, M. M., Franquelo, L. G., Portillo, R., Leon, J. I., Galvan, E., & Carrasco, J. M. (2003). A 3-D space vector modulation generalized algorithm for multilevel converters. *IEEE Power Electronics Letters*, 1(4), 110-114.
doi: 10.1109/LPEL.2004.825561

Prats, M. M., Portillo, R., Carrasco, J. M., & Franquelo, L. G. (2002). New fast space-vector modulation for multilevel converters based on geometrical considerations. *Proceedings of the IEEE 28th Annual Conference of the Industrial Electronics Society (IECON 02)*, 4, 3134-3139.
doi: 10.1109/IECON.2002.1182898

Rahim, N. A., Chaniago, K., & Selvaraj, J. (2011). Single-phase seven-level grid-connected inverter for photovoltaic system. *IEEE Transactions on Industrial Electronics*, 58(6), 2435-2443.
doi: 10.1109/TIE.2010.2064278

Rahim, N. A., Elias, M. F. M., & Wooi Ping, H. (2013). Transistor-clamped H-bridge based cascaded multilevel inverter with new method of capacitor voltage balancing. *IEEE Transactions on Industrial Electronics*, 60(8), 2943-2956.
doi: 10.1109/TIE.2012.2200213

Ramkumar, S., Kamaraj, V., Thamizharasan, S., & Jeevananthan, S. (2012). A new series parallel switched multilevel dc-link inverter topology. *International Journal of Electrical Power & Energy Systems*, 36(1), 93-99.
doi: http://dx.doi.org/10.1016/j.ijepes.2011.10.028

Rashid, M. H. (2004). Power electronics circuits, devices and applications (3rd ed.). Upper Saddle River, NJ: Pearson Education, Inc.

Rech, C., & Pinheiro, J. R. (2007a). Hybrid multilevel converters: unified analysis and design considerations. *IEEE Transactions on Industrial Electronics*, 54(2), 1092-1104.
doi: 10.1109/TIE.2007.892255

Rech, C., & Pinheiro, J. R. (2007b). Impact of hybrid multilevel modulation strategies on input and output harmonic performances. *IEEE Transactions on Power Electronics*, 22(3), 967-977.
doi: 10.1109/TPEL.2006.890010

Rekioua, D., & Rekioua, T. (2005). A new approach to direct torque control strategy with minimization torque pulsations in permanent magnets synchronous machines. *Proceeding of the IEEE Russia Power Tech*, 1-6.
doi: 10.1109/PTC.2005.4524699

Renge, M. M., & Suryawanshi, H. M. (2008). Five-level diode clamped inverter to eliminate common mode voltage and reduce dv/dt in medium voltage rating induction motor drives. *IEEE Transactions on Power Electronics*, 23(4), 1598-1607.
doi: 10.1109/TPEL.2008.925423

Restrepo, J. A., Aller, J. M., Viola, J. C., Bueno, A., & Habetler, T. G. (2009). Optimum space vector computation technique for direct power control. *IEEE Transactions on Power Electronics*, 24(6), 1637-1645.
doi: 10.1109/TPEL.2009.2014953

Rodriguez, J., Bernet, S., Bin, W., Pontt, J. O., & Kouro, S. (2007). Multilevel voltage-source-converter topologies for industrial medium-voltage drives. *IEEE Transactions on Industrial Electronics*, 54(6), 2930-2945.
doi: 10.1109/TIE.2007.907044

Rodriguez, J., Bernet, S., Steimer, P. K., & Lizama, I. E. (2010). A survey on neutral-point-clamped inverters. *IEEE Transactions on Industrial Electronics*, 57(7), 2219-2230.
doi: 10.1109/TIE.2009.2032430

Rodriguez, J., Correa, P., & Moran, L. (2001). A vector control technique for medium voltage multilevel inverters. *Proceedings of the 16th Annual IEEE Applied Power Electronics Conference and Exposition (APEC 2001)*, 1, 173-178. doi: 10.1109/APEC.2001.911644

Rodriguez, J., Franquelo, L. G., Kouro, S., Leon, J. I., Portillo, R. C., Prats, M. A. M., & Perez, M. A. (2009). Multilevel converters: an enabling technology for high-power applications. *Proceedings of the IEEE*, 97(11), 1786-1817. doi: 10.1109/JPROC.2009.2030235

Rodriguez, J., Jih-Sheng, L., & Fang Zheng, P. (2002). Multilevel inverters: a survey of topologies, controls, and applications. *IEEE Transactions on Industrial Electronics*, 49(4), 724-738. doi: 10.1109/TIE.2002.801052

Rodriguez, J., Pontt, J., Correa, P., Cortes, P., & Silva, C. (2004). A new modulation method to reduce common-mode voltages in multilevel inverters. *IEEE Transactions on Industrial Electronics*, 51(4), 834-839. doi: 10.1109/TIE.2004.831735

Rodriguez, J., Pontt, J., Silva, C. A., Correa, P., Lezana, P., Cortes, P., & Ammann, U. (2007). Predictive current control of a voltage source inverter. *IEEE Transactions on Industrial Electronics*, 54(1), 495-503. doi: 10.1109/TIE.2006.888802

Rohner, S., Bernet, S., Hiller, M., & Sommer, R. (2010). Modulation, losses, and semiconductor requirements of modular multilevel converters. *IEEE Transactions on Industrial Electronics*, 57(8), 2633-2642. doi: 10.1109/TIE.2009.2031187

Sanmin, W., Bin, W., Fahai, L., & Congwei, L. (2003). A general space vector PWM control algorithm for multilevel inverters. *Proceedings of the 18th Annual IEEE Applied Power Electronics Conference and Exposition (APEC '03)*, 1, 562-568. doi: 10.1109/APEC.2003.1179268

Selvaraj, J., & Rahim, N. A. (2009). Multilevel inverter for grid-connected PV system employing digital PI controller. *IEEE Transactions on Industrial Electronics*, 56(1), 149-158. doi: 10.1109/TIE.2008.928116

Serpa, L. A. (2007). Current control strategies for multilevel grid connected inverters. (Doctoral dissertation, Swiss Federal Institute of Technology Zurich). Retrieved from http://www.pes.ee.ethz.ch/uploads/tx_ethpublications/Diss_Serpa.pdf

Serpa, L. A., Barbosa, P. M., Steimer, P. K., & Kolar, J. W. (2008). Five-level virtual-flux direct power control for the active neutral-point clamped multilevel inverter. *Proceedings of the IEEE Power Electronics Specialists Conference (PESC 2008)*, 1668-1674.
doi: 10.1109/PESC.2008.4592181

Serpa, L. A., Ponnaluri, S., Barbosa, P. M., & Kolar, J. W. (2007). A modified direct power control strategy allowing the connection of three-phase inverters to the grid through LCL filters. *IEEE Transactions on Industry Applications*, 43(5), 1388-1400.
doi: 10.1109/TIA.2007.904438

Serpa, L. A., Round, S. D., & Kolar, J. W. (2007). A virtual-flux decoupling hysteresis current controller for mains connected inverter systems. *IEEE Transactions on Power Electronics*, 22(5), 1766-1777.
doi: 10.1109/TPEL.2007.904213

Sirisukprasert, S., Jih-Sheng, L., & Tian-Hua, L. (2002). Optimum harmonic reduction with a wide range of modulation indexes for multilevel converters. *IEEE Transactions on Industrial Electronics*, 49(4), 875-881.
doi: 10.1109/TIE.2002.801226

Srikanthan, S., & Mishra, M. K. (2008). Constant frequency current control using a ramp comparison method for a DSTATCOM application. *Proceedings of the IEEE Region 10 Conference TENCON 2008*, 1-6.
doi: 10.1109/TENCON.2008.4766477

Sung-Jun, P., Feel-Soon, K., Man Hyung, L., & Cheul, U. K. (2003). A new single-phase five-level PWM inverter employing a deadbeat control scheme. *IEEE Transactions on Power Electronics*, 18(3), 831-843.
doi: 10.1109/TPEL.2003.810837

Tae-Jin, K., Dae-Wook, K., Yo-Han, L., & Dong-Seok, H. (2001). *T*he analysis of conduction and switching losses in multi-level inverter system. *Proceedings of the IEEE 32nd Annual Power Electronics Specialists Conference (PESC 2001)*, 3, 1363-1368.
doi: 10.1109/PESC.2001.954310

Tae-Won, C., & Meong-Kyu, C. (1996). Development of adaptive hysteresis band current control strategy of PWM inverter with constant switching frequency. *Proceedings of the 11th Annual Applied Power Electronics Conference and Exposition (APEC '96)*, 1, 194-199.
doi: 10.1109/APEC.1996.500442

Taghizadeh, H., & Hagh, M. T. (2010). Harmonic elimination of cascade multilevel inverters with nonequal DC sources using particle swarm optimization. *IEEE Transactions on Industrial Electronics*, 57(11), 3678-3684. doi: 10.1109/TIE.2010.2041736

Tekwani, P. N., Kanchan, R. S., & Gopakumar, K. (2007a). A dual five-level inverter-fed induction motor drive with common-mode voltage elimination and DC-link capacitor voltage balancing using only the switching-state redundancy-Part II. *IEEE Transactions on Industrial Electronics*, 54(5), 2609-2617. doi: 10.1109/TIE.2007.892634

Tekwani, P. N., Kanchan, R. S., & Gopakumar, K. (2007b). Novel current error space phasor based hysteresis controller using parabolic bands for control of switching frequency variations. *IEEE Transactions on Industrial Electronics*, 54(5), 2648-2656. doi: 10.1109/TIE.2007.899849

Tolbert, L. M., Fang Zheng, P., & Habetler, T. G. (1999). Multilevel converters for large electric drives. *IEEE Transactions on Industry Applications*, 35(1), 36-44. doi: 10.1109/28.740843

Tolbert, L. M., & Habetler, T. G. (1999). Novel multilevel inverter carrier-based PWM method. *IEEE Transactions on Industry Applications*, 35(5), 1098-1107. doi: 10.1109/28.793371

Vargas, R., Cortes, P., Ammann, U., Rodriguez, J., & Pontt, J. (2007). Predictive control of a three-phase neutral-point-clamped inverter. *IEEE Transactions on Industrial Electronics*, 54(5), 2697-2705. doi: 10.1109/TIE.2007.899854

Veenstra, M., & Rufer, A. (2005). Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives. *IEEE Transactions on Industry Applications*, 41(2), 655-664. doi: 10.1109/TIA.2005.844382

Villanueva, E., Correa, P., Rodriguez, J., & Pacas, M. (2009). Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems. *IEEE Transactions on Industrial Electronics*, 56(11), 4399-4406. doi: 10.1109/TIE.2009.2029579

Wang, G. P., Tan, Y. M., & Yi, L. Z. (2011). Research of multi-level inverter in PVMS of micro-grid. *Proceedings of the 2011 Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, 1-4. doi: 10.1109/APPEEC.2011.5748975

Wilkinson, R. H., Meynard, T. A., & Du Toit Mouton, H. (2006). Natural balance of multicell converters: the general case. *IEEE Transactions on Power Electronics*, 21(6), 1658-1666.
doi: 10.1109/TPEL.2006.882951

Yen-Shin, L., & Fu-San, S. (2004). Optimal common-mode voltage reduction PWM technique for inverter control with consideration of the dead-time effects-part I: basic development. *IEEE Transactions on Industry Applications*, 40(6), 1605-1612.
doi: 10.1109/TIA.2004.836149

Yi-Hung, L., & Ching-Ming, L. (2011). Newly-constructed simplified single-phase multistring multilevel inverter topology for distributed energy resources. *IEEE Transactions on Power Electronics*, 26(9), 2386-2392.
doi: 10.1109/TPEL.2011.2157526

Yiqiao, L., & Nwankpa, C. O. (1998). A new type of STATCOM based on cascading voltage source inverters with phase-shifted unipolar SPWM. *Proceedings of the 33rd IEEE IAS Annual Meeting Industry Applications Conference*, 2, 1447-1453.
doi: 10.1109/IAS.1998.730333

Yousefpoor, N., Fathi, S. H., Farokhnia, N., & Abyaneh, H. A. (2012). THD minimization applied directly on the line-to-line voltage of multilevel inverters. *IEEE Transactions on Industrial Electronics*, 59(1), 373-380.
doi: 10.1109/TIE.2011.2143373

Yousefpoor, N., Fathi, S. H., Farokhnia, N., & Sadeghi, S. H. (2009). Application of OHSW technique in cascaded multi-Level inverter with adjustable DC sources. P*roceedings of the International Conference on Electric Power and Energy Conversion Systems (EPECS '09)*, 1-6.

Yu, L., & Fang-Lin, L. (2008). Trinary hybrid 81-level multilevel inverter for motor drive with zero common-mode voltage. *IEEE Transactions on Industrial Electronics*, 55(3), 1014-1021.
doi: 10.1109/TIE.2007.909072

Yu, L., Hoon, H., & Huang, A. Q. (2009). Real-time calculation of switching angles minimizing THD for multilevel inverters with step modulation. *IEEE Transactions on Industrial Electronics*, 56(2), 285-293.
doi: 10.1109/TIE.2008.918461

Zambra, D. A. B., Rech, C., & Pinheiro, J. R. (2010). Comparison of neutral-point-clamped, symmetrical, and hybrid asymmetrical multilevel inverters. *IEEE Transactions on Industrial Electronics*, 57(7), 2297-2306. doi: 10.1109/TIE.2010.2040561

Zare, F., Zabihi, S., & Ledwich, G. (2007). An adaptive hysteresis current control for a multilevel inverter used in an active power filter. *Proceedings of the 2007 European Conference on Power Electronics and Applications*, 1-8. doi: 10.1109/EPE.2007.4417233

Zhong, D., Tolbert, L. M., Chiasson, J. N., & Ozpineci, B. (2006). A cascade multilevel inverter using a single DC source. *Proceedings of the 21st Annual IEEE Applied Power Electronics Conference and Exposition (APEC '06)*, 1-5. doi: 10.1109/APEC.2006.1620573

Zhu, H., Hao, J., Zhang, W., Pan, W., & Liu, X. (2008). Performance analysis and design of two magnetic flux oriented control systems for bearingless induction motors. *Proceedings of the27th Chinese Control Conference (CCC 2008)*, 145-149. doi: 10.1109/CHICC.2008.4605064

Zmood, D. N., & Holmes, D. G. (2003). Stationary frame current regulation of PWM inverters with zero steady-state error. *IEEE Transactions on Power Electronics*, 18(3), 814-822. doi: 10.1109/TPEL.2003.810852

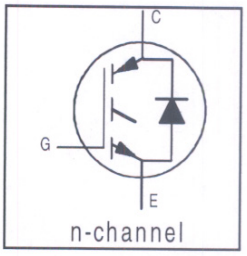
APPENDIX – DATASHEET

International
IOR Rectifier

PD - 94937

IRG4PC40UDPbF

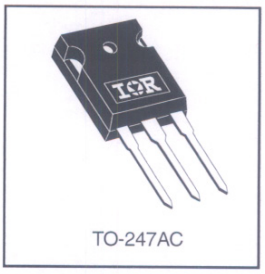
INSULATED GATE BIPOLAR TRANSISTOR WITH
ULTRAFAST SOFT RECOVERY DIODE



V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.72V

@V_{GE} = 15V, I_C = 20A



TO-247AC

Features

- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-247AC package
- Lead-Free

Benefits

- Generation -4 IGBT's offer highest efficiencies available
- IGBT's optimized for specific application conditions
- HEXFRED diodes optimized for performance with IGBT's. Minimized recovery characteristics require less/no snubbing
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBT's

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	40	A
I_C @ T_C = 100°C	Continuous Collector Current	20	
I_{CM}	Pulsed Collector Current ①	160	
I_{LM}	Clamped Inductive Load Current ②	160	
I_F @ T_C = 100°C	Diode Continuous Forward Current	15	
I_{FM}	Diode Maximum Forward Current	160	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	160	W
P_D @ T_C = 100°C	Maximum Power Dissipation	65	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	------	------	0.77	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	------	------	1.7	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	------	0.24	------	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	-----	-----	40	
Wt	Weight	------	6 (0.21)	------	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	----	----	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	----	0.63	----	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	----	1.72	2.1	V	I_C = 20A V_{GE} = 15V
		----	2.15	----		I_C = 40A See Fig. 2, 5
		----	1.7	----		I_C = 20A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	----	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	----	-13	----	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	11	18	----	S	V_{CE} = 100V, I_C = 20A
I_{CES}	Zero Gate Voltage Collector Current	----	----	250	µA	V_{GE} = 0V, V_{CE} = 600V
		----	----	3500		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	----	1.3	1.7	V	I_C = 15A See Fig. 13
		----	1.2	1.6		I_C = 15A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	----	----	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	----	100	150	nC	I_C = 20A
Qge	Gate - Emitter Charge (turn-on)	----	16	25		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	----	40	60		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	----	54	----	ns	T_J = 25°C
t_r	Rise Time	----	57	----		I_C = 20A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	110	165		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	----	80	120		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	----	0.71	----	mJ	diode reverse recovery.
E_{off}	Turn-Off Switching Loss	----	0.35	----		See Fig. 9, 10, 11, 18
E_{ts}	Total Switching Loss	----	1.10	1.5		
$t_{d(on)}$	Turn-On Delay Time	----	40	----	ns	T_J = 150°C, See Fig. 9, 10, 11, 18
t_r	Rise Time	----	52	----		I_C = 20A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	200	----		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	----	130	----		Energy losses include "tail" and
E_{ts}	Total Switching Loss	----	1.6	----	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	----	13	----	nH	Measured 5mm from package
C_{ies}	Input Capacitance	----	2100	----	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	----	140	----		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	----	34	----		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	----	42	60	ns	T_J = 25°C See Fig. I_F = 15A
		----	74	120		T_J = 125°C 14
I_{rr}	Diode Peak Reverse Recovery Current	----	4.0	6.0	A	T_J = 25°C See Fig.
		----	6.5	10		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	----	80	180	nC	T_J = 25°C See Fig.
		----	220	600		T_J = 125°C 16 di/dt 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	----	190	----	A/µs	T_J = 25°C
	During t_b	----	160	----		T_J = 125°C

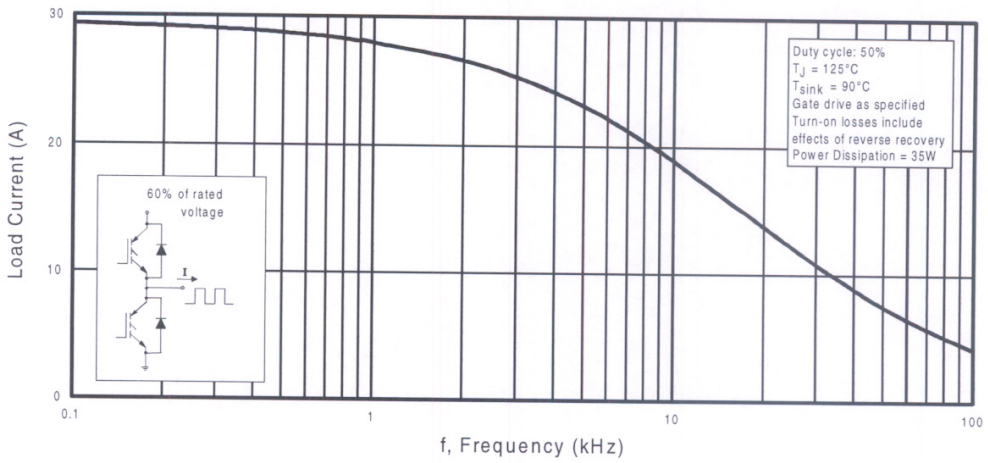


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

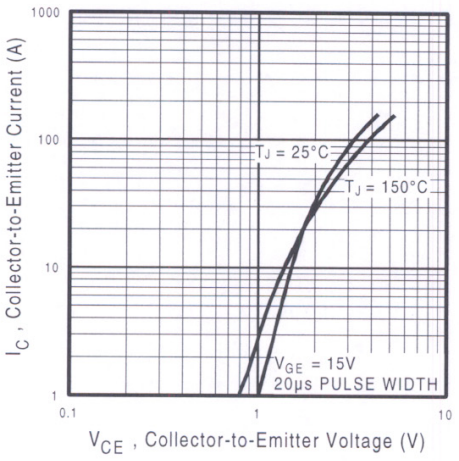


Fig. 2 - Typical Output Characteristics

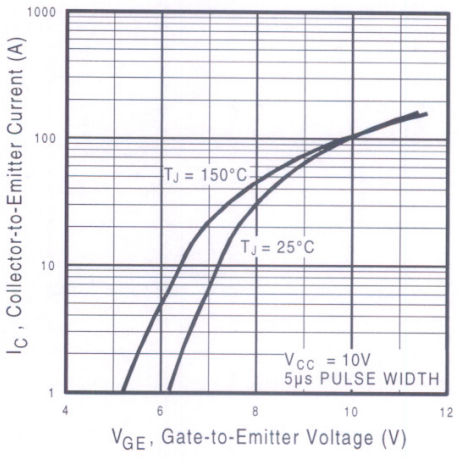


Fig. 3 - Typical Transfer Characteristics

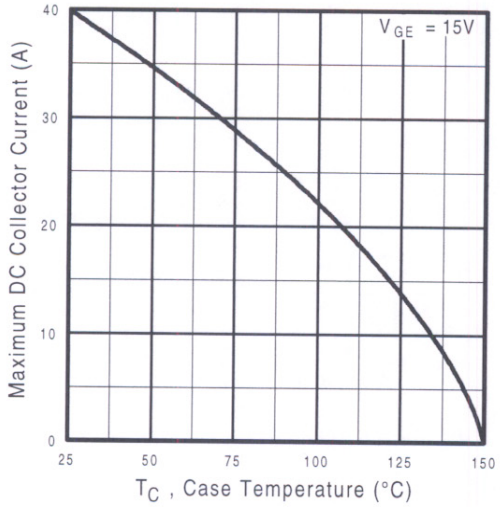


Fig. 4 - Maximum Collector Current vs. Case Temperature

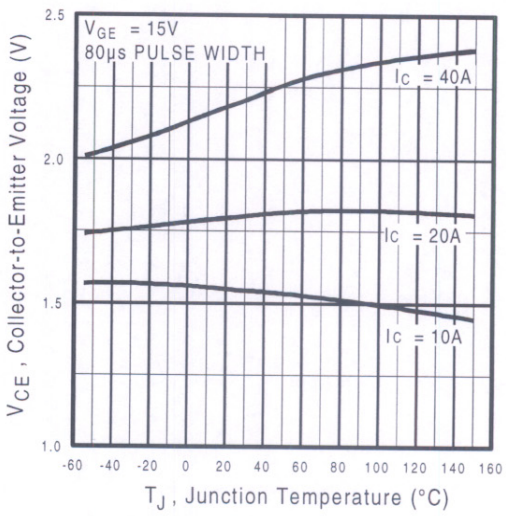


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

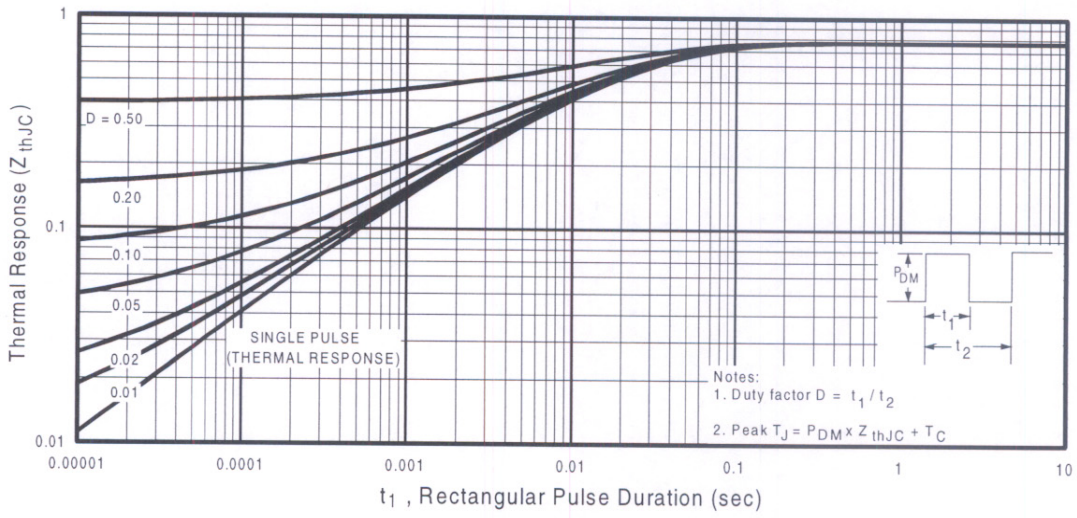


Fig. 6 - Maximum IGBT Effective Transient Thermal Impedance, Junction-to-Case

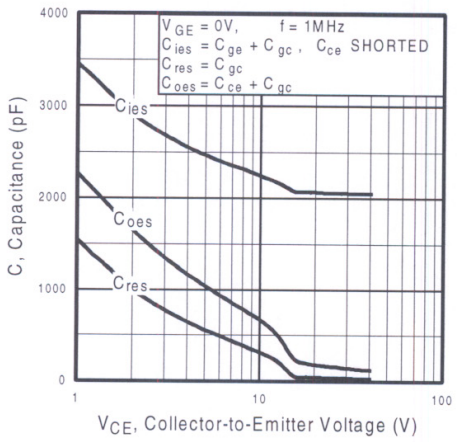


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

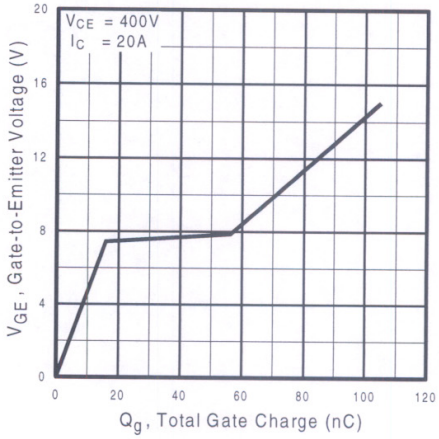


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

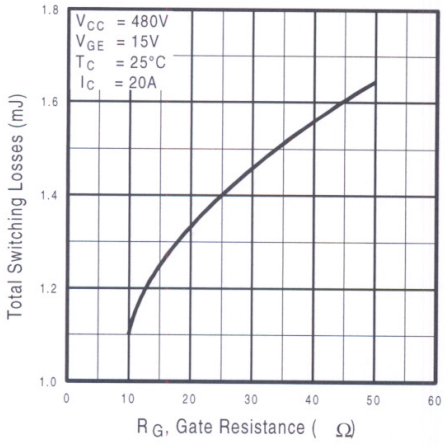


Fig. 9 - Typical Switching Losses vs. Gate Resistance

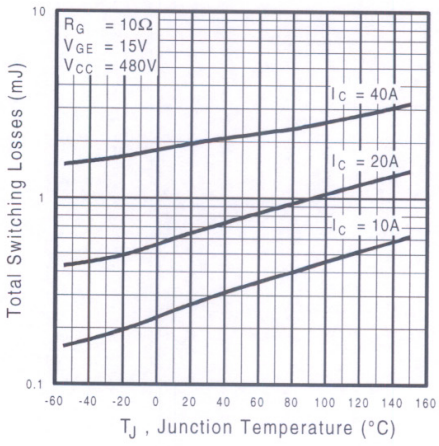


Fig. 10 - Typical Switching Losses vs. Junction Temperature

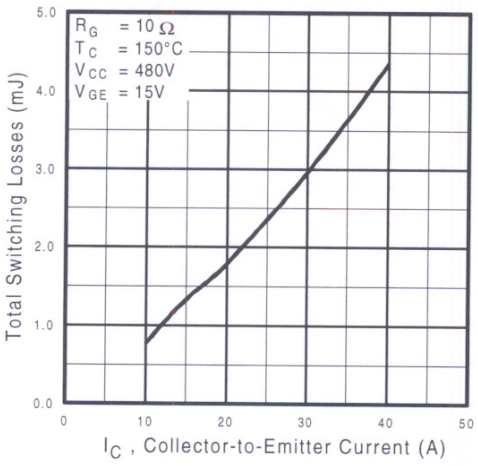


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

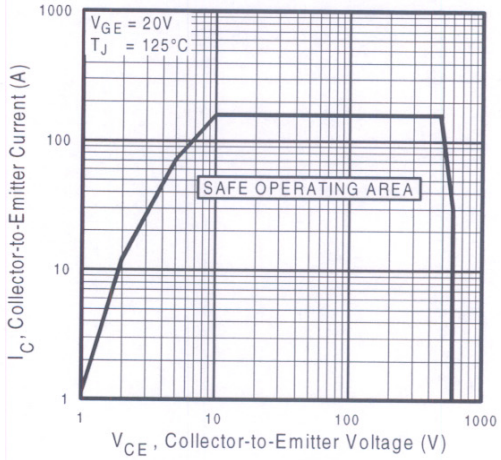


Fig. 12 - Turn-Off SOA

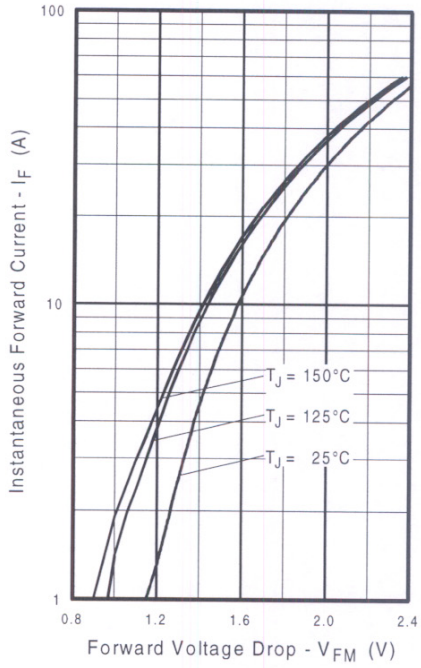


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

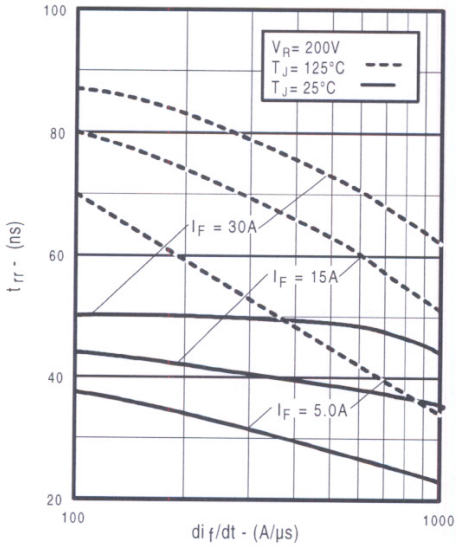


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

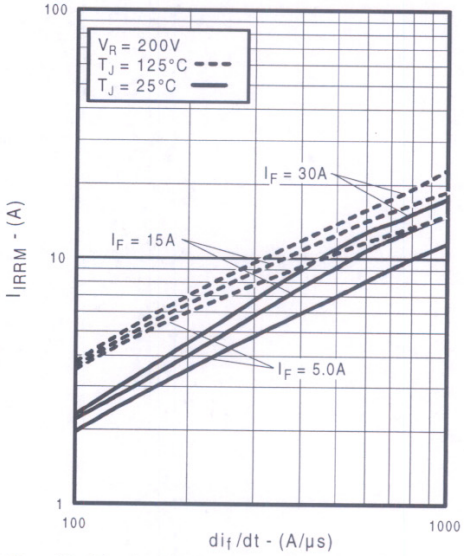


Fig. 15 - Typical Recovery Current vs. di_f/dt

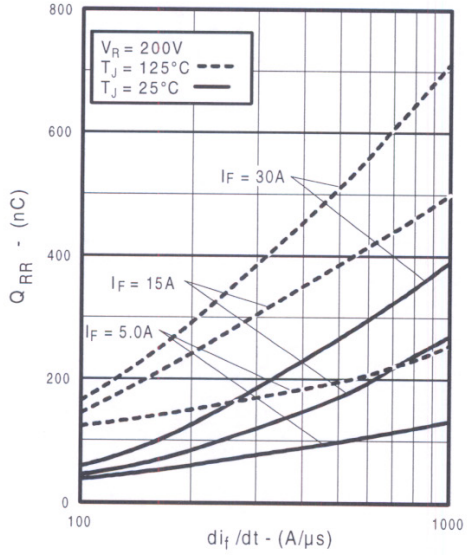


Fig. 16 - Typical Stored Charge vs. di_f/dt

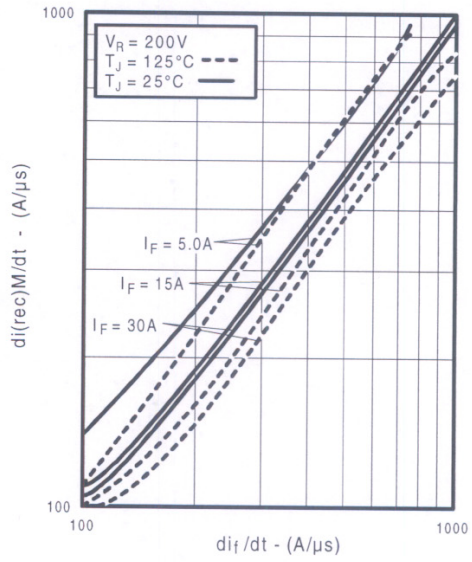


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

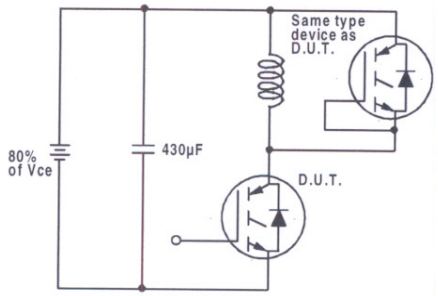


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

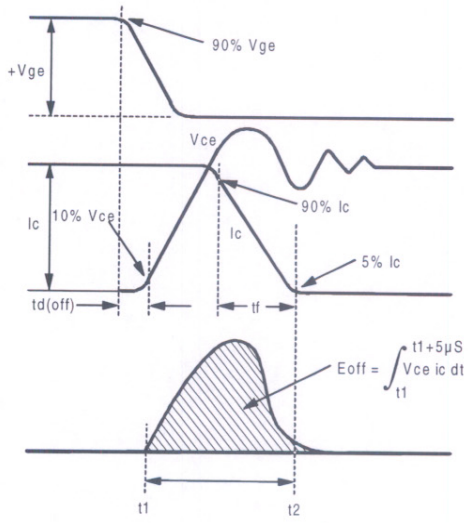


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

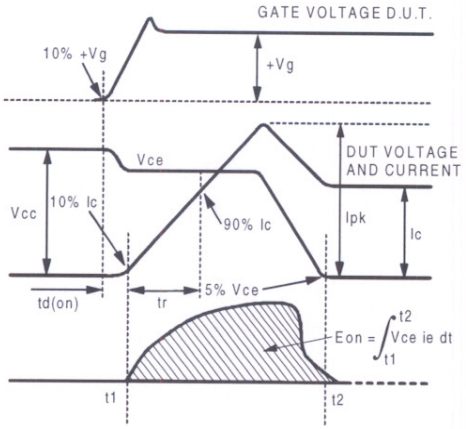


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

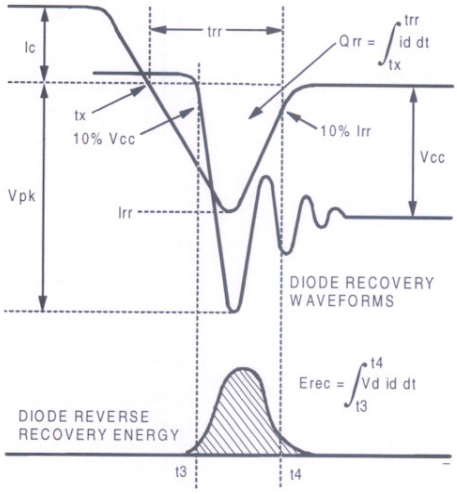


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

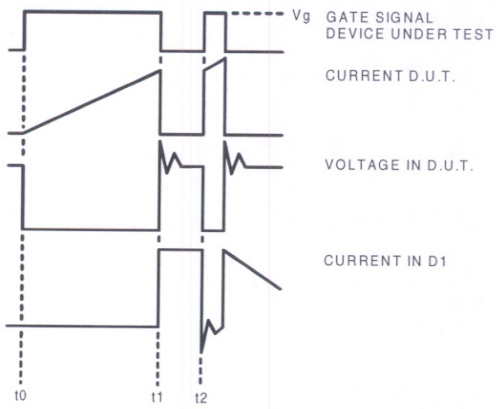


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

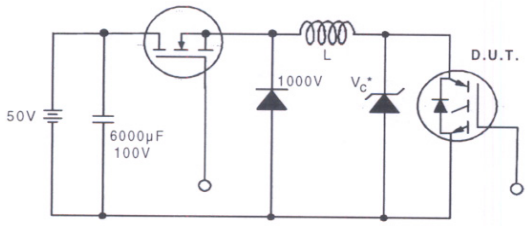


Figure 19. Clamped Inductive Load Test Circuit

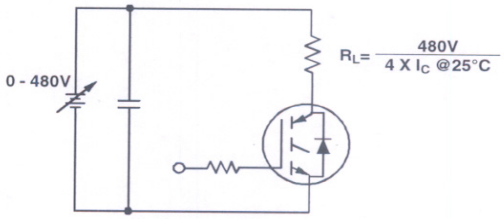
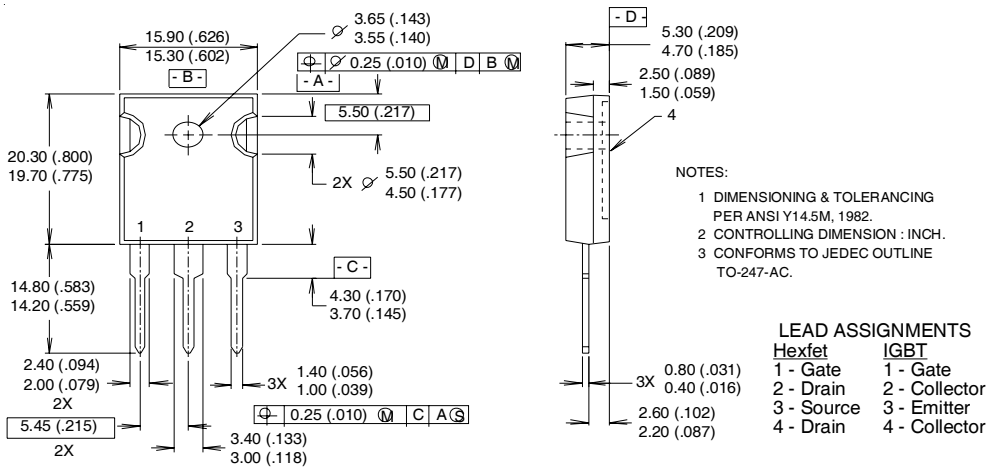


Figure 20. Pulsed Collector Current Test Circuit

TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-247-AC.

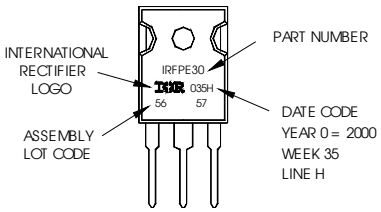
LEAD ASSIGNMENTS

Hexfet	IGBT
1 - Gate	1 - Gate
2 - Drain	2 - Collector
3 - Source	3 - Emitter
4 - Drain	4 - Collector

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2000
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position indicates "Lead-Free"



Notes:

① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10μH, R_G= 10Ω (figure 19)

③ Pulse width ≤ 80μs; duty factor ≤ 0.1%.

④ Pulse width 5.0μs, single shot.

Data and specifications subject to change without notice.

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.01/04

LIST OF PUBLICATIONS

Journals:

1. New Three-Phase Multilevel Inverter with Shared Power Switches

   Journal of Power Electronics, vol. 13, no. 5, September 2013, pp. 787-797.

2. An 11-Switch Multilevel Inverter with a Modified Space Vector Modulation

   Turkish Journal of Electrical Engineering and Computer Sciences, accepted for publication.

3. Multilevel Voltage Source Inverter with Optimized Usage of Bidirectional Switches

   IET Power Electronics, accepted for publication.

4. Switch-Sharing-Based Multilevel Inverter for Low Power Applications

   IEEE Transactions on Power Electronics, submitted for review.

Proceedings:

1. New-Topology Three-Phase Multilevel Inverter based on Modified Full-Bridge Topology

   2nd UMPEDAC Postgraduate Students Symposium, Malacca, Malaysia, 27-28 May 2011, pp. 60-64.

2. New Three-Phase Multilevel Voltage Source Inverter with Low Switching Frequency

   IEEE Region 10 Conference (TENCON) 2011, Bali, Indonesia, 22-24 November 2011, pp. 971-975.

3. A Three-Phase Five-Level Inverter with Switch-Sharing Capability

   2nd Power and Energy Conversion Symposium (PECS) 2014, Malacca, Malaysia, 12 May 2014, pp. 249-253.