CHAPTER 1

Introduction

1.1 Background

Growing world population together with the unquenchable thirst for technological advancement has resulted in a tremendous increase of global energy demand. The power industry has been encouraged to use renewable or alternative energy such as solar, wind, tidal etc. instead of conventional fuels. With the world population currently approaching 10 billion, future energy can be met by increasing alternative energy. It also helps alleviate concerns on growing environmental issues, increase of energy prices, reduction of energy availability and security. The use of renewable or alternative energy, rather than fossil fuel has led to positive consequences. Figure 1.1 shows the increase in worldwide energy production by source since 1970, with projections through 2025.

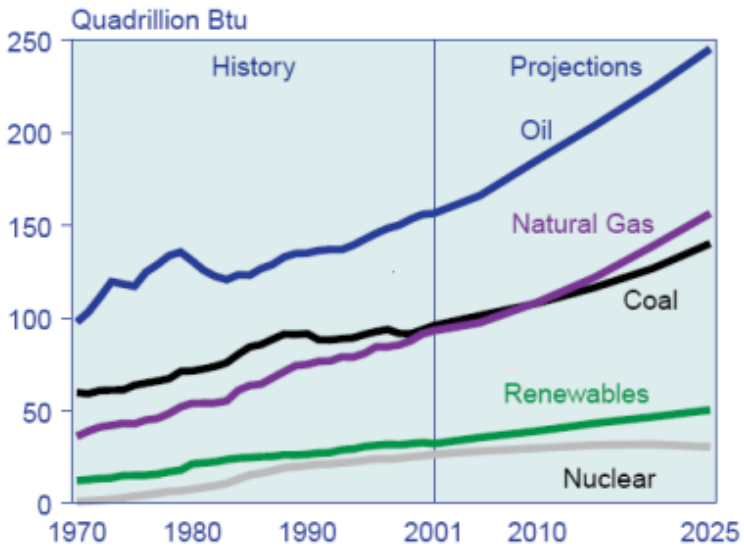


Figure 1.1 Growth of Worldwide Energy Production Since 1970 to 2025 (Wikipedia.org)

The economic and technical feasibility of renewable or alternative energy has extended to a large scale; however, they remain an expensive option. The production of renewable energy production has risen from 4225 TWh to 4447.5 TWh in the year 2011. This represents approximately 20.2% of the total global electricity production. Figure 1.2 shows the global fraction of renewable energy electricity production in 2011 (IEA International Energy Agency, 2010).

Photovoltaic energy sources are clean energy that allows independence and photovoltaics (PV) is the one of the technology that generates electric power. However, in most cases, PV deployment costs cannot compete with the initial installed direct cost of fossil sources of electrical generation.

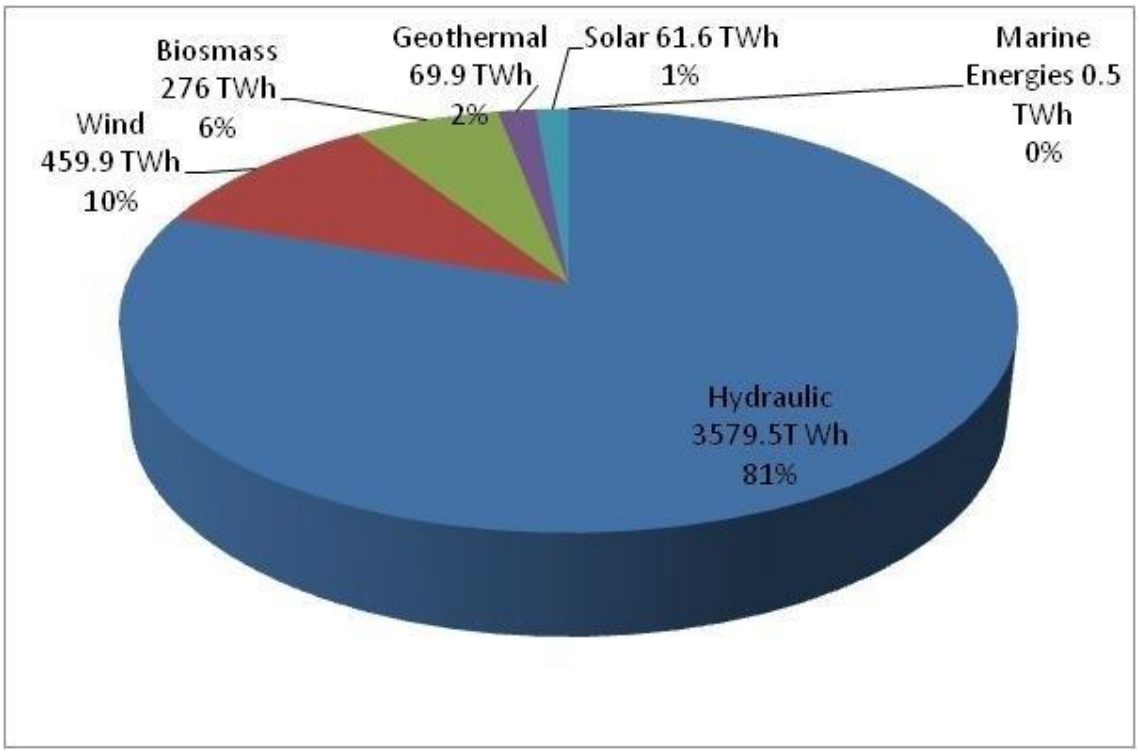


Figure 1.2: World total electricity production from renewable sources in 2011 (IEA International Energy Agency, 2010)

Solar photovoltaic (PV) technology has recorded an exponential growth for the past decade. Figure 1.3 shows the growing trend of PV capacity from 1995 until 2012. In 2012, the global capacity has reached a staggering milestone of 100 GW, ten times

the amount of capacity available five years earlier. 99% of this capacity is grid-connected.

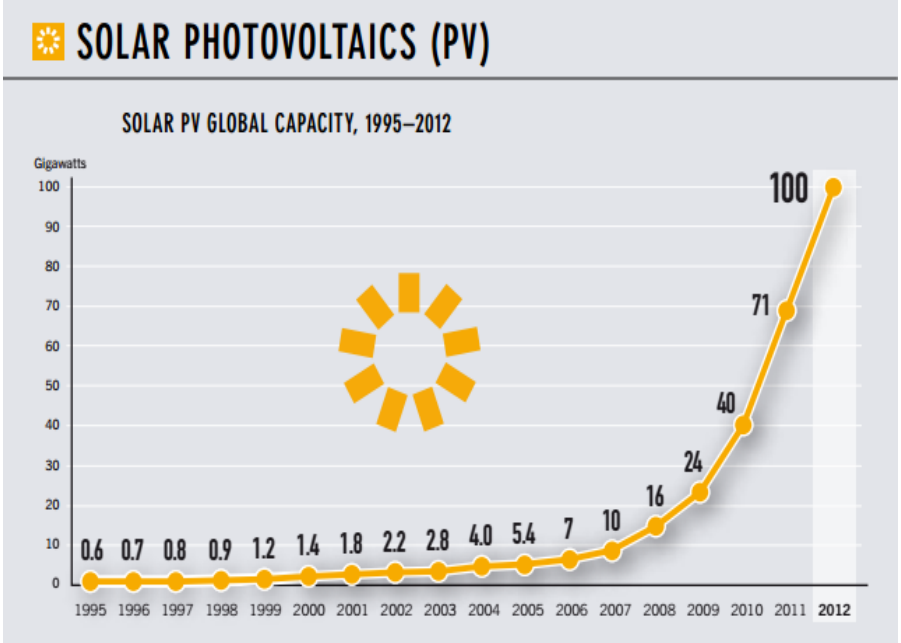


Figure 1.3: Solar PV global capacity 1995-2012 (REN21, 2013)

In solar PV system, power electronics is an enabling technology that plays an important part of solar PV energy generation as it influences the overall system efficiency and performance. Solar PV modules generate DC voltage and normally DC to AC power converter is used to convert it accordingly with regulated DC voltage and AC frequency synchronization. Due to irregular source of energy from the sun due to cloud, partial shading and blocking, maximum power point tracking (MPPT) is essential to maximize energy yields.

The most critical component of the photovoltaic system that enables the utilization of PV technology is the PV inverter, equipment that converts variable DC output from a PV system into a utility-based frequency AC output that can be supplied into the utility grid or utilized independently to supply off-grid loads. An inverter is used to convert from the photovoltaic DC power source to AC source that can be

connected to the grid. Figure 1.4 shows the world major inverter manufacturer in 2005 (Report Milestone, 2005).

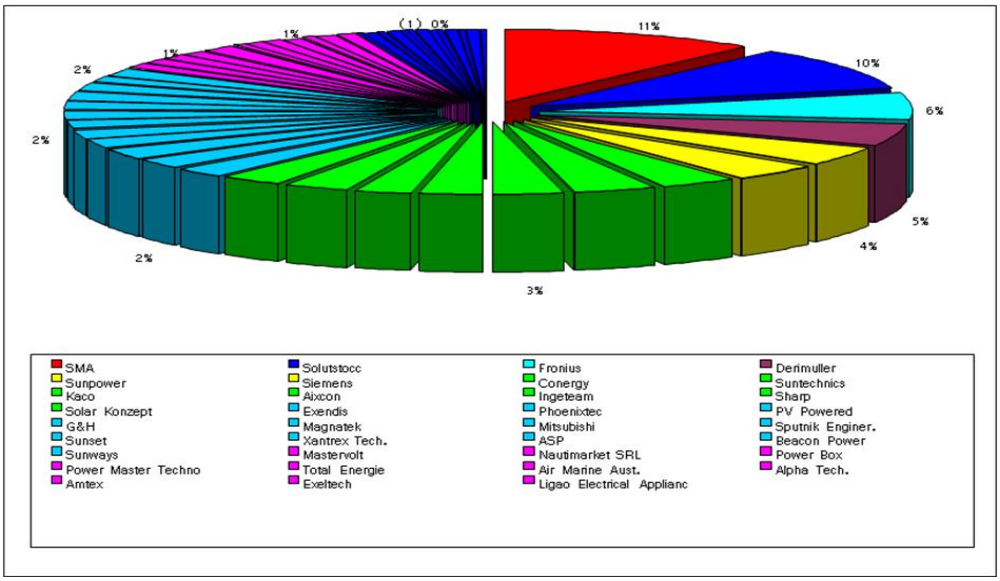


Figure 1.4: The world major inverter manufacturer in 2005 (Report Milestone, 2005)

In PV grid-connected applications, four different inverter system configurations have been widely developed; which are the centralized, string, multi-string and module-integrated inverter systems (Kjaer, et al., 2005; Li & Wolfs, 2008; Calais, et al., 2002; Kjaer, et al., 2002). The main benefit of the centralized inverter system technology is that it has a large number of PV modules interfaced to the grid (Calais, et al., 2002). However, the centralized inverter has several limitations. Most notable are high-voltage in the DC cable connecting the PV modules to the inverter, power losses because of the centralized MPPT and PV modules mismatch losses (Kjaer, et al., 2005). The drawback of the centralized inverter can be overcome with string, multi-string and module-integrated inverter (MII) system. Among these, the module-integrated inverter system has become the future trend for PV grid-connected system (Carrasco, at el., 2006; Kjaer, at el., 2005) due to a more efficient system since only one electrical device are integrated (Verhoeven, B., 1998).

Typically, the PV array voltage (V_{pv}) is in the range between 30 – 150 V (Calais, et al., 2002). However, the rms grid voltage (V_{grid}) is 220 V. Thus, the voltage adjustment element is required to realize the grid-connected function. In (Calais, et al., 2002; Kjaer, et al., 2002), the high-frequency transformer or line frequency transformer is included in the module-integrated inverter system to step-up the inverter output voltage (V_{ab}) to above $\sqrt{2}$ of grid voltage (V_{grid}). Nevertheless, these transformers have the disadvantages of increases larger, heavier and more expensive. In addition, when the transformer is eliminated under the same module-integrated inverter (MII) condition system, the efficiency can possibly be increased by 1%-2% (see Figure 1.5).

In order to increase efficiency, while reducing the dimensions, weight and cost of a PV grid-connected MII system, the transformerless MII system is employed. Direct connection between the PV sources and the grid in non-isolated systems may result in additional ground leakage currents because of the parasitic capacitance of the PV module (Huafeng & Shaojun, 2010; Myrzik & Calais, 2003; Cavalcanti, et al., 2010; Lopez, et al., 2010). For this to be done, the isolation capability and safety issues should be considered correctly. With reference to the German standard, VDE0126-1-1, the amplitude of ground leakage current must be less than 300 mA_{rms} to avoid electrical hazard when the PV array is touched (Myrzik & Calais, 2003). In addition, the high amplitude of ground leakage current can disturb the grid's current and produce additional losses in whole system (Cavalcanti, et al., 2010; Lopez, et al., 2010).

The fluctuating common-mode voltage at the output of a high switching power inverter terminal causes high ground leakage current in transformerless PV grid-connected system. In addition, the fluctuation of common-mode voltages will increase the voltage stress dv/dt of power semiconductor devices and reduce the lifetime of the device (Lopez, et al. 2010; Essakiappan, et al., 2011). Due to the above problems, the proposed transformerless inverter topologies are proposed in this thesis.

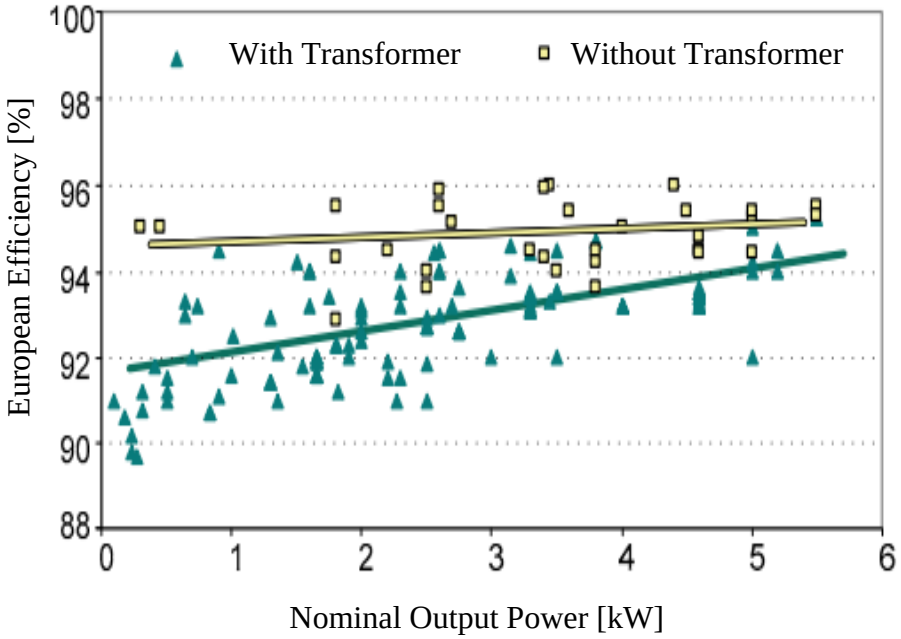


Figure 1.5: The effect of isolating transformers to European inverter efficiency (Schlumberger, 2007)

1.2 Objectives

The objectives of research work are:

1) To design, develop and compare six different types of boost converters suitable for a PV transformerless H-Bridge PWM inverter with high gain DC voltage conversion ratio and high efficiency.
2) To develop a hardware prototype and analyse the performance of the proposed suitable boost converter with the bipolar and proposed modified unipolar single-phase PV transformerless grid-connected H-Bridge inverter. The balancing power transfer algorithm is implemented to maximise PV power transfer to the grid. Ground leakage current and constant common-mode voltage reduction has been analysed.
3) To compare the single-stage inverter of proposed SC-HB inverter, the conventional unipolar H-Bridge inverter, the bipolar H-Bridge inverter and the

HB-ZVR inverter topology in term of THDi, common-mode voltage and reduction of ground leakage current.

4) To compare the percentage of THDi, constant common-mode voltage and ground leakage current with two-stage converter of the proposed modified unipolar H-Bridge inverter with CD-Boost converter, proposed bipolar H-Bridge inverter with CD-Boost converter, and proposed modified unipolar H-Bridge inverter with modified boost converter.

1.3 Methodology and Scope of Study

This thesis uses simulation and experimentation as the main tools to assess and validate the technical viability of each modulation strategy, six different types of DC-to-DC boost converters, and seven different types of DC to AC converters of the single-phase grid- connected transformerless PV inverter. The performance of the proposed suitable DC-DC converter with the bipolar and proposed modified unipolar H-Bridge single-phase PV transformerless grid-connected inverter are analyse further. The balancing power transfer algorithm is implemented to maximise power transfer to the grid. Ground leakage current and constant common-mode voltage reduction has been analysed.

Despite control system, maximum power point tracking and passive anti-islanding technique not forming the main core of this thesis, significant effort has been devoted to the presentation of the PV grid-connected inverter systems needed to facilitate safe operation of the experimental setups. Systematic approach of the control, maximum power point tracking and passive anti-islanding structure and design is presented appropriately.

1.4 Thesis Organization

The motivation of this research is to investigate the performance of single-phase transformerless PV grid-connected system. The thesis is organized into seven chapters.

Chapter 1 gives an overview of the research, highlighting the problems intended to be solved, the objectives and the research outline.

Chapter 2 presents the solar PV system, which includes the PV module behaviour, PV inverter connection system, PV inverter system, MPPT algorithm, protection for grid-connected PV inverter, power quality issues and performance PV inverter issues.

Chapter 3 describes an overview of the power converter PV system. The fundamentals of isolated DC-DC converter are presented. The single-phase PV inverter topologies with and without transformer elements are also described in this chapter. The modelling of common-mode voltage in the H-Bridge transformerless inverter circuit is discussed in this chapter. In addition, the modification to the transformerless H-Bridge circuit that includes ac-bypass and dc-bypass topologies are reviewed in this chapter together with a discussion on the performance of various transformerless H-Bridge inverter circuits.

Chapter 4 describes various new single-phase configurations of transformerless inverter. The detailed operation of the proposed circuits which includes the SC-HB inverter, bipolar H-Bridge inverter with CD-Boost converter, modified unipolar H-Bridge inverter with CD-Boost converter and modified unipolar H-Bridge inverter with modified boost converter are discussed in this chapter.

Chapter 5 describes the simulation of various proposed transformerless inverter topologies. This chapter also simulates the ground leakage current performance of the H-Bridge inverter with hybrid, unipolar and bipolar SPWM techniques. In this chapter

the high gain boost converter with H-Bridge inverters are simulated. The proposed minimal input ripple converter is also implemented using the simulation tool.

Chapter 6 describes the experimental results of the proposed PV transformerless inverter topologies. The comparison between conventional power converter and proposed power converter in terms of common-mode voltage, ground leakage current, ripple input dc current and their efficiency are discussed. The control algorithm of the proposed topologies is implemented using TMS32F2812DSP. The influence of filter configuration, the matching ratio of inductor filter between line and neutral of the grid is analysed in this chapter. The significance of the value of PV parasitic capacitance on the ground leakage is also studied.

Chapter 7 concludes the thesis with recommendations of future work. The author's contributions are listed in this chapter.

CHAPTER 2

Solar PV systems

2.1 Introduction

This chapter presents the types of PV modules available in the market and PV inverter connection systems which cover stand-alone, grid-connected and hybrid systems. This is then followed by an overview of several categories of PV inverter systems. The protection for grid-connected PV inverter is presents in a sub-chapter of islanding and anti-islanding. Performance of PV inverter system will be presented in last section of this chapter.

2.2 Photovoltaic Module

Photovoltaic modules consist of a string of PV cells connected in series and sealed for protection. They are at the heart of PV systems. The modules are than put into panels and can be configured into arrays for standard application. The diagram that represents these stages is shown in Figure 2.1. With silicon, single cell open-circuit voltages are typically close to 0.6 V, and maximum power voltage are close to 0.5 V at 25^0C (Messenger & Ventre, 2010). A PV panel is made up of several modules assembled together. A PV array is a combination of series and parallel connected modules set to produce the desired voltage and current.

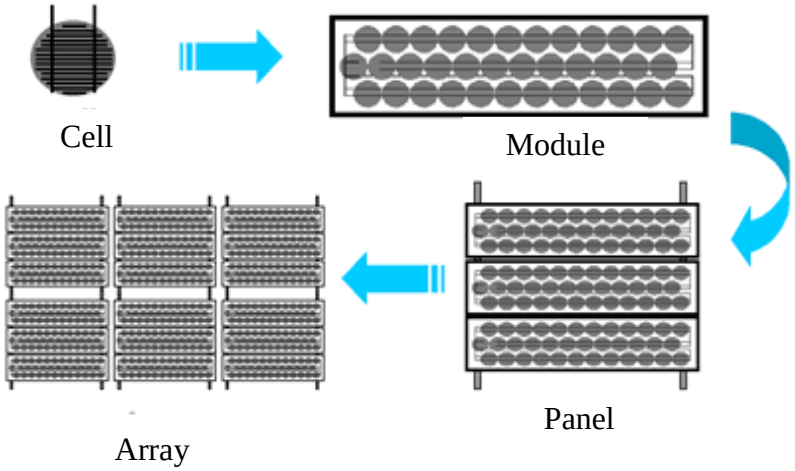


Figure 2.1: Photovoltaic cells, modules, panels and arrays

2.2.1 Types of PV Cell

The general types of silicon PV cell are shown in Figure 2.2. Commonly, there are three types of PV cell technology such as monocrystalline (single) silicon PV cell, polycrystalline (multi-crystalline) silicon PV cells and amorphous or thin film (Sulaiman et al., 2010).

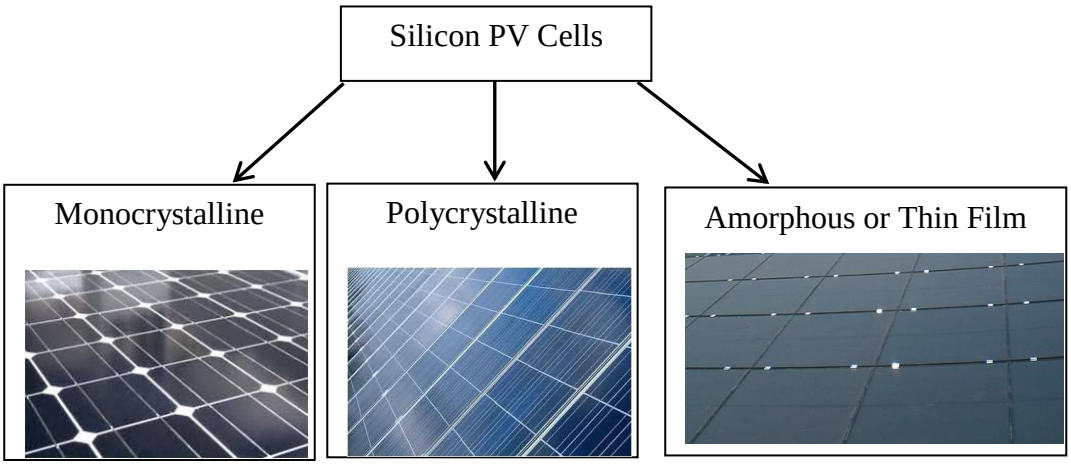


Figure 2.2: Types of Silicon PV Cells

Several manufactures are involved with other variations of crystalline cell types such as (Sulaiman et al., 2010):

a) Polycrystalline power silicon cells;

b) Ribbon-drawn silicon cells and crystalline silicon thin film cells;

c) Polycrystalline EFG silicon cells;

d) Polycrystalline String-Ribbon silicon cells;

e) Monocrystalline Dendrite-Web silicon cells;

f) Polycrystalline APEC cells.

The amorphous or thin film is another type of cell technology. The structure of this cell does not have a crystal lattice. This cell technology uses the condensation process of gaseous silicon to create cells. The arrangements of the atoms are completely in random fashion without an orderly crystalline structure (Sulaiman et al, 2010). On the other hand, the solid crystalline uses the wafer process (Messenger & Ventre, 2010). Therefore, thin-film photovoltaic has the potential for cost reduction in terms of material and manufacturing prices.

2.2.2 Operation of PV Cell

A photovoltaic (PV) cell operation requires three underlying factors:

1. Light absorption that triggers the creation of either electron-hole pairs or excitons;
2. Charge carriers separation between the proton and electron;
3. Separate carriers extraction to an external circuit.

2.2.3 PV Modules Behaviour

By connecting PV cell physically and electrically, they form a solar module. The PV module circuit diagram is presented in Figure 2.3. The electrical (current-voltage) behaviour of a single module is presented in characteristic curve form as shown in Figure 2.4 (Sulaiman et al., 2010). The figure plots the current-voltage (I-V) output characteristic of a PV module at a particular irradiance and temperature. These current-voltage operating points are plotted with the short-circuit current (I_{sc}) and open-circuit voltage (V_{oc}) of the PV module as the y-axis and x-axis limits respectively, known as

the I-V curve. The short-circuit current is produced by device at maximum current and zero voltage, while the open-circuit voltage is produced during zero current and maximum voltage. Maximum power point of a PV system occurs at somewhere around the knee of the I-V curve. When the PV device delivers its maximum power output and operates at its highest efficiency, the point is referred as the maximum power point (P_{mp}).

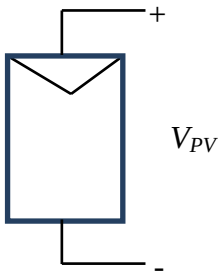


Figure 2.3: Representation of PV modules in circuit diagram

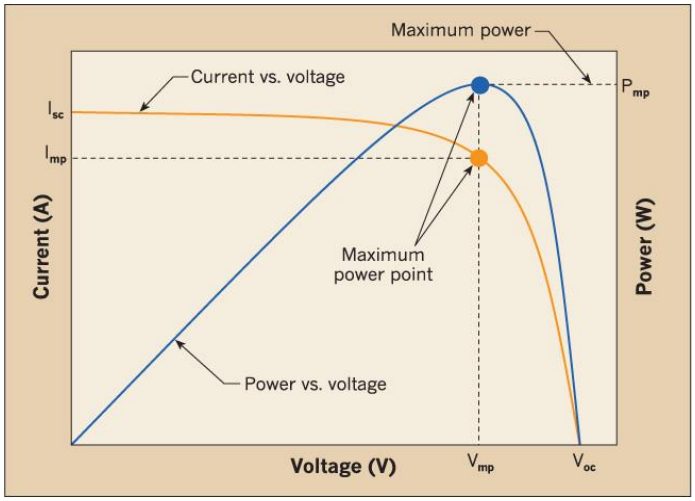


Figure 2.4: Single PV module characteristic curve

Since the module is often too small to be used in many practical applications, a combination of modules in series and parallel are needed. The combination consists of series, parallel and series parallel arrangement of same characteristic of PV modules (same short circuit current and same open circuit voltage) to prevent mismatch problem.

Mismatch losses occurs when modules with different properties and manufacturing conditions are connected together.

2.2.3.1 Series PV Modules

Figure 2.5 shows the PV modules connection in series. The series string is the resultant of the group of PV modules. For example of two modules connected in series, the current through the two modules is the same (I_{PV}). The total voltage (V_{PV}) produced is the sum of the individual module voltages (V_1 and V_2). For modules in series, the I-V curve characteristic is as shown in Figure 2.6 (Solanki, 2011). The dashed line represents the single PV module, while solid line represents the two series PV modules. From the Figure 2.6, the combination of two series PV module will add the V_{oc} and the current (I_{sc}) through of two series modules will be same.

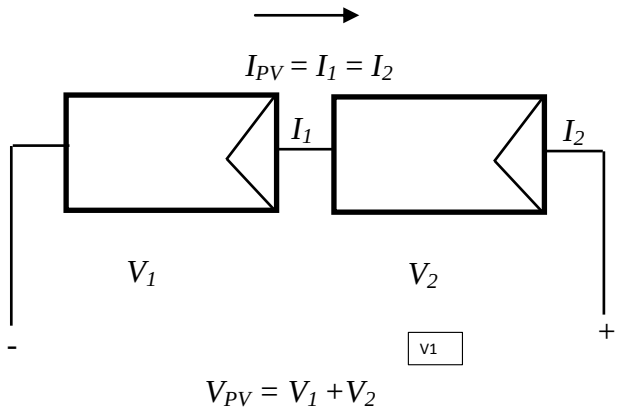


Figure 2.5: Series connection of PV modules

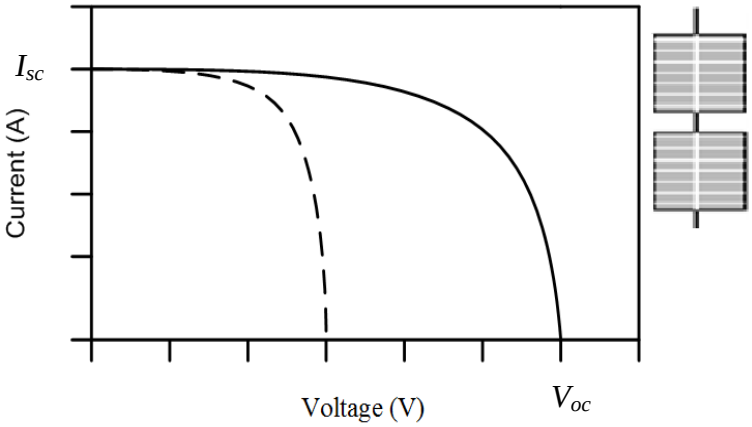


Figure 2.6: Series PV module connection IV curve

2.2.3.2 Parallel PV Modules

To boost the current output in the PV system, the parallel PV modules is required. The connection of parallel PV modules is shown in Figure 2.7.

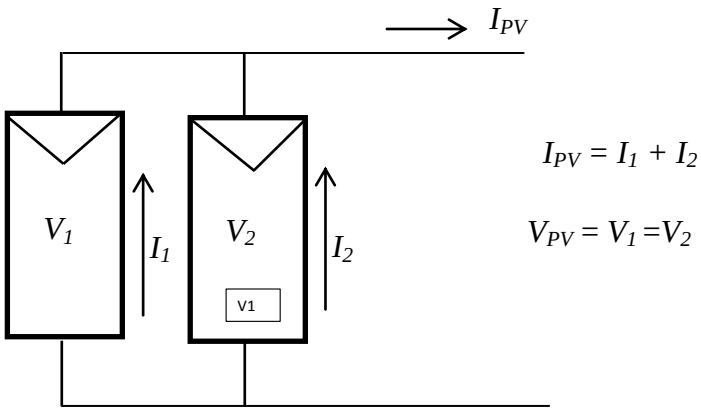


Figure 2.7: Parallel connection of PV modules

Since the PV module is connected in parallel, the total output of the PV module current (I_{PV}) is produced by summing the individual PV module current (I_1, I_2) while the total PV module voltage (V_{PV}) is a same. Figure 2.8 shows the resultant I-V curve characteristic of parallel PV modules connection (Solanki, 2011).

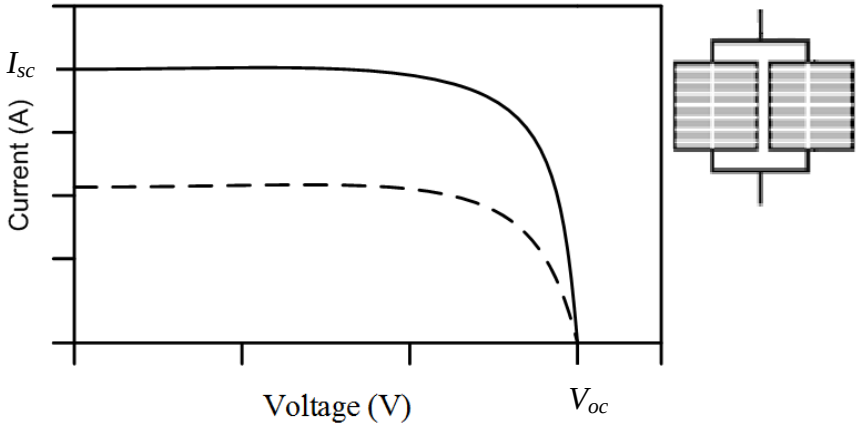


Figure 2.8: I-V Parallel PV modules curve

When two modules are connected in parallel, the current flows from the two modules will be added while the voltage of the modules combination will remain the same as that of a single PV module.

2.2.3.3 Series-Parallel PV Modules

To increase the voltage and current of PV source, the series-parallel PV modules configuration is required. Figure 2.9 shows the schematic diagram of this configuration for such PV module, which have combination of two PV modules in series and two such series in parallel.

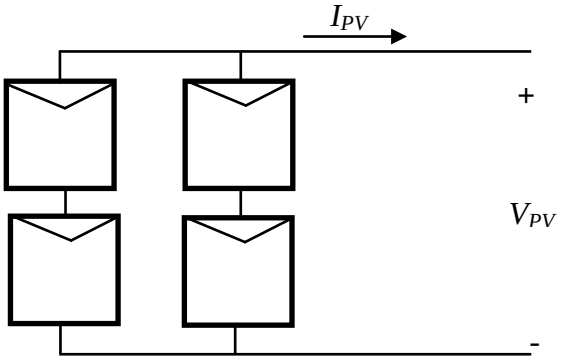


Figure 2.9: Series-parallel connection of PV module

Figure 2.10 shows the I-V curve of series-parallel configuration. The combination of this configuration will increase the open circuit voltage and short circuit current compared to single PV module.

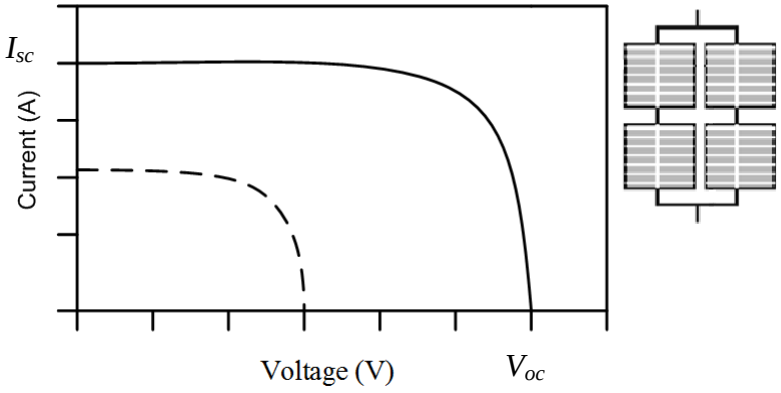


Figure 2.10: I-V curve for series-parallel configuration (Chetan, 2011)

2.3 PV Inverter Connection Systems

Generally, PV inverter connection system can be mostly classified into the three types;

1. Stand-alone or independent system;
2. Grid-connected system;
3. Hybrid system.

2.3.1 Stand Alone System

The stand-alone system type operates autonomously and supplies power to electrical loads independent from the electric utility. Photovoltaic cells, batteries, photovoltaic controller and inverter constitute a stand-alone PV generating system as shown in Figure 2.11. This system is often the series connection between PV array and battery via a DC-DC converter. For AC loads, the step-up inverter converts DC power from the battery to AC power. There are three general ways to connect the system and utilise the PV power source. They are PV direct conversion, PV interactive conversion and PV on-line conversion, shown in Figure 2.12, Figure 2.13 and Figure 2.14 respectively (Wai, et al., 2007; Masoum, et al., 2004; Vazquez, et al., 2008; Mazumder, et al., 2008). To optimize the battery charging efficiency and management, the PV parallel conversion is proposed in (Wang & Zhang, 2010) as in Figure 2.15.

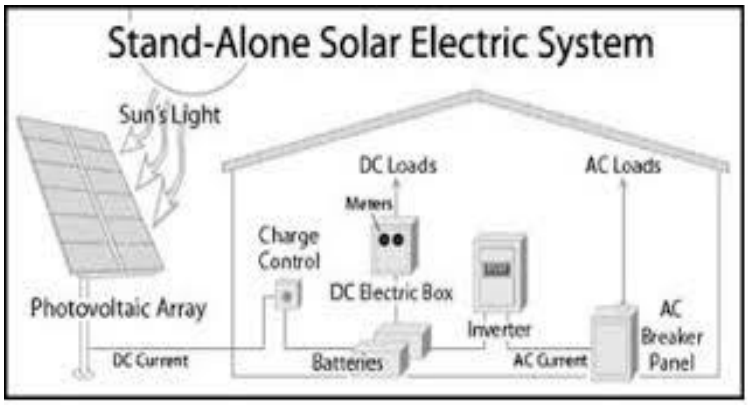


Figure 2.11: Stand-alone PV system (Chetan, 2011)

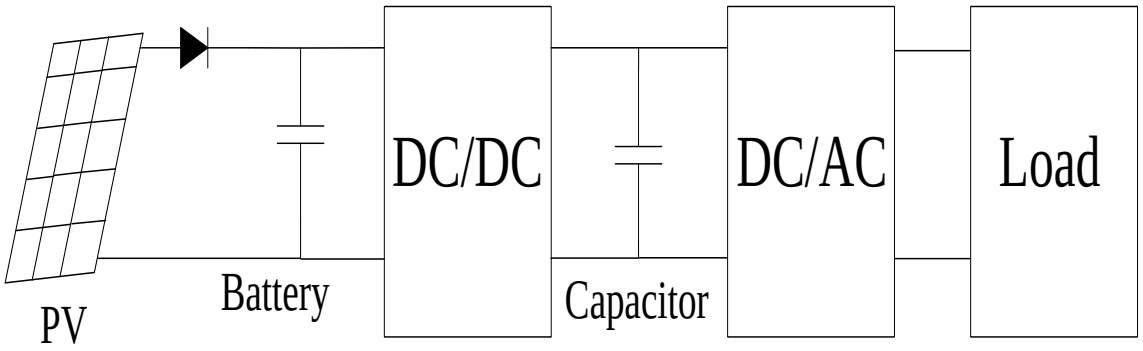


Figure 2.12: PV direct conversion

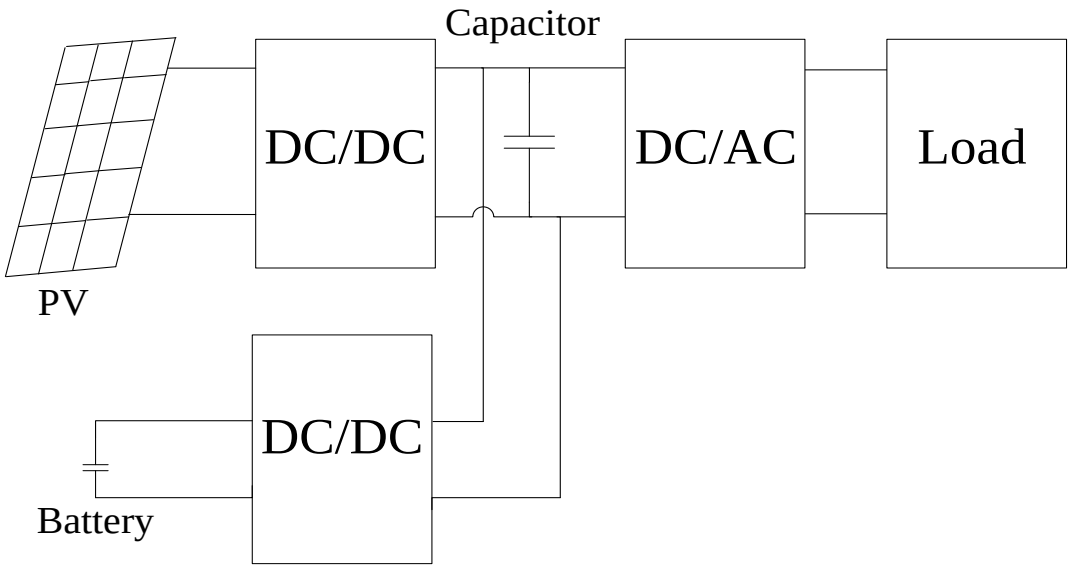


Figure 2.13: PV interactive conversion

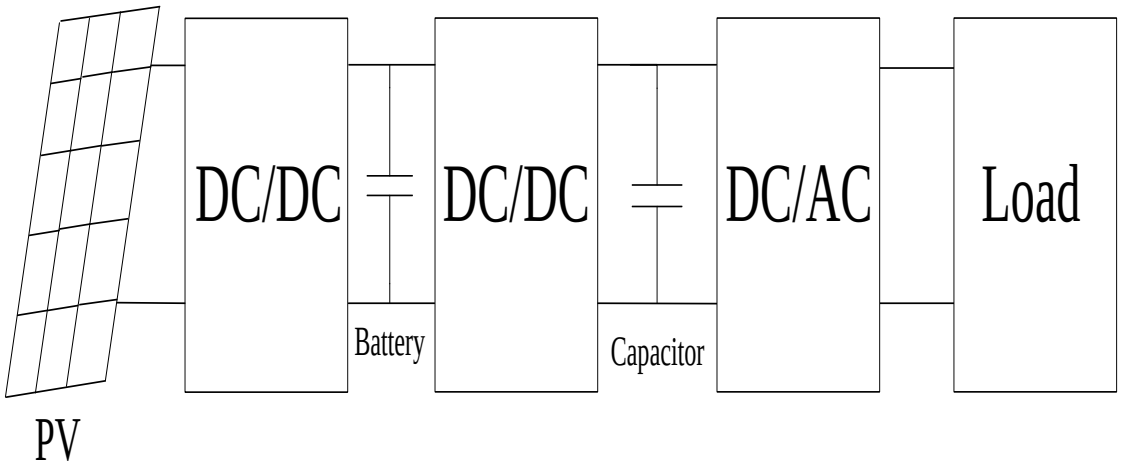


Figure 2.14: PV on-line conversion

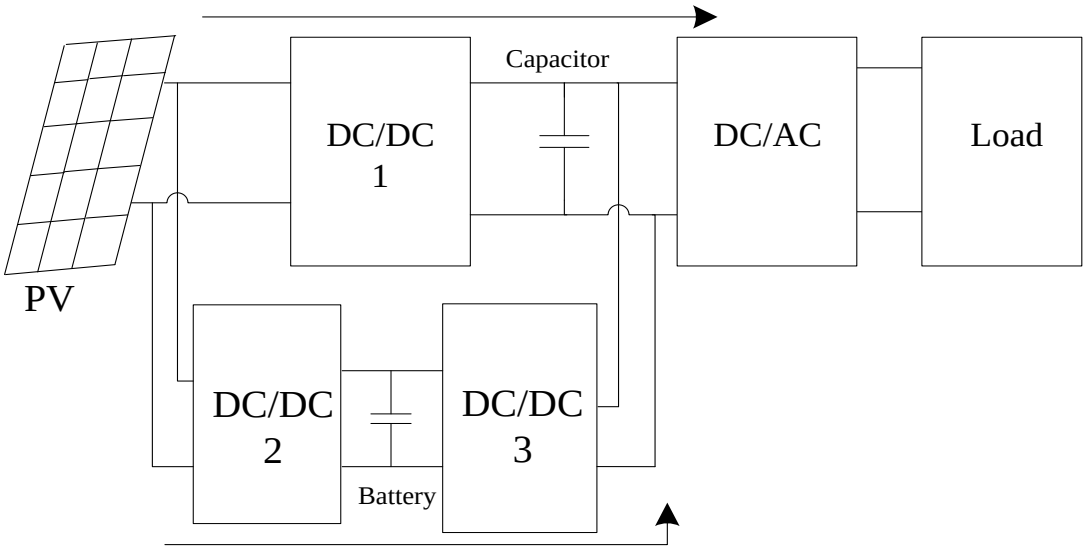


Figure 2.15: PV parallel coordinated conversion

2.3.2 Grid-Connected system

The grid-connected PV system is shown in Figure 2.16. This system uses the inverter to convert the DC power generated from the PV panel into AC power that can then be connected to the electric grid. Grid-connected PV inverter should have characteristics such as low cost of PV installation, compact, higher reliability, and high efficiency and safer. The distinct difference between traditional off-grid PV systems and grid-connected PV systems is that the latter do not need batteries. The electricity generated from the PV system is fed into the residential switchboard, which is then utilized to partially supply the home's load demand. If excess generation occurs, in which the PV supply exceeds the load requirement, electricity is exported to the distribution grid. Under certain agreement between the homeowner and the utility operator, the owner is paid for this excess energy. In general, the electricity from the PV system simply supplements the existing power supply (Sulaiman et al., 2010).

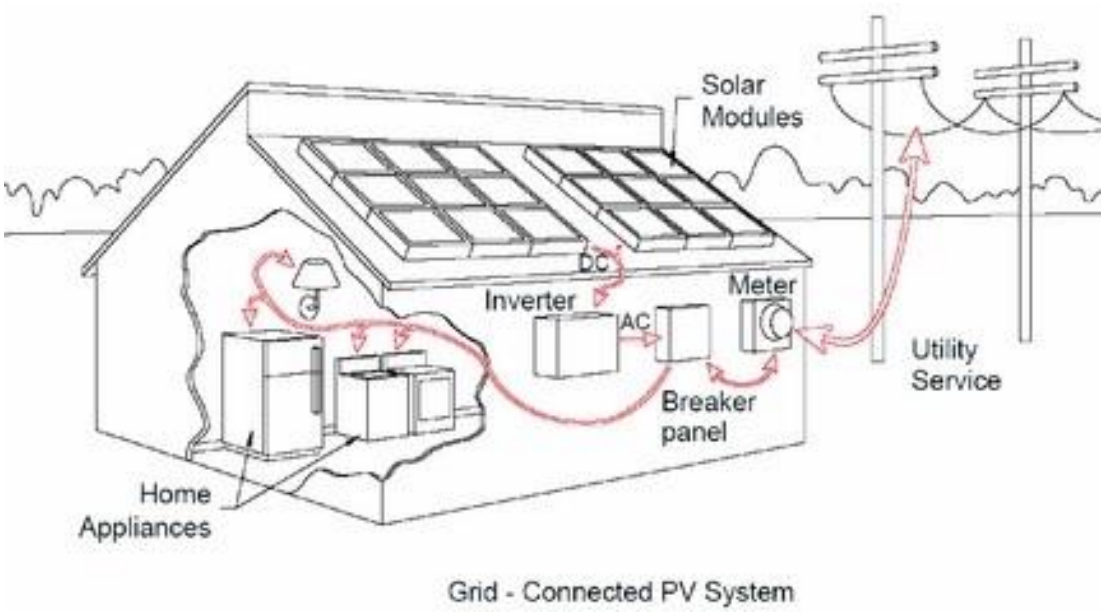


Figure 2.16: Grid-connected PV system (Chetan, 2011)

2.3.2.1 SEDA Malaysia Feed in Tariff (FiT) Mechanism

In Malaysia, the Feed in Tariff (FiT) was mandated under Renewable Energy Act 2011. The Sustainable Energy Development Authority of Malaysia (SEDA Malaysia) is a statutory body formed under the Sustainable Energy Development Authority Act 2011 (Act 726) (Sedamalaysia.com). Malaysia's feed in tariff system obliges distribution licenses to buy from Feed-in Approval Holders the electricity produced from solar grid-connected PV system and sets the FiT rate. The distribution licenses will pay for the energy supplied to the electricity grid for 21 years duration. Table 2.1 shows the FiT rates for individual solar PV from FiT commencement date (SEDA 2014).

Table 2.1: FiT Rates for Solar PV (Individual) (21 years from FiT Commencement Date 1st January 2014)

Solar PV FiT Rates	FiT Rates (RM per kWh)
(a) Basic FiT rates having installed capacity of	
(i) up to and including 4kW	1.0411
(ii) above 4kW and up to and including 24kW	1.0157
(iii) above 24kW and up to and including 72kW	0.7552
(iv) above 72kW and up to and including 1MW	0.7296
(v) above 1MW and up to and including 10MW	0.6080
(vi) above 10MW and up to and including 30MW	0.5440
(b) Bonus FiT rates having the following criteria (one or more)	
(i) use as installation in buildings or building structures	+0.2201
(ii) use as building materials	+0.2116
(iii) use of locally manufactured or assembled solar PV modules	+0.0300
(iv) use of locally manufactured or assembled solar inverters	+0.0100

NOTE: It should be noted that this price depreciates at a rate of 8% each year. The rate is also subject to revision every six months.

2.3.3 Hybrid System

The hybrid energy system is a system that is supplied by a combination of two or more different energy sources (A.EL-M.M.A.A El-Aal., 2003). Usually many hybrid systems application is a combination of a motor-generator set (genset) with other renewable energy source such as PV as shown in Figure 2.17 (Electricity Resources Branch, 2001). To handle the power in the generation system using PV, energy storable components such as batteries are required. The combination of PV and a battery bank enables the ability to supply a low load continuously overnight and, based on the installed PV capacity level, to cover some or all of the morning and mid-day load. The

diesel generator is used for peaking conditions and supplements the battery charging process as needed (IEA, 2013).

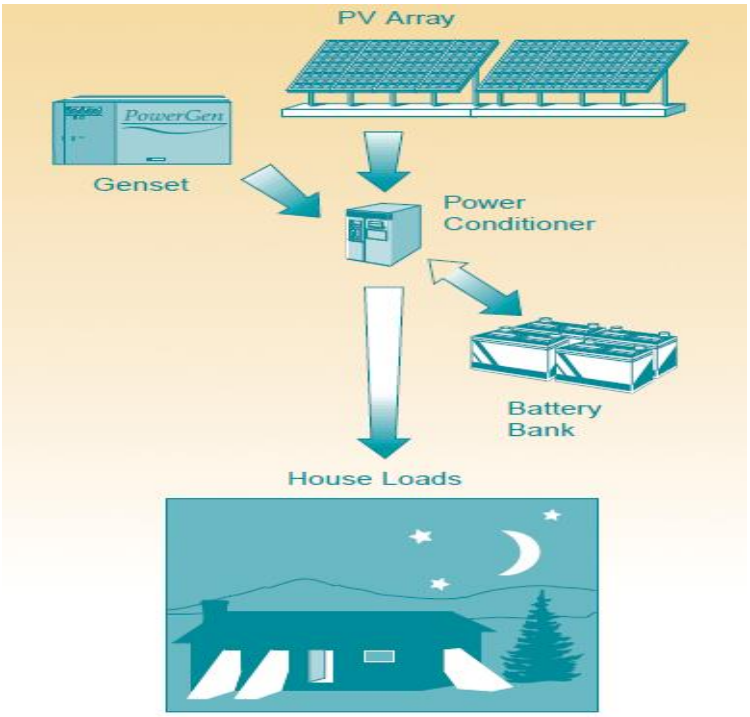


Figure 2.17: Hybrid PV system (Electricity Resources Branch, 2001)

2.4 PV Inverter Systems

2.4.1 Sizing

An inverter is used where DC power needs to converted into AC. The inverter's input rating must never go lower than the total load power. Current inverters are typically rated for maximum DC input power, which is the size of the array in watt-peak, maximum DC input current; and maximum specified output power. This is the AC power they can provide to the grid. In central inverter grid-connected PV system, the ratio between two powers is known as the "Sizing Factor" (*SF*), is defined as (2.1):

$$P_{INV} = SF \times P_{GF} \quad (2.1)$$

The size of the central inverter maximum power (P_{INV}) is related to the total installed peak power of the PV generator (P_{GF}) given in Standard Test Conditions (STC: 1000W/m^2 at 25ºC and for a solar spectrum of AM1.5) and needs to maximize the injected energy to the mains (Velasco, et al., 2007).The *SF* value chosen is normally lower than one since the PV generator generally operates above the temperature value and below the irradiance level given by the STC.

In (Bower et al., 2004) the inverter can be classified into three categories, which is defined by i) Small: 10 kW or less (may provide single or three phase output), ii) Medium: 10 kW to 100 kW (usually for three phase output) and iii) Large: 100 kW and greater (usually for three phase output). When the PV system is connected to the grid, the grid-connected inverters have to comply with the following:

i) Reduced THD and individual harmonic current level;
ii) Near unity power factor;
iii) Minimized level of injected DC current;
iv) Regulated voltage and frequency range for normal operation;
v) Detection of islanding and anti-islanding function;
vi) Synchronization and automatic reconnection;
vii) System grounding.

2.4.2 Types of Grid-Connected PV Inverter

A general classification of grid-connected PV inverters is as follows:

i) Central inverters;
ii) String inverters;
iii) Module-integrated inverter;
iv) Multi-string inverter.

2.4.2.1 Central Inverters

The structure of central inverter is shown in Figure 2.18. It typically serves as an interface to large PV arrays. The parallel strings are connected to one central inverter. Each series string connections generate a cumulative amount of voltage while each parallel connection produces a cumulative amount of current. These two are then combined to produce high power levels. However, the central inverters have its drawbacks, such as it requires high-voltage dc cable connecting the PV panels to the inverter, experience power losses due to centralized MPPT, power losses due to PV module mismatch, losses in string diodes and poor power quality due to the usual use of thyristors at grid-connected stage (Kjaer et al.,2005).

2.4.2.2 String Inverters

Figure 2.19 shows the arrangement of a string inverter (Verhoeven, B., 1998). In the string inverter, each PV string is connected to one inverter. Then the string is paralleled and connected to the AC bus line. When the required PV string voltage is not high enough, the boost DC-DC converter or a line transformer is needed for boosting voltage. The string inverter has its advantages such as no diode elements are required, each string has individual MPPT, and the overall efficiency is increased compared to central inverters and reduced price due to less mass production.

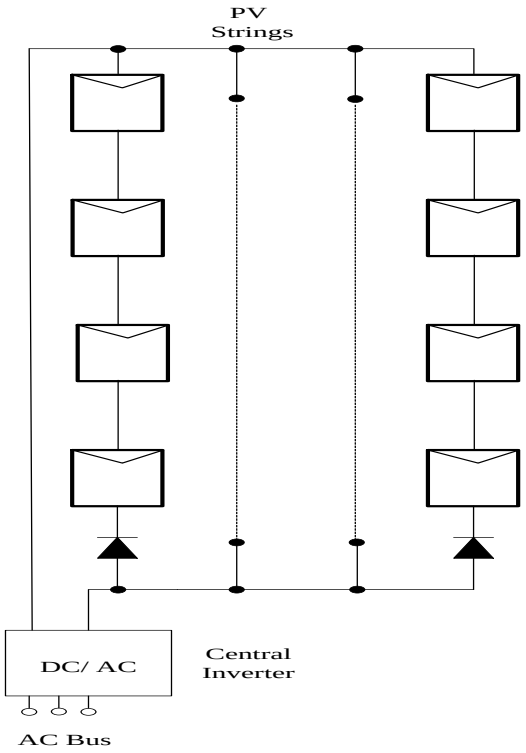


Figure 2.18: Central inverter connection

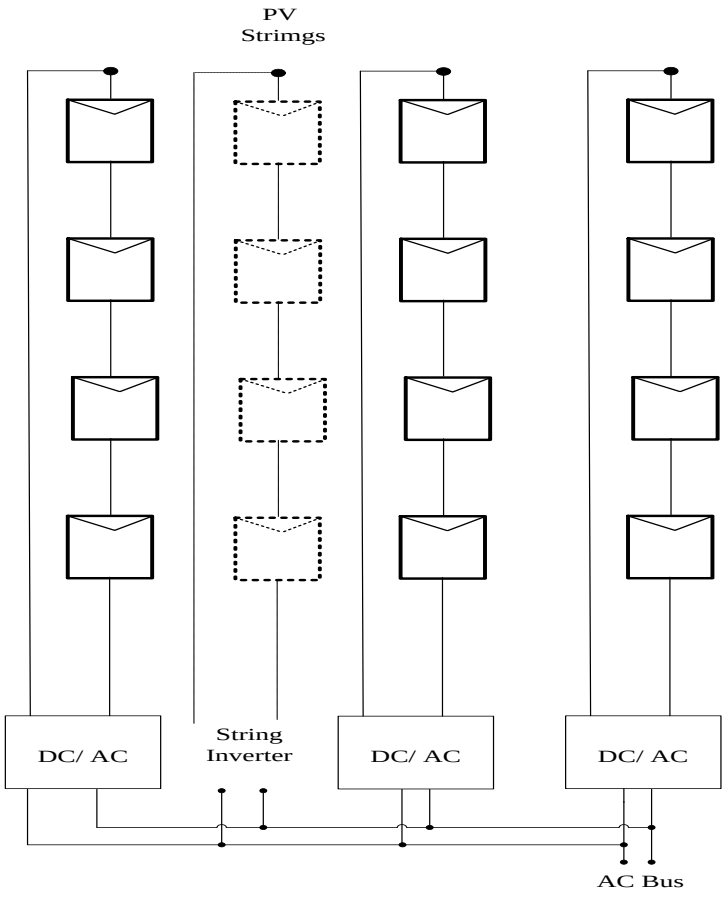


Figure 2.19: String inverter connection

2.4.2.3 Module-Integrated Inverter

The single PV module is connected to its own inverter as shown in Figure 2.20. One drawback of this configuration is that it is necessary to have high voltage-amplification that decreases the overall efficiency. On the other hand, the advantages of the module-integrated inverter is as follows (Xue.Y, et al., 2004):

i) No mismatch losses due to every single PV module have its own inverter and individual MPPT;

ii) Due to modular structure, the enlarging of the system is easy to handle;

iii) "Plug-and-Play" device characteristic.

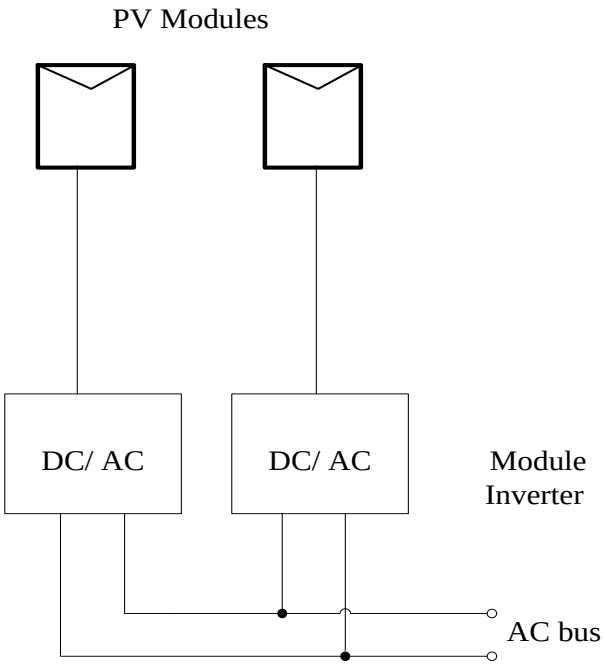


Figure 2.20: Module integrated inverter configuration

2.4.2.4 Multi-String Inverter

Figure 2.21 shows the multistring inverter configuration. This configuration combines the advantages of both string inverter and module inverter (Meinhardt, M., Cramer, G., 2000). The DC-DC converters have individual MPPT and feed its energy to one DC-AC inverter that is from the module integrated inverter concept. From the string

concept, the PV module is connected by series. The main advantage of this configuration is that weather condition does not affect the system since only one AC connected inverter is used.

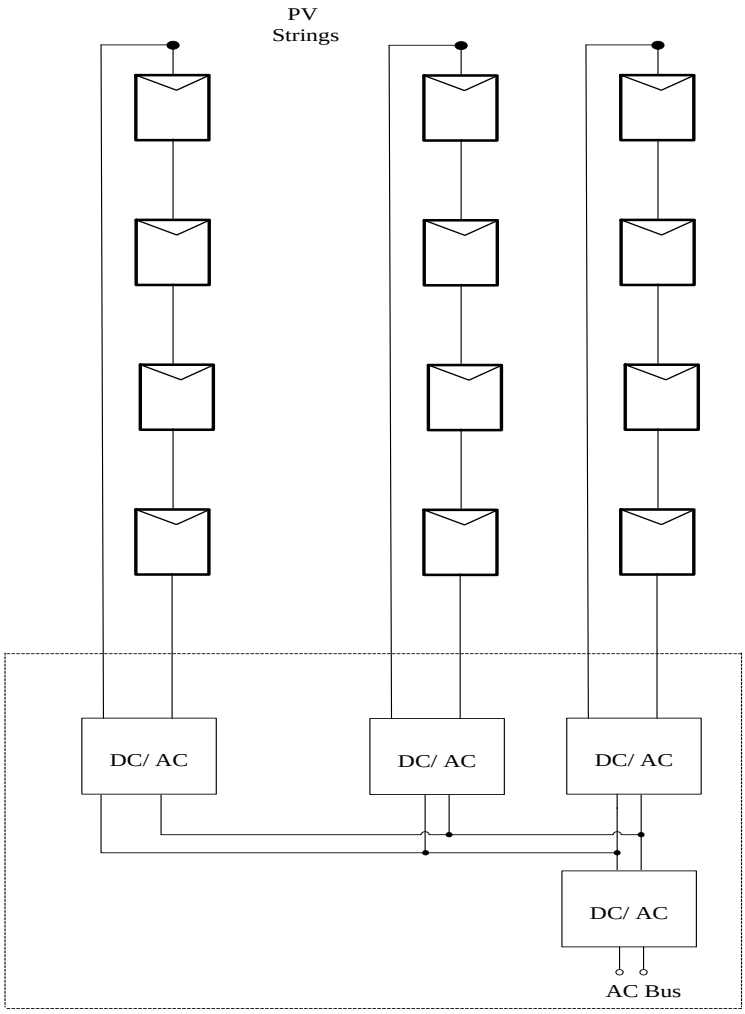


Figure 2.21: Multistring inverter configuration

2.5 PV grid-connected Inverter Configurations

2.5.1 Line Frequency Transformer

Generally, in PV grid-connected inverter system, the line frequency transformer is placed at some middle point between the output inverter and the grid (resolve problems with the injection of dc currents into the grid) (Kjaer, et al., 2005) step-up the output inverter voltage to 240 V_{rms} grid voltage. In multilevel PV inverter system (Rahim, et al., 2010), the configuration is designed as shown in Figure 2.22. The output

inverter voltage (V_{inv}) should be more than √2 of the grid voltage (V_{grid}) to ensure the power from the PV generator flows into the grid. With a ratio of 1:2 of transformer, the V_{inv} should be defined using equation 2.2. The line-frequency transformer used in inverters is regarded as a poor component because of larger size, weight and price (Kjaer, et al., 2005).

$$V_{inv} = \frac{\sqrt{2} \times V_g}{2} \tag{2.2}$$

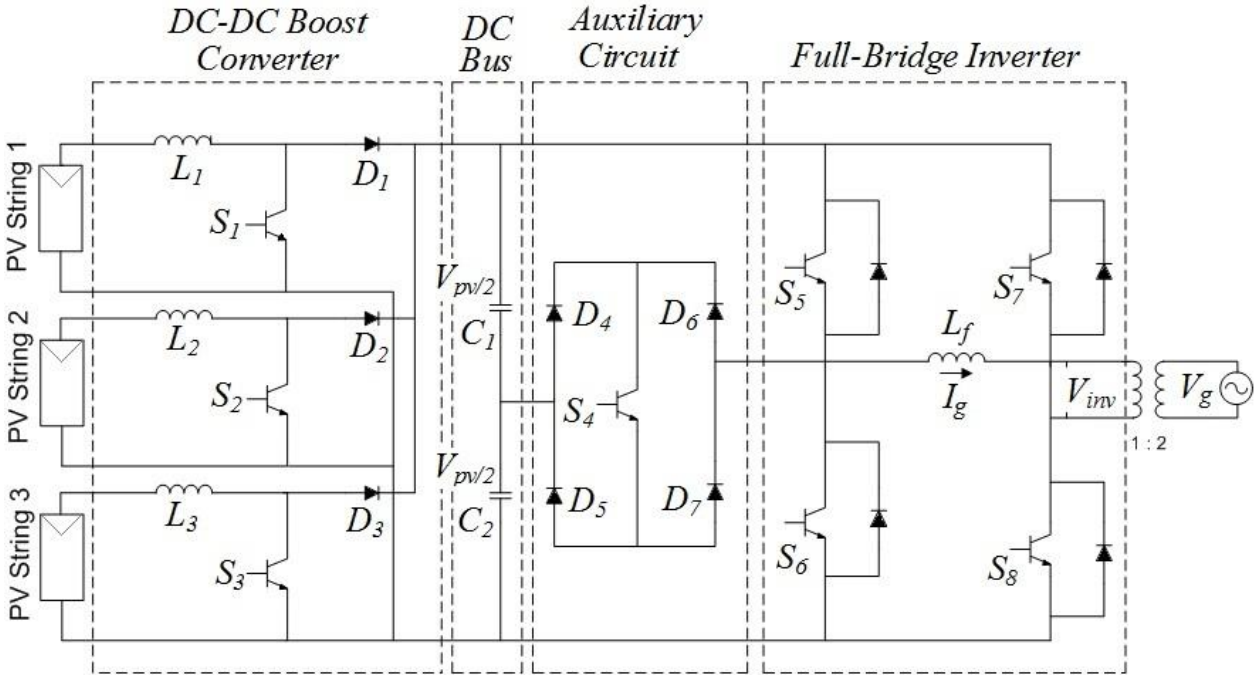


Figure 2.22: Single-phase multistring five-level inverter topology

2.5.2 High Frequency Transformer

In the existing inverter topology, the high frequency transformer is placed at the DC side to offer safety and galvanic isolation solution. However, the whole power converter efficiency is decreased due to extra power losses in this component. The high-frequency (HF) transformer side in the DC-DC converter is shown in Figure 2.23 (Xue, et al., 2004). The HF transformer leads to more compact solution but requires extra maintenance in order to minimize losses (Blaabjerg, et al., 2004).

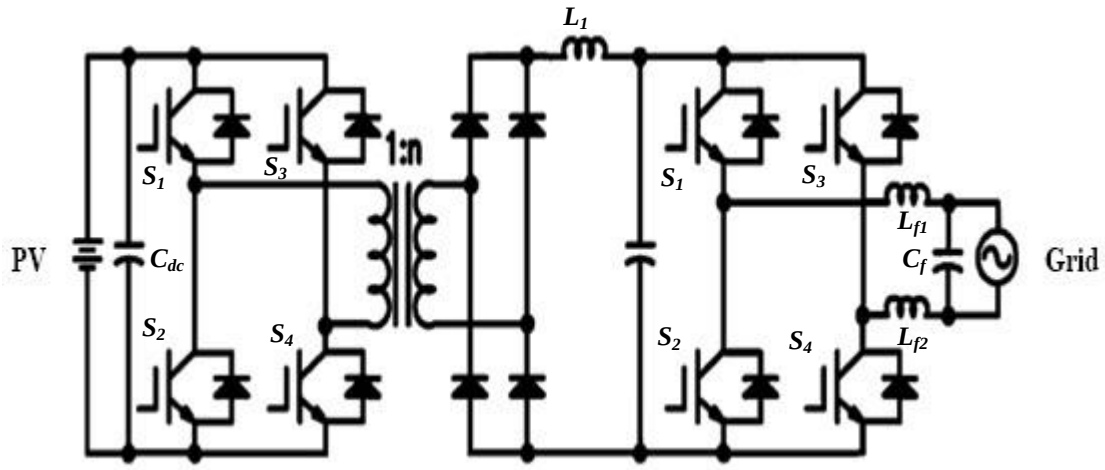


Figure 2.23: PV inverter with DC-DC converter and HF transformer

2.5.3 Transformer-less / without Transformer

Compared to PV grid-connected inverter system with galvanic isolation, either using line frequency transformer or high frequency transformer, the transformerless full bridge inverter is introduced in (Kerekes et al., 2011; Heribert et al., 2003) to increase the overall power converter efficiency. It can also minimize the ground leakage current, which is a counterpart in the galvanic isolation. The general diagram of PV transformerless full-bridge inverter system is shown in Figure 2.24 (Koutroulis & Blaabjerg, 2012).

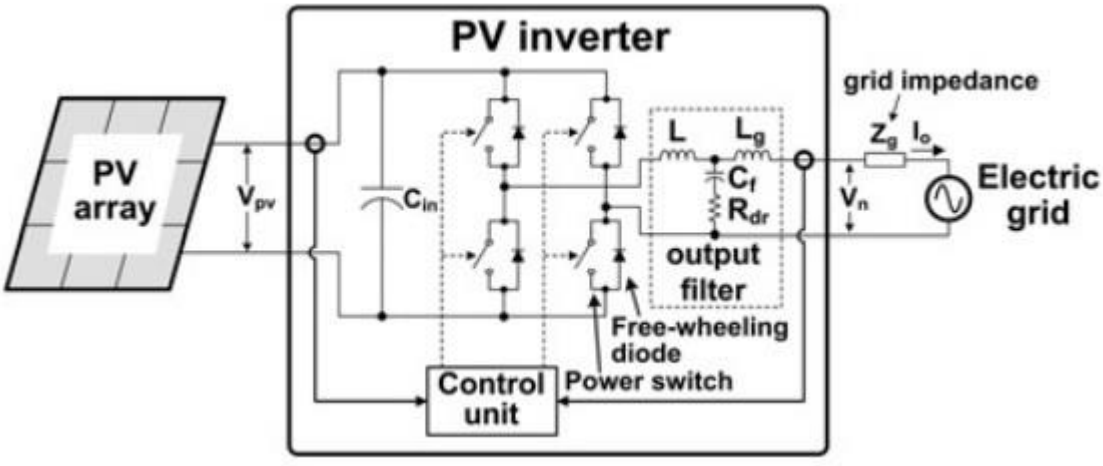


Figure 2.24: PV transformerless H-Bridge inverter system

2.6 Maximum Power Point Tracker (MPPT) Algorithms

Generally, the photovoltaic power generators have non-linear characteristics because output power from the PV modules depends on solar insolation, cell temperature and load level. Thus, in order to solve this problem, several methods of Maximum Power Point Tracking (MPPT) have been proposed (Cavalcanti et al., 2007; Esram & Chapman, 2007; de Brito et al., 2011) to extract the maximum power. Among them, the constant voltage control method, the perturbation and observation (P&O) method and the incremental conductance method (IC) have their own attractive advantages (Yuet et al., 2004).

2.6.1 Constant Voltage

In many severely budget-constrained systems, the converter is ran at a fixed duty cycle, which results in poor efficiency (de Brito et. al, 2013). A marginal improvement can be obtained by using the constant-voltage (CV) method. This algorithm is based on empirical results, with the MPP voltage hovers in between 70% to 80% of the solar cell open-circuit voltage (Hohm & Ropp, 2003). This provides a reference to determine which output voltage can to track. In this method, only the PV voltage is measured then compare to the reference voltage to reach the maximum power point (MPP). The benefit of CV method is more effective when the PV panel in low insolation conditions, compare to other method, such as P&O and IC (Faranda et al., 2008).

2.6.2 Perturbation and Observation (P&O)

The P&O method is computationally simple but requires both voltage and current sensors to find the direction of maximizing power change. This algorithm operates by comparing the output PV voltage with the power of the previous one perturbation cycle, which is perform by *dp/dv*.The flow chart of the P&O algorithm is

shown in Figure 2.25. If the PV array's operating voltage is perturbed in a given direction and *dp/dv*> 0, it is known that the perturbation moved the array's operating point toward the MPP. The P&O algorithm would then continue to perturb the PV array voltage in the same direction. If *dp/dv*< 0, then the change in operating point moved the PV array output away from the MPP, and the P&O algorithm reverses the direction of the perturbation (Hohm & Ropp, 2000).

This method is very easy to implement, therefore it is used commonly in the PV industry application when irradiance does not vary rapidly with time. Unfortunately, this method has its drawback, owning to the slow tracking oscillations around the maximum power point (MPP) (Hua et al., 1998). Thus, in order to eliminate the drawback, the modified P&O algorithms have been proposed in (Abdelsalam et al., 2011).

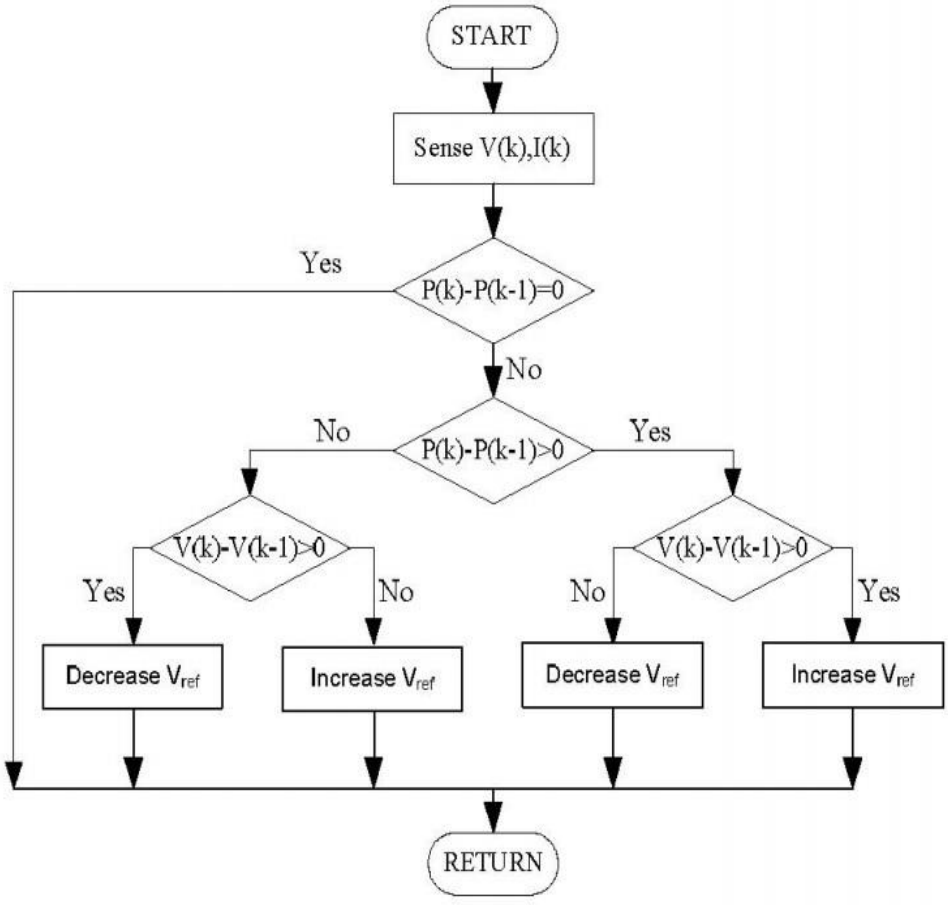


Figure 2.25: Perturbation and observation MPPT technique

2.6.3 Incremental Conductance (IC)

Due to fast tracking and higher accuracy than P&O method, the IC method has been proposed in (Hohm & Ropp, 2000). The flow chart of increment conductance (IC) MPPT method is shown in Figure 2.26. This method operates based on the PV panel's incremental conductance *dI/dv* to compute the sign of *dp/dv*.

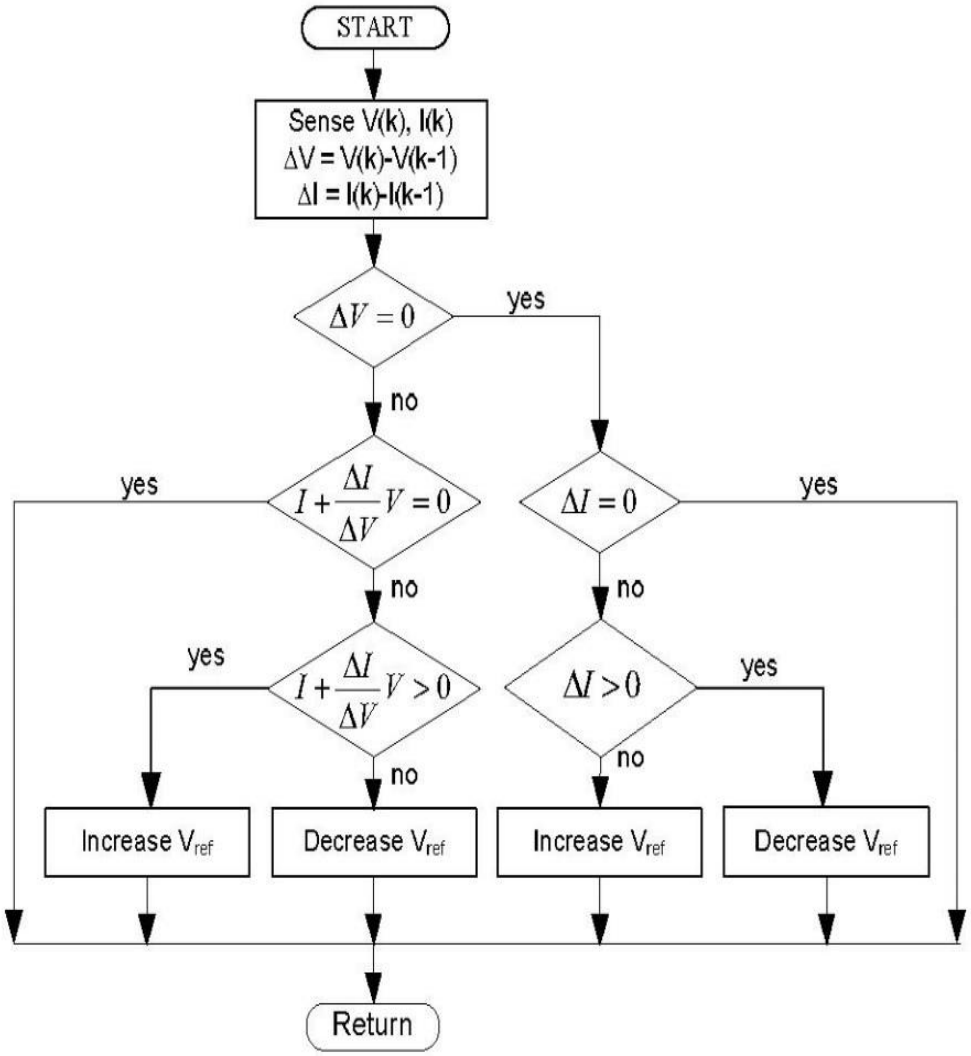


Figure 2.26: Incremental Conductance MPPT flowchart method

2.7 Protection for Grid-Connected PV Inverters

Islanding happens when distributed generators (DGs) continue to operate and supply power to the grid even when conventional power from the utility is not available.

Islanding pose serious hazards to utility service workers, who may be unaware that the circuit still has power. It may also prevent automatic reconnection of devices. Because of this, distributed generators are required to be able to detect islanding and halt power production immediately. This characteristic is referred to as anti-islanding. Recently, the anti-islanding detection technique for distributed generator (DG) have been reviewed in (Mahat et al., 2008), which is divided into remote and local techniques as shown in Figure 2.27.

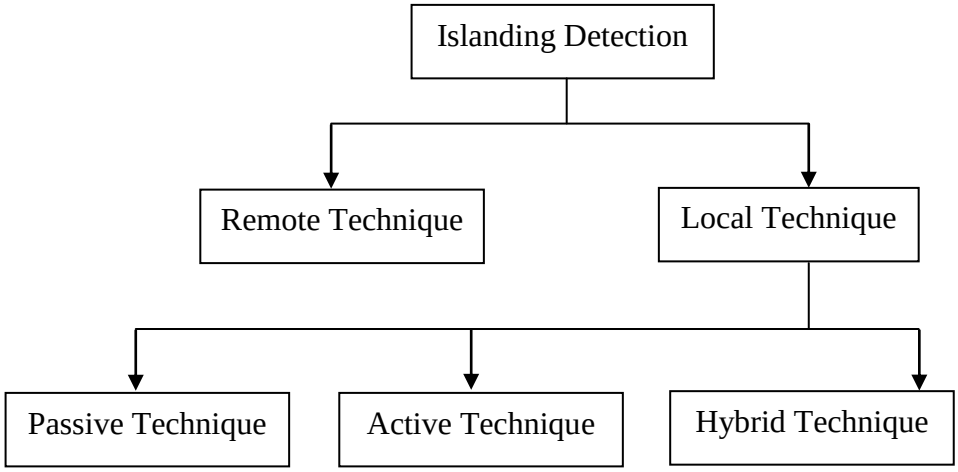


Figure 2.27: Islanding detection methods

For the local detection technique, the grid protection device shall include passive anti-island protection within set time, which is in the form of under voltage protection (UVP), over voltage protection (OVP), under frequency protection (UFP) and over frequency protection (OFP). For Malaysia the standard setting on the commercial inverter typically are 200 V- 230 V (for UVP), 250 V – 270 V (for OVP) and 48 Hz (for UFP) and 52 Hz (for OFP) (Sulaiman et al, 2010).

Monitoring the phase difference between the inverter voltage at the point of common coupling (PCC) and its output current inverter for unexpected phase jump is employed in voltage phase-jump detection method. Furthermore, another passive

technique is voltage and current harmonic detection to monitor the changes of total harmonic distortion (THD).

The small disturbance signal parameters (voltage and frequency) at PCC is employed in an active islanding detection technique that is detects by feedback circuit. This technique is involved in imbalance measurement, impedance detection at specific frequencies, slip mode frequency shift, active frequency drift, variation of active and reactive power, sandia frequency shift (active frequency drift with positive feedback), sandia voltage shift (uses positive voltage feedback) , frequency jump, main monitoring units with the predetermined all-pole switching devices connected in series and general electric frequency scheme. (Mahat et al., 2008)

2.8 Power Quality Issues

The power injected by the grid-connected PV systems into the grid must meet utility power quality requirement. These requirements are specified in the IEC 61000-4-30 international standard, which state that a PV system must deliver power to the grid with high power factor (PF) and low total harmonic distortion (THD).

2.8.1 Harmonics

Harmonics can be divided into low and high frequency harmonics. The low frequency harmonic generates impure sinusoidal wave at the inverter output and consequently includes harmonics apart from fundamental frequency. Thus, in order to minimize these harmonics, the inverter systems are equipped with a high frequency (several kHz) pulse width modulation (PWM) technique. Unfortunately, this technique will induce high order harmonic due to the inherent characteristics of a rectangular pulse. Therefore, in (Rockhill et al., 2011; Picardi et al., 2012; Singh et al., 2011) these harmonics can be easily attenuated using filters with respect to total harmonic distortion (THD) factor according to International and European standards.

2.8.2 Total Harmonics Distortion (THD)

The total harmonic distortion (THD) is used to quantify the harmonics effect on the power system voltage. It is can be expressed as a percent of the fundamental properties and is defined in (2.3), assuming no DC component is in the output waveform. Similar calculations for THD current are done using the same equation by substituting the voltage values with current (IEEE 519-1992, Jan 1993).

$$THD = \sqrt{\frac{\sum_{h=2}^{\infty}\left(V_{h,rms}\right)^2}{V_{1,rms}}} \times 100\% \tag{2.3}$$

With reference to Photovoltaic (PV) systems, some regulations and standards about harmonic content provide limits of the total harmonic distortion (THD) of voltage and current. According to IEEE 519-1992 standard, the harmonic voltage and current limit is set at the point of common coupling (PCC). This standard established a limit that the power delivered to the customer shall not have more than 5% of the current and voltage THD factors. Particularly in power quality, the IEC 61727 standard defines that, the THD limit for current output (THD_i) and voltage output (THD_v) are 5% and 2% respectively. In addition, the maximum individual voltage harmonic is 1%. Otherwise, the European standard EN50160 provides a limit for 40^{th} THD_v, which is equal to 8%.

2.8.3 Power Factor of PV Inverter

The reduction of power factor in the inverter's AC output affects voltage fluctuations in the power distribution system. Thus, it is vital to ensure that the AC output's power factor is stable. Survey results from (Report IEA-PVPS, 2002) indicate that with rated output, a power factor of 100% is obtained. The findings also state that even when the output power goes down to 10%, a power factor of 90% or over is obtained. Because the current control scheme is a prominent option in inverters, the

power factor is typically set to 100%. Some inverters are capable of adjusting the power factor. For current control based inverters, adjustment is done by phase shifting of the AC current's reference value with respect to the AC voltage. The intention of adjusting the power factor is to suppress any voltage rise that is caused by the PV system output power. Unaddressed issues of voltage rise at the point of common coupling (PCC) may cause excessive voltage at the distribution line.

2.9 Performance PV Inverter Issues

Performance testing of PV inverter system has been done in various ways (Bower et al., 2004), which includes conversion efficiency and MPPT accuracy. The conversion efficiency of the inverter is defined between the dc source input (PV) and the ac output. The idea of conversion efficiency is divided into two parts, the MPP tracker (η_{mppt}) and the DC to AC converter (η_{conv}). The function of both parts is to maximize the power delivered by the PV array, and then to convert the DC power into AC power. The static MPP-tracking efficiency η_{mppt} can be defined as in (2.4) (Haeberlin, et al., 2005).

$$\eta_{mppt} = \frac{1}{P_{mpp} T_M} \int_0^{T_M} V_A(t) i_A(t) dt \qquad (2.4)$$

Where $V_A(t)$ is the array voltage at inverter input, $i_A(t)$ is the array current at inverter input, T_M is the duration of measurement (started at t = 0) and P_{MPP} = maximum PV power at MPP array.

The DC/AC converter efficiency (η_{conv}) presents the ratio between the ac output power (P_{ac}) and dc input inverter power (P_{dc}) as defined in (2.5) (Haeberlin, et al., 2005).

$$\eta_{conv} = \frac{P_{ac}}{P_{dc}} \tag{2.5}$$

Therefore, the total efficiency (η_{total}) of the grid-connected inverter can be defined in (2.6) (Haeberlin, et al., 2005).

$$\eta_{total} = \eta_{mppt}\eta_{conv} \tag{2.6}$$

The performance of MPPT function often depends on the PV array properties that the unit is trying to track (Bower et al., 2004). Therefore, the MPPT accuracy can be obtained in (2.7).

$$MPPT = \frac{Measured}{Expected} \tag{2.7}$$

The expected value represents the voltage, current or power of the specified simulator's maximum power setting, while the measured value defines the measured voltage and the current or power at which the MPPT device works. The MPPT accuracy value can be calculated for voltage, current and power. The MPPT accuracy value will reach 1.0 when the MPPT device operates the simulator at the expected maximum power point. Otherwise, the value will be in range of 0 to 1 when the device operates the simulator at below or above the maximum power point.

2.10 Summary

This chapter began by discussing the three types of module configuration of PV modules, namely series, parallel and series-parallel. This is then followed by an overview of three common PV inverter connection systems which includes PV inverter sizing. Next, a summary of grid-connected PV inverters classification is presented which highlight the advantages and disadvantages for each category. Here, the

difference between inverters with and without transformers is also explained. Subsequently, three main algorithms used to maximise power through MPPT is reviewed. Finally, the protection, power quality and performance aspect of grid-connected PV inverters is discussed.

CHAPTER 3

Overview of Power Converter Photovoltaic System

3.1 Introduction

The concept of power electronics for power conversion system has gained widely acceptance in power system applications. Power electronics converters are increasingly used for power conversion and conditioning, compensation, and active filtering especially in renewable energy application such as solar photovoltaic. This chapter gives an overview of the power converter photovoltaic system topologies. The DC-DC converter and inverter topologies with and without transformers is presented in this chapter. Furthermore, parasitic capacitance of the PV array, common-mode voltage model and safety issues regarding common-mode voltage and ground leakage current is also discussed in this chapter.

3.2 Power Converter

The field of power electronics covered the processing of electrical power using power semiconductor devices either uncontrollable or controllable types. Various types of power semiconductor devices were made commercially available since 1970. Examples of common types of power semiconductor devices such as power diodes, thyristors, power bipolar junction transistors (BJTs), power MOSFETs, insulated gate bipolar transistors (IGBTs), gate-turn-off thyristor (GTO) and static induction thyristor (SITH).

Switching converter is the key element of power conversion. For the power conversion control, the conversion of the electric power from one form to another is

necessary and the switching properties of the power devices permit this conversion (Rashid, M. H., 2004). The power electronics circuits can be classified into:

a) DC to AC converters (Inverters)

The DC input power is converts to AC power by switching sequence. Voltage source inverter (VSI) and current source inverter (CSI) are two types of dc to ac converters as shown in Figure 3.1.

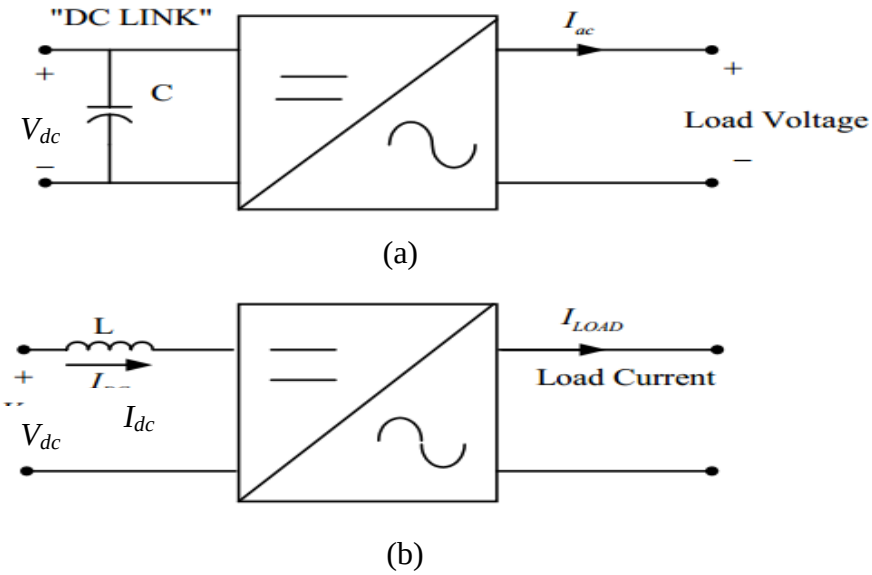


Figure 3.1: Types of DC to AC converter

b) DC to DC converters (DC choppers)

The unregulated DC input power can be regulated by DC-DC converters. The general block diagram of DC to DC converter is shown in Figure 3.2.

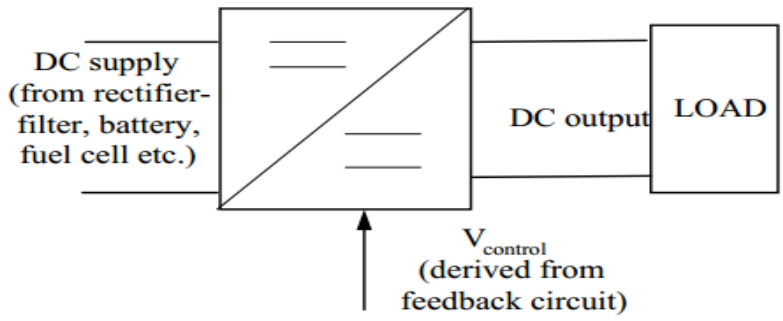


Figure 3.2: DC-DC converter block diagram

c) AC to DC converters (controlled rectifiers)

Controlling the power semiconductor devices in the rectifier circuit can convert the AC power signal from supply to the DC power signal. General block diagram of AC to DC converter is shown in Figure 3.3.

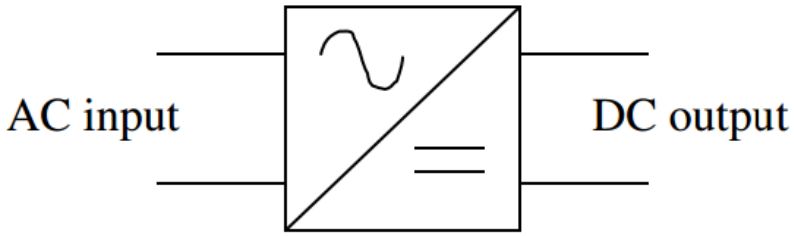


Figure 3.3: General block diagram of AC to DC converter

d) AC to AC converters (AC voltage controllers)

AC to AC converter is convert fixed AC power directly to variable AC power without change in frequency. Figure 3.4 shows the general block diagram of AC voltage converter.

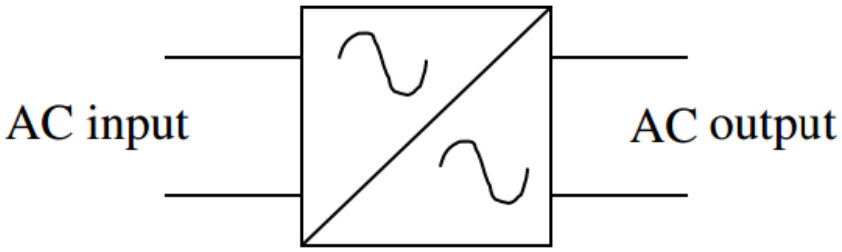


Figure 3.4: General block diagram of AC to AC converter

Only DC to AC converters and DC to DC converters are considered in this work.

3.3 Types of Non-Isolated DC-DC Converters Commonly Used

3.3.1 Non Isolated DC-DC Converters

The category of non-isolated DC-DC converters have been analysed in (Daniel, 2011). The DC analysis of PWM DC-DC converter is analysed for CCM operation. The DC voltage transfer function of converter and voltage stress of switches are determined.

3.3.1.1 Conventional DC-DC Boost Converter

Generally, the conventional boost converter has been used in PV system applications (Selvaraj, Rahim, 2009; Roman, et al., 2006). The converter's output voltage is larger than the input voltage, which is why it is called a boost converter. Figure 3.5 shows the boost converter circuit diagram, consisting of an inductor *L*, a power semiconductor device *S*, a power diode *D*, a filter capacitor *C* and a load resistor, *R*.

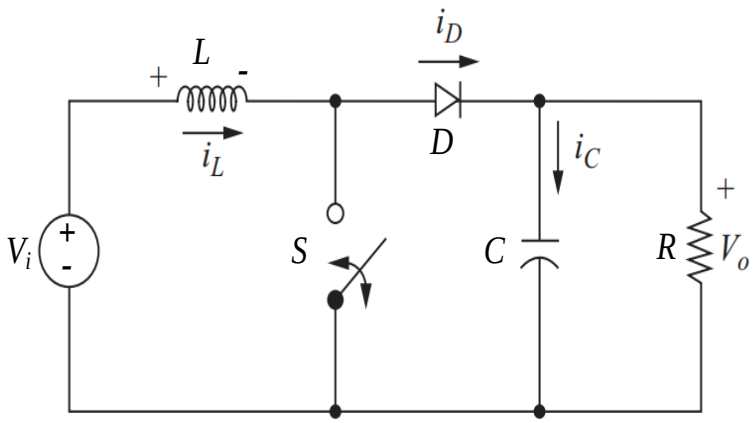


Figure 3.5: The DC-DC boost converter

Idealized waveform inductor voltage and inductor current of the converter during the switch's opening and closing is shown in Figure 3.6 (Daniel, 2011).

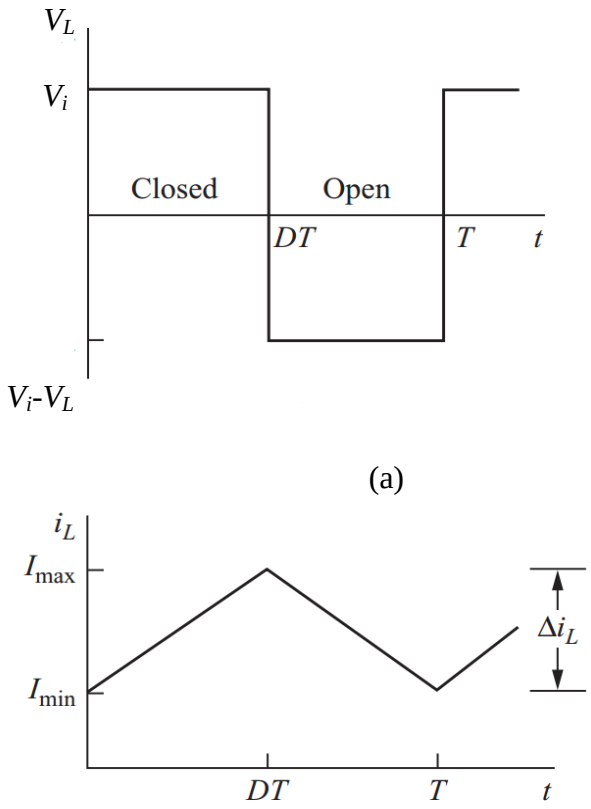


Figure 3.6: Boost converter waveform: (a) Inductor voltage, (b) Inductor current

When the switched is closed, the inductor voltage (V_L) and inductor current change rate ($\Delta_{iL,closed}$) can be rearranged as in (3.1) and (3.2).

$$V_L = V_i = L\frac{\Delta_{iL}}{DT} \tag{3.1}$$

$$\Delta_{iL} = \frac{V_i DT}{L} \tag{3.2}$$

The voltage across the inductor (V_L) when the switch is opened can be determined from (3.3). Since inductor current is constant, the change of current ($\Delta_{iL,opened}$) can be defined as in (3.4).

$$V_L = V_i - V_o = L\frac{\Delta_{iL}}{\Delta_t} \tag{3.3}$$

$$(\Delta_{iL,opened}) = \frac{(V_s - V_o)(1-D)T}{L} \tag{3.4}$$

The analysis of steady-state operation is analysed to determine the transfer voltage of converter, which is expressed in (3.5). V_o, V_i and D are represented as the output voltage, input voltage and duty cycle of the switch respectively. M represents the voltage conversion ratio.

$$V_o = \frac{V_i}{1-D} = M \tag{3.5}$$

The normalized voltage stresses (M_s) of the switch is given by:

$$M_s = \frac{V_i}{V_o} \tag{3.6}$$

3.3.1.2 Cuk-Derived Boost (CD-Boost) Converter

The CD-Boost converter is a combination of an inverting switched-capacitor (SC) cell and a classical Cuk converter (Ismail et al.,2008) as shown in Figure 3.7, which is analysed in CCM operation.

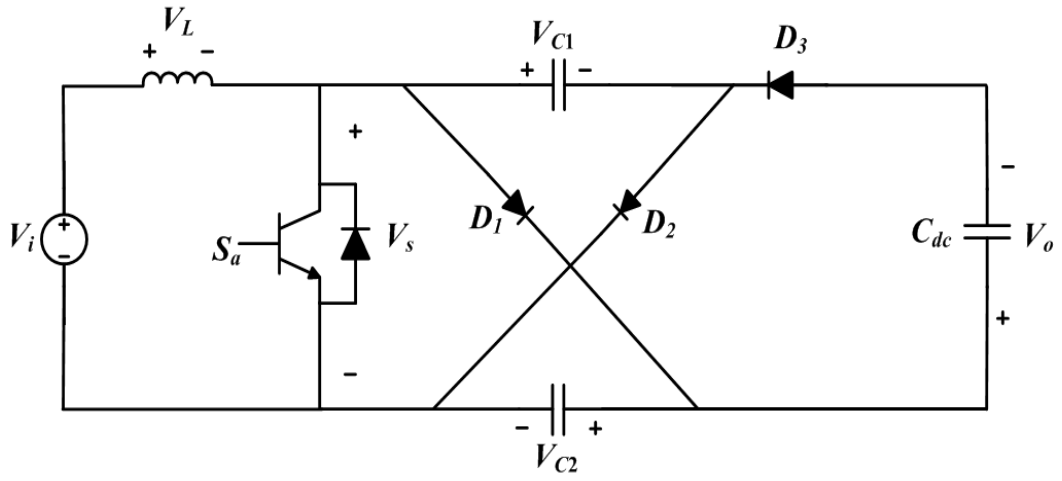


Figure 3.7: The CD- Boost converter circuit

The voltage conversion ratio *(M)* of the CD-Boost in steady-state analysis of the inductor is

$$\frac{V_o}{V_i} = \frac{2}{1-D} = M \tag{3.7}$$

where V_i is the DC input CD-Boost converter voltage, V_o is the output CD-boost converter voltage, and D is the duty cycle. From (3.7), the voltage conversion gain of the CD-boost converter is twice that of a conventional boost converter. Therefore, the output voltage is a step higher. In addition, the normalized voltage stresses (M_s) of the switch is low as given in (3.8) (Ismail et al, 2008).

$$M_s = \frac{V_i}{V_o} = \frac{1}{2} \tag{3.8}$$

3.3.1.3 Three-level DC-DC Boost Converter

In (Jung et al., 2008), a three-phase PV system with a three-level DC-DC boost converter has been used instead of the conventional boost converter because of smaller inductor sizes needed to achieve comparably low ripple. Figure 3.8 shows a three-level DC-DC converter. The operation of this converter can be classified into two regions; 1) region 1: when input voltage is lower than half of the output voltage ($V_i < V_o / 2$) or 2) region 2: when input voltage is larger than half of the output voltage ($V_i > V_o / 2$). The operation switching (S_1 and S_2) and inductor voltage are shown in Figure 3.9 (Zhang, 1995).

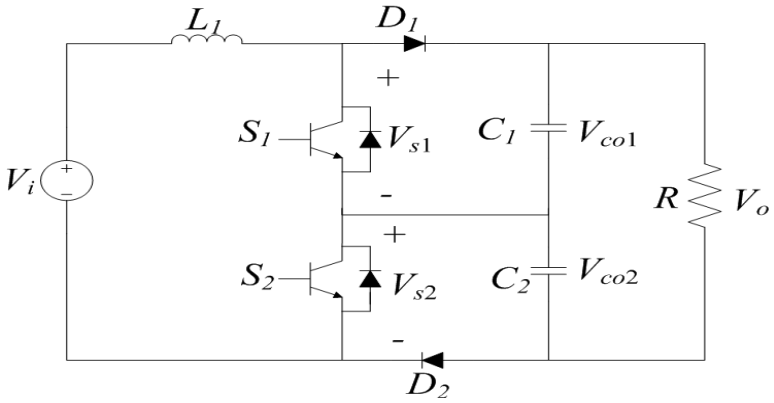


Figure 3.8: Three level DC-DC boost converter

The operation of this converter can be determined in three state conditions; 1) S_1 and S_2 are closed to charge the inductor; 2) S_1 is opened and S_2 is remain closed to transfer the energy to capacitor C_1 and 3) S_1 is closed and S_2 is opened to transfer energy to capacitor C_2. The capacitors (C_1 & C_2) use the same rated voltage during the steady-state analysis. When both switches S_1 and S_2 are closed, the rate of inductor current (Δ_{iL}) is defined in (3.9).

$$\Delta_{iL,S1\&S2closed} = \frac{V_i}{L}(DT) \tag{3.9}$$

Meanwhile, when S_1 is opened and S_2 remains closed, the change of inductor current (Δ_{iL}) is defined in (3.10).

$$\Delta_{iL,S1opened,S2closed} = \left(\frac{2V_i - V_o}{2L}\right)(1-D)T \tag{3.10}$$

The net change of inductor current must be zero for steady-state operation. The conversion ratio voltage is defined as in (3.11). This derivation is the same for state three ($S_{1,\,close}$ & $S_{2,\,open}$) as defined above.

$$\frac{V_o}{V_i} = \frac{2}{1-D} = M \tag{3.11}$$

The normalized voltage stress for each switch (S_1 & S_2) is half of the capacitor voltage (V_{co1}, V_{co2}) respectively, that is determined in (3.12).

$$M_{s1,}M_{s2} = \frac{V_{s1}}{V_{co1}} = \frac{V_{s2}}{V_{co2}} = \frac{1}{2} \tag{3.12}$$

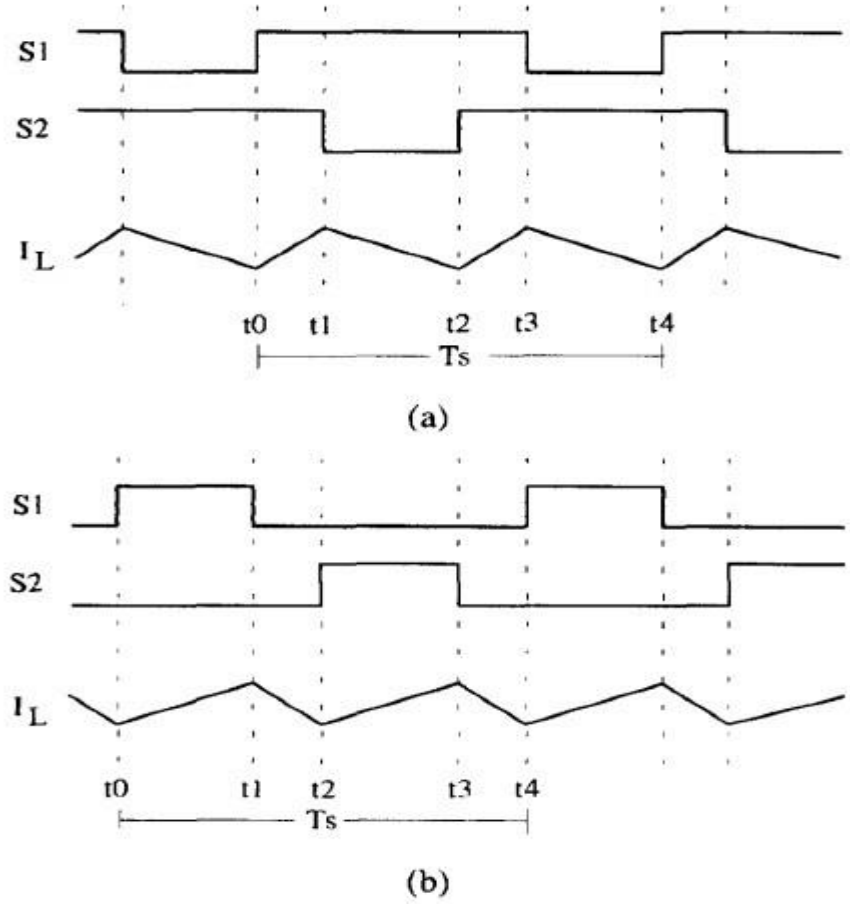


Figure 3.9: Switching pattern and inductor voltage waveform of three-level converter: (a) ($V_i < V_o/2$), (b) ($V_i > V_o/2$)

3.3.1.4 Cascaded DC-DC Boost Converter

In (Huber & Jovanovic, 2000), the cascade DC-DC boost converter has been introduced as shown in Figure 3.10, that consist of two conventional DC-DC boost converters. This converter can generate very high output voltage and is attractive for large-scale PV systems. The voltage stress of the switch for stage 1 is low due to low input voltage from the PV generator, whereas the switch voltage stress of stage 2

depends on stage 1's conversion output voltage that is defined in equations (3.13) and (3.14).

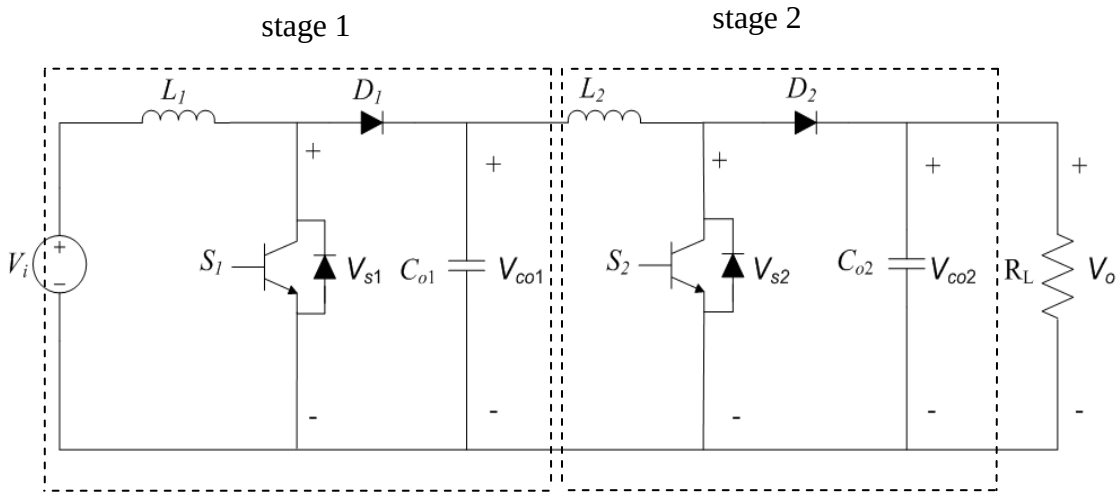


Figure 3.10: Cascaded DC-DC boost converter

$$M_{s1,} = \frac{V_{s1}}{V_{co1}} = 1 \tag{3.13}$$

$$M_{s2,} = \frac{V_{s2}}{V_{co2}} = 1 \tag{3.14}$$

Nevertheless, the converter is more complex and costly because it needs two power devices and associated driving circuits. Furthermore, the stability and the synchronization of two-power semiconductor is a point of concern (Xiaogang, 2002).

3.3.1.5 Inverting Zeta Derived DC-DC Converter

The new-generation DC-DC converter topology extends the switched-capacitor (SC) cell circuit into classical Zeta converter (see Figure 3.11). The SC cell circuit has three diodes and two identical capacitors C_1 and C_2 (Xiaogang, 2002).

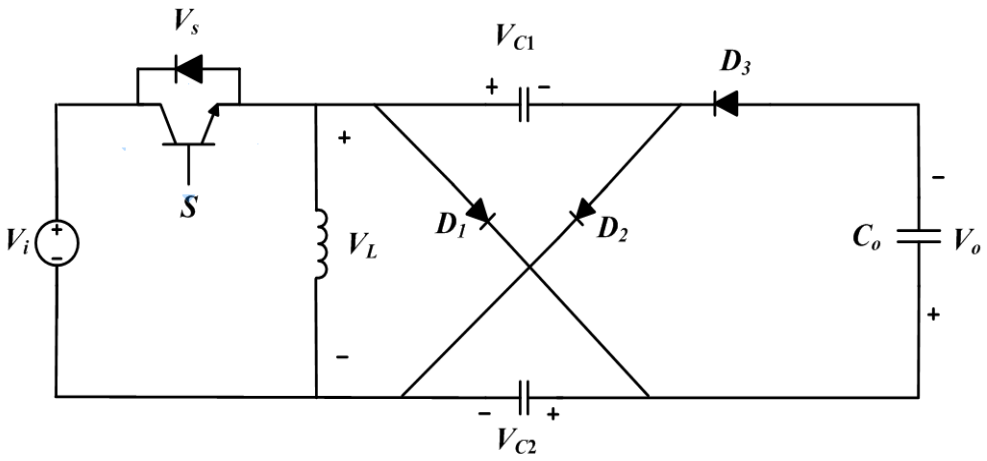


Figure 3.11: Inverting zeta derived boost converter

When the switch is on, D_1 and D_2 are forward-biased and D_3 is reversed biased. Consequently, C_1, C_2, and L_1 charge up while C_o discharges and transfers energy to the load. In the second-state mode, when the switch is open, D_3 is forward biased whereas $D_1$and D_2 are reverse biased.

C_1 and C_2 are discharged by the inductor current and C_o charges up. In steady-state analysis, there is no change to the inductor current. The voltage conversion ratio is expressed as (3.15). Furthermore, the normalized switch voltage stress of the converter is defined in (3.16) (Ismail et al., 2008).

$$M = \frac{V_o}{V_i} = \frac{2-D}{1-D} \tag{3.15}$$

$$M_s = \frac{V_s}{V_o} = \frac{M-1}{M} \tag{3.16}$$

3.4 Pulse Width Modulation (PWM) Scheme

The basic control in the power electronics is pulse width modulation (PWM) scheme. The advantages of PWM scheme are no any external components to obtained output voltage and low order harmonic can be minimized (Rashid, M. H., 2004). The

PWM groups are categorized into PWM based voltage forced strategy, hysteresis current control and predicted current control with fixed switching frequency.

3.4.1 PWM based Voltage Forced Strategy

The principle of sinusoidal PWM is based on comparing a sine modulating wave (V_{ref}) with a triangle carrier waveform (V_c). The principle of sinusoidal PWM for 360^0 period is shown in Figure 3.12.

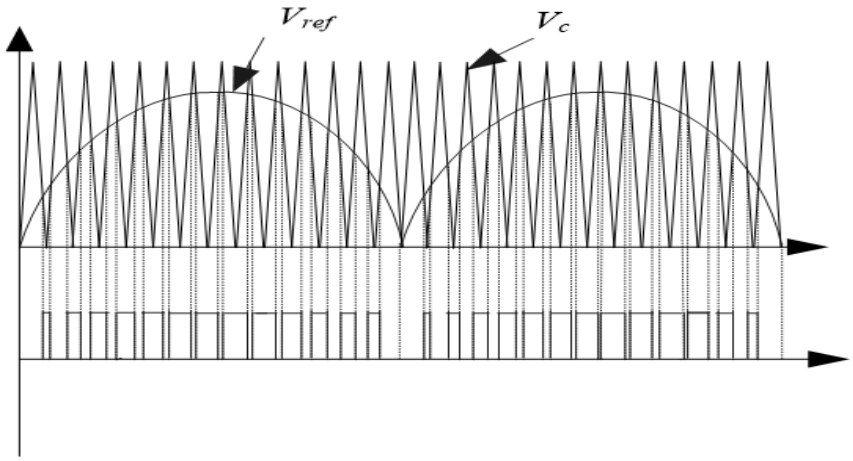


Figure 3.12: Principle of sinusoidal PWM technique

The points of intersection determine the switching points of the power devices. Depending on the application, the frequency and magnitude of the modulating wave can be adjusted to achieve a variable-frequency variable-magnitude output voltage. A carrier with free running frequency is known as an asynchronous PWM while a carrier with its frequency locked to the modulating frequency is known as a synchronous PWM. In digital designs, to avoid problems associated with natural sampling, a regular sampling technique is used. The symmetrical and asymmetrical samplings are the two most common regular sampling techniques.

3.5 PV Inverter Topologies

In order to feed energy from a PV source into the utility grid, the following tasks need to be fulfilled (Myrzik & Calais., 2003):

i) To shape the current into a sinusoidal waveform;

ii) Low total harmonic distortion;

iii) To ensure PV voltage is higher than grid voltage;

iv) Voltage regulation within specify range;

v) Frequency synchronization with the main frequency 50 $\pm$ 2 %

These three main functions can be executed with an appropriate inverter design and different inverter topologies. Based on the electrical isolation, the inverter can be classified as isolated inverters or non-isolated inverters. For isolated inverters, the H-Bridge topology with line frequency and unipolar PWM is usually used (Chen & Smedley, 2004; Mohan., 2003) due to its simplicity, having only four insulated gate bipolar transistors (IGBT's)as well as having a good trade-off between efficiency, complexity and price (Roberto at el., 2007). However, the transformer in the power converter system increases the volume and weight. Nowadays, to overcome that problem, various transformerless H-Bridge inverter topologies have been proposed.

3.6 Parasitic capacitance of PV system

The top and cross-section view of a PV module with its metallic frame is shown in Figure 3.13. The detailed picture of a cross-section view is shown in Figure 3.14. From the figure, the parasitic capacitance (C_{pv}) is formed in between the PV cells and grounded frame. The value of parasitic capacitance varies from nanofarads up to microfarads (Calaiset et al., 1999; Meinhardt & Mutschler., 1995). The value of parasitic capacitance depends on several issues such as the surface condition of the PV

array and frame, the distance between the PV cell to the module and the atmospheric conditions (Calais & Agelidis., 1998). Typically, the value of parasitic capacitance is chosen to simulate the behavior of the whole PV system in case of a transformerless PV installation is between the 50-150 nF/kW (Myrzik & Calais., 2003; Kerekes et al., 2007; Myrzik & Calais, 2003).

When the surface of the PV module is large, its parasitic capacitance values increases even higher than 200 nF/kWp in damp enviroments or on raining days (Myrzik & Calais, 2003). Therefore in the transformerless PV applications, the ground leakage current can reach at higher levels due to potential variations of parasitic capacitance. These high values can generate ground current with amplitudes well able the allowable stringent levels standards (Eisner., 2002). Ground leakage current can cause severe electromagnetic interferences either through conducted or radiated emission, distortion in the grid current, additional losses in the system and safety issues (Eisner, 2002; Myrzik & Calais., 2003). To minimize ground leakage currents, the common-mode voltage must be kept constant during all commutation states.

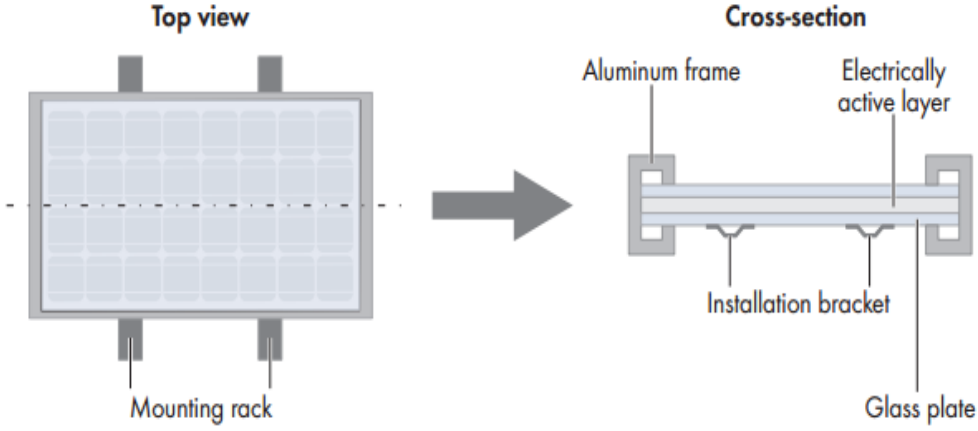


Figure 3.13: The top and cross-section view of PV module with mounting frame

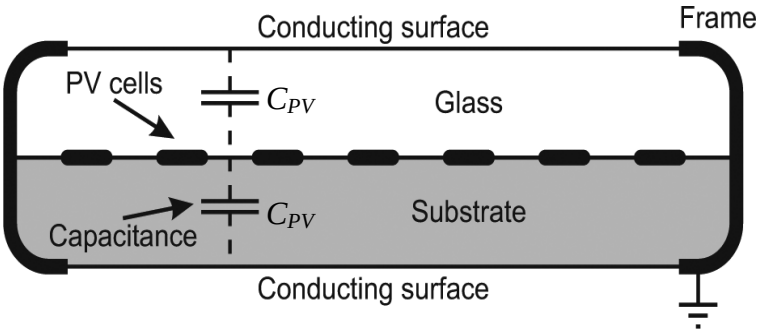


Figure 3.14: Detail cross-section of PV module

3.7 Ground Leakage Current in Transformerless PV Grid-Connected System

The cost, size and losses of the low power PV application system can be reduce when the transformers (line-transformer & high frequency transformer) is removed in the whole system. However, this system introduces additional ground leakage current in the galvanic connection between the grid and the PV panel. Due to parasitic capacitance (C_{pv}) of PV array and the ground, potential difference imposed on the parasitic capacitance through switching actions of the inverter inject a capacitive ground leakage current. The path of ground leakage current (I_g) flowing through the parasitic capacitance of the PV array is shown in dashed line in Figure 3.15. The ground leakage current is measure between neutral (N) and ground.

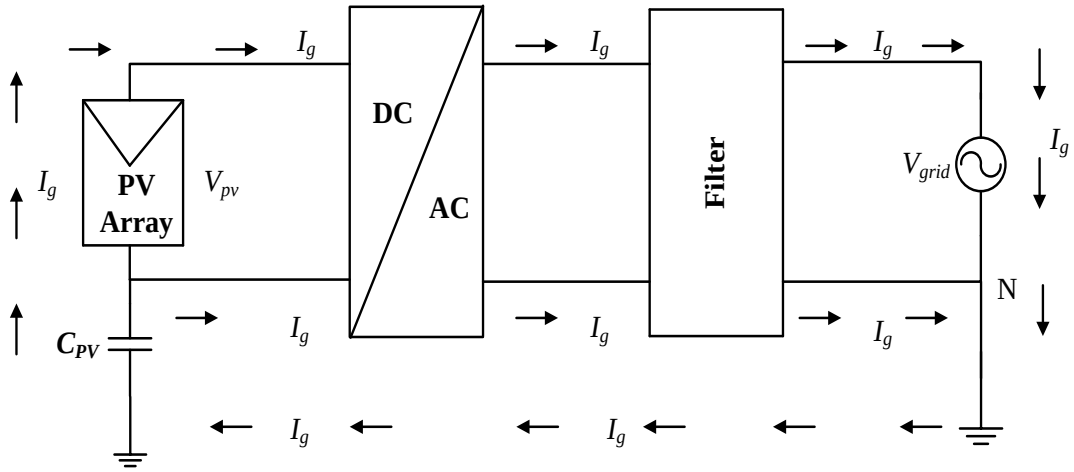


Figure 3.15: Transformerless single-phase inverter with parasitic capacitance.

The level of ground leakage current is depends on the frequency content of the voltage fluctuation of the PV terminal, which is through the parasitic capacitance. In addition, the level of parasitic capacitance will affect the level amplitude of ground leakage current (Calais, M. and Agelidis, 1998). The several recommendation to minimized the ground leakage current are listed below (Kerekes,T., 2009):

1) reducing the grounding frame of the PV array, which is reduce the capacitance;
2) choosing the correct topology and the modulation strategy, which is reducing the voltage fluctuation between PV array and ground;
3) disconnecting the inverter with corresponding disconnection time.

In order to monitor the safety issues of operation transformerless PV grid-connection system, the VDE 0126-1-1 standard according to ground leakage current is used.

3.8 Transformerless Single-Phase H-Bridge Inverter Topology

The single-phase H-Bridge inverter circuit is shown in Figure 3.16, comprising of semiconductor switches S_1-S_4 (IGBT or MOSFET), LC filter and utility grid. The ac voltage level can be synthesized from a dc source (V_{pv}) by appropriate sequence of switches. However, the combination of switches for leg 1(S_1 & S_2) and leg 2 or (S_3 & S_4) should not be closed at the same time to prevent short circuit to occur across the dc source (V_{pv}).

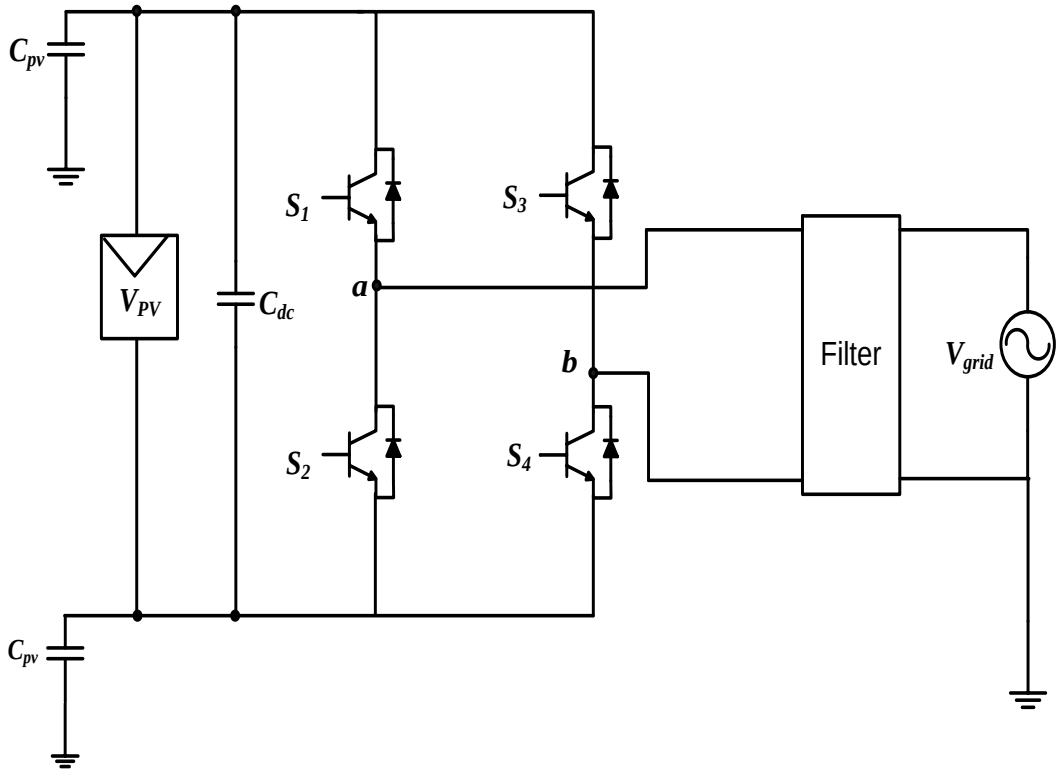


Figure 3.16: Single-phase transformerless H-Bridge inverter

Semiconductor switch is conducted in very fast times. The transition time from one conduction state to another is required to avoid shooting-through the dc source. In practice, the switch is turned off shortly before turning on the other switch in the same leg. The interval time between the turn-off and turn-on is called blanking time or dead time (Andrzej, 1998).

In the single-phase H-Bridge inverter circuit, the switches can be controlled by two switching techniques, either unipolar SPWM or bipolar SPWM. For unipolar SPWM technique, the switching uses two sinusoidal references that are 180^0 apart to modulate each phase leg switches. Assuming the power electronics switch in the inverter is ideal, the inverter's output voltage (V_{ab}) range in the positive half cycle are V_{pv} and 0, while in the negative half cycle the ranges are $-V_{pv}$ and 0, as shown in Figure 3.17. The advantage of unipolar switching technique is it offers low switching losses, low ripple grid current and grid filter elements are much smaller (Baker et al., 1997).

Figure 3.17: Output inverter voltage (V_{ab}) using unipolar PWM technique

Typically, in bipolar H-Bridge switching technique, the two level inverter output voltage (V_{pv} and $-V_{pv}$) waveform is produced (see Figure 3.18), that uses one sinusiodal reference to modulate the diagonal pair of switches (S_1 & S_4) and another pairs (S_3 & S_4) is switched alternatively at the switching frequency. The disadvantage of using the bipolar switching technique is low power converter efficiency due to large ripple grid current when the same filter value as the unipolar technique is used. Its drawback is also the high switching losses due to dual switches being turned on at same time.

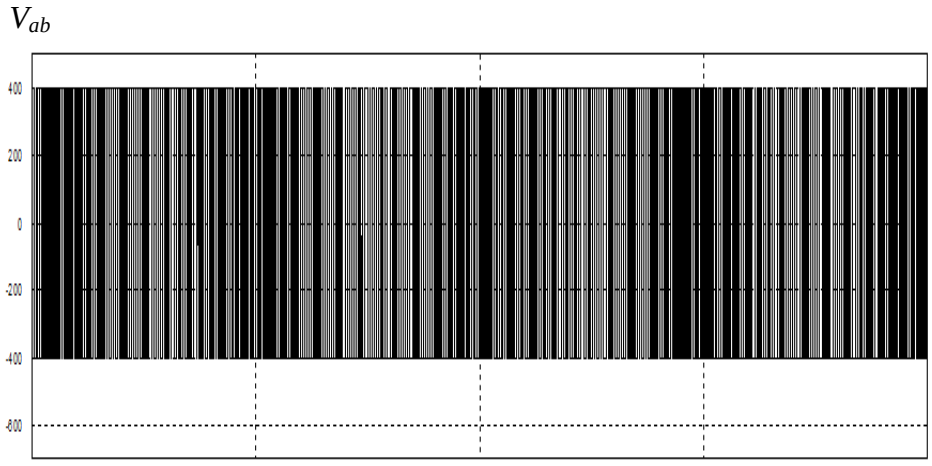


Figure 3.18: Output inverter voltage (V_{ab}) using bipolar PWM technique

3.9 Common-Mode Voltage Model in Transformerless Single-Phase H-Bridge Inverter Topology

Since the PV panel and grid are not isolated (without transformer), a common-mode resonant circuit appears, which consists of parasitic capacitance (C_{pv}), H-Bridge inverter, LC filter and utility grid. Figure 3.19 represents the behaviour of a common-mode resonant circuit model system (Gubia et al., 2007; Gonzalez Roberto et al., 2008; Ivan, 2011). This model has the common-mode voltage (V_{cmm}) and differential-mode voltage (V_{dm}) of an H-Bridge power inverter output. The inverter output is indicated by points *a* and *b*. In the transformerless PV system, the ground leakage current can be analyse with the help of both power inverter voltages (V_{cmm} & V_{dm}). The common-mode voltage (V_{cmm}) is the average of two-inverter output voltage as defined in (3.17). The common reference is taken from the negative terminal of PV panel as marked with "*o*".

$$V_{cmm} = \frac{V_{ao} + V_{bo}}{2} \tag{3.17}$$

The voltage difference between two-output power inverter is defined as differential-mode voltage (V_{dm}), which is defined in (3.18).

$$V_{dm} = V_{ao} - V_{bo} \tag{3.18}$$

From (3.17) and (3.18), the output power inverter voltage terminals and negative terminal can be expressed as in (3.19) and (3.20).

$$V_{ao} = \frac{V_{dm}}{2} + V_{cmm} \tag{3.19}$$

$$V_{bo} = -\frac{V_{dm}}{2} + V_{cmm} \tag{3.20}$$

According to (Bo Yang et al., 2012; Yunjie & Wuhua, 2013), the model of Figure 3.20 can be rearranged by using Thevenin's theorem and simplified equivalent model of common-mode resonant circuit, which is shown in Figure 3.21. The inverter equivalent common-mode voltage (V_{ecmm}) is defined in (3.21).

$$V_{ecmm} = V_{cmm} + \frac{V_{dm}}{2}\left(\frac{L_{f2} - L_{f1}}{L_{f1} + L_{f2}}\right) \tag{3.21}$$

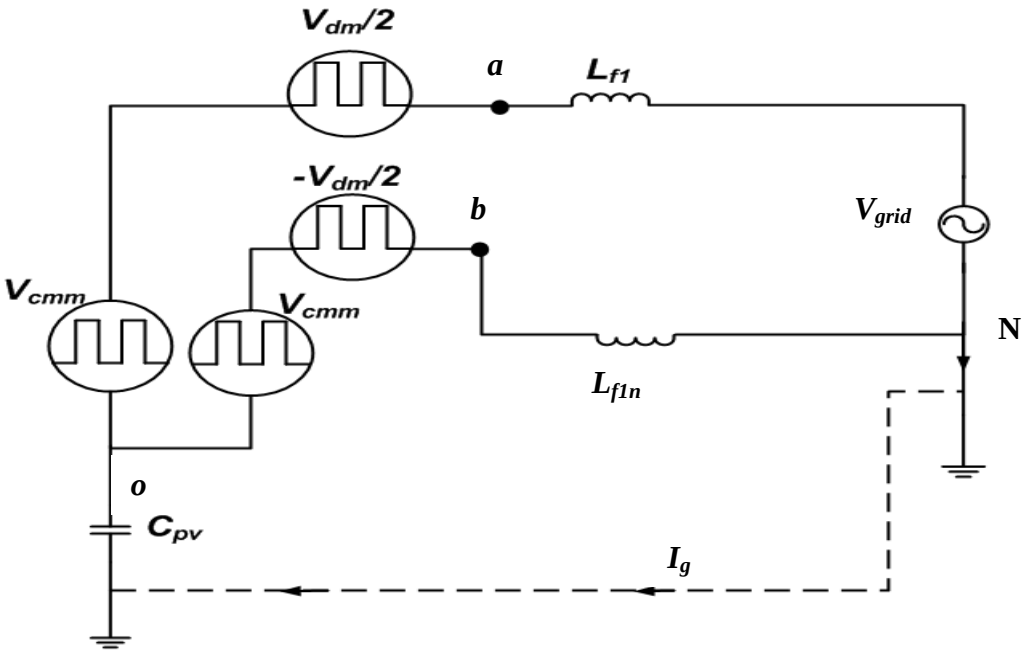


Figure 3.19: The common-mode model for the PWM voltage source inverter system

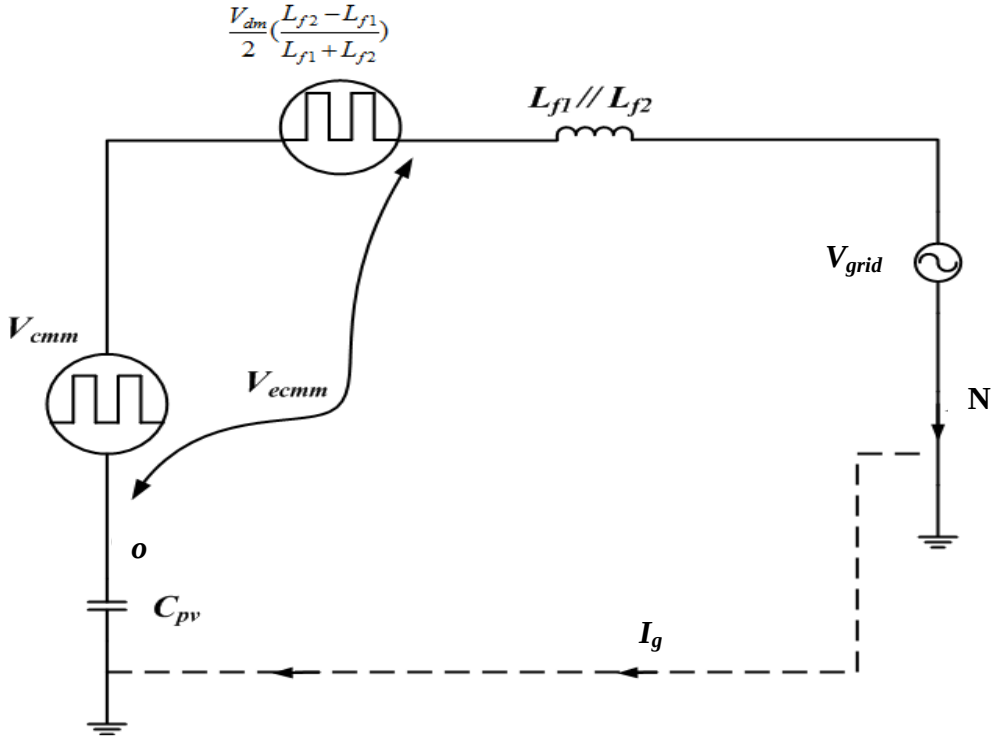


Figure 3.20: Simplified equivalent model of common-mode resonant circuit

In the H-Bridge inverter, the filter inductors (L_{f1} and L_{f2}) are usually selected with the same values. As a result, the inverter equivalent common-mode voltage is only defined by inverter common-mode voltage (V_{cmm}) as expressed in (3.22) and modeled in Figure 3.21.

$$V_{ecmm} = V_{cmm} = \frac{V_{ao} + V_{bo}}{2} \tag{3.22}$$

In addition, from the model of Figure 3.25, it can be seen that the ground leakage current (I_g) is excited by the defined inverter common-mode voltage (V_{cmm}) circuit. Compared to the inverter switching frequency, the grid frequency is low; therefore, the ground leakage current caused by the grid could be ignored (Gonzalez Roberto, at el., 2008).

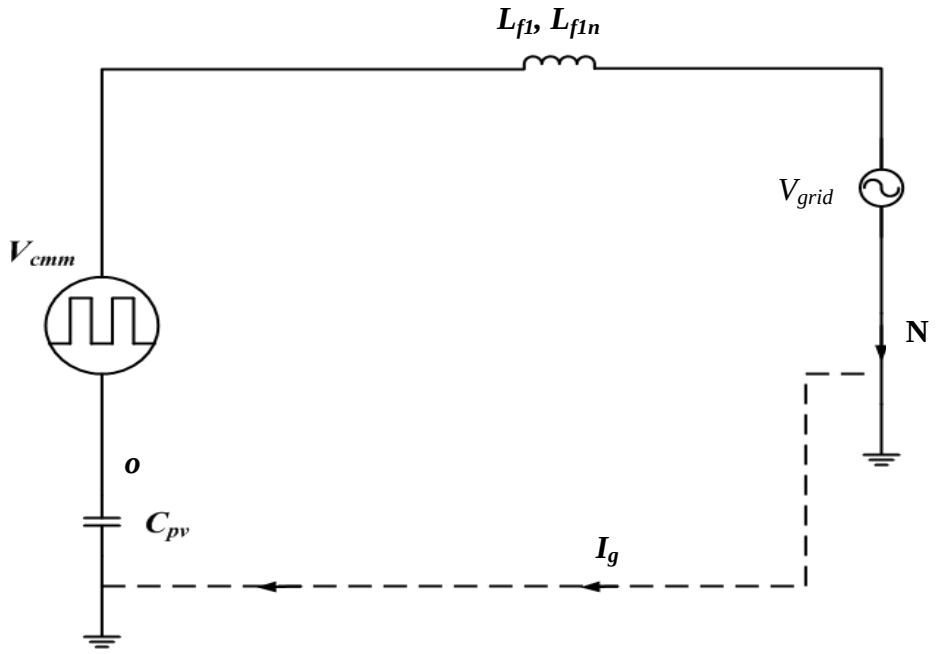


Figure 3.21: Equivalent circuit for the common-mode leakage current path

Finally, the ground leakage current depends only on the variations of the inverter common-mode voltage which is defined in (3.23) (Gonzalez Roberto, et al. , 2006).

$$I_g = C_{PV} \frac{dV_{cmm}}{dt} \tag{3.23}$$

From (3.23), to avoid high common-mode current, (or ground leakage current) (I_g < 300 mA) flowing through the common-mode model circuit, the variation of inverter common-mode voltage ($\frac{dV_{cmm}}{dt}$) should be kept constant.

3.10 Fourier Analysis of the Common-mode Voltage

In general, the symmetrical sampling SPWM produces symmetrical trapezoidal voltage waveforms. For Fourier analysis of symmetrical voltage waveform the switched inverter output voltages V_{ao} and V_{bo} of both legs can be represented as follows (Xuejun, et al., 2004):

$$V_{ao} = \frac{2V_d T}{n^2 \pi^2 \tau} \sin \frac{n\pi\tau}{T} \sin \frac{n\pi(d_1 T + \tau)}{2T} e^{j\frac{2n\pi\tau}{T}} \tag{3.24}$$

$$V_{bo} = \frac{2V_d T}{n^2 \pi^2 \tau} \sin \frac{n\pi\tau}{T} \sin \frac{n\pi(d_2 T + \tau)}{2T} e^{j\frac{2n\pi\tau}{T}} \tag{3.25}$$

Substituting (3.24) and (3.25) into (3.26) yields the absolute value of the common-mode voltage as,

$$\left| \frac{V_{ao} + V_{bo}}{2} \right| = \left| \frac{2V_d T}{n^2 \pi^2 \tau} \sin \frac{n\pi\tau}{T} \sin \frac{n\pi(d_1 T + d_2 T + 2\tau)}{2T} \cos \frac{n\pi(d_1 - d_2)}{2} \right| \tag{3.26}$$

where V_d is the DC bus voltage, T is the switching period, τ is the rise and fall time constant (both), and t_r and t_f are the rise time and the fall time respectively. The duty cycles of V_{ao} and V_{bo} are sequentially represented by d_1 and d_2.

3.11 Modified Transformerless Single-Phase H-Bridge Inverter Topologies

Previously, various modifications of H-Bridge inverter topologies were presented in order to keep the common-mode voltage constant (behaviour as in case of bipolar PWM). The modified H-Bridge inverter also generates low ground leakage ground that is suitable for transformerless PV system. The low ground leakage current in transformerless single-phase H-Bridge inverter topologies using the unipolar SPWM technique are achieved by disconnecting the PV array from the grid during zero vectors state. The disconnection can also be done by either ac-bypass or dc-bypass. Ac-bypass is an additional switch on the inverter ac-side, between the H-Bridge inverter and the grid, whereas dc-bypass is between the H-Bridge inverter and the PV array. Ac-bypass is proposed for HB-ZVR (H-Bridge Zero-Voltage Rectifier) (Kerekes at el., 2011; Selvaraj & Rahim, 2009) and HERIC (High-Efficiency Reliable-Inverter Concept)

(Heribert et al., 2003). Dc-bypass was introduced in H6, H5, and oH5 topologies (Gonzalez Roberto at el., 2007; German, 2006; Huafeng Xiaoet al., 2011).

Another solution is by connecting the mid-point of a dc-link capacitor to the neutral line of the grid as a neutral point capacitor (NPC) topology (Lin et al., 2009; Huafeng & Shaojun, 2012). However, this topology requires high voltage dc-link of up to 700V. Furthermore, the half bridge topology can be used in the transformerless PV system due to the fact that the middle point of DC-link capacitors are always connected to the neutral wire (Schekulin, 1996). Due to this connection, the common-mode voltage remains constant. As a result, the ground leakage current is below the VDE-0126-1-1 standard, thus satisfying the requirement.

3.12 HERIC Topology

In (Schmidt et al, 2003), it presents the modification of H-Bridge inverter circuit to a topology called HERIC. Figure 3.22 is the HERIC topology with additional switches (S_5 & S_6) at the ac side to disconnect the inverter circuit from the grid element during freewheeling or zero vector condition. The zero vectors are achieved by way of either S_5 or S_6 depending on the sign of the half-wave. S_5 is conducting when pair S_2-S_3 is in freewheeling period and S_6 with the corresponding pair S_1-S_4.

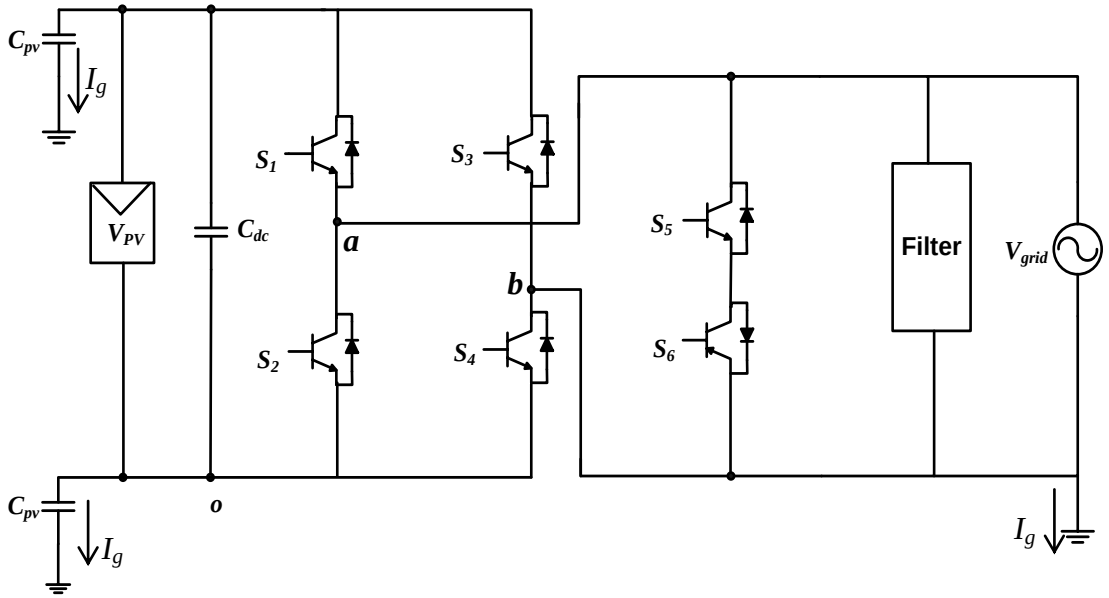


Figure 3.22: HERIC topology

As has been discussed in the previous section, when transformer is omitted in the whole PV inverter system, the problems of safety hazard are encountered. The ground leakage current (I_g) is clamped through the PV parasitic capacitance (C_{pv}).

3.13 HB-ZVR Topology

Another solution to disconnect the PV array system from the grid is by using the HB-ZVR topology as shown in Figure 3.23 (Tamas et al., 2009). In this circuit, the auxiliary switch; S_5 is attached as an ac-bypass switch at the ac side. During the positive half cycle S_1 and S_4 are commutated at switching frequency. S_5 is commutated inversely with S_1 and S_4 operation, while S_2 and S_3 are turned OFF at this time. Meanwhile, in the negative half cycle S_2 and S_3 were commutated at switching frequency. Moreover, S_5 switching position is the opposite of S_2 and S_3. During this cycle, S_1 and S_4 are in the OFF state condition.

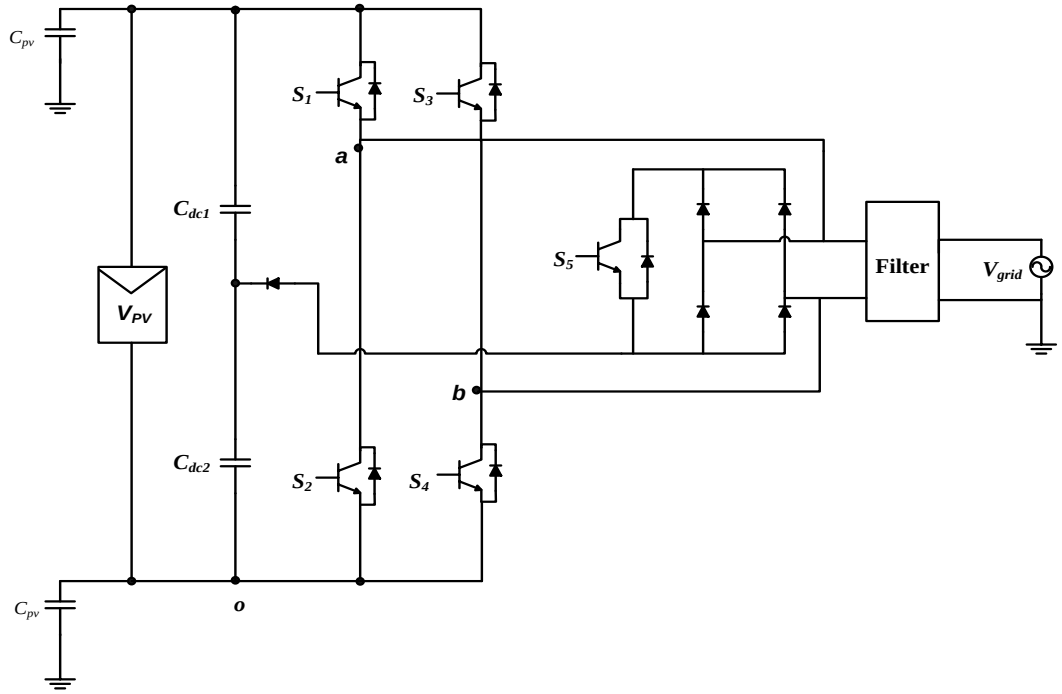


Figure 3.23: HB-ZVR topology

3.14 H6 Topology

Another solution to produce constant common-mode voltage is by disconnecting the PV array system from the grid in the DC side (dc-bypass). The additional switch connects at the line and the neutral part of the DC side in the H6 topology as shown in Figure 3.24. During the positive half wave, switches S_1 and S_4 are ON at low frequency (50Hz). When switches S_1 and S_4 are OFF, S_5 and S_6 commutate at high switching frequency. During the negative half cycle, S_2 and S_3 are ON, whereas S_5 and S_6 commutate at high switching frequency.

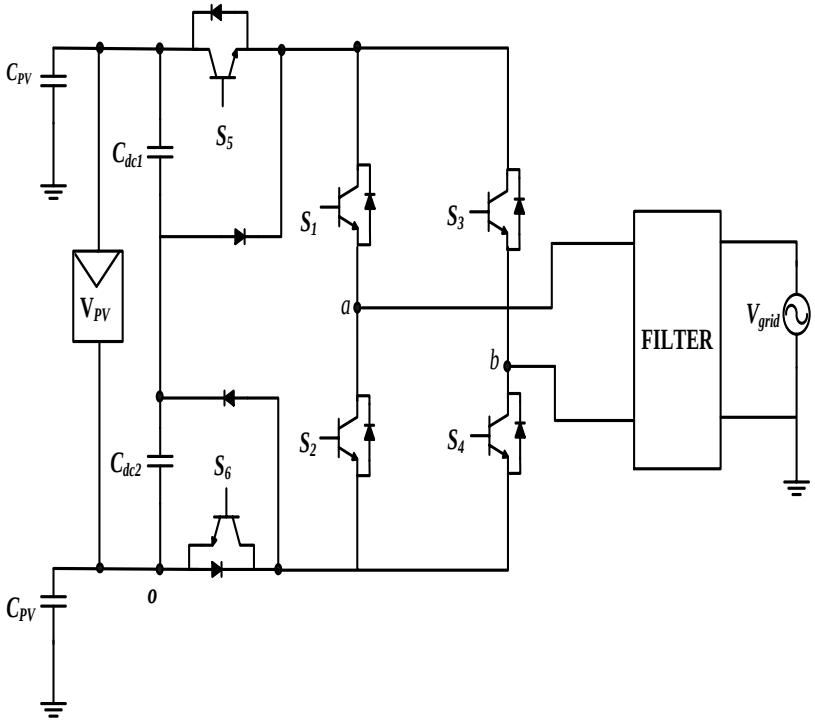


Figure 3.24: H6 topology (German Patent, 2003)

3.15 H5 Topology

Another modification of H-Bridge inverter with a dc-bypass circuit at the DC side of the inverter is introduced in (German, 2006). In Figure 3.25 (H5 topology), during the positive half wave, S_1 is switched ON with low frequency and S_4 is commutating at high frequency. During the negative half wave, switches S_2 and S_3 respectively function at low and high frequencies. Switch S_5, however, is always switching at high frequency during both cycles.

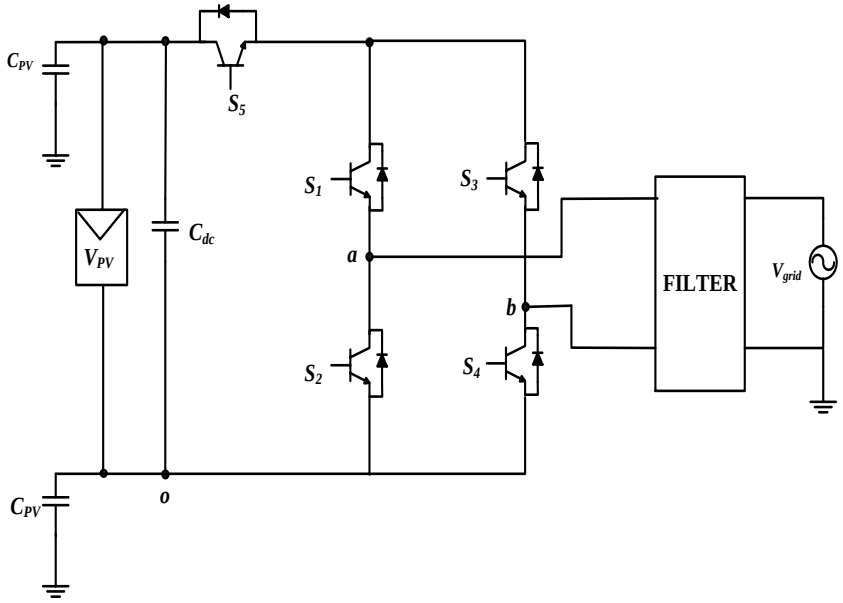


Figure 3.25: H5 topology

3.16 oH5 Topology

The oH5 topology as shown in Figure 3.26 have two additional switches (S_1 and S_2) on the DC side and commutate alternately at high switching frequency. S_2 connects at the two midpoints of the dc-link capacitors. During positive and negative cycles and at high frequency, S_3 & S_4 operate alternately with S_5 & S_6.

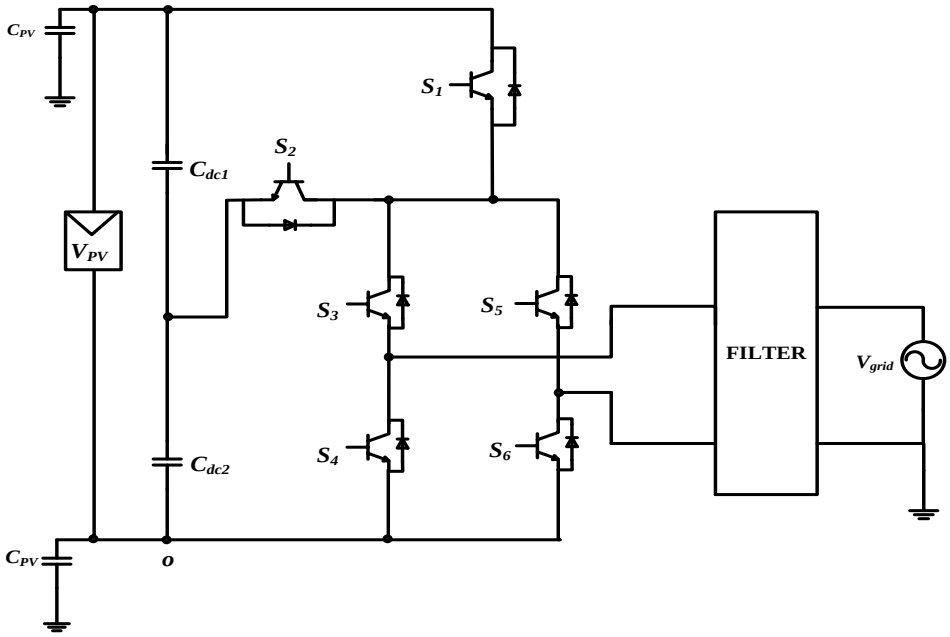


Figure 3.26: oH5 topology (Huafeng et al., 2011)

3.17 Half Bridge Topology

The half bridge topology has been introduced in (Schekulin, 1996). This topology only has two switches (S_1 & S_2) and the middle point between the two DC links capacitors (C_1 & C_2) are connected to the neutral grid as shown in Figure 3.27. The upper switch (S_1) is operated when the output is positive. Otherwise, when negative output voltage is required, the lower switch (S_2) is operated. Due to the connection of DC-link capacitors middle point and neutral grid, the remaining common-mode voltage is half of the PV voltage input. As a result, the ground leakage current is near to zero amplitude. Because of a small ground leakage current, this topology is suitable for transformerless PV grid-connected system. However, this topology's disadvantage is that higher input voltage is needed, which increases the rating of the components.

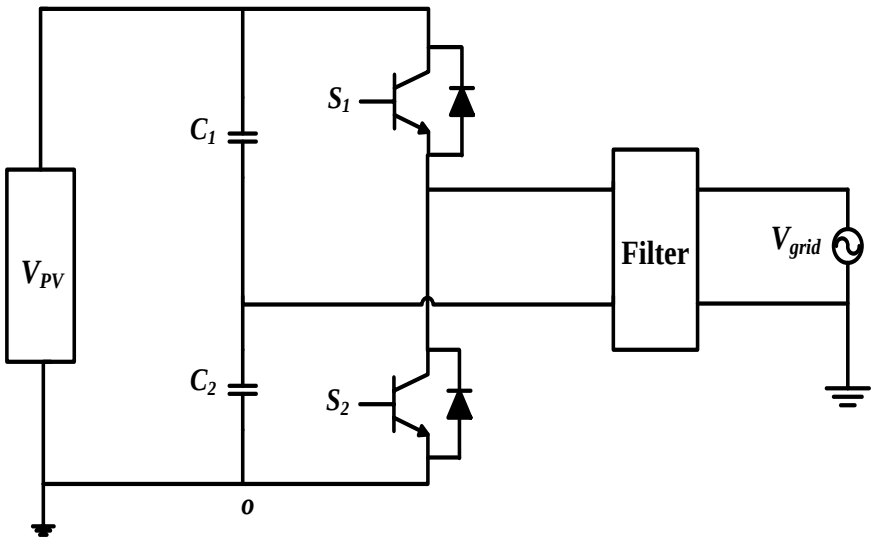


Figure 3.27: Half bridge inverter topology

3.18 Neutral Point Diode Clamped (NPC) Topology

The NPC inverter topology is shows in Figure 3.28, which have four switches (S_1-S_4) and two diodes (D_1 & D_2). The middle point of both DC-link capacitor (C_1 & C_2) is connected to the neutral grid. The positive inverter voltage output is generated by

turning on the switches (S_1 & S_2). On the other hand, the switches (S_3 & S_4) are turned on to generated the negative inverter voltage output. The zero output voltage is generated by turning on S_2 and S_3. This topology produces the constant common-mode voltage and reduces leakage ground current due to the connection of the middle point of the DC-link capacitors to the neutral grid. Unfortunately, these topologies require the boost stage before the inverter, which has to be twice the grid peak voltage.

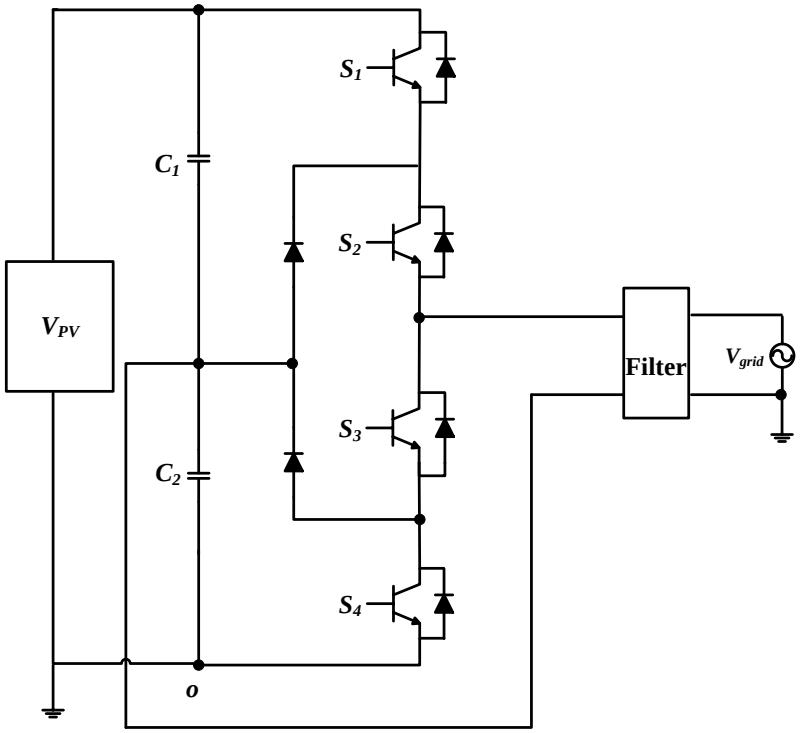
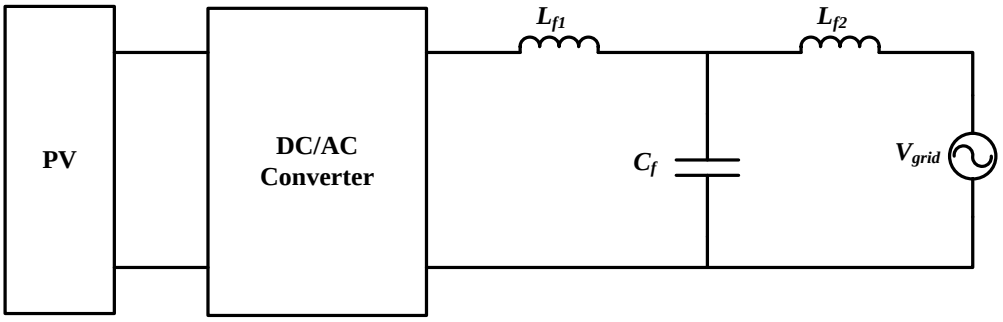


Figure 3.28: NPC inverter topology

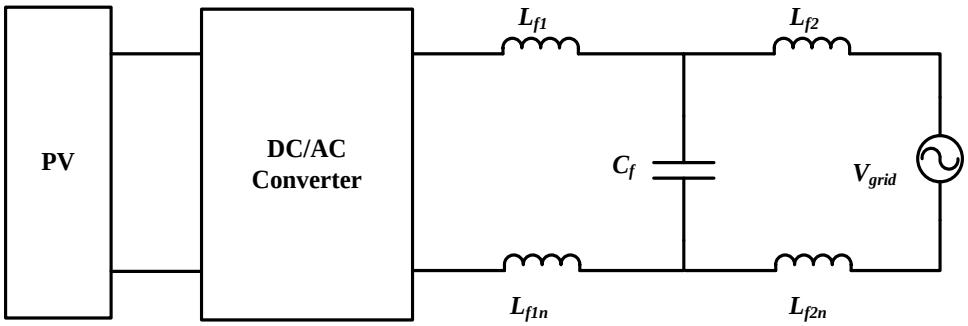
3.19 Filter Configuration and Ground Leakage Current

At the grid side, the two LCL filters can be considered, as presented in Figure 3.29. In Figure 3.29(a), only inductor (L_f) is connected at line branch as in case 1). In Figure 3.29(b) the inductor (L_f) split equally between line and neutral branch (as in case 2). The LCL filter configuration has better decoupling between the filter and grid impedance (Araujo et al. 2007). Due to the advantage of LCL filter configuration compared to L and LC filter configuration, the LCL filter configuration has been used

for grid side filter. The inverter current ripple is identical for both filter configurations (case 1 and case 2), although the ground leakage current is greatly influenced by the filter configuration, as present in experimental results.



(a): case 1



(b): case 2

Figure 3.29: (a) LCL filter configuration case (1), (b) LCL filter configuration case (2)

3.20 Comparison of Transformerless Single-Phase H-Bridge Inverter Topologies

The simulation of the transformerless single-phase inverter, which is the conventional H-Bridge (unipolar SPWM and bipolar SPWM), H-Bridge inverter with ac-bypass and dc-bypass topologies were performed using the PSIM 9.0 software. All the topologies use the same component and parameter. The parasitic capacitance was added at the DC generator supply to simulate the ground leakage current in the whole

system. To obtain good decoupling between the filter and grid impedance, the LCL filter configuration is used.

As have been discussed in the previous section, when transformer is omitted in the whole PV inverter system, the problems of high ground leakage current and safety electrical hazard are encountered. These problems can be investigated by observing the behaviour of common-mode voltage in the transformerless inverter topology. The common-mode voltage (V_{cmm}) can be measured at two-inverter output voltage (V_a & V_b) and common reference (o). The ground leakage current (I_g) is clamped through the parasitic capacitance (C_{pv}). For the case of unipolar SPWM transformerless H-Bridge inverter circuit as shown in Figure 3.30, the common-mode voltage is not constant (see Figure 3.30 (a)) and causes the high ground leakage current (I_g) as shown in Figure 3.30(b). Therefore, this topology with unipolar PWM technique is not suitable for transformerless PV inverter application. On the other hand, when using bipolar PWM technique in H-Bridge topology, the common-mode voltage (V_{cmm}) is constant as shown in Figure 3.31(a). For that reason, the ground leakage current (I_g) is low at nearly 0 A as shown in Figure 3.31(b).

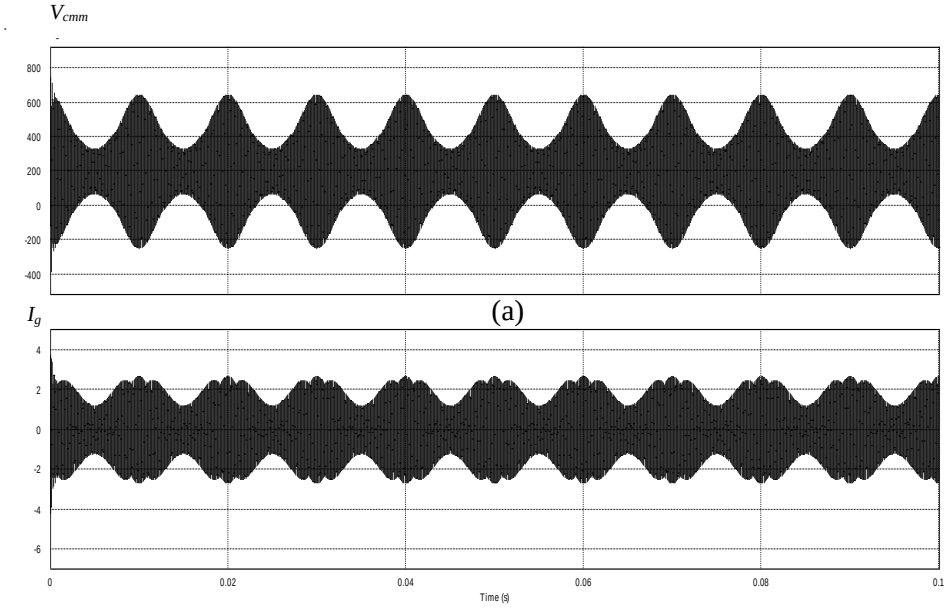


Figure 3.30: (a) Common-mode voltage and (b) ground leakage current when unipolar SPWM technique is used

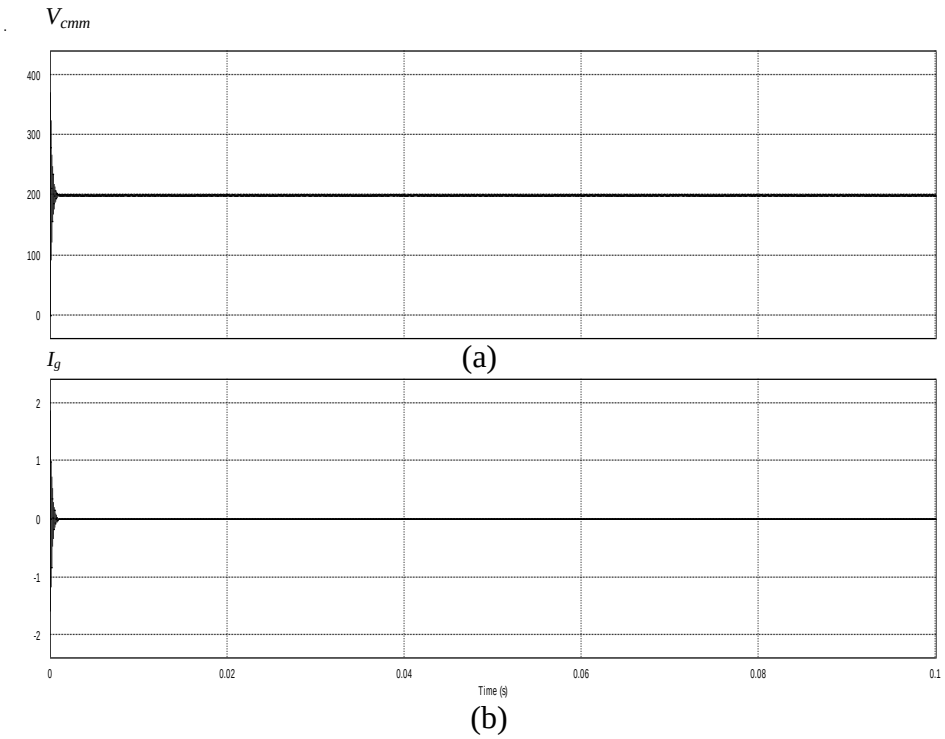


Figure 3.31: (a) Common-mode voltage (V_{cmm}) and (b) ground leakage current when bipolar PWM technique is used

The combination of high efficiency unipolar modulation and constant common-mode voltage of bipolar modulation were introduced in the modified transformerless single-phase H-Bridge inverter topologies. They are two types of modified categories; to disconnect the PV array system from the grid line that are ac-bypass and dc-bypass. Both of them offer high efficiency, constant ground voltage and low ground leakage current.

Focusing on the ac-bypass topologies, HERIC and HB-ZVR topology generates no varying common-mode voltage and low ground leakage current as shown in Figure 3.32 and Figure 3.33. The HERIC topology offers high efficiency due to additional switches (S_5 and S_6) commutated at low switching frequency compared to the HB-ZVR topology. However, in the case of HB-ZVR, it does not matter which direction the grid current is flowing. This current can find a path through the bidirectional switch that consists of one IGBT device (S_5) and a diode bridge. Nevertheless, in the HERIC approach, the direction current needs to be defined first (Gubiael, 2007).

The H-Bridge topologies with dc-bypass also offer constant common-mode voltage and low ground leakage current as shown in Figures 3.34, 3.35 and 3.36. The H5 topology has higher efficiency topologies due to fewer components compared to the other dc-bypass topologies.

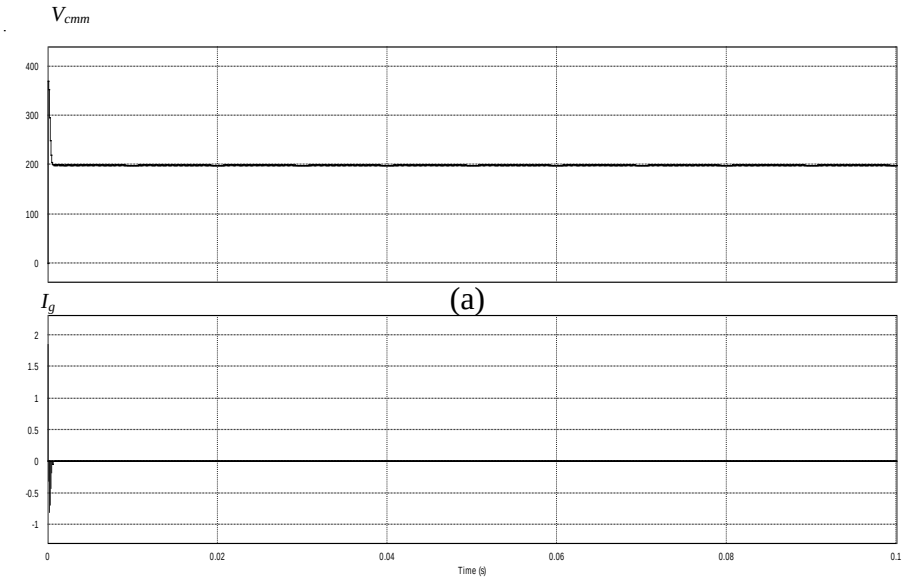


Figure 3.32: (a) Common-mode voltage and (b) ground leakage current in case of HERIC topology

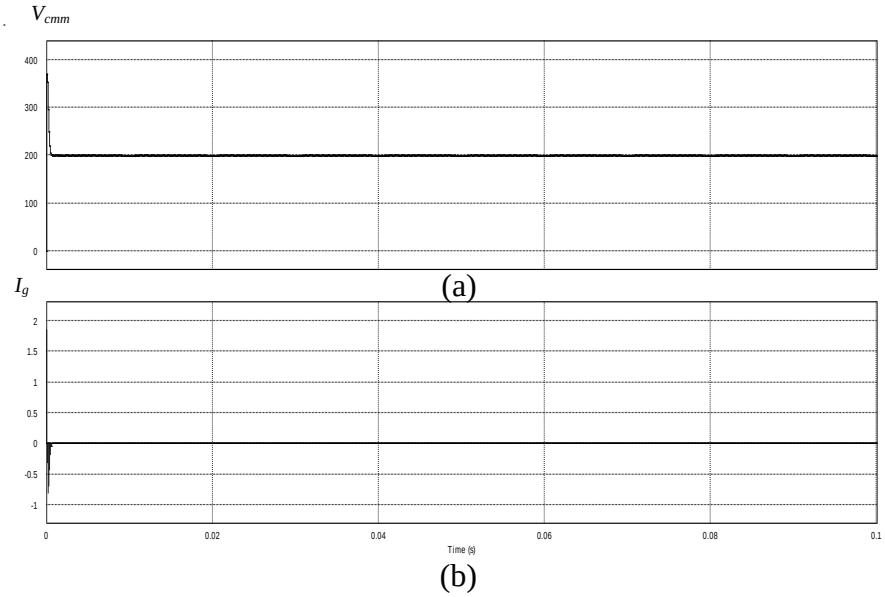
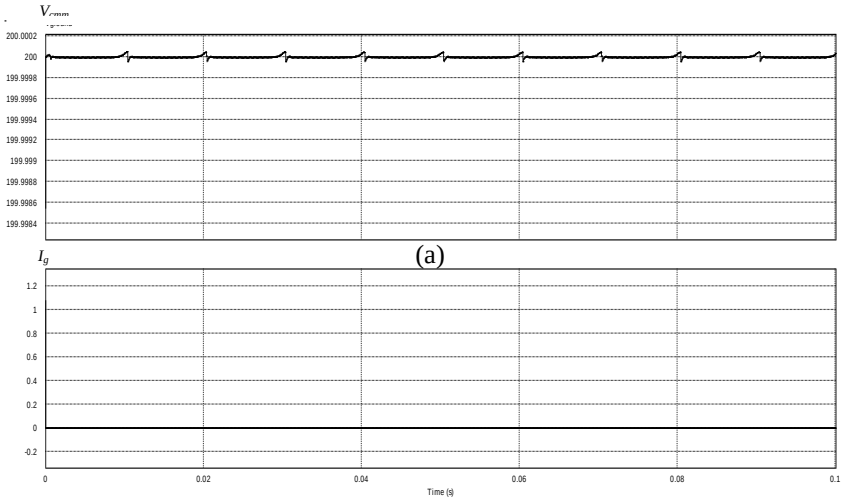


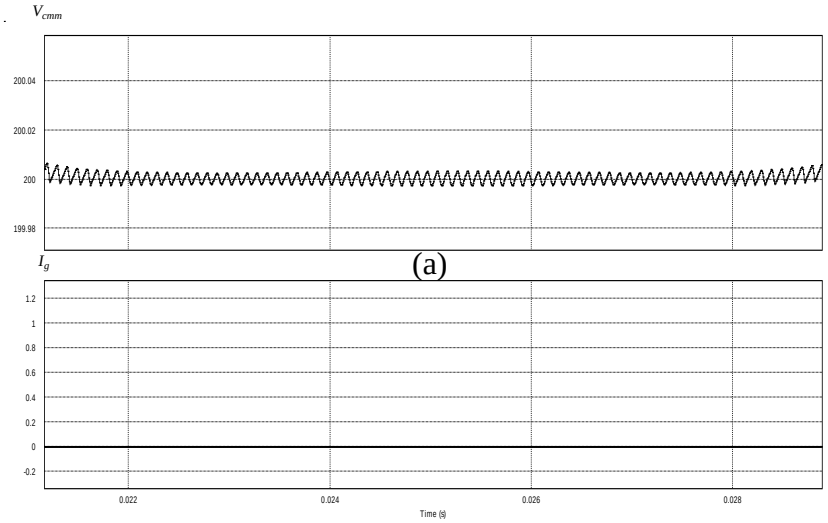
Figure 3.33: (a) Common-mode voltage and (b) ground leakage current in case of HB-ZVR topology



(a)

(b)

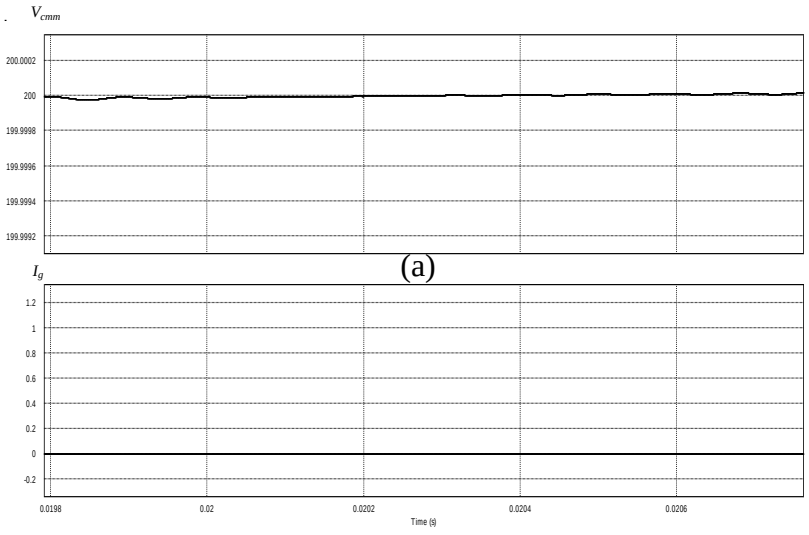
Figure 3.34: (a) Common-mode voltage and (b) ground leakage current in case of H6 topology



(a)

(b)

Figure 3.35: Common-mode voltage and ground leakage current in case of H5 topology



(a)

(b)

Figure 3.36: Common-mode voltage and ground leakage current in case of oH5 topology

The advantages and disadvantages of the selected transformerless inverter topologies are illustrated in Table 3.3.

Table 3.3: Advantages and disadvantages of selected topologies

Topology	Advantages	Disadvantages
H-Bridge Unipolar	-High efficiency -Three level output inverter voltage	-Large ground leakage current
H-Bridge Bipolar	-Low ground leakage current level	-Low efficiency -Two level output voltage
HERIC	-High efficiency -Three level output voltage -Low ground leakage current	-Current can only flow in a predefined direction
H5	-High efficiency -Three level output voltage -Low ground leakage current	-Short lifetime of the additional switch (S_5)
HB-ZVR	-Three level output voltage -Low ground leakage current -Not matter the direction of load current.	-Slightly low efficiency compare to HERIC topology

3.21 Single-Phase Multilevel Inverter Topologies

The multilevel cascaded converter topology without transformer components has been proposed in (Peng, at. el. 1996) and is shown in Figure 3.37. This topology consists of two full-bridge circuits and an AC output is connected in series. Each bridge can create three different voltage levels at its AC output, allowing for an overall five-level AC output voltage. This converter can be a good solution for using small dc bus voltage and THD improvement. However, the drawback of this converter is its control complexity and increased number of solid-state device (IGBTs and diodes). In addition, the commutation and conduction losses of solid-state devices can increase.

The single-phase five level diode clamped inverter topology is show in Figure 3.38. The two leg of inverter is connected to the mid-point of split capacitor (V_{c1} and

V_{c2}). In (Hung & Corzine; 2006), the flying capacitor multilevel inverter topology as shown in Figure 3.39 has been presented. This topology is not requiring additional clamping diode. However, the additional circuit is needed to identify initial capacitors charge. The modified H-Bridge multilevel inverter as shown in Figure 3.40 was applied to PV application has been proposed in (Rahim et al., 2010). The modified inverter consists of one auxiliary circuit that it four diodes and one switch. The input multistring PV sources are connected to the inverter via the DC-DC converter.

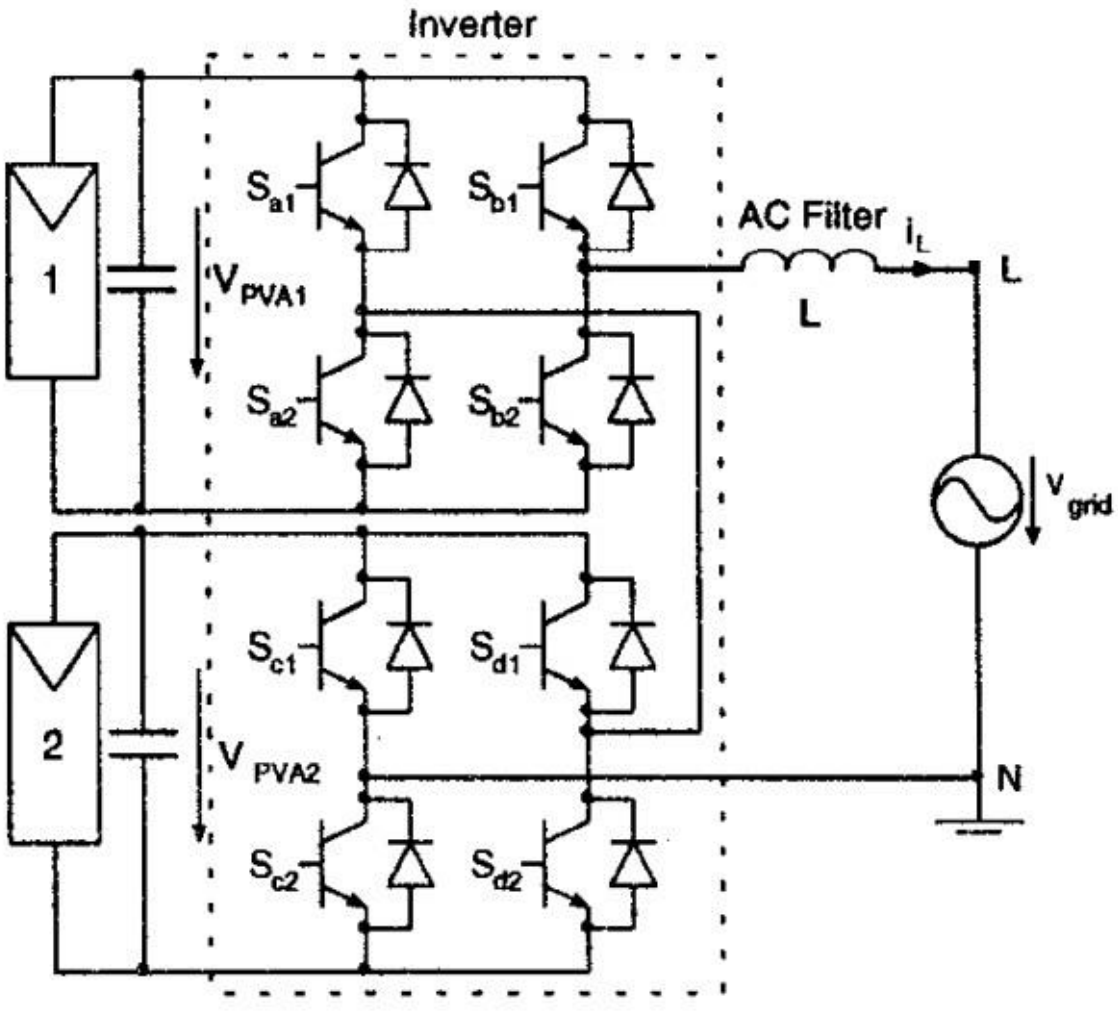


Figure 3.37: Transformerless multilevel cascade inverter (F. Peng at el., 1996)

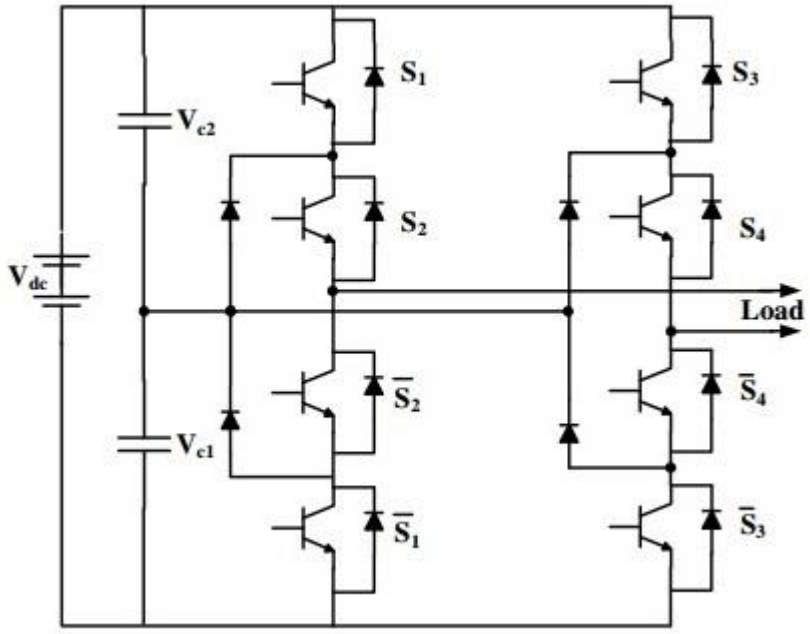


Figure 3.38: Single phase five level diode clamped inverter topology (Manjrekar M.D & Lipo T.A., 1998)

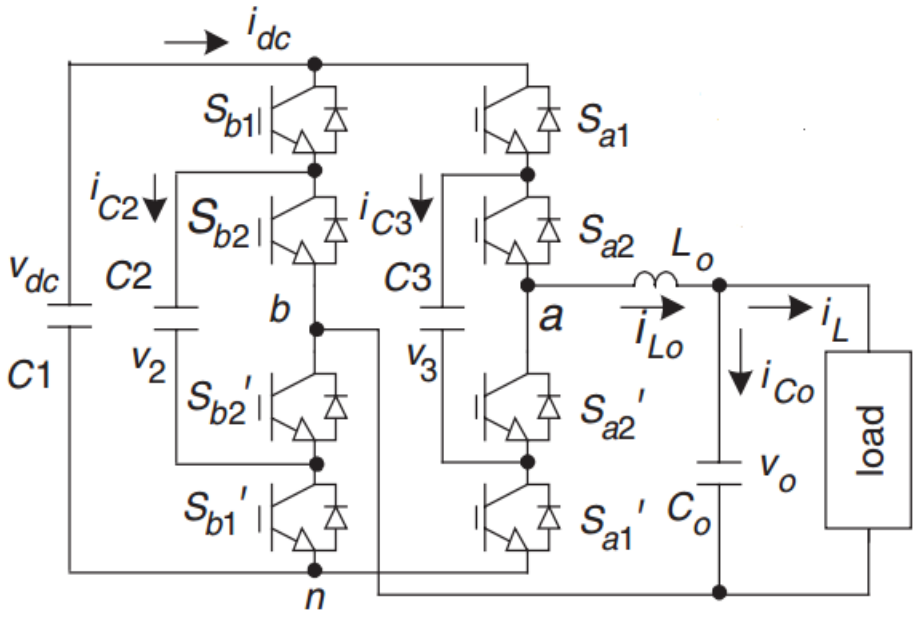


Figure 3.39: Flying capacitor topology (Hung & Corzine, 2006)

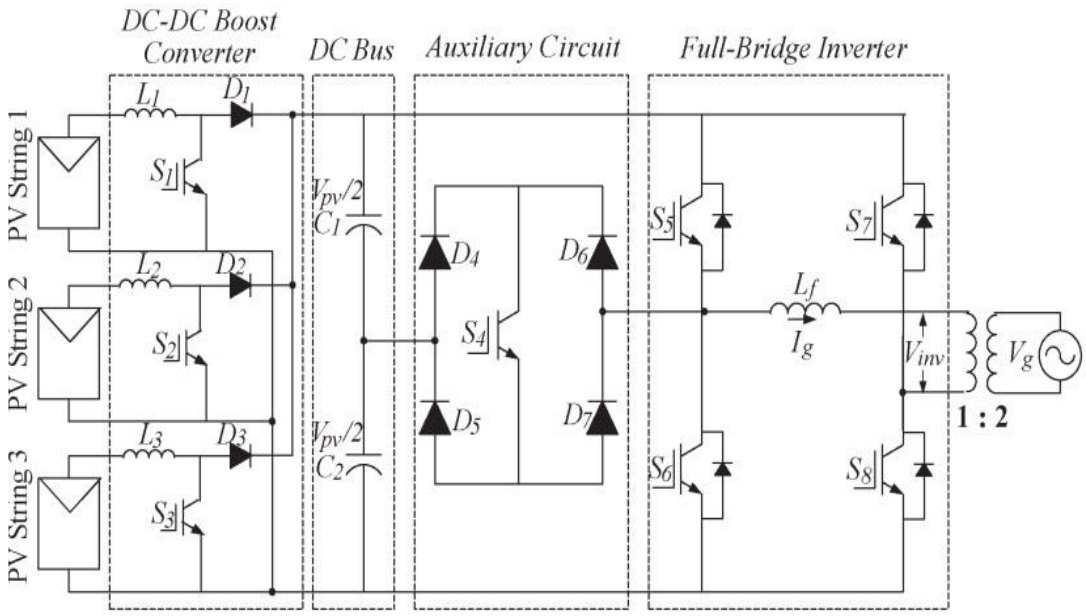


Figure 3.40: Multistring five-level single phase inverter (Rahim et al., 2010)

3.22 Module Integrated Converter (MIC) Topologies

Typically, the value of the open-circuit PV module voltage is below 45 V. Therefore, the MIC topologies have been a future trend for the PV grid-connected system. The implementation of MIC technology is shown in Figure 3.41.

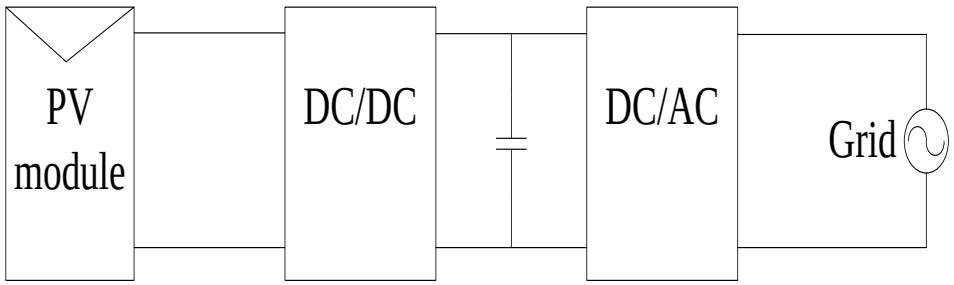


Figure 3.41: MIC arrangement

The MIC single-phase PV grid-connected with H-Bridge inverter topologies have been proposed as shown in Figures 3.42, 3.43, 3.44 and 3.45. In (J.Myrzik &

M.Calais, 2003), the single phase H-Bridge inverter by added the boost converter as shown in Figure 3.46 is proposed for PV grid-connected system.

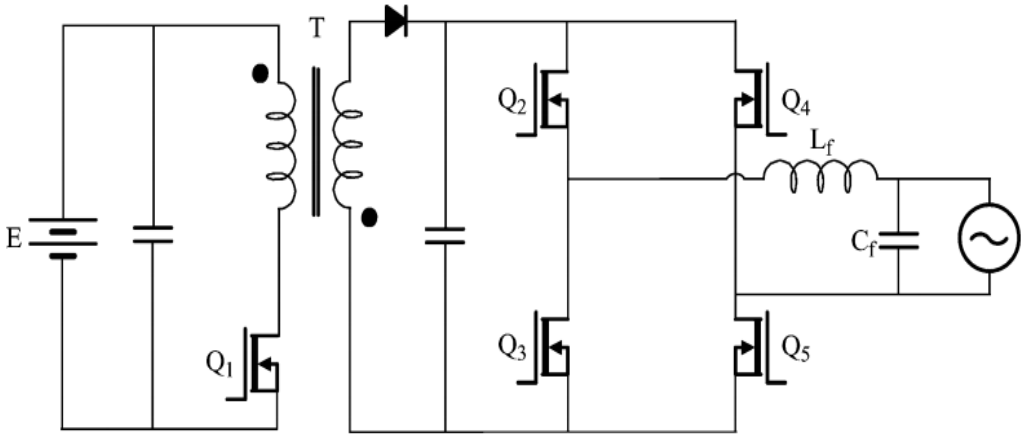


Figure 3.42: Grid-Connected PV system using two energy processing stages (Martin & Demonti, 2002)

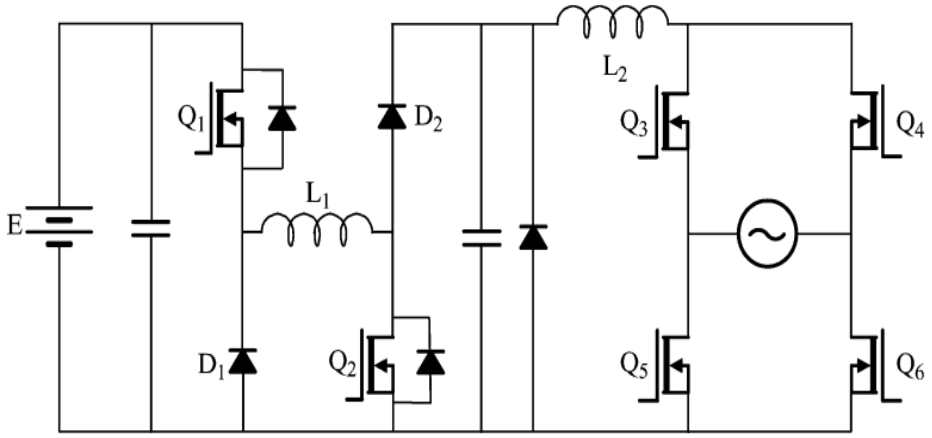


Figure 3.43: Modified inverter configuration (Saha et al., 1998)

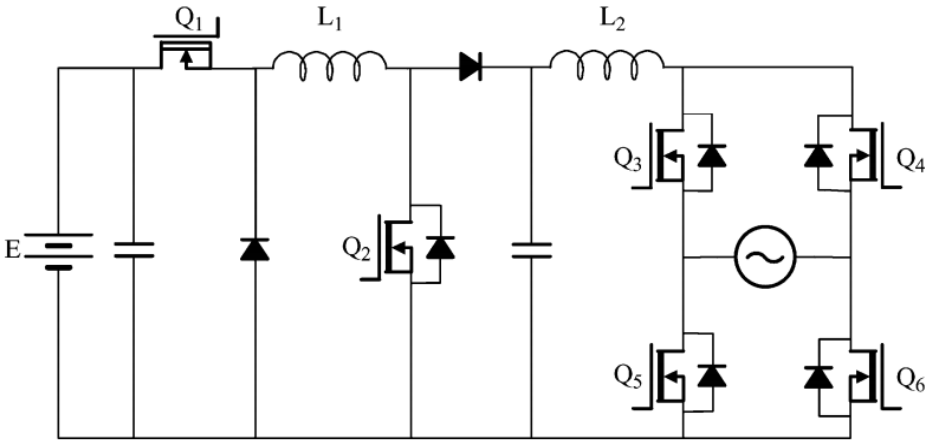


Figure 3.44: Two-stage photovoltaic grid-connected inverter (Chomsuwans et al., 2002)

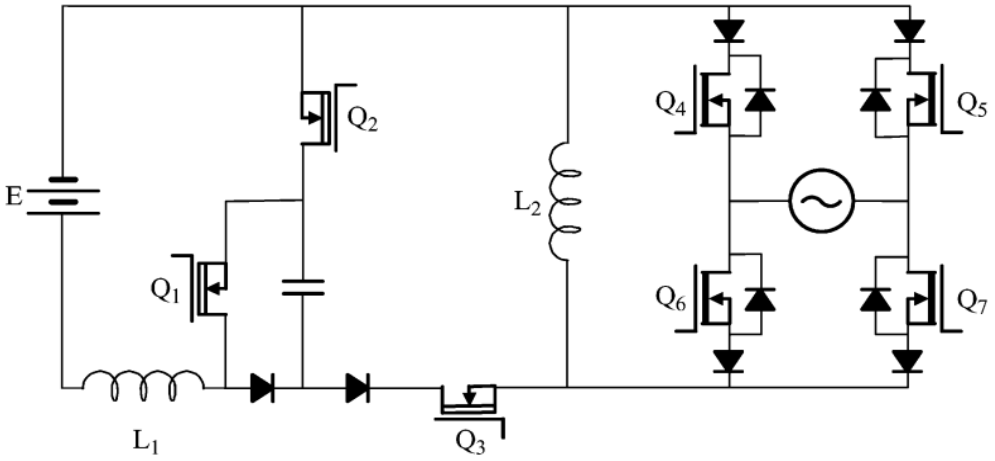


Figure 3.45: Buck-boost-operation-based sinusoidal inverter circuit (Funabikiet et al., 2002)

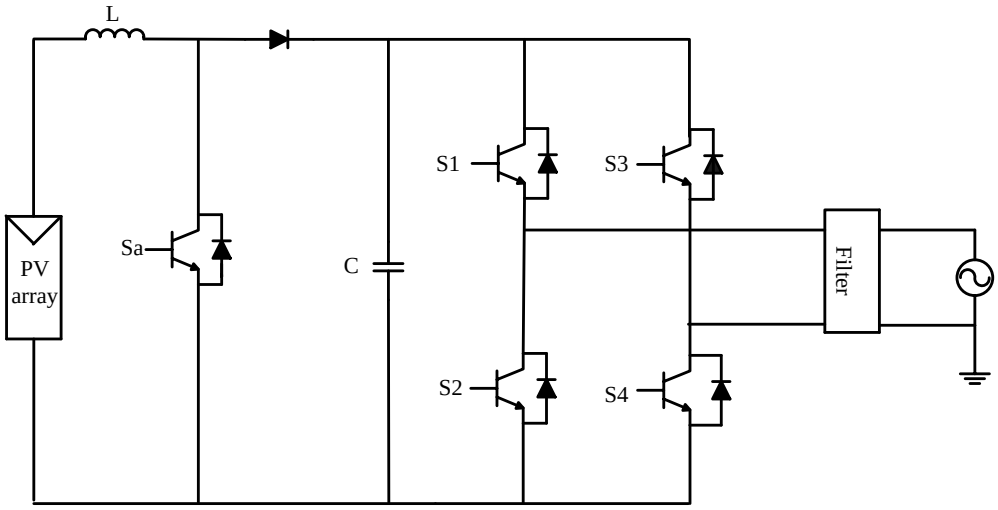


Figure 3.46: Transformerless PV inverter with DC-DC boost converter

Another way of boost single stage inverters is show in Figure 3.47. The inverter consists of two current bidirectional boost DC-DC converters (Boost A and Boost B). The both converters are modulated and produce a unipolar dc-biased sine wave output. Between each converter having 180^0 phase shift.

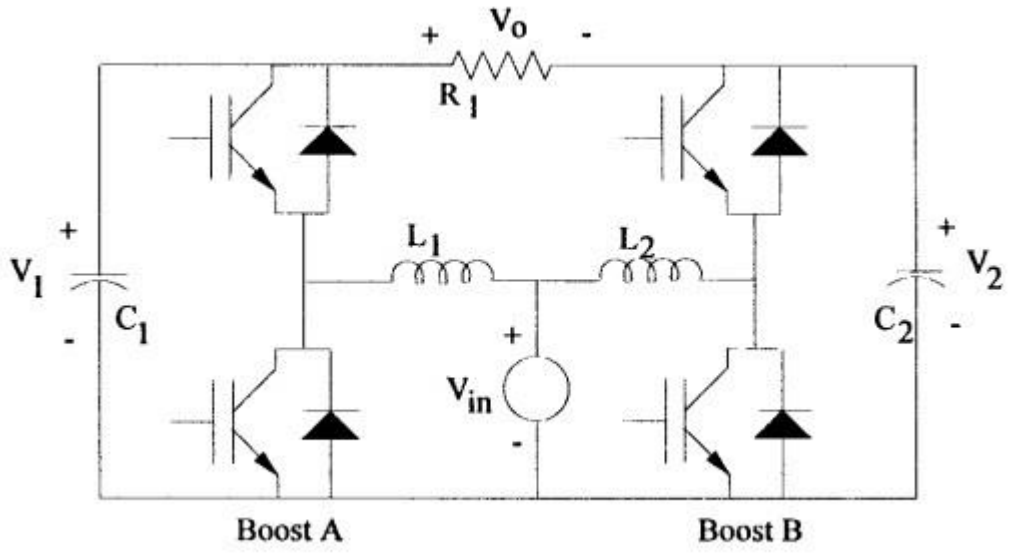


Figure 3.47: DC-AC boost inverter (Caceres & Barbi, 1999)

3.23 Summary

This chapter lays down the background of power converters in PV systems. Firstly, the types of DC-DC converters are explained, with particular emphasis on the transformerless type of converters. The challenges of using transformerless converters are also summarised. Then, the theory for various single-phase transformerless H-Bridge inverters, together with its corresponding performance was described. The problems associated with transformerless inverters are examined by observing the behaviour of common-mode voltage of each inverter topology. The context of using transformerless multilevel inverter is then briefly introduced. Finally, the chapter is ended with an explanation about module integrated converters (MIC).

CHAPTER 4

Proposed Single-Phase Transformerless Voltage Source Inverter

4.1 Introduction

This chapter describes the operation of the several proposed configurations. They consists of split capacitor H-Bridge (SC-HB) inverter with balancing circuit, modified unipolar H-Bridge inverter with CD-Boost converter, bipolar H-Bridge inverter with CD-Boost converter, and modified unipolar H-Bridge inverter with modified boost converter. The power conversion from DC signal into AC and the freewheeling stage in terms of common-mode voltage and ground leakage current are also discussed.

In this chapter, the filter design that complies with the IEEE 519 standard and ground leakage current standard (VDE-0126-1-1-standard) is presented. The selection of filter value that complies with both standards has been chosen.

The controlling algorithms were for MPPT and balancing power transfer from DC power to AC power is explained.

4.2 Block Diagram of the Proposed Single-Phase Transformerless PV Grid-Connected System

The block diagram of the proposed single-phase transformerless PV grid-connected system is shown in Figure 4.1. In order to comply with the safety regulation and installation standards of PV grid-connected inverter system the PV panel frame is connected to the ground. The system is more efficient, less expensive and not bulky due to transformer is eliminated in the whole system. When the transformer is omitted, the common ground between the PV panel and grid is directly connected and the system does

not have any galvanic isolation to provide protection. Figure 4.1 shows the PV grid-connected system installation without the transformer components.

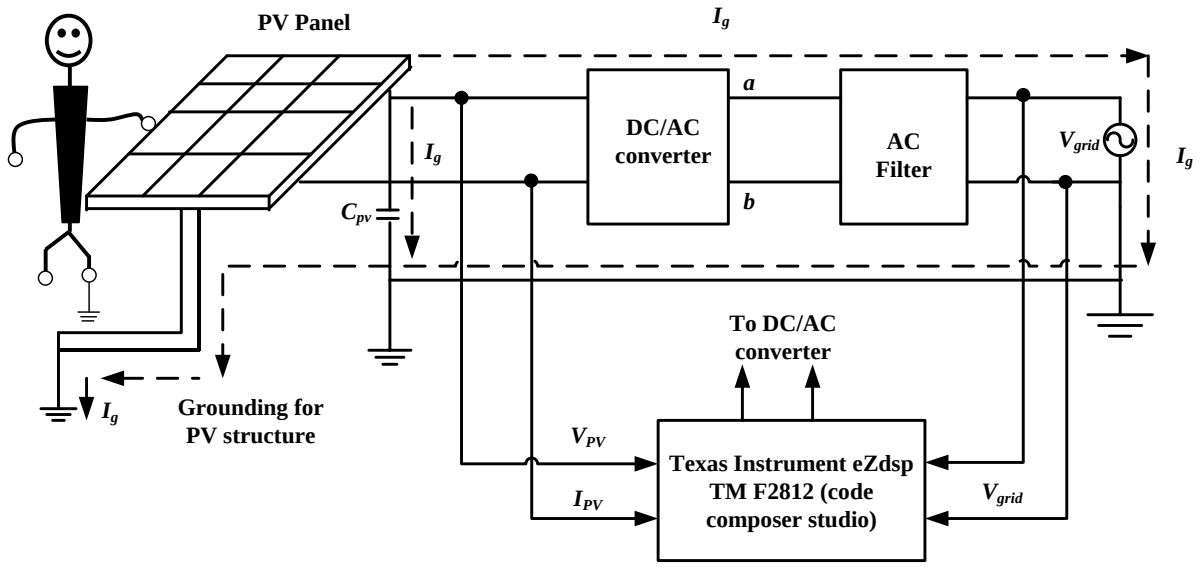


Figure 4.1: Block diagram of the proposed transformerless PV grid-connected system

Due to direct connection between the PV panel and the grid, the path of ground leakage current is flowing through the parasitic capacitance (C_{PV}) of PV panel as shown in Figure 4.1. Based on the VDE-0126-1-1 standard, the level of ground leakage current (I_g) should be well below the standard requirement of 300 mA, the threshold level that can cause ventricular fibrillation and involuntary muscle contractions (Eisner, 2002). The ground leakage current (I_g) through the parasitic capacitance can be analysed using the common-mode voltage (V_{cmm}) at the inverter output terminal point.

In Figure 4.1, the DC-AC converter is categories into two types (H-Bridge inverter without DC-DC converter and H-Bridge inverter with DC-DC converter). In this work, the H-Bridge inverter without DC-DC converter is defined as SC-HB inverter. On the other hand, the H-Bridge inverter with DC-DC converters are employed by modified unipolar H-Bridge inverter with CD-Boost converter, bipolar H-Bridge inverter with CD-Boost converter, and modified unipolar H-Bridge inverter with

modified boost converter. The conventional unipolar H-Bridge inverter without DC-DC converter and bipolar H-Bridge inverter without DC-DC converter are presented.

4.3 Conventional Transformerless H-Bridge Inverter

The conventional transformerless unipolar H-Bridge inverter configuration is shown in Figure 4.2. Typically, to indicate three level inverter voltages, the unipolar SPWM is implemented in the single-phase H-Bridge configuration. For signal generation in the configuration, two voltage references (V_{ref} & V_{ref2}) and one triangle carrier signal (V_c) are used. V_{ref2} is the negative value of V_{ref} (V_{ref} = - V_{ref2}).

When positive voltage reference (V_{ref}) is compared with the triangular carrier voltage (V_c), S_1 and S_2 are switched alternately. While S_3 and S_4 are switches alternately when negative voltage reference (V_{ref2}) is compared with V_c. The operation mode of half-positive cycle, inverter output voltage and common-mode voltage of this inverter is tabulated in Table 4.1.

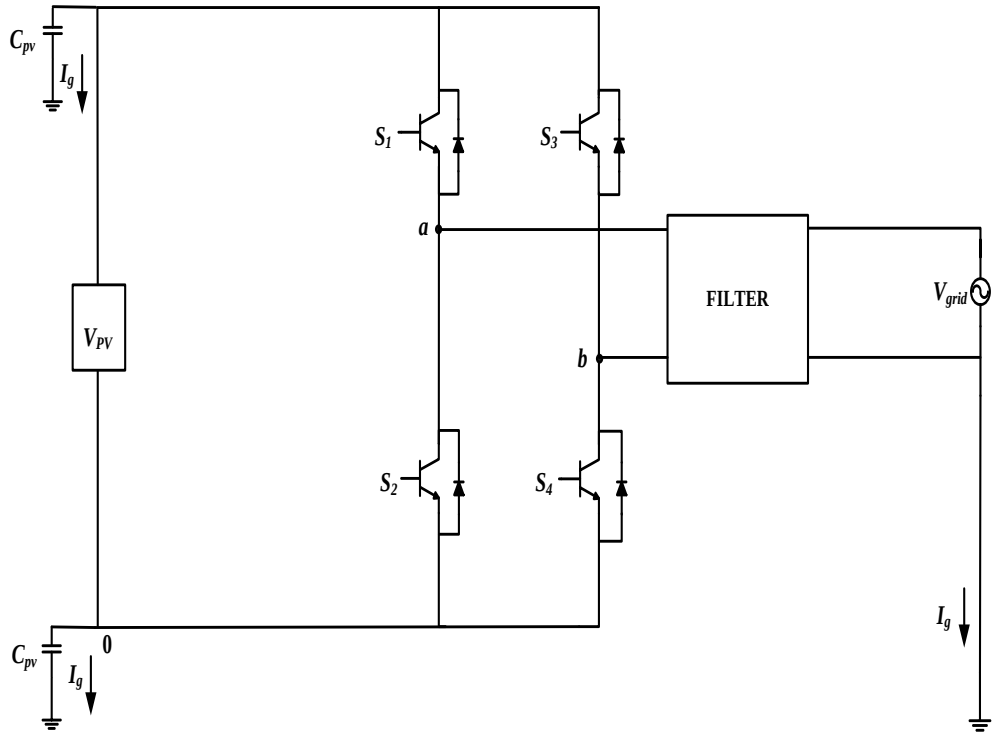


Figure 4.2: Conventional transformerless unipolar H-Bridge inverter

Table 4.1: Half-positive cycle operation mode of conventional unipolar H-Bridge topology

State	S_1	S_2	S_3	S_4	V_{ab}	V_{cmm}
I	ON	OFF	OFF	ON	V_{pv}	$V_{pv}/2$
II	ON	OFF	ON	OFF	0	V_{pv}
III	OFF	ON	OFF	ON	0	0

At state I, during the half-positive cycle, (S_1 and S_4 switches are ON), the power is transferred to the load as shown in Figure 4.3. The state II and state III in half-positive cycle are achieved by short-circuiting the output of the inverter as shown in Figures 4.4 and 4.5 respectively.

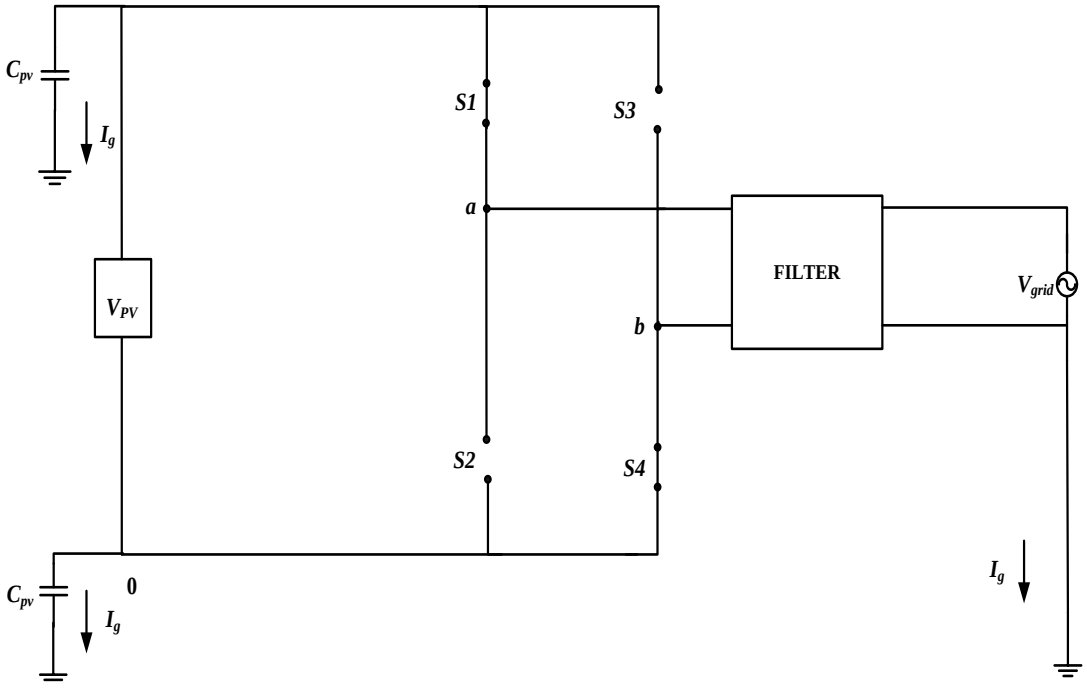


Figure 4.3: Half-positive cycle state for H-Bridge circuit (state I)

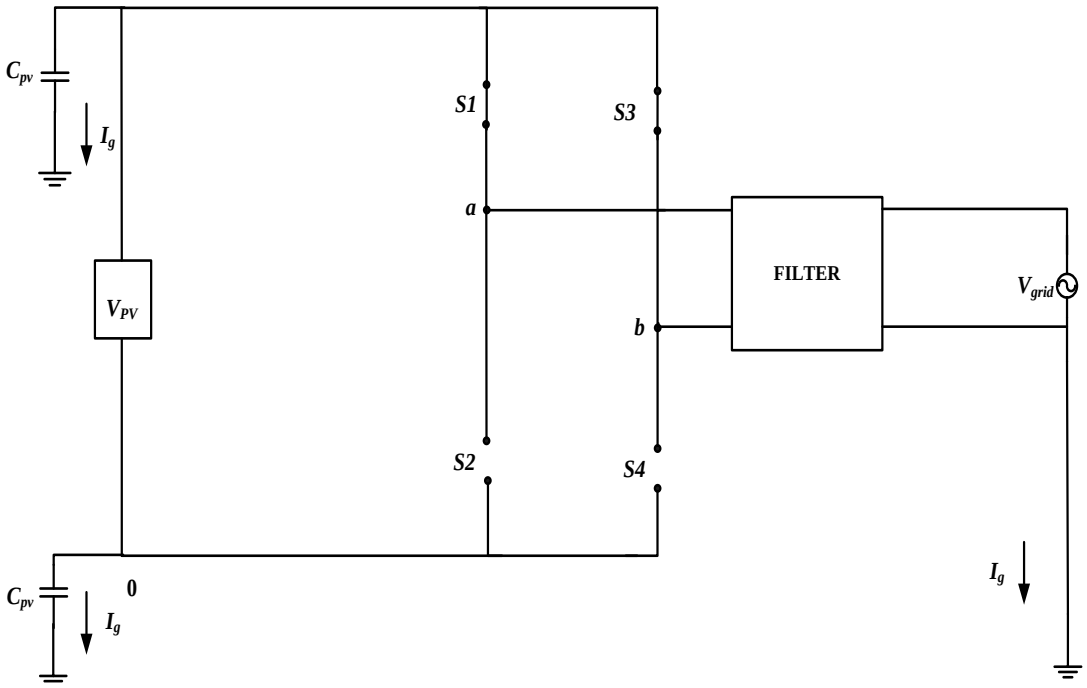


Figure 4.4: Zero state for half-positive cycle (state II)

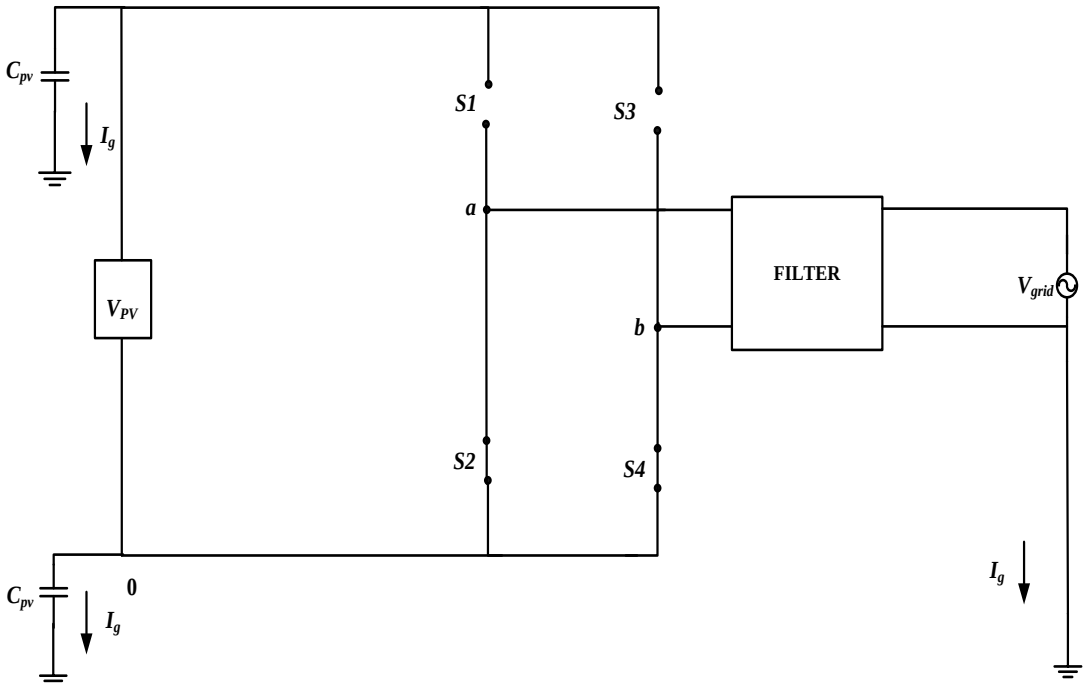


Figure 4.5: Zero state for half-positive cycle (state III)

The common-mode voltage (V_{cmm}) can be measured at points *a* and *b*, which is defined in equation (3.22). The detailed of common-mode voltage in all commutation states can be state in equations (4.1), (4.2) and (4.3).

State I : $V_{ao} = V_{pv}$ and $V_{bo} = 0$; $V_{cmm} = \frac{V_{pv}}{2}$ (4.1)

State II: $V_{ao} = V_{pv}/2$ and $V_{bo} = V_{pv}/2$; $V_{cmm} = V_{pv}/2$ (4.2)

State III : $V_{ao} = 0$ and $V_{bo} = 0$; $V_{cmm} = 0$ (4.3)

From equations (4.1), (4.2) and (4.3), the common-mode voltage fluctuates between V_{pv} / 2 V and 0 V and it not constant. This fluctuation voltage is unsafe for a transformerless PV grid-connected application system because it can generate high amounts of ground leakage current, causing potential harm to equipment and operating personnel.

When bipolar SPWM technique is applied in the conventional H-Bridge inverter circuit as shown in Figure 4.2, the behaviour of common-mode voltage is also analysed. Bipolar SPWM technique has two states, which is positive cycle (applied to the ac load using S1&S4) and negative cycle (applied to the ac load using S_2 & S_3) only. The dead time is not applied in the bipolar technique because the pair of switches (S_1 & S_4 and S_2 & S_3) are commutated at different H-Bridge legs (leg *a* and leg *b*) and the issue of dc link short circuit is ignored. In addition, the zero voltage state does not exist in this technique and fluctuation of common-mode voltage is not generated. The operation mode circuit of two states is shown in Figures 4.6 and 4.7 respectively.

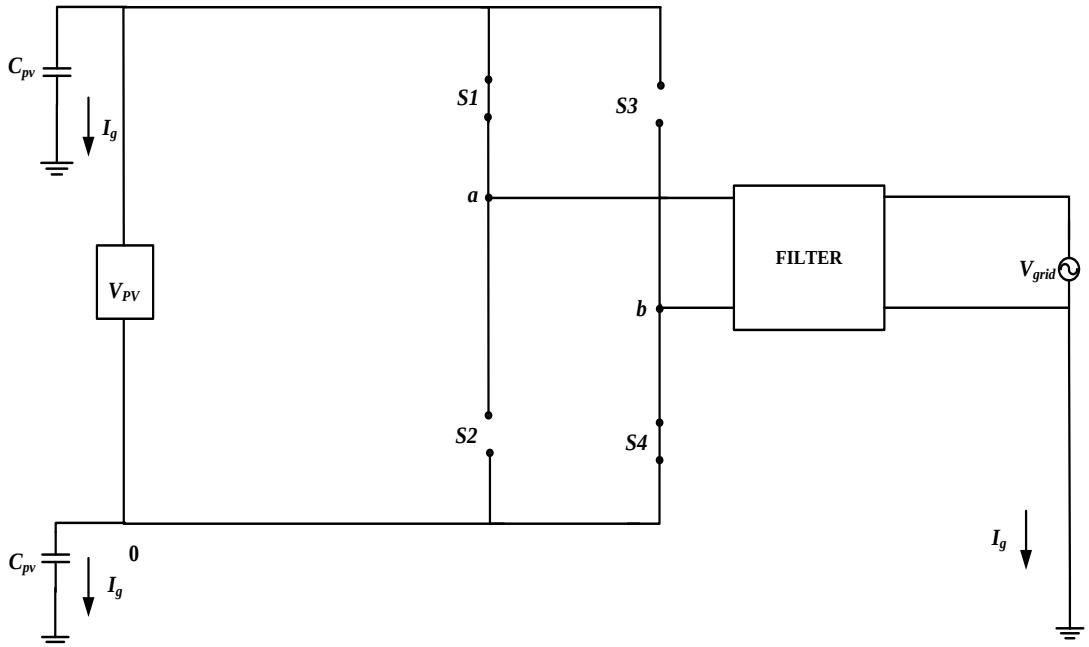


Figure 4.6: Positive cycle state for bipolar H-Bridge inverter circuit (state I)

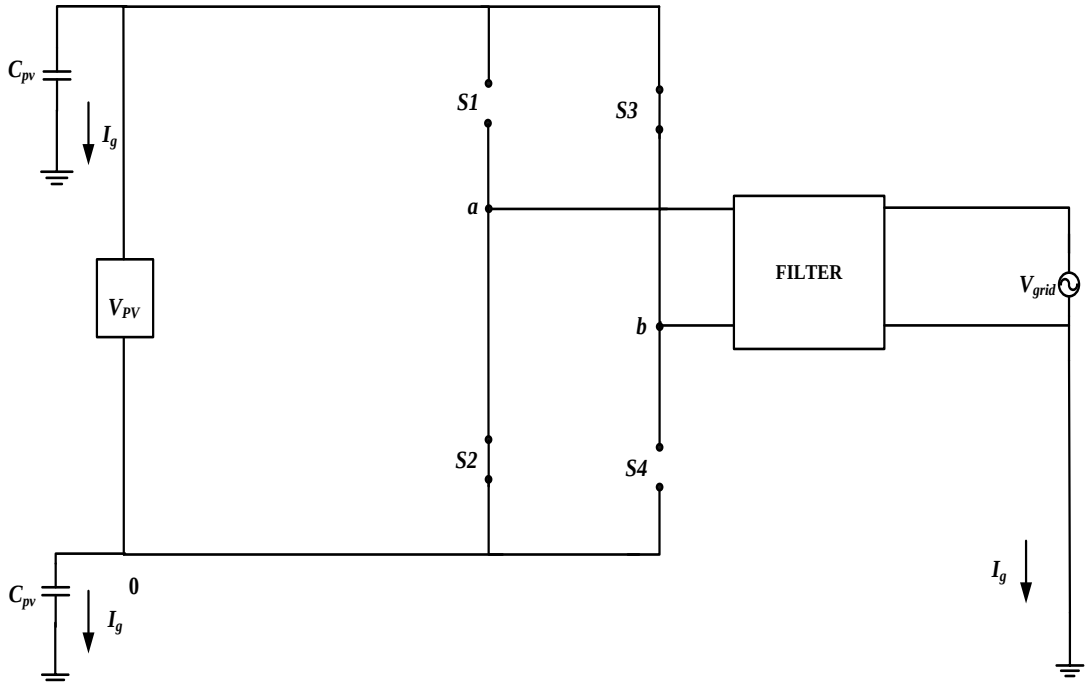


Figure 4.7: Negative cycle state for bipolar H-Bridge inverter circuit (state II)

The detailed of common-mode voltage in all commutation states can be state in equations (4.4) and (4.5).

$$\text{State I}: \quad V_{ao} = V_{pv} \text{ and } V_{bo} = 0;\ V_{cmm} = \frac{V_{pv}}{2} \tag{4.4}$$

$$\text{State II}: \quad V_{ao} = 0 \text{ and } V_{bo} = V_{pv};\ V_{cmm} = \frac{V_{pv}}{2} \tag{4.5}$$

From equations (4.4) and (4.5), the common-mode voltage does not fluctuate and is always constant at V_{pv} / *2*.

4.4 Filter Design

The configuration of LCL filter with split inductor has been used in the several proposed inverter topologies as shown in Figure 4.8. The configuration of inductor is split equally between the line *(L_{f1})* and neutral *(L_{f1n})* branches to deal with the common-mode voltage of transformerless power inverter (Tamas Kerekes, 2009).

The calculation of total filter inductance (L) is given in equation (4.6). The maximum ripple current ($\Delta_{ILripple,\max}$) was chosen to be 5%-20% of the rated current (Wang, et al., 2003).

$$L = \frac{1V_{dc}}{8\Delta_{ILripple,\max} f_s} \tag{4.6}$$

Filter capacitance (C_f) is determined by the reactive power absorbed in the filter capacitor is expressed in equation (4.7), with α being the reactive power factor. Its value was selected to be less than 5% (Wang, et al., 2003). P_{rated} is the rated power of the inverter and V_{rated} is its rated voltage.

$$C_f = \frac{\alpha P_{rated}}{2\pi f_{line} V_{rated}^{\ 2}} \tag{4.7}$$

By adding a capacitance C_f between the inverter side and grid side, the total inductance (L) are separated into two parts: L_{f1} and L_{f2}. The relationship of L_{f1} and L_{f2}

for LCL filter at inverter and grid side is defined by equation (4.8), where a ($a \geq 1$) is the inductance index of L_{f1} and L_{f2}. The inductance index can be calculated and defined using switching harmonic current attenuation ratio between inverter and grid inductors (Liserre et al.,2001; Channegowda & John, 2010). For stability reasons, L_{f2} must be designed with a lower value than L_{f1} (Fei et al., 2009; Channegowda & John, 2010).The resonant frequency (ω_{res}) for the LCL filter is defined in equation (4.9) (Fei et al., 2009). To avoid resonance effect and ensure carrier attenuation, the filter resonance frequency (f_{res}) should be lower than the switching frequency (f_{sw}) as described in equation (4.10).

$$L_{f1} = aL_{f2} \tag{4.8}$$

$$\omega_{res} = \sqrt{\frac{L_{f1} + L_{f2}}{L_{f1} L_{f2} C_f}} \tag{4.9}$$

$$f_{res} < f_{sw} \tag{4.10}$$

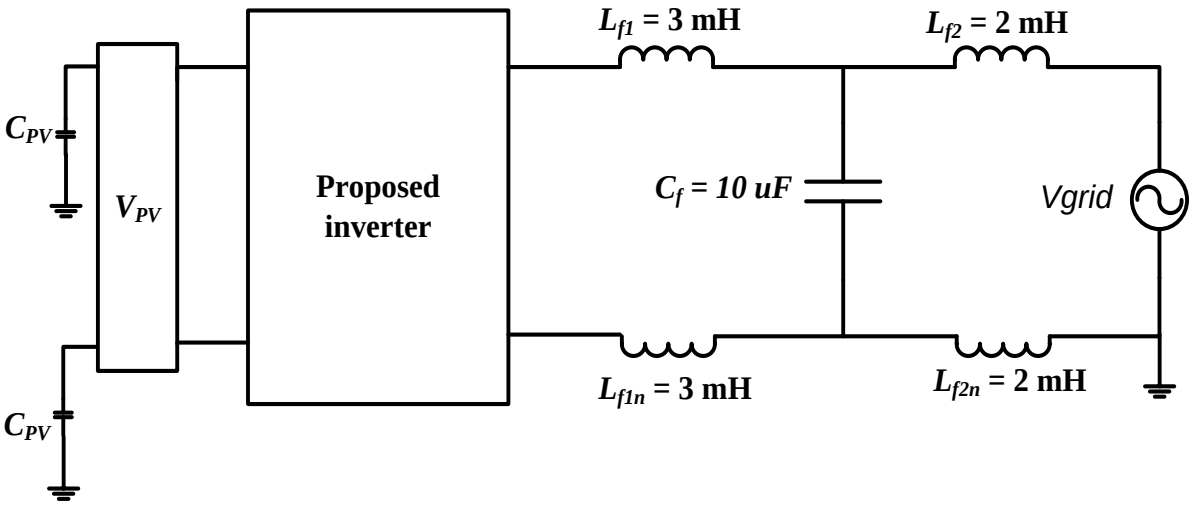


Figure 4.8: LCL configuration for the proposed transformerless PV system

4.5 Configuration of Proposed Split Capacitor H-Bridge (SC-HB) Inverter with Balancing Circuit

Figure 4.9 shows the configuration of an (SC-HB) inverter with balancing circuit. The configuration comprised a balancing circuit, single-phase H-Bridge inverter and split LCL filter. The high value of V_{pv} voltage (400 V) is applied in this topology to ensure maximum power transfer. In this topology, the function of the balancing circuit is to balance the series dc-link capacitors (V_{CB1} & V_{CB2}). However, the balancing circuit does not affect the reduction of common-mode voltage.

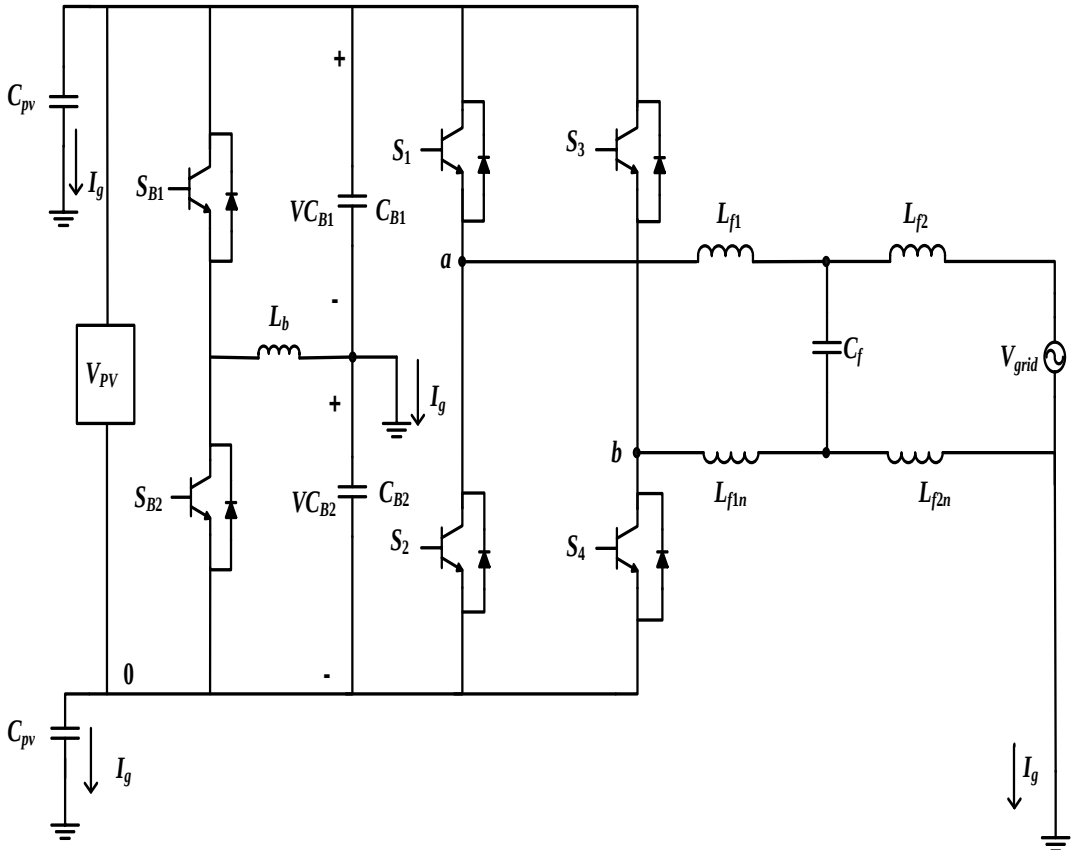


Figure 4.9: SC-HB transformerless inverter topology

4.5.1 The Balancing Strategy in SC-HB Inverter

In the proposed single-phase transformerless inverter topology, the ground leakage current (I_g) through PV parasitic capacitance (C_{PV}) can be reduced by connecting the midpoint of the two series dc-link capacitors (C_{B1} & C_{B2}) to the neutral point of grid. However, series-connected capacitors may have non-uniform voltage distribution. The capacitor-voltage balancing problem in the dc inverters link can be significantly reduced if the energy drawn from the series string of the dc-link capacitors can be controlled. This control is possible using a simple balancing circuit. The simple balancing circuit for controlling the dc-link capacitor voltage (Jouanne., 2002) applied in the proposed transformerless single-phase inverter topology is as shown in Figure 4.10(a). It has switches S_{B1} & S_{B2} and one inductor L_b connected to the series dc-link capacitors. S_{B1} & S_{B2} are important components to ensure voltage across DC link (V_{pv}) is divided equally. As a result, the voltage across C_{B1} (VC_{B1}) is approximately equal to the voltage across C_{B2} (VC_{B2}).The voltage variation against the capacitor voltage is given by:

$$\Delta V = VC_{B1} - VC_{B2} \tag{4.11}$$

where V_{CB1} and V_{CB2} are the voltage across the upper and the lower capacitor respectively. Variation in the capacitor voltage (ΔV) can be reduced by this circuit.

A simple control method is proposed for the balancing circuit, which is derived from buck and boost DC-DC converter topologies. When V_{CB1} is higher than V_{CB2}, i.e., $\Delta V > 0$, S_{B1} starts operating within a specific ON-state duty cycle to maintain the dc-link voltage balances (see Figure 4.10(b)). Energy is transferred from the upper capacitor C_{B1} to the lower capacitor C_{B2} through the inductor L_b when the S_{B1} is on. When the S_{B1} is switched off, the energy stored in L_b is released into the C_{B2} through the free-wheeling

diode D_{SB2}. On the contrary, if $\Delta V < 0$ (when V_{CB2} is larger than V_{CB1}), the S_{B2} reverses the energy transfer from the C_{B2} to the C_{B1}; see Figure 4.8(c). The energy is stored in the L_b when the S_{B2} is on. When the S_{B2} is off, the energy in the L_b is transmitted into the C_{B1} through the D_{SB1}.

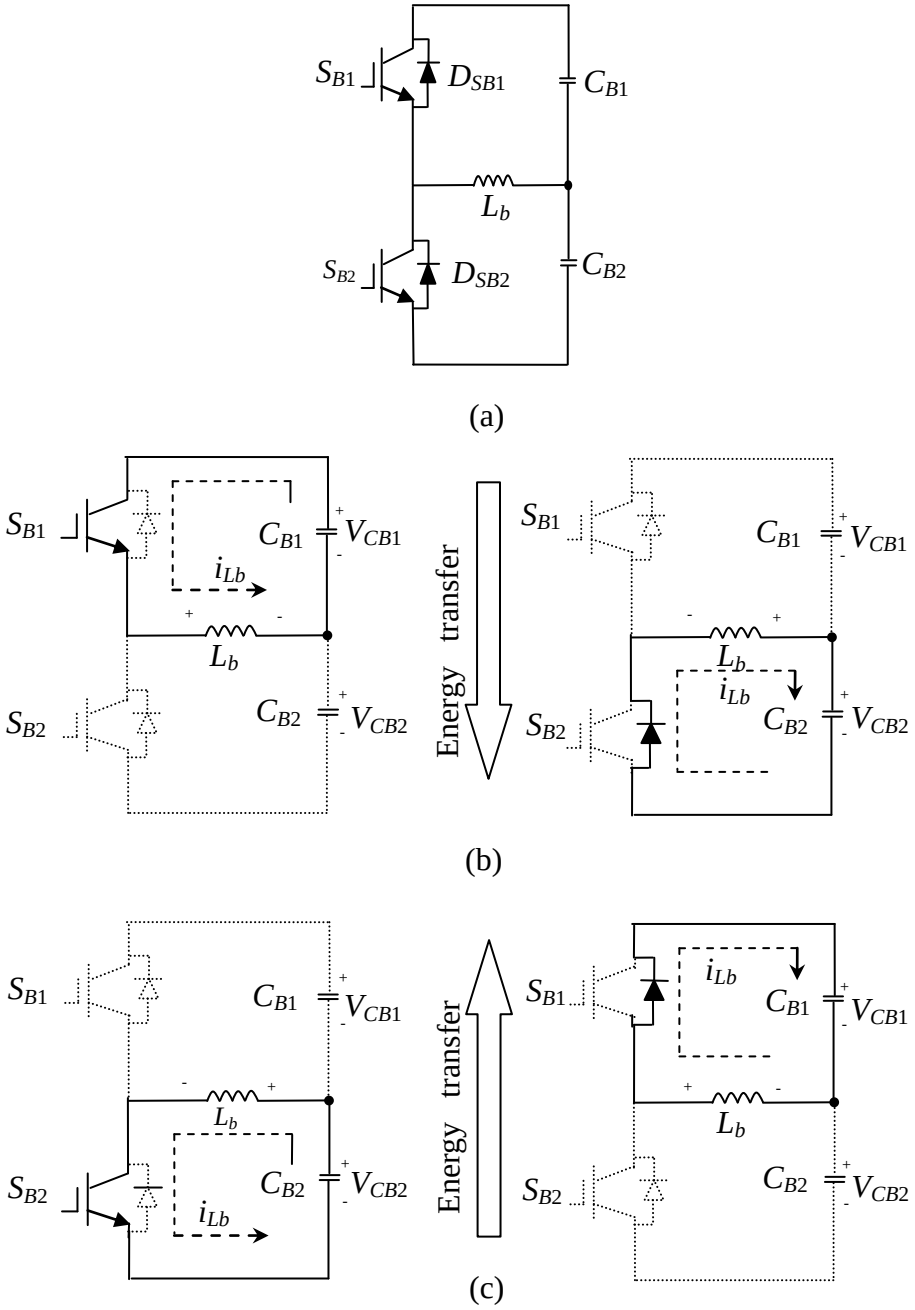


Figure 4.10: (a) The balancing circuit, (b) energy transfer from C_{B1} to C_{B2}, (c) energy transfer from C_{B2} to C_{B1}

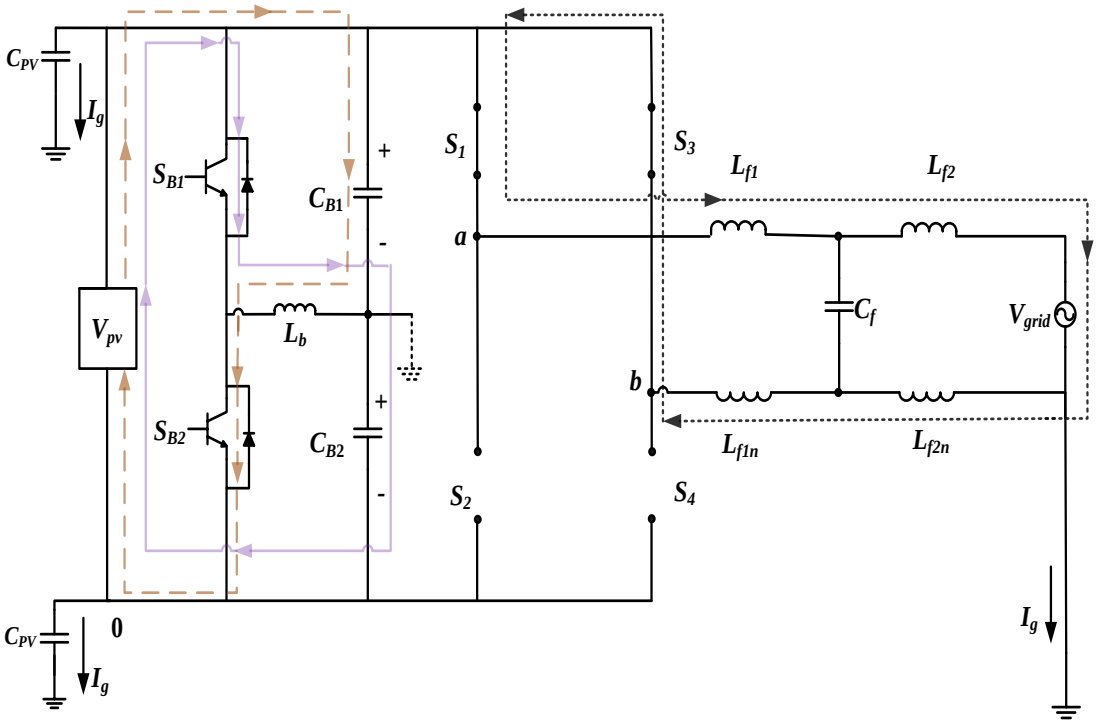
4.5.2 Ground Leakage Current Reduction in Proposed SC-HB Inverter Topology

Due to the advantages offered by the unipolar SPWM switching technique in improving the quality of injected inverter current; this switching technique is used in the proposed SC-HB topology. There are four states involved in unipolar SPWM switching technique, i.e. Zero Positive state (state I), Positive Active state (state II), Zero Negative state (state III) and Negative Active state (state IV). In the following explanations, operation of the first two states will be discussed. The other two states will not be explained as state I operation mode is similar to state III and the results of state IV is the same as state II. The only difference is in the polarity of the inverter outputvoltage (V_{ab}). The summary of common-mode voltage (V_{cmm}) during all commutation in the proposed topology is illustrated in Table 4.2.

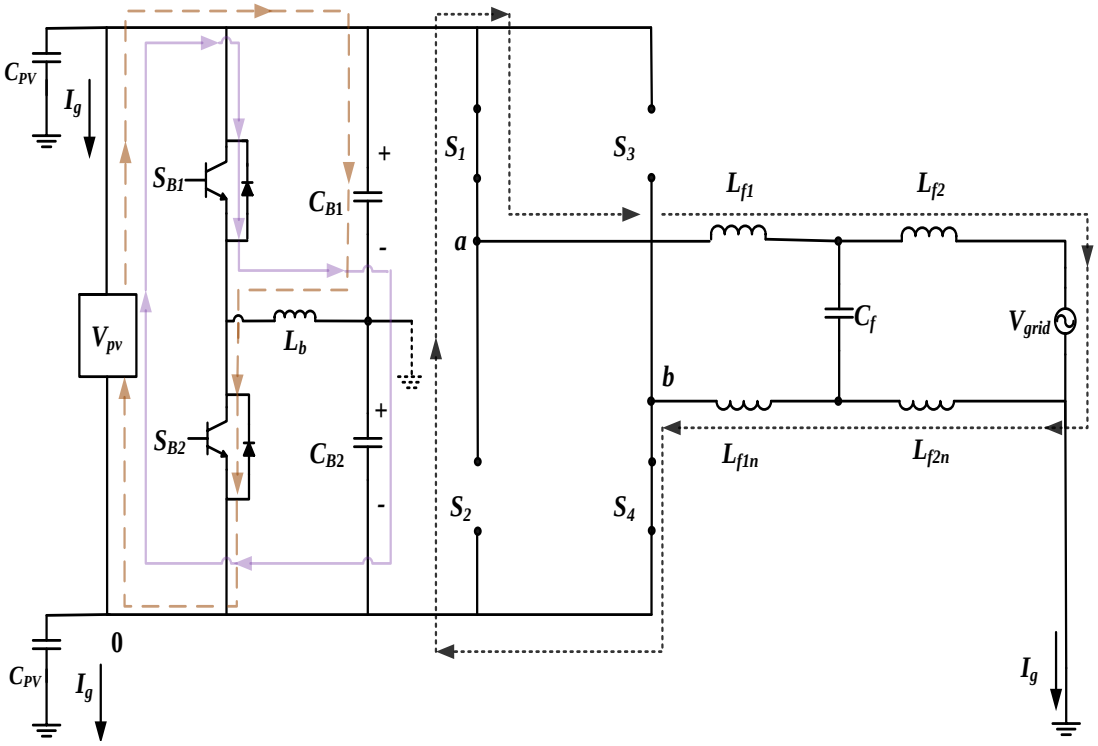
State I is applied by turning ON S_1 and S_3 as shown by the dotted lines of Figure 4.11(a). Meanwhile, state II is applied by turning ON S_1 and S_4 as shown by the dotted lines of Figure 4.11(b). In both figures, the balancing strategy operations are also highlighted. Solid lines represent the operation of the balancing circuit when $S_{B1}$is ON. Meanwhile dashed lines represent the balancing operation when S_{B2} is ON.

Table 4.2: Operation mode of SC-HB topology

State	Vector State	S_1	S_2	S_3	S_4
I	zero positive	ON	OFF	ON	OFF
II	positive	ON	OFF	OFF	ON
III	zero negative	OFF	ON	OFF	ON
IV	negative	OFF	ON	ON	OFF



(a)



(b)

Figure 4.11: Mode operation of SC-HB topology, (a) zero positive state, (b) positive active

Table 4.3 shows the common-mode voltage of SC-HB inverter during all switching states. From this table, the value of common-mode voltage (V_{cmm}) is maintained at $V_{PV}/2$ for all four states. This is due to the common ground connection of the series dc-link capacitor and PV frame. The implementation of the four states gives three levels of output voltage (V_{ab}), $+V$, 0 and $-V$ as tabulated in Table 4.3.

Table 4.3: Four states of SC-HB inverter

State	V_{cmm}	V_{ab}
I	$V_{PV}/2$	0
II	$V_{PV}/2$	V_{dc}
III	$V_{PV}/2$	0
IV	$V_{PV}/2$	$-V_{dc}$

4.6 Proposed Bipolar H-Bridge Inverter with CD-Boost Converter

Figure 4.12 shows the proposed system that has CD-Boost stage, single-phase bipolar H-Bridge inverter stage, and grid LCL filter configuration. The CD-Boost converter produce high gain conversion voltage ratio. Due to advantage of bipolar SPWM technique in term of constant common-mode voltage, which it produce low ground leakage current (has been explained in previous section 4.3), therefore that technique is applied into proposed H-Bridge inverter topology. In the proposed topology, the negative terminal "0" of the solar module is set as the reference point. The middle point of the bridge legs are set as "*a*" and "*b*" of the output inverter terminal. The calculation and selection components value of proposed topology is presented in the following section. The operation mode of CD-Boost converter is explained in detail.

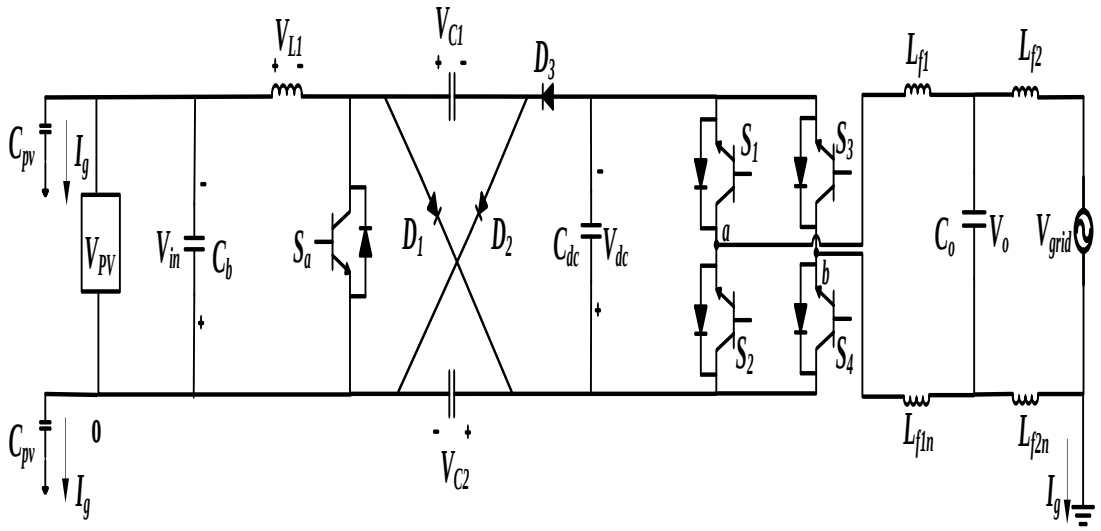


Figure 4.12: The proposed bipolar H-Bridge inverter with CD-Boost converter for grid-connected PV system

4.6.1 Power Decoupling Calculation

The input and output powers are in different forms (dc and ac respectively), so a decoupling capacitor is required to store and balance the instantaneous energy between them. The decoupling capacitor connects the input side of the DC-DC converter to the input side of the H-Bridge inverter, as shown in Figure 4.12. The sizes of capacitors C_b and C_{dc} are calculated using equation (4.12) below:

$$C_b, C_{dc} = \frac{P_{PV}}{2\omega_{grid} V_c \Delta u_c} \tag{4.12}$$

where P_{pv} is the rated power of the PV module, ω_{grid} the grid frequency (rad/s), V_c the rated capacitor voltage, and Δu_c the ripple voltage of the capacitor. A large capacitance is used to achieve a low dc-voltage ripple and a high MPPT efficiency. For example, with PV module ratings of P_{pv}= 200 W, V_{in} = 60 V and assuming a capacitor voltage with low ripple is chosen, Δu_c = 2.4 V, the required boost filter capacitance C_b will be approximately 2200 *uF*. In the second stage and with the same PV module, for V_{dc}= 350

V and Δu_c = 3 V (assuming low ripple capacitor voltage), the required capacitance C_{dc} is about 270 *uF*.

4.6.2 Cuk-Derived Boost (CD-Boost) converter

The CD-Boost converter is a combination of an inverting switched-capacitor (SC) cell and a classical Cuk converter as shown in Figure 4.13. Figure 4.14 shows the CD-Boost converter's continuous inductor current mode operation. Figure 4.14(a) shows that when S_a is turned ON, D_1 and D_2 become reverse biased while D_3 becomes forward biased, so the two capacitors discharge in series. When the switch is turned ON, the inductor voltage and current can respectively be expressed as equation (4.13) and (4.14). When $C_1 = C_2$, the voltage across the capacitors C_1 and C_2 (V_{C1} and V_{C2}) is half the output CD-Boost converter voltage (V_{dc}). This is shown in equation (4.15) below:

$$V_{L1} = V_{in} = \frac{L\Delta_{iL1(on)}}{DT} \tag{4.13}$$

$$\Delta_{iL1(on)} = \frac{V_{in}DT}{L} \tag{4.14}$$

$$V_{C1} = V_{C2} = V_C = \frac{V_{dc}}{2} \tag{4.15}$$

When S_a is turned OFF as in Figure 4.14(b), D_1 and D_2 become forward biased and the two C_1 and C_2 capacitors charge in parallel. The voltage across the inductor (V_{L1}) and the rate of change of the inductor current (Δ_{iL1}) can be obtained from Equations (4.16) and (4.17).

$$V_{L1} = V_{in} - V_c = L\frac{\Delta_{iL1(Off)}}{(1-D)T} \tag{4.16}$$

$$\Delta_{iL1(off)} = \left(\frac{V_{in} - V_c}{L} \right) (1 - D) T \tag{4.17}$$

As the rate of change of the inductor current is zero in steady-state operation, substituting equations (4.16) and (4.17) into equation (4.18) yields the capacitor voltage V_c, as shown in equation (4.19).

$$\Delta_{iL(on)} + \Delta_{iL(off)} = 0 \tag{4.18}$$

$$V_c = \frac{V_{in}}{1 - D} \tag{4.19}$$

From equations (4.15) and (4.18), the voltage conversion ratio *(M)* of the CD-Boost in steady-state analysis of the inductor is

$$\frac{V_{dc}}{V_{in}} = \frac{2}{1 - D} = M \tag{4.20}$$

where V_{in} is the DC input CD-Boost converter voltage, V_{dc} is the output CD-Boost converter voltage, and D is the duty cycle. From equation (4.20), the voltage conversion gain of the CD-Boost converter is twice that of a conventional boost converter. Therefore, the output voltage is a step higher than a conventional boost converter.

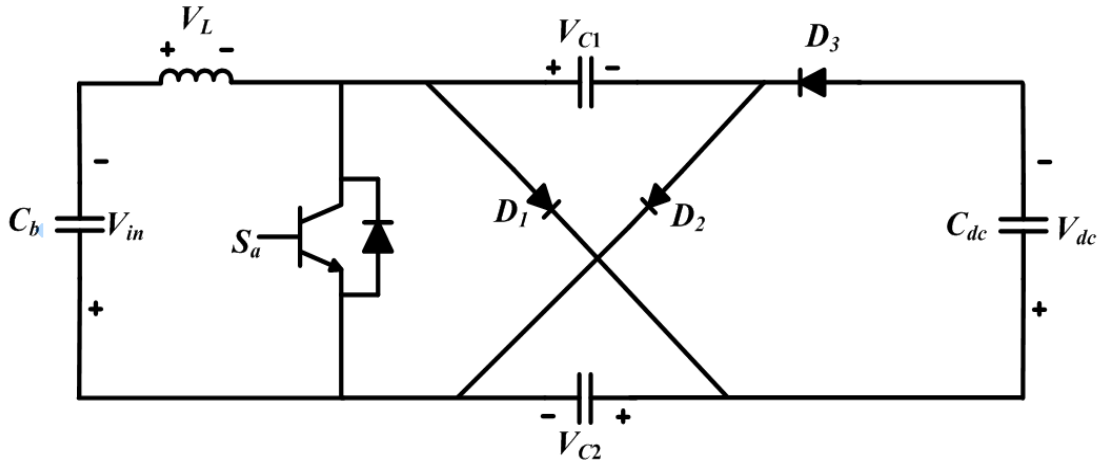
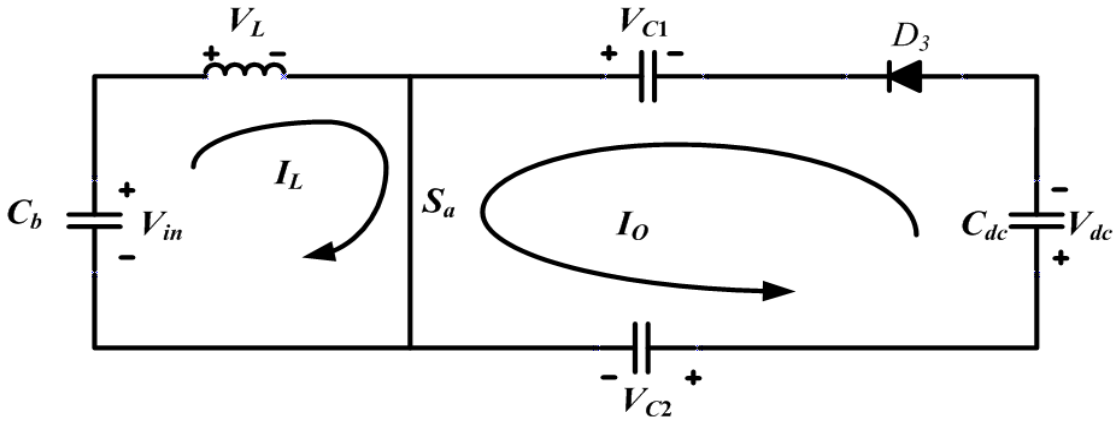
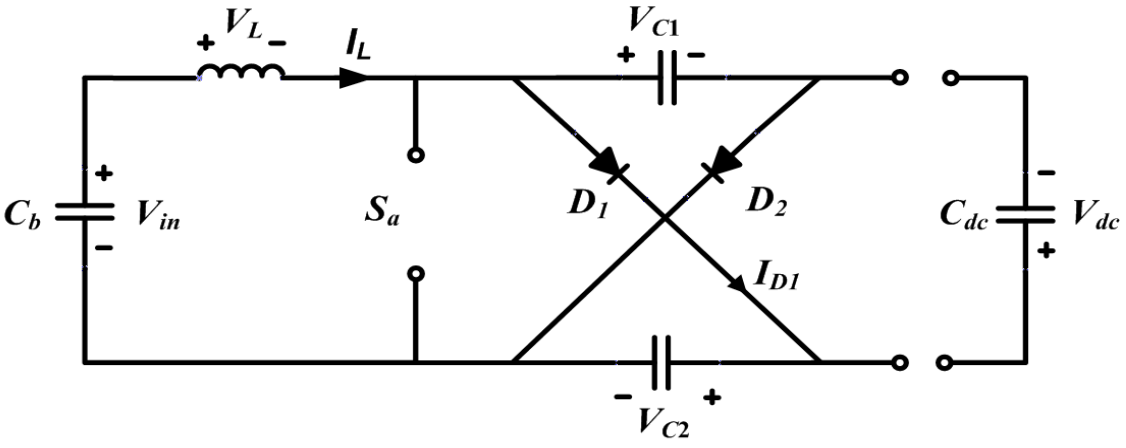


Figure 4.13: The CD- Boost converter circuit



(a)



(b)

Figure 4.14: Operation modes of the CD-Boost converter
(a) switch-on mode, (b) switch-off mode

4.6.3 Proposed Modified Unipolar H-Bridge Inverter with CD-Boost Converter

Figure 4.15 shows the proposed DC-AC topology that consists of a high gain DC-DC boost converter known as Cuk Derived Boost (CD-Boost) (Ismail et al., 2008), an H-Bridge inverter and an LCL filter. The CD-Boost converter combines the inverting switched capacitor (SC) cell and the classical Cuk converter. The proposed topology has two additional switches (S_b and S_c) at line and neutral branches of the dc-link terminal to disconnect the PV panel and grid during the zero vector state.

The proposed topology system has the combination advantage of a three level output inverter voltage (-V_{dc}, 0 and V_{dc}) with constant common-mode voltage and very low ground leakage current (< 300mA). With very low ground leakage current, the proposed topology is suitable for non-isolated PV grid-connected system and is safe for people maintaining, operating or standing near the system.

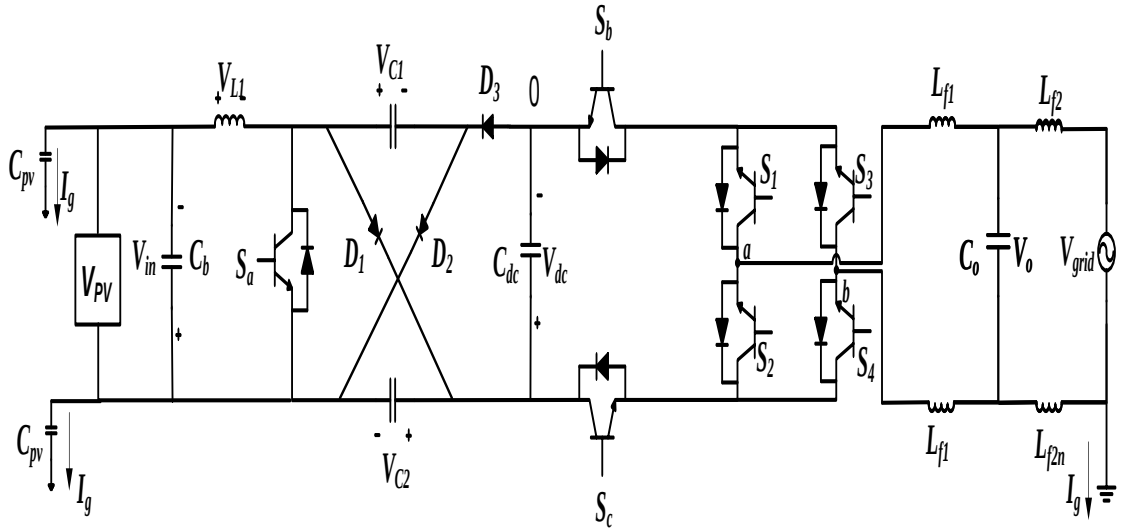


Figure 4.15: Modified unipolar H-Bridge inverter with CD-Boost converter

4.6.3.1 Switching Strategy of Modified Unipolar H-Bridge Inverter with CD-Boost Converter

The S_b and S_c switches are additional device components that functions when the H-Bridge inverter operates in active vector state and zero vector state. The S_a is alternately switched with S_b and S_c to charge and discharge the output capacitor (C_{dc}) of CD-Boost converter. The three-level output single-phase inverter voltage and constant common-mode voltage is produced based on the switch combination given in Table 4.4.

Table 4.4: Switching combination of proposed inverter (for positive grid voltage)

Mode/state / Switch	Mode 1 / active vector state	Mode 2 / zero vector state
S_a	OFF	ON
S_b	ON	OFF
S_c	ON	OFF
S_1	OFF	OFF
S_2	ON	ON
S_3	ON	OFF
S_4	OFF	ON

4.6.3.2 Mode of Operation for Modified Unipolar H-Bridge Inverter with CD-Boost Converter

In the active vector state, the switch S_a is turned OFF, while the switches S_b and S_c are turned ON as shown in Figure 4.16, D_1 and D_2 are forward-biased and the two capacitors, C_1 and C_2 are charged in parallel. Initially, the voltage across the dc-link capacitor (V_{dc}) is defined in (4.20).

During mode 1, the dc-link voltage (V_{dc}) is transferred to grid through S_c, S_2, S_3 and S_b. Since V_{ao} is V_{dc} and V_{bo} is 0 V in this state, the common-mode voltage is half of the dc-link voltage as expressed in (4.21).

$$V_{ao} = V_{dc},\ V_{bo} = 0 \tag{4.20}$$

$$V_{cmm} = \frac{V_{ao} + V_{bo}}{2} = \frac{V_{dc}}{2} \tag{4.21}$$

The mode operation during the zero vector state of the proposed system is shown in Figure 4.17, S_a is turned ON while S_b and S_c are turned OFF, D_1 and D_2 are reversed biased while D_3 is forward biased so that the two capacitors are discharged in series and the inductor current charging is increased. During this state, the current and voltage of the inductor can be expressed as equations (4.14) and (4.15) respectively. In this state, the dc-link capacitor (C_{dc}) is charged through L_1, S_a, C_2, D_3 and C_1. It is noted that the voltage across the dc-link capacitors (V_{dc}) is twice of the capacitors voltage (V_{C1} and V_{C2}) as given by equation (4.15). During the zero vector state, the H-Bridge inverter is separated from the PV panel due to the additional switches (S_b and S_c) being switched off. The zero vectors are applied to the load through by S_2, S_4 and filter inductors (L_{f1} and L_{f2}). The common-mode voltage in this state is expressed in equation (4.22).

$$V_{cmm} = \frac{V_{ao} + V_{bo}}{2} = \frac{V_{dc}}{2} \tag{4.22}$$

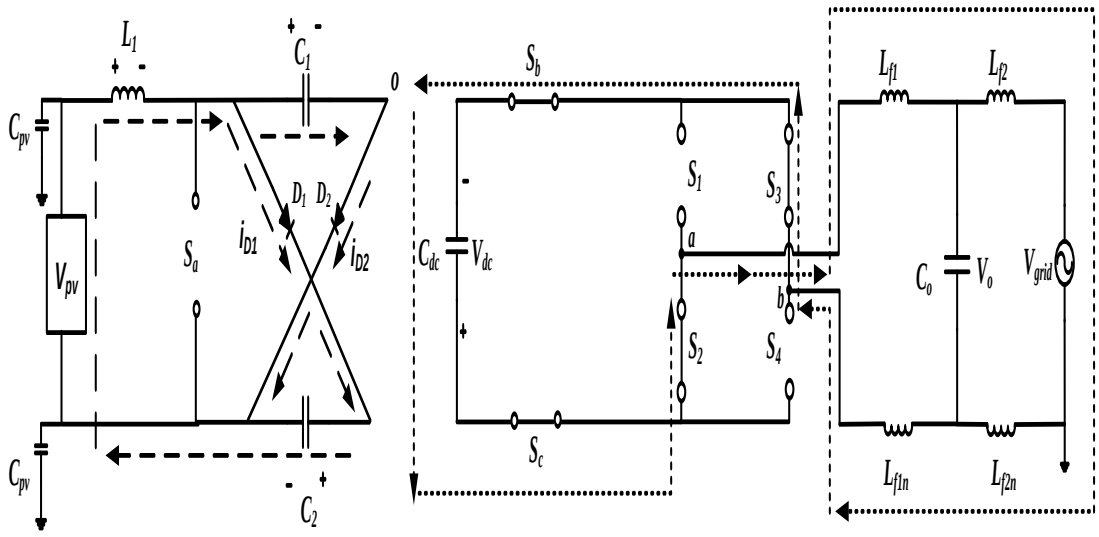


Figure 4.16: Active vector state applied to grid (mode 1)

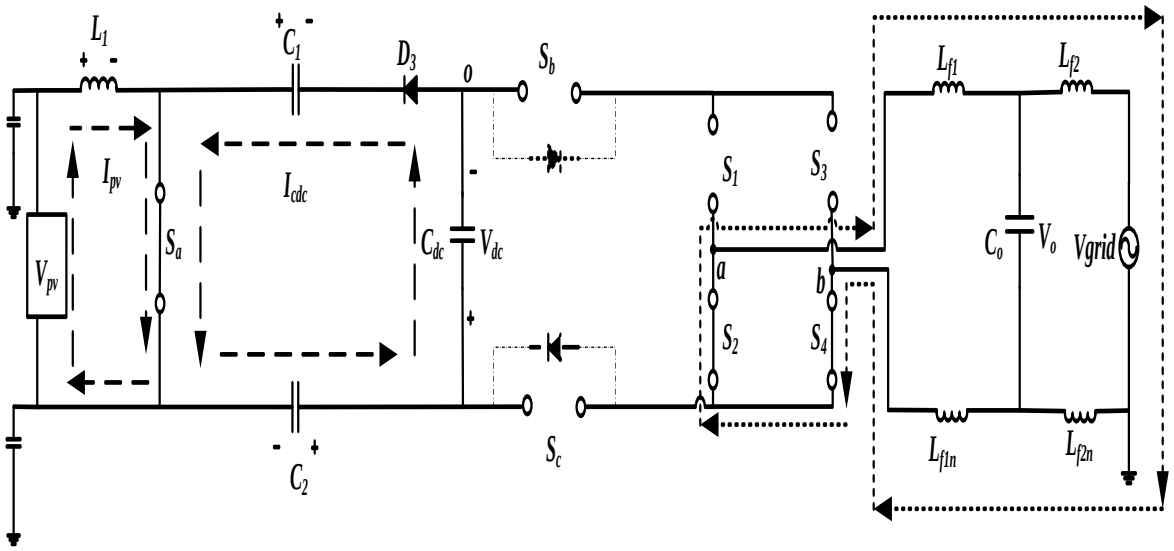
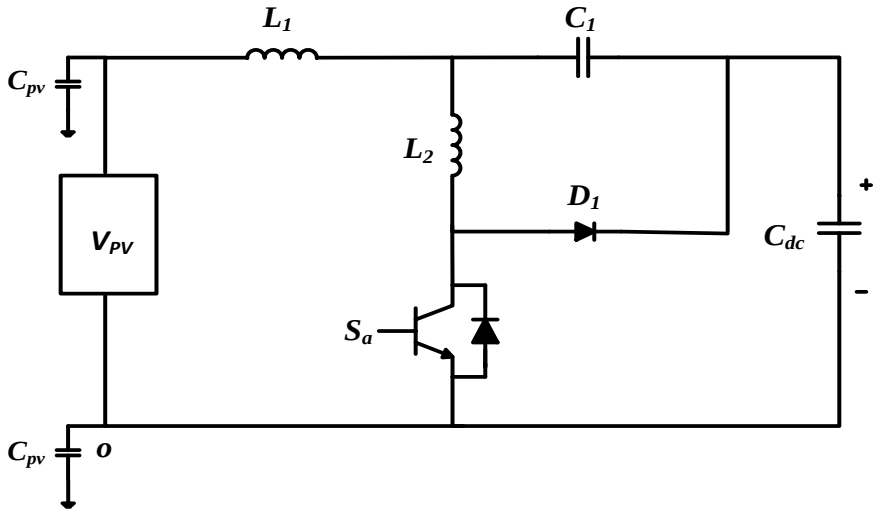


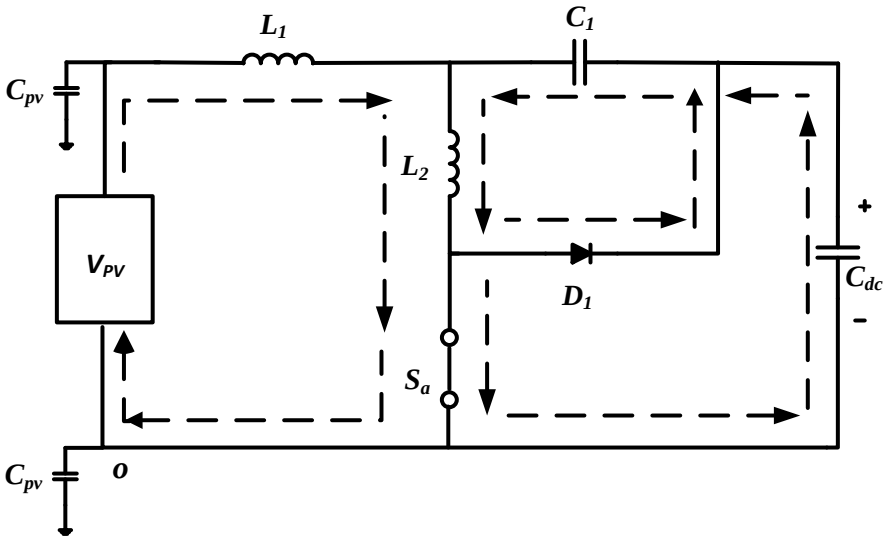
Figure 4.17: Zero vector state applied to grid (mode 2)

4.7 Proposed Modified Boost Converter with Low Input Current Ripple

Figure 4.18(a) shows the circuit configuration of proposed modified boost converter with low input ripple current. The steady-state operation of the converter is discussed for both switch-on and switch-off conditions as shown in Figure 4.18(b) and Figure 4.18(c) respectively. The proposed converter generates ripple-free input current in continuous inductor current mode (CICM) condition.



(a)



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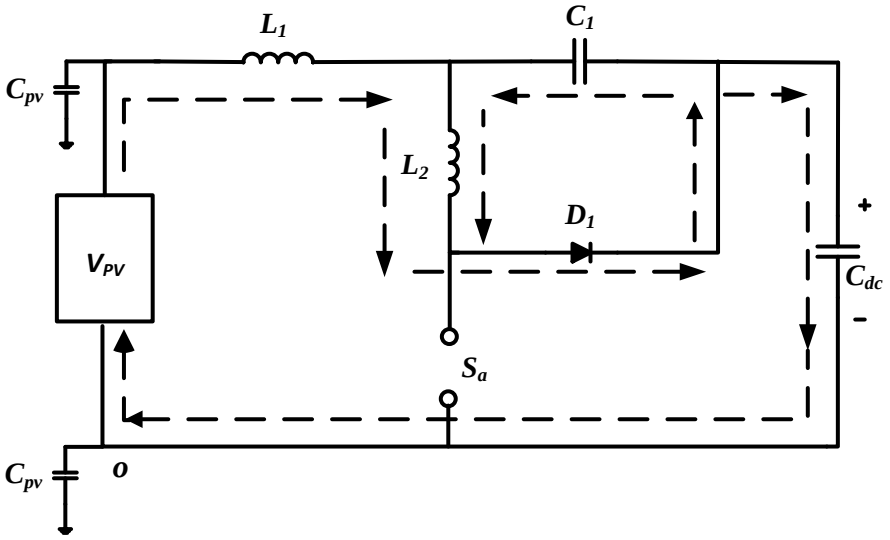


(c)

Figure 4.18: (a) Proposed modified boost converter circuit, (b) switch turn-on mode, (c) switch turn-off mode

When the switch is ON as shown in Figure 4.16(b), the input current is controlled by two series inductors (L_1 and L_2) across the source to keep the ripple low. During the ON state, the current of each inductor (L_1 and L_2) increases linearly. Equation (4.23) is derived from Kirchhoff's Voltage Law:

$$t_{on} = \frac{L_1 \Delta_{iL1} + L_2 \Delta_{iL2}}{V_{PV}} \tag{4.23}$$

When the switch is OFF, capacitor C_{dc} starts charging, and the currents of inductors L_1 and L_2 decrease linearly (see Figure 4.18 (c); equation (4.24) describes this.

$$t_{off} = \frac{L_1\Delta_{iL1} + L_2\Delta_{iL2}}{VC_{dc} - V_{PV}} \tag{4.24}$$

For the switching period (T), equation (4.25) defines the closed switch period whereas Equation (4.26) defines the open switch period.

$$t_{on} = DT \tag{4.25}$$

$$t_{off} = (1-D)T \tag{4.26}$$

By substituting (4.25) and (4.26) respectively into (4.23) and (4.24) during steady state operation, the net change in inductor current over one period is zero. The capacitor voltage (VC_{dc}) is as expressed in equation (4.27).

$$V_{cdc} = \frac{V_{PV}}{1-D} \tag{4.27}$$

The switching period (T_s) can be extracted from equation (4.25) and (4.26):

$$T_s = \frac{1}{f_s} = t_{on} + t_{off} = \frac{L_1\Delta_{iL1} + L_2\Delta_{iL2}}{V_{PV}} + \frac{-L_1\Delta_{iL1} - L_2\Delta_{iL2}}{V_{PV} - VC_{dc}} \tag{4.28}$$

During $t_{on,}$ period, the inductor current in L_2 increases linearly. The voltages of capacitors C_1 and C_{dc} are thus as defined by Equations (4.29) and (4.30).

$$VC_{dc} - VC_1 = \frac{L_2\Delta_{iL2}}{t_{on}} \tag{4.29}$$

$$t_{on} = \frac{L_2\Delta_{iL2}}{VC_{dc} - VC_1} \tag{4.30}$$

Equation (4.31) shows the current of inductor L_2 decreasing linearly during the period t_{off}.

$$t_{off} = \frac{L_2 \Delta_{iL2}}{VC_1} \tag{4.31}$$

The current of inductor L_2 operates during steady state. Equation (4.32) defines the capacitor voltage (VC_{dc}).

$$VC_{dc} = \frac{VC_1}{D} \tag{4.32}$$

From equations (4.30) and (4.31), the switching period T_s of inductor L_2 is as defined in equation (4.33).

$$T_s = \frac{1}{f_s} = t_{on} + t_{off} = \frac{L_2 \Delta_{iL2}}{VC_{dc} - VC_1} + \frac{L_2 \Delta_{iL2}}{VC_1} \tag{4.33}$$

The input ripple current in inductor L_2 is then:

$$\Delta_{iL2} = \frac{VC_1 (VC_{dc} - VC_1)}{L_2 VC_{dc} f_s} \tag{4.34}$$

By substituting equation (4.34) into equation (4.28), the input ripple current of the proposed converter is thus as defined by equation (4.35).

$$\Delta_{iL1} = \frac{V_{PV} (VC_{dc} - V_{PV}) - VC_1 (VC_{dc} - VC_1)}{L_1 VC_{dc} f_s} \tag{4.35}$$

The input ripple current of the proposed converter can then be defined in terms of the charging capacitor and expressed by equation (4.36).

$$\Delta_{iL1} = \frac{VC_{dc} D(1-D) - VC_{dc} D(1-D)}{L_1 f_s} \tag{4.36}$$

From (4.36) the peak-to-peak (Δ_{iL1}) input ripple current of the proposed modified boost converter is zero.

4.8 Proposed Modified Unipolar H-Bridge Inverter with Modified Boost Converter

Figure 4.19 shows the circuit configuration of proposed modified unipolar H-Bridge inverter with modified boost converter. The modified boost converter is connected at dc stage to boost the input dc voltage from low power PV generator. The advantages of this configuration are eliminated input dc ripple current and minimize ground leakage current for transformerless PV grid-connected inverter system. Due to minimal input dc current, the efficiency of system is increased. In addition, the safety person hazard during conducting the proposed system is achieved due the low ground leakage current.

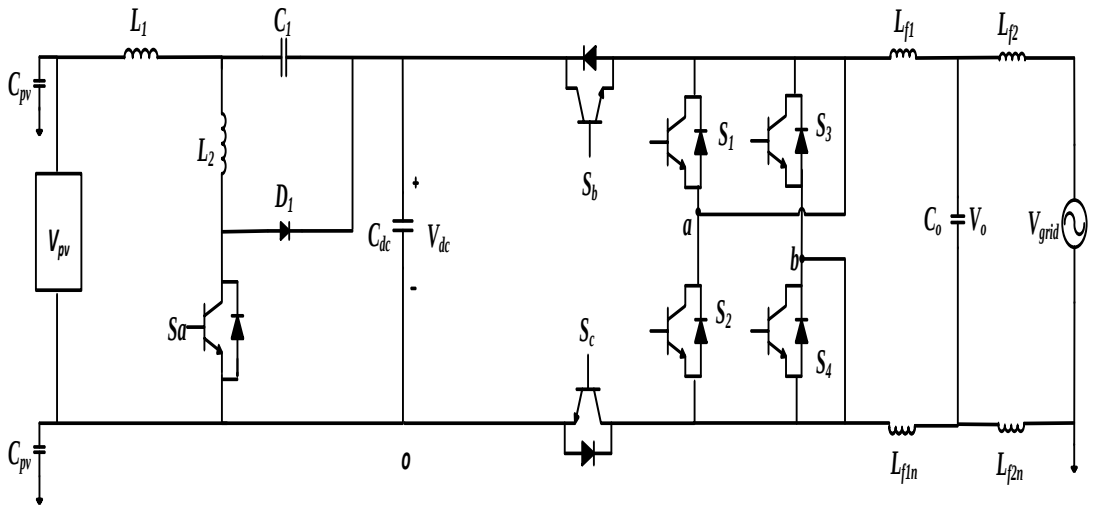


Figure 4.19: Modified unipolar H-Bridge inverter with modified boost converter circuit configuration

4.8.1 Mode Operation of Proposed Modified Unipolar H-Bridge Inverter with Modified Boost Converter

The active vector state mode operation of proposed converter is show in Figure 4.20. During this mode, the switch S_a is turned OFF while the additional switches S_b and

S_c are turned ON. The energy of PV is transfer to dc-link capacitor (C_{dc}) by controlling the switch (S_a) in modified boost converter The dc-link capacitor voltage is state in equation 4.37.

$$V_{dc} = \frac{V_{PV}}{1-D} \tag{4.37}$$

Where V_{PV} is photovoltaic voltage and D is duty cycle. During this state, the energy from dc-link voltage (V_{dc}) is transfered to the grid by sequences switching of additional switches (S_b & S_c) and H-Bridge inverter switches (S_1 & S_4). To improve injected current quality of the inverter, the modified unipolar switching technique is proposed in this circuit configuration.

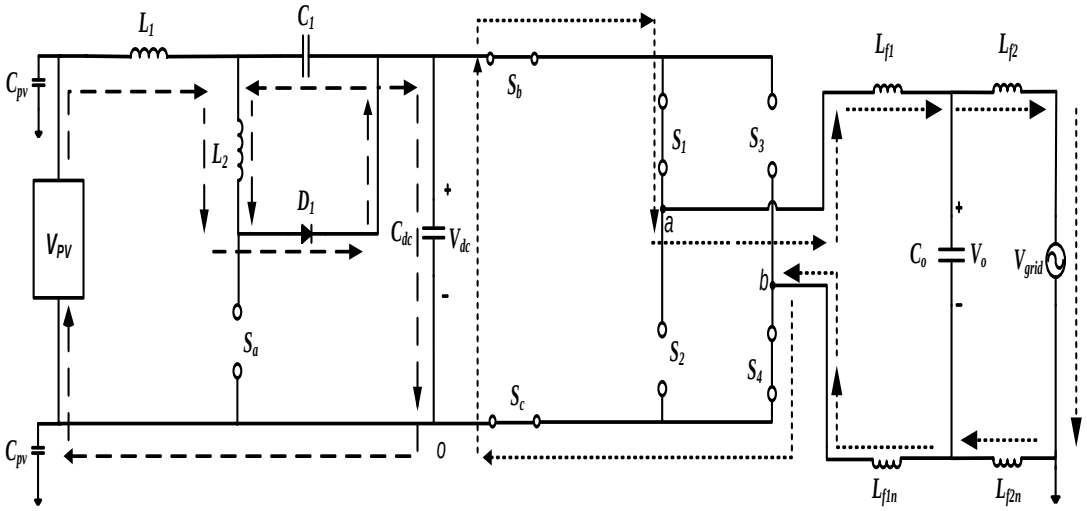


Figure 4.20: Active vector state mode, applied to grid for proposed unipolar H-Bridge inverter with modified boost converter

In order to minimize the ground leakage in the proposed circuit, the additional switches (S_b and S_c) are turned OFF to disconnect the PV generator and H-Bridge inverter. This disconnecting condition will isolated the whole system and produce low ground leakage current. The disconnection condition of the circuit is called zero vector state modes as shown in Figure 4.21. During this state the modified boost converter switch (S_a) is turn ON and the dc-link capacitor is charging until to desired voltage.

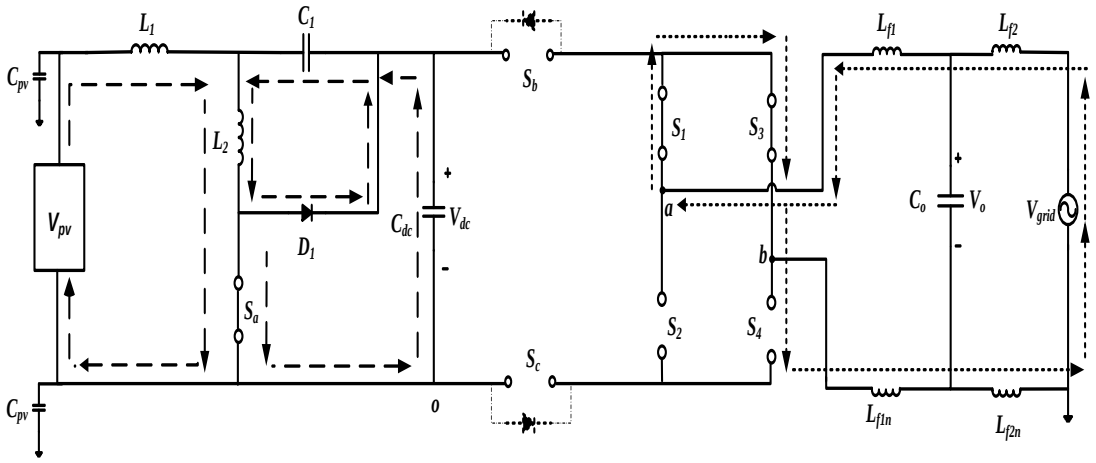


Figure 4.21: Zero vector state mode, applied to grid for proposed modified unipolar H-Bridge inverter with modified boost converter

4.9 Power Balancing Controller

To ensure the extraction of maximum power from the PV modules, the maximum power point tracking (MPPT) algorithm is incorporated into the proposed PV system. Several MPPT methods can be used to maximize output power P_{MPPT} and maintain that value at steady-state. The algorithm flow chart is shown in Figure 4.22. The control criteria that decreases, increases, or even maintains the MPPT power is based on the variation of the panel power with the voltage. Maximum power is extracted from the PV modules by adjusting the duty cycle of the boost converter. The amount of power transferred to the grid is controlled by adjusting the modulation index m_a of the inverter. Equation (4.38) expresses the relationship between the inverter output voltage V_{grid} and its inverter input voltage V_{dc}.

$$V_{grid} = m_a \times V_{dc} \tag{4.38}$$

4.10 Anti-islanding protection

The control algorithm of the passive islanding detection for single phase transformerless grid-connected inverter system is shown in Figure 4.23. The algorithm

is processed by collecting analogue input data from the under and over voltage (UV/OV) circuit. The analogue input data is sampled and compared with the normal voltage condition, which is 240 V. Meanwhile for frequency calculation, a simple zero crossing circuit has been fully utilized. The square wave produced by the zero cross detector is identical to the grid frequency (50 Hz).

4.11 Summary

This chapter discussed the operation principle of a proposed transformerless PV grid-connected inverter system. The operations of the conventional boost converter, conventional unipolar and bipolar SPWM H-Bridge inverter have been deliberated. To reduce the current inverter, the SC-HB inverter, the modified unipolar H-Bridge inverter with CD-Boost converter and the bipolar H-Bridge inverter with CD-Boost converter have been examined. The proposed inverter circuits (SC-HB inverter, bipolar H-Bridge inverter with CD-Boost converter, modified unipolar H-Bridge inverter with CD-Boost converter) produced constant common-mode voltage, which generated low ground leakage current. The low current satisfies the non-isolated PV grid-connected system (transformerless system) safety requirement. The proposed low input ripple of DC converter has also been presented in this chapter. In addition, the conventional high ripple input DC converter has been explained. The power balancing control of the proposed trasformerless PV grid-connected inverter has been presented. Finally, the standard anti islanding protection has been briefly explained.

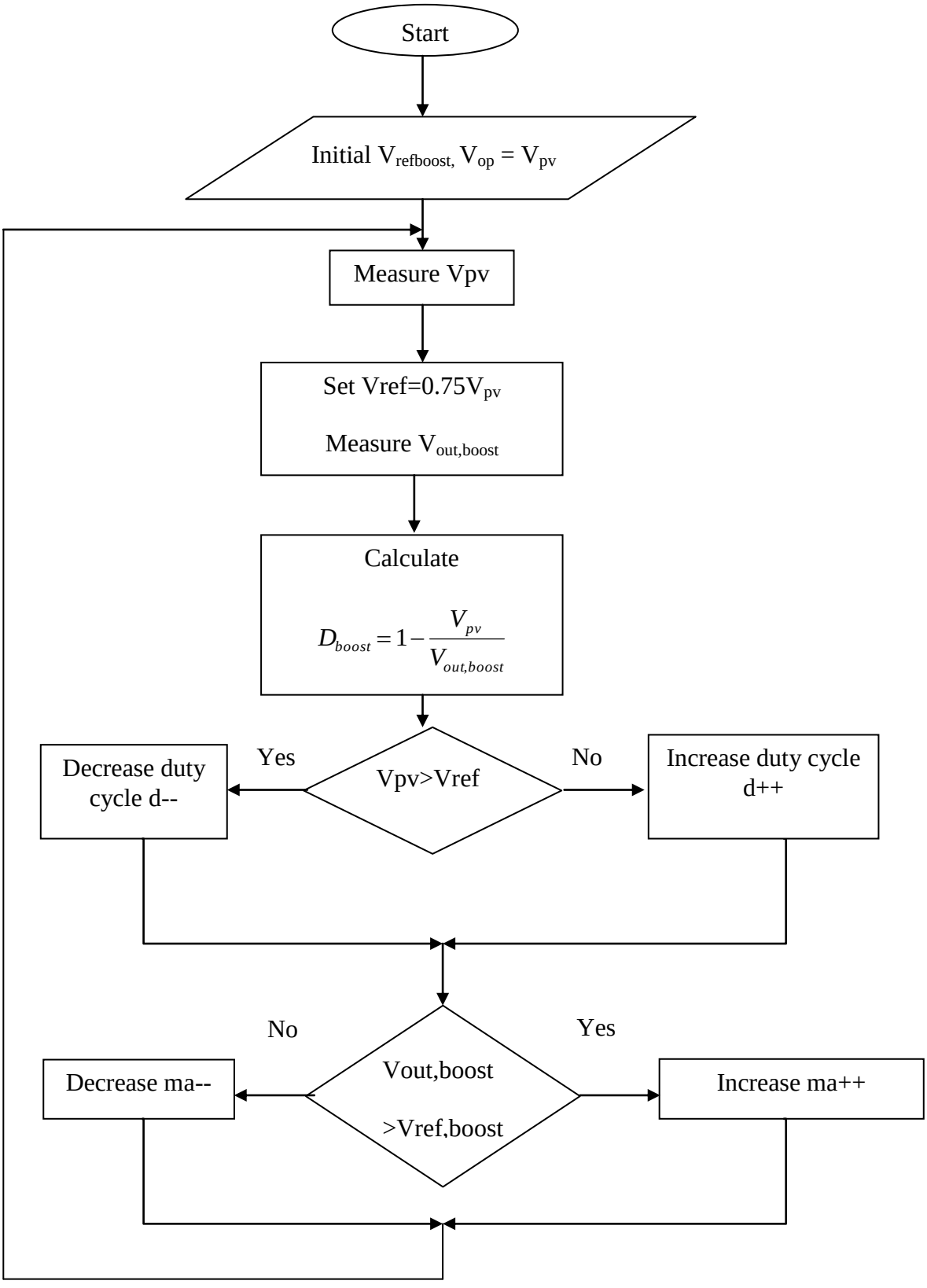


Figure 4.22: Flow chart of power balancing control

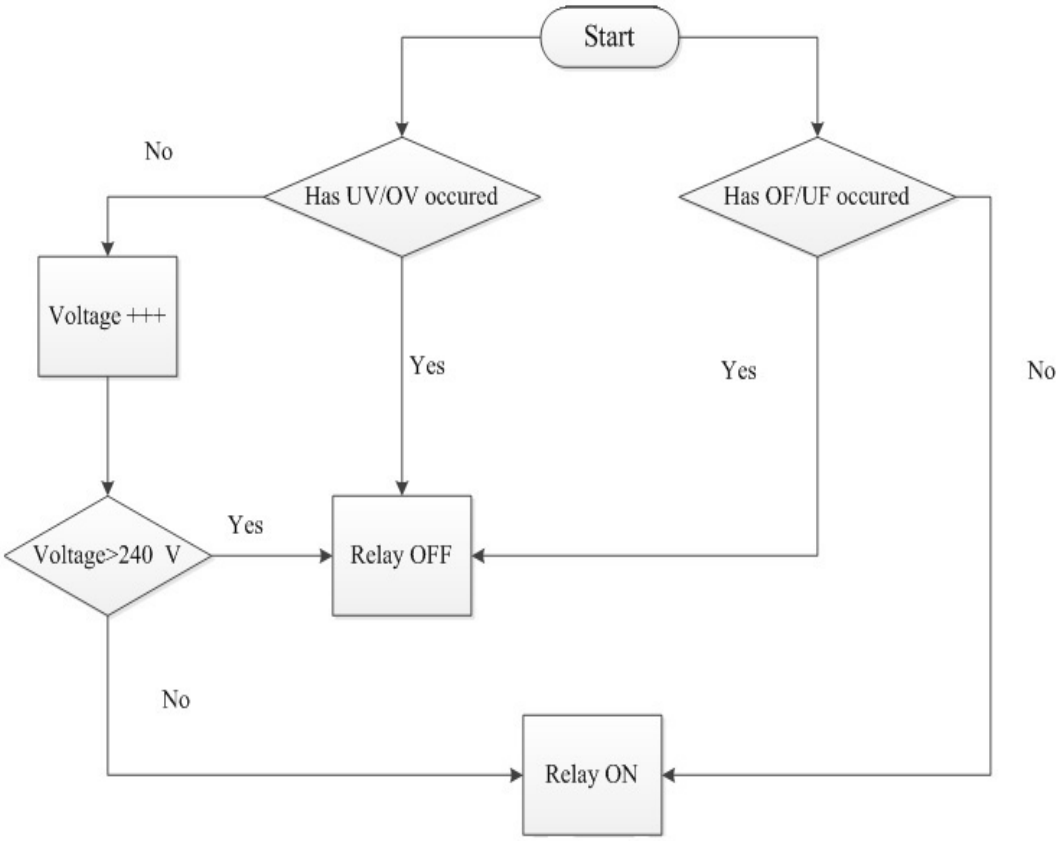


Figure 4.23: Flow chart of anti-islanding algorithm

CHAPTER 5

Simulation Results

5.1 Introduction

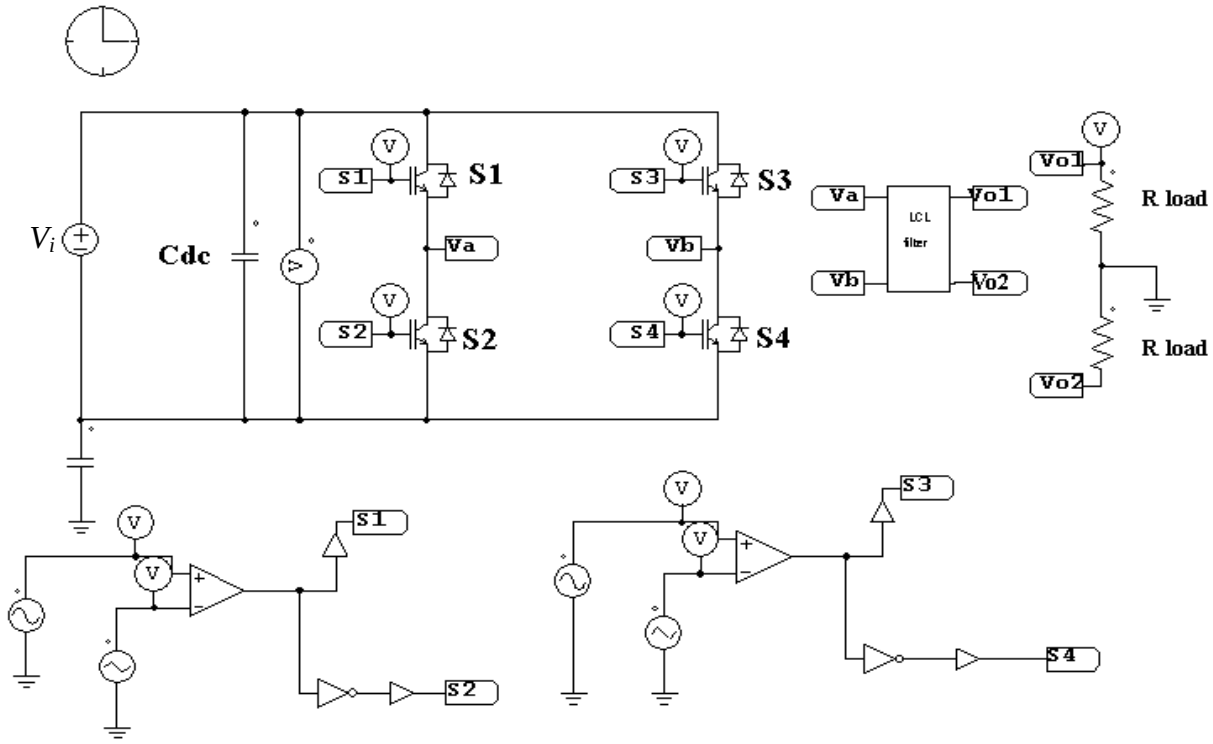
The proposed single-phase transformerless inverters have been developed through simulation using PowerSim (PSIM) software tool. The proposed inverter systems consists of SC-HB inverter, bipolar H-Bridge inverter with CD-Boost converter, modified unipolar H-Bridge inverter with CD-Boost converter and modified unipolar H-Bridge inverter with modified boost converter. In this chapter, the schematic diagrams of the proposed inverter systems have been presented. In addition, the simulation results in term of common-mode voltage and ground leakage current have been discussed.

5.2 Simulation of Single-Phase H-Bridge Inverter

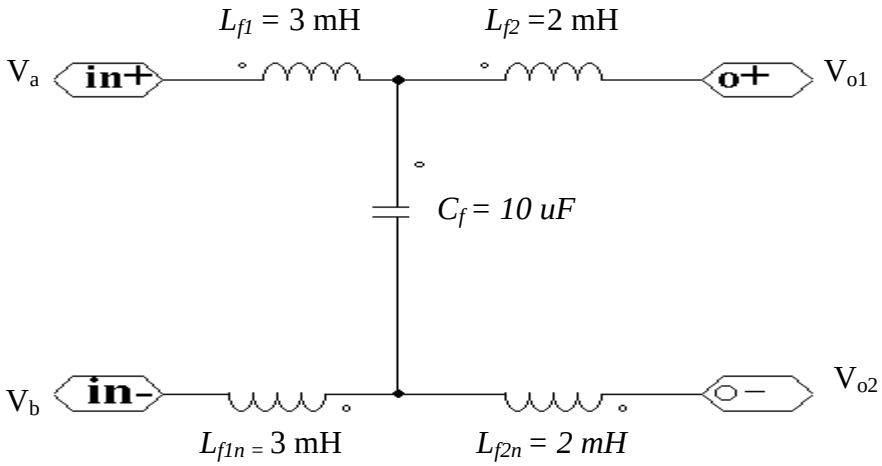
Figure 5.1 shows the schematic diagram of a transformerless single-phase H-Bridge inverter circuit. The H-Bridge inverter consists of two legs to generated single phase sinusoidal AC power. The four insulated gate bipolar transistor (IGBT) power semiconductor devices are used in the H-Bridge inverter. The power semiconductor devices (S_1-S_4) are controlled by sinusoidal pulse width modulation (SPWM) technique. The hybrid, unipolar and bipolar SPWM switching techniques are simulated in this circuit.

The inverter has 400 V DC voltage. As mentioned in section 3.6, the values chosen are; 100 nF parasitic capacitance (C_{pv}) , 240 Ω resistor AC load, and symmetrical LCL filter comprising 3 mH inverter filter, 2 mH AC inductor filter and 10 uF AC capacitor for stand-alone system. This inverter is performed with 4 kHz and 8

kHz switching frequency when unipolar SPWM and bipolar SPWM are applied respectively.



(a)



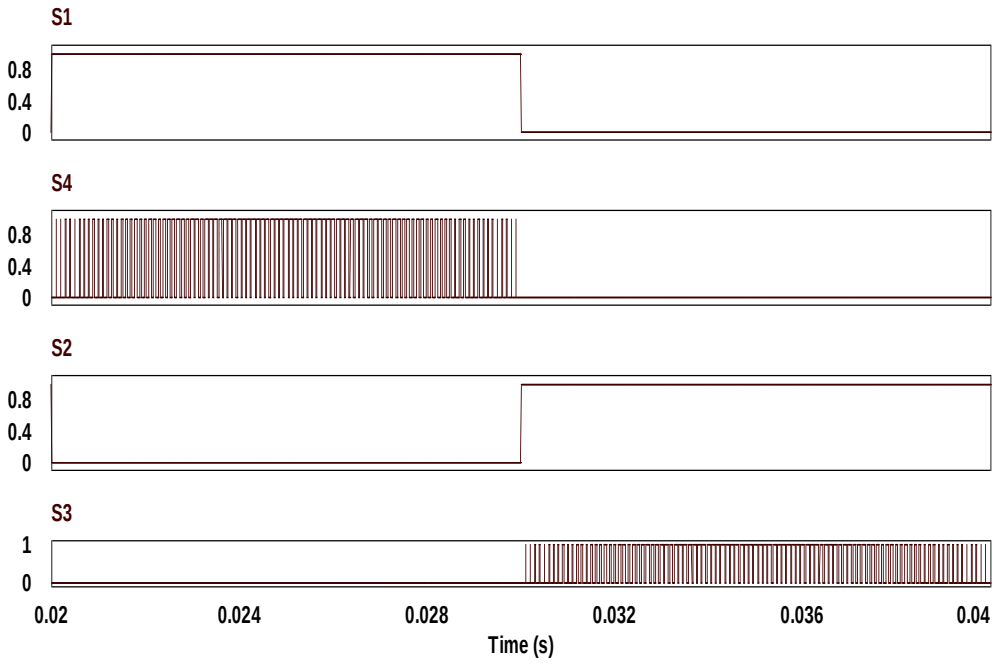
(b)

Figure 5.1: (a) Simulation set up for the single-phase transformerless H-Bridge inverter,(b) LCL filter configuration

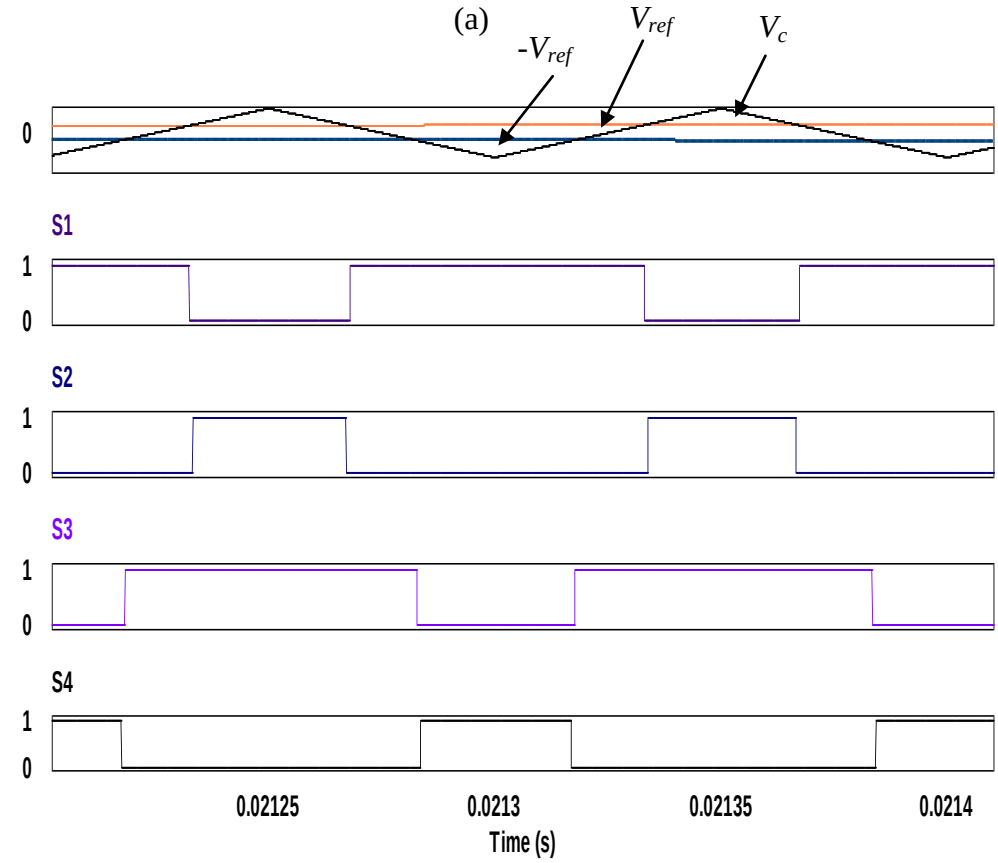
The switching patterns of the hybrid, unipolar and bipolar SPWM techniques are shown in Figure 5.2. In single-phase H-Bridge inverter with hybrid technique consists of two frequencies i.e. low frequency at 50 Hz and high frequency at 4 kHz. As shown in Figure 5.2(a), S_1 and S_2 are switched at low frequency, while the S_3 and S_4 are switched with high frequency. For the unipolar technique, the two-reference signal (V_{ref} and $-V_{ref}$) are used. V_{ref} and $-V_{ref}$ are created in positive and negative signs respectively. Figure 5.2(b) shows the switching pattern of unipolar technique. The pattern of the bipolar technique is illustrated in Figure 5.2(c), in which the two pair switches S_1&S_2, and S_2&S_3 are switched at same time. The two pair switches always turn ON and OFF alternately throughout its operation.

Figure 5.3(a) shows the output inverter voltage (V_{ab}) for the single-phase transformerless H-Bridge inverter topology when unipolar & hybrid and bipolar techniques are applied. As seen in Figure 5.3 (a), the three level output inverter ($+V_{dc}$, 0 and $-V_{dc}$) are generated. In contrast, the two level output inverter voltage ($+V_{dc}$ and $-V_{dc}$) when bipolar SPWM technique is applied in the H-Bridge circuit is shown in Figure 5.3(b).

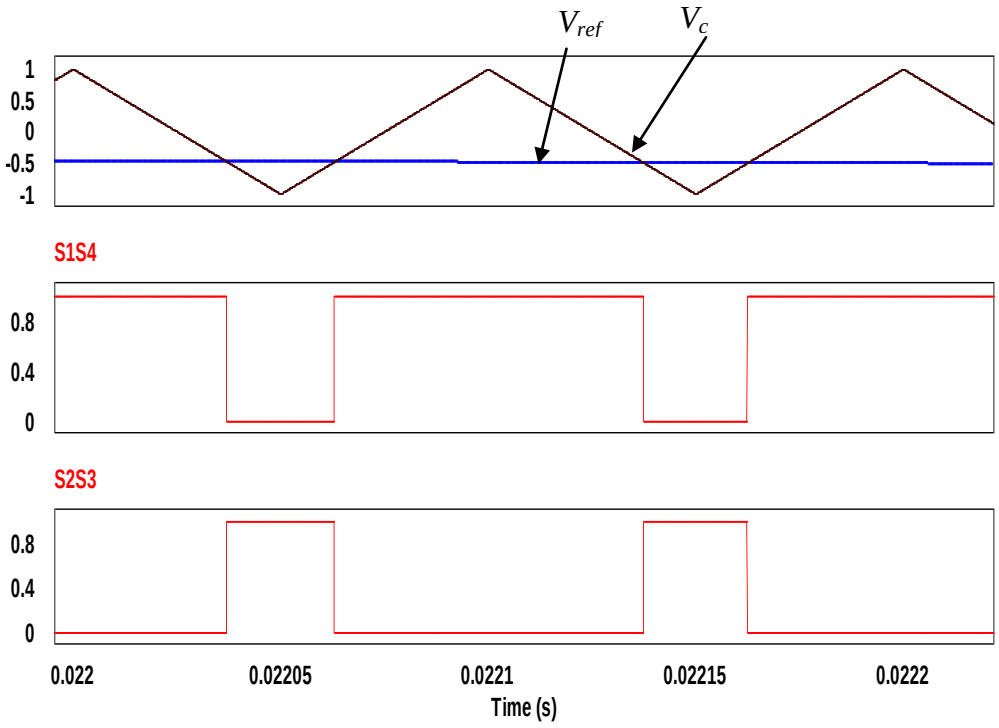
The common-mode voltage (V_{cmm}) is measured at the middle point between the two inverter output voltage to the ground (($V_{ao}+V_{bo}$) / 2). The voltage fluctuation appeared when the hybrid and unipolar SPWM technique is imposed in the transformerless H-Bridge inverter as shown in Figure 5.4(a). On other hand, Figure 5.4(b) shows a constant common-mode voltage when the bipolar SPWM technique is applied. Due to constant common-mode voltage (V_{cmm}) generated during all commutation states, the ground leakage current (I_g) flowing through the parasitic capacitance is very low ($\approx$ 0 A) as shown in Figure 5.5(a). Conversely, high-level amplitude of ground leakage current ($I_g \geq$ 300 mA) is produced when the fluctuating common-mode voltage is produced as shown in Figure 5.5(b).


S1
0.8
0.4
0
S4
0.8
0.4
0
S2
0.8
0.4
0
S3
1
0
0.02
0.024
0.028
0.032
0.036
0.04
Time (s)

(a)

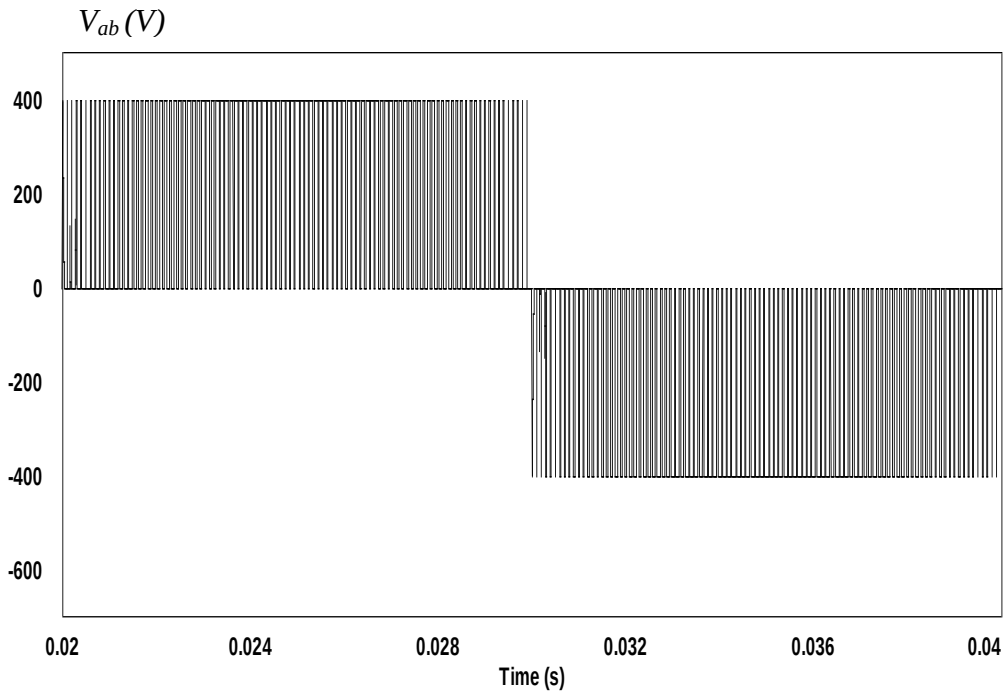

$-V_{ref}$
V_{ref}
V_c
0
S1
1
0
S2
1
0
S3
1
0
S4
1
0
0.02125
0.0213
0.02135
0.0214
Time (s)

(b)

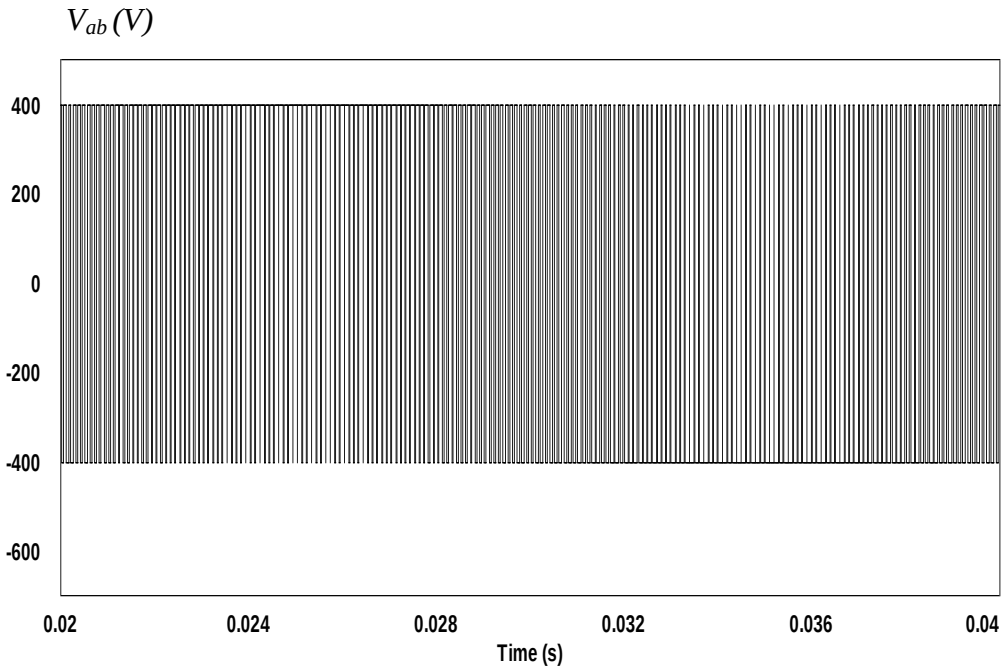


(c)

Figure 5.2: (a) Hybrid modulation technique, (b) unipolar modulation technique, (c) bipolar modulation technique of single-phase H-Bridge inverter

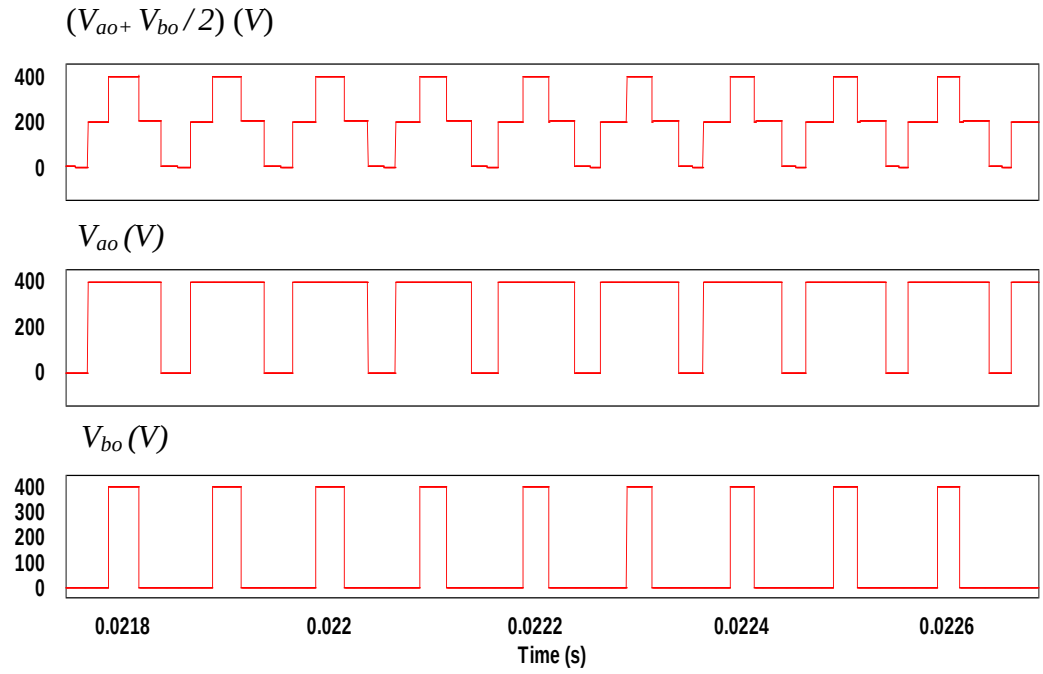


(a)

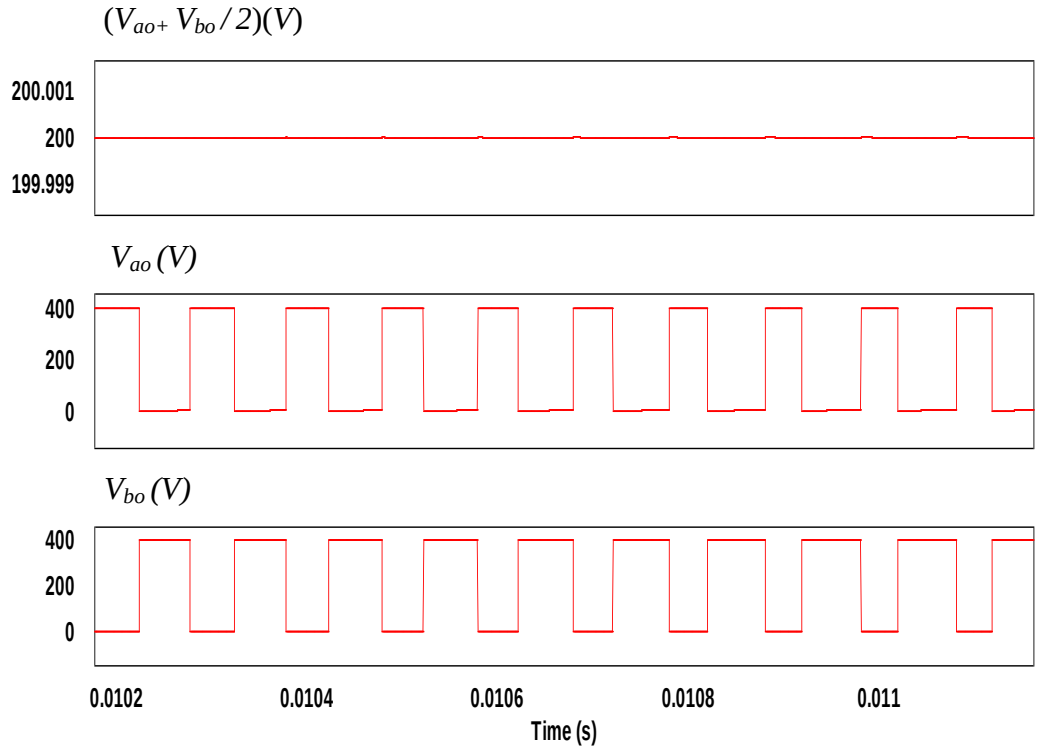


(b)

Figure 5.3: H-Bridge inverter output voltage for (a) hybrid & unipolar modulation techniques, (b) unipolar modulation technique

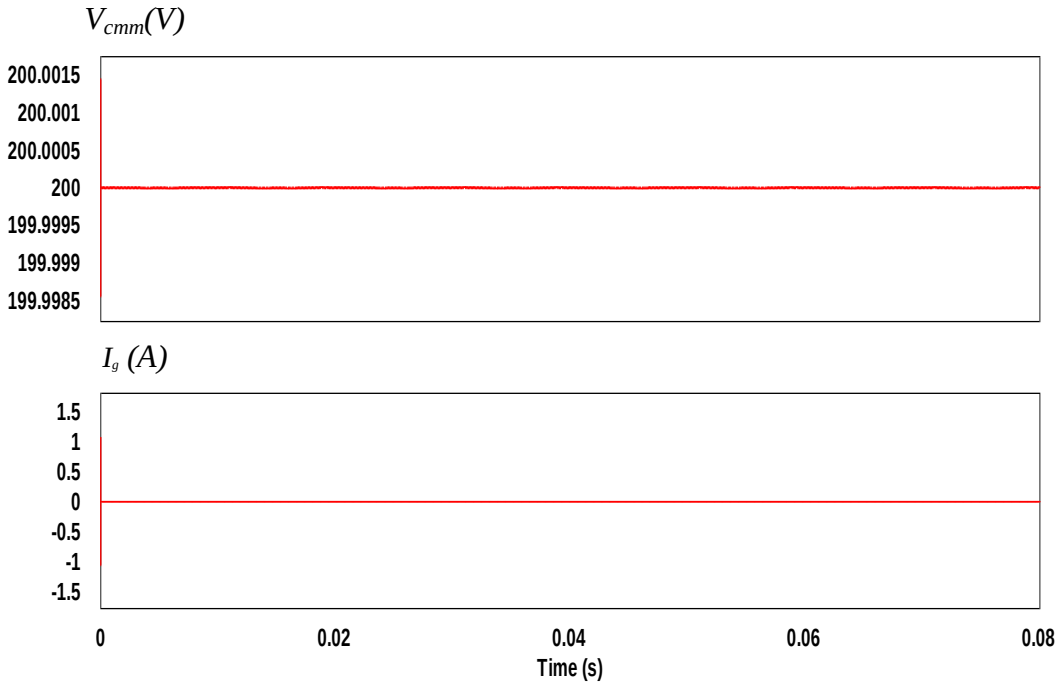


(a)

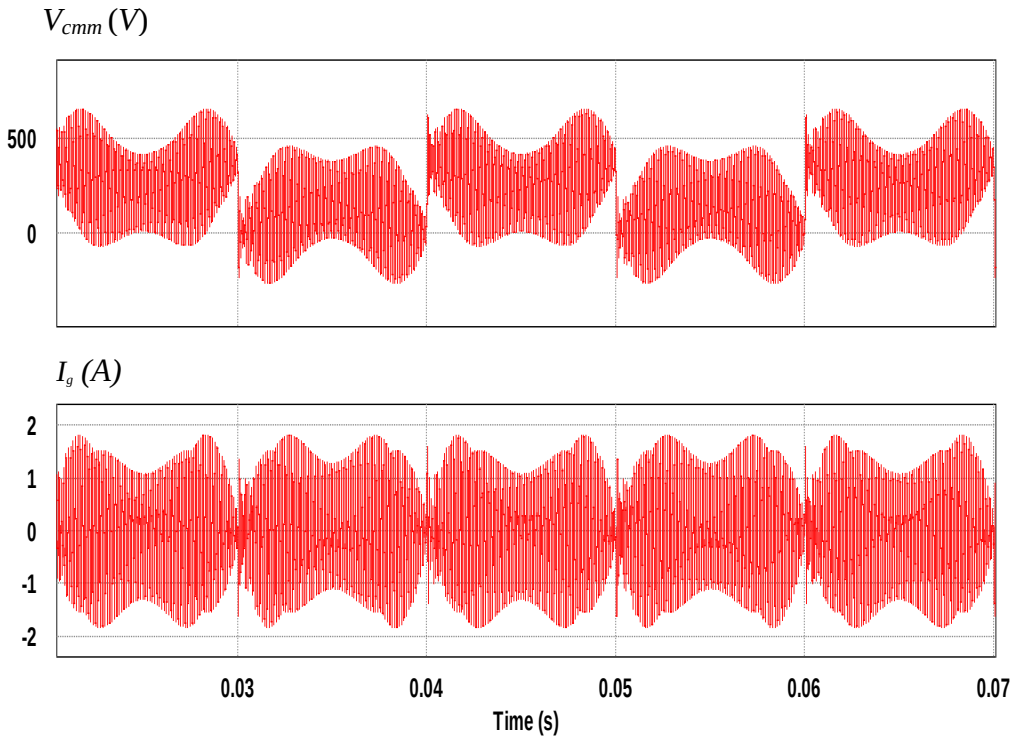


(b)

Figure 5.4: Common-mode voltage of H-Bridge inverter for (a) hybrid & unipolar modulation technique, (b) bipolar modulation technique



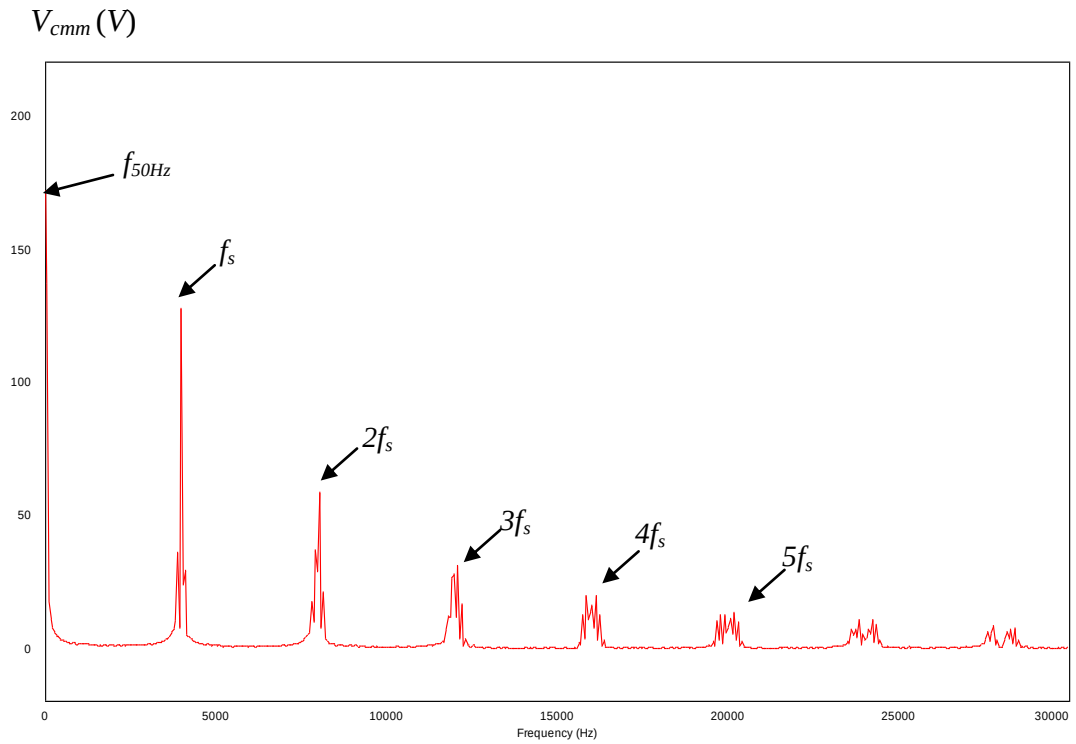
(a)



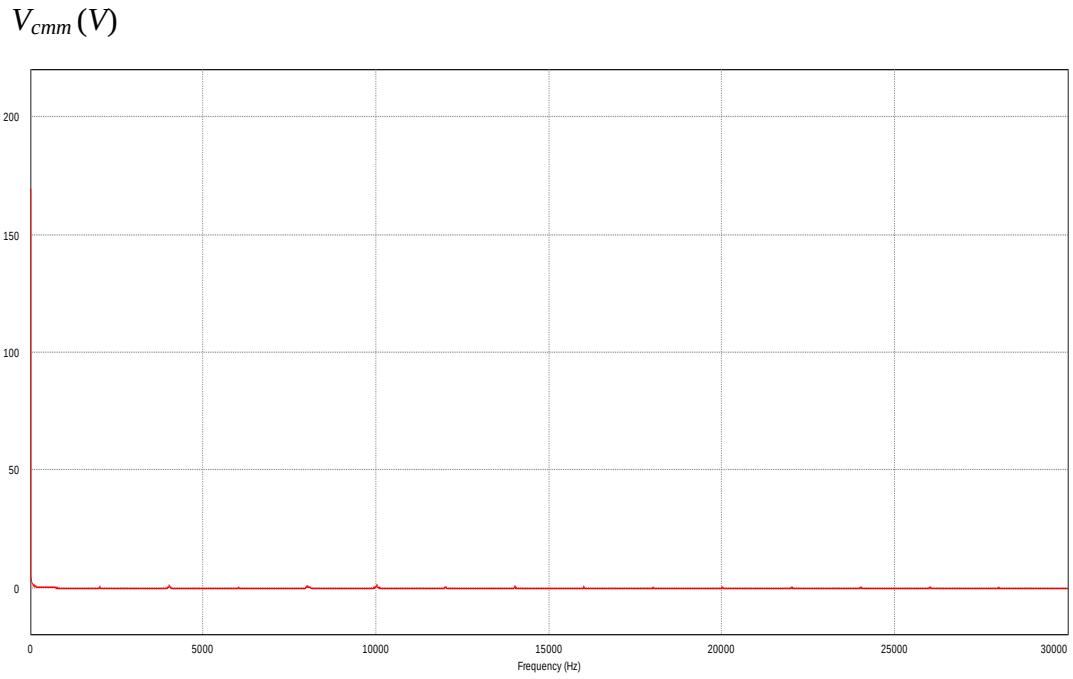
(b)

Figure 5.5: Ground leakage current of H-Bridge inverter for (a) bipolar modulation technique; (b) unipolar modulation technique

The harmonic spectrum of the common-mode voltage, which was generated using the PSIM simulation, is shown in Figure 5.6. The evaluation is based on V_i = 400 V, m_a = 0.8, f_{grid} =50 Hz, $f_{s,uni}$ = 4 kHz, and $f_{s,bi}$ = 8 kHz. Figure 5.6(a) shows high harmonic components appearing in every multiple of the switching frequency (f_s), when the unipolar SPWM technique was used. Figure 5.6(b) shows no harmonic components appearing when the bipolar SPWM technique was used.



(a)

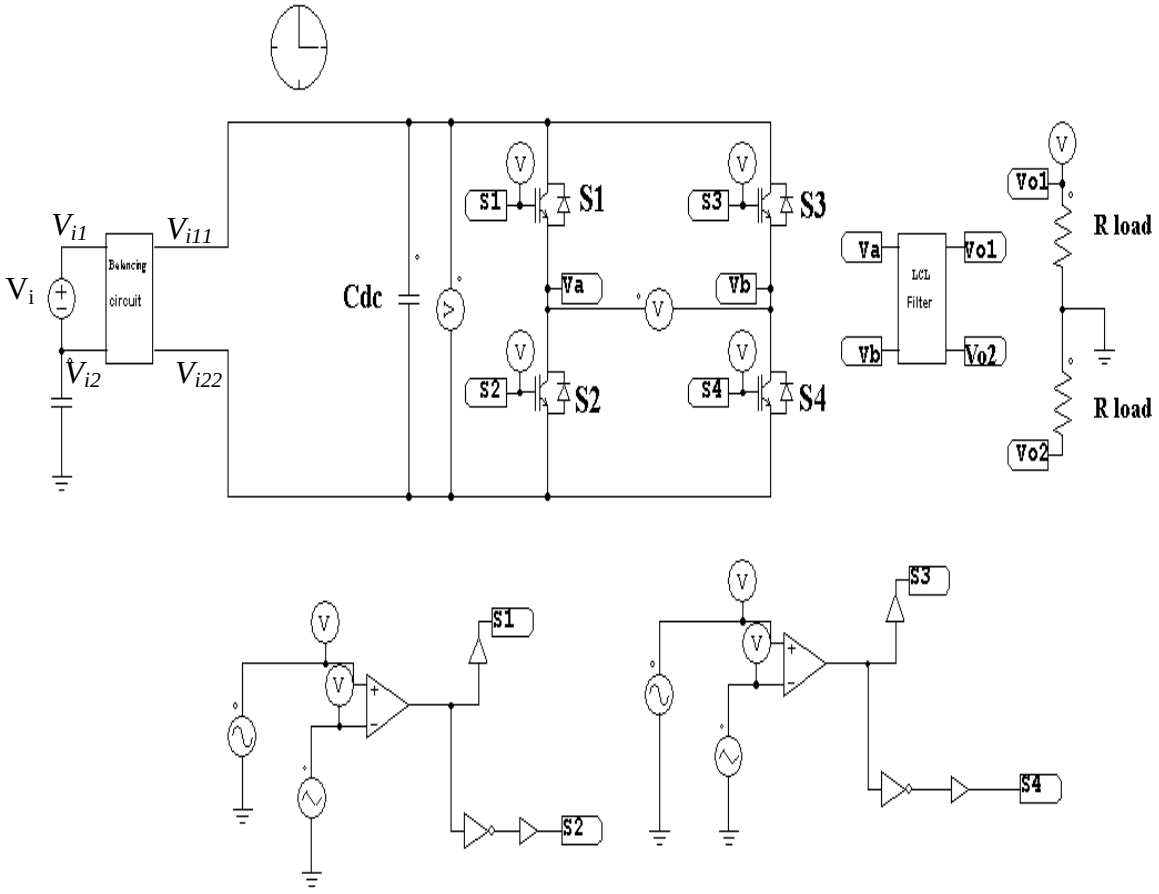


(b)

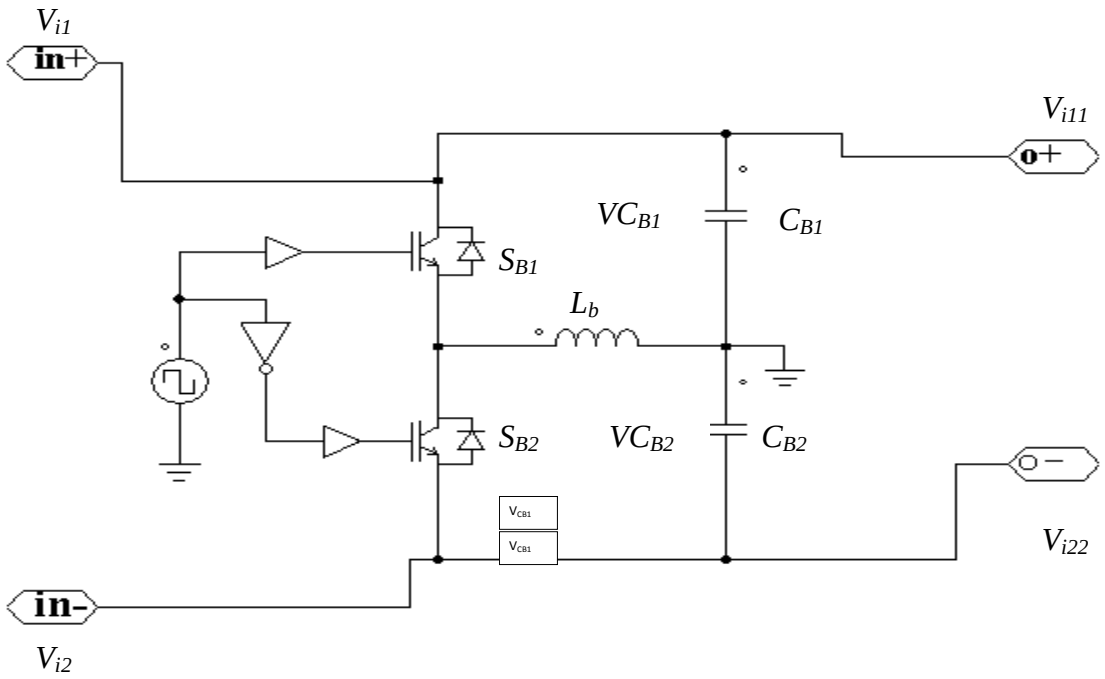
Figure 5.6: Simulated harmonic spectra of the H-Bridge inverter common-mode voltage of the (a) unipolar and (b) bipolar SPWM techniques

5.3 Proposed SC-HB Configuration

The schematic diagram of the proposed SC-HB inverter configuration is depicted in Figure 5.7. In this circuit, ideal IGBTs (integrated gate bipolar transistor) and ideal diodes have been used. The simulation is performed using PSIM 9 and the results are verified by a hardware prototype where its parameters are listed in Table 5.1. Dead time (t_d) of 0.8 µsec is chosen to avoid the dc-link from being shorted during the switching commutation. An LCL filter is placed at the output of the H-Bridge inverter to suppress the switching harmonics and to provide better grid decoupling.



(a)



(b)

Figure 5.7: (a) Shematic diagram of SC-HB inverter configuration,(b) balancing circuit

Table 5.1: Simulation and experiment parameters of proposed SC-HB inverter

Parameter	**Value**
L_{f1}=L_{f1n}	3 mH
L_{f2}=L_{f2n}	2 mH
L_b	1 mH
C_f	10 µF
C_{pv}	100 nF
C_{B1}=C_{B2}	2200 µF
V_i	400 V
Switching frequency for balancing circuit and H-Bridge inverter, f_s	4 kHz
Dead time, t_d	0.8 µs

In order to see the importance of the voltage balancing circuit, two simulations are conducted using PSIM simulation package. Firstly, the proposed inverter circuit is simulated without the balancing mechanism whereby S_{B1}, $S_{B2,}$ $L_{b,}$ C_{B1} & C_{B2} are excluded. Subsequently, simulation is repeated for the case where the balancing

mechanism is used together with the SC-HB inverter. The results are shown in Figure 5.8(a) and 5.8(b) respectively. For both simulations, the initial values of the series capacitor voltages, VC_{B1} and VC_{B2}, are set arbitrarily to 225 V and 175 V respectively to emulate the condition where both series dc-link capacitor voltages (VC_{B1} and VC_{B2}) are unequal. Results in Figure 5.8(a) shows that the both capacitor voltages are unbalanced in the absence of balancing circuit. With the balancing circuit, both series dc-link capacitor voltages are balanced and equal in the steady state period as shown in Figure 5.8(b).

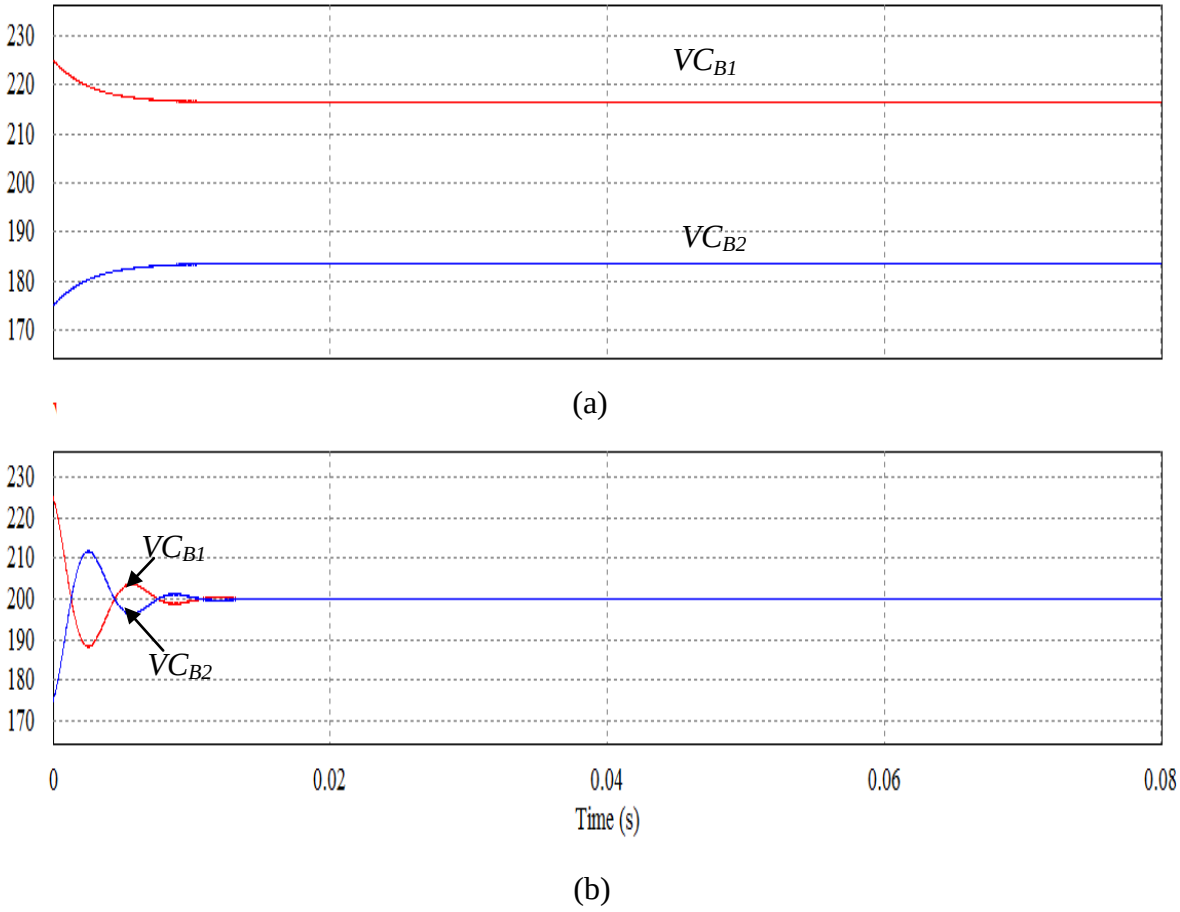


Figure 5.8: (a) Capacitor voltage (VC_{B1} & VC_{B1}) without balancing circuit, (b) capacitor voltage (VC_{B1} & VC_{B1}) with balancing circuit

Figure 5.9 shows the simulated common-mode voltage (V_{cmm}) and ground leakage current (I_g) waveforms for the SC-HB inverter topology. By adopting the balancing circuit, the common-mode voltage remains constant at half of V_{PV} , i.e. V_{cmm} = 400/2 = 200 V, as shown in Figure 5.9(a) . When common-mode voltage is constant, the ground leakage current through the PV parasitic capacitance becomes negligible, as proven by Figure 5.9(b). In this figure, the current I_g is observed to be approximately zero. The simulation results show the validity of the proposed topology in reducing the ground leakage current as stated before. The results are further verified with experiment results in the subsequent section.

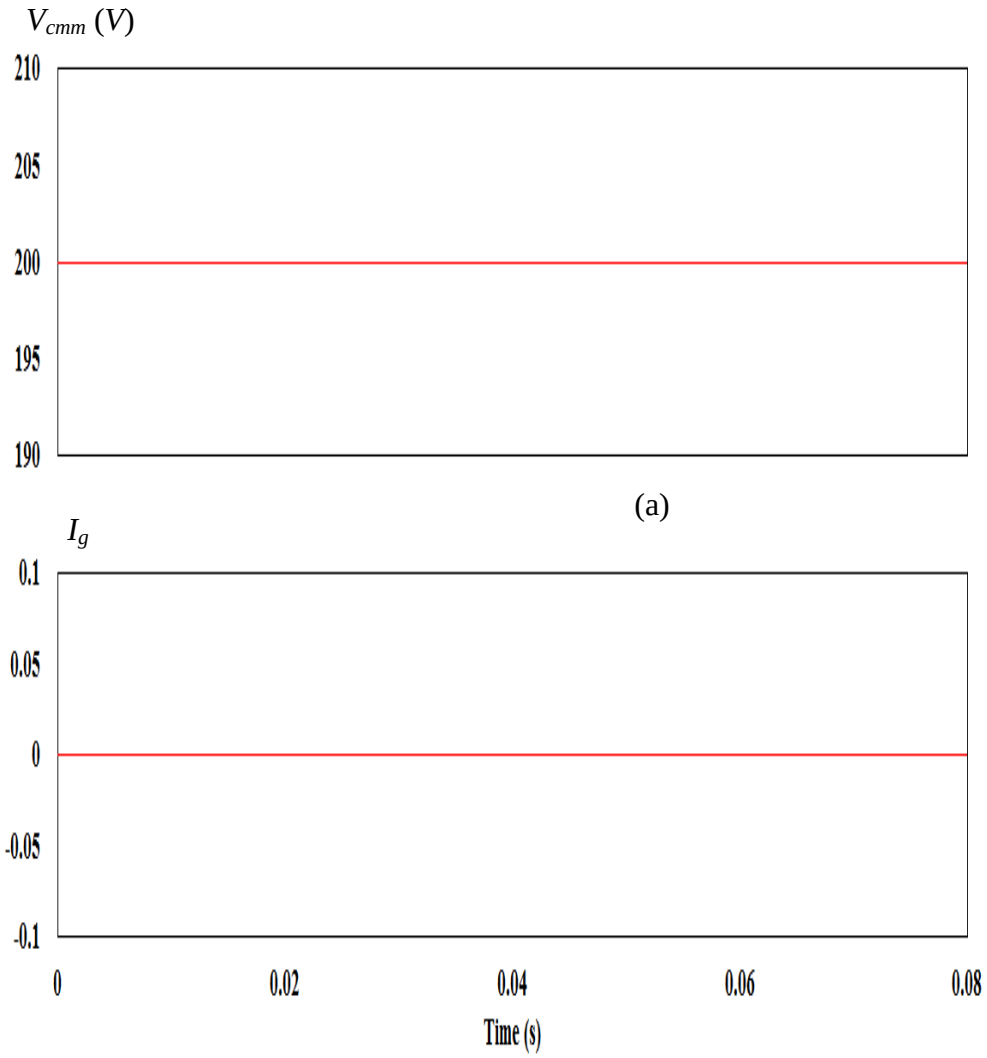


Figure 5.9: Simulation results of proposed SC-HB inverter topology; (a) common-mode voltage (V_{cmm}), (b) ground leakage current (I_g)

Figure 5.10 shows the simulated common-mode voltage (V_{cmm}) with respect to the dead time of switches S_1& S_2 (for leg *a* of unipolar H-Bridge inverter) and imbalanced dc-link capacitor voltages (VC_{B1} and VC_{B2}). Here, without the impact of dead time and imbalanced voltage, the common-mode voltage remains constant.

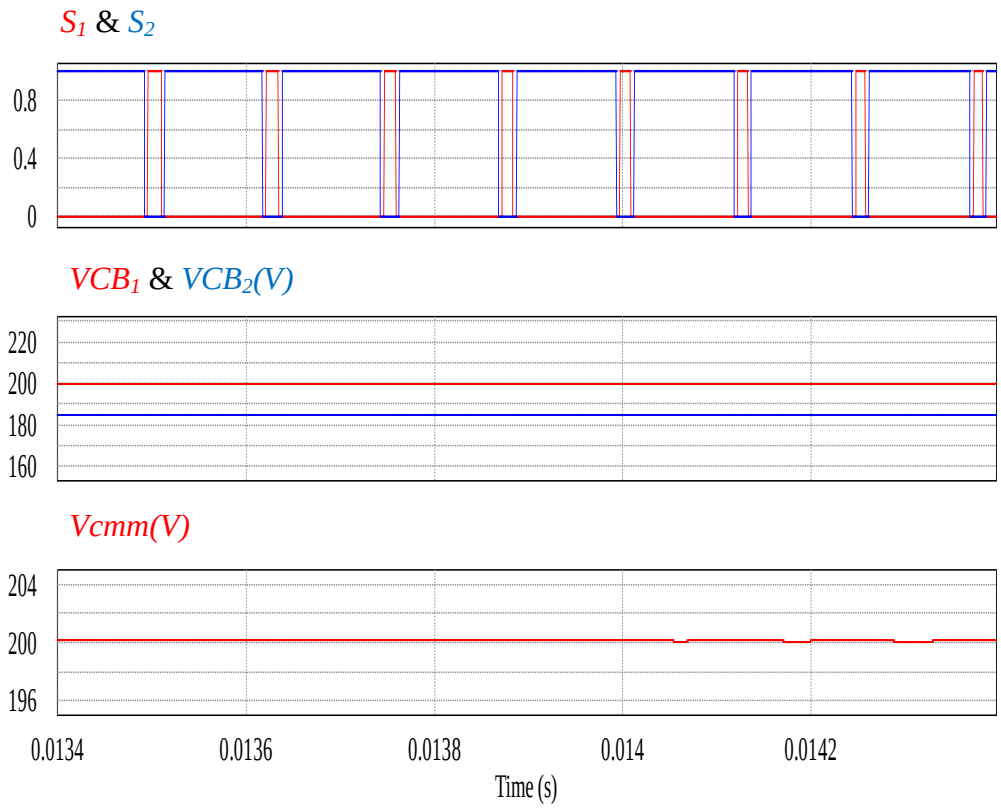
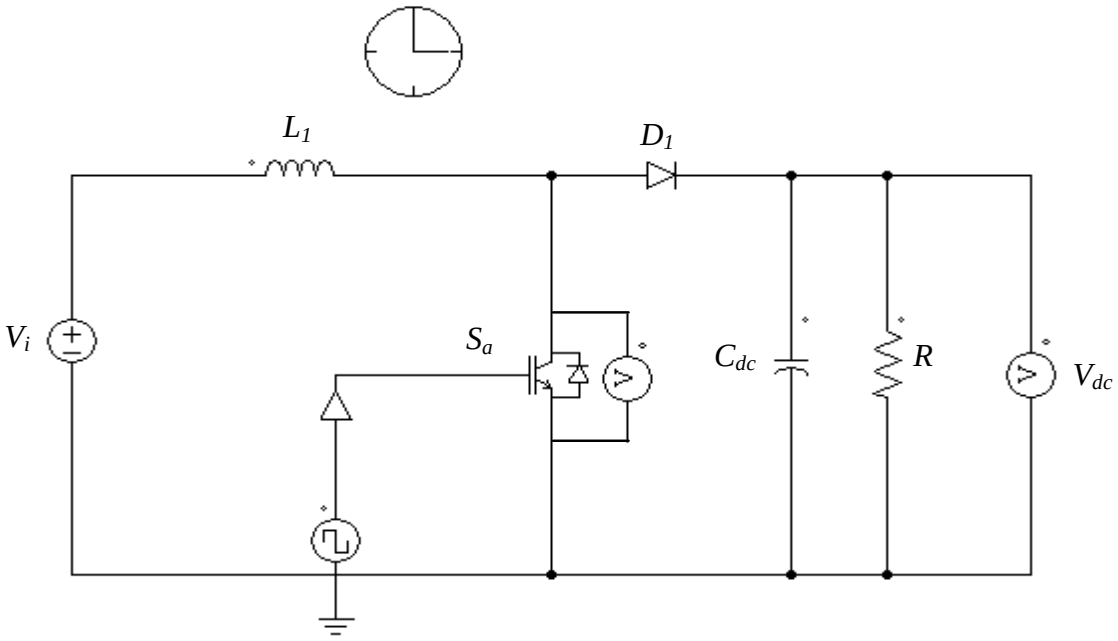


Figure 5.10: S_1&S_2 switching, dc link series voltage (VC_{B1} & VC_{B2}) and Common-mode voltage (V_{cmm}).

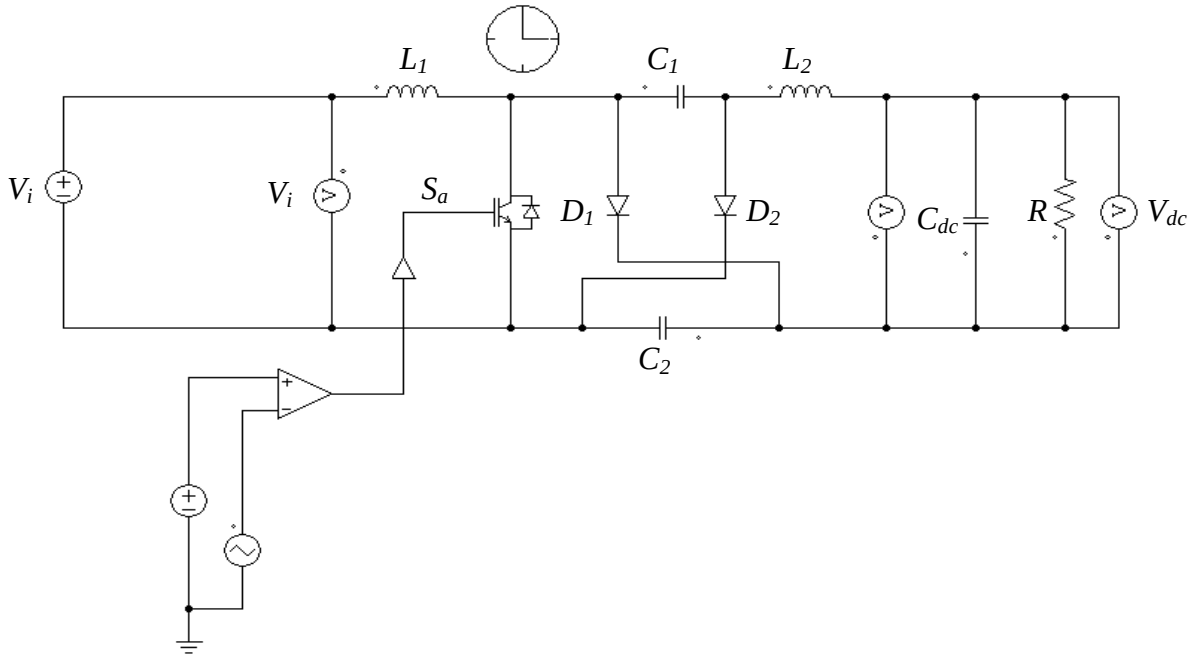
5.4 Conventional Boost Converter and CD-Boost Converter

The schematic diagrams of conventional boost converter and CD-Boost converters are shown in Figure 5.10. 60 V_i, L_1 = 1 mH and C_{dc} = 2200 uF are used to both converters. The output converter voltage (V_{dc}) and switch stress voltage (V_s) of the conventional boost converter and CD-Boost converter are depicted in Figure 5.11(a) and Figure 5.11(b) respectively. With the 60 V input dc voltage and 0.7 duty cycle, the output of conventional converter voltage is 200 V. While the CD-Boost converter output voltage is 400 V, which is higher compared to the conventional converter.

The switch stress voltage is measured between collector and emitter terminal of power device (S_a). From Figure 5.11(a), the switch stress voltage (V_s) of conventional converter is equal to the output converter voltage (V_{dc}). On the other hand, the switch stress voltage (V_s = ½ V_{dc}) of the CD-Boost converter is equal to half of the output converter voltage (V_{dc}).

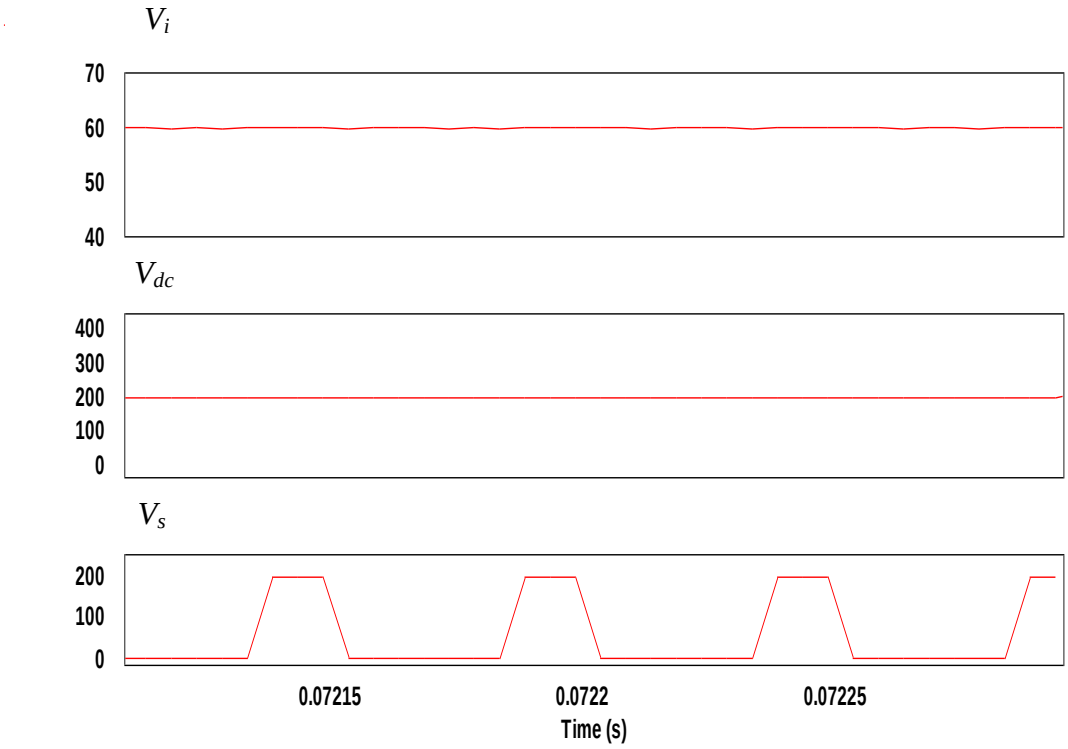


(a)

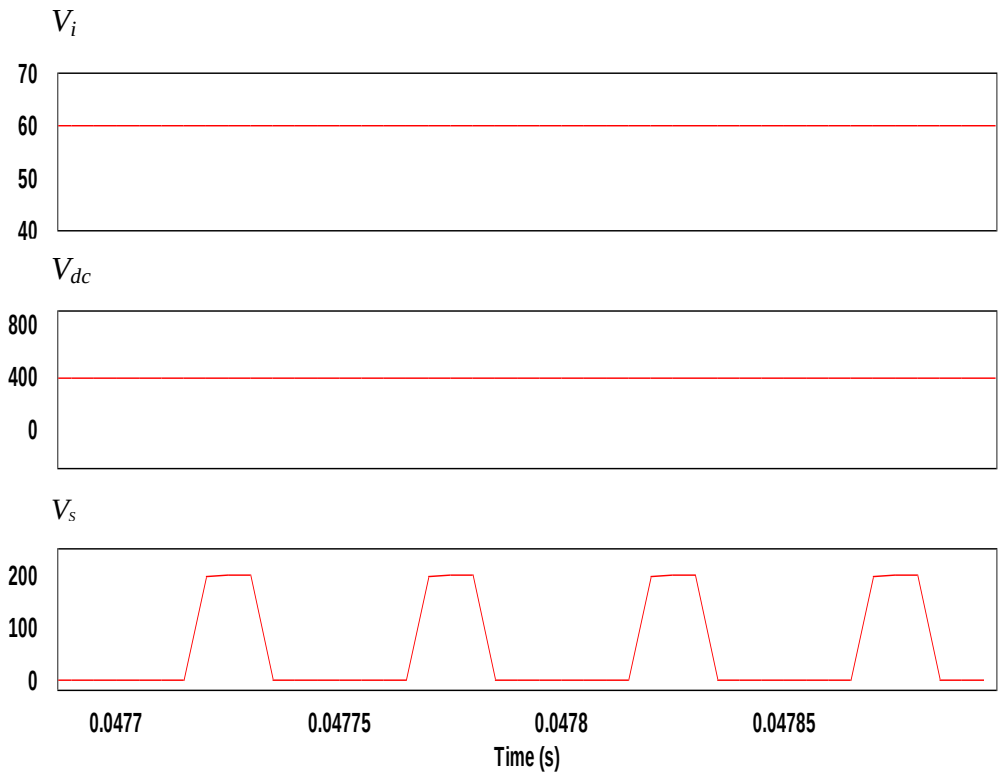


(b)

Figure 5.10: (a) Conventional boost converter circuit, (b) CD-Boost converter circuit



(a)



(b)

Figure 5.11: Input voltage (V_i), output converter voltage (V_{dc}) and switch stress voltage (V_s) for (a) conventional converter, (b) CD-Boost converter

5.5 Proposed Bipolar H-Bridge Inverter with CD-Boost Converter

Due to advantages of high output converter voltage and a lesser amount of switch stress voltage, the CD-Boost converter is integrated with bipolar H-Bridge inverter. Table 5.2 lists the parameters used in the bipolar H-Bridge inverter with CD-Boost converter. Figure 5.12 shows the schematic diagram of a bipolar H-Bridge inverter with CD-Boost converter. The 60 V input voltage is applied in this system. The output dc voltage of the CD-Boost converter is supplied to bipolar H-Bridge inverter. The output and ac voltage of bipolar H-Bridge inverter voltages are shown in Figure 5.13. Applying the bipolar SPWM technique produces constant common-mode voltage, as shown in Figure 5.14(a). The constant common-mode voltage generated low ground

leakage current (<300 mA) through the PV parasitic capacitance as indicated in Figure 5.14(b).

Table 5.2: Simulation and experiment parameter values of proposed bipolar H-Bridge inverter with CD-Boost converter and modified unipolar H-Bridge inverter with CD-Boost converter

Parameter items	Values
L_1	1 mH
C_b	2200 uF
C_1-C_2	15 uF
C_{dc}	270 uF
L_{f1},L_{f2}	3 mH, 2 mH
L_{f1n}, L_{f2n}	3 mH, 2 mH
C_f	10 uF
C_{pv}	100 nF

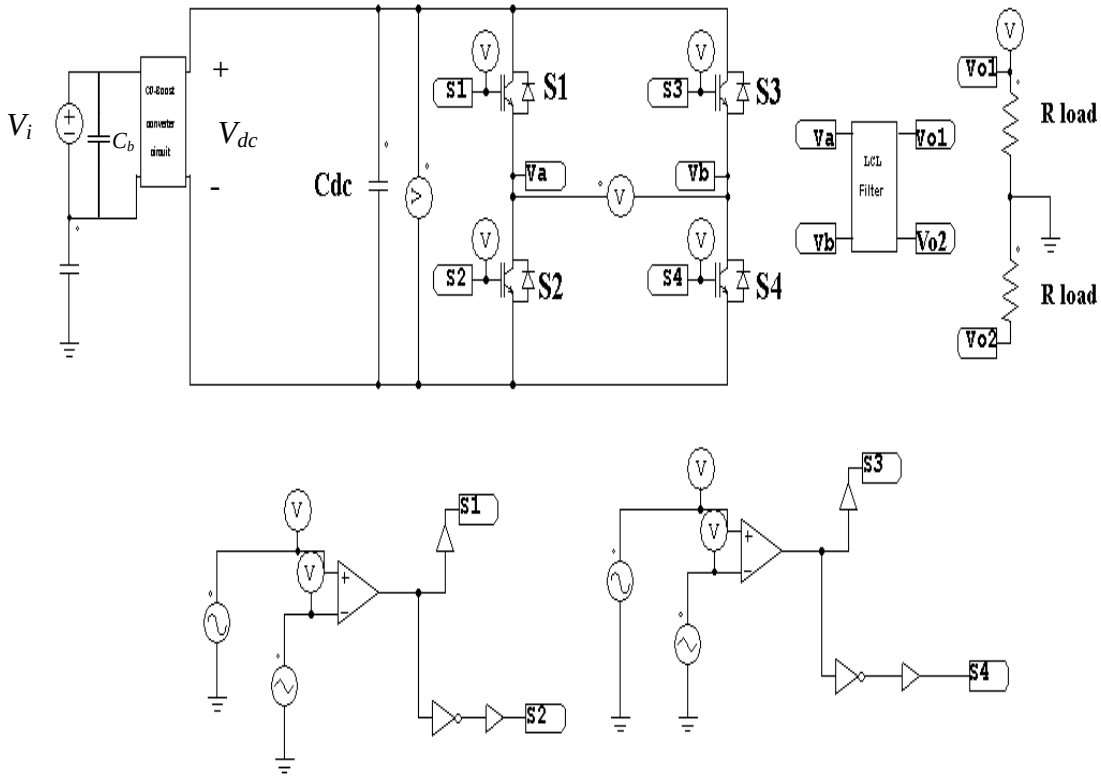


Figure 5.12: Schematic diagram of proposed bipolar H-Bridge inverter with DC-Boost converter system

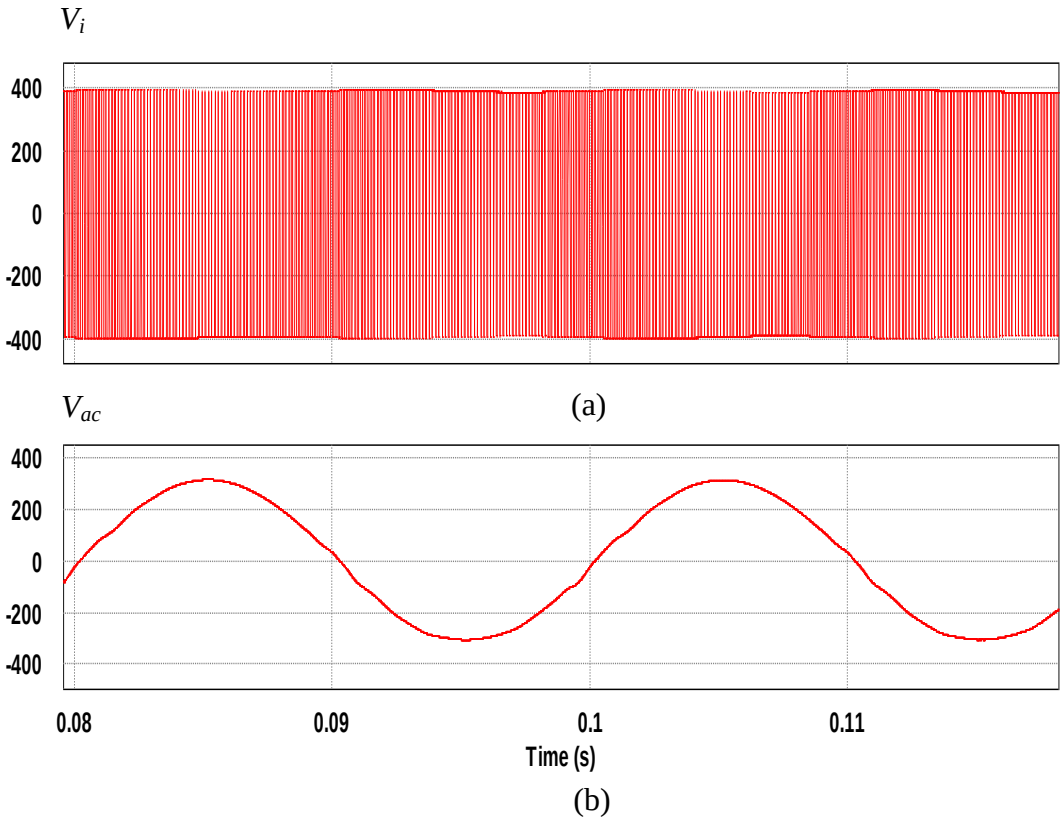


Figure 5.13: (a) Inverter voltage, (b) AC signal waveform of proposed bipolar H-Bridge inverter with CD-Boost converter

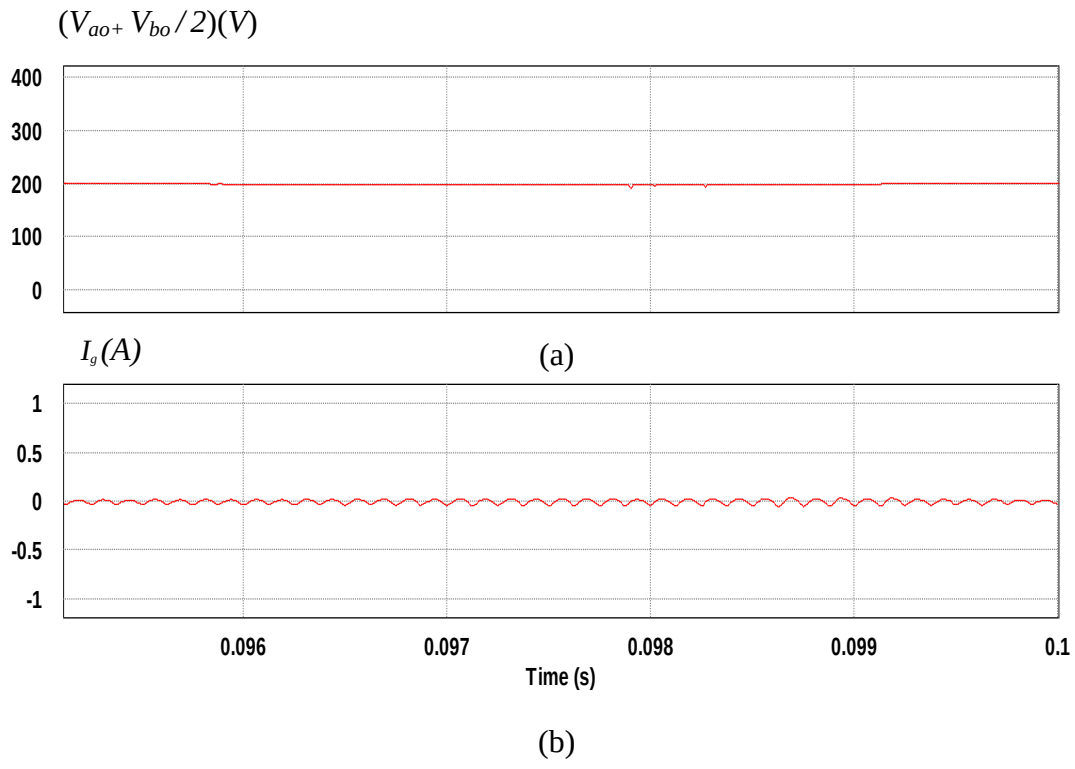


Figure 5.14 (a): Common-mode voltage, (b) ground leakage current of proposed H-Bridge inverter with CD-Boost converter system

5.6 Proposed Modified Unipolar H-Bridge Inverter with CD-Boost Converter

The schematic diagram of the proposed modified unipolar H-Bridge inverter with CD-Boost converter circuit is shown in Figure 5.15. The parameters value of proposed circuit is ilustrated in Table 5.2. The additional switches (*Sb* & *Sc*) are placed at the dc-link to disconnect the inverter from the PV source during zero state condition of the inverter circuit. As seen in Figure 5.16(a), during the positive zero state mode, *Sb* is turned off when *S1*&*S3* is opened. On the other hand, during the negative zero state mode, *S2* & *S4* is opened and *Sc* is turned off as shown in Figure 5.16(b).

Figure 5.17(a) shows the switching pattern for *Sa, Sb* & *Sc*. *Sa* is closed when both switches *Sb* & *Sc* are opened. During the *Sa* switching, the dc capacitor voltage reached 6.6 times of V_{PV} (V_{Cdc} = 6.6 V_{PV}), which functioned in boost operation. For this mode, when *Sb* & *Sc* are closed, the Sa is opened and the energy from the dc capacitor (C_{dc}) is transferred to the load by the H-Bridge inverter. The three-level inverter voltage is controlled by the unipolar SPWM H-Bridge inverter.

The proposed inverter circuit offers high gain conversion voltage, constant common-mode voltage and low ground leakage current. The constant common-mode voltage is shown in Figure 5.17(b) is controlled by simple switching of both switches (*Sb* & *Sc*). Due to the constant common-mode voltage, low ground leakage current is generated, depicted in Figure 5.17(b). Therefore, this is a good solution for transformerless inverter systems with high gain conversion voltage ratio and three-level inverter voltage.

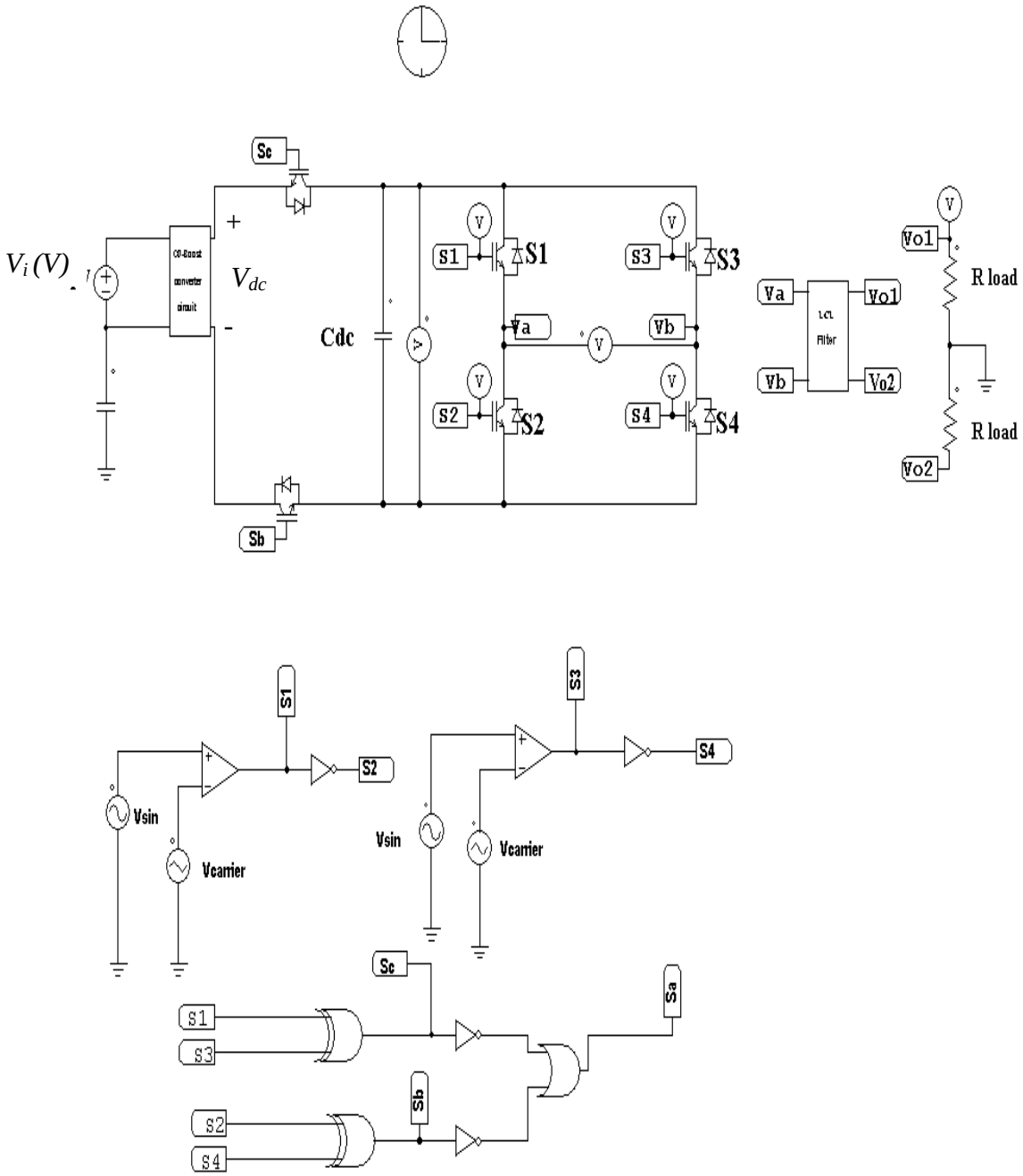
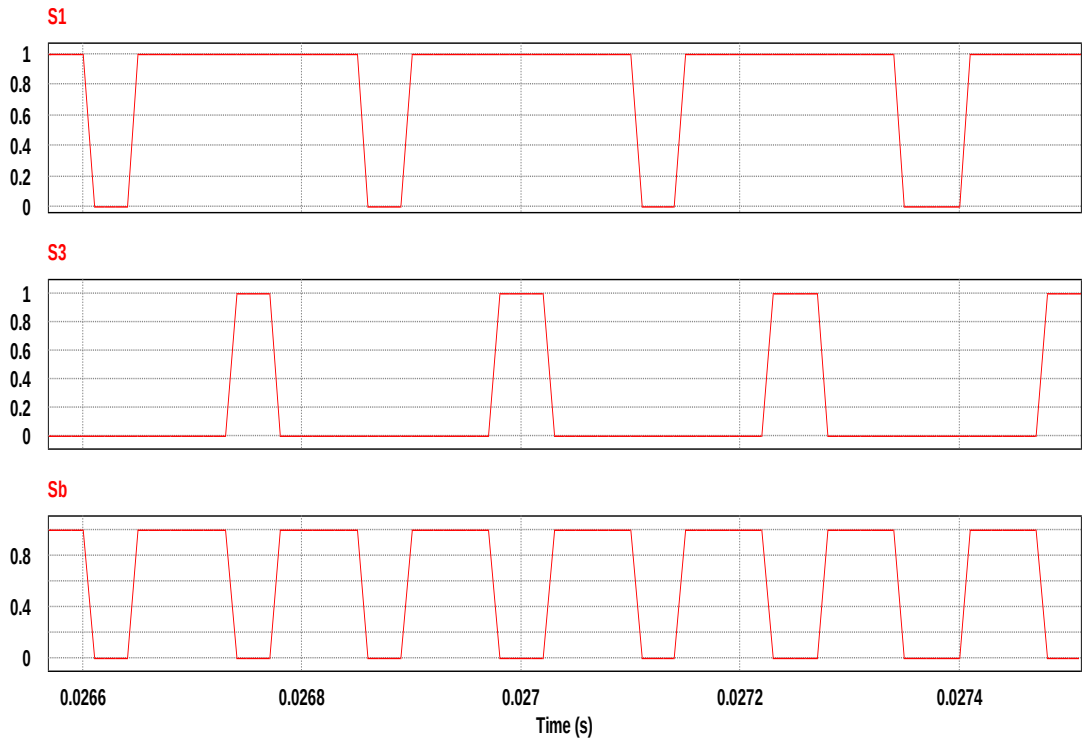
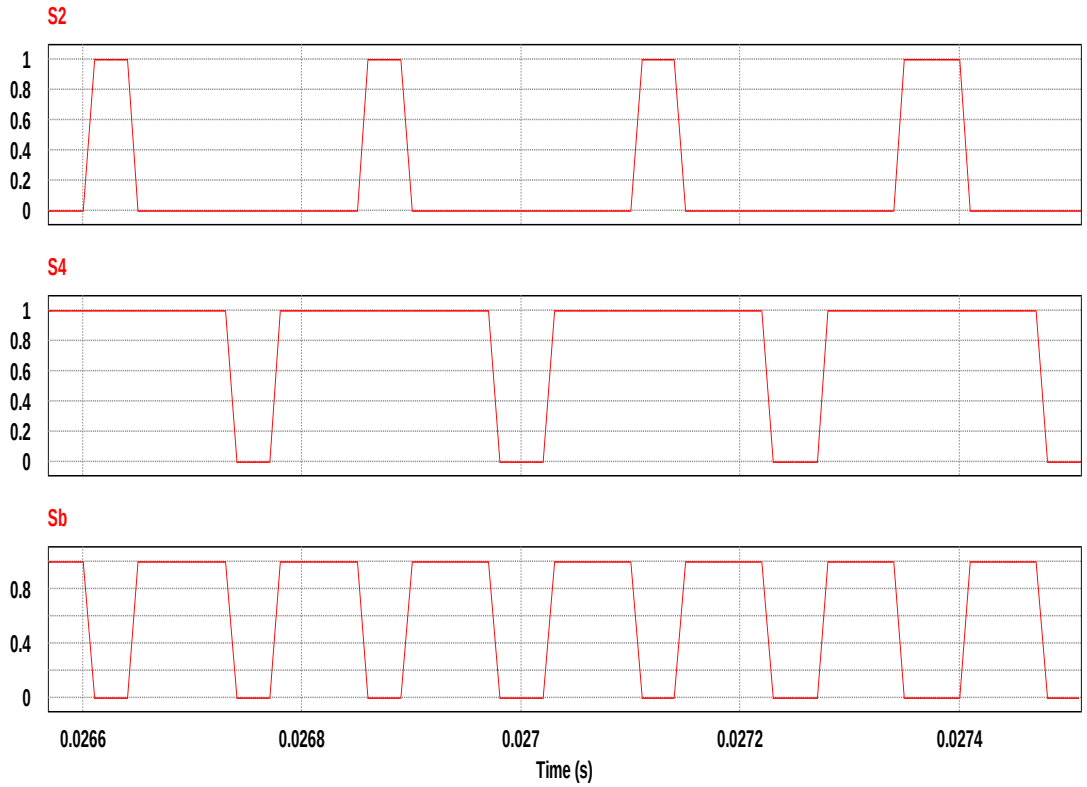


Figure 5.15: Modified unipolar H-Bridge inverter with CD-Boost converter circuit

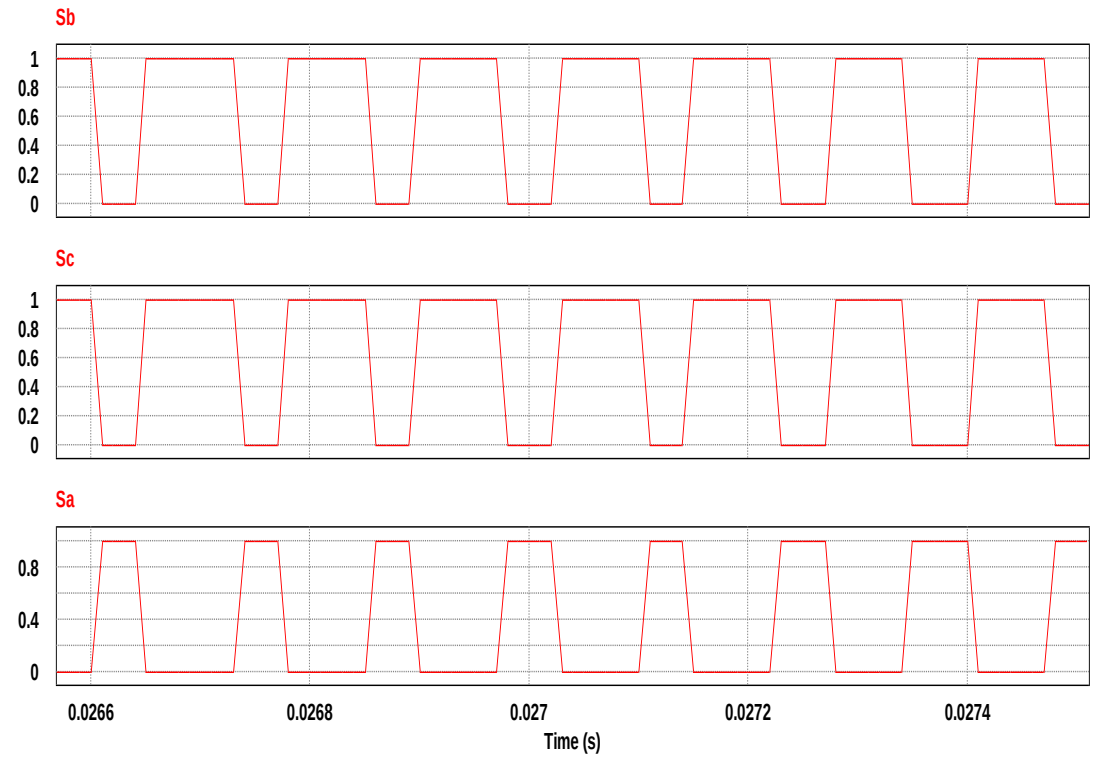


(a)

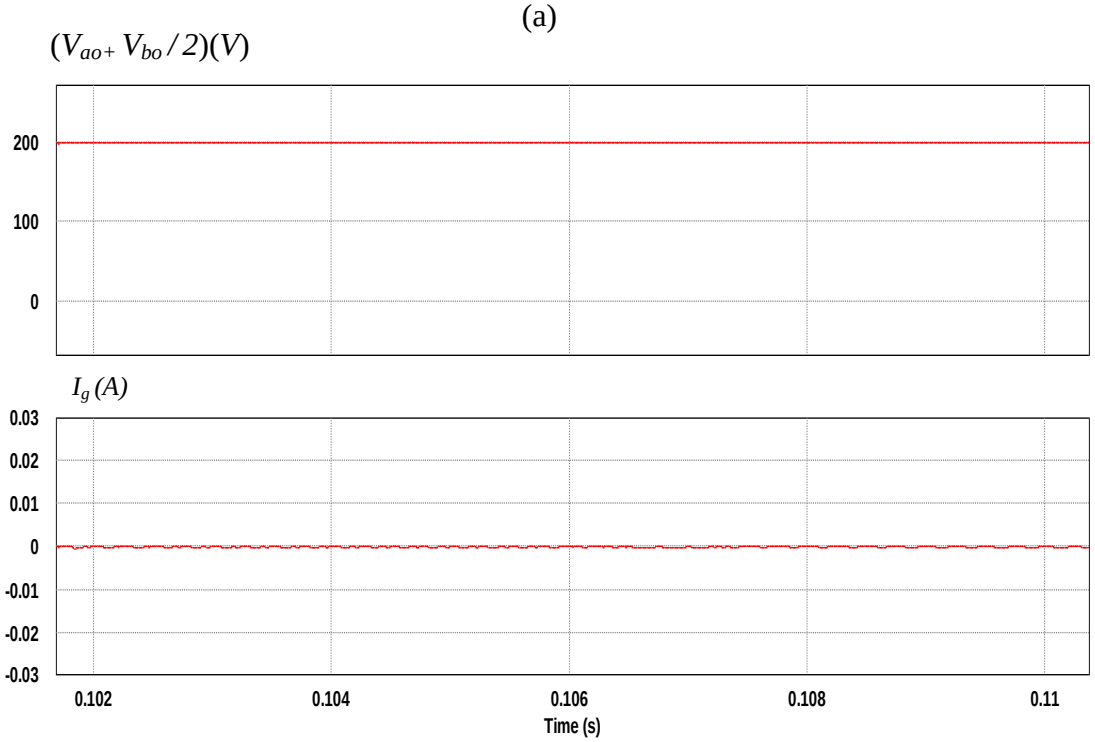


(b)

Figure 5.16: (a) Positive zero state mode for S1,S3 & Sc, (b) Negative zero state mode for S2,S4 & Sb of modified unipolar H-Bridge inverter with CD-Boost converter



(a)



(b)

Figure 5.17: Modified unipolar H-Bridge inverter with CD-Boost converter of (a) switching for Sb,Sc and Sa, (b) common-mode voltage and ground leakage current

5.7 Proposed Modified Unipolar H-Bridge Inverter with Modified Boost Converter

The schematic circuit of a proposed modified boost converter circuit with low input ripple current using the PSIM software is shown in Figure 5.18. Two inductors (L_1 & L_2 = 1 mH), and $C_1 = C_2$ = 15 uF are used in this circuit to decrease the input ripple. Figure 5.19 shows the input-current ripple waveform (ΔI_{L1}) of a conventional and the proposed boost converters during steady state. Figure 5.19(b) shows the proposed boost converter producing low input-current ripple (ΔI_{L1}) as compared to a conventional boost converter as shown in Figure 5.19(a). The advantages of the proposed low input current-ripple converter are less power transfer losses and higher power converter efficiency.

Due to low input current-ripple generated in the proposed converter, therefore that converter is integrated into modified unipolar H-Bridge inverter. The parameter of modified unipolar H-Bridge inverter is listed in Table 5.2. The schematic diagram of a transformerless modified unipolar H-Bridge inverter with modified boost converter is simulated using PSIM software and is depicted in Figure 5.20. The standard ac voltage with non-fluctuating common-mode voltage and low ground leakage current waveform are generated as shown in Figure 5.21. Therefore, this proposed inverter is another solution for the transformerless single-phase inverter system, which has low input current ripple and low ground leakage current.

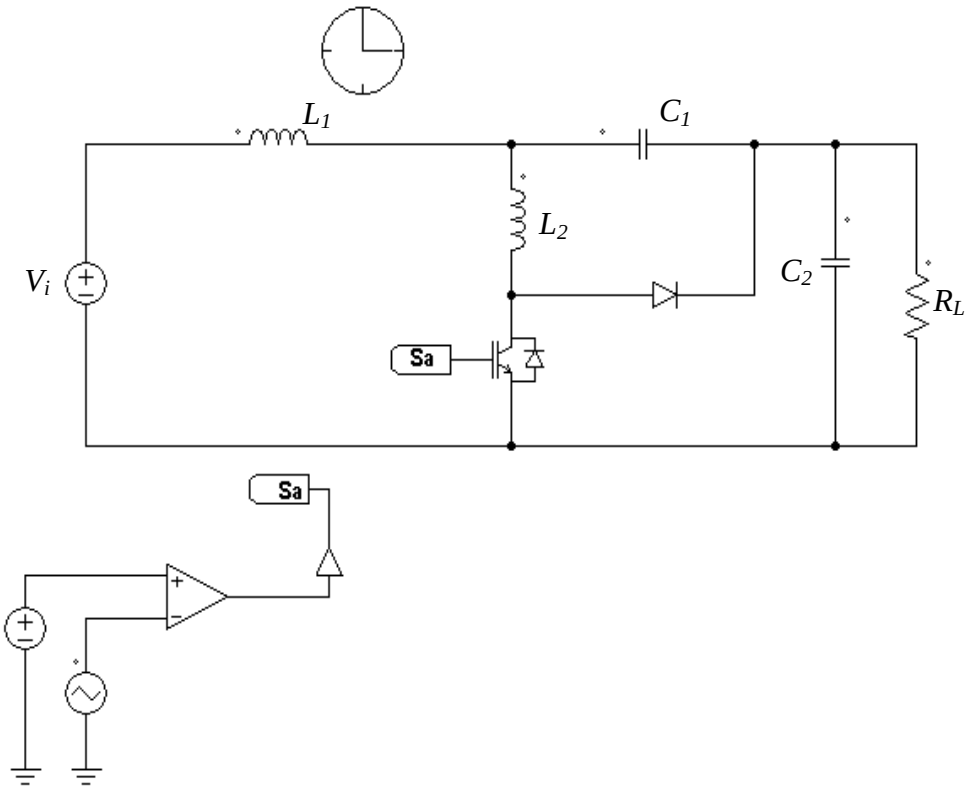
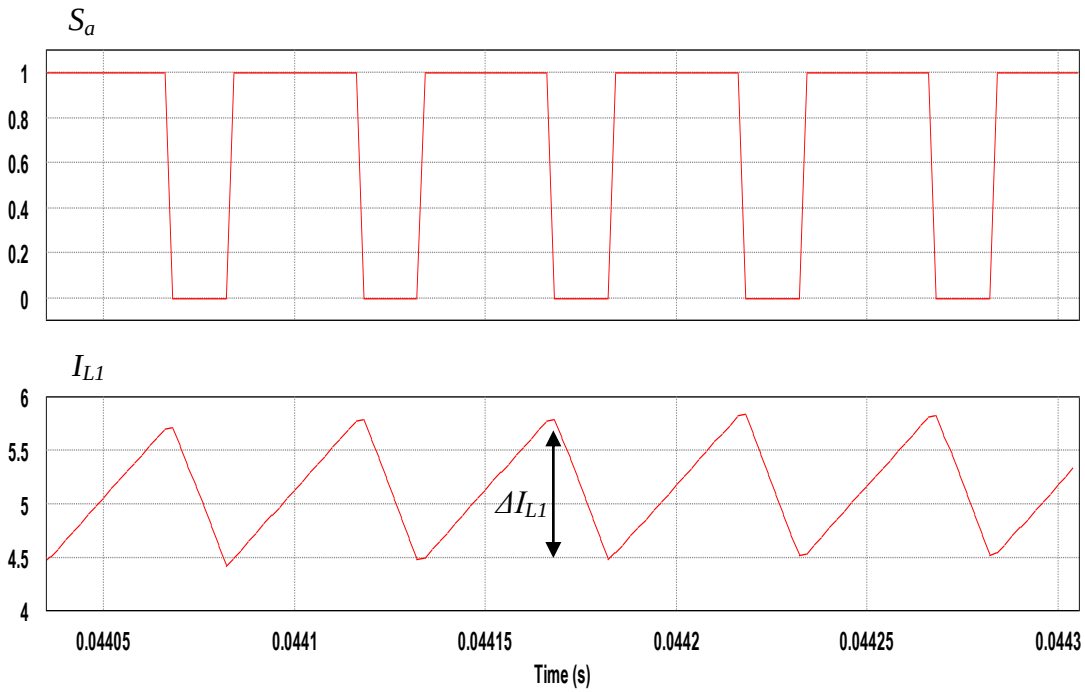
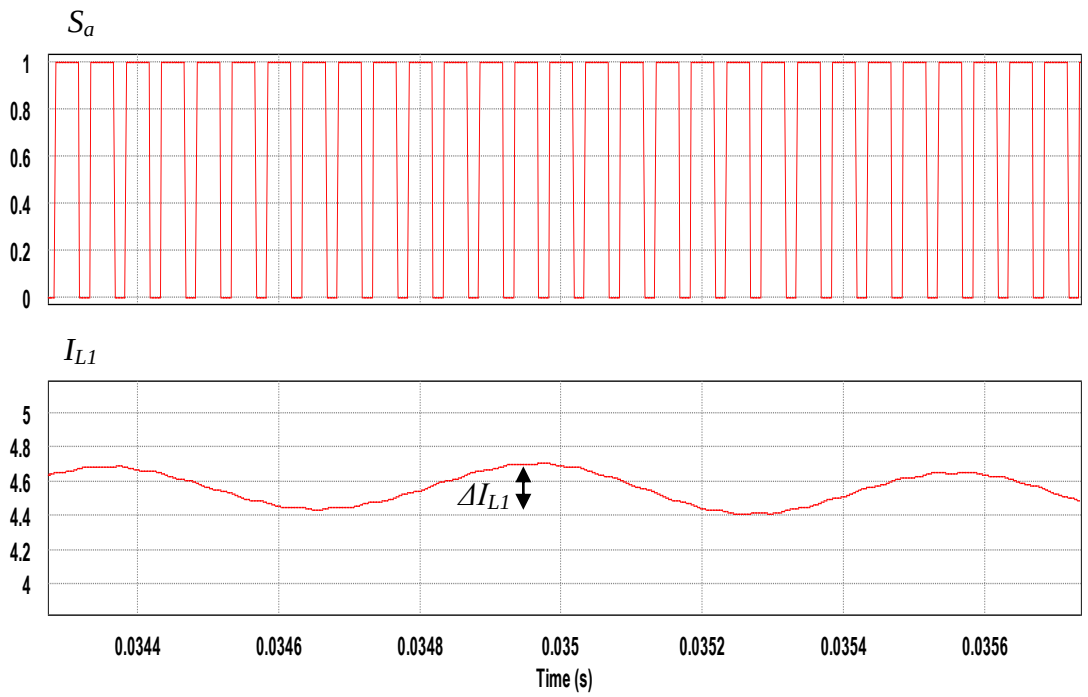


Figure 5.18: PSIM simulation results for the input currents of a proposed boost converter



(a)



(b)

Figure 5.19: (a) Δ_{IL1} of conventional boost converter, (b) Δ_{IL1} proposed modified boost converter

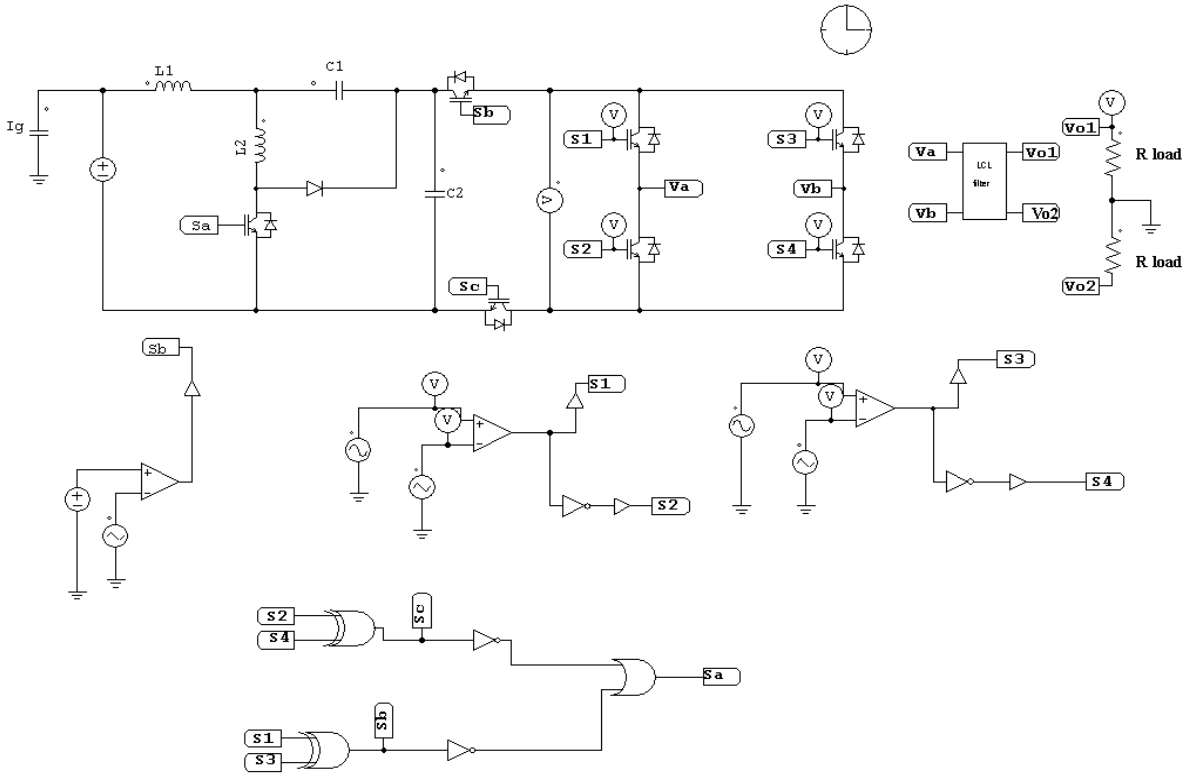


Figure 5.20: Shematic diagram of modified unipolar H-Bridge inverter with modified boost converter

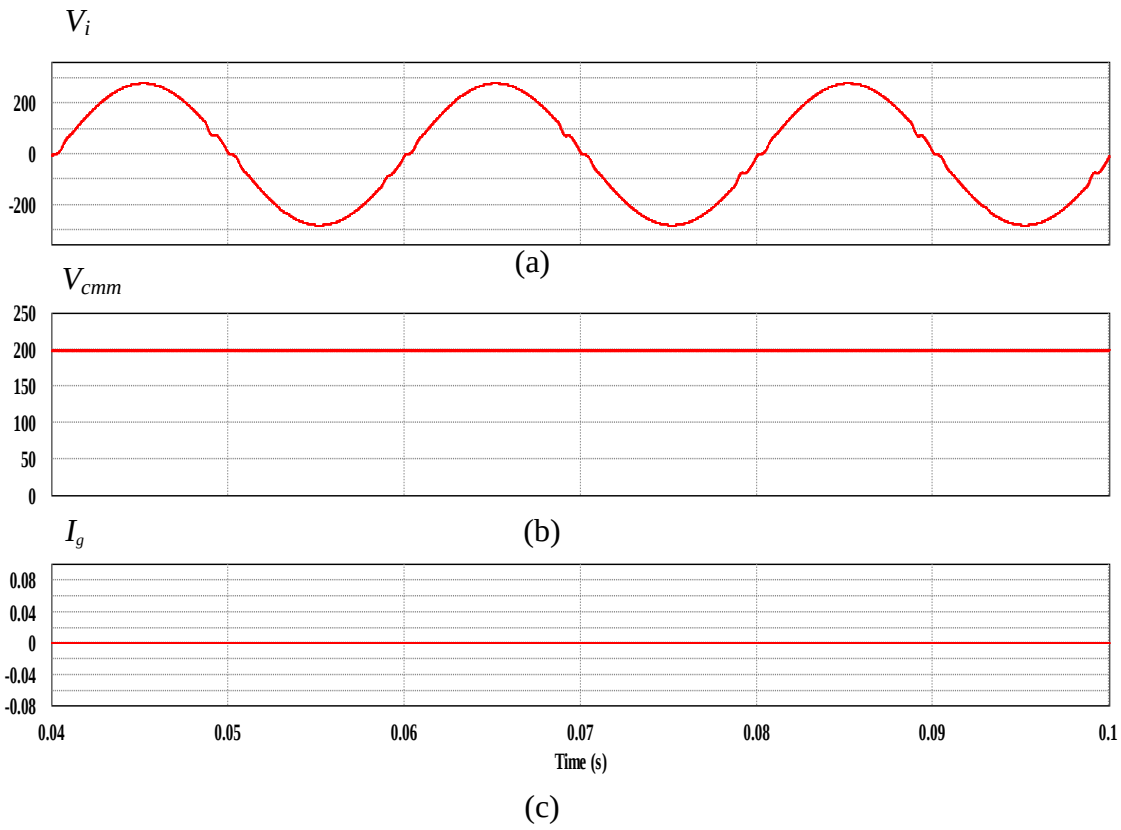


Figure 5.21: (a) AC voltage, (b) common-mode voltage, (c) ground leakage current of modified unipolar H-Bridge inverter with modified boost converter

5.8 Summary

The design of the proposed and conventional single phase H-Bridge inverter has been presented. The proposed modified boost converter with low input ripple has also been explained. The design of the proposed and conventional boost converter and inverter is carried out using PSIM simulation software. The simulation results of the constant common-mode voltage, low ground leakage current and low ripple input current have been presented and discussed.

CHAPTER 6

Experimental Results

6.1 Introduction

This chapter describes the implementation of hardware prototypes for testing the various non-isolated boost converters, the proposed modified boost converter with minimal ripple input dc current, the conventional transformerless H-Bridge inverter with conventional unipolar and bipolar PWM technique, proposed SC-HB inverter, proposed bipolar H-Bridge inverter with CD-Boost converter, proposed modified unipolar H-Bridge inverter with CD-Boost converter and proposed modified unipolar H-Bridge inverter with modified boost converter. The hardware prototypes are controlled by TMS320F2812 DSP (CCStudio 3.1). The system was tested for MPPT algorithm, power transfer balancing from DC power to AC power and anti-islanding protection.

6.2 Hardware Configuration

The experimental step-up of the prototype system is shown in Figure 6.1. The hardware includes a DC source (Sorensen, 600V/25A), the lab prototype proposed and conventional inverter, the lab prototype proposed and conventional boost converter, an LCL filter and a resistor load bank (3.3 kW Terco load resistor). The IGBT (G4PC50UD-E) and Diode (30CPF10) are used in this set-up.

Figure 6.1: Experimental setup

The IGBT switching signals and the power balancing control for the hardware prototype is generated using the Texas Instrument eZdsp ^{TM} F2812 kit as shown in Figure 6.2. This board includes the Code Composer Studio DSK Tools, power supply and parallel port cable.

Figure 6.2: eZdsp ^{TM} F2812 board kit

The overview functional block diagram of eZdsp ^{TM} F2812 board kit is shown in Figure 6.3. The C28x CPU has a very efficient C/C++ engine, able to control the system using a high-level language and enable math algorithms using C/C++. The DSP board supports two control peripherals, that is the event manager (EVA/EVB) to generate PWM signal with no extra circuitry and the 12-bit built-in analogue-to-digital converter (ADC) with sample-and-hold (S/H).

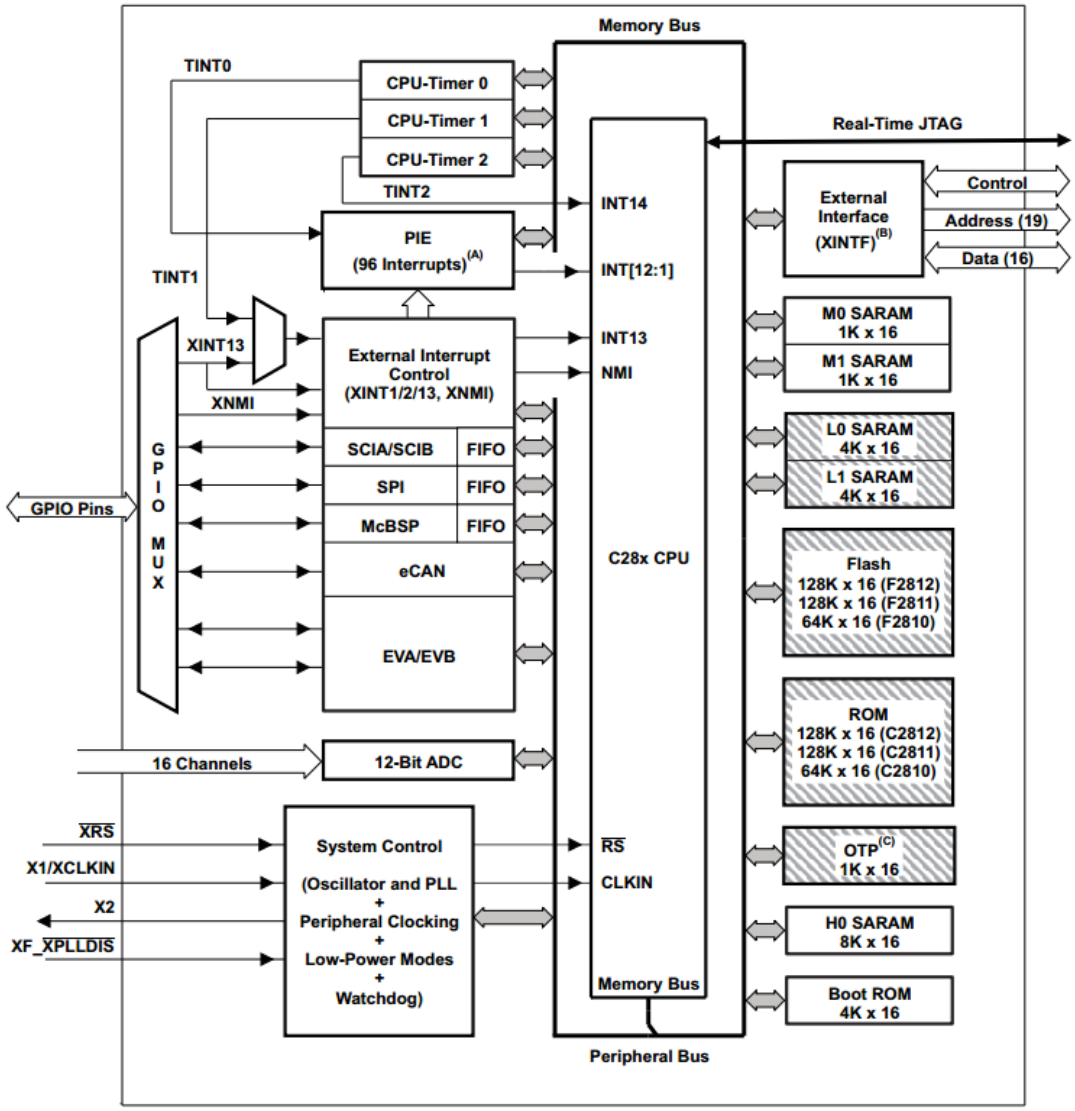


Figure 6.3: Functional block diagram of of eZdsp ^{TM} F2812 board kit

The Event Manager (EVA/EVB) module as shown in Figure 6.4 includes the general-purpose (GP) timers and full-compare / PWM unit. The Event Manager Module generates the PWM transition signal. Asymmetric and symmetric waveform generator and the related output logic control the transition signal. The asymmetric and symmetric waveform generator is based on the GP-timer. The related output logic control is active high, active low, forced high and forced low.

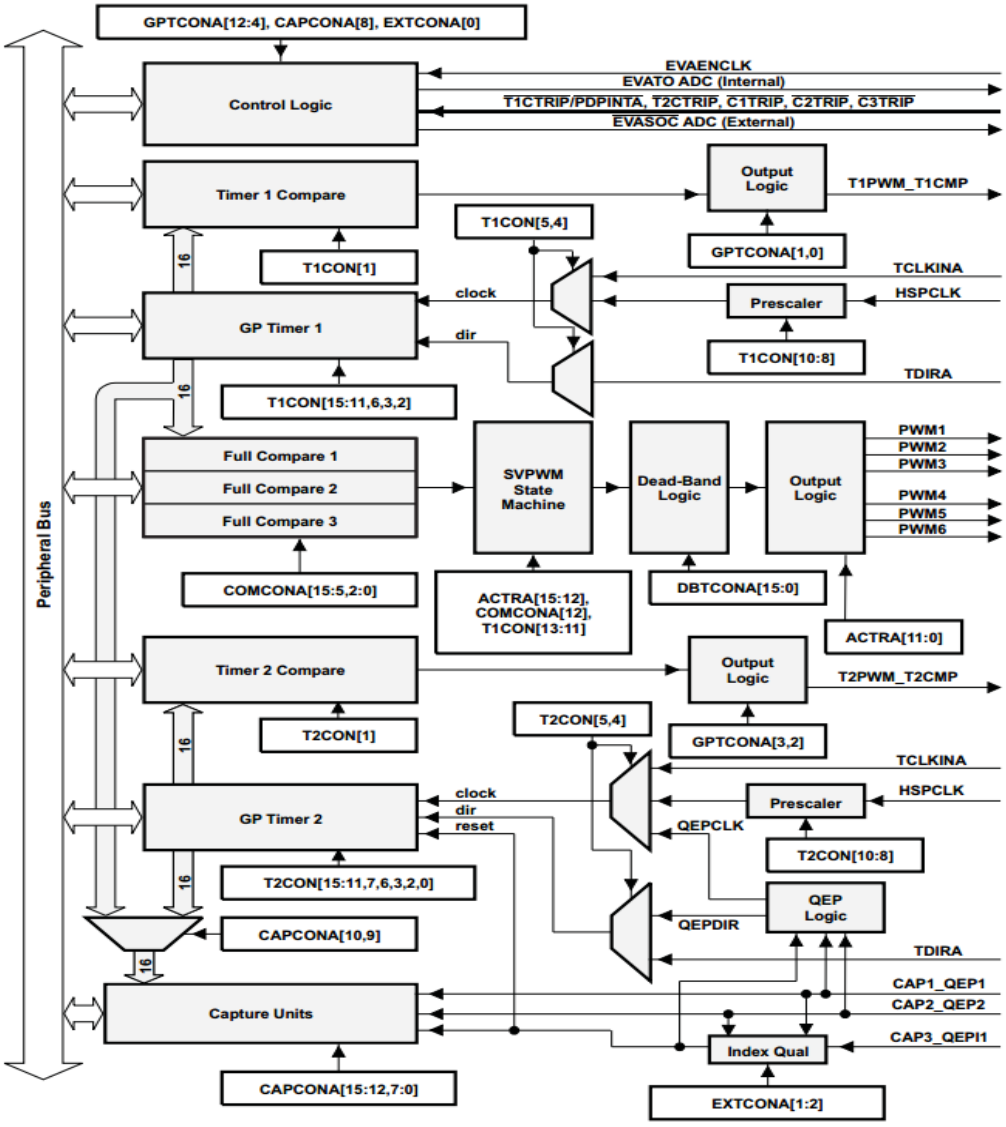


Figure 6.4: Block diagram of eZdsp ^{TM} F2812 board kit (Texas Instrument)

6.3 Experimental Results

6.3.1 Non-Isolated DC-DC Boost Converter

The various non-isolated DC-DC boost converter parameter values are shown in Table 6.1. The selection of these value is based on the continues current mode (CCM) condition. The cascaded boost converter and three-level boost converter have two switches (S_1 & S_2). The capacitance value of both converters is much higher compared to other converters.

Comparison between different types of non-isolated step-up DC-DC boost converters have been demonstrated. The various converters consist of conventional boost converter, cascade boost converter, inverting zeta-derived boost converter, cuk-derived boost (CD-Boost) converter and modified boost converter. The various non-isolated DC-DC boost converter prototype topologies are designed for 360 W and the duty cycle value is 0.7. The performance of each converter, determined from parameters such as the conversion voltage ratio and switch voltage stress are verified with the experiment results.

Table 6.1: Experiment parameter values of various DC-DC converters

Parameters	**Values**
Output Voltage, V_o	350 Vdc
L_1, L_2 (all DC-DC boost converter topologies)	1 mH
C_o (conventional boost converter)	270 uF
$C_{o1,}$ C_{o2} (cascade boost converter)	2200 uF
$C_{o1,}$ C_{o2} (three-level boost converter)	3200 uF
C_o (CD-Boost converter)	270 uF
C_o (inverting zeta derived boost converter)	270 uF
$C_{1,}$ C_2 (modified boost converter)	10 uF

Figure 6.5 shows the PWM of IGBT for the conventional boost, cascade boost, inverting zeta derived DC-DC boost, three-level boost converter CD-Boost and modified boost converters. For the cascade boost converter, both switches (S_a & S_b) are switched at same time. The PWM pattern for the three-level DC-DC boost is shown in Figure 6.6, where the switching of S_a and S_b are generated when ($V_i < V_o / 2$) .

The input voltage (60 V_i), output voltage (200 V_{dc}) and the switch voltage stress (V_s) for a conventional boost converter and modified boost converter is shown in Figure

6.7. It is shows that, the voltage stress of the switch is the same with the output boost voltage ($V_s = V_{dc}$).

Figure 6.5: PWM for conventional boost converter, cascade boost converter, inverting zeta derived boost converter, CD-Boost converter and modified boost converter

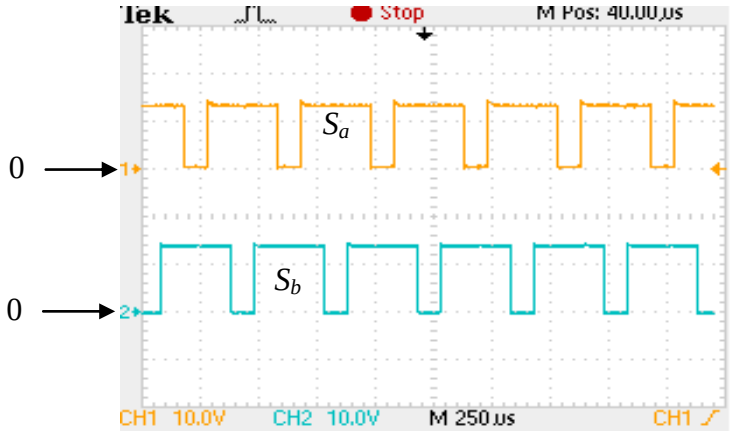


Figure 6.6: Three-level boost converter PWM pattern

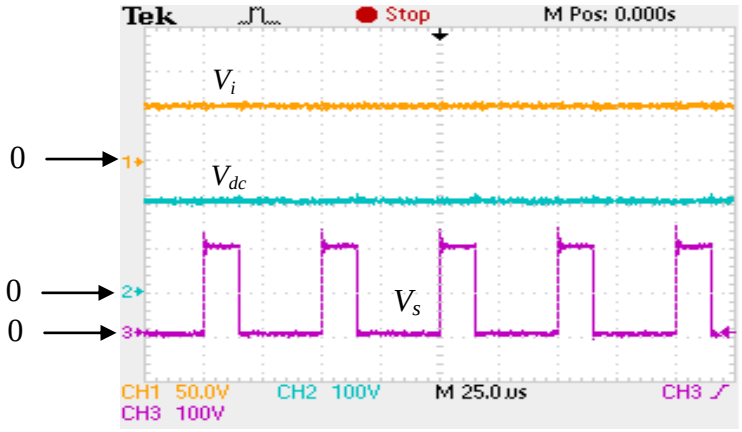


Figure 6.7: Voltage input, (V_i) voltage output (V_{dc}) and switch voltage stress (V_s) for conventional boost and modified boost converter

The input, output and switches (S_a & S_b) voltages of the cascade boost converter are presented in Figure 6.8. For that converter, the input voltage at the first stage is 18 V and the output voltage is 60 V (V_{dc1}). Then, the output voltage (V_{dc1}) is boosted to the second stage of the converter to 200 V. As seen in Figure 6.8, the switch voltage of stage 1 (V_{Sa}) is the same with V_i. The switch voltage of stage 2 (V_{Sb}) is the same with V_{dc}.

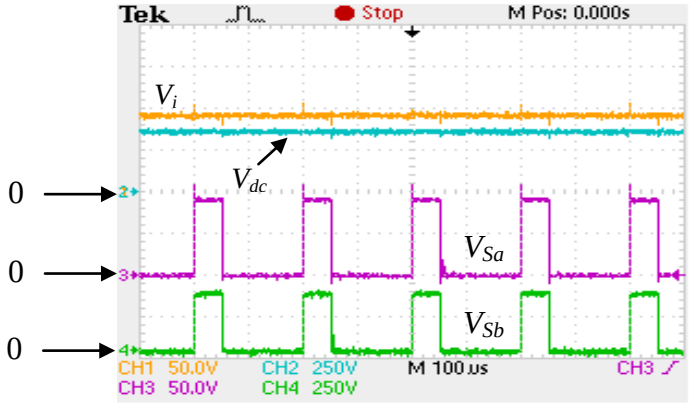


Figure 6.8: Voltage input (V_i), voltage output (V_{dc}) and switch voltages stress (V_{Sa} &V_{Sb}) of cascade boost converter

Figure 6.9 shows the experimental results of a three-level boost converter, which includes the voltage input (V_i), voltage output (V_{dc}) and switch voltage (V_s). It is observed that the voltage stress of the IGBT device is half of the output voltage (V_{dc}). Therefore, the rating of the IGBT device can use half of the conventional boost converter's rating.

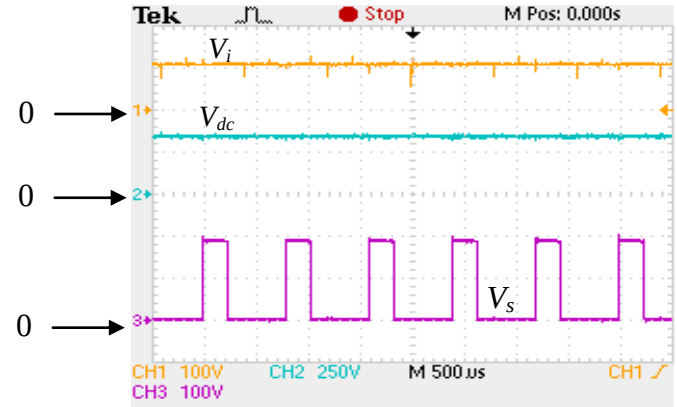


Figure 6.9: Voltage input (V_i), voltage output (V_{dc}) and switch voltage stress (V_s) of three-level converter

The voltage input (V_i), voltage output (V_{dc}) and switch voltage (V_s) of an inverting zeta-derived boost converter is plotted in Figure 6.10.

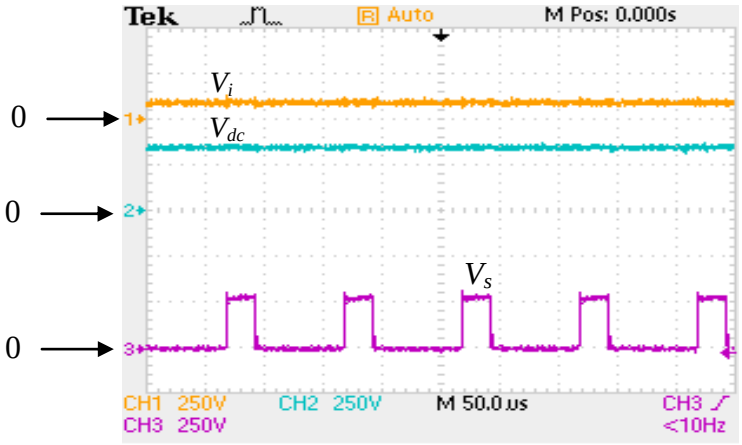


Figure 6.10: Voltage input (V_i), voltage output (V_{dc}) and switch voltage stress (V_s) of inverting zeta derived boost converter

In Figure 6.10, channel 1 represents the voltage input (V_i) while channel 2 and 3 represent the voltage output (V_{dc}) and voltage (V_s) of switch respectively. The ratio between the voltage of the switch (channel 3) and voltage output (channel 2) is validated approximately using (3.57).

The prototype of the CD-Boost converter has been tested. The input voltage (V_i), output voltage (V_{dc}) and switch voltage (V_s) is indicated in Figure 6.11. In this figure, the switch voltage stress reduced approximately half of the output voltage. Therefore, this converter has the option of using a low-voltage-rated IGBT device in order to reduce the conduction loss of the switch

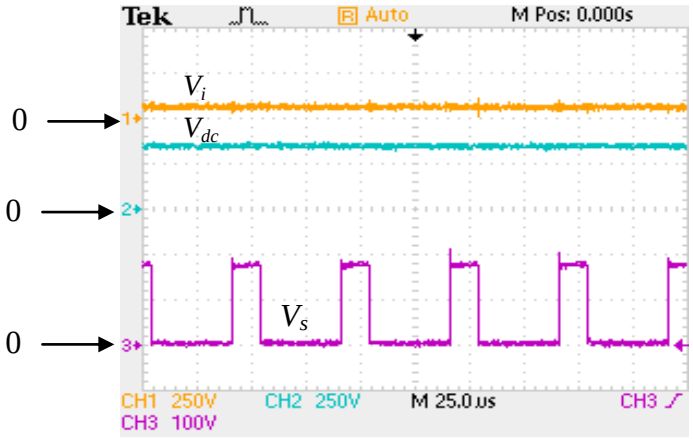


Figure 6.11: Voltage input (V_i), voltage output (V_{dc}) and switch voltage stress (V_s) of CD-Boost converter

6.3.2 Ripple of Input DC Current

The different types DC-DC boost converter are analysed in term of ripple input dc current. The circuit of different types DC-DC boost converters have been developed and tested with the same input voltage (45 Vdc). The performance of the converter according to ripple input current is represented in Figure 6.12, Figure 6.13, Figure 6.14, Figure 6.15, Figure 6.16 and Figure 6.17. The input dc current ($\Delta I_{i\ ripple}$) peak-to-peak ripple is generated in the different type DC-DC boost converters compared to the proposed modified converter as shown in Figure 6.17. The input current ($\Delta I_{iripple}$) peak-to-peak ripple is smoothed out by the two series-connected inductors (L_1 + L_2) in the input. For other converters, the input current is switched.

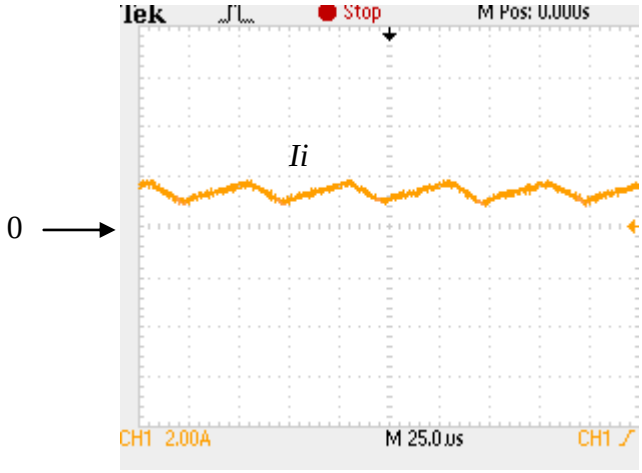


Figure 6.12: Input current (*Ii*) waveform of conventional boost converter

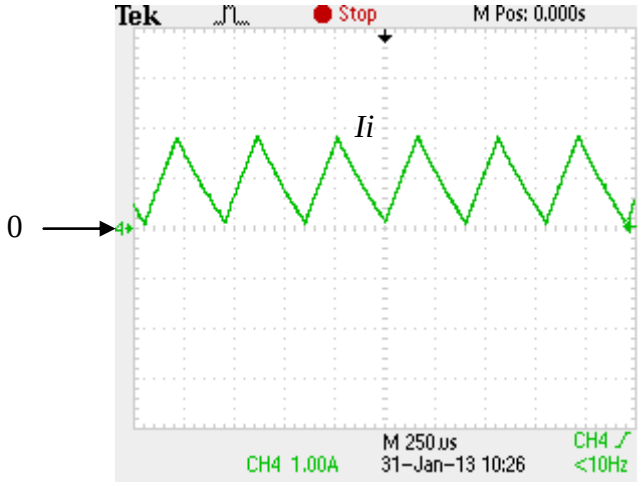


Figure 6.13: Input current (*Ii*) waveform of three-level boost converter

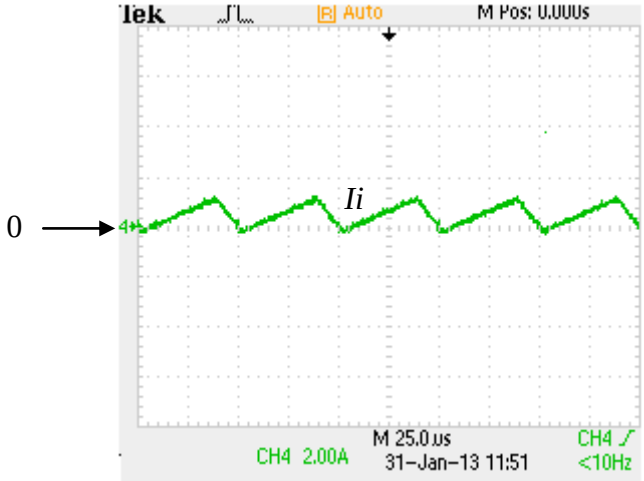


Figure 6.14: Input current (*Ii*) waveform of CD-Boost converter

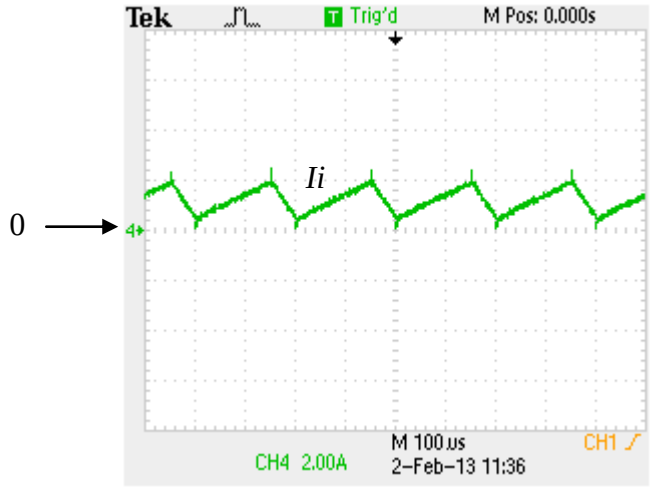


Figure 6.15: Input current (*Ii*) waveform of inverting zeta derived boost converter

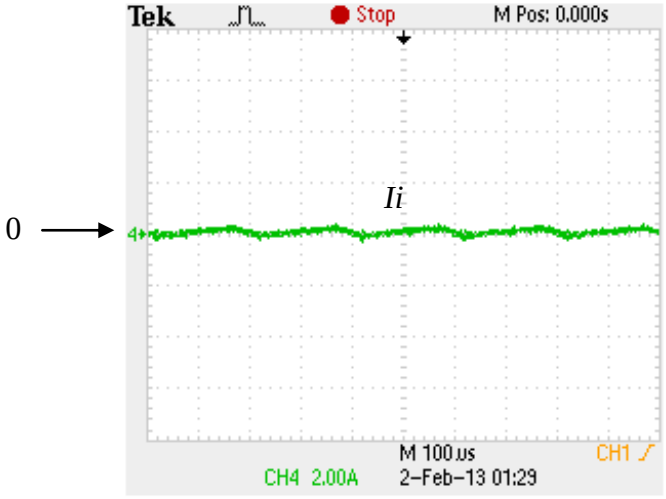


Figure 6.16: Input current (*Ii*) waveform of cascade boost converter

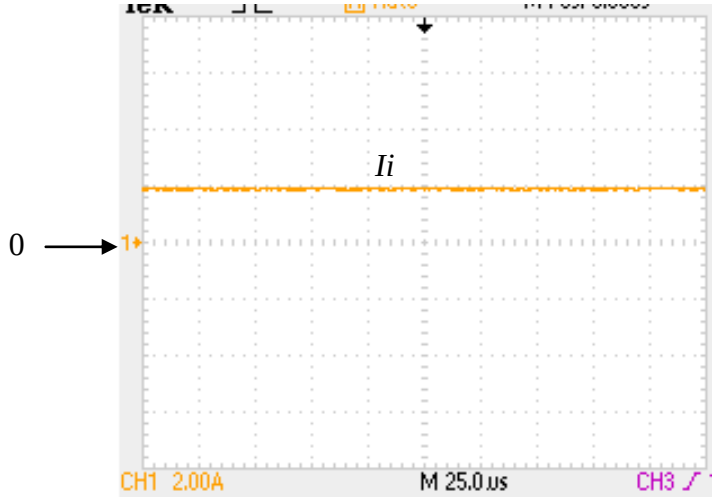


Figure 6.17: Input current (*Ii*) waveform of proposed modified boost converter

6.3.3 Comparison for Various Non-Isolated DC-DC Boost Converter

The conversion voltage ratio against the duty cycle and normalized switch obtained by various DC-DC converter configurations discussed above are compared in Figures 6.18 and 6.19. In Figure 6.18, the CD-Boost converter exhibits higher conversion ratio for $D > 0.7$ compared to other converters. In Figure 6.19, CD-Boost converter has the lowest normalized switch stress at $D = 0.7$ compared to other DC-DC converter configurations. The formulas of normalized switch stress of each converter have been discussed in section 3.3.2. The inverting zeta-derived converter produced negative normalized stress due to the high values of M, as the switch voltage stress approaches the output voltage.

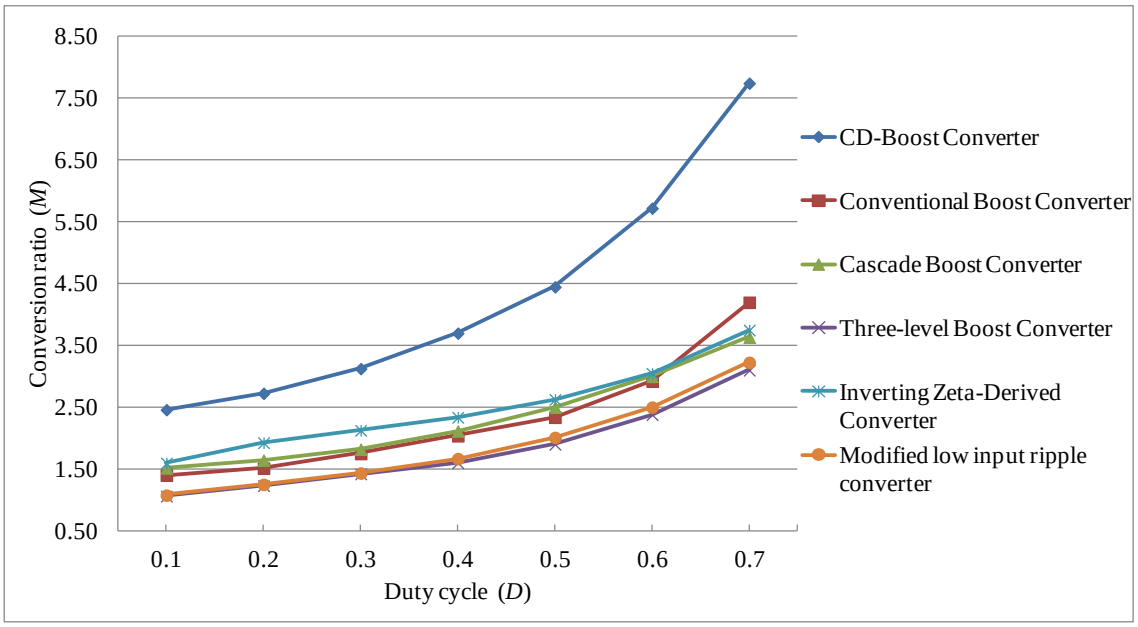


Figure 6.18: Conversion ratio gains of the various DC-DC converters

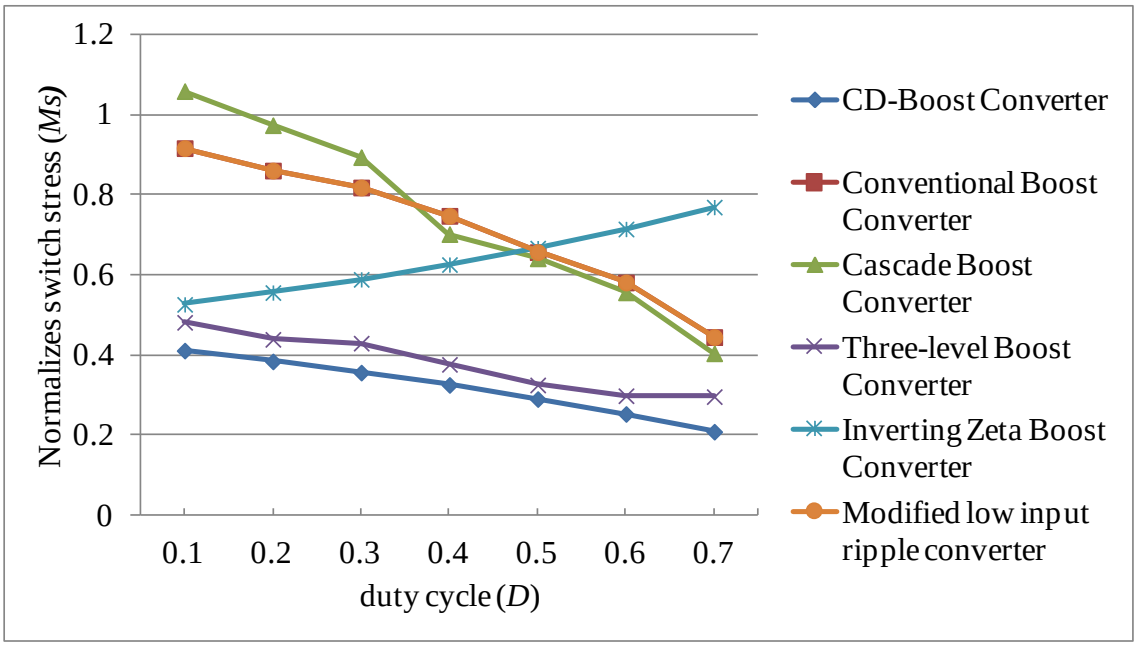


Figure 6.19: Normalized switch stresses of the various DC-DC converters

Figure 6.20 shows the measured efficiency of various DC-DC converters. From Figure 6.20, as expected, at 360 W, the modified boost converter has the highest efficiency of about 98% due to minimal input dc current ripple. However the modified boost converter has less conversion ratio voltage compare to CD-Boost converter. The conventional boost converter and CD-Boost converter are 1% less efficient compared to modified boost converter. The corresponding figures are 87% for inverting zeta derived boost converter, 91% for three-level boost converter and 80% for cascaded boost converter.

Table 6.2 presents the performance of the various DC-DC converters. The performances are analysed in term of conversion voltage ratio, voltage switch stress, and input dc current ripple.

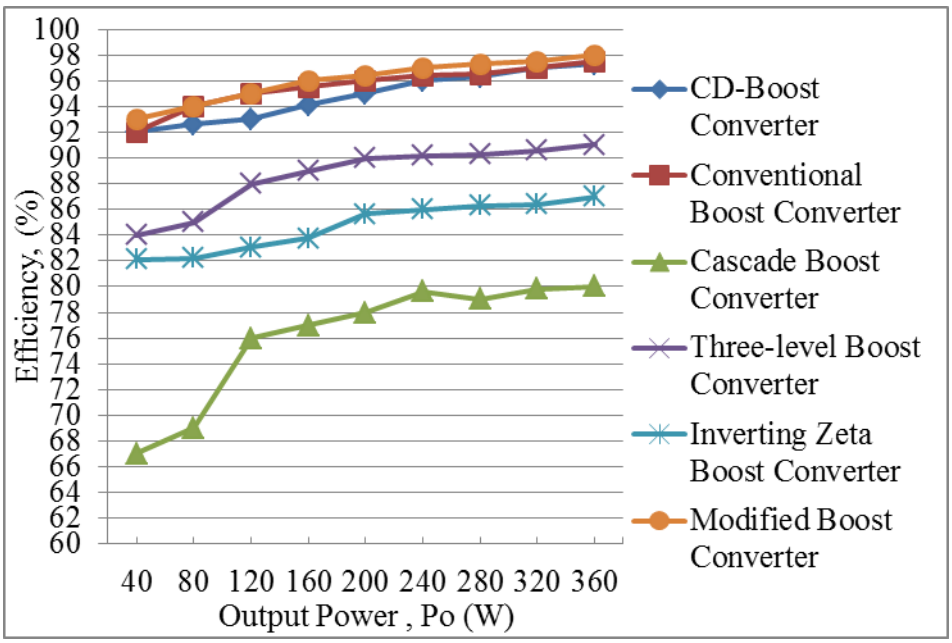


Figure 6.20: Efficiency of various converters

Table 6.2 Experimental data results of various DC-DC converters

DC converters	**Voltage gain ratio (*M*)**	**Voltage switch stress (M_s)**	**$\Delta I_{i\ \text{ripple}}$**	**Integrate to H-Bridge inverter**
Conventional Boost Converter	$\frac{1}{1-D}$	Vo	0.8 A	no
Modified Boost Converter	$\frac{1}{1-D}$	Vo	≈ 0 A	yes
Three-level Boost Converter	$\frac{1}{1-D}$	$\frac{1}{2}$ Vo	1.6 A	no
Cascade Boost Converter	$\frac{1}{1-D}$	Vo	1.40 A	no
CD-Boost Converter	$\frac{2}{1-D}$	$\frac{1}{2}$ Vo	1.36 A	yes
Inverting Zeta Derived Boost Converter	$\frac{2-D}{1-D}$	$\frac{2}{1-D}$ Vo	1.2 A	no

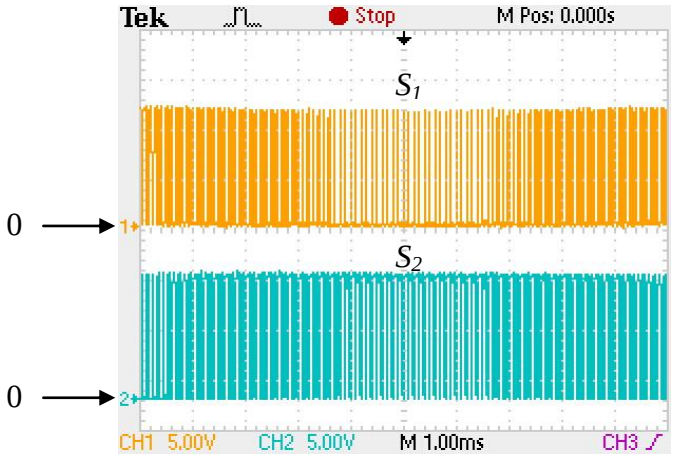
Due to ≈ 0 input dc current ripple and high efficiency of modified boost converter, that converter is integrated to H-Bridge inverter. The CD-Boost converter is also integrated to H-Bridge inverter due to advantage of high conversion voltage ratio and less switch voltage stress. The both converters are tested for transformerless module integrated grid-connected H-Bridge inverter system.

6.4 Experimental Results of Single-Stage H-Bridge Inverter Topologies

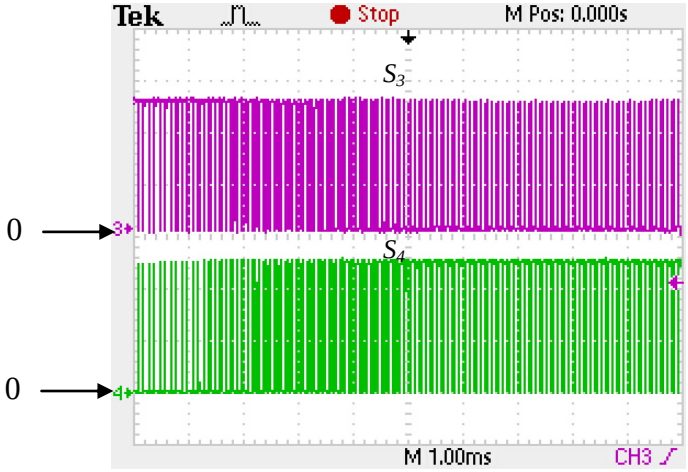
The single-stage of H-Bridge inverter topplogy with conventional unipolar and bipolar PWM techniques have been tested and analysed. The single-stage topologies have been tested with 400 *Vdc* input voltage. In this section the common-mode voltage and ground leakage current of conventional unipolar H-Bridge inverter, bipolar H-Bridge inverter, proposed SC-HB inverter and the recent HB-ZVR topology are examined.

6.4.1 Conventional Unipolar and Bipolar H-Bridge Inverter topology

The conventional unipolar and bipolar SPWM techniques have been tested using the single-phase H-Bridge topology. The switching pattern for unipolar SPWM technique is depicted in Figure 6.21. The three level output inverter voltage (V_{dc}, 0,$-V_{dc}$) when using conventional unipolar PWM strategy is illustrated in Figure 6.22. The variation of common-mode voltage and high level of ground leakage current are shown in Figure 6.23. Figure 6.24 shows the detailed spectrum of common-mode voltage, which is generated at a high amplitude switching frequency (f_s). Due to high ground leakage current level, the ac current waveform of conventional unipolar techniques is distorted as shown in Figure 6.25. The current THD of conventional unipolar H-Bridge is given as 4.4% as shown in Figure 6.26.



(a)



(b)

Figure 6.21: PWM pattern of conventional unipolar techniques (a) S_1&S_2, (b) S_3&S_4

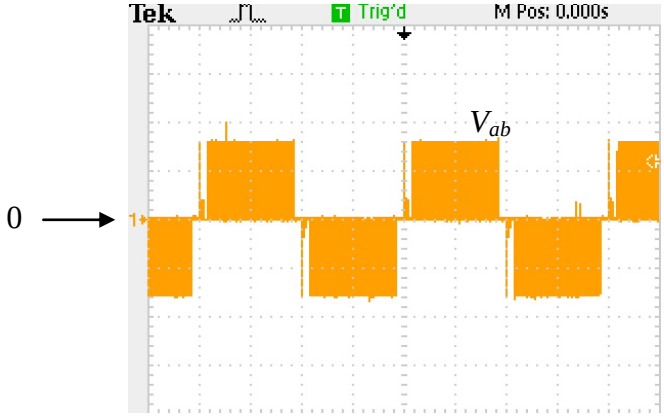


Figure 6.22: Output inverter voltage (V_{ab}) (Channel 1, 250 V/div, t: 5 ms/div)

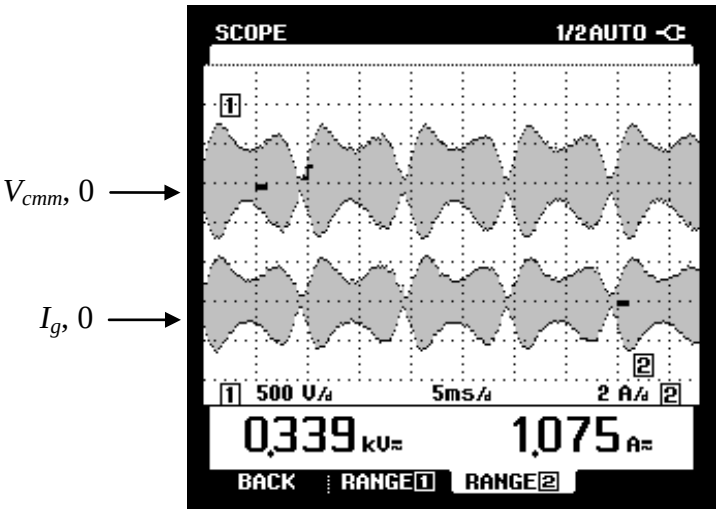


Figure 6.23: Common-mode voltage (V_{cmm}, channel 1) and ground leakage current (I_g, channel 2) for conventional unipolar PWM technique (measured by Fluke 434 Power Quality Analyzer)

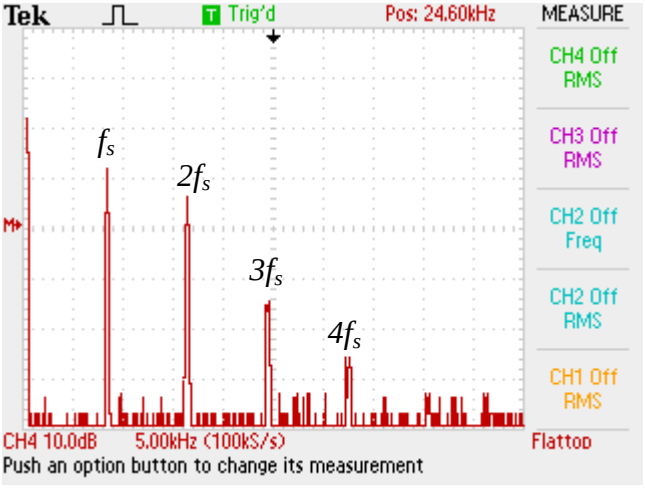


Figure 6.24: FFT of Common mode voltage for conventional unipolar H-Bridge inverter

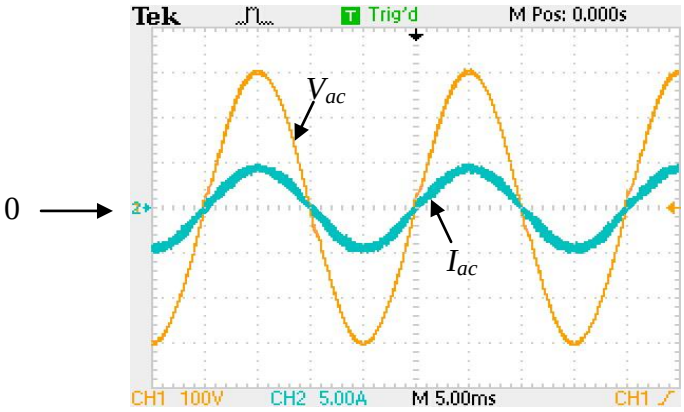


Figure 6.25: AC waveform of conventional unipolar H-Bridge inverter

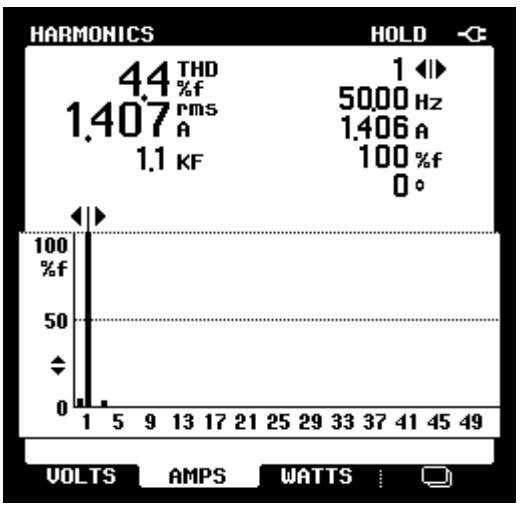
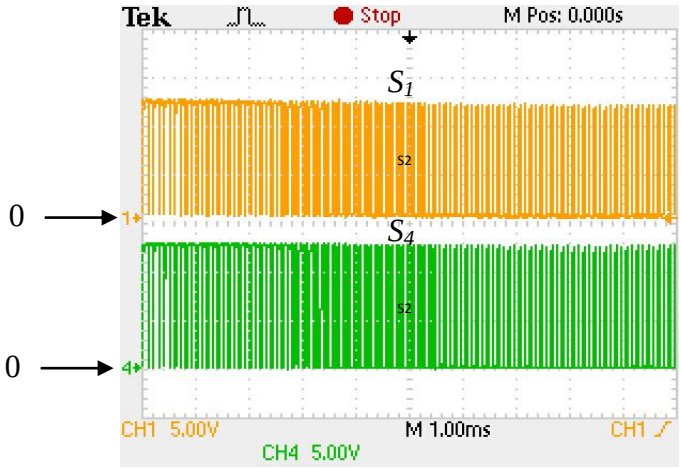


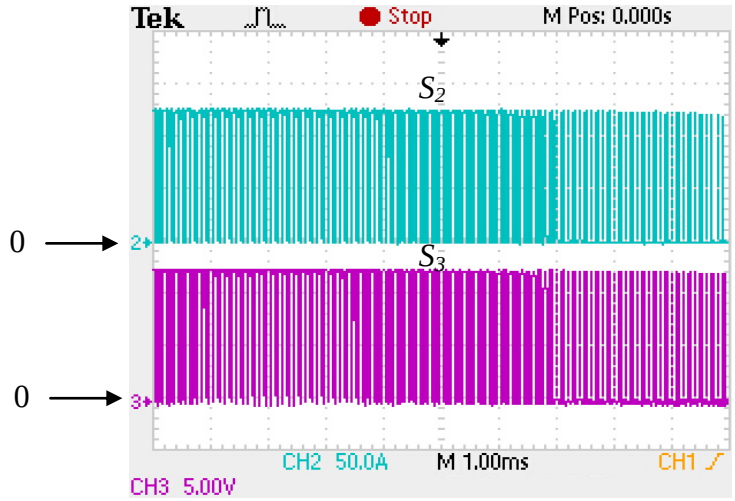
Figure 6.26: THD ac current for conventional unipolar H-Bridge inverter

The switching pattern of the bipolar SPWM technique is depicted in Figure 6.27. The inverter output voltage (V_{dc} & $-V_{dc}$) is shown in Figure 6.28. To maintain the filter value as is used in unipolar H-Bridge inverter technique, the switching frequency is

double the frequency of the unipolar SPWM. The grid waveforms for bipolar SPWM are given in Figure 6.29. Due to the behaviour of the bipolar switching pattern, the common-mode voltage is constant with a small amount of ground leakage current as shown in Figure 6.30. The high amplitude of common-mode voltage does not appear at switching frequency as shown in Figure 6.31. Figure 6.32 shows, that the current THD of bipolar H-Bridge inverter is 3.0 %.



(a)



(b)

Figure 6.27: Bipolar H-Bridge inverter switching pattern; (a): S_1& S_4,(b): S_2 & S_3

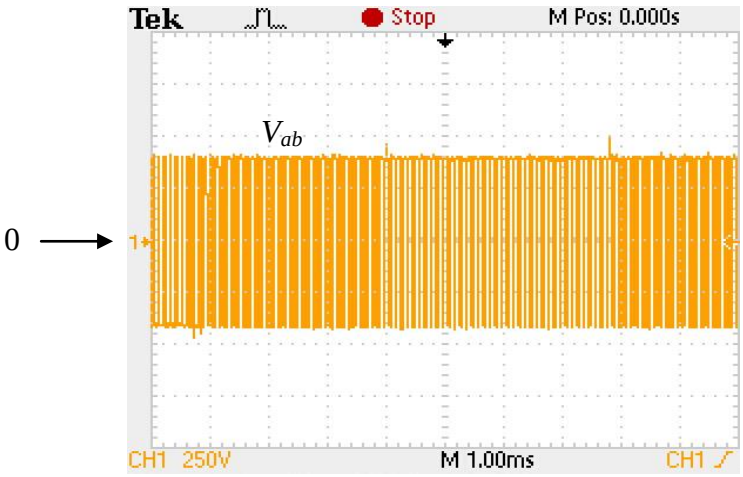


Figure 6.28: Output inverter (V_{ab}) (for bipolar H-Bridge inverter)

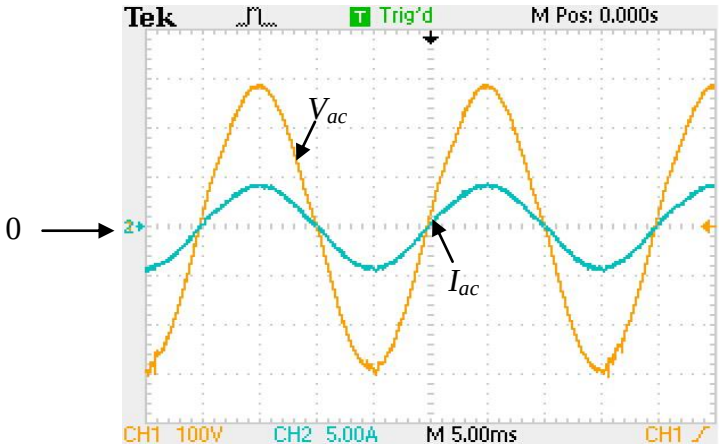


Figure 6.29: AC waveforms for bipolar H-Bridge inverter

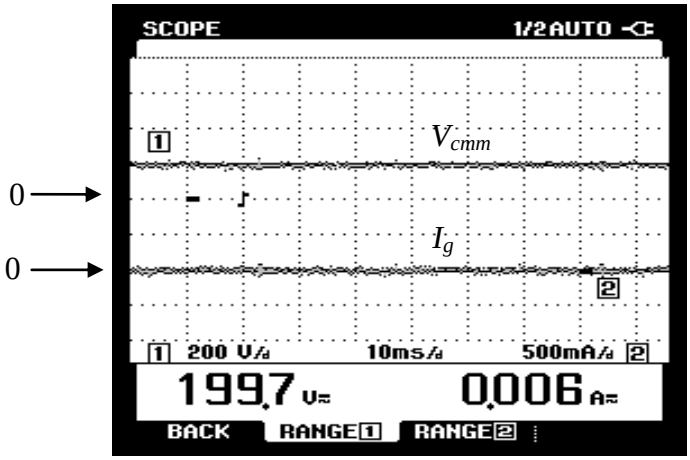


Figure 6.30: Common-mode voltage (V_{cmm}, channel 1) and ground leakage current (I_g, channel 2) for bipolar H-Bridge inverter (measured by Fluke 434 Power Quality Analyzer)

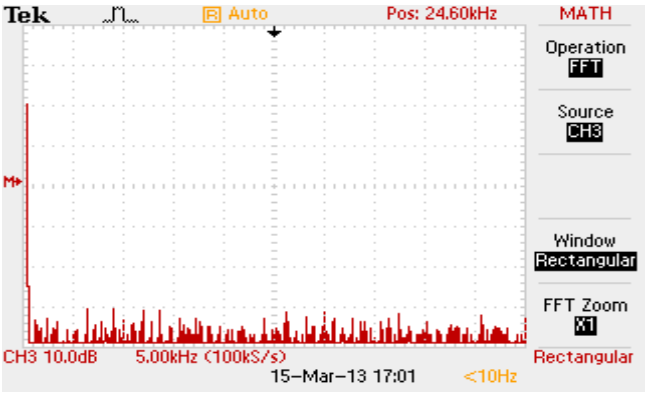


Figure 6.31: FFT of Common mode voltage for conventional bipolar H-Bridge inverter

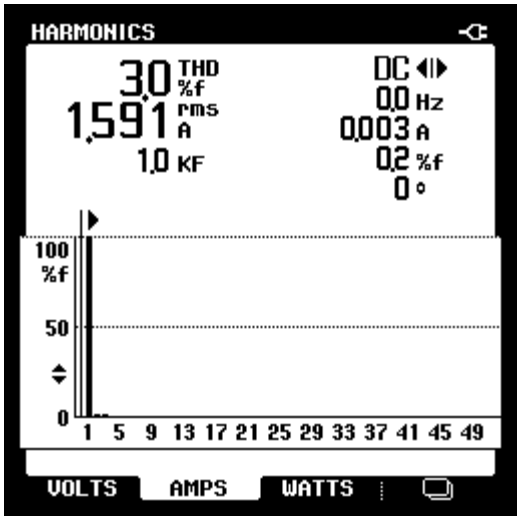


Figure 6.32: THD current for bipolar H-Bridge inverter (measured by Fluke 434 Power Quality Analyzer)

6.4.2 Effect of Filter Impedance Matching and Parasitic Capacitance to Ground Leakage Current in Bipolar H-Bridge Inverter

Due to low ground leakage current of bipolar H-Bridge inverter as shown in Figure 6.29 compared to conventional unipolar H-Bridge inverter as shown in Figure 6.23, the effect of filter impedance matching and parasitic capacitance has been analysed. On the effect of impedance mismatch between L_{f1} & L_{f1n} and L_{f2} & L_{f2n}, Figure 6.33 shows that a very high (> 300 mA) ground leakage current was produced when the filter impedance matching is not matched. Figure 6.34 shows a detailed spectrum of the ground leakage current with very high harmonic contents for matchless filter impedance.

Table 6.3 describes the inductance matching (L_r) at inverter grid side. The ground leakage current level varies according to the ratio of inductance impedance matching (L_r) (see Figure 6.35, where the lowest ground leakage current was recorded when L_{f1} & L_{f1n} and L_{f1} & L_{f1n} are matched, i.e., L_r = 1). Therefore, impedance matching is recommended in transformerless grid-connected PV systems. The parasitic capacitance reaches significant value in wet environment e.g. 10-100 nF/kWp (Kerekes, 2009). Therefore, in this work, the parasitic capacitance (C_{pv}) value affects the ground leakage current level has been analysed. Figure 6.36 shows the ground leakage current increases as parasitic capacitance increases.

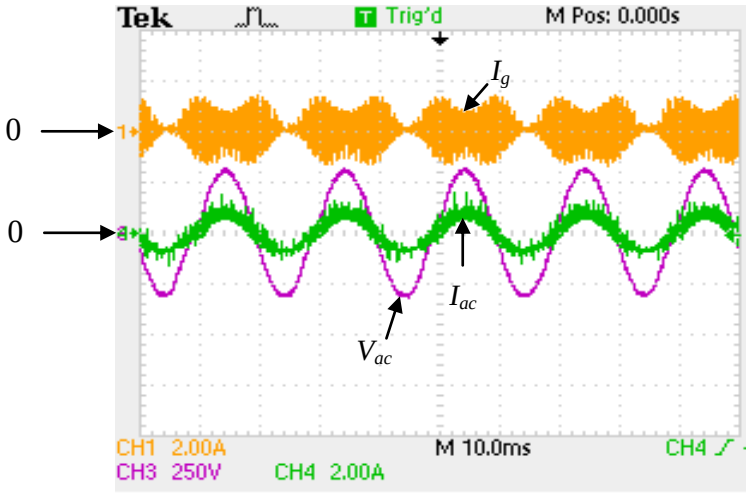


Figure 6.33: The effect of filter impedance mismatch on ground leakage current levels and ac waveforms

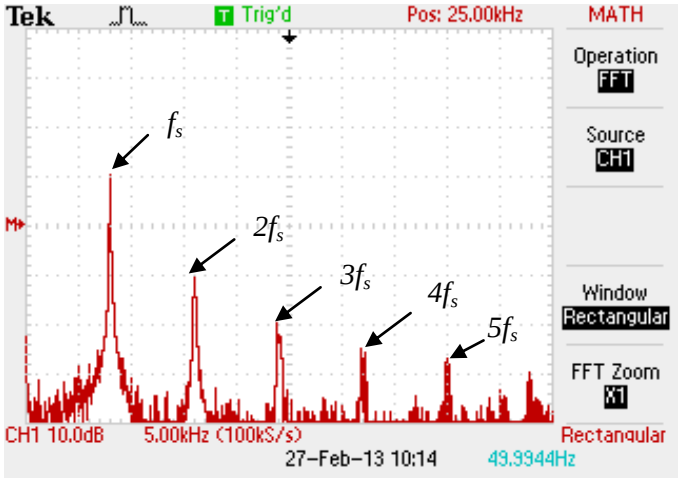


Figure 6.34: The ground-leakage current (500 mA/div) spectrum when the impedances mismatched

Table 6.3: The matching value of impedances (L_r)

L_{f1} (mH)	L_{f2} (mH)	L_{f1n} (mH)	L_{f2n} (mH)	$L_r = \frac{(L_{f1}+L_{f2})}{(L_{f1n}+L_{f2n})}$
3	2	3	2	1
4	2	2	2	1.5
4	3	1	2	2.3
4	4	1	1	4
5	4	0.5	0.5	9

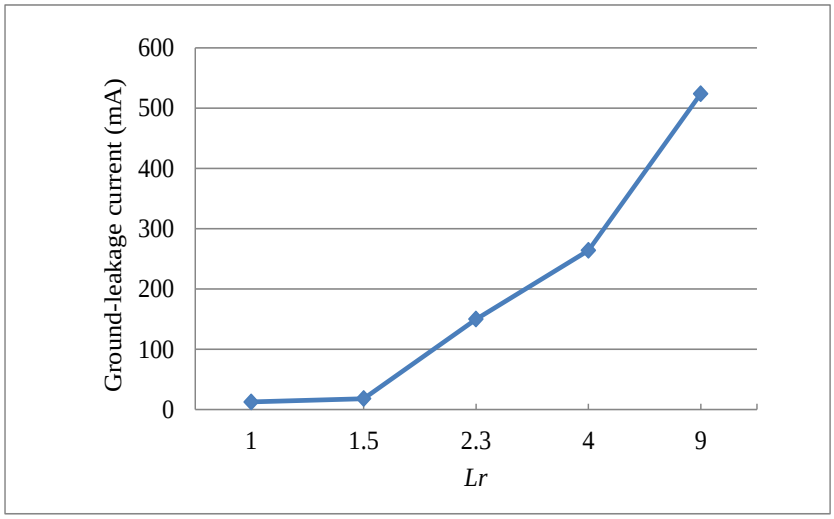


Figure 6.35: Ground leakage current levels against filter ratio values L_r (L_{f1} / L_{f1n} & (L_{f2}>L_{f2n})

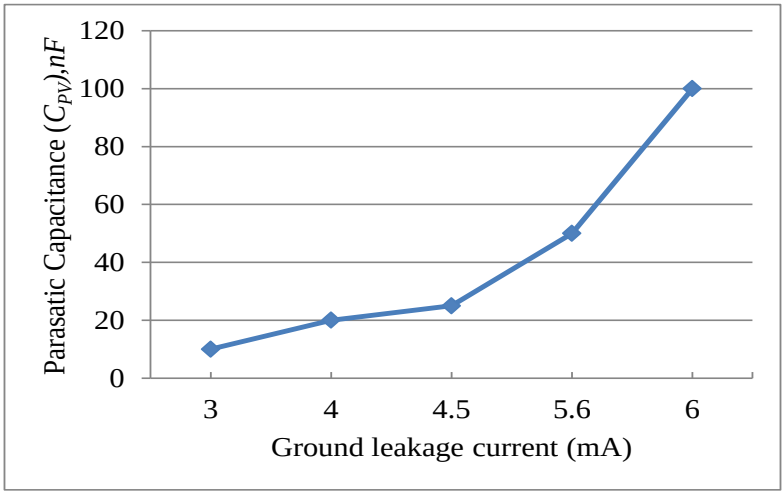


Figure 6.36: Parasitic capacitance vs. ground leakage current

6.4.3 HB-ZVR Inverter Topology

The existing HB-ZVR topology has been developed and tested in this work since it generate low ground leakage current, high efficiency and the direction of load current is not predefined (Kerekes, T. et al., 2011). The switching pattern for the HB-ZVR topology is depicted in Figure 6.37. The voltage and current of ac output waveform is illustrated in Figure 6.38. Figure 6.39 shows THD current of HB-ZVR topology. The constant common-mode voltage and low ground leakage current is shown in Figure 6.40. Figure 6.41 shows that high amplitude of common-mode voltage is not generated at the switching frequency. The main disadvantage of HB-ZVR topology is the balancing problem of series dc-link capacitors (C_{dc1} & C_{dc2}) as shown in Figure 6.42.

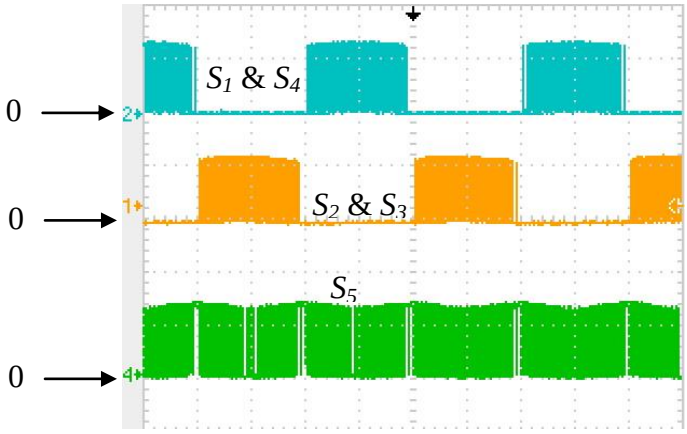


Figure 6.37: Switching pattern for HB-ZVR topology

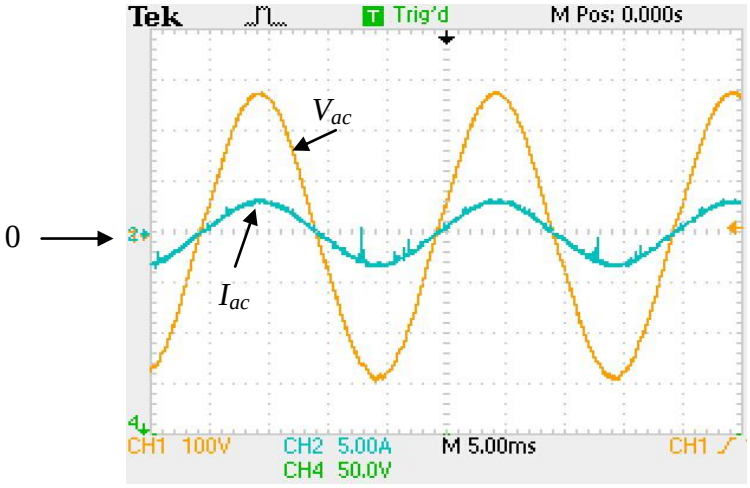


Figure 6.38: AC waveform for HB-ZVR topology

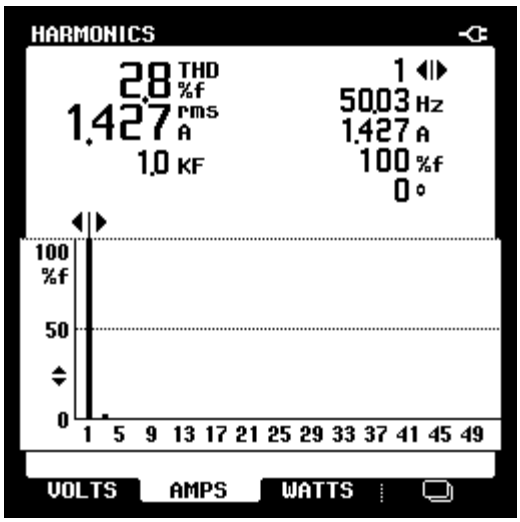


Figure 6.39: THD ac current for HB-ZVR topology

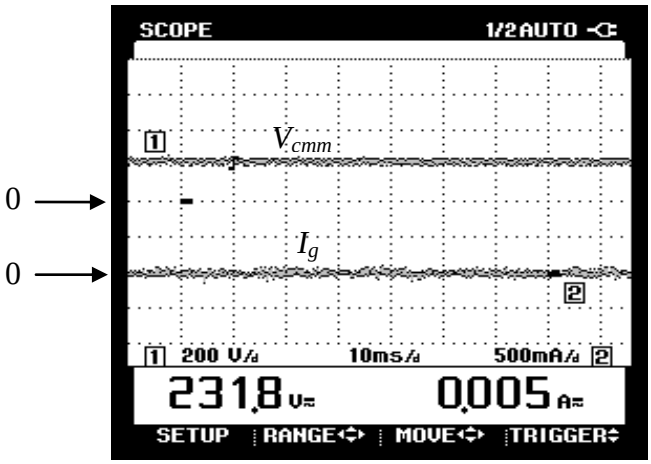


Figure 6.40: Common-mode voltage and ground leakage current for HB-ZVR topology (Measured by Fluke 434 power Quality Analyzer)

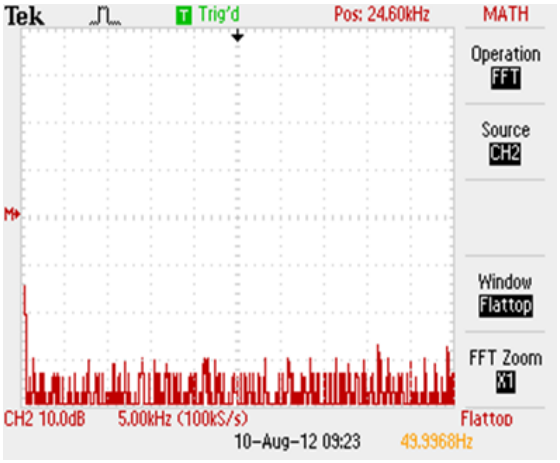


Figure 6.41: FFT of common-mode voltage of HB-ZVR topology

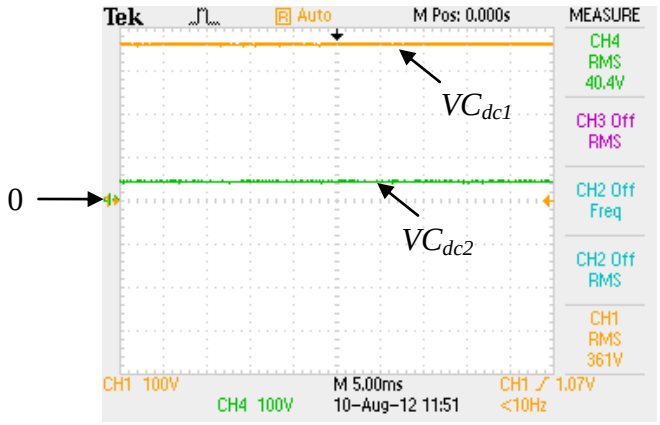


Figure 6.42 : Series dc-link capacitor voltages (VC_{dc1} & VC_{dc2}) of HB-ZVR topology

6.4.4 Proposed SC-HB Inverter Topology

In the proposed SC-HB inverter topology, the balancing of series dc-link capacitor voltage is controlling by the switching technique of a swithes (S_{B1} & S_{B2}) is shown in Figure 6.43. Figure 6.44 shows the experimental results for the series dc-link capacitor voltage balancing. The capacitor voltages are initially balanced, i.e. $VC_{B1} = VC_{B2} = 200$ V. When operating without the balancing circuit, the dc-link voltages are found to drift apart as shown in Figure 6.44(a). This indicates that the inverter is not capable of providing self-balancing and the dc-link voltage balancing is necessary. With the use of dc-link voltage balancing control, the dc-link voltages $VC_{B1} = VC_{B2}$ at all times, as shown in Figure 6.44(b). This proves the effectiveness of the balancing circuit.

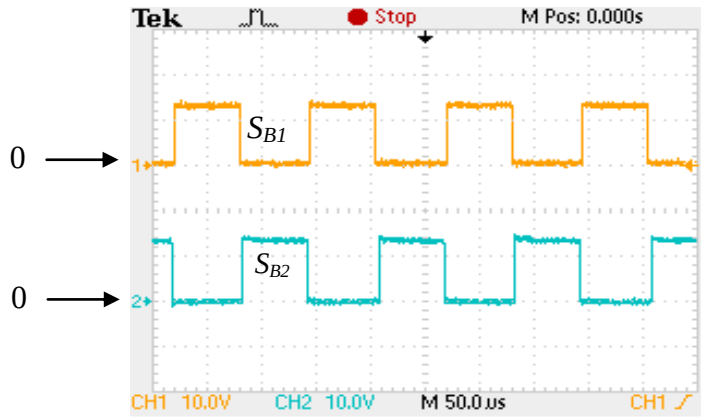


Figure 6.43: Switching pattern for balancing circuit

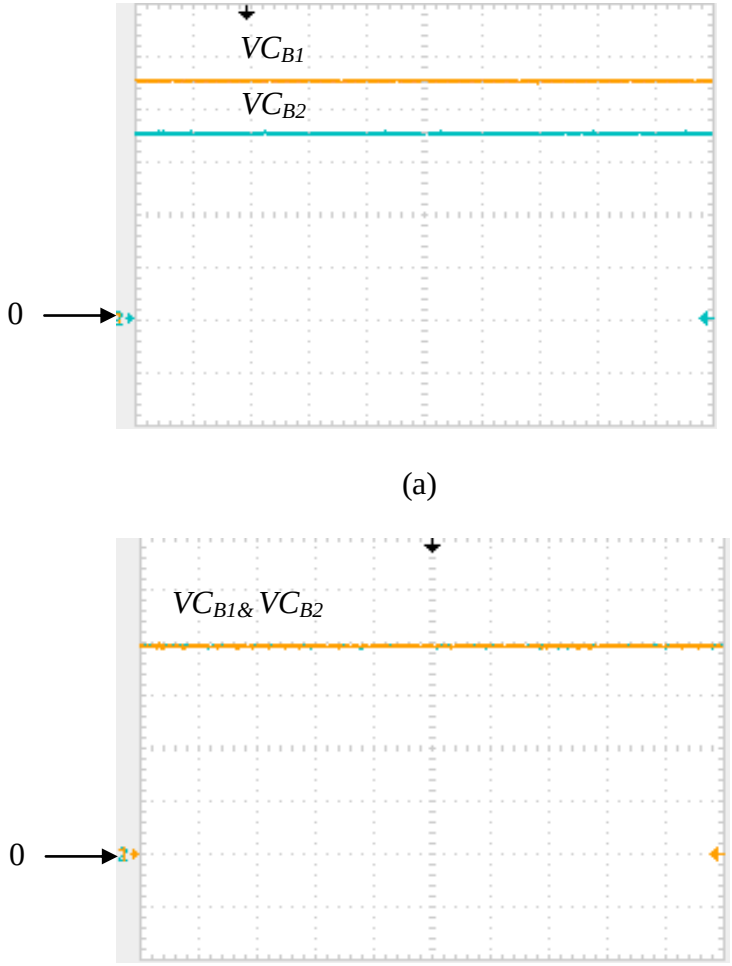


Figure 6.44: Series dc-link capacitors, (a) without balancing circuit, (b) with balancing circuit (vertical scale: 50 V/div; horizontal scale: 2.5 ms/div)

Figure 6.45 displays the constant common-mode voltage (V_{cmm}) and low ground leakage current (I_g) waveforms. The ground leakage current is found to be almost zero, confirming the performance of this topology in reducing leakage current. At high switching frequency, the high amplitude of common-mode voltage is not generated as shown in Figure 6.46. As seen in Figure 6.47, the ac voltage and current waveforms are sinusoidal. The results show that the ac voltage and current are in phase, operating at unity power factor. The THD value of ac current is analysed using Fluke 435 Power Analyzer with low grid current THD at 2.9%. This result can be seen in Figure 6.48.

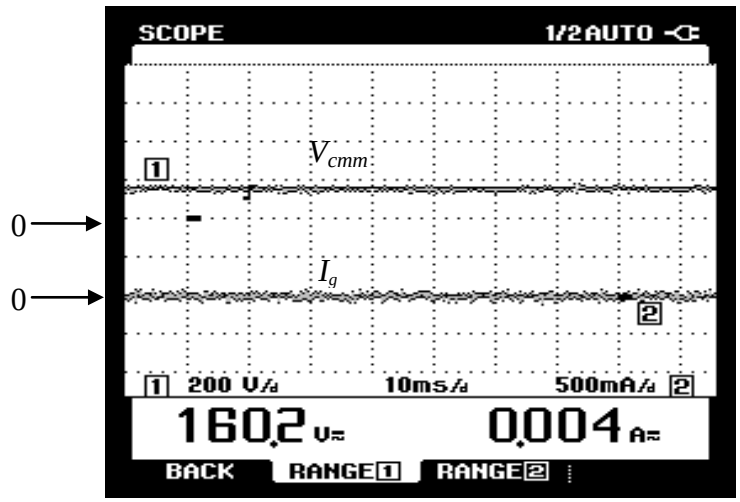


Figure 6.45: Common-mode voltage and ground leakage current of SC-HB topology (measured by Fluke 434 Power Quality Analyzer)

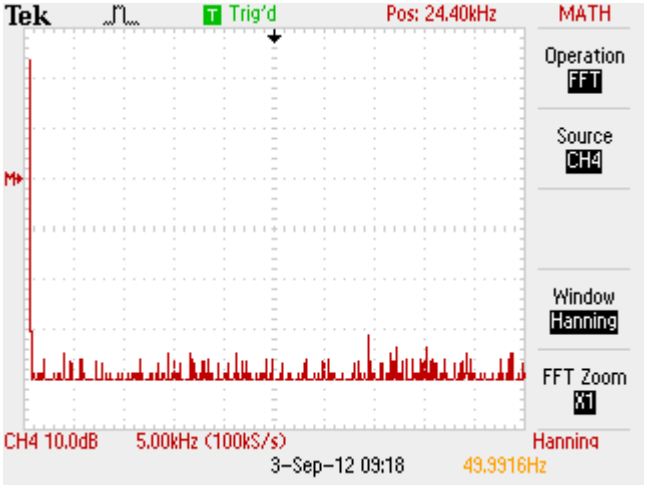


Figure 6.46: FFT of common-mode voltage for SC-HB inverter topology

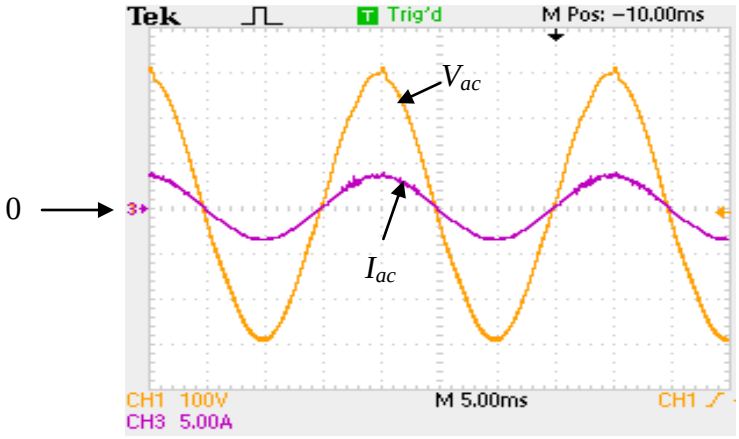


Figure 6.47: Grid waveforms; ac voltage (100V/div) and ac current (5A/div) for unipolar proposed SC-HB inverter topology

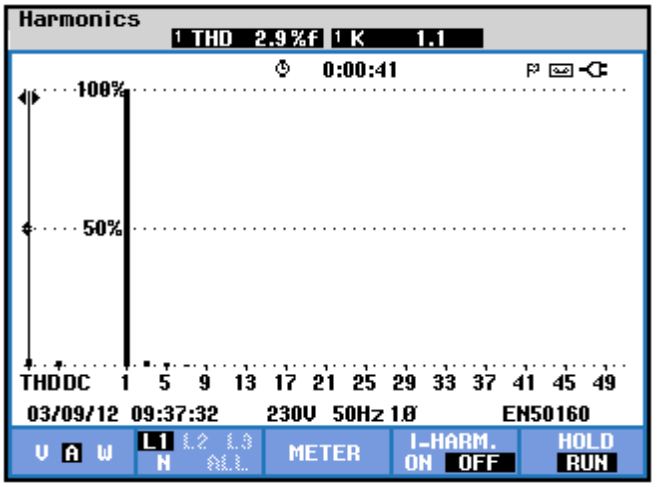


Figure 6.48: THD current for SC-HB topology converter (measured by Fluke 435 series II Power Quality and Energy)

6.5 Experiment Results of Proposed Two-Stage Inverter System

The lab-prototype hardware of the proposed two-stage inverters are tested in this section. The proposed two-stage inverter consists of bipolar H-Bridge inverter with CD-Boost converter, modified unipolar H-Bridge inverter with CD-Boost converter and modified unipolar H-Bridge inverter with modified boost converter. Common-mode voltage and ground leakage current are examined.

6.5.1 Proposed Bipolar H-Bridge Inverter with CD-Boost Converter

From previous Figures 6.7 and 6.11, by using same input voltage shows that the voltage conversion ratio (M) of the CD-Boost converter is higher ($M = V_{dc} / V_{in}$ = 400 V / 60 V = 6.7) than that of the conventional boost converter, which only has M = 200 V/ 60 V = 3.3 of the voltage conversion ratio respectively. In addition, the switch voltage stress V_s of the CD-Boost converter was found to be lower than the conventional converter, as shown in Figures 6.7 and 6.11 respectively. The V_s is equal to V_s = ½ x V_{dc} = 400 V/ 2 = 200 V for the CD-Boost converter and $V_s = V_{dc}$ = 200 V for the conventional boost converter. The CD-Boost converter topology is selected for the transformerless H-Bridge inverter topology as it has a high voltage conversion ratio (M)

and low switch voltage stress (V_s). The combination of both topologies is known as the bipolar H-Bridge inverter with CD-Boost converter.

The performance of proposed bipolar H-Bridge inverter with CD-Boost converter in term of common-mode voltage and ground leakage current are analysed. Figures 6.49 illustrate the common-mode voltage signals, indicate that the common-mode voltage is constant or in a dc form when the bipolar SPWM technique is used.

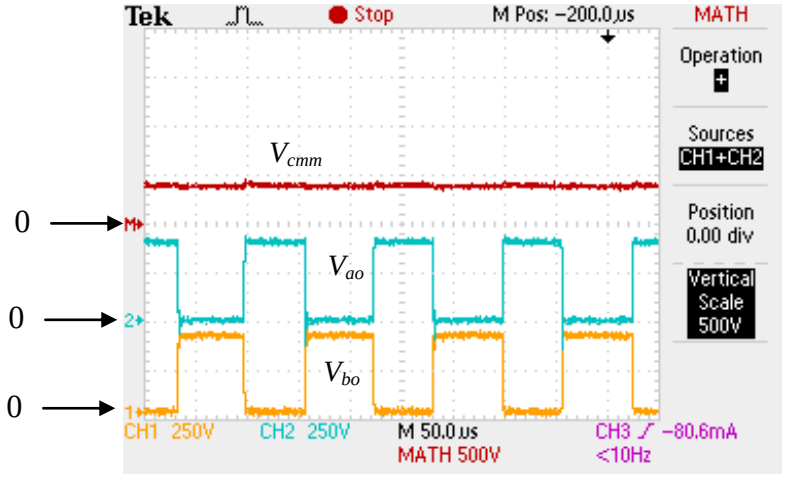


Figure 6.49: Common-mode voltage (V_{cmm}) obtained for bipolar H-Bridge inverter with CD-Boost converter

The common-mode voltage harmonics spectrum is shown in Figure 6.50 was measured using the Tektronix TDS2014C digital oscilloscope. From Figure 6.50, no high frequency harmonic components in the common-mode voltage are shown.

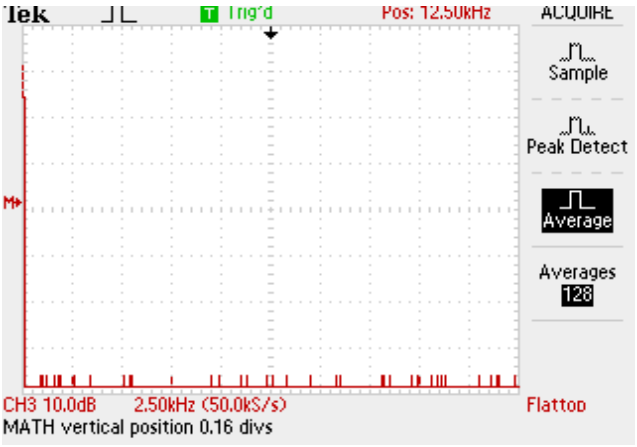


Figure 6.50: Harmonic spectrum of the common-mode voltage of bipolar H-Bridge inverter with CD-Boost converter

Figure 6.51 shows the ground leakage current and the ac waveform for the proposed bipolar H-Bridge inverter with CD-Boost converter. The ground leakage current is below 300 mA, which complies with the standard limit. Low ground leakage current means no significant current is flowing through the parasitic capacitance, thus producing a very smooth and sinusoidal grid current. Figure 6.52 shows that the high frequency harmonics of the ground leakage current for the proposed bipolar H-Bridge inverter with CD-Boost converter is minimised. The THD current of 3.4 % for the proposed bipolar H-Bridge inverter with CD-Boost converter is shown in Figure 6.53.

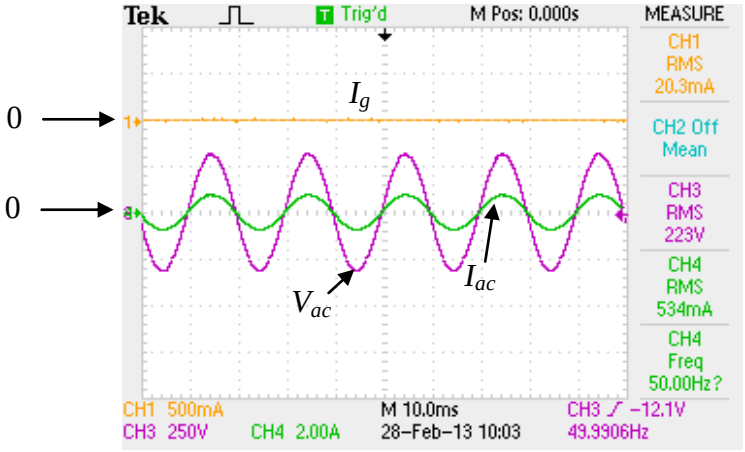


Figure 6.51: The ground leakage current, ac voltage, and ac current, of the bipolar H-Bridge inverter with CD-Boost converter

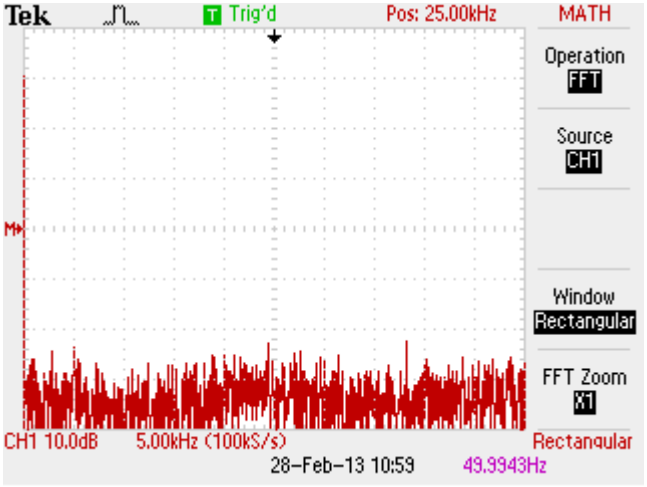


Figure 6.52: The ground leakage current (10 mA/div) spectrum of the bipolar H-Bridge inverter with CD-Boost converter

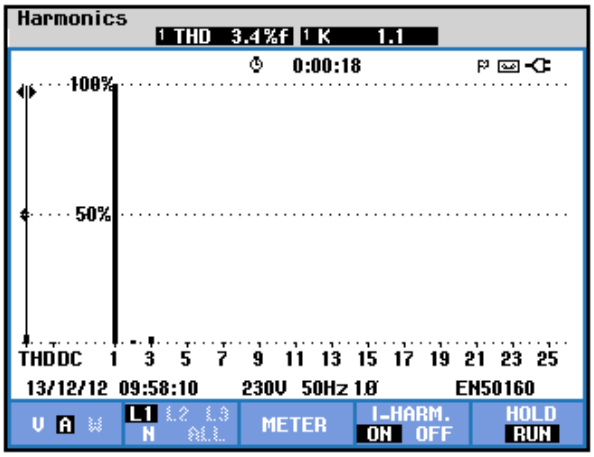
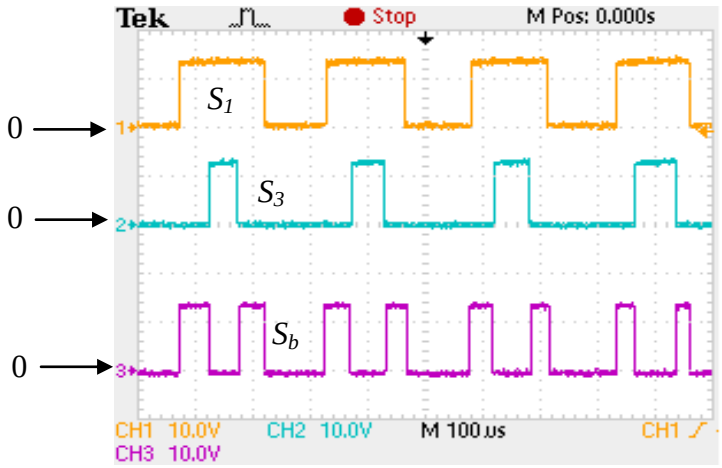


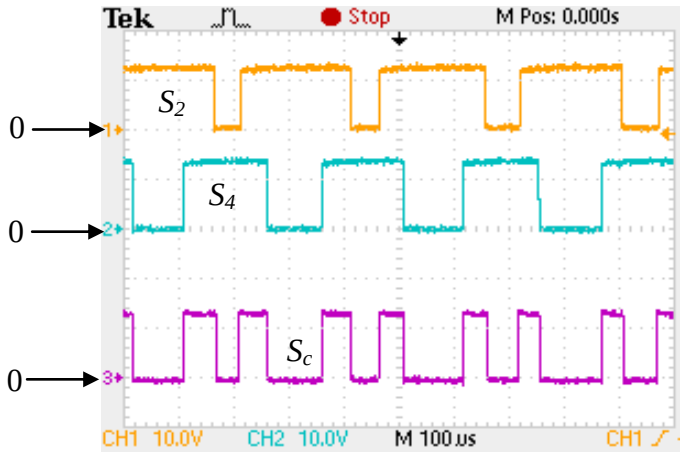
Figure 6.53: THD current for the bipolar H-Bridge inverter with CD-Boost converter (measured by Fluke 435 series II Power Quality and Energy)

6.5.2 Proposed Modified Unipolar H-Bridge Inverter with CD-Boost Converter

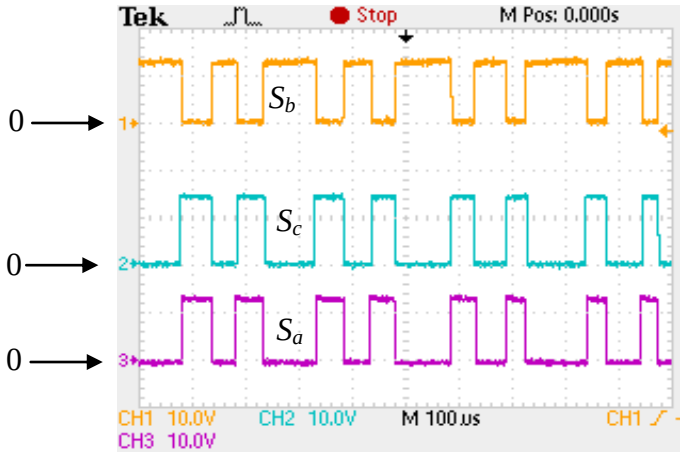
The switching pattern for the proposed modified unipolar H-Bridge inverter with CD-Boost converter topology is shown in Figure 6.54. Figure 6.55 shows the three-level output inverter, constant common-mode voltage and very low ground leakage current for the proposed topology.



(a)



(b)



(c)

Figure 6.54: Switching pattern for modified unipolar H-Bridge inverter with CD-Boost converter

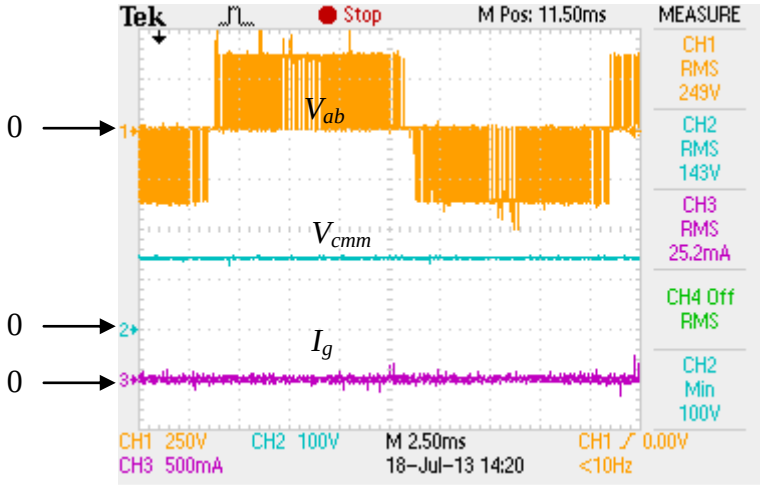


Figure 6.55: Output inverter (V_{ab}, channel 1), common-mode voltage (V_{cmm}, channel 2) and ground leakage current (I_g, channel 3) for modified unipolar H-Bridge inverter with CD-Boost converter

The ground leakage current spectrum result is displayed in Figure 6.56. The figure reveals that no high frequency harmonic components are present. The ac voltage and current for the proposed topology is shown in Figure 6.57. Figure 6.58 validates the low THD grid current produced, is 1.7 %.

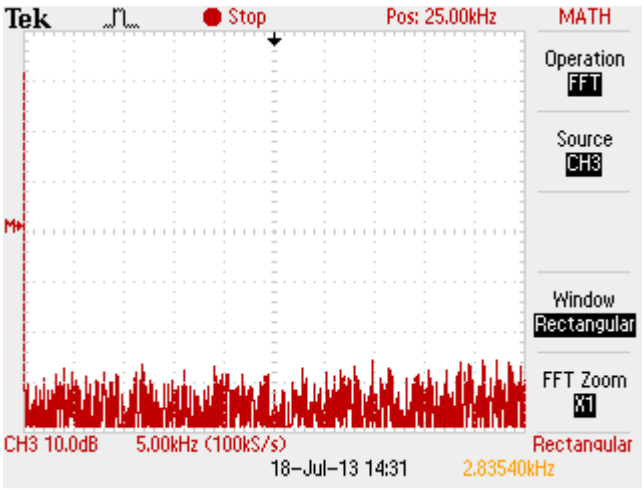


Figure 6.56: FFT of ground leakage current (10 mA/div) for modified unipolar H-Bridge inverter with CD-Boost converter

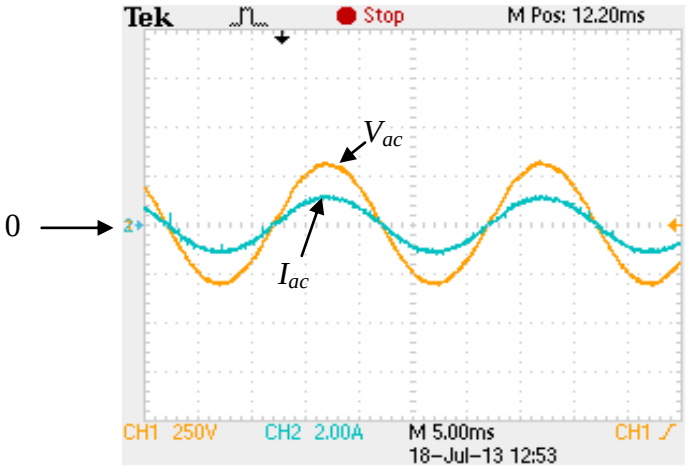


Figure 6.57: Ac voltage and ac current waveforms for modified unipolar H-Bridge inverter with CD-Boost converter

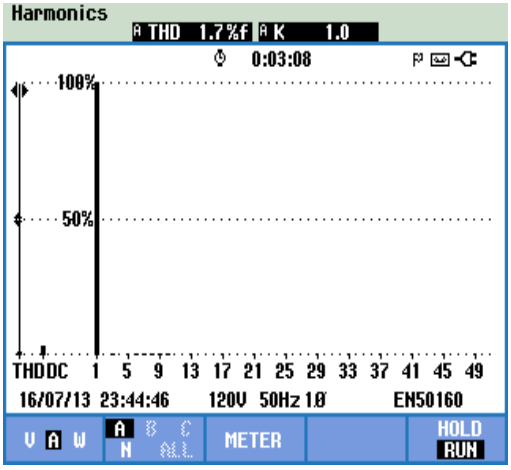


Figure 6.58: THD grid current for modified unipolar H-Bridge inverter with CD-Boost converter

6.5.3 Proposed Modified Unipolar H-Bridge Inverter with Modified Boost Converter

The switching pattern for the proposed modified unipolar H-Bridge inverter with modified boost converter topology used the same pattern as shown in Figure 6.54. Figure 6.59 shows the inverter voltage, constant common-mode voltage of 260 V and low ground leakage current of 17.7 mA for proposed modified unipolar H-Bridge inverter with modified boost converter. The ac waveform is shown in Figure 6.60 and 6.61 show the ac voltage, current and its THD current of 3.3 % respectively.

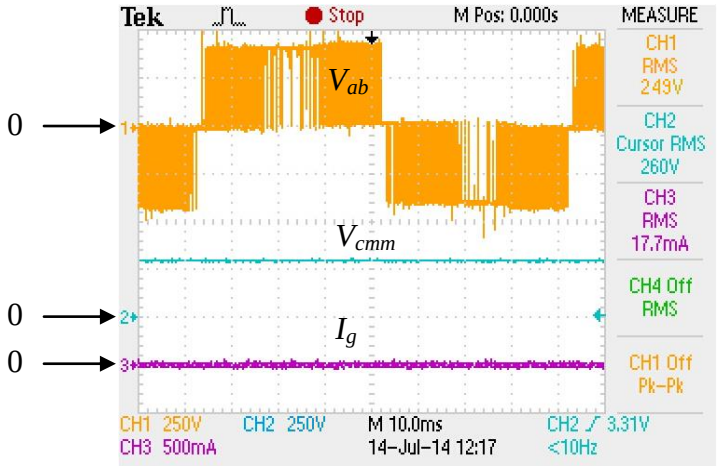


Figure 6.59: Inverter voltage, common-mode voltage and ground leakage current for proposed modified unipolar H-Bridge inverter with modified boost converter

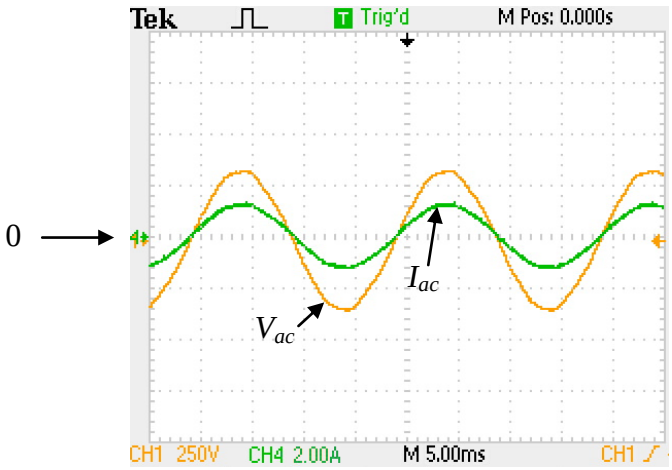


Figure 6.60: AC waveforms of proposed modified unipolar H-Bridge inverter with modified boost converter

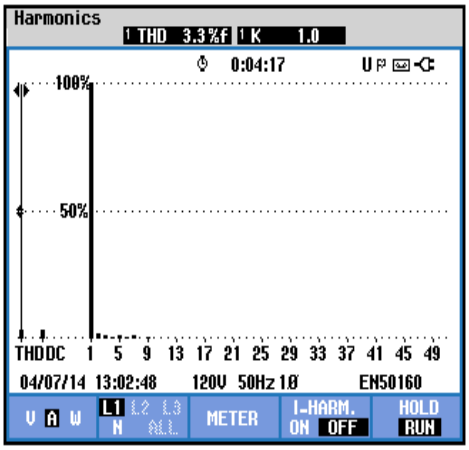


Figure 6.61: THD current for the proposed modified unipolar H-Bridge inverter with modified boost converter (measured by Fluke 435 series II Power Quality and Energy)

6.6 Performance Comparisons for Various Inverters

The comparison of power conversion efficiency between the different single-stage (H-Bridge inverter without boost converter) topologies is plotted in Figure 6.62. The power conversion efficiency is calculated as the ratio of the average ac output power to the average dc input power measured from the experiments. The results show that proposed SC-HB inverter topology has a higher conversion efficiency of 97.46 % at its rated power (P_o = 300 W) as compared to other topologies. Table 6.4 is listed the

performance comparison of different single-stage inverter topologies. The Californian efficiency of the various inverter topologies can be defined in (6.1).

$$\eta_{CEC} = 0.04\eta_{10\%} + 0.05\eta_{20\%} + 0.12\eta_{30\%} + 0.21\eta_{50\%} + 0.53\eta_{75\%} + 0.05\eta_{100\%} \quad (6.1)$$

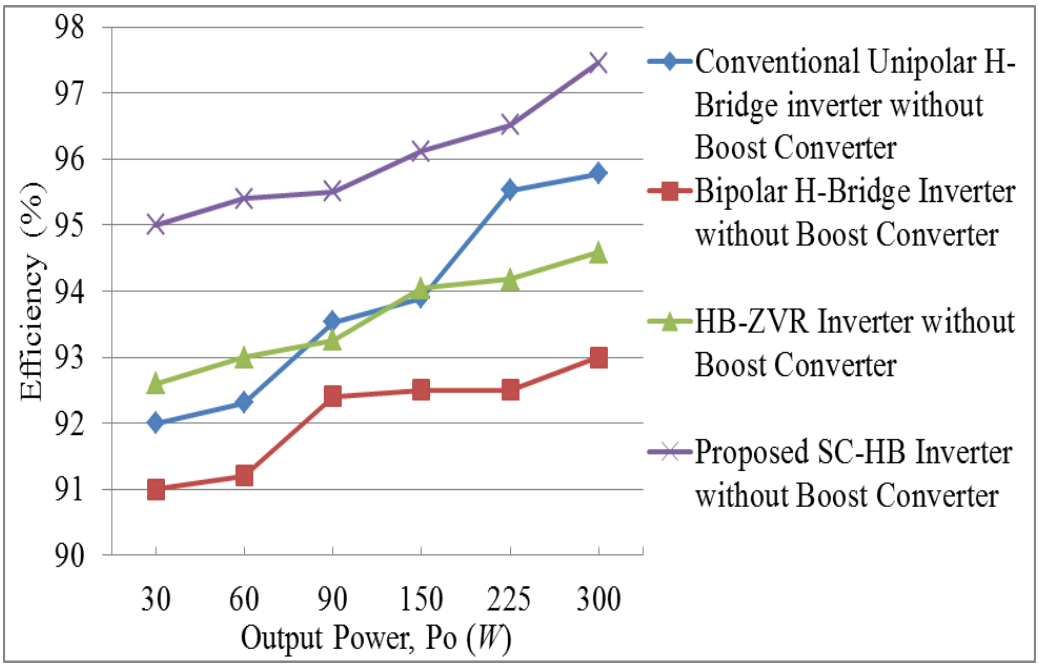


Figure 6.62: Conversion efficiency of different single-stage inverter topologies

Table 6.4. Performance comparisons of various single-stage inverter topologies

Inverter	**THD_i**	**Common - mode voltage (rms)**	**Ground leakage current (rms)**	**Californian efficiency (%)**	**Conversion efficiency**	
					W	**%**
Conventional unipolar H-Bridge without boost converter	4.4 %	339 V	1.075 A	94.7	30	92
					60	92
					90	94
					150	94
					225	96
					300	96
Bipolar H-Bridge inverter without boost converter	3 %	199.7 V	6 mA	92.7	**W**	**%**
					30	91
					60	91
					90	92
					150	93
					225	93
					300	93

HB-ZVR inverter without boost converter	2.8 %	231.8	5 mA	93.9	**W**	**%**
					30	93
					60	93
					90	93
					150	94
					225	94
					300	95
Proposed SC-HB inverter without boost converter	2.9 %	160.2 V	4 mA	96.2	**W**	**%**
					30	95
					60	95
					90	96
					150	96
					225	96
					300	97

From Table 6.4, the performance of ground leakage current and common-mode voltage are lowest for proposed SC-HB inverter without boost converter. In addition, at 300 W the highest conversion efficiency (97 %) and Californian efficiency (96 %) is performed by proposed SC-HB inverter without boost converter. The conversion efficiency and Californian efficiency is estimated using the ratio of power input and power output. The bipolar H-Bridge inverter without boost converter has lowest Californian and conversion efficiency, that it 92.7 % and 93 % respectively.

Figure 6.63 shows the conversion efficiency of different two-stage inverter topologies. The performance comparison of different two-stage inverter topologies is listed in Table 6.5. the proposed modified unipolar H-Bridge inverter with modified boost converter has highest Californian efficiency (95.8 %) and conversion efficiciency (97 %) compare to other topologies due to modified boost converter generates zero input dc current ripple. In addition the proposed topology generates lowest level of ground leakage current (17.1 mA) compare to other two-stage topologies.

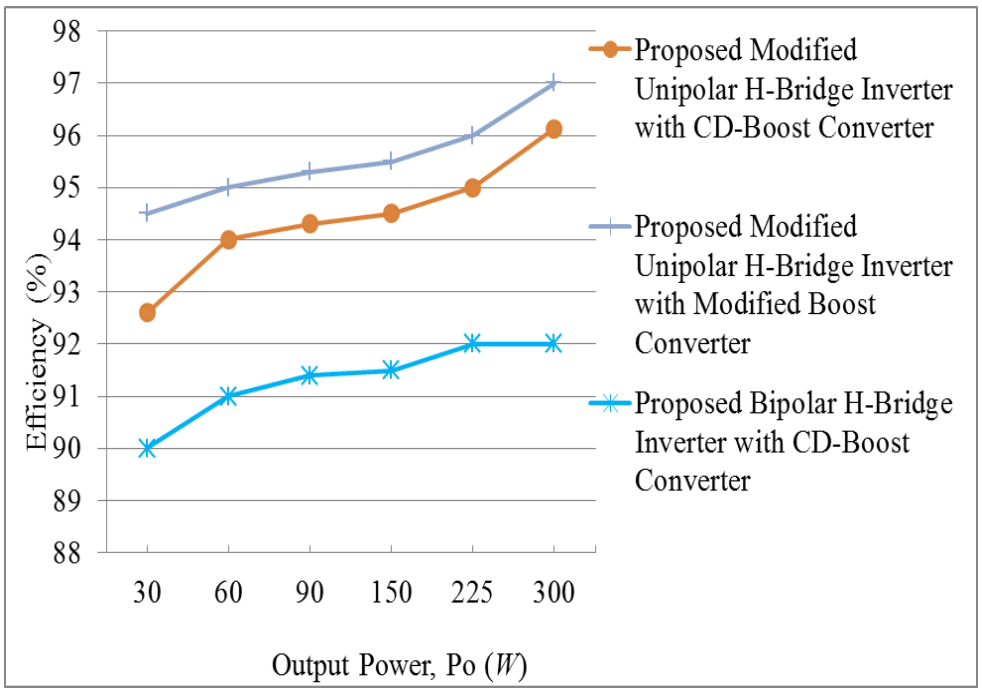


Figure 6.63: Conversion efficiency of different two-stage inverter topologies

Table 6.5. Performance comparisons of various two-stage inverter topologies

Inverter	**THD_i**	**Common-mode voltage (rms)**	**Ground leakage current (rms)**	**Californian efficiency (%)**	**Conversion efficiency**	
					W	**%**
Proposed bipolar H-Bridge inverter with CD-Boost converter	3.4 %	200 V	20.3 mA	91.7	30	90
					60	91
					90	91.4
					150	91.5
					225	92
					300	92
Proposed modified unipolar H-Bridge inverter with CD-Boost converter	1.7 %	100 V	25.2 mA	94.72	**W**	**%**
					30	92.6
					60	94
					90	94.3
					150	94.5
					225	95
					300	96.1
Proposed modified unipolar H-Bridge inverter with modified boost converter	3.3 %	260 V	17.7 mA	95.75	**W**	**%**
					30	94.5
					60	95
					90	95.3
					150	95.5
					225	96
					300	97

6.7 Controlling Algorithm for MPPT

Figure 6.64 shows the result of extracting maximum power from the PV module using the MPPT algorithm. As the power increased, the voltage decreased from 80 V to approximately V_{mp} = 60 V whereas the current increased from zero to I_{mp} = 0.6 A. The power transfer from PV generator to grid load is balanced by controlling the duty cycle and modulation index of boost converter and H-Bridge inverter. The power transfer balancing between dc sources to ac load is controlled by adjusting the converter's duty cycle and inverter's modulation index, as shown in Figure 6.65. The stable response of a boost converter is obtained as illustrated in Figure 6.66. That stable response of dc link voltage is controlled by PI algorithm.

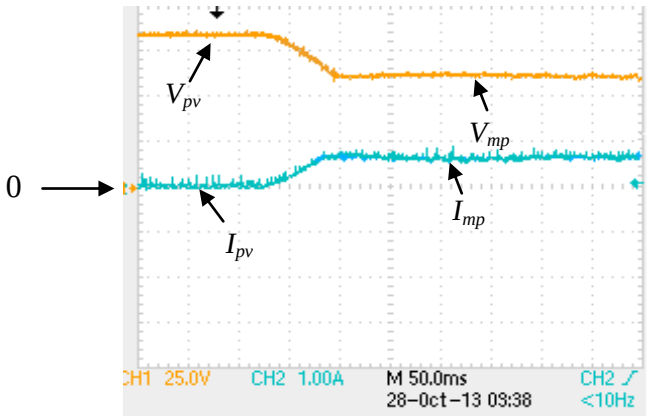


Figure 6.64: Time responses of V_{pv}, I_{pv}, V_{mp} and I_{mp}, at open-circuit mode (V_{pv}) and MPP mode (V_{mp})

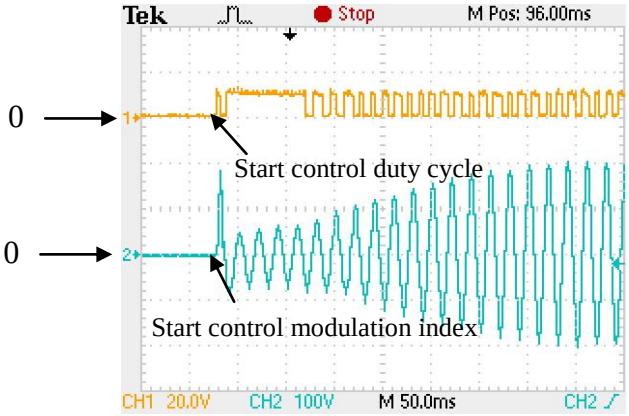


Figure 6.65: Duty cycle and modulation index control

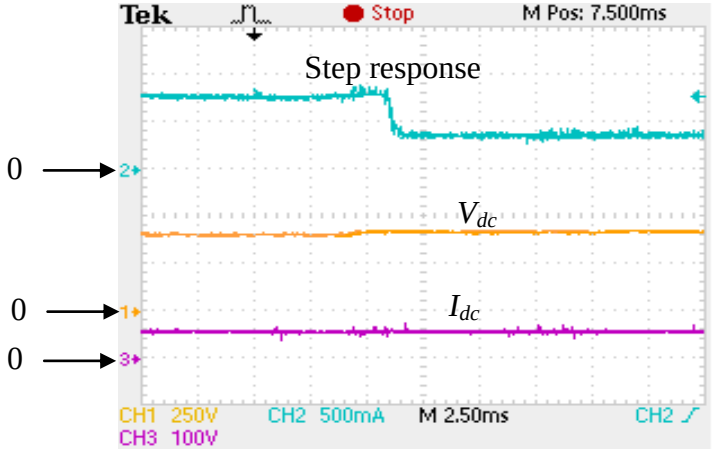


Figure 6.66: DC output current and voltage when the output power changes from 115 W to 63 W

6.8 Anti-islanding

Test on islanding has been carried out using Chroma programmable ac source model 600 series, even though it is not forming the main core of this work as stated in section 1.3. Three types of anti-islanding tests have been carried out under-frequency, over-frequency and under-voltage test as shown in Figures 6.67, 6.68 and 6.69 respectively. Overvoltage test cannot be carried out due to the limitation of maximum ac voltage in Chroma programmable ac source model 600 series. The disconnection time of over-frequency test is 109 ms, under-frequency 174 ms and for under-voltage is 62 ms.

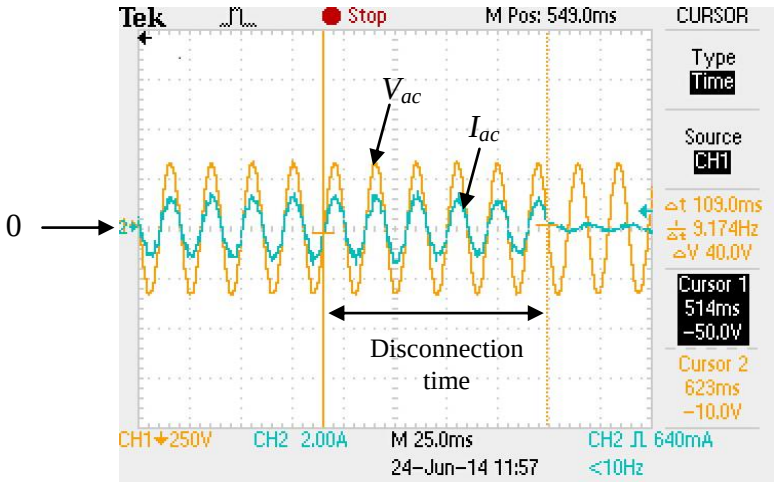


Figure 6.67: Anti-islanding of over-frequency test (51 Hz)

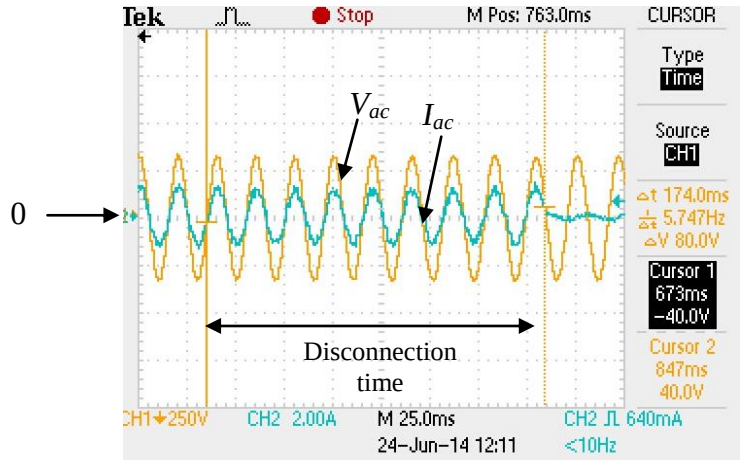


Figure 6.68: Anti-islanding of under-frequency test (49 Hz)

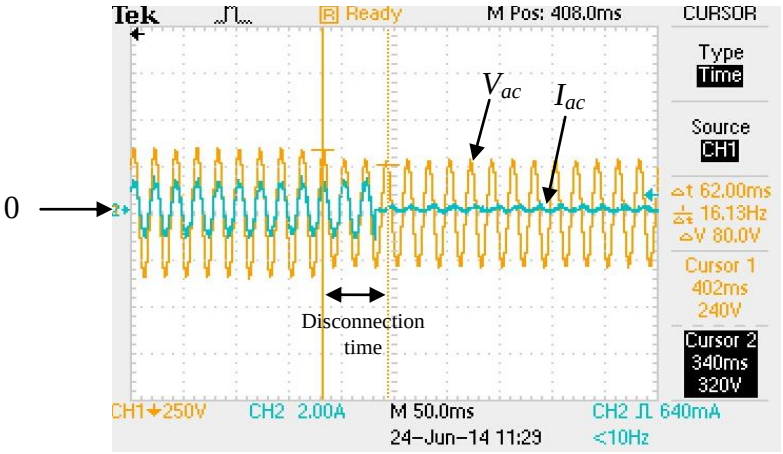


Figure 6.69: Anti-islanding of under-voltage test (200 V)

6.9 Summary

The hardware implementations of the proposed and existing prototype have been presented in this chapter. The block diagram platform of DSP TMS320F2812 was presented. The experimental results of the proposed and existing inverter were discussed. Some configuration such as SC-HB inverter, bipolar H-Bridge inverter with CD-Boost converter, modified unipolar H-Bridge inverter with CD-Boost converter and modified unipolar H-Bridge inverter with CD-Boost converter have been tested. Despite control system, maximum power point tracking and passive anti-islanding not forming the main core of this work, however it is well presented. The experimental results of those inverters and conventional inverter were presented and the measured values were compared.

CHAPTER 7

Conclusion and Future Works

7.1 Concluding Remarks

In this thesis, single-phase transformerless photovoltaic grid-connected inverters that generate high efficiency with constant common-mode voltage and low ground leakage current have been developed and analysed. This work uses simulation and experimentation as the main tools to assess and validate the technical viability of each modulation strategy, six different types of DC-to-DC boost converters, and seven different types of DC to AC converters of the single-phase grid-connected transformerless PV inverter. The performance of the proposed suitable DC-DC converter with the bipolar and proposed modified unipolar H-Bridge single-phase PV transformerless grid-connected inverter are analyse further.

The conversion voltage ratio against the duty cycle and normalized switch obtained by various DC-DC converter configurations such as CD-Boost converter, conventional boost converter, cascaded boost converter, three-level boost converter, inverting Zeta-derived converter and modified low input ripple converter has been analysed and discussed. The CD-Boost converter exhibits higher conversion ratio for $D > 0.7$ compared to other converters. CD-Boost converter has the lowest normalized switch stress at $D = 0.7$ compared to other DC-DC converter configurations. The inverting zeta-derived converter produced negative normalized stress due to the high values of M, as the switch voltage stress approaches the output voltage.

The modified boost converter has the highest conversion efficiency of about 98% due to minimal input dc current ripple. However the modified boost converter has less conversion ratio voltage compare to CD-Boost converter. The conventional boost converter and CD-Boost converter are 1% less efficient compared to modified boost

converter. The corresponding figures are 87% for inverting zeta derived boost converter, 91% for three-level boost converter and 80% for cascade DC boost converter.

The comparison of power conversion efficiency between two types of single phase transformerless grid-connected inverter topologies, with DC-DC converter and without DC-DC converter has been developed and analysed. Single- phase with DC-DC converter comprises of proposed bipolar H-Bridge inverter with CD-Boost converter, proposed modified unipolar H-Bridge inverter with CD-Boost converter, proposed modified unipolar H-Bridge inverter with modified boost converter and without DC-DC converter comprises of conventional unipolar H-Bridge without boost converter, bipolar H-Bridge inverter without boost converter, HB-ZVR inverter without boost converter and proposed SC-HB inverter without boost converter,

The power conversion efficiency is calculated as the ratio of the average ac output power to the average dc input power measured from the experiments. The results show that proposed SC-HB inverter topology has a higher conversion efficiency of 97 % at its rated power (P_o = 300 W) as compared to other topologies. Californian efficiency calculation has been presented.

Lowest value of ground leakage current is the proposed SC-HB inverter without boost converter. The ground leakage current is high for conventional unipolar H-Bridge inverter due to highest level of common-mode voltage compare to other topologies. For the two-stage inverter, the efficiency of proposed modified unipolar H-Bridge inverter is best efficiency within the compared topologies due to minimal input dc current ripple of proposed modified boost converter.

The balancing power transfer algorithm is implemented to maximise power transfer to the grid. Ground leakage current and constant common-mode voltage reduction has been analysed. The theoretical basis of each proposed strategy and technique is provided and supported with comparative analysis. Despite control system,

maximum power point tracking and passive anti-islanding technique not forming the main core of this thesis, significant effort has been devoted to the presentation of the PV grid-connected inverter systems needed to facilitate safe operation of the simulation and experimental setups. Systematic approach of the control, maximum power point tracking and passive anti-islanding structure and design is presented appropriately. The simulation results were verified by experiment through a laboratory prototype. In the experiment, TMS320F2812 DSP has been used to implement the entire algorithm.

7.2 Author's Contribution

The development of ground leakage current reduction in single-phase transformerless inverter for PV grid-connected system was crucial in this study. This work has the following features:

i) The high efficiency, low ground leakage current and balance series dc link capacitor of a new single-stage configuration (SC-HB inverter) was achieved.

ii) Reduction of ground leakage current in used of two-stage power converter configuration comprising bipolar H-Bridge inverter with CD-Boost converter, modified unipolar H-Bridge inverter with CD-Boost converter and modified unipolar H-Bridge inverter with modified boost converter.

iii) The effect matched of LCL filter at AC side inverter with regard to the ground leakage current.

iv) Since the value parasitic capacitance changes depending on construction and environment conditions, the various values with regard to the ground leakage current was presented.

v) The algorithm, which is based on balancing power, which comprises constant voltage, MPPT, dc-link bus voltage controller and anti-islanding protection.

7.3 Future Works

Future work can be performed on the existing power converter, to decrease the ground leakage current and to increase the efficiency of the power converter. Suggested future works are:

i) Investigate the viability of new-pulsed width modulation techniques during low voltage ride with very low ground leakage current of the grid-connected current source inverters.

ii) The efficiency can be improved by improving the utilizing better capacitor with lower ESR (Equivalent Series Resistance).

iii) An improved PWM technique with reduced common-mode voltage and satisfactory performance can be proposed.

iv) Developing new control methods for DC-to-DC switching converter with very low ripple. Employing new Fuzzy logic controller for MPPT for rapid irradiation changes and its uncertainties.

v) Extension of the work to multilevel current source photovoltaic grid-connected inverter.

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