A NEW THREE PHASE TRANSFORMERLESS SHUNT ACTIVE POWER FILTER WITH REDUCED SWITCH COUNT FOR HARMONIC COMPENSATION IN GRID-CONNECTED APPLICATIONS

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FACULTY OF ENGINEERING
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ABSTRACT

The demand for electricity in the modern industrial world is rapidly increasing, from household utilities to commercial industries. In the power utilization industry, an increasing number of renewable energy devices, as well as linear and nonlinear loads, are being introduced; these devices include the nonlinear rectifier and static Var compensator (SVC), which affect daily life. Integrated grid-connected energy systems produce certain harmonics, heat, and other complicated power-quality issues. Therefore, proper current harmonic and power-quality mitigation methods are required to enhance the reliability of the grid-connected systems. Various solutions have been proposed to solve the power-quality issues, the active power filter (APF) is the most dominant and liberal solution against problems of power quality, with reactive power and current harmonics compensation. The shunt active power filter (SAPF) topologies for harmonic compensation use numerous high-power rating components and are therefore disadvantageous. Hybrid topologies combining low-power rating APF with passive filters (PFs) are used to reduce the power devices (IGBTs) rating of voltage source inverter (VSI). Hybrid APF (HAPF) topologies for high-power rating system applications use a transformer with large numbers of passive components. When connected to the electrical grid, the increased number of semiconductor switch components produces higher switch losses, which contributes to harmonics in the output voltage waveform, degrades the system efficiency, and causes the overall system performance to deteriorate. In this thesis, a novel APF circuit based on reduced switch count and transformer-less configuration is presented. A new four-switch two-leg VSI topology is proposed for a three-phase SAPF that decreases the number of power switching devices in the power converter, hence minimizing the system cost and size. It comprises a two-arm bridge structure, four switches, coupling inductors, inductors and capacitors sets of LC PFs. The third leg of the three-phase VSI is removed by eliminating the set of power switching devices, thereby

directly connecting the phase with the negative terminals of the DC-link capacitor. The feasibility of the power distribution system is improved by eliminating the transformer and reducing power component to provide accurate performance, small volumetric size, and less cost compared with other existing topologies. The proposed topology enhances the harmonic compensation capability and reactive power compensation compared with conventional APF topologies in grid-connected systems. The series ac coupling inductors overcome the fixed reactive power compensation limitation, due to fixed value of the LC filters (inductors and capacitors set). The series LC PF tuned at the 5th and 7th order harmonic frequencies improves the active filtering capability and the reactive power compensation performance. The control algorithm ensures the regulated sinusoidal voltage, phase amplitude, and low THD in the power distribution system along with constant DC-link voltage. The new hardware prototype is tested in the laboratory to validate the results in terms of total harmonic distortion, reactive power compensation and harmonic mitigation, following the IEEE-519 standard. All the experimental and simulation results verify the feasibility performance of proposed transformer-less shunt active power filter (SAPF) with comparison to conventional full-bridge APFs and hybrid active power filter (HAPF) topologies.

ABSTRAK

Dalam dunia perindustrian moden, permintaan untuk tenaga elektrik semakin meningkat hasil daripada kepesatan utiliti isi rumah kepada industri. Dalam industri penggunaan kuasa, peningkatan jumlah peranti tenaga boleh diperbaharui, serta beban linear dan tak linear, sedang diperkenalkan; alat-alat ini termasuk penerus tak linear dan statik Var pemampas (SVC), yang memberi kesan kepada kehidupan seharian. Sistem tenaga grid Bersepadu menghasilkan harmonik, haba, dan beberapa isu-isu kuasa-kualiti yang lain, oleh itu, kaedah harmonik dan kuasa yang berkualiti tebatan semasa yang betul diperlukan untuk meningkatkan kebolehpercayaan sistem grid yang berkaitan. Pelbagai penyelesaian telah dicadangkan untuk menyelesaikan isu-isu seperti kualiti sistem kuasa yang tidak seimbang, pengimbangan beban, suntikan harmonik, arus neutral berlebihan, beban kuasa reaktif dan campur tangan dalam rangkaian sistem elektrik. Topologi SAPF untuk pampasan harmonic menggunakan banyak komponen berkuasa tinggi dan ia mempunyai banyak kelemahan. Topologi hibrid menggabungkan APF berkuasa rendah dengan penapis pasif (PF) digunakan untuk mengurangkan peranti kuasa (IGBTs) pada penyongsang sumber voltan (VSI). Bagi pengunaan kuasa tinggi, topologi penapis kuasa aktif hibrid (HAPF) diggunakan bersama pengubah dengan jumlah komponen pasif yang banyak. Apabila disambungkan kepada grid elektrik, peningkatan bilangan komponen suis semikonduktor menghasilkan kehilangan kuasa semasa pengsuisan yang lebih tinggi, dimana ia menyumbang kepada harmonik dalam bentuk gelombang voltan output, mengurangkan kecekapan sistem, dan menyebabkan prestasi sistem keseluruhan merosot. Dalam tesis ini, litar APF baharu berdasarkan pengurangan kiraan suis dan konfigurasi pengubah-voltan “transformer” dibentangkan. Bagi mengurangkan kos sistem dan saiz berdasarkan fakta-fakta ini, topologi penyongsang empat suis dua kaki VSI dicadangkan untuk penapis kuasa aktif `tiga fasa. Ia mempunyai struktur dua lengan jejambat, empat suis, induktor gandingan dan beberapa set LC PF. Fasa ketiga VSI dikeluarkan dengan

menghapuskan set peranti kuasa pensuisan pada fasa tersebut, dengan itu terus menyambung fasa tersebut kepada terminal negatif kapasitor DC-link. Kemungkinan sistem pengagihan kuasa bertambah baik dengan menghapuskan pengubah-voltan transformer dan mengurangkan komponen kuasa untuk memberikan prestasi yang jitu, saiz isipadu kecil, dan kurang kos berbanding dengan topologi lain yang sedia ada. Topologi yang dicadangkan meningkatkan keupayaan pampasan harmonik dan pampasan kuasa reaktif berbanding dengan topologi APF konvensional dalam sistem grid yang berkaitan. Induktor gandingan siri ac mengatasi reaktif had pampasan kuasa tetap dengan menetapkan nilai optimum penapis LC (induktor dan kapasitor set). Penapis pasif LC PF ditala pada harmonic ke-5 dan ke-7 frekuensi asas untuk meningkatkan keupayaan penapisan aktif dan prestasi pampasan kuasa reaktif. Algoritma kawalan memastikan voltan terkawal berbentuk sinusoidal, fasa amplitud, dan THD rendah dalam sistem pengagihan kuasa bersama-sama dengan voltan DC-link. Prototaip eksperimen yang baru diuji di makmal untuk mengesahkan hipotesis dari segi jumlah herotan harmonik (THD), keseimbangan bekalan semasa dan pampasan harmonik, menurut standard IEEE-519. Semua keputusan eksperimen dan simulasi mengesahkan prestasi kebolehlaksanaan pengubah-kurang shunt kuasa penapis aktif (SAPF) yang dicadangankan dicadangkan meningkatkan keupayaan pampasan harmonik dan menyediakan pampasan kuasa reaktif, berbanding dengan topologi APF konvensional.

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Wajahat Ullah Khan Tareen

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LIST OF ABBREVIATIONS

APF	:	Active Power Filter
DER	:	Distributed Energy Resources
EMI	:	Electromagnetic Interference
FB	:	Feed-Back
FF	:	Feed-Forward
HAPF		Hybrid Active Power Filter
HPF		High Pass Filter
ML-MFI		Multilevel Multifunctional Inverter
PCC	:	Point of Common Coupling
PFC	:	Power Factor Correction
PF		Passive Filter
PI	:	Proportional Integral
PLL		Phase Locked Loop
PV		Photo voltaic
PQ	:	Power Quality
PWM	:	Pulse Width Modulation
RE		Renewable Energy
STATCOM	:	Static Synchronous Compensators
SPWM		Sinusoidal Pulse Width Modulation
SRF	:	Synchronous Reference Frame
SVM	:	Space Vector Modulation
SVC	:	Static VAR Compensator
THD	:	Total Harmonics Distortion
VSC		Voltage Source Converter
WECS		Wind Energy Conversion System
WT		Wind turbines
UPFC	:	Unified Power Flow Controller
UPQC	:	Unified Power Quality Conditioner

LIST OF SYMBOLS

C_F	:	Capacitor filter
c_{dc}	:	DC-link capacitor
f_{sw}	:	Switching frequency
i_d	:	Instantaneous active current
i_q	:	Instantaneous reactive currents
$i_{d_{AC}}$	:	Instantaneous active AC current
$i_{q_{AC}}$	:	Instantaneous reactive AC currents
$i_{d_{DC}}$	:	Instantaneous active DC current
$i_{q_{DC}}$	:	Instantaneous reactive DC currents
i_{sabc}	:	(a, b, c) three-phase source current
i_{Labc}	:	(a, b, c) three-phase load current
I_F	:	(a, b, c) Inverter output filter compensator current
K	:	Control gain
K_P	:	Proportional Gain
K_I	:	Integral gain
L_{AC}	:	Load-side inductor
L_s	:	Source-side Inductor
L_F	:	Inductor filter
R	:	Resistance
V_{AF}	:	Inverter output Voltage
v_{AF}^*	:	Voltage reference of each phases *(abc)*
v_{sabc}	:	(a, b, c) three-phase source voltage
v_{dc}	:	DC-link voltage
v_f	:	(a, b, c) Inverter output filter voltage
V_L	:	Load voltages
$\omega 1$	:	Fundamental frequency
θ	:	Phase angle
z_s	:	Source impedance
Z_F	:	Filter impedance

CHAPTER 1: INTRODUCTION

This chapter firstly discusses the background and motivation of this Ph.D. thesis, a new three-phase transformer-less shunt power filter (SAPF) based on four-switch two-leg voltage source inverter for harmonic compensation performance in grid-connected applications. Important features of the state-of-the-art work in both transformerless and reduced switch count APFs system has been explained briefly. Next, the problem statement and objectives of this work have been stated. The dissertation outline is stated at the end of this chapter.

1.1 Background and motivation

The demand for electricity in the modern industrial world is rapidly increasing, from household utilities to commercial industries. Integration of distributed energy resources (DER) and storage devices improves the reliability and electric power quality (PQ) while decreasing the loss of power distribution or transmission networks. The solar photovoltaic (PV) and wind energy (WE) power are the two leading renewable energies resources for reducing the continuous burden on the national power grid and the global environment. In the power utilization industry, an increasing number of renewable energy devices, as well as linear and nonlinear loads, are being introduced; these devices include the nonlinear rectifier and static VAR compensator (SVC) (Montero, Cadaval, & Gonzalez, 2007). These solid states switching converters draw reactive power and current harmonics from the AC grid which produces current and voltage distorted waveforms, resulting in various disturbance, harmonic pollutions and directly impact the human life activities.

Integrated grid PV and wind energy systems produce certain harmonics, heat, and other complicated power-quality issues. Thereby affecting the supply current and voltage sinusoidal waveform spectra (Montoya, Garcia-Cruz, Montoya, & Manzano-Agugliaro, 2016), in terms of lower system efficiency, overheating of transformers, increased

malfunction of motors and cables, increased power loss, necessity of protection devices (Salomonsson, Soder, & Sannino, 2009), limited life period of wind turbine generator (Carrasco et al., 2006) and solar PV modules (Kannan, Leong, Osman, Ho, & Tso, 2006). The renewable power output is stochastic and the energy resource is intermittent. Therefore, proper current harmonic and power-quality mitigation methods are required to enhance the reliability of the grid-connected system. Various solutions have been proposed to solve the power-quality issues and the network interference in electrical systems. (Zeng, Yang, Zhao, & Cheng, 2013). Filters are traditionally used in grid-integrated systems in combination with passive filters (PFs) (Ostroznik, Bajec, & Zajec, 2010b) against series harmonics.

According to surveys of grid-integrated systems, the power-quality issues are addressed by the use of more advanced filter technologies, such as a static synchronous compensator, active power filter (APF), dynamic voltage regulator, and multilevel inverter. In the past, series harmonics grids problems are mitigated with the PFs devices (R. Beres, Wang, Blaabjerg, Bak, & Liserre, 2014). They are considered as an initial stage of development to mitigate the current harmonics, along with low cost solutions to the power quality issues (Ringwood & Simani, 2015). As such, PFs have limited use because of issues, including limited filtering, specific load ranges, fixed compensation, larger sizes, parallel and series negative resonance between grids, and filter impedance; these issues cause the rapid decay of passive components (R. Beres et al., 2014).

The active power filters (APFs) are considered as a second stage of development and effective solution to overcome the limitation of the passive filter (PFs). The shunt APF (SAPF) is the most dominant devices against the problems of power quality, with reactive power and current harmonics compensation (H. Akagi & Isozaki, 2012; Kolar, Friedli, Rodriguez, & Wheeler, 2011). The filter performance depends on inverter parameters,

control schemes, and reference current detection techniques (A. Luo, Zhao, Deng, Shen, & Peng, 2009). With the increasing load demand, the APF rating also increases with the accumulating system capacity and cost (Litran & Salmeron, 2012). As a solution, hybrid APFs (HAPF) are used to configure the PF with SAPF (Lao, Dai, Liu, & Wong, 2013). In HAPF operation, both filters are controlled, such that the low-order harmonics are eliminated by SAPFs operation (L. W. Qian, D. A. Cartes, & H. Li, 2008), whereas the higher frequency harmonics are canceled by PFs. APFs reduce the load current disturbances, which improve current and voltage harmonic compensation.

Recently, several HAPF topologies use transformers and an excessive number of passive components as key tools to manage the filter size, cost, and weight optimization. However, the transformer-less topologies achieve a safer and higher system efficiency, smaller volumetric size, cheaper cost, and more compact structures as compared with older transformer-based topologies. Furthermore, the HPFs technology evaluates to fourth stage of development as unified power quality conditioner (UPQC) (Khadkikar & Chandra, 2008).

For grid-connected systems, an inverter is the key device required to convert AC power to DC power. The inverter is mounted from the low-power KW range to the higher-power MW range to construct the output sinusoidal waveform, which is accomplish by the series or parallel combination of electronic switch devices . Developments in the large-scale PV power system and wind generation systems subject inverters to continuous evolution and make these inverters indispensable. Despite the increasing demand, a major issue of inverters is the larger amount of power switching components, such as insulated gate bipolar transistors (IGBTs) and metal-oxide semiconductor field effect transistors (MOSFETs). Several pure SAPFs are limited by the use of high-power-rating components to improve the utility power factor correction and current harmonic compensation. When

connected to the electrical grid, the increased number of semiconductor switch components produces higher switch losses, which contributes to harmonics in the output voltage waveform, degrades the system efficiency (Elbaset & Hassan, 2017), and causes the overall system performance to deteriorate (Sajid Hussain Qazi & Mohd Wazir Mustafa, 2016). Recently, a reduced switch count has become a cutting-edge solution in power electronics technology. Despite the importance of component reduction for advancing energy issues, literature on the reduction of switches in APFs is limited. Therefore, this dissertation will focus on the design of a new three-phase transformer-less shunt power filter (SAPF) based on four-switch two-leg voltage source inverter for grid application.

1.2 Problem statement

The development in the power industries increases the number of both linear and non-linear loads in every system. In the non-linear loads conditions, many solid states switching converters draw reactive power and current harmonics from the AC grid. These non-linear loads generate harmonics, which produces disturbance and directly impact every equipment, power system and services. The shunt active power filter (SAPF) topologies for harmonic compensation use numerous high-power rating components and are therefore disadvantageous. Hybrid topologies combining low-power rating APF with passive filters (PFs) are used to reduce the power devices (IGBTs) rating of voltage source inverter (VSI) (Limongi, da Silva, Genu, Bradaschia, & Cavalcanti, 2015). Hybrid APF (HAPF) topologies for high-power rating system applications use a transformer with large numbers of passive components (A. Bhattacharya, Chakraborty, & Bhattacharya, 2012). When connected to the electrical grid, the increased number of semiconductor switch components produces higher switch losses, which contributes to harmonics in the output voltage waveform, degrades the system efficiency, and causes the overall system performance to deteriorate (Fatemi, Azizi, Mohamadian, Varjani, & Shahparasti, 2013).

Also as a limitation the series LC passive filter produces an unavoidable fundamental leading current flow in the system (L. Zhang, Loh, & Gao, 2012). Furthermore, the reactive power compensation capability of conventional hybrid APF is limited (J. C. Wu et al., 2007) due to series LC passive filters (fixed value), which is the main disadvantage of the hybrid APF system.

1.3 Objectives of the study

The aim of this study is to design a novel SAPF circuit based on reduced switch count inverter configuration in order to ensure enhanced and superior performance in the reactive power compensation, harmonic mitigation, and good power quality for the grid connected applications. In order to achieve this aim, the following specific objectives will be conducted;

1. To propose a new three-phase transformer-less shunt active power filter (SAPF) based on four-switch two-leg voltage source inverter for grid applications.
2. To implement the hardware prototype of the proposed SAPF circuit.
3. To analyze the thorough performance of proposed transformer-less SAPF system.
4. To compare the performance of proposed transformer-less SAPF system with the conventional full-bridge APFs and hybrid active power filter (HAPF) topologies.

1.4 Dissertation outline

This dissertation focus on the collection of the related publications and project findings. Therefore, it covers the design analysis, theoretical study, simulation and experimental analysis of the proposed APF model. Centered on the flow of the contributions, background, state-of-the-art work, problem statement and dissertation objectives are presented in Chapter 1. The remaining research of this dissertation is divided into five chapters, as follows.

In Chapter 2 a comprehensive literature review about the APF is presented. This chapter aims to assess the most advanced APFs by reducing the number of power switches in grid-connected inverters. The most advanced APF topologies and their classifications; namely AC–AC inverter, parallel inverter and split DC-leg inverter, under the three-phase systems have been explained in detail and comparison of their characteristics is performed. Important features of the transformerless inverters and reduce switch count components in PV and wind energy conversion systems have been greatly explored. Besides, complex control schemes with their limitations for reconfigurable VSIs systems are discussed with justifications.

The **Chapter 3,** explains the mathematical modeling and design procedure of a four-switch two-leg inverter structure with *LC* filter system. Different configuration parts and overall control schemes analysis of both the filters system have been explained in detail. Moreover, a detail study on the four-switch two-leg inverter, PFs design analysis, filtering characteristic including the robustness and reactive power compensation capability of the entire system is analyzed.

The **Chapter 4** summarizes the prototype developed stages and the experimental results of the proposed APF designed for harmonic mitigation and reactive power compensation of a 5 kW diode rectifier. First, the practical implementation of the proposed APF prototype is presented, describing the design parameters with other components selections, the auxiliary circuits, and the overall snapshot of the laboratory test rig. Then, the simulation and experimental results with some merit figures, show the performance of the APF for harmonic mitigation and reactive power compensation are presented. Also, the comparison of the relevant experimental work by displaying the output utility current and voltage spectrum is analyzed in detail. A comparison study is

carried out in terms of the output THD, cost and volumetric size comparison of the proposed APF system is evaluated with other state of the art works.

The C**hapter 5**, summarizes the main contributions and presents the conclusion of the dissertation. Also, provide future work based on this study and suggestion for extension of this project.

CHAPTER 2: LITERATURE REVIEW

2.1 Introduction

This chapter presents an in-depth systematic literature on the advance reduction of switches in the APFs system. All conference/journal/transaction published papers are categorized based on comparison in the field of APFs grid-connected applications and their characteristics to operate the transformer-less and reduced switch count topologies. This chapter focuses on the collection of the related SAPF publications in the topic of advance reduced switch count topologies and complex control schemes for the reconfigurable VSIs. Besides, a comparison on recent developments and their characteristics is performed in detail.

2.2 Mitigation of power quality and distributed generation systems

2.2.1 Grid-connected APF-PV inverter

The excessive penetration of the renewable devices in the power transmission network, creates the various power quality challenges for the engineers and researchers. The main aim of installing the PV system at the point of common coupling (PCC) is to improve the operation of power distribution systems and to generate active power (Momeneh, Castilla, Miret, Martí, & Velasco, 2016). However, to prevent the additional cost of the power circuit, several PV-fed grid interactive topologies combined the PV inverter with the additional functionality of SAPF (Amjad & Salam, 2014), as well as voltage and reactive power support. Therefore, the PV inverter injects the compensating current into the grid to filter the load current harmonics (Calleja & Jimenez, 2004; Ouchen, Betka, Abdeddaim, & Menadi, 2016; Romero-Cadaval et al., 2013). In addition, the inverter uses the active power produced from the PV solar energy system. On the other hand, the APF are introduced in the PV system to improve the power conversion efficiency, reliability, and current harmonic distortions of the distribution systems

(Biricik, Komurcugil, & Basu, 2016; Kumar & Varma, 2016). Figure 2.1 illustrates the hierarchical structure of renewable energy with power sources and energy storage resources in a power distribution network (Krishna & Kumar, 2015; Patrao, Figueres, Gonzalez-Espin, & Garcera, 2011).

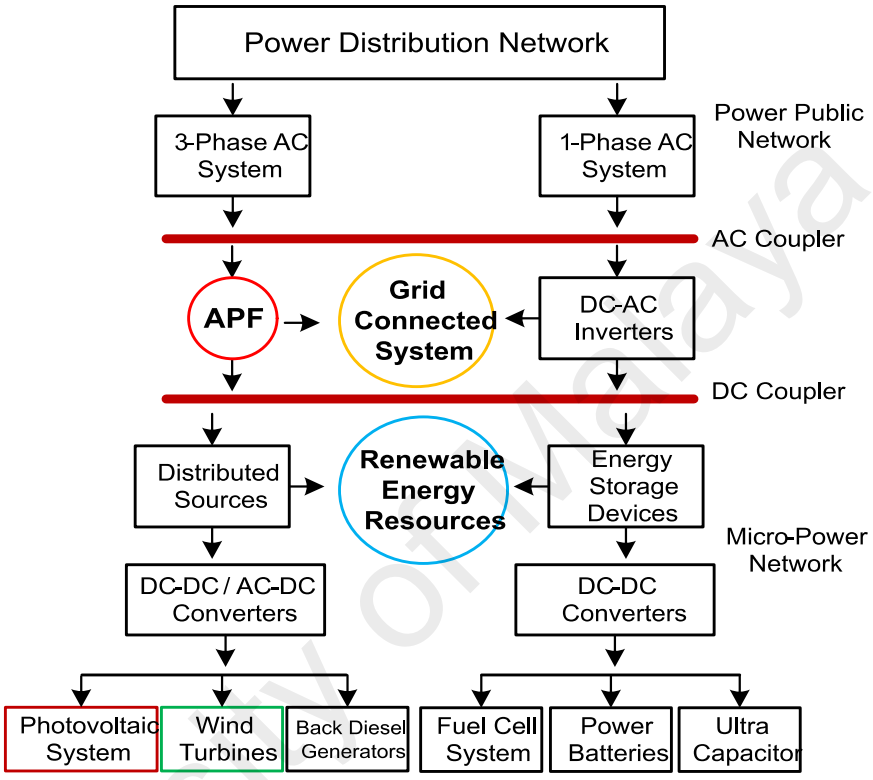


Figure 2.1: Hierarchical structure of renewable power sources and grid-connected inverters in a power distribution network

Recently, the multilevel multifunctional inverter (ML-MFI) has become the most dominant technology used in the PV grid-integrated electrical power generation systems. At high DC-rated voltage, it produces the output waveform in steps with low harmonic distortion waveform. It easily controls multifunctional inverter issues such as grid current harmonic and unbalance mitigation, reactive power compensation, control voltage at PCC and transient process in between the PV generator to utility grid during the APF operation (Wosik, Kozlowski, Habrych, Kalus, & Miedzinski, 2016). The ML-MFI topologies are installed in high-rated and large PV systems, due to its several advantages, such as low harmonic, less power dissipation and low electromagnetic interference (EMI) outputs.

Table 2.1 summarizes the comparison between the grid-integrated PV inverter topologies and the additional functionalities of APFs (Zeng et al., 2013). The elimination of a transformer generates several problems, including efficiency degradation, safety complications, leakage current, and the installation of a resonant circuit.

Depending on the topology structure and modulation scheme, many combinations of power converter configurations are shunted at the PCC to work as an interface between the utility grid and renewable energy source. However, the common mode voltage and the absence of leakage current in the PV grid-connected system provide improvement to the overall system voltage and frequency as compared with traditional topologies. In study (Mahela & Shaik, 2016; Tsengenes & Adamidis, 2011), a three-level NPC-MFGCI PV system is controlled more efficiently with a modified voltage-oriented control and space vector PWM (SVPWM) technique to provide shunt active filtering, reactive power compensation and load current balance to the utility grid.

Table 2.1: Comparison of three-phase PV-APFs in grid-inverter topologies

Authors	Topology	Modulation	Capacity (kVA)	No. of switches	No. of DC capacitors (uF)	THD (%)	PV/DC-link voltage (V)
(T.-F. Wu, Shen, Chan, & Chiu, 2003)	H-bridge	SPWM/PI	1.1	6	1@2200p	7.8	400
(Yu, Pan, & An, 2005)	H-bridge	SPWM/PI	10	6	-	-	-
(Mohod & Aware, 2012)	H-bridge	Hysteresis	150	6	1@5	1.29	800
(Marei, El-Saadany, & Salama, 2004)	H-bridge	SPWM/FLC, PI	-	6	0	2.5	500
(Abolhassani, Enjeti, & Toliyat, 2008)	H-bridge	SPWM/FLC, PI	20	12	-	-	-
(Gajanayake, Vilathgamuwa, Loh, Teodorescu, & Blaabjerg, 2009)	ZVI	SPWM/FLC, PI	7.5	6	2@1500	4.21	100–60
(Tsengenes & Adamidis, 2011)	3L- NPC	SPWM/FLC, PI	1	14	2@3m	-	1100
(Sawant & Chandorkar, 2009)	Four bridge	3D-SVPWM	-	8	1@850	13	350
(Majumder, Ghosh, Ledwich, & Zare, 2009)	Full bridge	Hysteresis/LQR	-	12	1@-	<0.5	350
(Han, Bae, Kim, & Baek, 2006)	H-bridge	SPWM/FLC, PI	30	12	2@3300	-	700

SAPF can integrate with the PV grid-connected system for harmonic elimination content and reactive power compensation to keep the DC-link voltage constant (Demirdelen, Kayaalp, & Tumay, 2017). Therefore, a precise and independent mathematical model is needed against the parameter variation (Puhan, Ray, & Panda, 2016). By contrast, energy storage systems, such as batteries, super capacitors, and flywheels, are programmed to overcome the intermittency problem in renewable PV energy systems. The inherent characteristics of the PV systems decreased the power generation to 15% per second, thereby affecting the performance of the grid network. Therefore, the energy storage systems maintain the constant voltage by reducing voltage fluctuation and maintaining higher PV efficiency (X. H. Liu, Aichhorn, Liu, & Li, 2012). Altogether, the PV systems also help to suppress the harmonic content and regulate the

compensating reactive power, thereby enhancing the reliability of the PV grid-integrated system (Tang, Yao, Loh, & Blaabjerg, 2016).

2.2.2 Grid-connected APF-WE inverter

In recent times, the energy industry is leaning more toward renewable energy consumption. Wind energy is a more legitimate source of power, less expensive, and available throughout the years (Sajid Hussain Qazi & Mohd Wazir Mustafa, 2016). Compared with fossil fuels and solar energy, wind energy has the additional advantage of being cost effective, absence of greenhouse gas emissions, a progressive renewable energy source, accessible and production is flexible. Thus, the energy demand can be met and more environment friendly at the power distribution network level (Shafiullah, Oo, Ali, & Wolfs, 2013). However, poor power quality is a complicated issue in grid-connected WECS.

The high demand of mounting the WTs with main grid affects the reactive power, voltage fluctuations, and produces output voltage and current flicker at the PCC, due to the switching operations (Paliwal, Patidar, & Nema, 2014). The variable-speed WT operation depends upon the active and reactive power control and behavior of the nonlinear and unbalanced loads. In this aspect, the nonlinear characteristics of power electronic devices generate high THD value current and output voltage, weakening the WT generator (WTG) performance (Phan & Lee, 2011), cause more heat and low system efficiency, and decrease the life span of WTG (Alnasir & Kazerani, 2013). Therefore, an appropriate harmonic mitigation and reactive power compensation technology is necessary to improve the power quality of wind energy in the grid-connected systems (Ullah, Bhattacharya, & Thiringer, 2009).

A WTG operates at the constant wind speed to control the permanent magnet synchronous generator (PMSG) to mitigate the current harmonics (dos Reis et al., 2006).

Therefore, a forward modified modulation technique is used to control the APF system based on different reference signal extraction techniques (S. H. Qazi & M. W. Mustafa, 2016). A more advanced variable frequency-based WT system (WTS) operates in the islanding mode to cancel the harmonics (Muller, Deicke, & De Doncker, 2002). Therefore, the doubly fed induction generator (DFIG) in the fixed speed, adopts the WT with ability of APF. During the voltage unbalance environment and to reduce the converter cost, a reduced-switch-count topology for WECS system is installed with a split-capacitor leg configurations (Ahmed, Abdel-Latif, Eissa, Wasfy, & Malik, 2013; Mlodzikowski, Milczarek, & Malinowski, 2014; Raju, Chatterjee, & Fernandes, 2003). However, this topology has decoupling issues between the multipole PMSG and the grid. In addition, it requires an extra DC-link capacitor that needs a more complex control, and faces higher semiconductor stress (Ng et al., 2008).

In grid-connected WECS, reactive power control and compensation is an important requirement and an essential parameter to the power distribution grid. It is essential to maintain the constant voltage profile of the WTG to control the minimum losses in transferring the reactive power exchange to the power grid. The under load tap changer transformer is the main device that controls reactive power compensation in the grid. Furthermore, several WT produce limited voltage and reactive power in the coupled induction generator (Lima, Luna, Rodriguez, Watanabe, & Blaabjerg, 2010). As a solution, several devices, such as STATCOM (B Singh, Saha, Chandra, & Al-Haddad, 2009), SVCs, on-load tap changer (OLTC) and switching capacitors, PWM inverter, and a combination of capacitor and inductor (Muller et al., 2002), are installed with the induction generators. Several devices, such as DBR, OLTC, and manual switched capacitor banks, are not capable of overcoming harmonics and voltage flicker. By contrast, the DSTATCOM, SVC, STATCOM, and DFIG devices improve the static and dynamic stability behavior of the reactive power and fixed speed wind generators (Mahela

& Shaik, 2015). These devices regulate the voltage balance, which helps in increasing the use of the wind power in power grid networks. Table 2.2 demonstrates the reactive power compensating devices (Salam, Tan, & Jusoh, 2006) in grid-connected WECS compared with other parameters (Saqib & Saleem, 2015). The control parameters related to reactive power compensating devices are as follows: on-load tap changer (OLTC), automatic voltage control (AVC), dynamic voltage restorer (DVR), series dynamic breaking resistor (SBBR), static synchronous compensator (STATCOM), static VAR compensators (SVC), thyristor-controlled series capacitor (TCSC), and unified power flow controller (UPFC) .

Table 2.2: Control parameters affected by the reactive power devices

Parameters	OLTC	Capacitor & Reactor Bank	AVC	DVR	SDBR	STATCOM	SVC	TCSC	UPFC
Reactive power	*	***	**			****	***	**	****
Active power	*	**	**	**	**	*	*	**	
Voltage stability	*	**	**			****	***	***	****
Voltage	*	**	**			****	***	**	****
Flicker		*				****	***		****
Harmonic reduction		*							****
Power flow								***	****
Oscillation damping		*		**	***	***	**	***	****

High number of "*" is preferred

2.3 Methods for Mitigating Harmonics

2.3.1 Traditional methods for mitigating harmonics

Over the course of time, different methods are adopted to mitigate harmonic contents in power distributed grid-tied systems (Khadem, Basu, & Conlon, 2011; Stratford, 1980). The passive filters (PFs), and active power filters (APFs) are the enhance technologies for power quality and harmonics problems are discussed in this section.

2.3.2 Shunt passive filters (PFs)

The passive filter (PFs) was first introduced as an initial stage solution to mitigate the current harmonics and power quality issues in the power distribution network. It presents

a simple economical solution consisting of a different series and parallel combination of inductor, capacitors and damping resistors (Al-Zamil & Torrey, 2001). The regularly used configuration of the PFs is depicted in Figure 2.2, depending the filtering characteristics on the values of inductance and capacitance set. Each operation is influenced the fundamental source impedance, and is tuned at prerequisite harmonic order such as first, second, and third order to track the requisite harmonics.

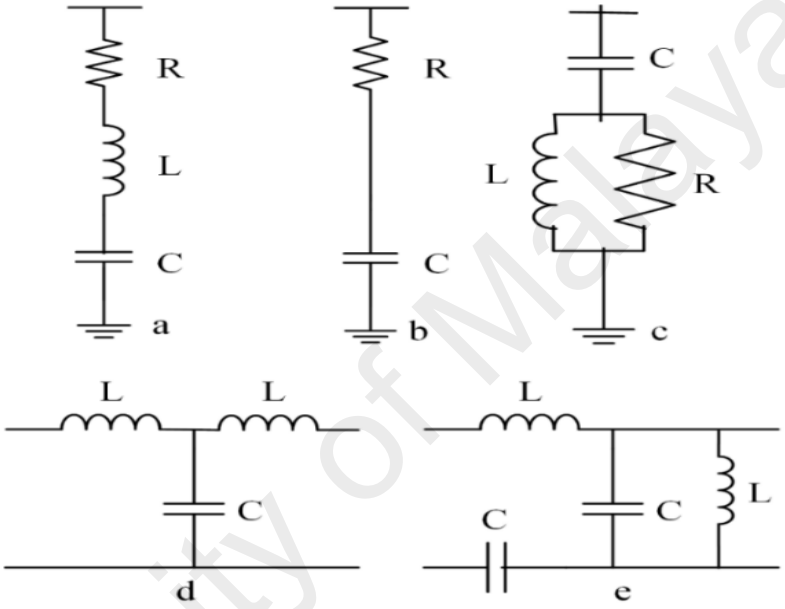


Figure 2.2: Passive filter structures (a) Single tuned filter, (b) First order high pass filter, (c) Second order high pass filter, (d) LCL filter, (e) LLCC filter.

The literature study consists of many PFs designing techniques, including the series filter, shunt filter, single tuned filter (Cristian Lascu, Asiminoaei, Boldea, & Blaabjerg, 2007), double tuned filter (Hirofumi Akagi, 2006), low-pass filter (Cristian Lascu et al., 2007), high-pass filter (Hirofumi Akagi, Nabae, & Atoh, 1986), band-pass filter , LCL filter , and LCC filter (Tang et al., 2012) respectively. The series PF configuration are installed in series with the power distribution system to provide a high impedance to cancel the flow of harmonic current. Usually, for better harmonic mitigation and reactive current components compensation the PFs is coupled with the thyristor-controlled reactor (TCR) (Rahmani, Hamadi, Al-Haddad, & Dessaint, 2014). Many of the shunt PFs

limitations are overcome by the quasi typed passive filter (QPF) (Mahanty, 2008), some of the key practical limitations (Das, 2003) are discussed below:

(i) The PFs needs a separate filter for each harmonic current, put the limitation in the range of filtering.

(ii) The PFs only passes one component through it at a time namely as a harmonic or fundamental current component.

(iii) The high amount of harmonic current, makes the filter saturated or overloaded. Causing the series resonance with AC source leading the excessive harmonic flow into the PFs.

(iv) Causing the source side harmonics contents amplifications (Hirofumi Akagi & Fujita, 1995), due to parallel and series negative resonance between grid and the filter impedance (J.-C. Wu, H.-L. Jou, K.-D. Wu, & H.-H. Hsiao, 2012).

(v) In AC system, the design parameters of the PFs are depended on the system operating frequency. Therefore, the frequency changes around its nominal value as per the variable load conditions.

(vi) PFs only eliminate frequencies to whom they are tuned, resulting in limited compensation, larger size, and tuning issues.

2.3.3 Shunt active power filters (APFs)

As a solution to the passive filter limitations, active power filters (APFs) are introduced and researched. It consists of an active switching device and passive energy storage devices, such as inductors and capacitors to provide superior compensation characteristics such as voltage and current harmonics, voltages unbalance compensation to utilities, and current imbalance compensation to consumers. Furthermore, it provides mitigation for reactive power, neutral current, changing line impedance, variation in frequency and eradication for voltage notch, sudden voltage distortion, suppressing voltage flicker,

transient disturbances, voltage balance (B. Singh, Al-Haddad, & Chandra, 1999) and power factor improvement (Jovanovic & Jang, 2005).

With the course of time, different APFs topologies and controls methodologies are proposed and progressively investigated by the researcher, as a perceived solution to the critical issues in the high-power loads applications (Hirofumi Akagi, Kanazawa, & Nabae, 1984; Mehrasa, Pouresmaeil, Zabihi, Rodrigues, & Catalão, 2016). The classifications of active power filter are divided into many categories, based in accordance to the subsequent measures. Usually, the circuit structure of the APF includes a voltage source pulse width modulation (PWM) inverter with a DC-link capacitor. As noticed, the current source APF is superior in terms of compensating current dynamics, but the voltage source APF performance is better in terms of filter losses and its capability to reduce PWM carrier harmonics. Figure 2.3 illustrates the basic compensation principle of the three-phase shunt APF to eliminate the current harmonics. Generally, the APFs are installed in a shunt position near to the non-linear load to compensate the effect of harmonics non-linearity. The current harmonics are generated by the non-linear load and travels back towards the source or grid. The function of the APF is to eliminate these harmonics by injecting the reactive current or compensating current at the PCC and protect the utility. It generates the inverse harmonics as mirror image to the load nonlinearities harmonic, canceling current harmonics and leaving the fundamental component to make the source current purely sinusoidal.

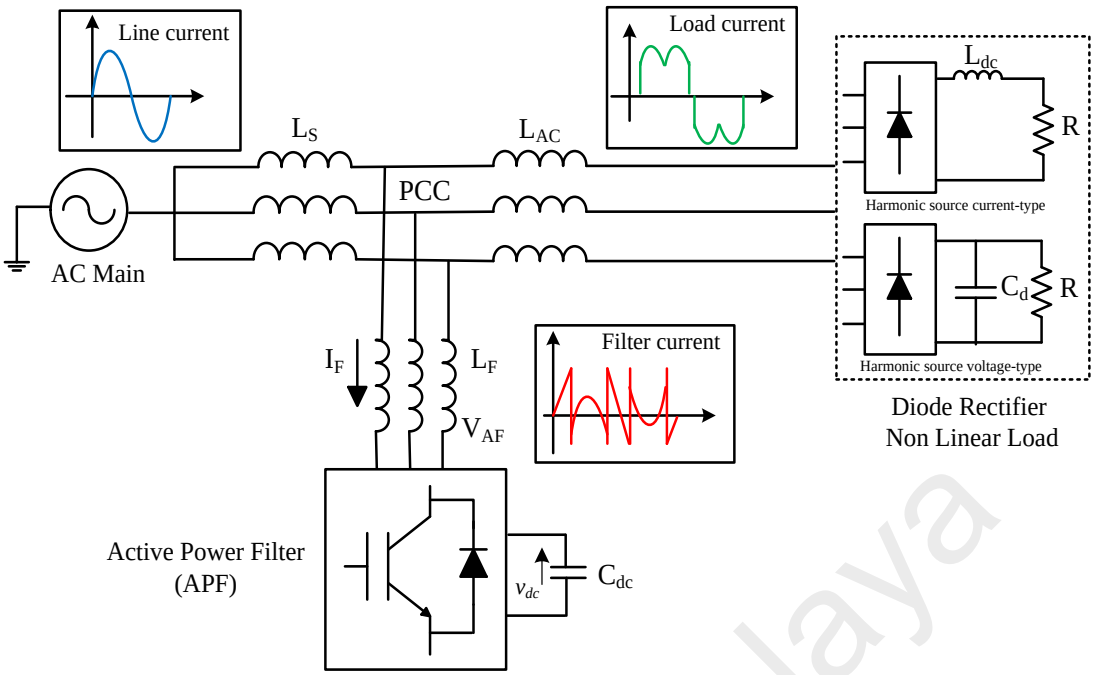


Figure 2.3: Basic compensation principle of the SAPF

2.4 Classification of grid-tied APF

Generally, the active power filters are classified under two categories; DC power filters and AC power filters (Hirofumi Akagi, 1996). The DC-APFs are installed as thyristor configurations for high-power, high-power drives (Gole & Meisingset, 2001) and high-voltage DC system (HVDC). In AC power configuration consists of active solutions, such as active power quality conditioners (APQC), active power line conditioners (APLC), and instantaneous reactive power compensator (IRPC) (Ostroznik, Bajec, & Zajec, 2010a) for current and voltage harmonics. Basically, the shunt APFs is classified under three categories, i.e. topology-type, converter-type and phases-type configurations. The number of phases (wires) are divided into single-phase (two wires), three-phase (three wires), and three-phase (four wires) systems (C. Lascu, Asiminoaei, Boldea, & Blaabjerg, 2009). Altogether, the Figure 2.4, shows the hierarchical structure of active power filter (APF) classification.

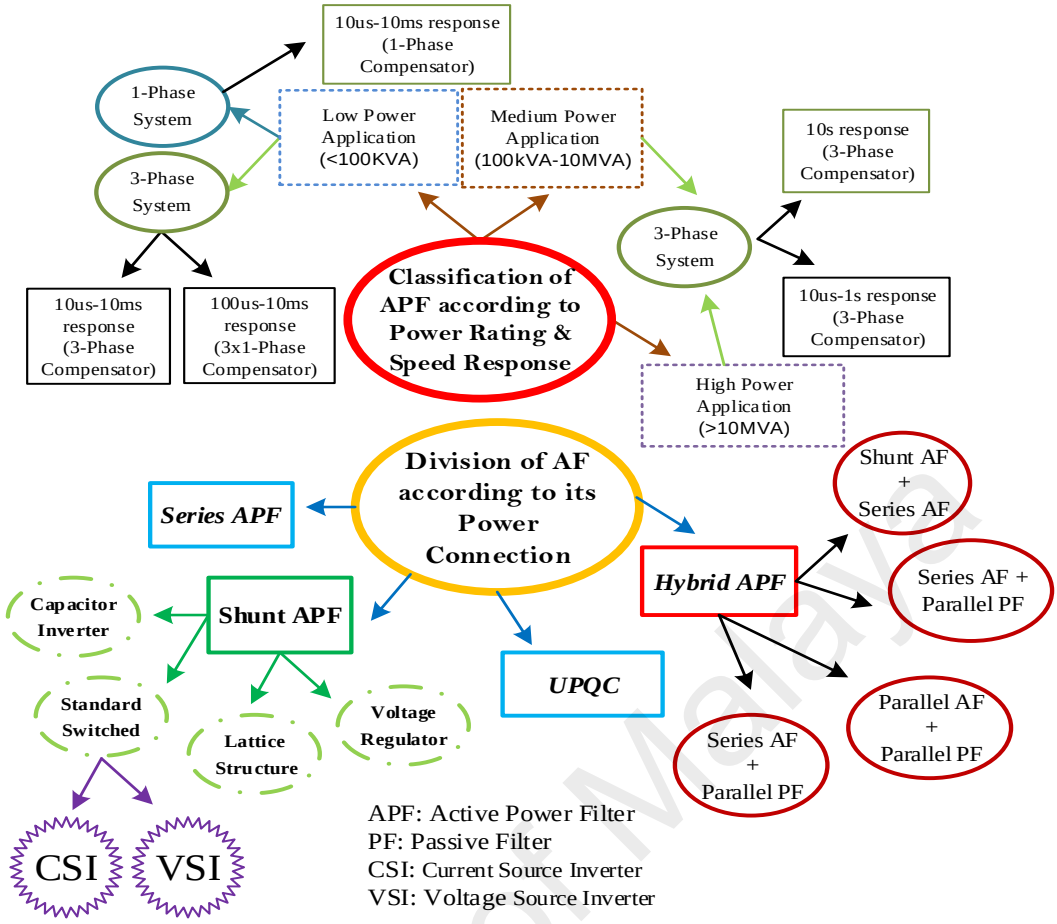


Figure 2.4: Hierarchical structure of active power filter classification.

The topology-based type category is sub classified into three types: SAPF, series APF, and HAPF configuration as shown in Figure 2.5. The series APF reduces the negative sequence of voltage harmonic propagation caused by the system resonance (Z. A. Wang, Wang, Yao, & Liu, 2001), which improves the electrical utilities of terminal voltage. In the energy industry, the increasing demand of high load current generates current rating loss and filter size limitation. Table 2.3 shows the comparison of three APF topologies (B. Singh et al., 1999).

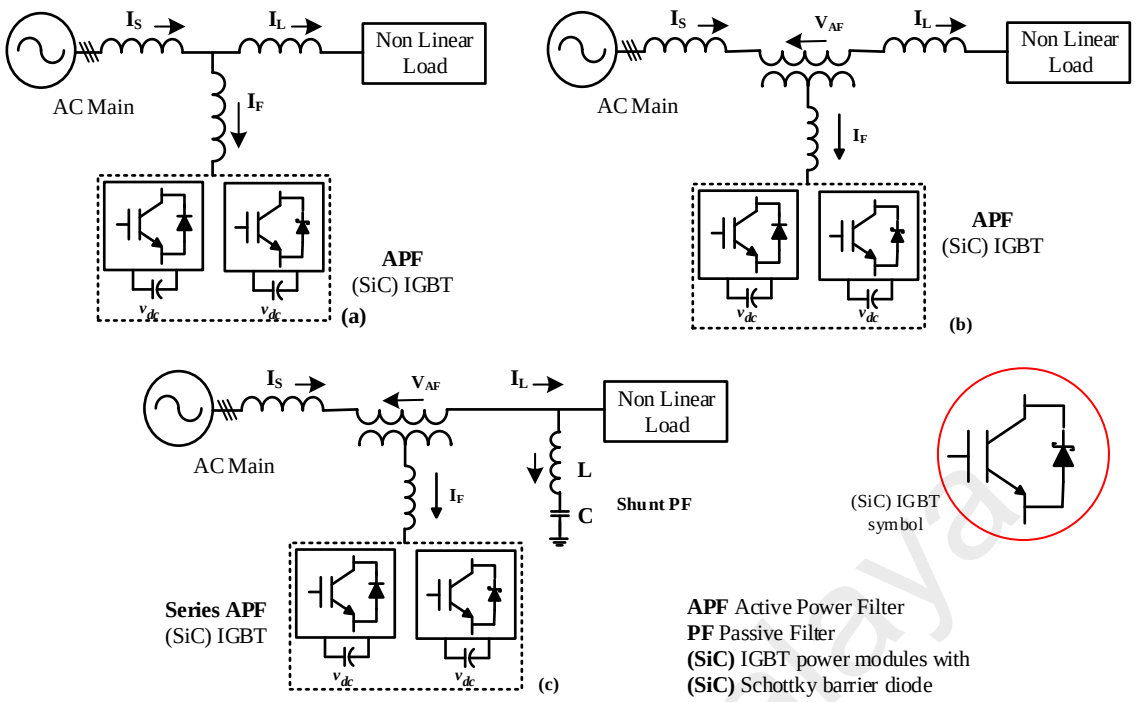


Figure 2.5: (a) Shunt APF (b) Series APF (c) Hybrid APF

Table 2.3: Comparison of APF topologies

Parameters	Shunt Active Filter	Series Active Filter	Hybrid APF
Circuit configuration	Figure 2.5 (a)	Figure 2.5 (b)	Figure 2.5 (c)
Power range			
Small scale	<350 W (power ratings below 100 kVA)		
Medium scale	<350 kW (three-phase systems ranging from 100 kVA to 10 MVA)		
Large scale	<350 kW (systems with ratings above 10 MVA)		
Converter efficiency			
Small	Lowest (up to 98%)		
Medium	High (up to 98%)		
Large	Highest (up to 98%)		
APF operates as	Current source (CSI)	Voltage source (VSI)	Both (CSI/VSI)
Current harmonics	**	-	***
Reactive power	***	-	**
Neutral current	**	-	*
Voltage harmonics	-	***	**
Voltage regulation	*	***	**
Voltage flicker	***	**	-
Voltage sag and dips	*	***	**

High number of "*" is preferred

Three different combinations of HAPF circuit are illustrated in Figure. 2.6 in terms of connections with the main power systems, it is divided into three configurations such as series, shunt and arrangements of series and parallel as UPQC (Kesler & Ozdemir, 2011). The series APF with shunt PF offers high impedance for the harmonic isolation in the medium voltage system as depicted in Figure 2.6 (c). It delivers reactive power, voltage harmonic compensation, and balancing of the three-phase voltages (Hamadi, Rahmani, & Al-Haddad, 2013). On the other hand, SAPF alongside shunt PF is used to eliminate the fundamental reactive power and high order load current harmonics as shown in Figure 2.6 (b). In high-power application, both systems provide reactive power compensation with less switching cost (V. F. Corasaniti, M. B. Barbieri, P. L. Arnera, & M. I. Valla, 2009). In medium- and high-voltage applications, the constant DC-link voltage and grid fundamental voltage are maintained by using series APF together with shunt PF as depicted in Figure 2.6 (a), which effectively reduces the system volumetric size and cost (Salmeron & Litran, 2010).

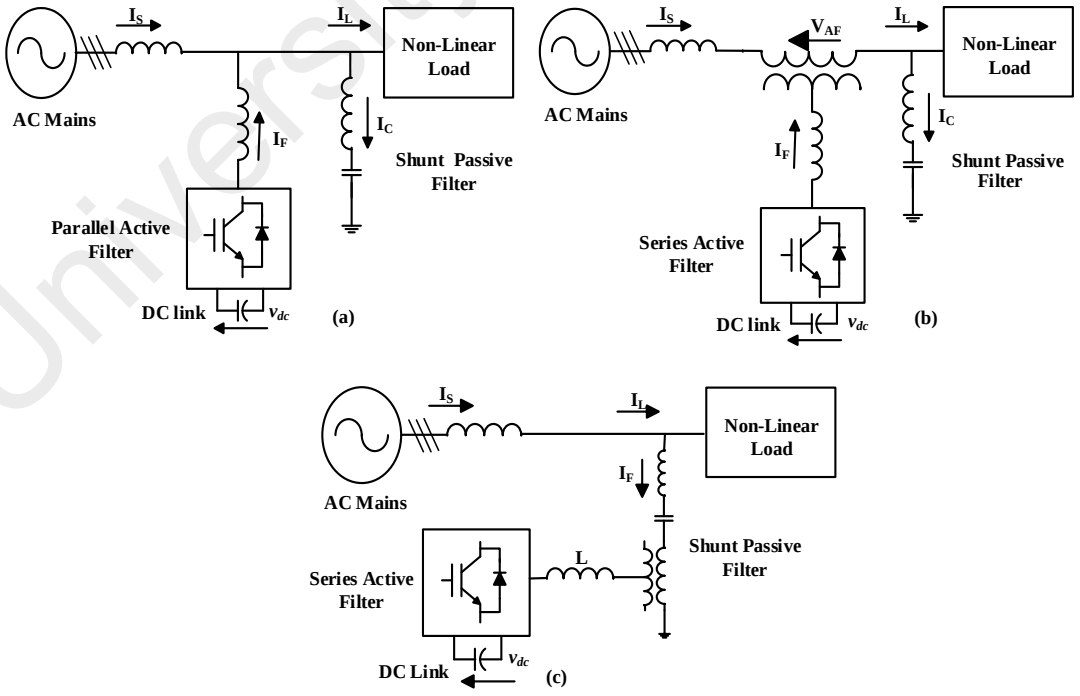


Figure 2.6: (a) Shunt APF with shunt PF, (b) Series APF with shunt PF, and (c) Series APF with shunt PF.

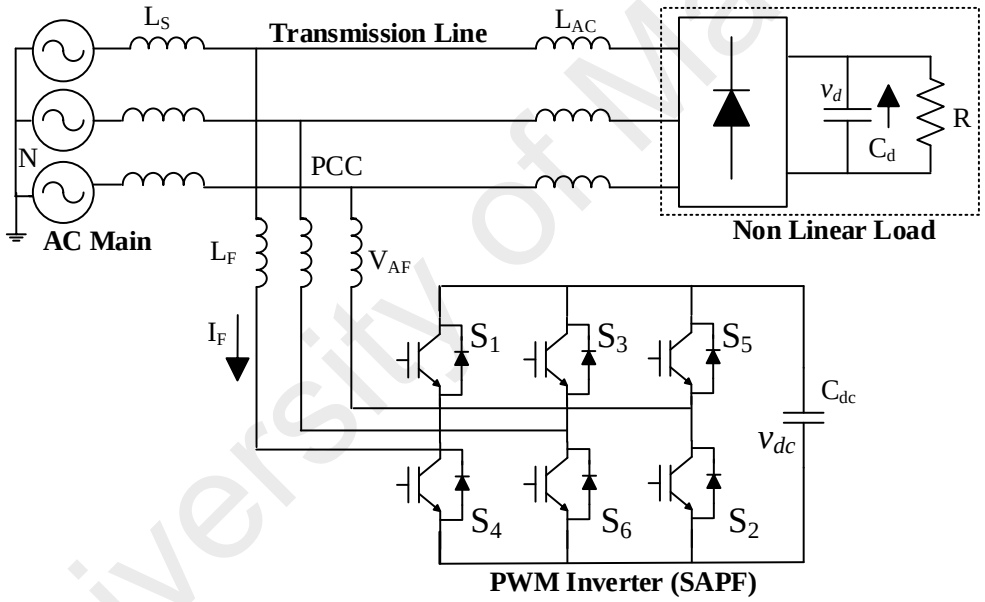
2.5 Conventional three-phase APFs

Generally, a typical APF consists of a voltage source inverter (VSI) of a three-leg bridge structure with a DC-link capacitor (Tangtheerajaroonwong, Hatada, Wada, & Akagi, 2007). Conventional APF topologies require a matching transformer and a large number of active switching devices, such as the IGBT; thus, these topologies are disadvantageous. These considerations result in heavy weight and costly system and are therefore undesirable. In (L. Asiminoaei, Lascu, Blaabjerg, & Boldea, 2007; Inzunza & Akagi, 2005; Rahmani, Mendalek, & Al-Haddad, 2010; S. Srianthumrong & Akagi, 2003; Verma & Singh, 2009), a transformer-less three-phase pure SAPF is integrated with diode rectifier non-linear load.

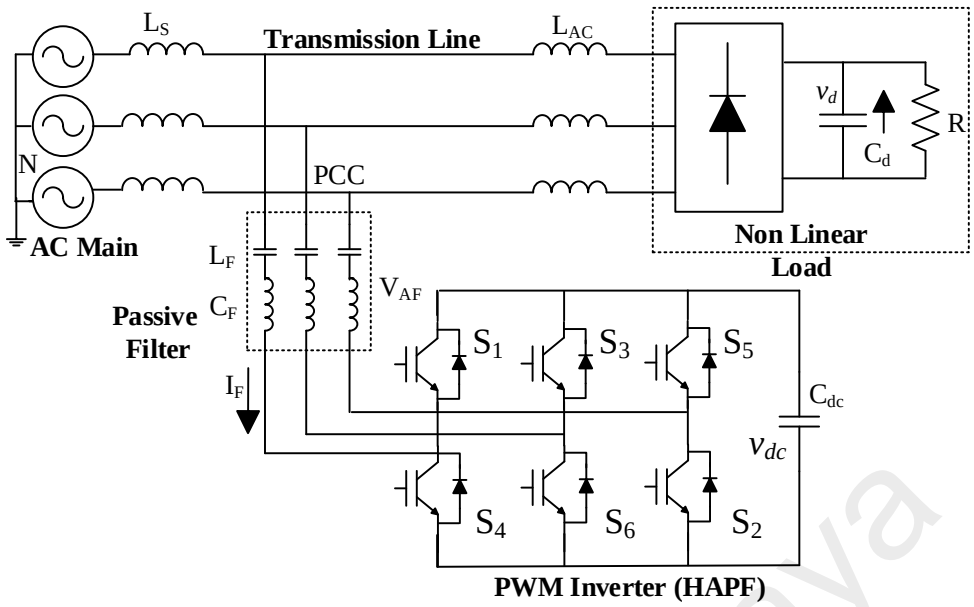
The power circuit of the conventional shunt active power filter (SAPF) is depicted in Figure 2.7 (a). The SAPF is connected through the coupling inductor at the point of common coupling (PCC) in the shunt position with the power distribution system. This topology is composed of a six-switch three-leg full-bridge VSI with a DC-link capacitor and coupling inductors. The designed AC-link inductors are implemented to shape the input current and compensate the current harmonics. As notice, the AC-link coupling inductors offers the same inductance value as of the filters inductors L_F (Inzunza & Akagi, 2005). For harmonic compensation in a three-phase system, the SAPF generates the compensating current by uniting all the single-phase harmonic components and fundamental reactive components of the load currents. The filtering compensation is performed by injecting the compensating current in phase with the utility voltage at the PCC into the power distribution system.

The HAPFs are the low-cost filters system with the combination of passive and active filters devices to compensate the harmonic and voltage regulation (J. C. Wu, H. L. Jou, K. D. Wu, & H. H. Hsiao, 2012). In HAPF configurations, the series AC-link coupling

inductors of shunt APF is replaced with the series inductors and capacitor set (LC Passive filter) as shown in Figure 2.7 (b). It helps in reducing the power rating of voltage source inverter (VSI), along with DC-link voltage rating. During the filtering stage, both the filters are controlled in such a manner that the low-order harmonics are eliminated by the shunt APF operation (L. Qian, D. A. Cartes, & H. Li, 2008), while the higher frequency harmonics are cancel by passive filters (Salmeron & Litran, 2010). However, the installed series PFs produces a unavoidable fundamental leading current flow into the APF system, furthermore limiting the reactive power compensation capability (due to fixed LC values), which is the main disadvantage of the conventional HAPF systems.



(a)



(b)

Figure 2.7: The connection diagram of 3-phase 3-wire APF VSI (a) Pure Shunt APF circuit. (b) Hybrid shunt APF circuit.

2.6 Reduced switch count as cutting-edge technology

The new growing trend in the field of power electronics targeting to minimize the number of the power semiconductor components like IGBTs switches, aiming to determine the overall lower price of the power converter devices. To design a cost-effective topologies based on the reduced number of semiconductor devices in the range of few ten kilowatts and above, is always attractive to the researcher. Based on these facts and attentions the transformer-less APF system is showing an important development to a mature level. Furthermore, with the advancement and development in the microprocessor, controllers and fast switching devices, mainly proficient APF systems have been proposed with high rated megawatt range value. Moreover, the reduced switch count inverter topologies limit the cost and size, the switching losses, and the complexity of the control structure and algorithm and interface circuits. As noticed, new trends in the efficient modulation techniques to guarantee the high reliability, fast transient and dynamic response, low THD, and high stability against the sudden load variations. Further

less sensitive to DC-link voltage fluctuations, low AC currents THD, low distortion in the uncontrolled inverter phase.

New trends in the hybrid APF topologies, aims in the developed of a more advanced APF system, with less rated power components systems and added dual functionality. Particularly, in low-power range industrial applications such as power filters, variable-speed motor drives, uninterruptible power supply (UPS), and static frequency changers, etc. The cost reduction is an important aspect in design of the power converter (Lohia, Mishra, Karthikeyan, & Vasudevan, 2008). A reduced number of power converter or inverter is tested as describe in Table 2.4 (Baroudi, Dinavahi, & Knight, 2007), illustrating the comparison between the different DC-AC inverters in detail to each attributes and parameters.

Table 2.4: Comparison of different power DC-AC inverters topologies.

Topologies	Electrical isolation	Efficiency (%)	Advantages	Disadvantages
-Single bus inverter with two paralleled half bridge	No	-	-Minimum component count	-Large DC filter components
-Dual bus inverter with two split half bridge single	No	-	-Reliability and flexibility	-High component count
-Phase (3 wire) inverter	Yes	-	-Small passive component	-Complex control; for non-isolated circuit
-Dual phase inverter with transformer	Yes	-	-Boosting capability	- Higher cost and size
-Three-phase PWM inverter	Yes	~98%	-Simple design and control	-
-High frequency link inverter	Yes	~96%	-Boosting capability	-Highly complex; higher cost and size
-Z source inverter	No	~98%	-Boosting capability; save cost, no need for extra DC-DC converter	-Complex control; current stress is high

2.7 Reduced-switch-count APF inverter topologies and their control

In recent years, power electronics are being developed with the aims of reducing the system volumetric size and cost and improving the system reliability by reducing the number of switching devices in power converters. Depending on the total number of switches or switch reduced count configuration, modified APFs inverters are classified as AC-AC power converter, parallel inverter and split DC-leg inverter topologies. The complete cycle of reduced switch count integrated into grid application, starting from twelve to three switches is explained in Figure 2.8.

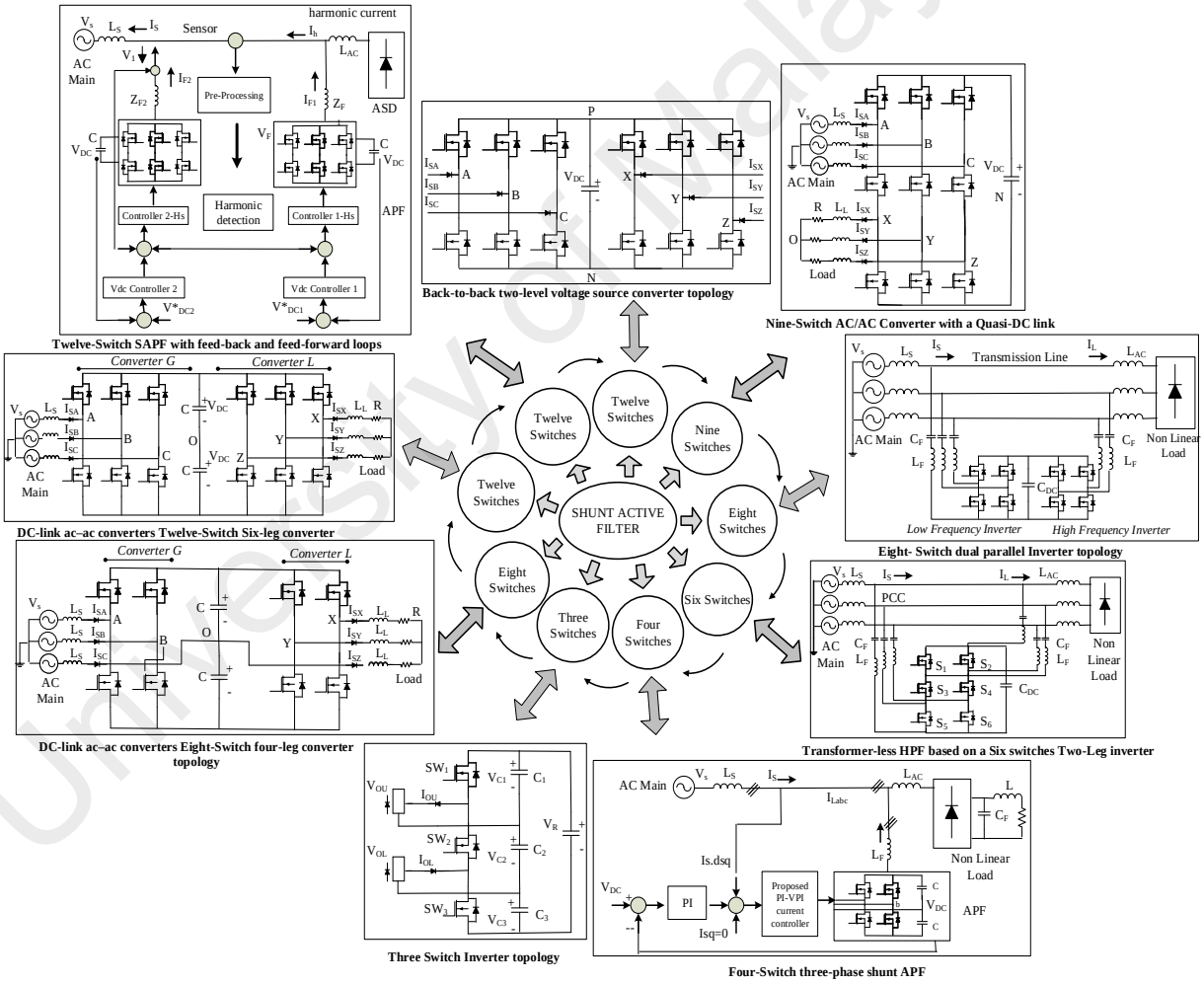


Figure 2.8: Overview of reduced switch-count inverter topologies in grid-application.

2.7.1 AC–AC power converter

In three-phase three-wire (3P3W) AC-AC inverter topology, the voltage source inverter (Kolar et al., 2011) is connected in parallel with the DC-link capacitor as illustrated in Figure 2.9. The circuit represents the letter "H" (Patnaik & Panda, 2013), so-called H-bridges converter circuit connected with a single DC-link capacitor (C_{dc}), consuming a different numbers of switches installed in series, shunt and hybrid combination of SAPF systems. The principle of operation is to inject the compensating current into the AC distribution network at the PCC through a coupling AC inductors or transformers.

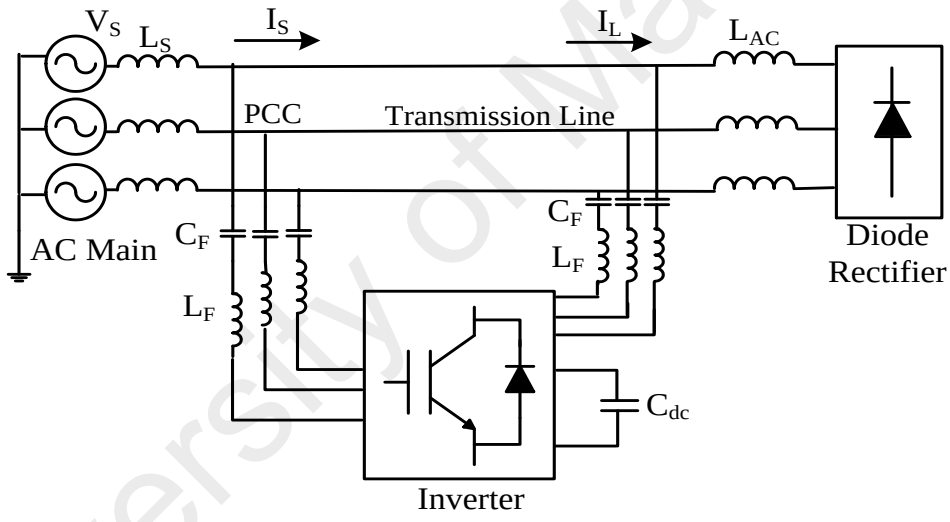


Figure 2.9: AC–AC inverter topology.

2.7.1.1 Three-phase (three-wire) APFs

A three-phase APF system consists of four-switch converter (J. C. Wu et al., 2007) and eight-switch converter configurations (B. R. Lin & Ou, 2004). It uses a two-arm bridge inverter and a DC-link capacitor to eliminate the harmonics, reactive power problems, and subsequent variations in the DC-link voltage (El-Kholy, El-Sabbe, Ei-Hefnawy, & Mharous, 2006; B. R. Lin, Lee, & Yang, 2003; B. R. Lin & Ou, 2004; B. R. Lin & Wei, 2003), aside from removing the current sensors in several applications

because of common mode current strategy. This design uses four switches to test the two-leg bridge inverter by connecting the removed leg with the negative terminal of the DC-bus. Apart from reducing cost, this topology also offers less complex structure, highly reliable filtering compensation, and controlled and balanced DC-link voltage. The only constraint in high-power applications is that it requires high-voltage stress switches because of the large turns on resistance. However, a soft switching converter technique is used to reduce one-half of DC bus voltage and to increase the total output power (F. X. Liu, Yan, & Ruan, 2010).

The two-clamping diodes, four MOSFETs, one flying capacitor, and magnetic cores reduce the PWM controller volumetric size and cost compared with the conventional three-level converter. By controlling the output voltage for leading and lagging switching operation at the secondary side; two center-tapped rectifiers reduce the current rating of the rectifier diodes, output filter inductors, and transformer windings (B. R. Lin & Chao, 2013). It results in reducing switch voltage stress, zero voltage switching (ZVS), and load current sharing. Three-phase conventional matrix converter requires eighteen IGBT switches with complex switching scheme. Fifteen switches with reduced-count IGBT switch converter is presented in (Kolar, Schafmeister, Round, & Ertl, 2007).

Presenting a better reduced switch count, a unidirectional power flow twelve IGBT switches is designed in an ultra-sparse matrix converter (Schonberger, Friedli, Round, & Kolar, 2007). Overcoming the limitation of three-leg nine-switch inverter (C. W. Liu, Wu, Zargari, Xu, & Wang, 2009) as depicted in Figure 2.10, the improved two-leg six-switch inverter is presented in (Limongi et al., 2015). This topology consists of a three-phase six-switch bridge inverter connected in series with a passive filter (PF). The low-power rating inverter compensates the current harmonics at the PCC flowing into the utility source and improves the filtering characteristic of the series LC PF. Figure. 2.11

demonstrates an HAPF topology connected to a three-phase load without using the matching transformer consisting of a two-leg six-switch reduced inverter connected in series with two passive LC filters. Tuned at different harmonic frequencies, it provides better compensation than both the conventional HAPF topology and the three-phase VSI topology.

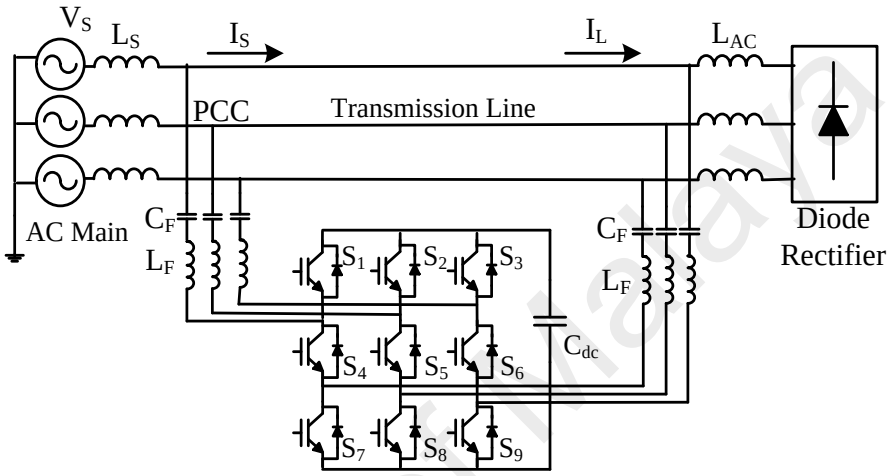


Figure 2.10: Nine-switch AC–AC inverter circuit.

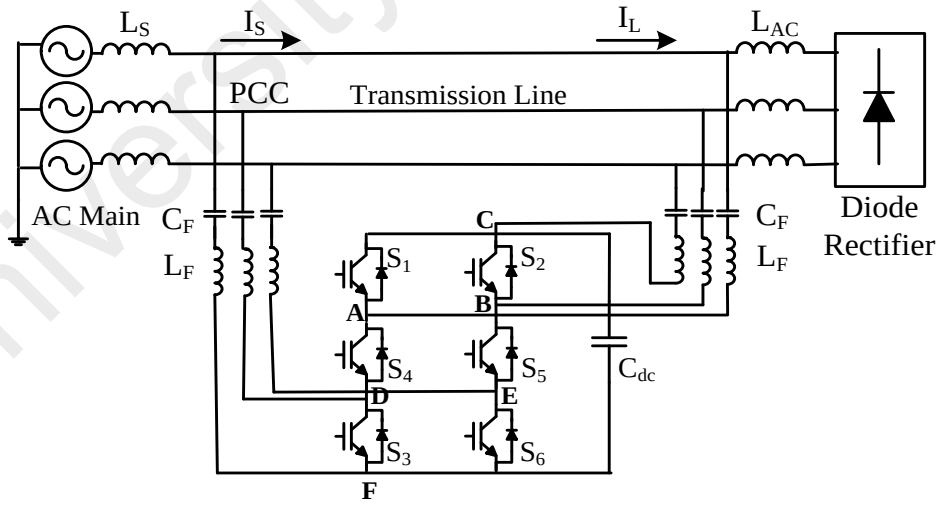


Figure 2.11: Six-switch AC–AC inverter circuit.

A combination of feedback and feed-forward controls loops is adopted as an advance control scheme (H. Kim & Sul, 2005; Limongi et al., 2015; Bhim Singh et al., 2004). Figure 2.12 illustrates the control block diagram, consisting of three subsystem to control

each unit including the top inverter unit, the bottom inverter unit and the shared control unit. Each PFs tuned at different harmonics frequencies to mitigate the 5th, 7th harmonics at the top inverter, and 11th, 13th harmonics at bottom inverter and also keep the balance DC-link voltage compensation (A. Luo, Xu, Fang, Wu, & Wu, 2010).

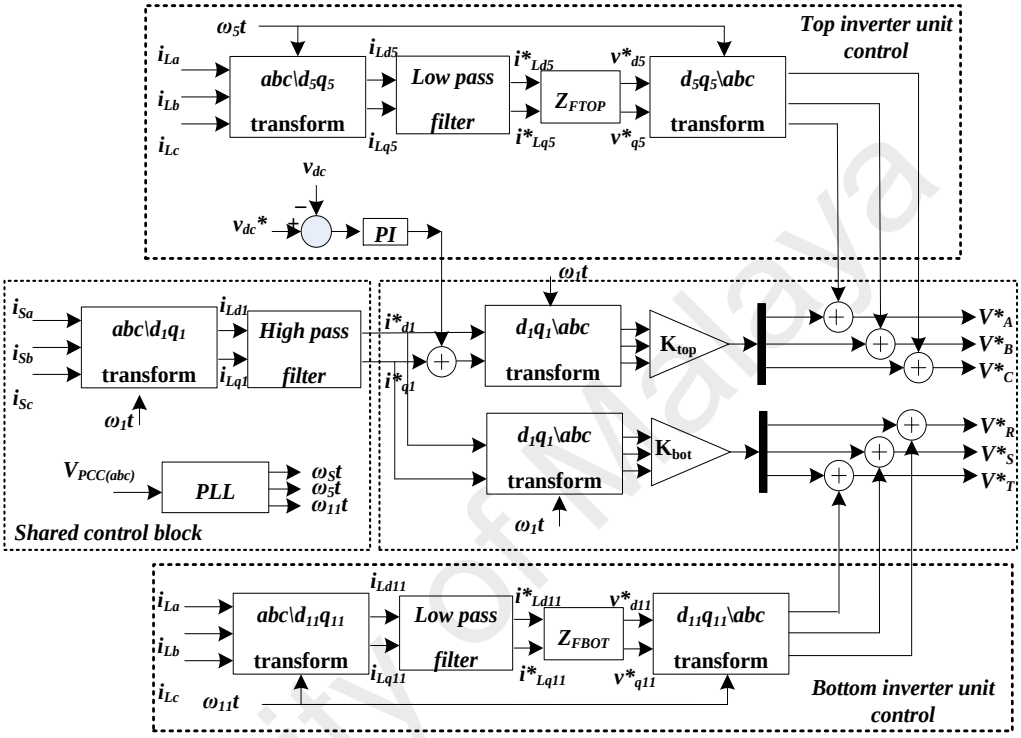


Figure 2.12: Control block of the proposed HPF based on SSTL inverter.

To reduces the DC-link current through the DC-side of the system, a capacitor is installed in between the DC-link poles and the PCC (T.-L. Lee, Wang, Li, & Guerrero, 2015). However, the shared control unit operates with PLL scheme, consists of a simple, and robust voltage pre-filter. It generates a quasi-square wave proofing the advanced compensation and harmonic contents as compare to the conventional APFs systems. Additionally, the H-bridges modular structure type reduces the manufacturing cost, production speed fast and high reliability. The controller needs to track a single capacitor voltage, which reduces the complexity of the voltage regulation, extra need of the voltage sensors in terms of multi-level inverter configurations.

Another pair of reduced-switch-count dual-leg six-switches and the single-leg three-switch leg structure topologies are connected to a two individual single-phase loads (Fatemi et al., 2013; Khadkikar, Chandra, Barry, & Nguyen, 2011). Moreover, the single-leg inverter operates as a two half-bridge inverters with minimum achievable three switches split capacitors technique as depicted in Figure 2.8 (three-switch inverter topology). Both systems operate independently as a two full-bridge and half-bridge inverters connected with single-phase and three-phase critical loads.

2.7.2 Parallels inverter APF

A dual-terminal converter topology offers researchers the capability to reduce switch count configurations (A. Bhattacharya et al., 2012; Fatemi et al., 2013; C. W. Liu et al., 2009). Figure 2.13 illustrates the three-phase three-wire parallel inverter topology, i.e. rectifier and inverter are coupled with a parallel DC-links storage device in the APF topology.

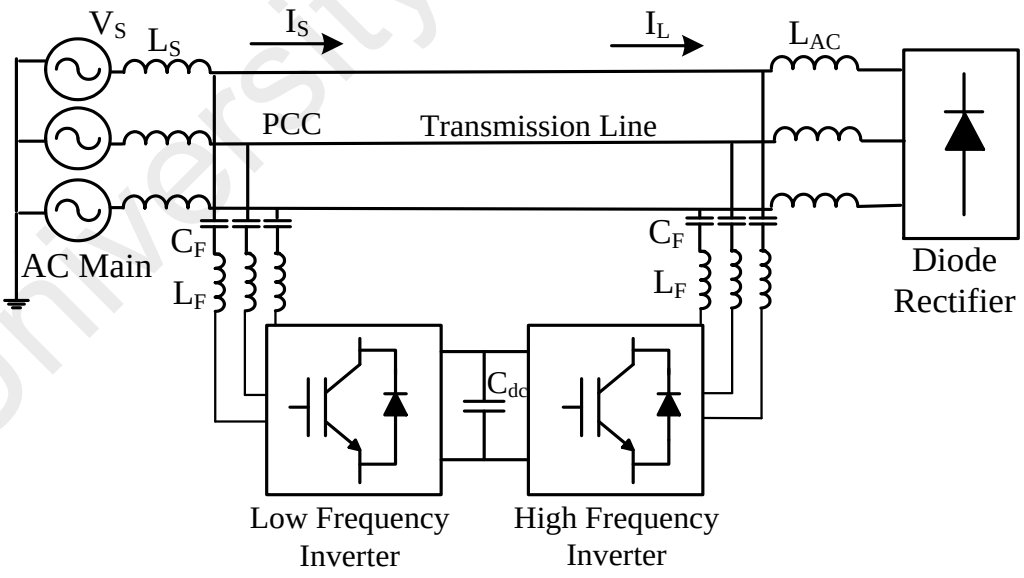


Figure 2.13: Parallel inverter topology.

The main advantage of this configuration is that it improves the APF compensation capability. However, at the cost of a high amount of the switching devices. Basically, the

conventional two coupled back-to-back H-bridge inverter is a well-established low voltage configuration used in many industrial applications (H. Wang, Liserre, & Blaabjerg, 2013), usually consists of a twelve switches structure. The enhanced configuration eliminates the four switches from each inverter, thus reducing the total number of switches to eight, the scheme adopted to eliminate the single leg in each power converter (L. Asiminoaei et al., 2007; A. Bhattacharya et al., 2012; A. Bhattacharya, Chakraborty, C, Bhattacharya, S., 2009), by connecting the third phase to the negative terminal of the individual VSIs (K. Karanki, G. Geddada, M. K. Mishra, & B. Kumar, 2013) as shown in Figure 2.14. However, connecting the removed leg or phase with the split-capacitor leg causes voltage balancing problem across the DC-link capacitor. Also, improving the system reliability and decreases the voltage stress across the active switches. Larger DC-link voltage variations can be solved by operating the power converters at the same frequency to stop the fundamental current flowing in the DC-link bus.

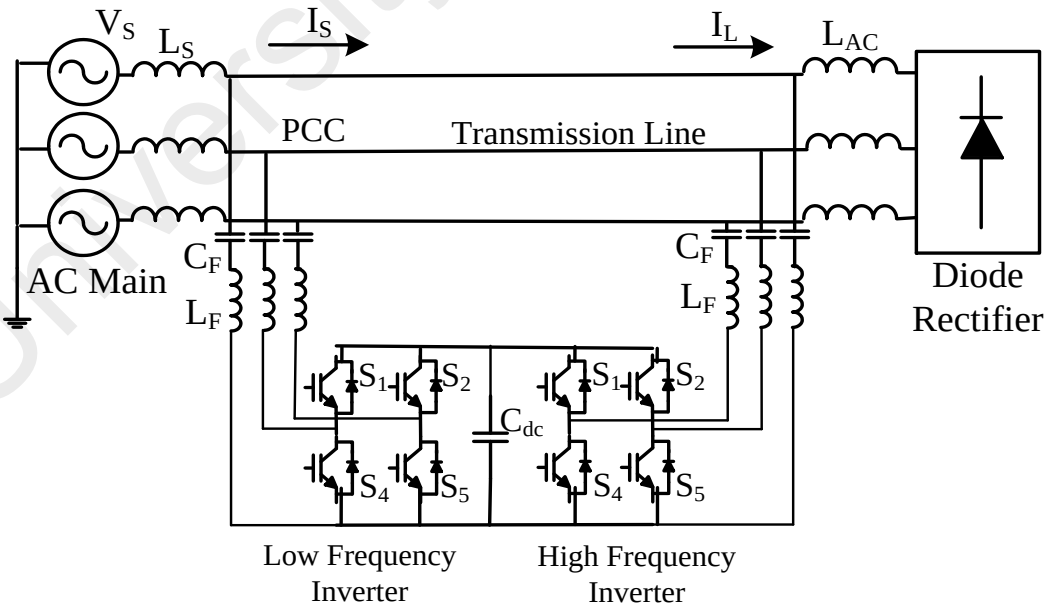


Figure 2.14: Eight-switch parallel inverter circuit

To stabiles the voltage balance across the DC-link capacitors, a larger rated value DC capacitor is needed for the higher rated dynamic loads system, additionally for harmonics and reactive power compensation. However, the DC-side energy storage component is the main limitation factor contributing to the circuit failure. The DC energy storage components are the largely fails components in a power electronics circuit, also expensive and contribute to shorten the converters life time (Y.-M. Chen, Wu, Chou, & Lee, 2008). Many factors contributed to its high failure rate such as dissipation of heat, degradation of energy parameters and higher value of voltage capability. The DC energy storage component in the arrangement of the aluminium electrolytic capacitors which act like a filters and energy buffers to the AC voltage ripples in the APFs system. The ageing of the aluminium electrolytic capacitors increase its internal resistance, contributes to most frequently be damaged in operation, expensive in cost, size and weight. However, the capacitor is a prominent cause of the power converter failure (Venet, Perisse, El-Husseini, & Rojat, 2002).

The reduction of switches leads to more complex control and structure design to stop the flow of zero sequences current circulating in between the two power converters. The best solution is to install the transformer or isolate the DC capacitors (A. Bhattacharya, Chakraborty, C, Bhattacharya, S., 2009). The parallel inverter topology exits limitations in terms of oversized DC-link capacitor, restricted amplitude sharing and limited phase shift in the output terminals. To overcome the issue of switching losses and electromagnetic interference due to the high switching frequency, a soft switching technique such as zero voltage transition (ZVT) and zero current transition (ZCT) schemes is adopted (Mohammadi & Farzanehfard, 2015). A control technique scheme is implemented based on feed forward and feedback loops, as explain in Figure 2.11. The low-frequency inverter (LFI), tuned at 550 Hz, is design to mitigate the lower-order harmonics and also maintain the DC-link voltage constant and reactive power demand on

the system. In the arrangement, the high-frequency inverter (HFI) tuned at 750 Hz, eliminates the remaining higher-level harmonics. The control block functions in two loops modes, such as a feed forward loop to control the LFI and to improve the dynamic response from the system, and feedback loop to operate the HFI, also for higher steady-state and harmonic compensation results. The clerks and parks transformation technique is adopted to find the cosine and sine components and by using the synchronous reference frame method to generate the reference current for the parallel APFs inverters topology (D. Chen & Xie, 2004). Table 2.5 shows the comparison in between the main stream power converter topologies discussing different topology parameters (Tripathi, Tiwari, & Singh, 2015).

Table 2.5: Comparison of mainstream power converter topologies.

Converter topology Features	Diode rectifier	2L-B2B VSC	ZSI	Multi-level converter	Matrix Converter	Nine switch AC-AC converter
Need controlled switches	None	Less	Less	Large	Large	Least
Circuit configuration	Simple	Simple	Simple	Complex	Complex	Simple
Cost	Very low	Moderate	High	Very high	high	Low
DC-link capacitor	Yes	Yes	Yes	Yes	No	Yes
Operational stages	Two	Two	Two	Two	One	One
Waveform quality	Good	Better	Better	Best	Better	Depends
Harmonic distortion	High	Moderate	Low	Least	Low	Depends
Switches losses	None	High	High	Low	Low	High
Conduction losses	Low	Low	Low	Highest	High	Low
Reliability	High	Low	High	Low	High	Low
Bi-directional power flow	No	Yes	Yes	Yes	Yes	Yes
Control complexity	Easy	Moderate	Moderate	Most complex	More complex	complex

2.7.3 Split DC-leg inverters

The split DC-link topology provides a neutral common point for three-phase VSI or 3P3W and three-phase four-wire (3P4W) systems (Cursino Brandão Jacobina, de Freitas,

& Lima, 2007; J. Kim, Hong, & Nam, 2009; Miveh, Rahmat, Ghadimi, & Mustafa, 2016). It split the single leg to provide a neutral path or midpoint connection by using a two pair of capacitors (B. Jacobina, de Rossiter Correa, Lima, & AM Cabral da Silva, 2003; Liang, Green, Feng, & Weiss, 2009) as depicted in Figure 2.15. As noticed, the three-leg split capacitor and four-leg VSI-based topologies are the most demanding configurations for the 3P3W APF system. However, for high-power applications the two-level VSI configuration is inappropriate for filtering and harmonic compensation. In four switch (B4) inverter (Z. Luo, Su, Sun, Zhang, & Lin, 2016; Tripathi et al., 2015; Welchko, Lipo, Jahns, & Schulz, 2004) uses the four number of switches and four number of diodes as compare to the practical six switch inverter (B6) (Miveh et al., 2016; Van Der Broeck & Van Wyk, 1984). The split DC-link topology uses fewer numbers of semiconductors devices, which helps the neutral current to comprise small fundamental AC components value. Table 2.6 explain the performance comparison of split DC-leg APF with the conventional APFs topologies (Khadkikar, Chandra, & Singh, 2011).

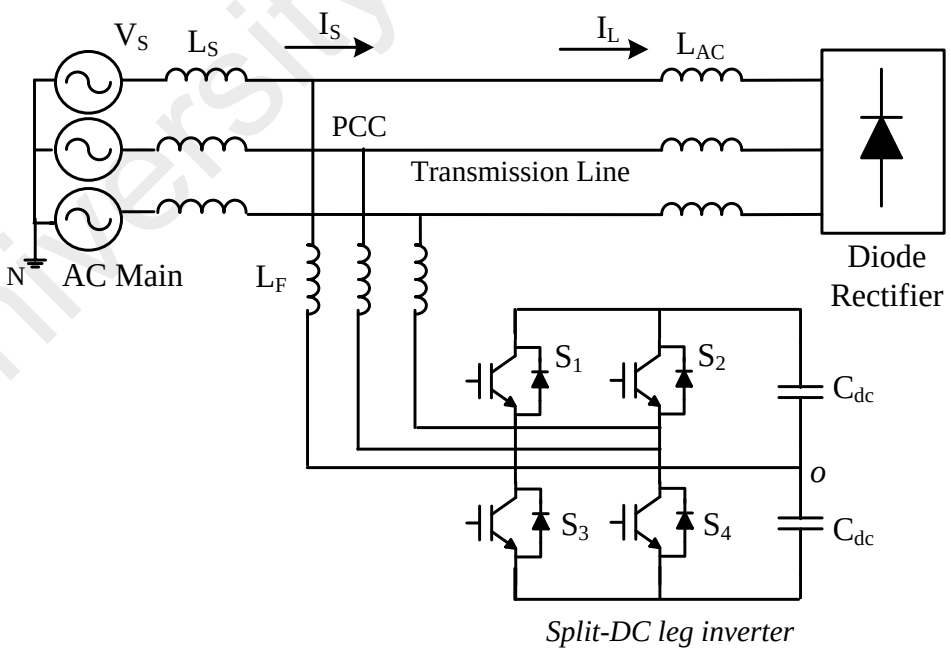


Figure 2.15: Four-switch dc-split voltage source inverter topology.

Table 2.6: Performance comparison of split DC-leg APF with the conventional APFs topologies.

Split DC-link topology		Conventional topology	
Advantages	***Disadvantages***	***Advantages***	***Disadvantages***
Simple design	Unequal voltage sharing in between the split capacitors legs	Handle unbalanced and nonlinear conditions	Need two or many extra switches
Converter switches	Need an expensive capacitors	Low DC-bus voltage	Complicated control strategy
Simple and fast current tracking control	Unbalanced and nonlinear loads reason a split voltages perturbation	AC output voltage can be greater [about %15] than the output of split DC-link topology	-
Other features	Need a neutral point balancing technique	Lower ripple in the DC-link voltage	-

The drawback in this topology is the need of expensive and a large capacitor value to achieve equal voltage sharing between the split capacitors (E. C. dos Santos, Jacobina, Dias, & Rocha, 2011). Under severe unbalanced and nonlinear conditions a large amount of neutral current flows through the neutral path causing the perturbation in the control scheme. However, due to its circuitry this topology utilizes less expensive capacitors to provides a maximum available line-line peak voltage ($v_{dc}/2$) to maintain a lower ripple DC-link voltage. The dual bridge inverter practices B4 technique and eliminates the variation in the DC-link capacitors current and voltage. In three-phase four-wire (3P4W) inverters the AC voltage is 15% higher than the split DC-link inverters (Mechouma, Azoui, & Chaabane, 2012). It concluded that the 3P4L inverter (F. Zhang & Yan, 2009), shows superior performance under the unbalanced and nonlinear conditions at the cost of complicated controls scheme (Bhim Singh et al., 2004). A pulse-width modulation PWM or space vectors modulation SVM techniques are adopted to generate the reference signals for the PWM inverter. The main limitation in the split DC-link power converter topology is as follows;

1. In four switched B4 inverters, the third phase is connected clearly to the middle point or neutral point of the DC-link capacitors (Welchko et al., 2004). As noticed, the DC-bus current straight chargers one of the capacitors and discharge the other. The dynamic unbalances current and voltage loading in between the capacitors discharge at a faster rate than the other, causes a more current ripple in the imbalance output waveform. To prevent the distortion, unbalance three phase currents and fluctuations of the DC-bus voltage across the inverter output, a larger DC-link capacitors are installed (J. Kim et al., 2009).
2. In three-phase system, a phase circulating current flows through the DC-link capacitors (Blaabjerg, Freysson, Hansen, & Hansen, 1997). So they are exposed to low frequency harmonics, which creates the limitation of utilizing higher DC-link capacitors valued.

2.8 Performance comparison between the reduced-switch-count APFs topologies

Performance comparison among the three different reduce-switch-count topologies is summarized in Table 2.7. They are evaluated based on amount of reduced switches, efficiency, component ratings, and THD. It was observed in studies (C. W. Liu et al., 2009) and (Trinh & Lee, 2013) that they have moderate efficiency because of a high number of inverter switches. However, three switches had the highest estimated efficiency (94%–96%), although it had high-rating components (Fatemi et al., 2013). As noticed, the reduction of switches and inverter legs highly affects the voltage rating and DC-link capacitor size. In fact, distributed between the inverter legs, the conventional inverter topology demonstrates a low DC-link voltage as compared with reduced–switch-count topologies (C. W. Liu et al., 2009). To compensate for the effect of reduced switches, the DC level is aided by the combination of series capacitors, thus increasing

the number of active and passive components (Trinh & Lee, 2013), which contributes to higher system cost (Limongi et al., 2015).

Another parallel inverter or back-to-back topology has been proposed in study (L. Asiminoaei et al., 2007), which tested low-rating components to generate high output power (15 kVA) and mitigate harmonics. In practice, report (Daniel & Abirami, 2013) demonstrated the highest estimated efficiency based on the design of eight switches as compared with other configurations. A greater number of switching components produces more switching and conduction losses (A. Bhattacharya et al., 2012), thereby lowering the inverter efficiency (L. Asiminoaei et al., 2007). In the evaluation stages, research (A. Bhattacharya et al., 2012) demonstrated a medium level of efficiency with extra single DC capacitors as compared with study (L. Asiminoaei et al., 2007). However, the APF mitigate the grid-connected harmonics in report (Daniel & Abirami, 2013) to maximum achievable level of 0.03% (grid current) as compare to results reported by other studies (L. Asiminoaei et al., 2007; A. Bhattacharya et al., 2012).

A recent advancement for the split DC-leg inverter topology is dynamically researched and presented in existed previous report (C. B. Jacobina, Correa, Lima, & da Silva, 2003); maximum efficiency is achieved with the grid current THD values of 0.8% and 0.6%. Compared with another report (Cursino Brandão Jacobina, De Freitas, Da Silva, Lima, & Ribeiro, 2006), this topology has 6 switches and 28 total estimated components with medium efficiency. The authors modeled the APF system for low efficiency (L. Asiminoaei, Aeloiza, Enjeti, & Blaabjerg, 2008), this work aimed to reduce the number of inverter switching components (15 components), with a THD value of 2%. However, in grid-connected PV and WECs with AFP, the target of reducing the number of switches is directly related to the output DC-link capacitor value and high-power passive devices.

Table 2.7: Comparison of reduced-switch-count AC–AC, Parallel Inverter and Split DC-leg inverter topologies.

Author	(Fatemi et al., 2013)	(C. W. Liu et al., 2009)	(Trinh & Lee, 2013)	(Limongi et al., 2015)	(A. Bhattacharya et al., 2012)	(L. Asiminoaei et al., 2007)	(C. B. Jacobina et al., 2003)	(Cursino Brandão Jacobina et al., 2006)	(L. Asiminoaei et al., 2008)
Topology	One leg	Three leg	Two leg	Two leg	H-bridge	Full bridge	Four, Three, Five legs	Five leg	Six leg
Modulation/control	SPWM/EF-DF	SPWM	PI/VPI current	SPWM/PI	SPWM/PI/FF-FB	SPWM/PI/FF-FB	SPWM	SPWM	SPWM/PI
Capacity (kVA)	2.5	5	1.5	1.8	3 kW	15 kVA	~1.5 kVA	~1.5 kVA	5 kVA
Switching frequency (kHz)	6	3.2	10	20	550 Hz and 20 kHz	12.6 kHz	5	10	12
Conventional topology	6	12	6	9	12	12	+	12	12
Reduced switch count	3	9	4	6	8	12	8, 6, 10	10	12
No. of filter inductors	1	3	3	6	5	6	-	3	12
No. of filter capacitors	+	0	0	6	5	6	3	+	6
No. of DC capacitors (μF)	3@2200	1@2350	2@2000	1@4700	1@4700	2@4.4mF	2@1000	2@2200	1@2.2mF
THD %	60 - 1	64.74 – 1	24.4 - 1.89 (RL) 30.2 - 1.97 (RLC)	36 - 3 (no load) 43 - 5.6 (load)	4.70, 23.50	1.26, 1.11	0.8 (8 Switch), 0.6 (6 Switch)	1.54 (1st) 0.8 (2nd)	27 - 2
Estimated efficiency	High	Medium	Medium	Low	Medium	Low	High	Medium	Low
DC-link voltage (v_{dc})	200	320	420	120	26	400	100	200	250
Grid interface (Transistor)	3 VSI	6 VSI	4 VSI	3 VSI	4 VSI	6 VSI	2 VSI, 4 VSI	4 VSI	12 VSI

2.9 APFs CONTROL TECHNIQUES

The primarily operation of the power converter depends on the control modulation strategies for controlling the parameters like switching losses, harmonic reduction, THD of the output current or voltage, frequency and phase synchronization, dynamic response to the sudden transients, proper current distribution, and power factor correction. Generally, the APFs control is divided into two categories specifically the reference signal estimation technique and control technique respectively (Hirofumi Akagi, 1996; Angulo, Ruiz-Caballero, Lago, Heldwein, & Mussa, 2013; El-Habrouk, Darwish, & Mehta, 2000; Mattavelli, 2001). The reference signal estimation technique is classified into two sub-category specifically current or voltage reference synthesis and current or voltage reference calculation (Badihi, Zhang, & Hong, 2015), as shown in Figure 2.16.

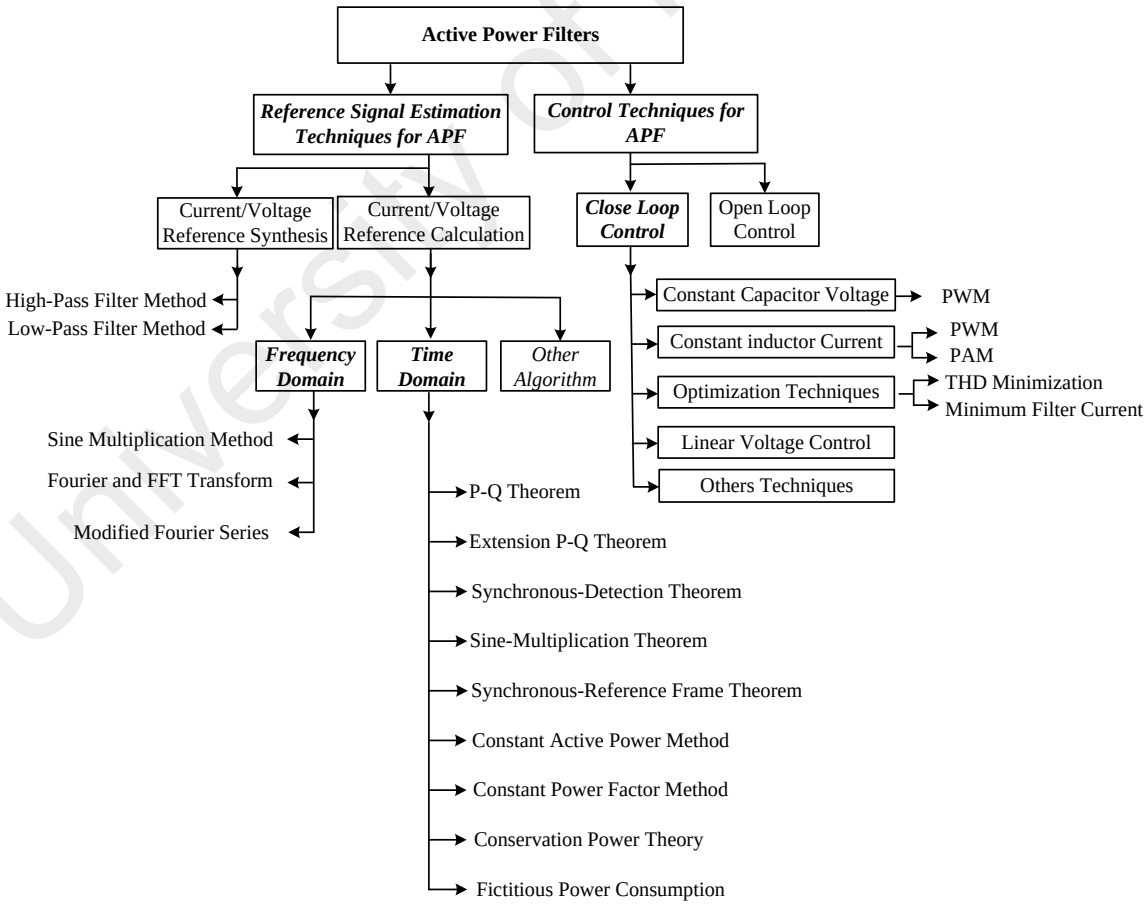


Figure 2.16: Different control techniques

2.9.1 Advanced control techniques for APFs

The reduction of the switching components in the SAPF systems, causes some limitation in the circuit. To overcome these limitations, two advanced control techniques for operating the switch reduce count inverter are adopted. These enhanced techniques namely sinusoidal pulse width modulation (SPWM) and Space vector pulse width modulation (PWM-SVM) operate in open-loop and closed-loop strategy (Wen Wang et al., 2013; Y. Zhang & Qu, 2015). Thus, the SVM is more complex than the SPWM scheme. The selection and optimization process of the different APF control techniques is based on the inverter appropriate design and different topologies.

2.9.1.1 Sinusoidal PWM (SPWM)

In power switching converters, sinusoidal PWM (SPWM) technique is one of the most standard modulation techniques. In modulating gate switching signal operation, a low-frequency sinusoidal reference signal as comparators is compared with a high-frequency triangular carrier signal of the inverter (de Rossiter Correa, Jacobina, da Silva, & Lima, 2006; Monfared & Golestan, 2012; Sarath, Raju, & Boppana, 2016). The comparator output defines the operating range of the switching orders and the key factor to be considered in the modulator design is the amplitude distortion, caused by the variation of DC voltage source. To control the desired line voltage frequency, the frequency of the modulating sinusoidal signal defines the inverter output (Dasgupta, Mohan, Sahoo, & Panda, 2013). The amplitude distortion of the PWM waveforms stops the amplitude of the fundamental component and produces low order harmonic contents (Miveh et al., 2016). However, the THD and power dissipation is one of the key issues in high-power converters applications. To minimize the switching losses and optimizing the harmonic contents, a fundamental frequency SPWM control method is adopted (Colak, Kabalci, & Bayindir, 2011). The SPWM modulation scheme is easily adopted for both the single and

multiple carrier applications. As noticed, the multi-carrier SPWM control techniques increase the performance of the high-level inverters.

The sinusoidal SPWM is the most enhanced technique in the PWM method (T.-S. Lee & Liu, 2011). However, the key benefits are as: easy execution, lower THD, and low switching losses. In four switch reduced, SPWM is implemented similar to the six-switch converter. The comparators and the carrier signals are same like conventional SPWM, but the only difference is in the command to control the reference signal pattern to control the four-switch power converter. In switch reduced count inverters are not symmetry, so the phase shift between the references signals changes. To compensate the DC-bus voltage fluctuations and to minimize the single-phase current lowing through the DC-link capacitors (C. W. Liu et al., 2009), at the cost of complex control strategies and additional hardware (Bhim Singh et al., 2004). The phase voltages are preferred for power converter as explain in Figure 2.15, are discuss below;

$$v_a = V_m \sin(\omega t) \tag{1.1}$$

$$v_b = V_m \sin\left(\omega t - \frac{2\pi}{3}\right) \tag{1.2}$$

$$v_c = V_m \sin\left(\omega t + \frac{2\pi}{3}\right) \tag{1.3}$$

No control on the third-leg phase of the VSI, the middle connection point of the DC-link (point O) is taken as the reference (Figure 2.15), therefore:

$$v_{an} = V_a - V_c = \sqrt{3}V_m \sin\left(\omega t - \frac{2\pi}{6}\right) \tag{1.4}$$

$$v_{bn} = V_b - V_c = \sqrt{3}V_m \sin\left(\omega t - \frac{2\pi}{2}\right) \tag{1.5}$$

$$v_{cn} = V_c - V_c = 0 \tag{1.6}$$

The infinite value of the modulation bandwidth of periodic signal produces harmonics (L. Wang, Hao, Hao, & Song, 2014). Theoretically, these harmonics are neglected in the SPWM control; however, the harmonic in the carrier and data modulation signal is filter out by using the digital filters such as Butterworth, Chebyshev, Bessel, Elliptic, and ITEA filter. These filter minimum the time integral and enhance the filtering functions to eliminate the carrier signal harmonics. Table 2.8, summarizes the evaluation of harmonic detection techniques for active power filter applications (Lucian Asiminoaei, Blaabjerg, & Hansen, 2007) .

Table 2.8: Evaluation of harmonic detection methods.

	Fast Fourier transform FFT	Discrete Fourier transform DFT	Recursive discrete Fourier Transform RDFT	Synchronous Fundamental DQ Frame	Synchronous individual Harmonic DQ Frame	Instantaneous power PQ theory	Generalized Integrators
Number of Sensors (For a Case of Three-Phase Application)	Three currents	Three currents	Three currents	Three currents, two/three voltages	Three currents, two/three voltages	Three currents, three voltages	Three currents
Number of Numerical Filters Required by the Harmonic Detection Algorithm	0	0	0	2 × HPFs	2 × LPFs × *N**	2 × HPFs	2 × *N**
Additional Tasks Required by the Harmonic Detection Algorithm	Windowing, synchronization	Windowing, synchronization	.	PLL	PLL	Voltage Pre-processing	.
Calculation Burden (Excluding the Numerical Filters)	−−	−−	+	+	−−	+	−
Numerical Implementation Issues	Calculation Burden,	Calculation Burden,	Instability for low precision	Filtering	Filtering, Tuning	Filtering	Tuning control
Related Algorithms or Implementations	Similar FFT algorithms	.	Rotating frame	Filter type	Filter type	Filter type; other theories *pq*r, *pq*0	Resonant filters type
Applications in Single- or Three-Phase Systems	Both 1-ph/ 3-ph	Both 1-ph/ 3-ph	Both 1-ph/ 3-ph	Inherently 3-ph	Inherently 3-ph	Inherently 3-ph	Both 1-ph/ 3-ph
Usage of the Voltage Information in the Algorithm	No	No	No	Yes	Yes	Yes	No

Method's Performance for Unbalanced and Pre distorted Line Voltages	++	++	++	+	+	–	++
Method's Performance for Unbalanced Load Currents	++	++	++	+	++	++	+
Applied for Selective Harmonic Compensation	No	Yes	Yes	No	Yes	No	Yes
Transient Response Time	––	–	+	++	+	++	+
Steady-State Accuracy	+	+	+	–	+	+	–

"+" indicates an increase in performance

2.10 Evaluations of topologies and control techniques

2.10.1 Reduced-switch-count inverters

Based on the section 2.7 analysis, a comparison among various transformerless and reduced–switch-count grid-connected inverter topologies are summarized in Table 2.9. To produce AC-voltage amplitudes in back-to-back or parallel inverter topology, a much larger DC-link capacitor and DC voltage is needed. This high voltage generates switching losses because of overstress across the semiconductor switches. To overcome this problem, z-source network and discontinuous modulation scheme are implemented (X. Chen, Fu, Infield, & Yu, 2009; Dehghan, Mohamadian, & Yazdian, 2010; Lei, Cao, & Peng, 2014). However, reduced B8 (Ledezma, McGrath, Munoz, & Lipo, 2001) and B4 converter (L. Zhang et al., 2012) topologies use a two-leg bridge structure. The B8 converter configuration practices eight switches with shared split DC link (Ledezma et al., 2001). By sharing a common single DC bus between two individual converters, no fundamental current flows through DC link if both the system is functioning and synchronized at the same frequency.

The B8 converter creates a large DC voltage variation in the value DC link and lower AC voltage in the output. The high value of the DC-link capacitor results in disadvantages, such as increased cost, short lifespan, and DC-link voltage balancing problem. To overcome the B8 converter limitation, a five-leg converter is introduced by sharing the fifth-phase leg between the two converter interface (Jones, Vukosavic, Dujic, Levi, & Wright, 2008). Roughly, no large DC variation is observed in fundamental voltage, but it has the limitation of the common frequency imposition in between the two AC-interfaced systems, including applications like series-shunt power conditioners and adjustable powered speed drives.

Table 2.9: Evaluation of three-phase reduced switch count APF topologies.

Authors	Modulation/ control	Capacity kVA/kW	Switching freq. (kHz)	Actual topology	Reduced switches	No. of diodes	No. of filter inductors	No. of filter capacitors	No. of transmission line inductors	Grid voltage (V)	No. of DC capacitors (μF)	THD (%)	DC-link voltage (v_{dc})
(Fatemi et al., 2013)	SPWM/E F-DF	2.5	6	6	3	0	1	-	-	-	3@2200	2	200
(Yeh & Manjrekar, 2007)	PWM/PI	1	10	8	6	0	1	0	1	120	2@-	3.54	700
(Choi, Kwon, Jung, & Kwon, 2005)	SPWM	3VA	15	8	6	0	1	0	-	220	1@1880	3.5	192
(Lam, Choi, Wong, & Han, 2012)	SPWM/A daptive DC-link	-	7.5	8	6	0	3	3	3	55	2@190	3.00	40
(C. W. Liu et al., 2009)	SPWM	5	3.2	12	9	0	3	0	3	208	1@2350	2	320
(Trinh & Lee, 2013)	PI/VPI current	1.5	10	6	4	0	3	0	3	127	2@2000	1.89, 1.97	420
(Limongi et al., 2015)	SPWM/PI	1.8	20	9	6	0	6	6	6	220	1@4700	3, 5.6	120
(Jou, Wu, Wu, Li, & Hsu, 2008)	SPWM/PI	4	20	6	4	0	3	3	3	220	1@2200	4.96.	400
(J. C. Wu et al., 2007)	SPWM/PI	7	20	6	4	0	3	3	3	380	1@4700	4	370
(B. R. Lin & Ou, 2004)	Hysteresis	5	7.0–9.1	9	6	0	3	0	-	110	2@2200	3.6.	400
(B. R. Lin & Wei, 2003)	SVPWM/ PI	2	20	12	8	4	3	0	3	110	2@2200	3.10	400

(Kolar et al., 2007)	SVPWM	6.8	10	18, 15	15, 9	18, 18	-	3, 3	-	400	-	-	-
(Vodyakho & Mi, 2009)	SV/PWM	7.5	7.2	16	12	6	4	4	-	400	1@4.4mF	6.08	700
(Khadkikar, Chandra, & Singh, 2011)	SVPWM/ PQ	20	7	8	6	0	4	0	4	35	2@1200	4.91	125
(Vodyakho & Kim, 2009)	Hysteresis	15	6.85	8	6	0	4	3	-	-	2@4.4mF	6.88	700
(W. Wang et al., 2013)	SVPWM	50	6.4	6	4	0	3	0	-	380	2@5000	17.8	1400
(Itoh, Noge, & Adachi, 2011)	SVM/SP WM/PI	1	10	24	12	36	3	0	-	200	8@47, 100, 220	3.40	-
(A. Bhattacharya et al., 2012)	SPWM/PI /FF & FB	3	550 Hz / 20	12	8	0	5	5	9	110	1@4700	4.70 23.50	26
(Daniel & Abirami, 2013)	SPWM/PI	3.3	550 Hz / 20	12	8	0	6	6	6	110	2@3300	0.03	1500
(L. Asiminoaei et al., 2007)	SPWM/PI /FF & FB	15	12.6	12	12	0	6	6	6	300	2@4.4mF	1.26 1.11	400
(Heydari, Varjani, Mohamadian, & Fatemi, 2012)	PWM	1	6	9	6	0	6	0	3	200	3@2200, 1100,2200	1.50	208
(Barrero, Martinez, Yeves, Mur, & Martinez, 2003)	DEAD-BEAT	3	15.6	-	6	0	6	3	3	110	2	2.66	720
(C. B. Jacobina et al., 2003)	PWM	~1.5	5	-	8, 6, 10	0	-	-	3	60	2@1000	0.8 0.6	100
(Cursino Brandão Jacobina et al., 2006)	PWM	~1.5	10	12	10	0	3	0	-	100	2@2200	1.54 0.8	200

(L. Asiminoaei et al., 2008)	SPWM/PI	5	12	12	12	0	12	0	6	400	1@2.2mF	2	250
(Lam et al., 2014)	SPWM/Adaptive DC-link	10	5	8	6	0	4	3	3	200	2@3.3mF	4.5	
(Ooi, Maswood, & Lim, 2015)	SRF-LS-PWM	1	1	18	12	24	3	0	-	60	4	5	200
(dos Santos Jr, Jacobina, Dias, & Rocha, 2011)	SPWM/PI	3	10	12	10	0	3	0	-	110	2@2200	1.65	140
(S. B. Karanki, N. Geddada, M. K. Mishra, & B. K. Kumar, 2013)	PI/ HYSTERESIS	5	3.10–6.8	12	12	0	6	6	6	230	1@2200	2.80	225, 125
(E. dos Santos, Jacobina, Rocha, Dias, & Correa, 2010)	SPWM/PI	2	5.2	10	8	0	3	3	3	100	2@2200	-	260
(B.-R. Lin, Wei, & Chiang, 2003)	SVPWM/ PI	2	20	12	8	4	3	0	3	110	2@2200	4.20	400
(Anand, Gundlapalli, & Fernandes, 2014)	SVPWM/ PI	10	7.5	6	6	0	3	3	3	400	1@25	5.90	300
(Khadkikar & Chandra, 2006)	SPWM/PI	1	-	16	14	0	6	6	-	100	1@5000	2.30	220

Recently, the evolution of SAPF in grid-connected and renewable energy conversion system became important because of power-quality-related problems. Over the last years, several conventional and advanced topologies and control methods have been documented for capacities, harmonics mitigation, reactive power compensation, and auxiliary functionalities. Table 2.10 summarizes the conclusions and parameters based on the recently developed APF topologies described in section 2.7. Each topology is evaluated and compared with each other to select low-cost, efficient, and suitable configurations. After reviewing the existing research works in the field of the shunt APFs, mainly in terms of reduction of components and their effects on the control strategies. The followings are the short coming of the existing works, as revealed from this chapter:

1. The traditional back-to-back or parallel power converter topology is limited by an oversized DC-link capacitor, limited amplitude sharing, and uncontrolled phase shift between the two converters at output terminals sets.
2. The parallel inverter topology offers less complicated and independent control for the two individual decoupled converters. It is limited by low modulation ratio which causes computational problems in spite of topological aspect (Newman & Holmes, 2002). Different frequencies and limited phase-shift constraint put a limit on maximum modulation ratio and requires the addition of the triple offset to avoid the crossover.
3. Reducing the switches improves the total efficiency, and lessens dissipated conduction and switching losses, but this is subjective to the quantity of the switches. In high-power rated system, all switching components are under high-voltage and current stress, which eventually affect the inverter performance.
4. The AC–AC topology shows limited phase shift and strict amplitude sharing in between the two terminal sets, such as dual motor drives (Kominami & Fujimoto, 2007), rectifier–inverter systems, and UPS (C. Liu, Wu, Zargari, & Xu, 2007).

5. By sharing the carrier at two converters, output terminals set for same output voltages and the DC-link voltage and semiconductor stress doubled. This doubling effect is removed in reduced-switch-count topologies.
6. In parallel inverter topology, the output voltage per phase at different frequencies generates transitions, which block the forbidden states. This blocking effectively generates range limitations on the reference amplitudes and phase shift.
7. Generally, in reduced switched power converter, the modulation strategy adopted is the sinusoidal PWM (SPWM), to compensate the DC-bus voltage fluctuations issues (C. W. Liu et al., 2009; L. Zhang et al., 2012) and for suitable switching scheme. As compare to the conventional six-switch converter, the phase shift between the reference signals does not track the three-phase balance and in symmetry order.
8. The reduction of switches generally leads to interdependencies between AC inputs and outputs frequencies as compare to full bridge converters. This restriction put the limitation of references used for modulation operating power converters at same frequency, even at the gain of the lower switching losses. As for four switch B4 converter, the voltage doubling and semiconductor stress is not an issue, due to maintain a maximum modulation ratio of unity as compare to nine-switch H6 converter (Fatemi et al., 2013).
9. The parallel inverter topology offers less complex and independent control for the two individual decoupled converters. It is limited by low modulation ratio which causes computational problems (Jones et al., 2008) in spite of topological aspect. Different frequencies and limited phase-shift constraint put a limit on maximum modulation ratio, forces to add the triple offset to avoid the crossover.
10. The reduced switch count (four switches) topologies faces the limitations in their switching states, as compare to the conventional six switch converter that uses six switches. However, in six switch power converter, two switching states (0, 0) and (1,

1) are stated as zero-vectors, stopping the flow of current towards the load. As mentioned before, in four switch converter the current flow even in the zero-vectors states, therefore, in the two other switching states (0, 1) and (1, 0), the resultant uncontrolled current of the other two phases flows through this phase, due to the direct connection between the DC-link capacitor and the AC terminal.

2.10.2 Grid-connected PV inverter

In some studies, the SAPF circuit topologies are similar to the grid interactive inverter to mitigate the harmonics and offer better power quality in the power distribution systems. To fix the high inverter cost and great number of components, several PV grid interactive system are combined to improve the reliability and efficiency of the system. In this manner, utility grids are integrated with the transformerless multilevel and multifunctional inverters based on the APF in the PV and WECS. To reduce the cost, volumetric size, and weight of the inverter stage in grid-connected systems, the transformerless configuration is considered an excellent solution in the PV inverters. However, the elimination of a transformer causes the absence of galvanic isolation (Salas & Olías, 2009), thereby causing an induced leakage current, unstable common mode voltage (e.g., efficiency degradation and safety problems), and safety hazards.

The H5 transformerless inverters topology (Araújo, Zacharias, & Mallwitz, 2010) is designed for high efficiency (Vazquez et al., 2009) to suppress the leakage current and reduce the leakage current. The main difficulty in this topology is that the leakage current still remains high during the freewheeling mode because of the existence of junction capacitance between the switches (Schimpf & Norum, 2008). By contrast, to overcome the voltage fluctuating issues, two techniques are implemented. First, during the free-wheeling periods, the PV panels are disconnected from the grid. Second, the neutral wire is used to connect with one pole of the PV panels. The most interesting feature of cascaded H-bridge topology is the high efficiency and to boost the AC output voltage levels, with

a disadvantage of excessive amount of switches (Lopez, Teodorescu, & Doval-Gandoy, 2006).

An alternative is the high efficient and reliable inverter concept (HERIC) (Araújo et al., 2010) and H5 inverters, especially in the half-bridge topologies. The neutral point is connected to the midpoint of the input voltage, but requires synchronization between gate signals. Therefore, a special circuit based on six switches and two diodes in the transformerless PV inverter suppress the leakage current and stable common mode voltage. To improve the leakage current, enhanced multi-level inverter topologies are installed rather than the conventional topologies.

Table 2.10: Summary and remarks for reduced switch count APF configurations.

Ref	Switches	Control	Action performed	Problems	Solution	Comments
(Limongi et al., 2015)	Six switches	Synchronous DQ	The single leg is removed to connect the single phase to the middle point in the system.	The imbalanced DC-link voltage is caused by sharing the same DC-link voltage in six switches of a two-legged structure.	The phase terminal is connected to the negative or positive pole of the dc link, thereby inducing the circulation of the dc current and the injection of a grid dc voltage in the system. Capacitors are used between the DC-link poles and PCC. The LC-filter capacitor reduces the dc current and DC-link voltage.	Problems, such as the voltage balance across the DC-link capacitor and the DC-link voltage imbalance, are encountered.
(Fatemi et al., 2013)	Three switches	Pulse width modulation (PWM); reference shifted	By removing the circuit legs, two dual-legged and single-legged switches are reduced to count the topologies of six switches and three switches in the leg structure.	By reducing the number of switches, the consumable switching states are limited as compared with the traditional fully decoupled converter topology, thereby avoiding the dc-bus short circuit and floating of loads.	Two modes of operation are achieved in the upper and lower loads of the current path by switching the state frequency independent of the output voltage. The inverter operates in all ON and OFF states. Both outputs are zero when the switches of the same row are OFF. When the upper and bottom layer of switches are ON, the others are working in the operating states. The corresponding output is in zero state. When both outputs are in the active state, the opposite switches of the two legs are OFF.	Problems are avoided by coordinating the two modulating references per phase across the upper and lower terminals. Hard switching operation occurs.

(Trinh & Lee, 2013)	Four switches	Proportional–integral (PI)/vector proportional–integral (VPI)	The accuracy of the system is affected by extracting the harmonic components in the load current. The reference filter current depends on the current controller and the harmonic current detector. A slow response time and steady-state response was observed when adaptive filters in the control were used. These filters affect the accuracy of APF.	By eliminating the need for a harmonic detector, the need for a current sensor is minimized. The control of the performance of harmonic tracking is unaffected by the proposed control.	By applying indirect current control schemes, the harmonic detector is eliminated without requiring the load current. The proposed PI/VPI controllers indicate the direct supply of current, which is regulated according to the change in the fundamental reference of harmonics. The controller uses the minimum current sensors and conventional four-switch three-phase inverter to mitigate the harmonic current and reactive power, as well as simplify the hardware structure. The overall cost is reduced and the accuracy of the APF system is improved.	The overvoltage spikes are higher. Lower costs and smaller sizes are achieved because of the lower rating.
(A. Bhattacharya et al., 2012)	Eight switches	Feed forward and feedback	By connecting both inverters in the back-to-back topology with parallel DC-links, such that both operate in parallel at different switching frequencies. The number of switches is reduced by eliminating the	The high voltage across the DC-link capacitor creates a voltage balance problem, thereby affecting the stability of the overall system.	The system aims to connect the phase in the negative or positive pole of the DC-link.	For the present problems, this paper does not consider the distortion of the source voltage and reference dc-bus voltage. Given the lower limit on a DC-link capacitor, a theoretical value of the voltage ripple is restricted to 2% half cycle at the

			complete leg from both VSI inverters.			fundamental or affecting frequency.
(L. Asiminoaei et al., 2007)	Twelve switches	Master–slave	To reduce the system cost, both inverters are connected in a feedback and feed forward loop configuration by sharing a single load current sensor and a single DC-link capacitor.	Complicated control produces a zero-sequence current circulation between inverters.	The proposed control operates at both filters as frequency- sharing or load-sharing, with or without redundancy. The feedback configuration provides the steady-state operation of harmonic mitigation. The feed forward filter configuration improves the dynamic response of the system. Both controls operate as a current source and a voltage source.	The need for an isolation transformer to stop the circulation of the zero sequence current between inverters is eliminated. Several of advantages over the single unit inverter APF include the reduction of line current ripple and grid high frequency losses, as well as the loading of harmonic compensation and EMI. This treatment reduces the size and cost of the switching ripple filter by combining a single DC-link.
(C. W. Liu et al., 2009)	Nine switches	Sinusoidal PWM (SPWM)	By sharing the rectifier and inverter, the middle switches were used in each leg of the nine switch converters.	The input/output voltage control is performed by three switches per phase on each leg.	Proper inverters and the DC equalizer push the rectifier-modulating wave. At any time, the rectifier modulating wave should not be lower than the inverter modulating wave.	The diode rectifier B2B 2L-VSC is replaced with the PWM voltage source rectifier with the DC-link capacitor

			The power and voltage are delivered via these middle switches and the dc-capacitor.	By sharing the middle switches between the rectifier and inverter, the inverter leg voltage cannot exceed the rectifier leg voltage.	The modulating waves are prevented from intersecting with each other.	because the DC-link capacitor has a limited lifespan.
(Cursino Brandão Jacobina et al., 2006)	Ten switches	PWM	The proposed circuit shares a common leg to reduce the number of power switches	The cost and number of power conversing devices, like power switches, are reduced.	By reducing the size of the gate driver circuit, the five-leg circuit with an increased power rating provides better performance as compared with the six-leg circuit when the load frequency is equal to the grid frequency power.	The grid and load converter voltages do not depend on the individual capacitor voltage. This value fluctuates between the rectifier and the inverter. The AC does not flow through the DC-link capacitors.
(L. Asiminoaei et al., 2008)	Twelve switches	Synchronous DQ reference frame	By interconnecting the two voltage-source APF inverters, the system components are reduced by the common-mode coils and a DC-link capacitor.	The single dc-capacitor creates a conduction path between the two inverters, thereby producing a circulating cross-current, which is equal to the switching frequency.	Common mode coils replace the isolation transformer to provide minimum bandwidth, a simple and flexible circuit, faster harmonic tracking response, smaller line inductance, and harmonic current compensation during any module failure. Interleaving reduces the inductor size, line-current ripple, and switching stress in the DC-link capacitor; higher switching and controller bandwidth is achieved in high-power applications.	The core saturation in the isolation transformer limits the switching frequency. The degree of each inverter current is higher because of the lower boost inductor and total current ripple. Each inverters is tuned at the half-rated power because of sharing the common load,

						thereby increasing the controller bandwidth, with high switching frequencies.
(C. B. Jacobina et al., 2003)	Eight, six, ten switches	PWM	By sharing a common leg, both the inverters are connected as single-phase to two-phase systems and single-phase to three-phase systems	The harmonic voltage pattern changes because of the distributing factor (THD) by varying the freewheeling period. The range of the distributing factor is difficult to select for the given mutually dependent grid and load	The flow of fundamental AC is stopped by the DC-link capacitor. The circuit provides a smaller THD. The stable input/output voltage converters are controlled.	Its complex PWM requires more complex and complicated control to effectively produce zero sequence current problems.

2.11 Summary

In summary, cost effective solutions to reduce the number of components in PV and wind energy conversion systems have been greatly explored. This study aims to assess the most advanced APF topologies, based on classification and recent control schemes in domain of grid-connected inverters. The reduced-switch-count PWM-VSI is more convenient for SAPF applications, due to light-weight, cheaper cost, and expandable to transformerless and multilevel configuration to improve its performance for higher power rating compensation. Oppositely, the conventional and transformer-based APF systems are robust, and reliable but have large volumetric size, bulky, and expensive in cost. Therefore, a transformerless and reduced switch counts inverter is proposed for grid-connected APFs system. The four switch two leg inverter structure is extracted from the conventional six switch three leg APF configuration. Different control schemes such as SPWM and SVC scheme are applied to configurable VSI-APF systems has been explained in this chapter. During nonlinear loading, the SPWM control scheme is adopted to show fast response and low THD during transient conditions.

CHAPTER 3: THE PROPOSED TRANSFORMERLESS SHUNT ACTIVE POWER FILTER

3.1 Introduction

Generally, every APF system consists of three parts: the power converter, the passive components and the control scheme. A significant amount of research has been devoted to this project in the design of H-bridge two-leg power inverter to reduce the system cost and volumetric size. Based on these facts, this chapter presents a novel four-switch two-leg VSI topology for three-phase APF system. The most important characteristic of the new topology is to reduce the number of switches with enhance harmonic mitigation capability and provides full reactive power compensation as compared to the conventional APF topologies. Detail step by step design procedure, control scheme and mathematical modeling of both the filters (APF and PFs model) verify its feasibility, particularly for the grid-connected applications. This chapter is organized into five sections. The proposed system configuration and system analysis are described in section 3.2 and section 3.3. The system analysis is subdivided into four-switch two-leg inverter analysis, PF analysis, design and reactive power compensation and filtering characteristic and section 3.5 reports the overall control system.

3.2 Proposed four-switch two-leg VSI-SAPF

In this research, a novel four-switch two-leg VSI topology for a three-phase SAPF is proposed for reducing the system cost and size. The proposed SAPF is composed of the three-phase two-leg bridge version of the four-switch inverter (Figure 3.1). It comprises a two-arm bridge structure, four switches, coupling inductors and sets of LC PFs. The adopted modulation strategy in this study is the sinusoidal PWM (SPWM) for a proper switching scheme. The carrier signal is compared with the comparators with single modification to pattern the reference signals (J. C. Wu et al., 2007).

The third leg of the three-phase VSI is removed by eliminating the set of power switching devices, thereby directly connecting the phase with the negative terminals of the DC-link capacitor. The elimination of single phase-leg generates the DC-link voltage imbalance or voltage fluctuations issues (Cursino Brandão Jacobina et al., 2006). This problem can be solved by connecting the removed leg terminal with the negative terminal of the DC-bus PWM-VSI to stop the unbalance charging of the DC-link capacitors (Limongi et al., 2015). Furthermore, to stop the flow of decoupling power ripples, the AC film capacitor stores the power ripples as connected to the AC terminals (B.-K. Lee, Kim, & Ehsani, 2003) to provide the balanced output currents and voltages. Unlike other existing topologies, the new circuit is derived from the six-switch full-bridge inverter presented in (Rahmani et al., 2010; Tangtheerajaroonwong et al., 2007). The new model enhances harmonic filtering and reactive power compensation comparable to conventional full-bridge topologies (S. Srianthumrong & Akagi, 2003).

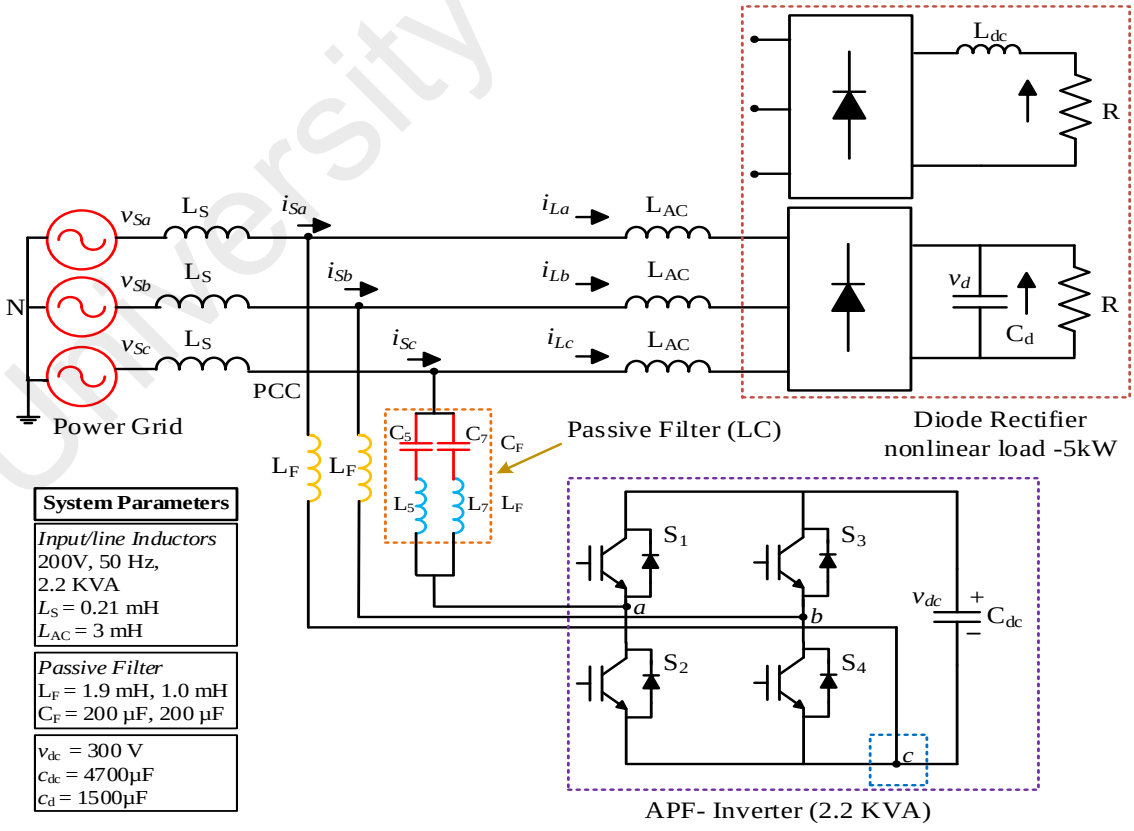


Figure 3.1: Proposed transformerless APF system.

The proposed design mainly aims to provide superior compensation capability and less complex structure without increasing the number of power switching devices for three-phase applications. The series AC-coupling inductors overcome the fixed reactive power compensation by the LC PF. The new topology provides superior overall performance as compare to the DC-bus midpoint configuration, in terms of harmonic compensation capability owing to the balanced current and voltage. No AC fundamental flows through the DC-bus capacitors because of the minimum current ripple in the imbalance output waveform. Less complex structure and straightforward connection between the transmission line and the terminal of the DC-bus reduce the constraint of voltage balancing across the DC-link capacitor (A. Bhattacharya et al., 2012). This configuration also eliminates the need of extra controller and transformer in between the LC PF and the filter inverter for preventing magnetic saturation. As a result, the design configuration presents low cost, reduced volumetric size, light weight and simplicity.

The two AC-link inductors are coupled to the two phases of VSI. The reduced leg terminal is linked through the sets of LC filters, including the inductor and capacitor set. In the reduced leg, the direct connection between the utility power line and the DC-link terminal divides the DC voltage and shifts it to the output voltage of the power converter. Therefore, the PFs are used to reduce the power and voltage requirement against the utility fundamental component at the output of the inverter (*phase c*). In addition, the inductors are used as a filter against the switching ripple generated from the switching converter. The capacitor of the PF provides the fundamental reactive power demand to the load and reduces the DC current and DC voltage circulation. However, it presents poor performance at low-order harmonic frequencies, except at the tuned seventh harmonic frequency. However, the two sets of LC filters are tuned at the 5th and 7th harmonic frequencies to compensate the current harmonics and improve the filtering characteristic.

3.3 System analysis of proposed three-phase APF system

3.3.1 Four-switch two-leg inverter analysis

For simplicity of analysis, source voltage $(V_{sx} = V_{xf} = V_{pcc})$ and load voltage (V_x) are considered as sinusoidal waveforms $(V_x = V_{pcc})$, without the harmonic components $(V_{sx} = V_x)$. The coupling passive power component is represented by $(Z_{shF} = Z_{PPFf} = Z_{Fabc})$ which comprises a series resistor, an inductor, and a capacitor. The inductance is a short circuit path owing to the low rated value as demonstrated in Figure 3.2.

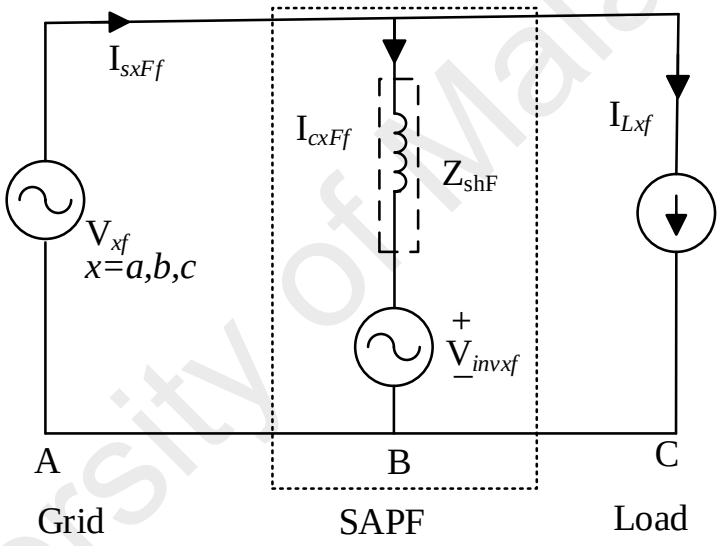


Figure 3.2: Fundamental equivalent circuit of the proposed APF system.

Figure 3.2 illustrates the single-phase fundamental equivalent reference circuit from the APF inverter fundamental voltage phasor $(V_{inv-shxf})$ to the output, where "*f*" shows the fundamental frequency component.

$$V_{inv-shxf} = V_x - Z_{shf}.\ I_{cxFf} \tag{3.1}$$

where the inverter fundamental compensating current phasor (I_{cxFf}) is divided into real and reactive components as;

$$I_{cxFf} = I_{cxFfp} + jI_{cxFfq} \tag{3.2}$$

where the subscripts "*p*" and "*q*" represent the active and reactive components. I_{cxFfp} is the fundamental active current component that compensates the loss and DC-link voltage control, and I_{cxFfq} is the fundamental reactive current component that compensates the reactive power in the system load. Thus, equation (3.1) can be simplified as follows:

$$V_{inv-shxf} = V_{inv-sxfp} + j\, V_{inv-sxfq} \tag{3.3}$$

$$V_{inv-sxfp} = V_x + I_{inv-sxfq}.X_{Ff} \tag{3.4}$$

$$V_{inv-sxfq} = -I_{inv-sxfp}.X_{Ff}$$

As shown in equations (3.2) and (3.4), the fundamental compensating active current (I_{cxFfp}) and the reactive compensating current (I_{cFxfq}) are extracted into

$$I_{cFfp} = -\frac{I_{inv-sxfq}}{X_{Ff}} \tag{3.5}$$

$$I_{cFfq} = -\frac{I_{inv-sxfp} - V_x}{X_{Ff}} \tag{3.6}$$

The value of the reactive DC current (i_{qDC}) is controlled in the quadrature axis and the value of the direct axis is set to zero to compensate the fundamental reactive power and protect the APF from being damaged. In the steady state, the active fundamental current (I_{cFxfp}) is insufficiently small ($I_{cFxfp} \approx 0$); thus, this current is generated by the inverter to maintain the constant DC-link voltage level. Therefore, with constant DC voltage level and modulation index around (m≈1), the ratio between the DC-link voltage and the load voltage (V_x) is expressed in equation (3.7), where $(V_{inv-sxf})$ is the inverter fundamental RMS voltage.

$$R_{v_{dc}} = \pm\frac{V_{inv-sxf}}{V_x} = \pm\frac{v_{dc}}{2\sqrt{2}V_x} \tag{3.7}$$

3.3.2 PF design and analysis

The design stages of the proposed transformerless APF consists of two parts; 1) the design of active filter inverter and 2) the design of the passive filter. Generally, each PFs consists of inductors and capacitors sets connected in series with the active inverter. The PFs are installed in the single removed leg of the power VSI to provide reactive power compensation and absorbing harmonic currents from a diode rectifier load.

In design process, the value of the (L_F), and (C_F) parameters are identified, referring to the harmonic content of the three phase diode rectifier load. Thus, the three-phase diode rectifier load produces few harmonics at the 11th and 13th harmonic frequencies. Therefore, the LC filters are tuned at the most dominant order 5th and 7th harmonic frequencies in between the grid phase and negative terminal of the DC-link capacitors. The low value filter inductance makes the APF system unstable and increases the switching ripples (Sunt Srianthumrong, Fujita, & Akagi, 2000). Therefore, the filter inductance value (L_F) should be ten times larger than the supply inductance (L_S) in order to acquire an attenuation ratio of 10%. To achieve the lower impedance (550 Hz and 650 Hz) of the PF, it is tuned to 350 Hz than the PF tuned to 250 Hz. Likewise, the PF is tuned to 7th dominant harmonic frequency in order to reduces the bulky weight than a 5th harmonic filter for the filter capacitor (C_F) (Al-Zamil & Torrey, 2001).

The selection criteria of the LC passive filter design depends upon two factors; 1) The larger value of the capacitance will makes the PF bulky and results in a high reactive current. 2) And the lower value of inductance increases the switching ripples produces from the inverter. The L_F and C_F parameters are calculated (Al-Zamil & Torrey, 2001) as follows; $Q_{sh} = \frac{V^2}{|Z_c|}$, $|Z_c| = \frac{1}{2\pi fC}$ and $f_{tuned} = \frac{1}{2\pi\sqrt{LC}}$.

In demand to PFs design specification and define criteria, a less expensive and cost effect 2.0 kVAR passive filter at 200V utility line voltage tuned around 360 Hz is tested and installed in the switch reduced leg of the hybrid APF system (R. N. Beres, Wang, Liserre, Blaabjerg, & Bak, 2016). The calculated values of the LC parameters are selected as C_F = 200 μF and L_F = 1.9 mH at the resonance frequency of F_{res} = ωres/2π = 258 Hz for L_F (5^{th} order). Similarly, the second LC parameters are selected as C_F = 200 μF and L_F = 1 mH at the resonance frequency of F_{res} = ωres/2π = 357 Hz for LF (7^{th} order). The resonance frequency should be chosen rightfully between the tuning frequency range in 200 and 550 Hz, because without the APF inverter the harmonic amplifying occur in the frequency range of 200–340 Hz. All the parameters of the PF design are detail in the Table 3.1.

Table 3.1: Parameters of Passive filter (PF)

Parameters	Value	Unit	Symbol
Passive filter rating	2.0	kVAR	-
Filter inductor	1.9	mH	(L_F) (5^{th})
Filter Capacitor	200	μF	(C_F) (5^{th})
Filter inductor	1	mH	(L_F) (7^{th})
Filter Capacitor	200	μF	(C_F) (7^{th})
Resonance frequency (PF)	258	Hz	(5^{th})
Resonance frequency (PF)	357	Hz	(7^{th})
Quality Factor	57	-	(Q)

The circuit schematic of the proposed APF model is shown in Figure 3.3. The high voltage rating of the model helps in reducing the device conduction and switch losses to nearly zero. The exiting of the high amount of current results in high winding loss; however, the current peak is low because of being tuned to the 5th and 7th harmonic frequencies, thereby resulting in low inductor losses.

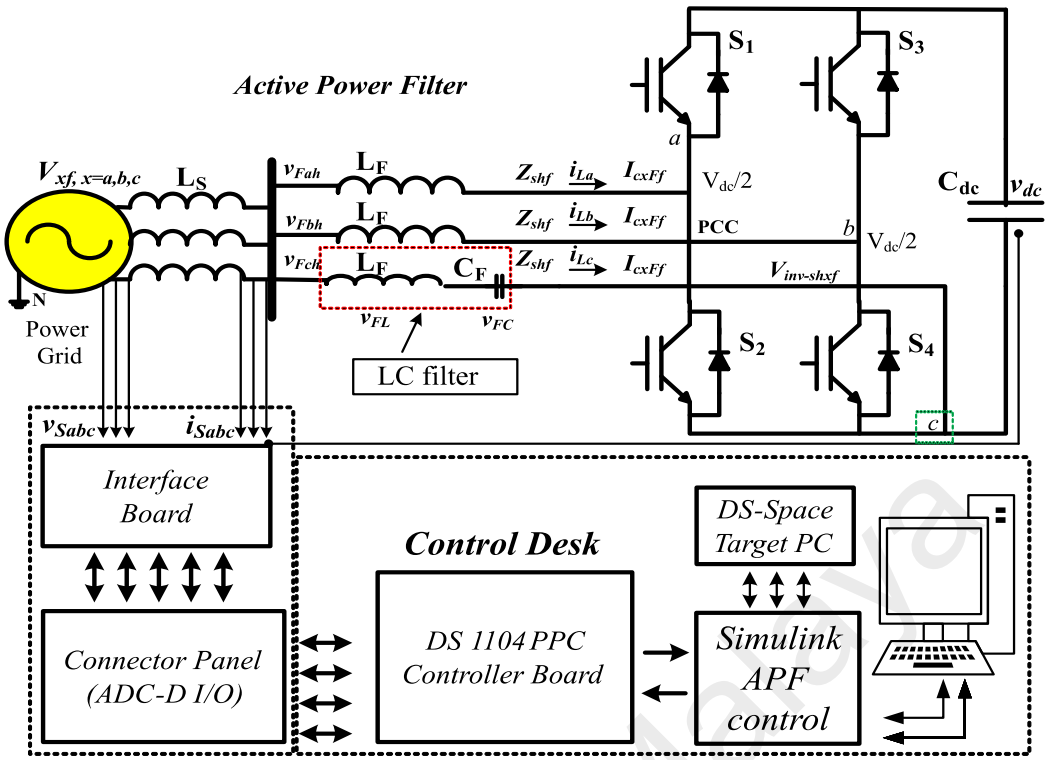


Figure 3.3: Circuit schematic of the proposed SAPF system

The effective filtering characteristic depends on the equivalent impedance of the PF and system ($Z_F = Z_{Fabc}$). However, the PF is tested at low impedance to avoid the harmonic amplifying phenomena. The harmonic resonance in the PF (Victor Fabián Corasaniti, Maria Beatriz Barbieri, Patricia Liliana Arnera, & María Inés Valla, 2009) causes wide range frequency tuning. Therefore, the use of PF is limited to the single phase of the power converter compared with other topologies. In other words, the capacitor of the LC filter stops the DC-link voltage component and provides the required stability margin caused by the utility voltage. The direct connection of the utility phase line to the negative terminal reduces the DC-link voltage and shifts half of the DC-link voltage to the output voltage at the power converter; therefore, this converter is composed of switching ripple, DC-link, and amplified modulation components (Hirofumi Akagi & Kondo, 2010; J. C. Wu et al., 2007), as mention in equation (3.8).

$$\frac{v_{dc}}{2} + k_{con}\, v_m(t) + v_{swr}(t) \tag{3.8}$$

where v_{dc} is the DC-link voltage, $v_m(t)$ is the modulation signal, k_{con} is the gain of the power converter, and $v_{swr}\ (t)$ is the switching ripple voltage of the power converter.

The DC-link component of the output voltage is compensated by the PF capacitor, and the series inductors filter out the switching frequency of the power converter. Given that the utility does not represent the DC voltage component, the DC component is regarded as a short circuit and the power converter is represented as two DC voltage sources in phases *a* and *b.* Considering that the series inductor and capacitor are under the steady state, the DC voltage source is regarded as capacitance (X. Wang, Liu, Yuan, & Wang, 2006) and the inductor is regarded as a short circuit. Therefore, the suitable rated capacitor having the DC voltage component is represented by equation (3.9).

$$V_{pha(dc)} = V_{phb(dc)} = \frac{v_{dc}}{2} \tag{3.9}$$

$$V_{phc(dc)} = -v_{dc},$$

where $V_{phc(dc)}$ is the DC voltage component across the series capacitor in phase *c*.

The fundamental frequency voltage component is examined and regulated with the DC voltage component. No fundamental component flow exists in the output voltage because of the fixed reactive power generated from the series capacitor and inductor set. At the fundamental frequency, the coupling inductor and series capacitor represent a capacitive characteristic to stop the excessive fundamental current through APF. The impedance of the inductor is small and negligible compared with the capacitor set. The series capacitor provides necessary fundamental reactive power and blocks the redundant fundamental current through APF to withstand the utility fundamental.

3.3.3 Reactive power compensation capability

When the passive power component in equation (3.4) and (3.7) is a pure inductor value (L_F), the APF acts similar to a traditional pure APF. When the passive power component consists of a series connection of an inductor (L_F) and a capacitor (C_F), the APF behaves

similar to an HAPF with leading capacitive (C_F) controlling the passive values at the fundamental frequency. In steady state condition, given the DC-link voltage controller ($I_{cFxfp} = 0$), ($X_{Ff} = X_{LFf}$) for pure APF and ($X_{Ff} = -|X_{cFf} - X_{LFf}|$) for *LC*-HAPF. The ($Q_{Cf}$) present a fundamental reactive power injection with negative signs as the inductive loading compensation. The ratio between the DC-link voltage and the load voltage ($R_{v_{dc}}$) determines the operational range of the APF. The DC-voltage value (v_{dc}) of the APF must be larger than the peak of the load voltage, regardless of the coupling inductance (L_F); the inverse setting is required for the HAPF. Therefore, the APF cannot support the inductive loading compensation when it operates as a pure PF.

On the contrary, the HAPF can exhibit such support depending on the passive parameters because of the fixed reactive compensation (Q_{Cf}). The fundamental voltage component across the series capacitors causes fixed reactive power compensation, as suggested in equation (3.10) of study (A. Bhattacharya et al., 2012). In the proposed two-leg VSI topology, the fixed reactive power compensation phenomenon is limited in the single reduced leg compared with other two phases. The reason is that the tuned LC filter without APF provides higher reactive power capacity than the tuned LC filter with APF, as mention in equation (3.10).

$$Q_c\ (MVAr) = (2\pi f)\ x\ (cv_s^2) \tag{3.10}$$

where c is the capacitance of the capacitor, v_s is the mean value of the source voltage, and ω is the fundamental frequency. As notice the maximum reactive power compensation capacity depends on the impedance value (Z_{sh} = inductive) in the three-phase APF is demonstrated in equation (3.12),

$$Q_{shf}(MVAr) = 3\ x \left(\frac{V_{pcc}^2}{Z_{sh}}\right) \tag{3.12}$$

To compensate the reactive power, the voltage of the VSI inverter is greater than the PCC voltage as written as ($V_{sh} > V_{pcc}$). As we noticed, that the (θ_{shv}) is very small as compare to the (θ_{shi}), due to the (θ_{shz}). Hence the AC inductors impedance is inductive, so the (θ_{shz}= 90^o), therefore resulting the active fundamental power shift from the APF inverter to the point of common coupling PCC is zero, as presented below,

$$P_{shf} = \left(\frac{V_{pcc}.V_{sh}}{Z_{sh}} \cos\theta_{shv} - \frac{V_{pcc}^2}{Z_{sh}}\right) \cos\theta_{shz} \rightarrow P_{shf} = 0$$

$$Q_{shf} = \left(\frac{V_{pcc}.V_{sh}}{Z_{sh}} \cos\theta_{shv} - \frac{V_{pcc}^2}{Z_{sh}}\right) \sin\theta_{shz} \rightarrow Q_{shf} = V_{pcc}.I_{sh} \quad (3.13)$$

$$H_{sh} = \frac{V_{pcc}.V_{sh}}{Z_{sh}} \sin\theta_{shz} \rightarrow H_{sh} = V_{pcc}.I_{sh}$$

where V_{sh} is the VSI output voltage, V_{pcc} is the voltage at PCC, θ_{shi} is the capacitance of the capacitor, θ_{shz} is the mean value of the source voltage, and θ_{shv} is the fundamental frequency. The VA rating of the APF inverter for reactive and harmonic power compensation as presented in equations (3.14) and (3.15) as follow, where P_{loss}, represents the total active power loss of the APF. The I_{sh}, is the compensating currents, R_{sh} is the switching losses in each phase of the VSI inverter.

$$VSI_{q-rating} = S_{q-vsi} = \sqrt{(Q_{shf}^2 + P_{loss}^2)} \quad (3.14)$$

$$VSI_{h-rating} = S_{h-vsi} = \sqrt{(H_{shf}^2 + P_{loss}^2)} \quad (3.15)$$

$$\text{Where,} \quad P_{loss} = 3\,(I_{sh.}^2\, R_{sh})$$

In the steady state, the active fundamental current (I_{cFxfp}) shows the minimum value (($I_{cFxfp} \approx 0$). However, the APF inverter injects pure reactive fundamental current equal to $\left(I_{cFxf} = jI_{cFxfq}\right)$. Hence, ($V_{inv-shxf}$) in equation (3.16) verifies the pure active component as;

$$V_{inv-sxfp} = V_{inv} + I_{inv-sxfq}.(X_{cFf} - X_{LFf}). \quad (3.16)$$

At full compensation power of the PF, the HAPF compensating reactive power (Q_{Cf}) is equal to the reactive power provided by the passive component (Q_{CFf}), which can be expressed as equation (3.17). In this equation, $Q_{CFf} < 0$ proofs the injecting reactive power as the leading reactive power.

$$Q_{cFf} = -\frac{V_x^2}{|X_{cFf} - X_{LFf}|} < 0 \quad (3.17)$$

3.3.3.1 Dedicated inductors to enhanced reactive power capability

To enhance the reactive power flow, the designed coupling inductors controls the active and reactive power flow, similar foundation on the working principle of STATCOM system. The power flow is regulated intentionally using the function of two coupling inductors. Therefore, the dedicated inductors for reactive power flow is shown in Figure 3.4 (a) to Figure 3.4 (c). In contracts, suppose the inductors in leg-b (L_b) and leg-c (L_c) is eliminated as shown in Figure 3.4 (b) and Figure 3.4 (c), the reactive power actions by means of coupling inductors are split into two rectifier legs (L_a) and (L_b) as the inductor in leg-c, ($L_c = 0$) and in leg-b ($L_b = 0$) are eliminated. Therefore, it proofs the split reactive power flow function through the control of smoothing inductors (L_b) and (L_a) of three-phase rectifier. The new APF model usages the coupling inductor of the rectifier to deliver the compensating current ($L_c = 0$), as more detail in the three-phase unbalanced equivalent circuit (Figure 3.4 (d)). Additionally, in phase c the compensating current is filter out using the LC set.

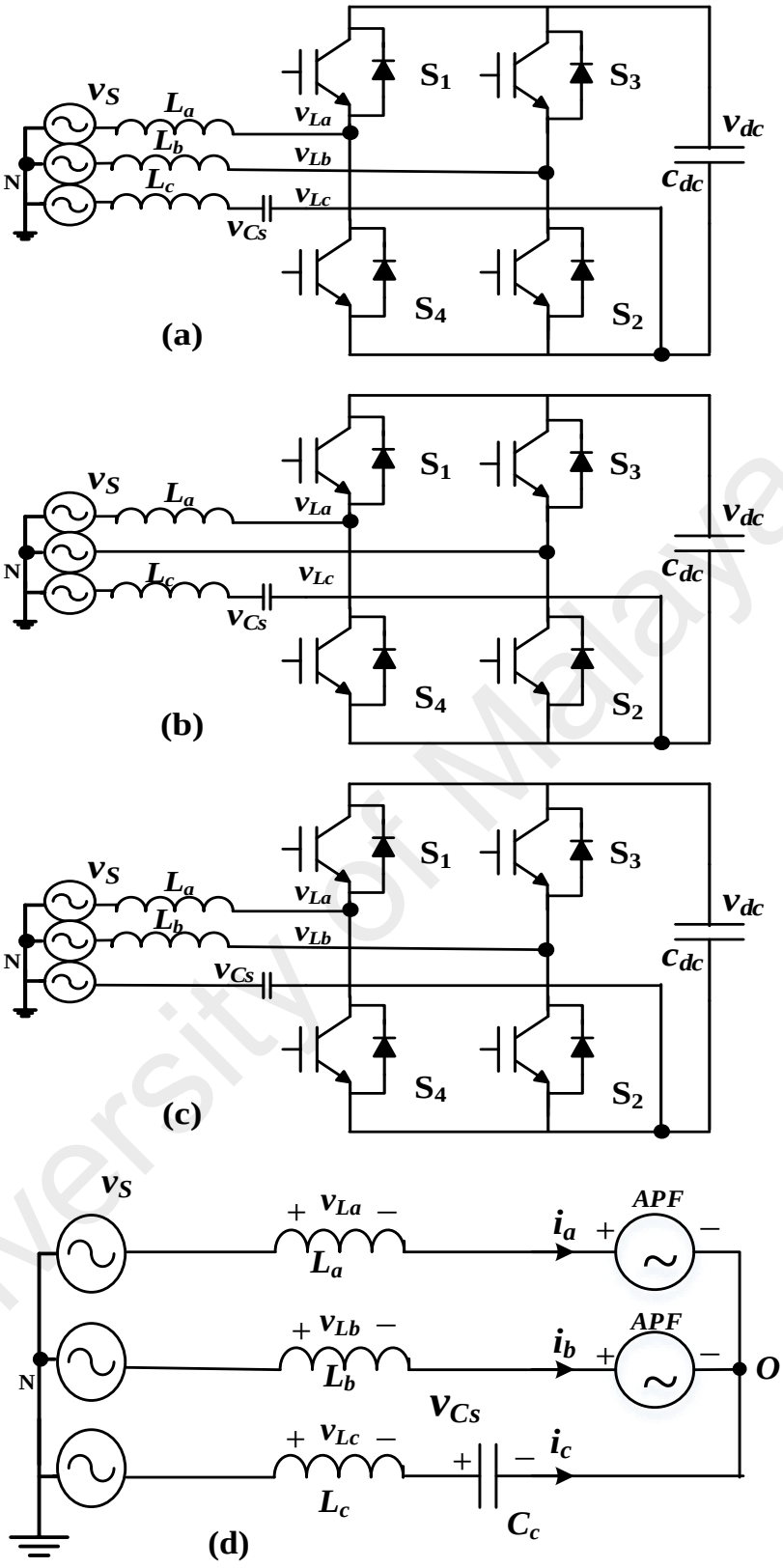


Figure 3.4: Operation modes of the proposed APF topology. (a) Basic APF circuit. (b) Show ($L_b = 0$). (c) Show ($L_c = 0$). (d) Equivalent circuit of three-phase power converter with the feature of APF.

To stop the source current to become susceptible to switching actions of rectifier dedicated legs, the store energy in dedicated smoothing inductor (L_c) overcome this issue $(L_b = 0)$ and proposed APF delivers the power from grid. The distribution grid voltage and current are explained as:

$$v_s(t) = \sqrt{2}\, V_s \sin(\omega t) \tag{3.18}$$

$$i_a(t) = \sqrt{2}\, I_a \sin(\omega t) \tag{3.19}$$

Follow by the active power flow, because of the inductors behavior the $v_c(t)$ is lagging the $v_s(t)$ by (δ). Where (v_s) and (v_c) are the RMS grid voltage and charger output voltage respectively, (ω) is the angular frequency (rad/sec), (*f*) is the system frequency and (I_c) is the RMS value of the rectifier.

$$v_c(t) = \sqrt{2}\, V_c \sin(\omega t - \delta) \tag{3.20}$$

$$i_c(t) = \sqrt{2}\, I_c \sin(\omega t - \theta) \tag{3.21}$$

The grid voltage v_c and current i_c make active power flow towards the converter, hence the capacitor voltage and current to be written as:

$$v_{cs}(t) = \sqrt{2}\, V_{cs} \sin(\omega t + \theta) \tag{3.22}$$

$$i_c(t) = \sqrt{2}\, I_c \cos(\omega t + \theta) = \omega C_s V_{cs} \cos(\omega t + \theta) \tag{3.23}$$

In the three-phase three-wire system, we have:

$$i_c(t) = \sqrt{2}\, (i_a + i_b + i_c) = 0 \tag{3.24}$$

To reduce the current stresses, due to relatively large inductances (L_a, L_b, L_c). The reactive power cannot be ignored, therefore, the instantaneous power draws from the distribution grid is expressed in equation (3.25);

$$p_s(t) = V_s(t)\, i_c(t) \tag{3.25}$$

And input instantaneous power of the coupling inductors and received power from the distribution grid, plugging equations (3.18), and (3.21) into equation (3.25), can be written as follow:

$$p_{ab} = V_s i_a - L_a \frac{di_a}{dt} i_a - L_b \frac{di_b}{dt} i_b \tag{3.26}$$

$$= \frac{V_s I_a}{2} - \frac{V_s I_a}{2}\cos(2\omega t) - \frac{\omega(L_a + L_b) I_a^2}{2}\sin(2\omega t)$$

$$+ \frac{\omega L_b I_c^2}{2}\sin(2\omega t + 2\theta) - \omega L_b I_a I_c \cos(2\omega t + \theta)$$

As noticed, the instantaneous input power (p_{ab}) contain two components, the constant part and ripple part as shown in equation (3.27) and (3.28), resulting in equation (3.29) of the system are respectively,

$$P_o = \frac{V_s I_a}{2} \tag{3.27}$$

$$p_{ripple}(t) = p_{ripple}\cos(2\omega t + \beta) \tag{3.28}$$

$$p_{ab_r} = -\frac{V_s I_a}{2}\cos(2\omega t) - \frac{\omega(L_a + L_b) I_a^2}{2}\sin(2\omega t) \tag{3.29}$$

$$+ \frac{\omega L_b I_c^2}{2}\sin(2\omega t + 2\theta) - \omega L_b I_a I_c \cos(2\omega t + \theta)$$

Therefore, the instantaneous power generated by the inductor and capacitor set leg c, can be written as:

$$p_c = L_c \frac{di_c}{dt} i_c + v_{cs}\, i_c = \left(\frac{1}{2\omega C_s} - \frac{\omega L_c}{2}\right) I_c^2 \sin(2\omega t + 2\theta) \tag{3.30}$$

To eliminate the second order ripple factor, the capacitor voltage (v_{cs}), is controlled as:

$$p_c(t) = p_{ab\_r} \tag{3.31}$$

The instantaneous power the inverter received is written as equation (3.33), suppose (Lc = 0), is adopted and submitting equations (3.29) and (3.30) into equation (3.33), produces as:

$$p_{ab}(t) = p_c(t) \tag{3.32}$$

$$-P_o \cos(2\omega t) - P_L \sin(2\omega t) \tag{3.33}$$

$$= \left(\frac{1}{2\omega C_s} - \frac{\omega L_c}{2}\right) I_c^2 [\sin(2\theta)\ \cos(2\omega t)$$

$$+ \sin(2\omega t)\ \cos(2\theta)]$$

Where, the reactive power consumed by the inductors are as follow:

$$P_L = \frac{\omega L_a I_a^2}{2} \tag{3.34}$$

The following equation based on instant of time, show the reference of capacitor voltage and current in equation (3.33). To adjust the APF reactive power capability, equations (3.35) and (3.36), are equal to instantaneous active (P_{rd}), and instantaneous reactive (P_{rq}) power as follow:

$$P_o + \left(\frac{1}{2\omega C_s} - \frac{\omega L_c}{2}\right) I_c^2 \sin(2\theta) = 0 \tag{3.35}$$

$$P_L + \left(\frac{1}{2\omega C_s} - \frac{\omega L_c}{2}\right) I_c^2 \cos(2\theta) = 0 \tag{3.36}$$

From equations (3.35) and (3.36), the reference of the capacitor voltage and current can be explained as:

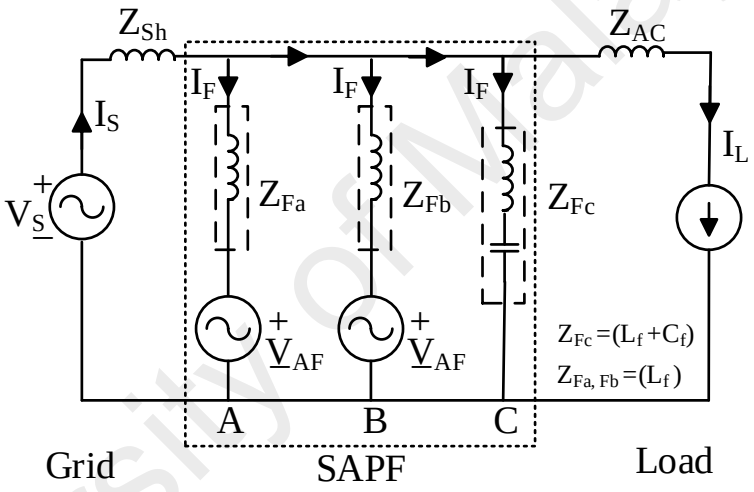
$$v_{cs}(t) = \sqrt{2}\, V_{cs} \sin(\omega t + \theta) \tag{3.37}$$

$$i_c(t) = \sqrt{2}\, I_c \cos(\omega t + \theta) = \omega C_s V_{cs} \cos(\omega t + \theta) \tag{3.38}$$

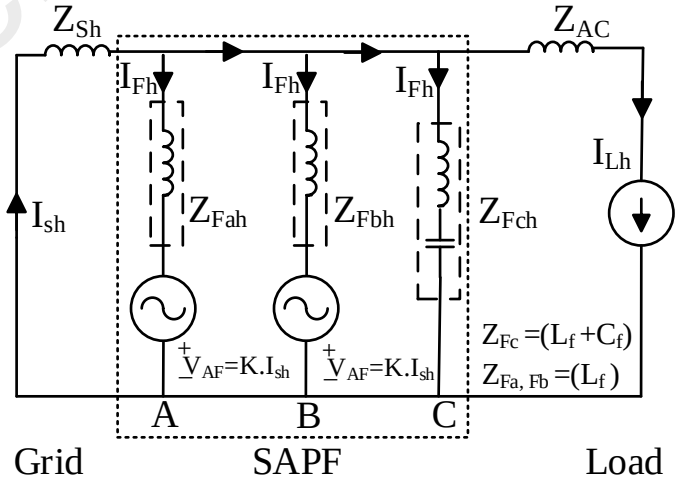
3.4 Filtering characteristic of the proposed APF model

A three-phase equivalent circuit of the proposed configuration is illustrated in Figure 3.5 (a). The APF is used as a regulated voltage source (V_{AF}) with two independent control

source (V_S) and (I_L) and a filter impedance ($Z_F = Z_{Fabc}$) to compensate for the specific harmonics of interest [17]. In the practical system, operating the load as a model harmonic current source is difficult because of the system impedance [18]. However, in the equivalent circuit, the non-linear load is considered a model current source (I_L) with pure sinusoidal waveforms. The APF operates as the voltage source proportional to the component of line current harmonics ($V_{AF} = K \times I_{sh}$), where *K* represents the gain of the filter, I_{sh} shows the source current, I_{Fh} is the APF compensation current and I_{Lh} is the load current.



(a)



(b)

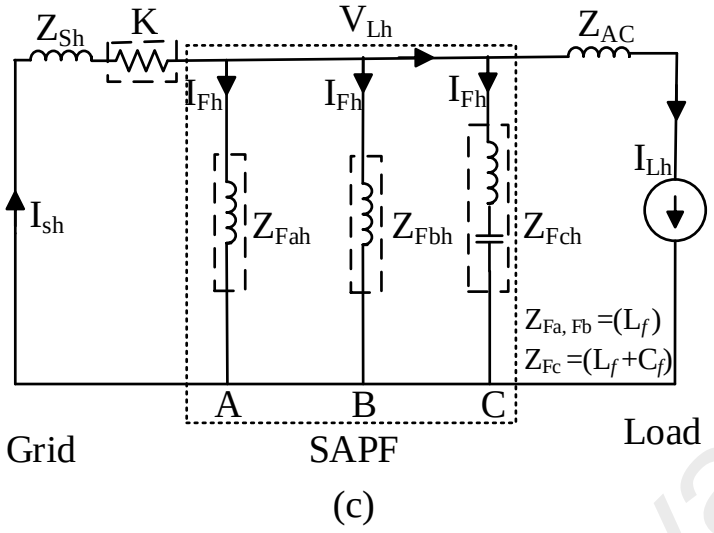


Figure 3.5: (a) Total equivalent circuit of a three-phase system (b) Harmonic equivalent component circuit (c) Resistive equivalence of harmonic filter.

An SPWM switching scheme is adopted to compensate the harmonic contents and lower the ripples in the output voltage waveform and consequently avoid the zero utility current. With regard to a proper PWM switching scheme, the modulation signal is compared with the high-frequency triangular wave (V_{tri}). At low harmonic frequency, the VSI operates as an inductor (Mesbahi, Ouari, Abdeslam, Djamah, & Omeiri, 2014) and advances to stop the flow of fundamental current in the APF branch. However, keeping the high K value reduces the resonance and background harmonic voltage (S. Srianthumrong & Akagi, 2003). For reactive current damping, the passive filter operates without controlling the voltage source as shown in Figure 3.5 (b), and the utility is studied as a pure sinusoidal source. Applying Kirchhoff's voltage law (KVL), we calculated the following equation (3.39).

$$V_{sh} - I_{sh}Z_{sh} - I_{Fh}Z_{Fh} - V_{af} = 0 \qquad (3.39)$$

Where;

$$V_{sh} = 0 \text{ and } V_{af} = KI_{sh} \qquad (3.39a)$$

$$I_{sh} = I_{Lh} + I_{Fh} \qquad (3.39b)$$

Combing the equations (3.39a) and (3.39b), the ratio $\frac{I_{sh}}{I_{Lh}}$ between the harmonic line current and the non-linear load when no APF is connected (K = 0) is presented in equation (3.40).

$$I_{sh} = \left(\frac{Z_{Fh}}{Z_{Fh} + Z_{sh}}\right) \times I_{Lh} \tag{3.40}$$

The excellent filtering characteristic depends on the impedance value ($Z_{Fh} \lll Z_{sh}$), where Z_{Fh} is the PF impedance ($Z_F = Z_{Fabc}$) and Z_{sh} is the system impedance. Figure 3.5 (c) shows that the APF operates similar to a practical impedance (Xiaoyu et al., 2007) in series with the source impedance (Z_S) to operate as a pure resistor (K = Ω). At the fundamental frequency, the APF operates at zero impedance and act like a damping resistor to pushes the harmonics to follows the inductor path at harmonic frequencies in equation (3.40). During the APF operation, the K value determines the flow of the harmonic and stops the harmonic by pushing toward the APF leg. However, the APF follows the inductor path at harmonic frequencies, as shown in equation (3.41).

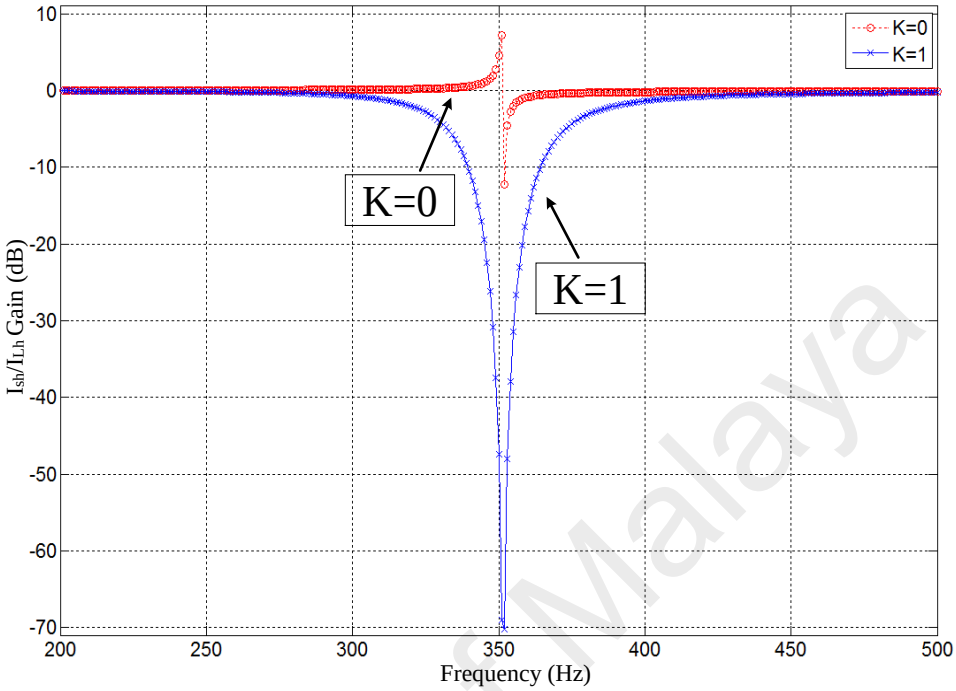
$$\frac{I_{sh}}{I_{Lh}} = \frac{Z_{Fh}}{K + Z_{Fh} + Z_{sh}} \tag{3.41}$$

The K value is always kept higher than the impedance Z_S value to improve the filtering characteristic and prevent the stability and resonance problems between Z_S and Z_F.

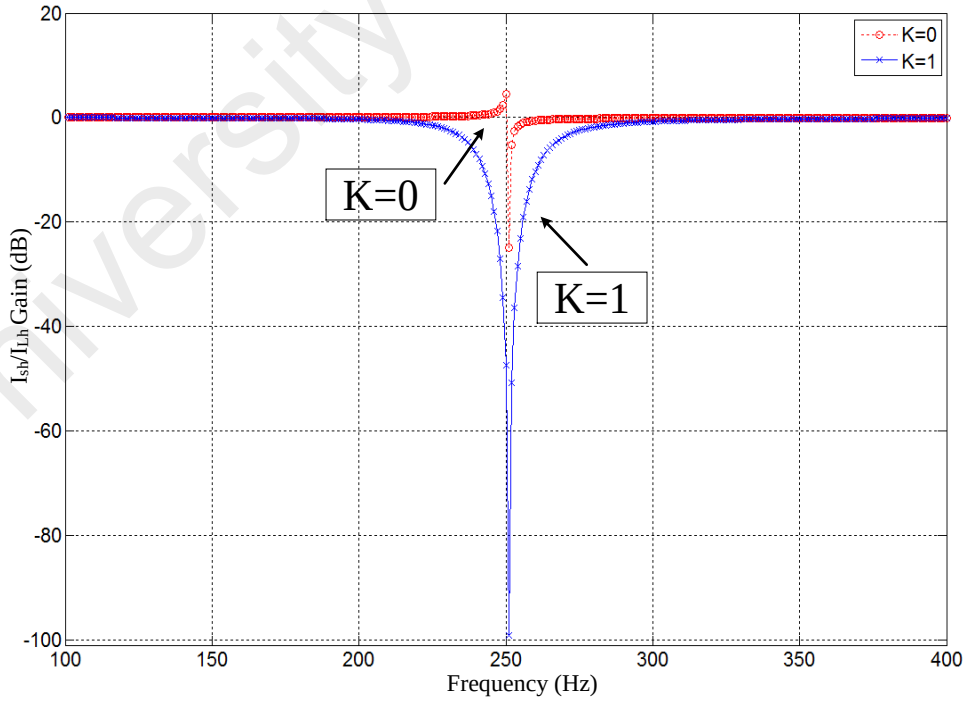
3.4.1 APF capability to improve filtering performances

The feedback control gain K suppresses the resonance between the utility grid and the PF is shown in Figure 3.3 and Figure 3.5 (c). The LC filter is tuned to 250 Hz and 400 Hz frequency to suppress the harmonics below and above the tuning frequency. Therefore, the tuning frequency is range in between the 200 and 550 Hz. It is worth to note that the rectifier load produces fewer harmonic at 11^{th} and 13^{th} harmonic frequencies, so these harmonics are not a series issue. Therefore, the LC-filters in tuned at 5^{th} and 7^{th} dominant harmonics in between the grid phase and DC-link capacitors as shown in Figure 3.6 (a)

and Figure 3.6 (b). These results verify the filtering capability of proposed APF is satisfactory at 5th (250 Hz) and 7th (352 Hz) harmonic frequencies.



(a)



(b)

Figure 3.6: Capability to improve the filtering performances of APF (K = 0, K = 1) due to tuning frequency: a) I_{sh}/I_{Lh} at 352 Hz. and b) I_{sh}/I_{Lh} at 250 Hz.

Figure 3.7 shows a bode plot of the filtering characteristics of the proposed APF. Different K values against the harmonics $I_{sh}/I_{Lh} = \left(\frac{Z_{Fh}}{K+Z_{Fh}+Z_{sh}}\right)$ (equation 3.41) in dB and inter harmonic frequencies in Hz, proof the frequency response of the LC filter. When only PF is connected (K=0) in (equation 3.40), the harmonic amplifying phenomena occur at the frequency range between 340 and 350 Hz. However, when the APF is connected (K>0), harmonic damping increases and no amplification phenomena occurs. And all the harmonic contents components are considerably reduced as shown in Figure 3.8. The feedback gain K value range up to infinite values to disappear the harmonic content entirely but its range is limited to certain values due to the stability issues. The problem of harmonic resonance in the PF (Victor Fabián Corasaniti et al., 2009) put the limitation of wider range frequency tuning. Therefore, as notice the use of PF is limited to the single phase of the power converter as compare to other APF topologies. It proof that the proposed APF is capable to improve the filtering performances, no harmonic amplification phenomena and compensate the current harmonic contents produces from the nonlinear rectifier load.

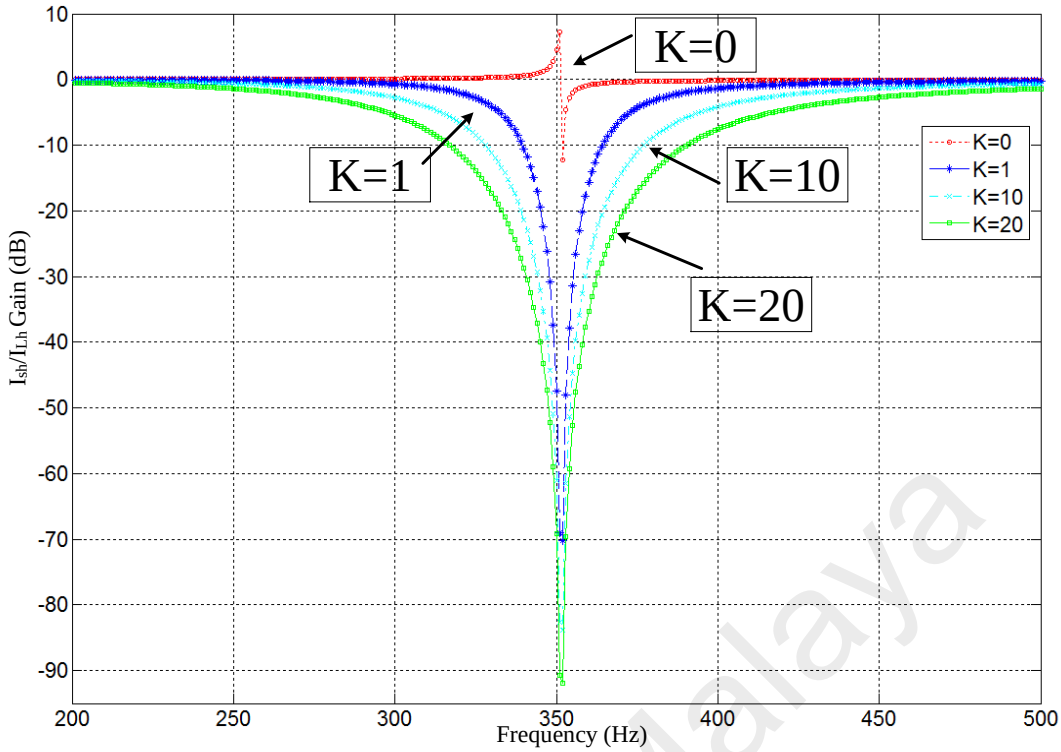


Figure 3.7: Filtering characteristics and frequency response of the proposed APF.

3.4.2 APF capability to enhance system robustness

In order to proof the system robustness, a bode plot of I_{sh}/I_{Lh} (equation 3.41) is plotted against the different L_S values (Figure 3.8) when the APF is connected. In the bode diagram, the harmonic current amplification increases and shift to lower frequency with the increase L_S value and vice versa. Furthermore, the results verifies that the adopted APF does not change the harmonic current compensation characteristic. Here, both results in Figures 3.7 and 3.8 verifies the proposed APF has capability to enhance the system robustness and to improve the filtering performances.

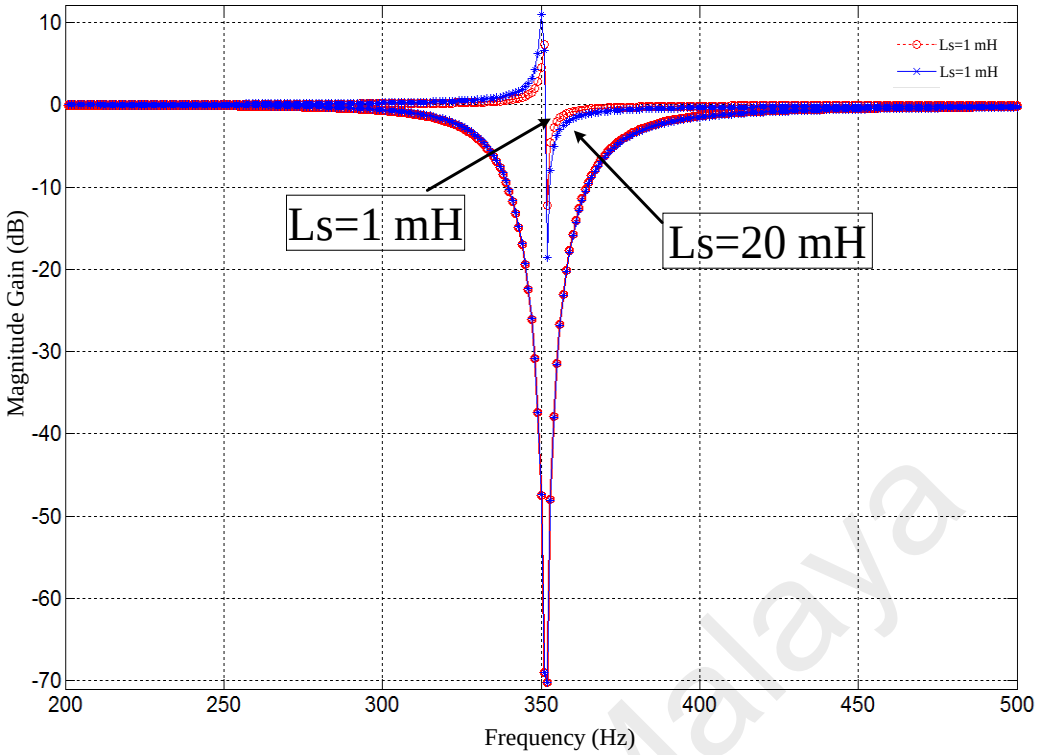


Figure 3.8: Capability to enhance the system robustness due to varying Ls: a) without APF (K = 0) and b) APF is employed (K =10).

3.5 Controller design

The discussion of the controller for the proposed inverter can be divided into three control parts; 1) grid synchronization, 2) APF system reference generator and 3) DC-link voltage controller. The overall block diagram of the controller is shown in Figure 3.9. The controller is designed to measure the current references and voltage reference to generate the modulation signals. An appropriate control is tested for each phase gate signals of the semiconductor switches and to eliminate the current harmonics and maintain constant DC-link voltage. The overall control algorithm is tested in a *dSPACE* modular unit based on a *DS1104* processor board in the Matlab-Simulink environment.

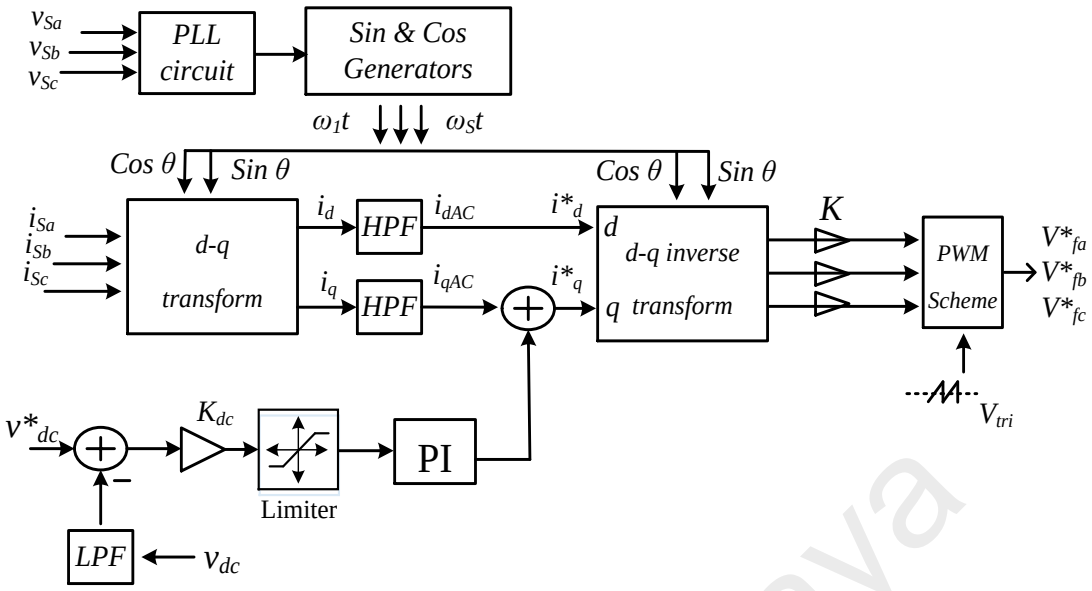


Figure 3.9: Overall control system of the proposed SAPF

3.5.1 Grid synchronization

The phase lock loop (PLL) scheme offers transient free locking to the rotating synchronous frame with the positive sequence of the three-phase supply voltages; this scheme is thus used to control the system reference voltage for VSI operation (Dong, Wen, Boroyevich, Mattavelli, & Xue, 2015). At the fundamental input component, the phase locking system keeps the positive sequence and constant amplitude of the output and input line voltage. The transformation matrices, keeps the operation on the fundamental input component and controls the input current in accordance with the input voltage harmonics. As the zero sequence is neglected because of the three-phase system and the voltage source inverter (VSI) provides the AC voltage to compensate the system harmonics (Jintakosonwit, Fujita, Akagi, & Ogasawara, 2002). Normally, the phase angle is locked to the supply voltage (Phase-a) in the three-phase system between the (0 to 2π), as depicted in Figure 3.10.

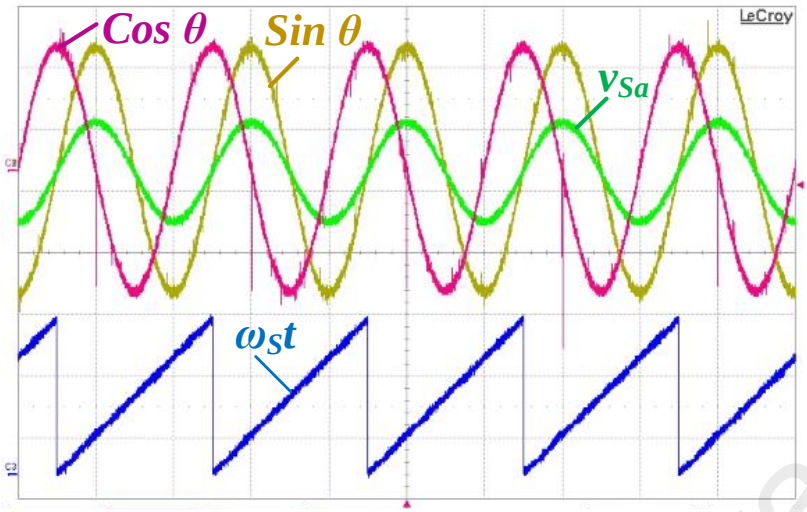


Figure 3.10: PLL output at steady state waveform.

3.5.2 Controller reference generator

To control the system output reference voltage of the PWM-VSI, the control system senses the three-phase instantaneous supply currents (i_{Sa} , i_{Sb} , i_{Sc}) by using a current sensor model (LA55-P/SPI Hall-effect) and three-phase supply *voltages* (v_{sa} , v_{sb} , v_{sc}) *using* voltage sensor model (LEM LV25-P Hall-effect). Hereafter, both the sensed signals are sampled to analog to digital converter (ADC ports) at fixed sample rate and loop time.

3.5.2.1 Synchronous reference frame method

The harmonic content of the load is extracted from the distorted main line current, by means of synchronous reference frame (SRF) (Cho, Oh, Kim, & Kim, 2007). The SRF method is adopted to calculate the reference current in the three-phase APF system as depicted in Figure 3.11. The SRF method operate the transformation process of *abc*-vectors into synchronously rotating direct (*d-axis*) and quadrature axis (*q-axis*) reference frame. By utilizing the Clarke transformation and Park transformation, the three phase supply current (vectors) are mapped into the *dq*-frames at the fundamental frequency ($\omega 1$).

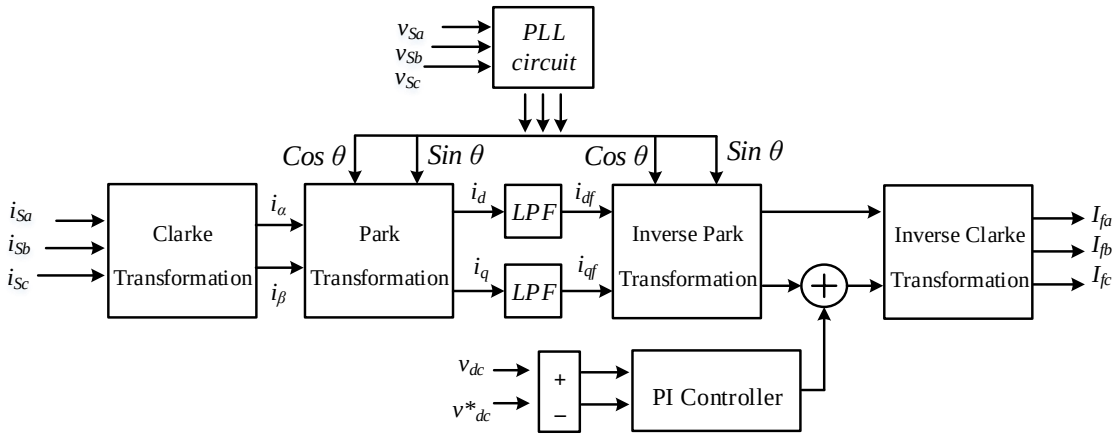


Figure 3.11: Block diagram of synchronous reference frame control scheme.

In order to calculate the harmonic components of the mains current, using the Clarke transformation, the three-phase instantaneous currents is transformed into the *abc*-axis of the harmonic components and further into the stationary *αβ*-axes. Here the vectors are transformed from stationary reference frame into the synchronously rotating reference frame by utilizing Park transformation. Clarke's transformation matrix is represented as;

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \\ 0 & \frac{\sqrt{3}}{\sqrt{2}} & -\frac{\sqrt{3}}{\sqrt{2}} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{3.42}$$

Followed by the Park transformation, the phase angle (θ) of the supply voltage is calculated by the phase lock loop (PLL) circuit, to transform the *αβ*-components into the *dq*-coordinate system, here transformation matrix is given as;

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \mathrm{P} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{3.43}$$

However, the combine operation of both the Clarke transformation and Park transformation will result in the synchronous transformation matrix, as shown in equation (3.44).

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (3.44)$$

In order to separate harmonic and fundamental components, the fundamental component of the mains current operate as a DC signal, once the current vectors are transformed into synchronously rotating *dq*-reference frame, then the harmonic components will operates as AC signals rotating with a constant angular frequency, as shown in Figure 3.12.

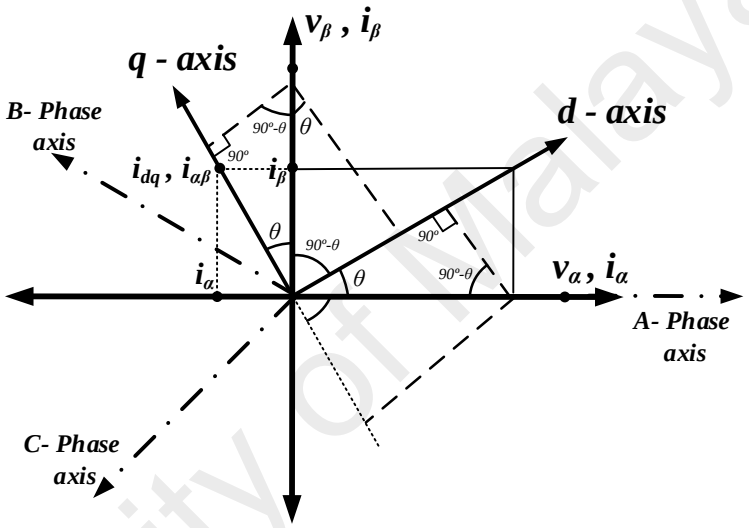


Figure 3.12: Voltage and current characteristics in different reference co-ordinates

Using the low pass filter (LPF), the fundamental frequency currents is separated from the harmonic currents. Therefore, the current in the *dq*-frame can be decomposed into the instantaneous active and reactive current, as explain in equation (3.45).

$$i_d = \bar{i_d} + \tilde{i_d} \quad (3.45)$$

$$i_q = \bar{i_q} + \tilde{i_q}$$

where $\bar{i_d}$ and $\bar{i_q}$ are DC component of load current in *d* and *q* axis, $\tilde{i_d}$ and $\tilde{i_d}$ are AC component of load current respectively. The division of the AC and DC can be obtained using the low pass filter (LPF), resulting the compensating reference signals in *d* and *q* axis are obtained as:

$$i_d^* = \widetilde{i_d} \tag{3.46}$$

$$i_q^* = \widetilde{i_q}$$

The reference signals current in *dq*-reference frame are calculate by giving the harmonic components into inverse park transformation matrix will give back the *abc*-reference frame, given in equation (3.47).

$$\begin{bmatrix} i_a^* \\ i_b^* \\ i_c^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\omega_s t) & -\sin(\theta) \\ \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) \\ \cos(\theta + \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix} \tag{3.47}$$

Furthermore, the inverse transformation from rotating frame into stationary frame is achieved by the following equation

$$\begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{\sqrt{2}} & \frac{\sqrt{3}}{\sqrt{2}} \\ -\frac{1}{\sqrt{2}} & -\frac{\sqrt{3}}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} \tag{3.48}$$

To drive the VSI, the switching pulses are generated by modulating the reference currents signals compared with the actual currents signals.

3.5.3 Feedback control method

In feedback control, the three phase instantaneous supply currents (i_{Sa}, i_{Sb}, i_{Sc}) are detected and inputs to the control system. As shown in Figure 3.13, using the reference frames, it converts three-phase supply current into a two-phase instantaneous active i_d and instantaneous reactive i_q currents at a fundamental frequency of $\omega 1$.

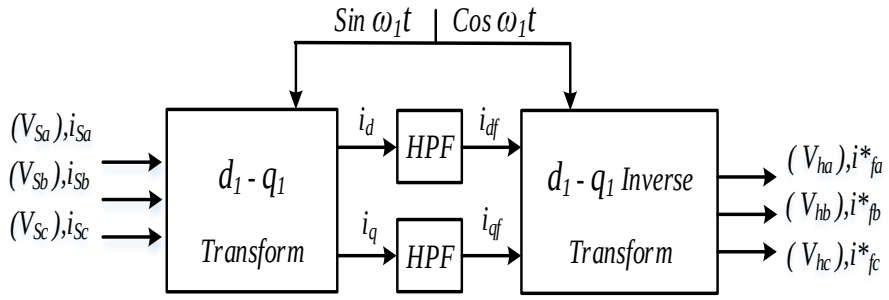


Figure 3.13: Block diagram of the harmonic voltage and current detection scheme.

This synchronous rotating frame is in phase with the positive sequence of three-phase supply voltages (v_{Sa}, v_{Sb}, v_{Sc}) by using the PLL. The zero sequence is neglected because of the three-phase system and the VSI provides the AC voltage to damp the system harmonics (Victor Fabián Corasaniti et al., 2009).

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin(\omega_s t) & \sin(\omega_s t - \frac{2\pi}{3}) & \sin(\omega_s t + \frac{2\pi}{3}) \\ \cos(\omega_s t) & \cos(\omega_s t - \frac{2\pi}{3}) & \sin(\omega_s t + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_{Sa} \\ i_{Sb} \\ i_{Sc} \end{bmatrix} \tag{3.49}$$

The active and reactive quantities are decomposed into DC and AC values at the fundamental ω1 (ω1=50Hz) and harmonics frequencies with accurate phase angle (θ) to track the utility voltage.

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} i_{d_{DC}} \\ i_{q_{DC}} \end{bmatrix} + \begin{bmatrix} i_{d_{AC}} \\ i_{q_{AC}} \end{bmatrix} \tag{3.50}$$

It decomposed the supply currents into the instantaneous active current component i_d and reactive i_q current components. The fundamental component is a DC signal quantities, and the harmonics component is AC signal components respectively.

$$\begin{bmatrix} i_{d_{AC}} \\ i_{q_{AC}} \end{bmatrix} = \begin{bmatrix} i_d \\ i_q \end{bmatrix} - \begin{bmatrix} i_{d_{DC}} \\ i_{q_{DC}} \end{bmatrix} \tag{3.51}$$

Two second-order high-pass filters (HPFs) at cut-off (50 Hz) frequency is designed to extract the AC current harmonics $i_{d_{AC}}$ and $i_{q_{AC}}$. The sampling time delay of 50μs for the

digital filter is short enough to be neglected for calculation. This filter delay effects the dynamic voltage damping performance of the APF (Yeh & Manjrekar, 2007). At the end of the operation, the supply harmonics current components are regenerated by the inverse *d-q* transformation operation.

$$\begin{bmatrix} i_{fa} \\ i_{fb} \\ i_{fc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin(\omega_s t) & \cos(\omega_s t) \\ \sin(\omega_s t - \frac{2\pi}{3}) & \cos(\omega_s t - \frac{2\pi}{3}) \\ \sin(\omega_s t + \frac{2\pi}{3}) & \cos(\omega_s t + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix} \tag{3.52}$$

The APF parameter and characteristics are dependent upon the gain K value. As notice, the voltage reference v_{AF}^* of each phase is amplified by the gain K for right gate switching.

$$v_{AF}^* = K \times i_{f_{abc}} \tag{3.53}$$

3.5.4 DC-bus voltage control

For harmonic component generator, a proportional integral (PI) control scheme is used to build and maintain the required voltage level at the DC-link capacitor of the PWM inverter. To maintain the constant voltage level, it leads the current to the DC capacitor eliminating the need of external power source. During APF operation, the excessive absorption of the active power will affect the filtering operation and increasing the DC side voltage levels. To control the loss inside the APF and to stop the excess flow of DC voltage. The proportional integral (PI) controller regulate the DC-voltage and delivers the active power to the DC-link capacitor. The overall block diagram of the DC voltage control is illustrated in Figure 3.14.

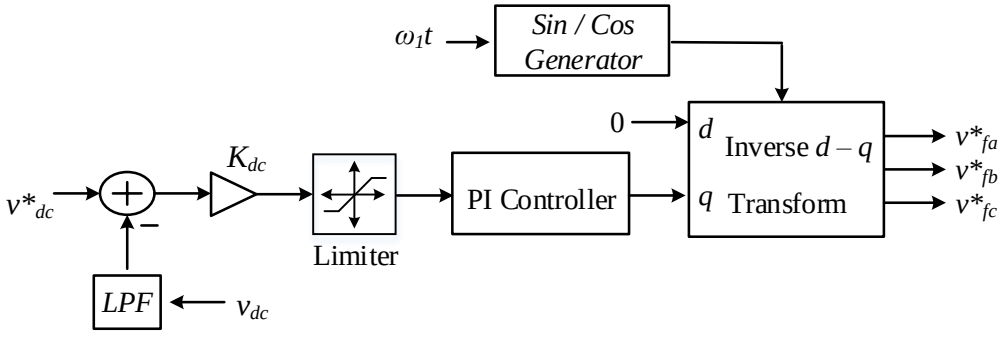


Figure 3.14: Block diagram of the DC-bus voltage.

The APF generate the active power in order to control the fundamental AC voltage in phase with the leading current. However, this active power is the product of the leading fundamental current and AC voltage controlled. The leading fundamental current is flowing into the passive filter and the fundamental AC voltage is produces by the APF. The PI controller, amplifies the error between the permanent reference DC-link voltage (v_{dc}^{*}) and measured DC-link voltage (v_{dc}) to reference output level as;

$$i_q^* = K_p \times (v_{dc}^* - v_{dc}) + \frac{\mathrm{K_I}}{s} \times (v_{dc}^* - v_{dc}) \tag{3.54}$$

The DC value of the reactive current $i_{q_{DC}}$ of the quadrature axis is controlled and direct axis is set to zero value. As a result, the reference current (Δi_{d1}) is added into the reactive current component i_{dh}, as explain in Figure 3.14. As noticed, the DC-bus voltage is sensed and compared with the reference voltage signal. The output error is feed into the quadrature axis of the inverse transformation in order to generate a three-phase fundamental voltage reference. The output error is multiple with the control gain (K) to amplify the signal and feed into the limiter. In some cases, a limiter is added to prevent the sudden changes and for smooth transient response in the DC-bus voltage. However, the limiter range is selected according to the maximum fundamental peak to peak voltage of the control signal and to prevent the numerical saturation of the digital controller like DSP or *dSPACE*. In addition, a low pass filter LPF can be used to eliminate the ripples and harmonic components in the detected DC voltage v_{dc}.

3.5.4.1 Calculating the $\mathbf{K_p}$ abnd $\mathbf{K_I}$ gains

The proportional integral (PI) controller maintains the harmonic current time derivatives for the active filtering operation. To maintain the constant DC-link voltage level, the controller parameters are estimated and the transfer function for PI compensator is defined in equation (3.55);

$$G_v(s) = K_p + \frac{K_I}{S} \tag{3.55}$$

The proportional and integral gains are derived using $K_p = (2.\varsigma.\omega_{nv}.C_{dc})$, it determines the dynamic response of the DC-link voltage controller and the integral gain is derived using $K_I = C_{dc}.\omega_{nv}^2$, which also determines its settling time (Rahmani et al., 2010). The PI controller provide critical damp regulation due to stable DC-link voltage with $\varsigma = 1$ or the optimal value of $\sqrt{2}/2$. The reference signal is to be set high at 300 V, limiting the high rating voltage of IGBTs devices. However, the voltage reference is maintained higher than the peak value of the AC supply voltage. Therefore, the proportional (K_p) and integral (K_I) gain values are considered as 0.2 Ω^{-1} and 31 Ω^{-1}.

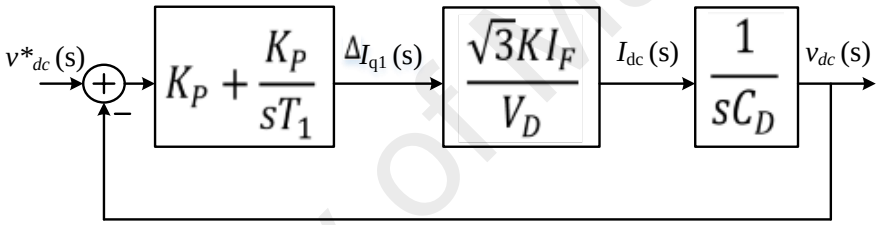


Figure 3.15: Block diagram of the DC-link voltage control.

The transfer function (Figure 3.15) is presented as second order lag system (Tangtheerajaroonwong et al., 2007) is given as follows:

$$V_c^*(s) = \left(K_P + {}^{K_I}/_{ST_1}\right)\left(\frac{\sqrt{3}KI_F}{V_D}\right)\left(\frac{1}{SC_D}\right) \tag{3.56}$$

$$\frac{v_{dc}(s)}{v_{dc}^*(s)} = \frac{\frac{\sqrt{3}KK_PI_F}{V_DC_D}S + \frac{\sqrt{3}KK_PI_F}{V_DT_1C_D}}{S^2 + \frac{\sqrt{3}KK_PI_F}{V_DC_D}S + \frac{\sqrt{3}KK_PI_F}{V_DT_1C_D}} \tag{3.57}$$

The damping ratio ς, and the natural angular frequency ω_n, can be considered by;

$$\varsigma = \frac{1}{2}\sqrt{\frac{\sqrt{3}KK_PT_1I_F}{V_DC_D}}, \quad \omega_n = \frac{1}{2}\sqrt{\frac{\sqrt{3}KK_PI_F}{V_DT_1C_D}} \tag{3.58}$$

Here, the voltage reference is kept constant. For simplicity, all the values are assumed as $i_{d_1=}\, i_{q_1=}\, \mathrm{v}^*_{\mathrm{AF}=0}$, assuring that the output signal of the voltage control Δi_{q_1} directly determine the reference signal $\mathrm{v}^*_{\mathrm{AF}_A}$, $\mathrm{v}^*_{\mathrm{AF}_B}$, $\mathrm{v}^*_{\mathrm{AF}_C}$, as follow;

$$\begin{bmatrix} i_{CA} \\ i_{CB} \\ i_{CC} \end{bmatrix} = \sqrt{\frac{2}{3}} K \begin{bmatrix} \cos(\omega_1 t) & -\sin(\omega_1 t) \\ \cos(\omega_1 t - \frac{2\pi}{3}) & -\sin(\omega_1 t - \frac{2\pi}{3}) \\ \cos(\omega_1 t + \frac{2\pi}{3}) & -\sin\,(\omega_1 t + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} 0 \\ \Delta i^*_{q_1} \end{bmatrix} \tag{3.59}$$

$$= \sqrt{\frac{2}{3}} K \Delta i^*_{q_1} \begin{bmatrix} -\sin(\omega_1 t) \\ -\sin(\omega_1 t - \frac{2\pi}{3}) \\ -\sin\,(\omega_1 t + \frac{2\pi}{3}) \end{bmatrix}$$

The RMS voltage reference of each phase, $\mathrm{v}^*_{\mathrm{AF}_A}$ is given by

$$\mathrm{v}^*_{\mathrm{AF}_A} = \frac{1}{\sqrt{3}} K \Delta i^*_{q_1} \tag{3.60}$$

So, the active filter delivers the full active power from the three-phase power supply, P_{AF} is given by

$$P_{AF} = \frac{1}{\sqrt{3}} K I_F \Delta i_{q1} \tag{3.61}$$

The APF is assumed to produces zero loss, so the $\mathrm{v}^*_{\mathrm{AF}_{ABC}}$, are in phase with the phase current flowing into the APF. Here, the K= 11 Ω, $I_F = \sim$10 A, and $v_{dc} = 300$ V. The APF delivers the P_{AF}, to the DC-link capacitor without any losses, Therefore the Laplace form of the DC current flowing into the DC-link capacitor can be derived as follows:

$$I_{dc}(s) = \frac{\sqrt{3} K I_F}{V_D} \Delta \mathrm{I}_{q1}(s) \tag{3.62}$$

3.6 Summary

The proposed configuration uses a two-leg bridge structure and decreases the number of switching power devices in the power converter, thereby minimizing the system size and cost. The feasibility of the power distribution system is improved by eliminating the transformer and reducing the power component to provide accurate performance, reduced volumetric size, and low cost compared with other existing APF topologies. The mathematical modeling and design procedure of both the filters has been explained in

detail. The series LC PF tuned at the 5th and 7th order harmonic frequencies improves the active filtering capability. Also, the series AC coupling inductors overcome the fixed reactive power compensation caused by the fixed value of the LC filter leg. Lastly, a control algorithm scheme ensures the regulated sinusoidal voltage, phase amplitude, and low THD in the power distribution system along with DC-link voltage control.

CHAPTER 4: HARDWARE IMPLEMENTATION, RESULTS AND DISCUSSION

4.1 Introduction

This chapter presents a hardware set-up and experimental verification of proposed novel three-phase SAPF system based on reduced switch count and transformer-less configuration. The proposed prototype (2.2 kVA) is tested in the laboratory to verify the results in terms of its superior performance and analytical reasoning with the extensive simulation and experimental verifications. This chapter also investigates and recorded the different parameter results such as total harmonic distortion (THD), harmonic mitigation, constant DC-link voltage and reactive power compensation under steady state and dynamic load change conditions. Firstly, the test rig overview, inverter design specifications and hardware implementation are given. Finally, based on the define specifications, the simulation and experimental results are briefly described. Evaluating the steady state analysis, dynamic load change, reactive power compensation simulation and experimental results and comparison of cost analysis are explained.

4.2 Hardware implementation

To validate the performance and concept of switch reduced count modularity, this section presents the construction details of laboratory APF prototype. The experimental test rig setup mitigates the current harmonics and compensate the reactive power compensation of a 5 kW nonlinear load, according to the IEEE-519 standard. An experimental setup is constructed and tested at University Malaya (UM) Electrical Engineering Department in Power Electronics and Renewable Energy Laboratory (PEARL). The simulation and experimental test results are discussed later in this chapter.

4.2.1 Experimental system overview

The experimental prototype of the proposed shunt APF system can be divided into main four parts: the converter power stage, interfacing passive components, software (simulation) and control circuits. The converter power stage part consists of two-leg VSI with DC-link capacitor. The interfacing passive components part consists of filters inductors, line reactors, pre-charge units and filter circuit breakers. The PC system run the software simulation to control the electronic circuitry. Finally, the control circuits is divided into signal conditioning boards, connects panel board (ADC-D I/O), DS1104PC protection board, gate driver board and circuit breaker driver board. Figure 4.1 shows the block diagram of the main four elements in the experimental setup, installed in shunt position at the PCC to a three-phase distribution network system.

The detected quantities utilizes for the VSI-APF controller system are as follow; the power distribution grid voltages vs_{abc}, the grid currents is_{abc}, and the DC-link capacitor voltage v_{dc} is feed into a *dSPACE* modular system unit based on a *DS1104* processor board through A/D converters. Different processor boards drives the communication with a personal computer (PC) and power devices of the two-leg VSI-APF system. Interpret instructions from Matlab-*Simulink* is carried out to the PI controller and feedback controller to test the proposed APF system.

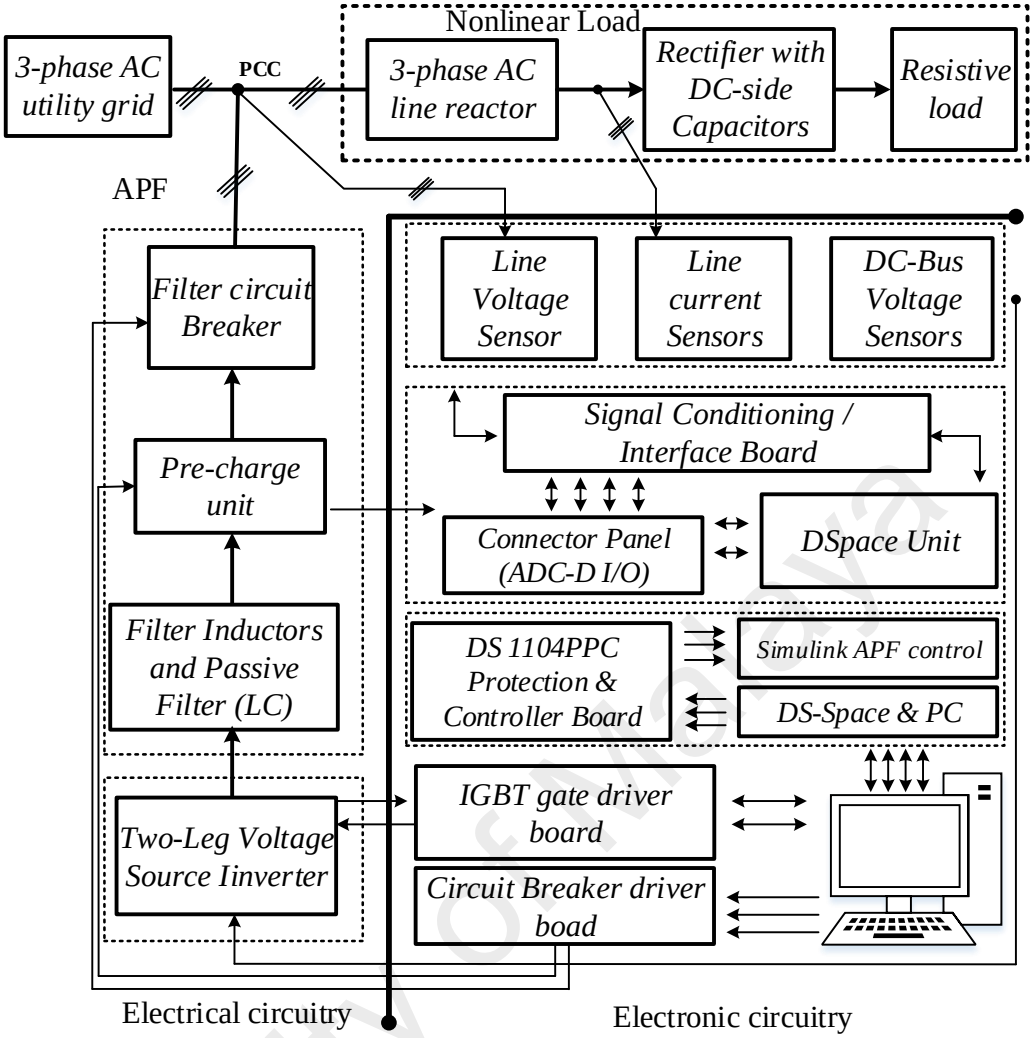


Figure 4.1: The basic electrical power circuitry of the overall APF system.

4.3 Hardware schematic

For the purpose of laboratory evaluation, the experimental setup is tested in laboratory and demonstrate in hardware to show the reduced switch count structure accuracy, while connected to a 200V, 50 Hz three-phase AC distribution power grid. The electrical power circuitry of the overall system is shown in Figure 4.2. In detail, a 2.2 kVA three-phase VSI is connected to full-bridge diode uncontrollable rectifier module SEMIKRON-SKD (1600V, 100A) and utility grid at the point of common coupling (PCC) for grid-connected application. For protection purpose, the proposed APF is installed with three-phase 30A automatic fuse, three-phase 30A circuit breaker and three-phase in-line smoothing reactor (L_{AC} = 3 mH/phase, 45 A RMS current rating), which stop the back flow of input inrush

current and higher distortion towards the utility grid. The two-leg of the VSI inverter is installed in series with a coupling inductors L_F, while the reduced switch-leg is connected in series with a passive filter (2.0 kVAR) fabricated as per design specification.

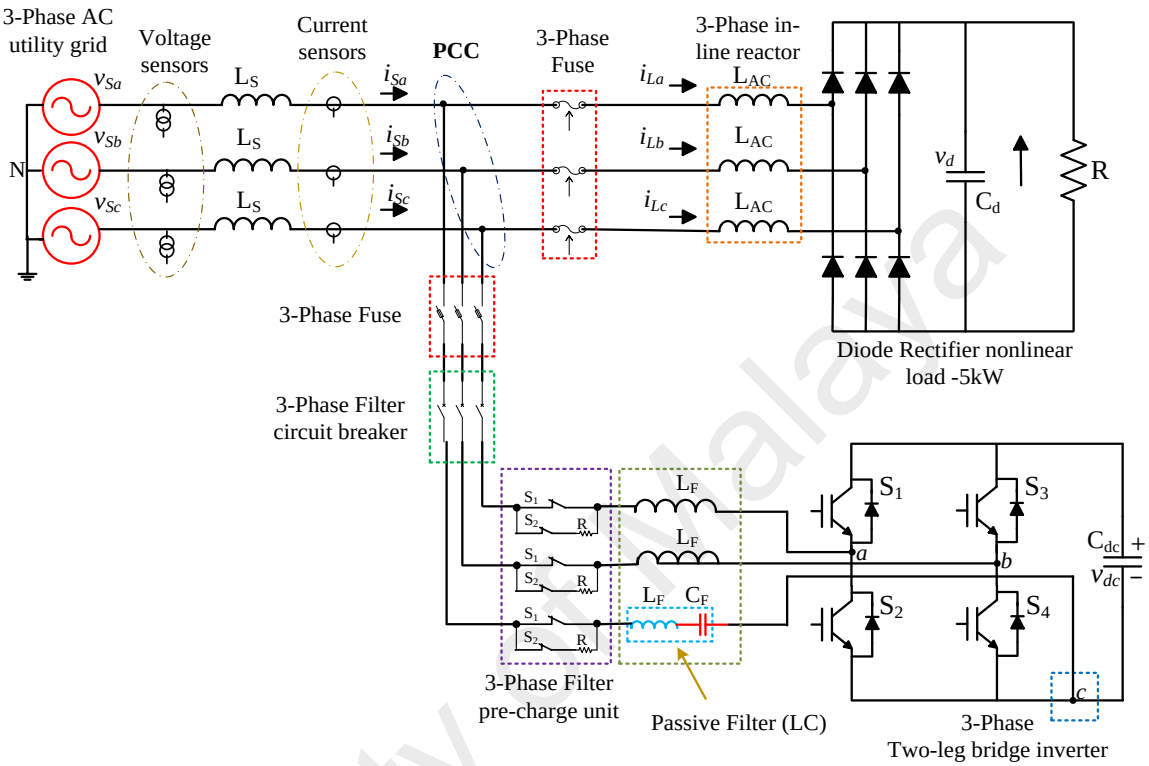


Figure 4.2: The electrical power circuitry of the overall APF system.

4.3.1 Start-up procedure

The prototype startup insertion operation is considered in Figure 4.2, interfacing with the distribution grid. Prior to starting, the switches (S_1 and S_2) or magnetic contractor are switched off. For protection purpose, the proposed APF is installed with three-phase automatic fuse, circuit breaker and transmission line smoothing reactor to stop the inrush current and higher distortion. During the start-up of the uncontrolled rectifier or when the switches are closed, the current flow through the small sized 10 Ω resistor R and 40 W power rating each to prevent the inrush current flowing into the filter and to stop the premature charging of the DC-link capacitor. The mandatory condition for this insertion procedure, the two upper top switches of the IGBTs inverter must be turned on and the

lower two IGBTs switches must be turned off. After some cycles (400 ms), the switch S_2 is turned on and switch S_1 is off to directly connect the APF system to the power grid.

4.4 Prototype description

Figure 3.9 show the operation controller scheme of the laboratory prototype of transformer-less SAPF system. All the parameters and each components are highlighted in Figure 3.1. The voltage source inverter (VSI) consists of two-leg four modules of insulated gate bipolar transistor (IGBTs) devices rated at 600 V, operating at 20 kHz switching frequency. The model 61511 from Chroma ATE. INC instruments has been used as a power supply. Hereinafter, the prototype is tested at 200V AC source connected directly with the grid for flexible testing. The design load is a three-phase diode rectifier at DC-side with smoothing capacitor $C_d = 1500\ \mu F$ and resistor of 40 Ω. The APF system operates at the maximum rating of 2.2 kVA, consisting of 5 kW diode rectifier load, with DC-link capacitor value $C_{dc} = 4700\ \mu F$ and DC-link voltage $v_{dc} = 300\text{V}$. Therefore, the DC-link capacitor rating is designed to operate at voltage ripple less than 10%.

The two-leg of the VSI inverter is installed in series with a coupling inductors L_F, while the reduced switch-leg is installed through a passive filter (2.0 kVAR). Two sets of PFs are tuned at 5^{th} and 7^{th} harmonics frequencies to mitigate the current harmonics and compensate the reactive power compensation. To compensate the 5kW diode rectifier load system, a 2.2kVA APF system and 2.0kVAR PFs system is satisfactory to mitigate the harmonics and reactive power compensation. The complete experimental and simulation system parameters are listed in Table 4.1, Table 4.2, and Table 4.3.

Table 4.1: Experimental system specification.

Parameters	Value	Unit	Symbol
Diode Rectifier rating	5	kW	-
line to line RMS voltage	200	V	(v_s)
Output RMS voltage	200	V	V_{out}
Grid Frequency	50	Hz	-
Supply Inductor	0.21	mH	(L_s)
AC load inductor	3	mH	(L_{AC})
Rectifier DC capacitor	1500	μF	(C_d)
Nonlinear load resistor	40	Ω	(R)

Table 4.2: Parameters of the APF.

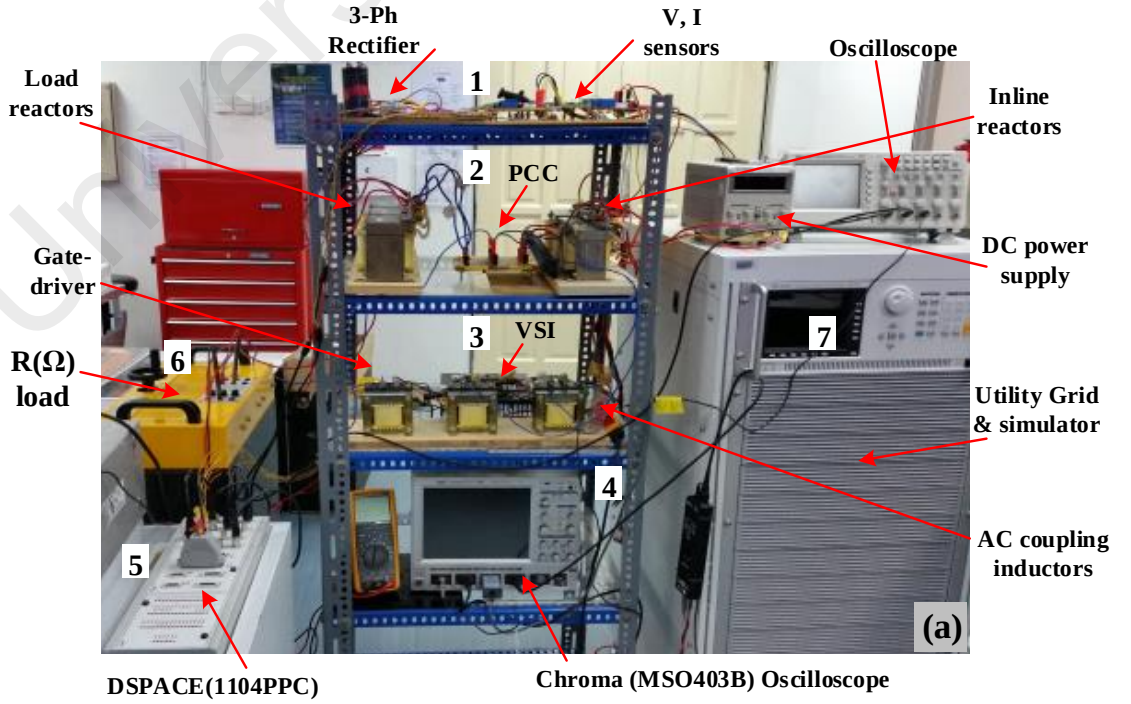
Parameters	Value	Unit	Symbol
Active filter rating	2.2	kVA	
Filter AC Inductor	1.9	mH	(L_F)
DC capacitor of APF	4700	μF	(c_{dc})
DC voltage of APF	300	V	(v_{dc})
HPF Cut off frequency	50	Hz	(F_{HPF})
Gain	11	Ω (p.u)	(K)
Switching Frequency	20,000	Hz	f_{sw}
Switches Types	Infineon IKW75N60T		$S_1 - S_4$

Table 4.3: Parameters of the PF.

Parameters	Value	Unit	Symbol
Passive filter rating	2.0	kVAR	
Filter inductor	1.9	mH	(L_F) (5^{th})
Filter Capacitor	200	μF	(C_F) (5^{th})
Filter inductor	1	mH	(L_F) (7^{th})
Filter Capacitor	200	μF	(C_F) (7^{th})
Resonance frequency (PF)	258	Hz	(5^{th})
Resonance frequency (PF)	357	Hz	(7^{th})
Quality Factor	57	-	(Q)

4.5 Proposed Prototype

Figure 4.3 (a, b) shows the picture of the laboratory prototype of the manufactured APF to validate the performance. In the figure, the hardware prototype is constructed and explain in the following sections: (1) Non-linear rectifier load, and (*V, I)* Sensors, (first) shelf. (2) Inline and load transmission line reactors and PCC (second) shelf. (3) The complete inverter system is shown as two-leg bridge structure inverter, DC-link capacitor, gate-drives and AC coupling inductors. The devices includes are detail as follow: IGBT module (IKW75N60T) which is a (600 V, 85 A) four single module from Infineon, its gate driver SKHI 61R manufactured by SEMIKRON, and the 1500 μF 450 (V_{dc}) DC-link capacitor, LC-filter which consists of a 1.9 mH and 1 mH, 45 A three-phase inductor, and two 200μF 400 V capacitors (third) shelf. (4) Chroma (MSO4034B) oscilloscope (fourth) shelf. (5) *dSPACE* (1104PPC), and control desk (PC). (6) Resistive 40 Ω load. (7) Utility grid, oscilloscope, DC power supply and grid simulator. The list of components used to construct the laboratory prototype is summarizes in Table 4.4.



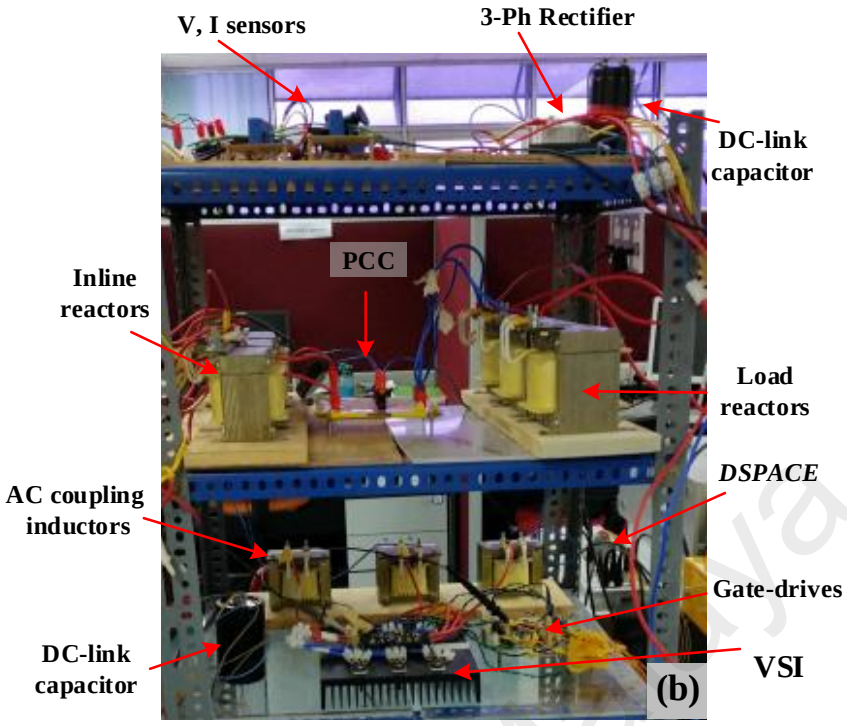


Figure 4.3: (a) Hardware circuit of proposed APF system. (b) Zoom snapshot of VSI, DC-bus capacitor and other components.

Table 4.4: List of key components tested in the APF.

Device	Part / Value	No. of Devices
DSPACE	1104PPC	1
IGBT	Infineon IKW75N60T	4 each
IGBT Drivers	SEMIKRON-SKHI 61R	4 each
Heat sink	FISCHER ELEKTRONIK 99AS	1 each
Current sensors	Hall-Effect LA55-P/SP1	2 each
Voltage sensors	Hall Effect LEM LV25-P	3 each
Inline Reactors	Sendust, Kool Mμ, Magnetics Inc	6 each
Filter AC Inductor	Schaffner RWK 305 Series 400 V/ 45A	3 each
DC-bus capacitor	EPCOS Electrolytic Capacitors 2200 μF/450V	1 each
Rectifier DC capacitor	KEMT Electrolytic Capacitors 2200 μF/450V	1 each
Filter inductor	Toroidal; High Frequency 2.0Uh, 1.0Uh;Tol +/-10%;Cur 9.7A;Thru-Hole	3 each
Filter Capacitor	EPCOS Polypropylene film PH450/4.7uF	2 each
3-Ph bridge rectifier	SKHI 61R, SEMIKRON	2 each

4.6 Simulation and experimental verification

Early, the hardware description of the laboratory test rig set-up was provided in the previous section. The aim of this study is to test the harmonics attenuation performance and enhance reactive power compensation capability of the proposed APF model. The measured experimental results including the utility line current THD*i*, line voltage THD*v*, cost and size analysis, and PFs installed at the PCC in terms of reactive power compensation, all these results validate the simulation waveforms. The developed results validates the configured power stage of the full-bridge inverter implemented using the two-leg VSI stage. The system parameters, circuit specifications and control parameters have been listed in Table 4.1, Table 4.2 and Table 4.3 in previous section 4.4.

All the experimental data are recorded by Lecroy Wave Runner 500 MHz digital scope (4-channel). Frequently, the waveforms are recorded in the following sequence: utility voltage v_{Sabc}, utility current i_{Sabc}, load current i_{Labc} filter compensation current i_{Fabc} and DC-link capacitor voltage v_{dc}.

4.6.1 Steady state filtering performance

The steady-state load and step-change load tests are evaluated, by installing a nonlinear three-phase uncontrolled diode rectifier load in parallel with the APF system. The diode rectifier load has been designed according to the IEC and IEEE standards, listing the three-phase diode rectifier circuit specifications in Table 4.1. The measured utility line current THD*i* for the non-linear load is 30.1%, as shown in Figure 4.4.

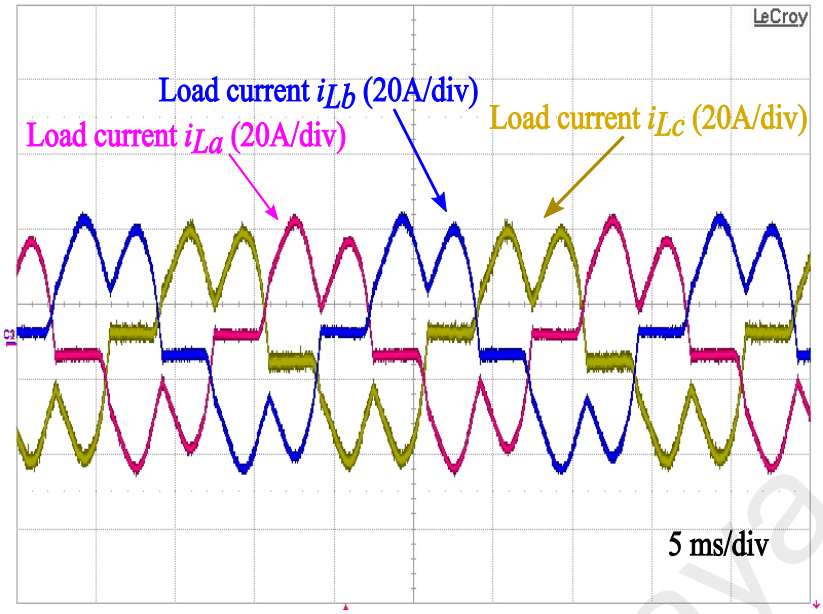


Figure 4.4: Experimental waveform of output current for nonlinear three-phase diode rectifier load.

Prior to the current harmonic compensation, the utility voltage v_{Sa}, load current i_{La}, and source current i_{Sa} are distorted and non-sinusoidal waveforms. Figure 4.5 presents the nonlinear experimental result of the SAPF connected with the diode rectifier load.

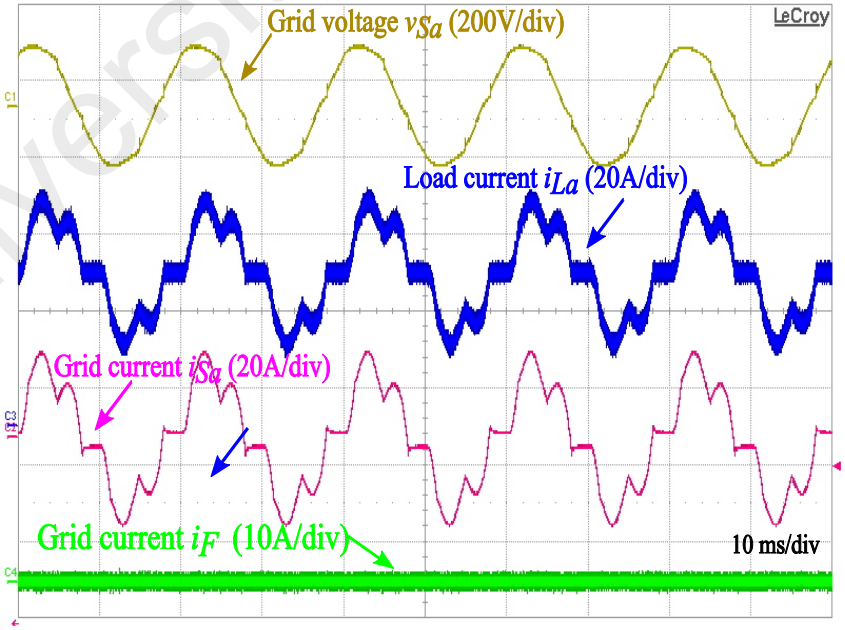


Figure 4.5: Experimental result under for nonlinear load condition a) Utility voltage (THD*v*=4%) b) Load current (THD*i*=30.1%) c) Utility current (THD*i*=4.1%) and d) Filter current.

Figure 4.6 shows the simulation results of the utility voltage, source current, load current, and filter compensating current. Therefore, both the load current and source current is seriously distorted because of the three-phase rectifier load with THD*i* of 30.1%. As observed after compensation, the source current is sinusoidal waveform but load current is distorted waveform connected with the nonlinear load.

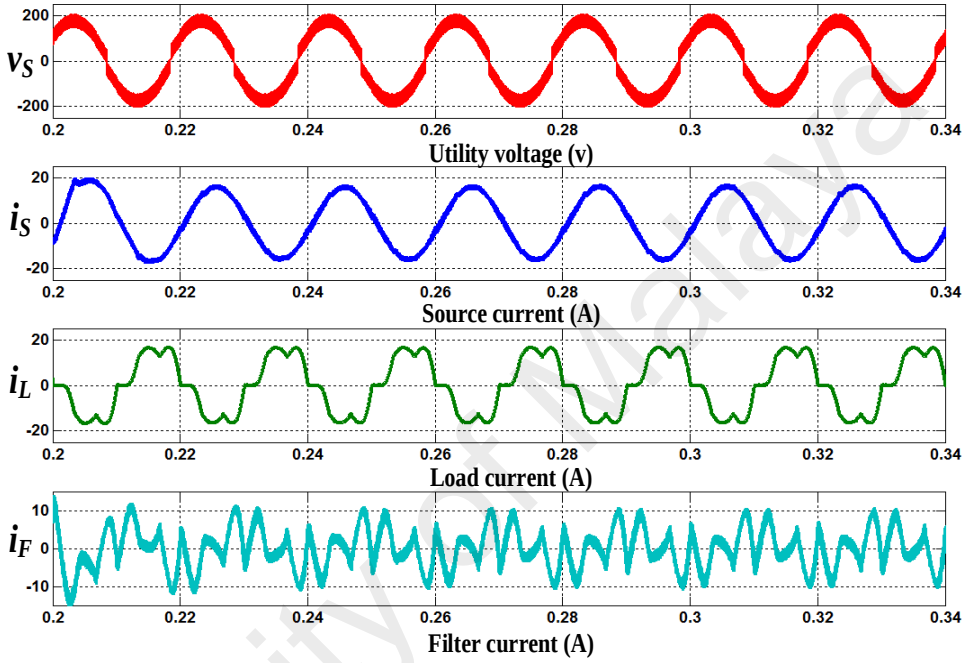


Figure 4.6: Steady state operation of the proposed SAPF a) Utility voltage (THD*v*=4%) b) Utility current (THD*i*=4.1%) c) Load current (THD*i*=30.1%) d) Compensating filter current.

The DC-link voltage of the APF is maintained constant without the need of external DC power supply as depicted in Figure 4.7. At the point of injection, the DC-link voltage rise nearly up to 10% and remain constant during the step change presenting no stability problem. The DC voltage ripple offset at the fundamental frequency is stopped, due to the capacitive effect in phase (a, b) but in phase (c), the LC passive capacitor prevents the DC current flow towards the power supply.

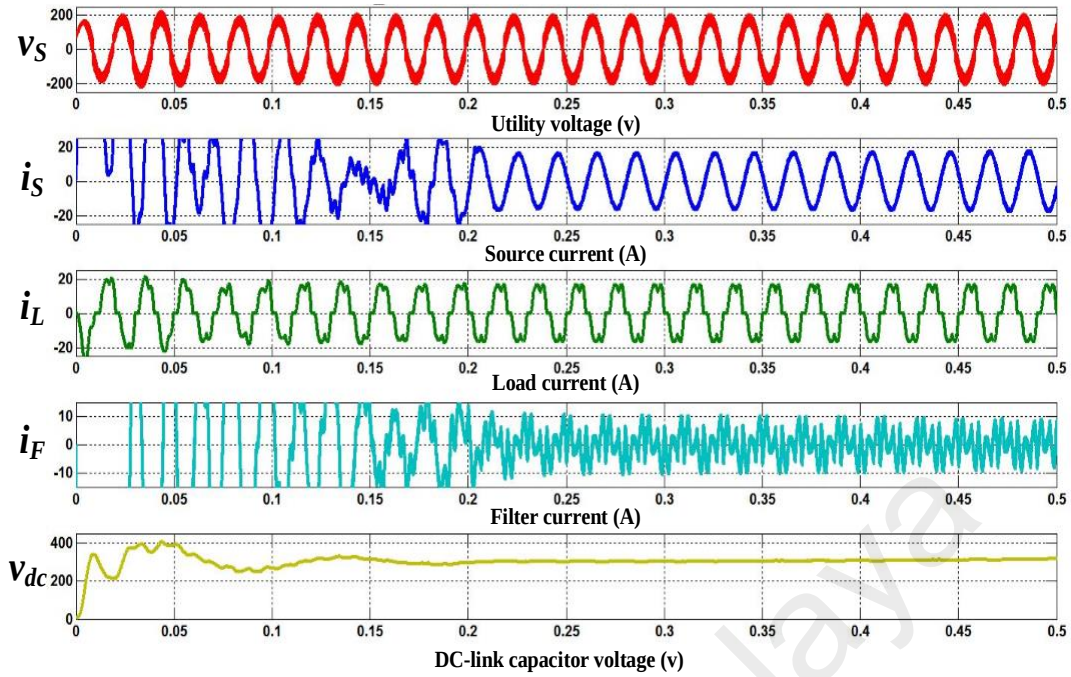


Figure 4.7: Steady state APF operation at point of injection. a) Utility voltage (THD*v*=4%) b) Utility current (THD*i*=4.1%) c) Load current (THD*i*=30.1%) d) Compensating filter current e) DC-link capacitor voltage.

The THD of the utility voltages and utility current shown in Figure 4.6, Figure 4.7 and Figure 4.8 are well below the limits of IEEE 519 standard. The experimental results in Figure 4.8 is compared with the Simulink data to strengthen the simulation results. The comparison results verify the effectiveness harmonic mitigation of the proposed APF system. It can be seen from these results that the THD of the utility current and utility voltage are below (5%) even for severe operating condition. However, for excellent filtering characteristics the control gain is set to a high value (K = 11 Ω). The fundamental voltage to the inverter exhibits large amount of switching ripple because of the PWM. Hence, the series inductor with the power converter eliminates these switching ripples with harmonic compensation.

The harmonic current waveforms verify the effective filtering of the proposed APF; specifically, the utility current THD*i* is reduced from 30.1% to 4.1%, as shown in Figure 4.8. Though, connected with the three-phase rectifier load the load current is distorted but

after compensation, the utility current have been changed to sinusoidal waveform and harmonic load current meet the IEEE 519 standards. Here, the waveforms are recorded in the following order such as; utility voltage v_{Sa}, load current i_{La}, and source current i_{Sa} respectively.

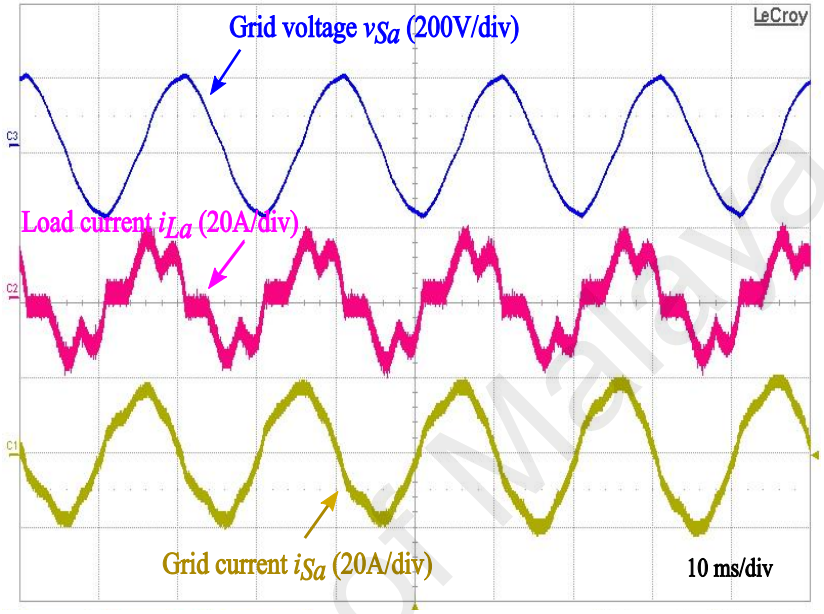


Figure 4.8: Experimental result for the active power filtering mode a) Utility voltage (THD*v*=4%) b) Load current (THD*i*=30.1%) c) Utility current (THD*i*=4.1%).

The output filter compensating current for APF have been shown in Figure 4.9. The waveforms comprises a high order harmonics generated due to switching operation of the two-leg VSI.

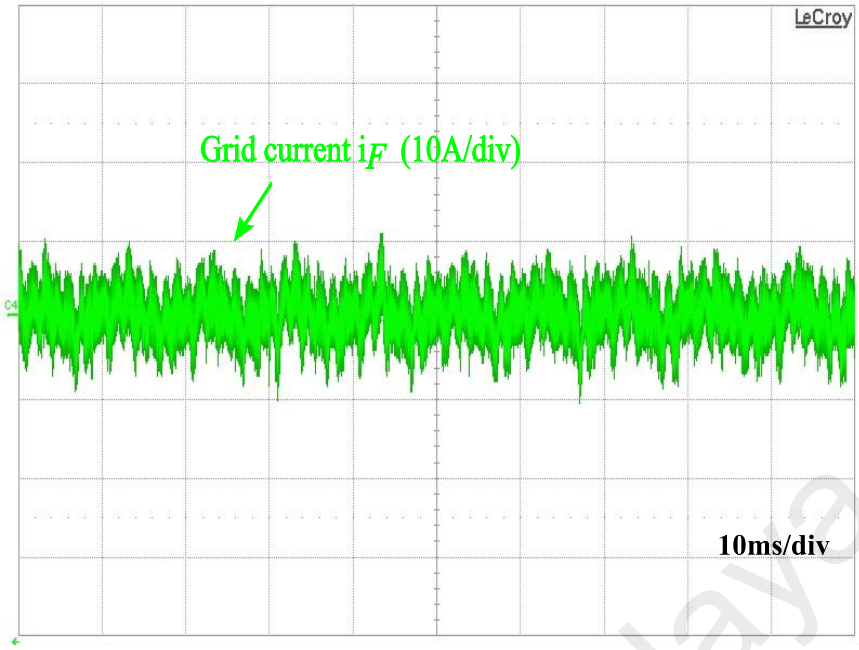


Figure 4.9: Experimental result for the active power filtering mode, Filter compensating current waveforms.

Figure 4.10 shows the constant DC-link voltage across the DC-bus capacitor. The DC-link voltage is kept constant at 300V and it control the voltage references for feedback control loop and enhanced reactive power demand with the minimum value of ripple without amplification phenomenon at dominant harmonic frequency.

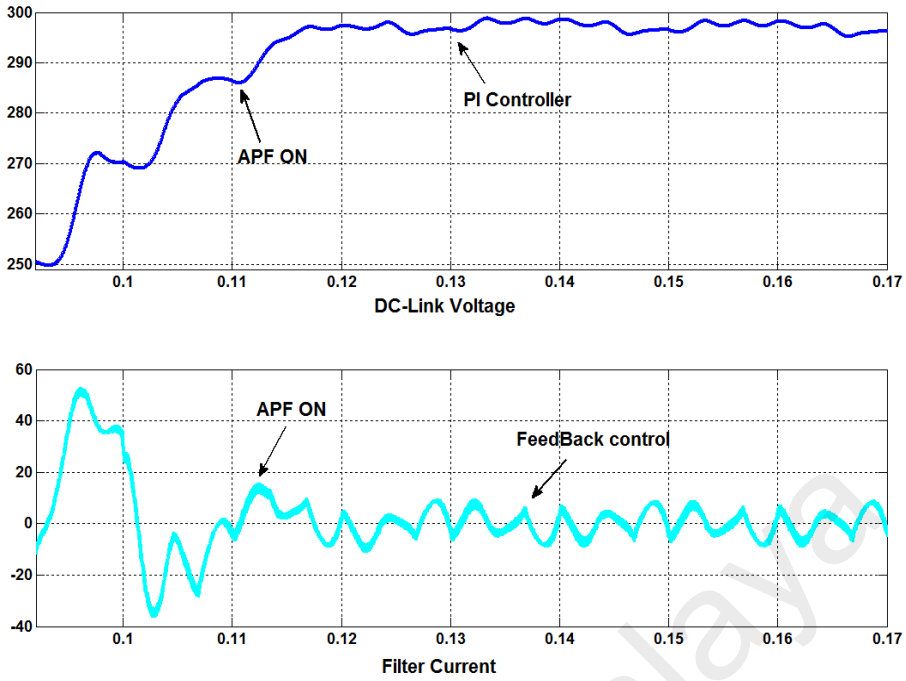


Figure 4.10: DC-link voltage (50V/div), Filter current (100A/div), at filter switched on (t=0.15).

To test the DC-link voltage controller and its stability, the experimental results for DC-link voltage before and after load step-change are shown in Figure 4.11. An appropriate control for DC-bus control, produces a stable DC-bus voltage. Therefore, the switching filter start point after time t=0.12 ms as the APF start the operation.

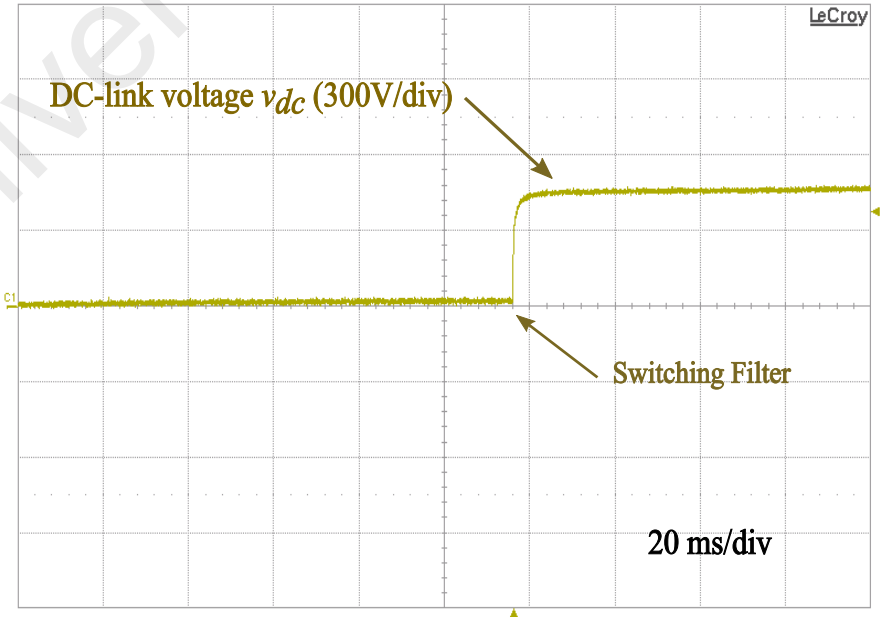


Figure 4.11: a) Testing of DC-link voltage controller b) DC-bus voltage at filter switched on.

To check the proposed APF accuracy and stability, after a time of t=0.12 ms the APF is tested the switching filter start time operation, it inject the filter compensating current into the transmission line. The starting performance of the proposed APF to compensate the reactive power and harmonics current mitigation is depicted in Figure 4.12. The load current and utility current waveforms are seriously distorted but as soon as the active filter is inserted, the utility current is a stable and sinusoidal waveform. The THD of the supply current is dropped from 30.1% (without APF) to 4.1% (with APF) effectively.

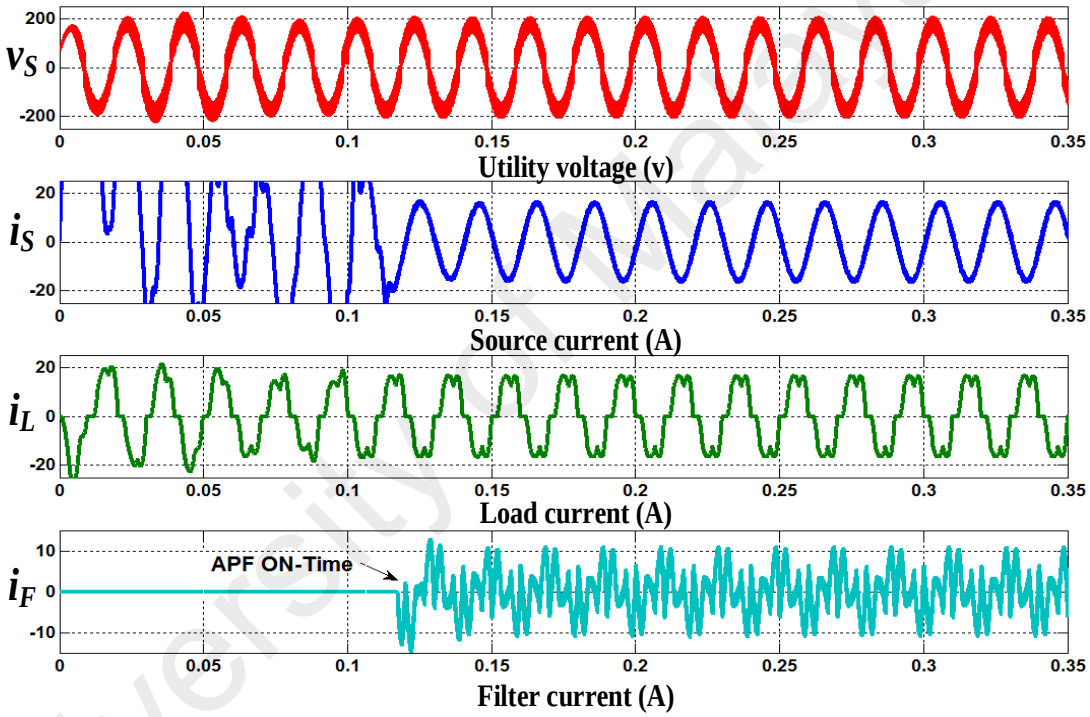


Figure 4.12: Starting performance of the proposed SAPF. a) Utility voltage (THD*v*=4%) b) Utility current (THD*i*=4.1%) c) Load current (THD*i*=30.1%) d) Compensating current at filter switched on.

Figure 4.13 validates the filter waveforms of the three-phase source currents (a, b, c) and three-phase load current. Before harmonic compensation, the three-phase load current is distorted with THD*i* of 31.36%. Later, after compensation the three-phase utility current is sinusoidal waveform and three-phase utility THD*i* reduced to minimum value of 4.86%, 4.73%, and 6.04% respectively. The top three waveforms are recorded as

compensated source currents and lower three waveforms show an uncompensated load current. Furthermore, the harmonic contents of source and load current per phase of three-phase SAPF system are summarizes in Table 4.5.

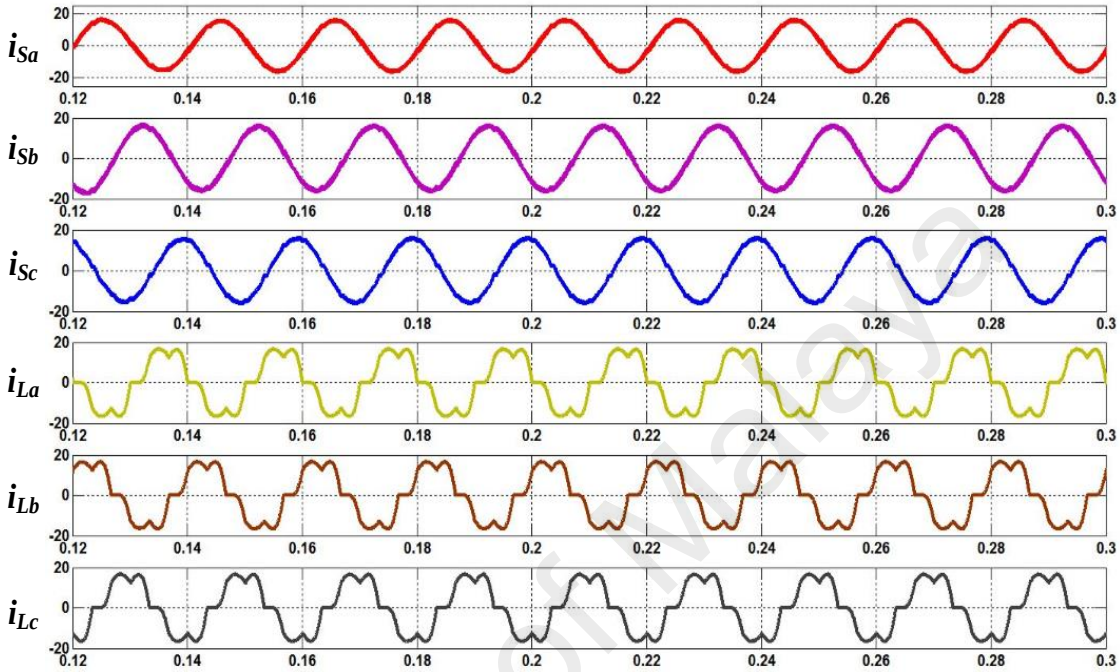


Figure 4.13: Steady state waveforms of the proposed SAPF. Upper three utility current after compensation, and lower three utility current before compensation.

Table 4.5: Source current harmonic contents (5th PF tuned).

Order	**Before Compensation**			**After Compensation**		
Harmonics	Peak current i_{sa} (A)	Peak current i_{sb} (A)	Peak current i_{sc} (A)	Peak current i_{sa} (A)	Peak current i_{sb} (A)	Peak current i_{sc} (A)
Fundamental	100	100	100	100	100	100
3rd	0.2	0.24	0.01	0.2	0.07	0.14
5th	19.51	19.57	19.76	0.9	0.87	0.98
7th	7.29	7.48	7.16	2.13	2.55	4.66
9th	0.03	0.04	0.06	0.08	0.18	0.12
11th	2.64	2.60	2.55	1.45	0.85	2.28
13th	2.13	2.16	2.06	0.68	1.3	1.98
15th	0.05	0.02	0.06	0.1	0.04	0.06
17th	1.32	1.30	1.30	0.77	0.5	1.27
19th	0.98	1.01	0.94	0.33	0.61	0.94
21st	0.02	0.01	0.01	0.18	0.3	0.51
THD	**31.20**	**31.32**	**31.36**	**4.86**	**4.73**	**6.04**

Figure 4.14, shows the harmonic spectrum analysis of the compensated and uncompensated source current, before and after compensation. The two-leg APF model

is coupled with LC PF tuned at 5th order dominant harmonic frequency. Here, after applying the APF and PF filter the THD*i* of the supply current is satisfactory in the phase (a) and phase (b) (<5.0%) respectively, however unsatisfactory performance followed in phase c (>5.0%).

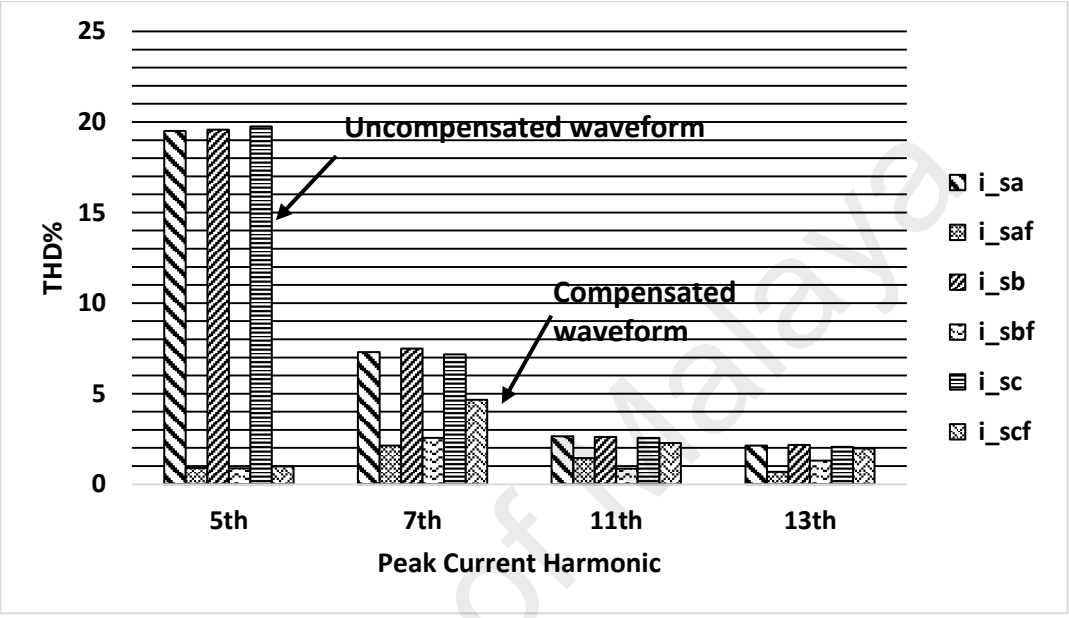


Figure 4.14: Spectral analysis of the source current before and after filtering.

The proposed APF is a low-cost structure and successfully reduces power devices for providing harmonic and reactive power compensation. In verifying this deduction, the utility current in each of the three phases is shown in Figure 4.14. This figure shows that the proposed APF system injects different compensating currents to control the load current demand in each phase. Also, it operates as expected even with reduced switch devices against the critical problems in the power distribution system. Table 4.6 tabulates the harmonic contents of source and load current in each phase of the three-phase SAPF system. The table also illustrates the comparison of the compensating and non-compensating source currents and demonstrates a substantial amount of 5th and 7th harmonic frequencies in the non-compensating source current. However, the system offers the best response at a compensating source current, including fixed load, step load

change, after harmonics and reactive power compensation. In addition, the THD decreases from 30.1% (without APF) to 3.61% (with APF). Therefore, the LC filter tuned at the 5th and 7th harmonic frequencies is installed in phase *c* to stop the flow of non-negligible harmonic amounts in the system.

Table 4.6: Source current harmonic contents (5th and 7th PF tuned).

Order	**Before Compensation**			**After Compensation**		
Harmonics	Peak current i_{sa} (A)	Peak current i_{sb} (A)	Peak current i_{sc} (A)	Peak current i_{sa} (A)	Peak current i_{sb} (A)	Peak current i_{sc} (A)
Fundamental	100	100	100	100	100	100
3rd	0.2	0.24	0.01	0.05	0.09	0.1
5th	19.51	19.57	19.76	0.79	0.97	0.69
7th	7.29	7.48	7.16	0.36	0.41	0.29
9th	0.03	0.04	0.06	0.08	0.12	0.07
11th	2.64	2.60	2.55	0.96	0.54	1.41
13th	2.13	2.16	2.06	0.54	0.98	1.48
15th	0.05	0.02	0.06	0.05	0.1	0.06
17th	1.32	1.30	1.30	0.72	0.39	1.1
19th	0.98	1.01	0.94	0.31	0.52	0.82
21st	0.02	0.01	0.01	0.01	0.05	0.06
THD	**31.20**	**31.32**	**31.36**	**4.06**	**3.93**	**3.61**

The harmonic compensation of the PFs is shown in Figure 4.15 (a), the PF performance is evaluated in on-state and off-state. Table 4.5 shows that the single tuned PF filtering performance is not good against the current harmonics (phase c). Table 4.6 tabulated the harmonic contents of source and load current connected with the PFs set per phase of the three-phase SAPF system. Figure 4.15 (b) and Table 4.6 explain that source THD*i* of the two sets of PFs reduces from 31.36% (without PF) to 3.61% (with PF) against the high-order 5th and 7th harmonic frequencies.

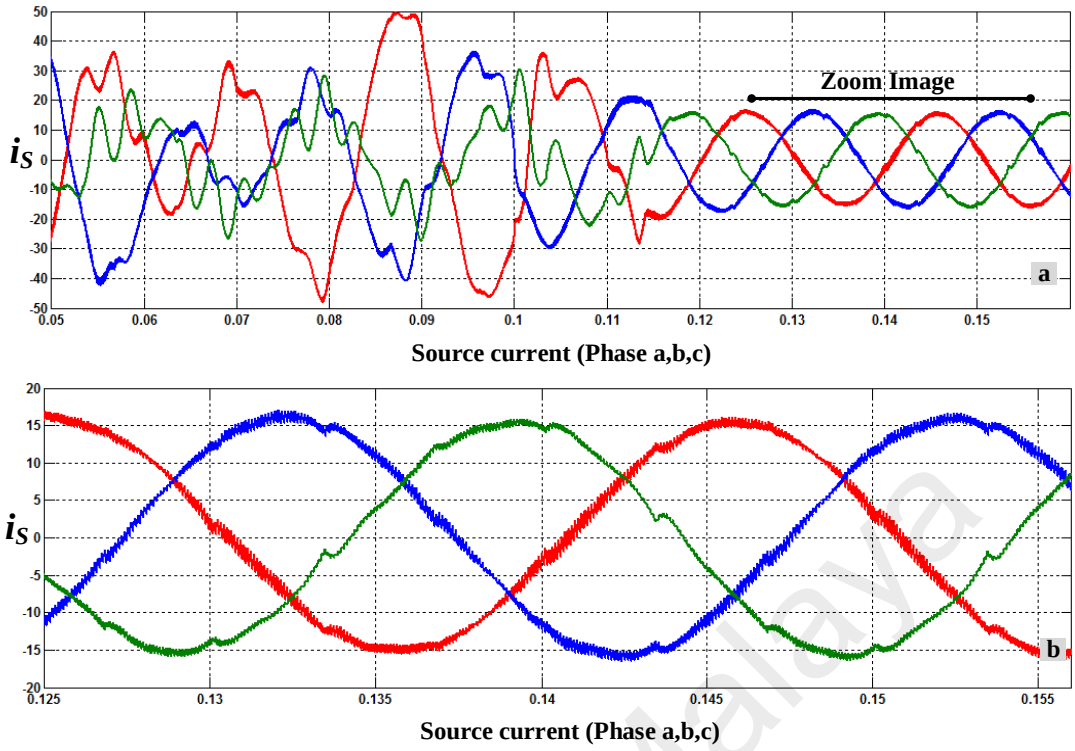
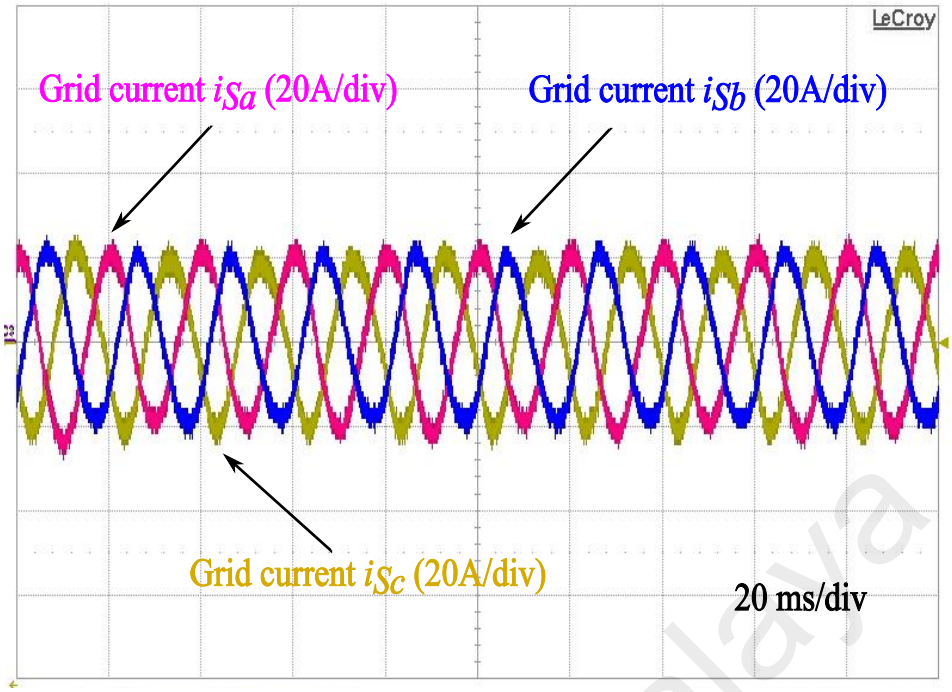
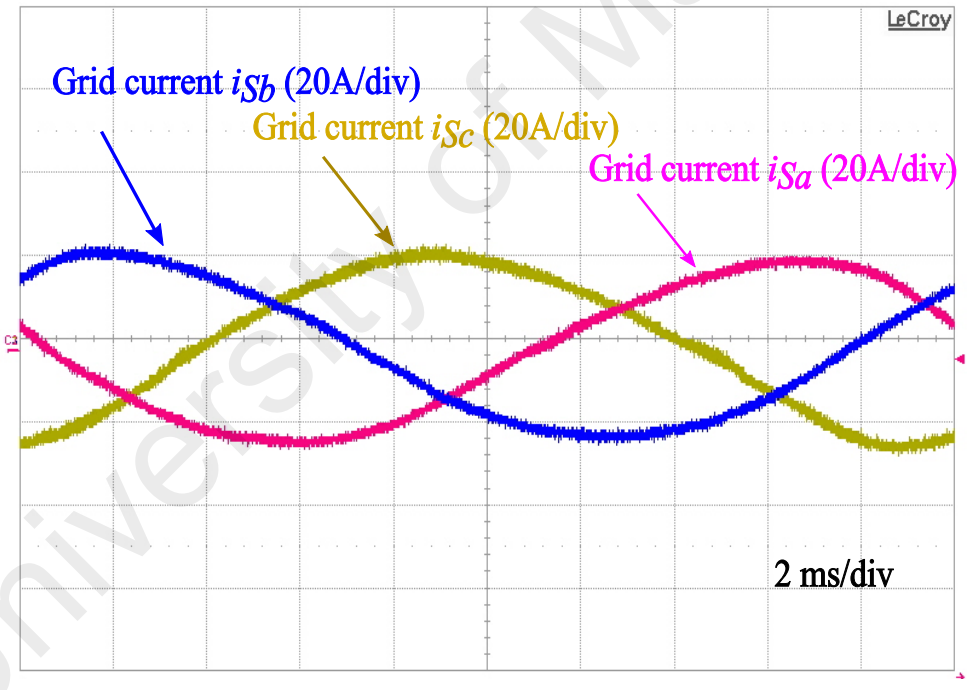


Figure 4.15: a) On-state and Off-state APF operations. B) Zoom image of utility line current (i_{Sabc}) at 5th and 7th order harmonics.

Roughly the same experimental result is obtained using the same equivalent system parameters and control scheme. After compensation, the three-phase utility currents are nearly sinusoidal with the reduced switch count devices in Figure 4.16 (a) and Figure 4.16 (b). The three-phase utility current validates that the proposed two-leg APF effectively compensates the predominant current harmonics.



(a)



(b)

Figure 4.16: Steady state operation of the proposed SAPF. a) Utility current (i_{Sabc}) b) zoom image of utility current (i_{Sabc}).

Figure 4.17 illustrate the comparison of the compensating and un-compensating source current before and after filtering with two sets of PF. However, there exists a large amount of 5th and 7th harmonic in the uncompensated source current before the APF filtering. The

system offers the best response after filtering at fixed load and step load change. The LC filter tuned at 5th and 7th harmonic frequencies reduces the flow of non-negligible amount of harmonics in the system, with THD*i* values from 30.1% (without APF) to 3.61% (with APF). The comparison of the source THD values between the Figure 4.14 and Figure 4.17, show a significant improvement in the THD with the dual sets of LC PF and two leg APF for non-linear loads. Here, after compensation, the THD*i* of the source current is successfully reduced, which validates that the proposed APF system, effectively compensates the current and voltage THD.

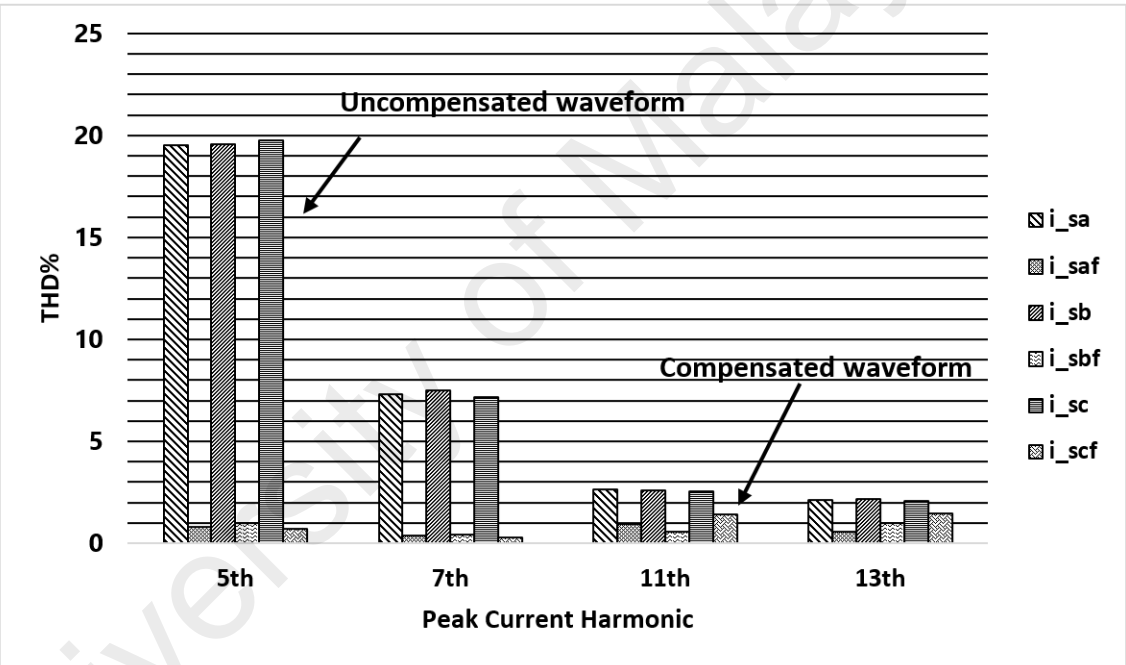


Figure 4.17: Spectral analysis of the source current before and after filtering.

4.6.2 Dynamic/Transient state filtering performance

In order to verify the transient filtering performance of the proposed model, the standard tests has been carried out. Figure 4.18, shows the dynamic performance of the proposed APF during the step-on load change for R-L and inductive (VAR) non-linear loads. The step change starts at time t=0.1 ms and other at time t=0.25 ms to response the settling time for compensating the step load change effect in less than one cycle. It is noticed that the proposed APF compensate the unbalance impedance ratio effect in each

phase and operate as conventional APF. It provides the necessary negative sequence compensation at the step-change with less unbalanced source current waveform for the only R-L load.

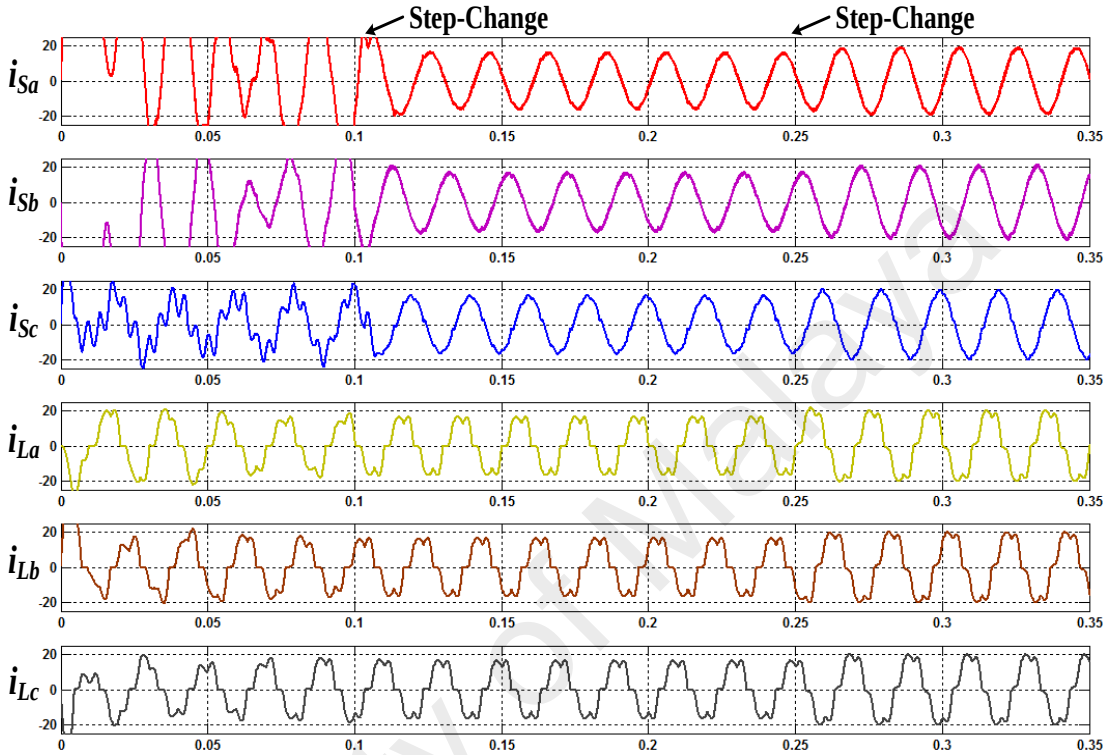


Figure 4.18: Dynamic performance with the R-L load step-change waveforms of the proposed SAPF. Upper three utility current after compensation, and lower three utility current before compensation.

The proposed APF is tested under the sudden variations in non-linear load to verify the dynamic behavior in terms of utility voltage v_{Sa}, load current i_{La}, and source current i_{Sa}. The source current waveform (i_S) is under distortion effect for half a cycle during the step change operation but reaches a steady state within one cycle. Figure 4.19 and Figure 4.20 illustrates the results under the step-on and step-off load conditions. During the step change operation, the load is sharply decreased from 0% to 100% and vice versa. The response and recovery time are fast between the changeovers, thereby demonstrating the excellent compensation capability of the proposed APF scheme. The

source current remains sinusoidal without aggregating the THD. The source current THD of the APF system decreases by 4.1%, which is within the IEEE-519 standard of 5.0%.

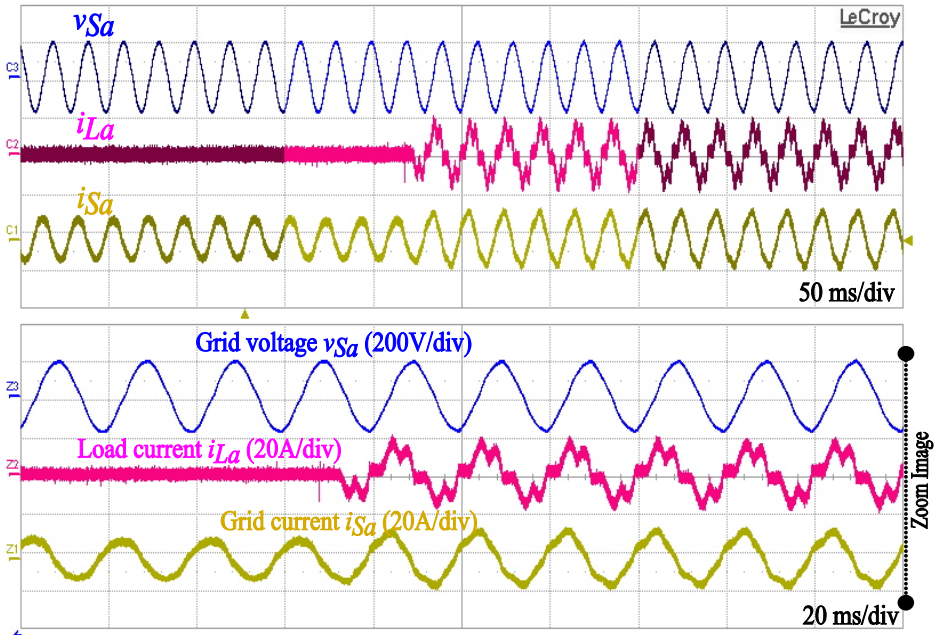


Figure 4.19: Experimental results under transient condition at step load. a) Utility voltage b) load current c) utility current (0% load to 100% load).

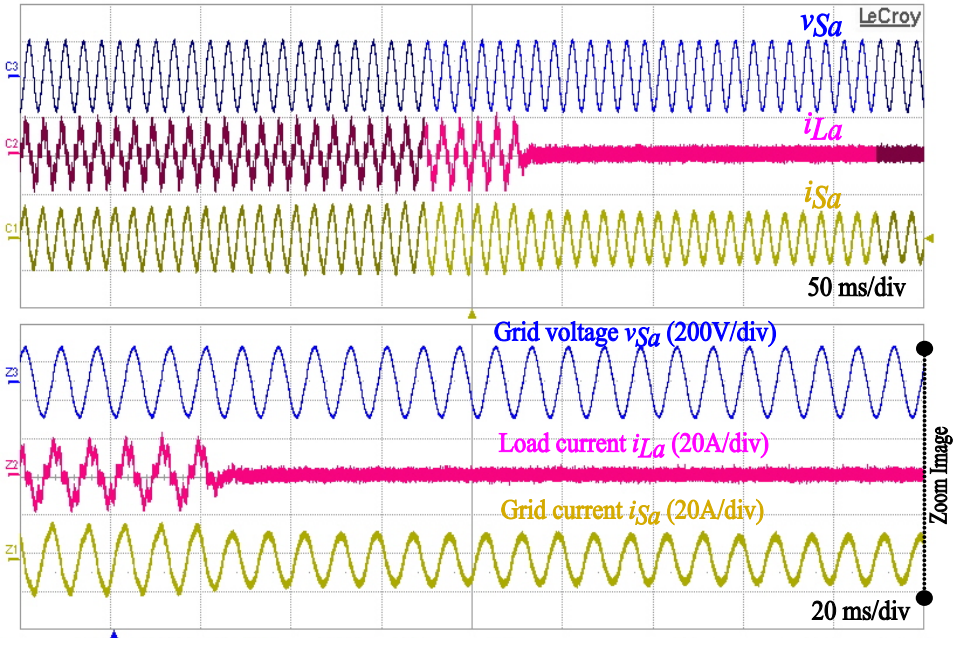


Figure 4.20: Experimental results under transient condition. a) Utility voltage b) load current c) utility current at step load (100% load to 0% load).

With increasing and decreasing load, the proposed APF compensates the voltage drop caused by the energy storage requirement across the DC-link capacitor. The DC controller compensates the voltage effect by increasing and decreasing the supply current asset according to the reference value. The simulation and experimental results verify that the proposed APF scheme provides reactive and harmonic load current compensations under dynamic and steady states.

4.7 Active and reactive power compensation results

In order to proof the enhanced reactive power capability of the proposed APF system for injecting the active power (P), and reactive power (Q) flow into the power distribution grid is precisely control through shunt connected coupling inductors. For enhanced reactive power compensation, the proposed APF work similar on the principle of STATCOM devices. The proposed model enhances better harmonic filtering and reactive power compensation in equivalent to conventional full-bridge topologies. The series AC-coupling inductors overcome the problem of fixed reactive power compensation, as the LC passive filter offers fixed reactive power compensation. However, under the condition of lagging power factor angle than the condition of leading power factor angle, the voltage saturation and current waveform distortion is avoided by keeping the DC-link capacitor voltage v_{dc} constant and at high rated value as shown in Figure 4.21.

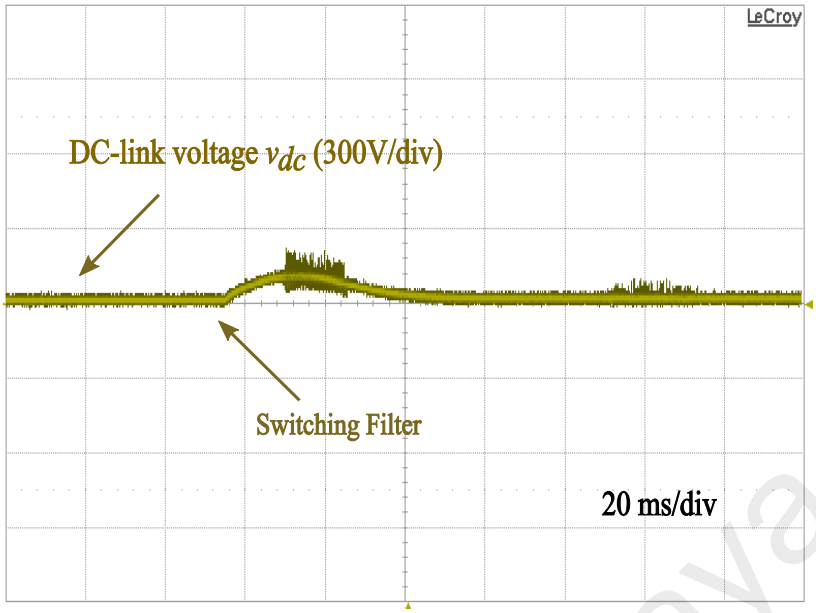


Figure 4.21: Output DC-bus voltage for active (P) and reactive (Q) power flow.

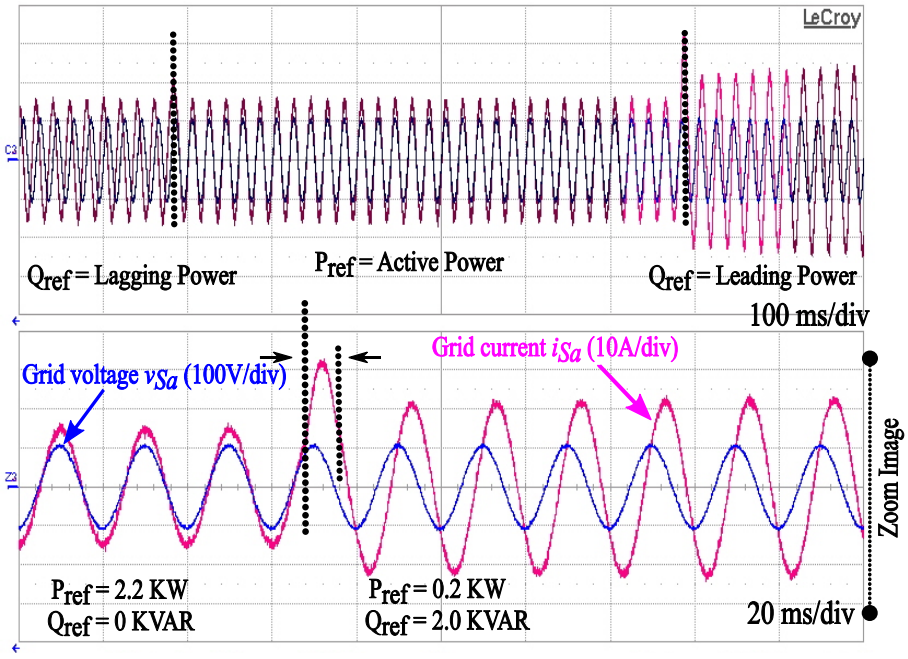
Due to the active filtering operation and duty cycle saturation, the output current waveform behaves to be distorted, therefore, under the lagging reactive power flow, the DC-link voltage need to be higher than the designed rating for the active power flow. In order to avoid the saturation and waveform distortion, the DC-link voltage setting from 300V to 320V to maintain the continuous control of the active and reactive power flow. To analyses the enhanced reactive power compensation operation, three different cases are experimentally verified in Figure 4.22 (a, b, c) as detail in Table 4.7.

Table 4.7: Three different scenario for reactive power compensation.

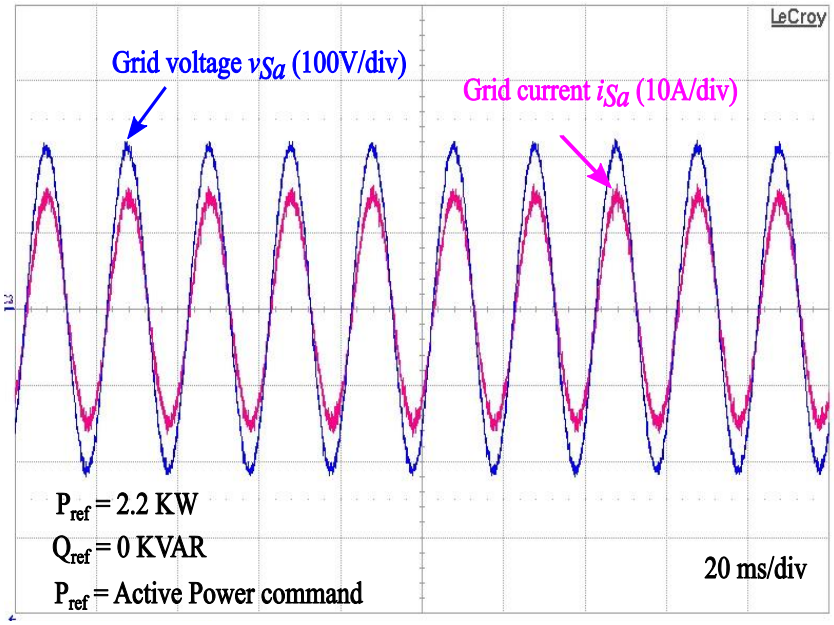
Active Power (P_{ref}) KW	Reactive Power (Q_{ref}) kVAR	Apparent Power (S_{ref}) kVA	Power Factor (PF)
0.2	2.0	2.2	lag
2.2	0	2.2	1.0
0.2	2.0	2.2	lead

The first scenario is pure 2.2 kVAR lagging reactive power condition, the second scenario is pure 2.2 KW pure active power condition, and third scenario is pure 2.2 kVAR

leading reactive power flow condition. During the change of power sceneries, the phase angle of grid current (i_{Sa}) changes from 90° to –90° compare to grid voltage (v_{Sa}).



(a)



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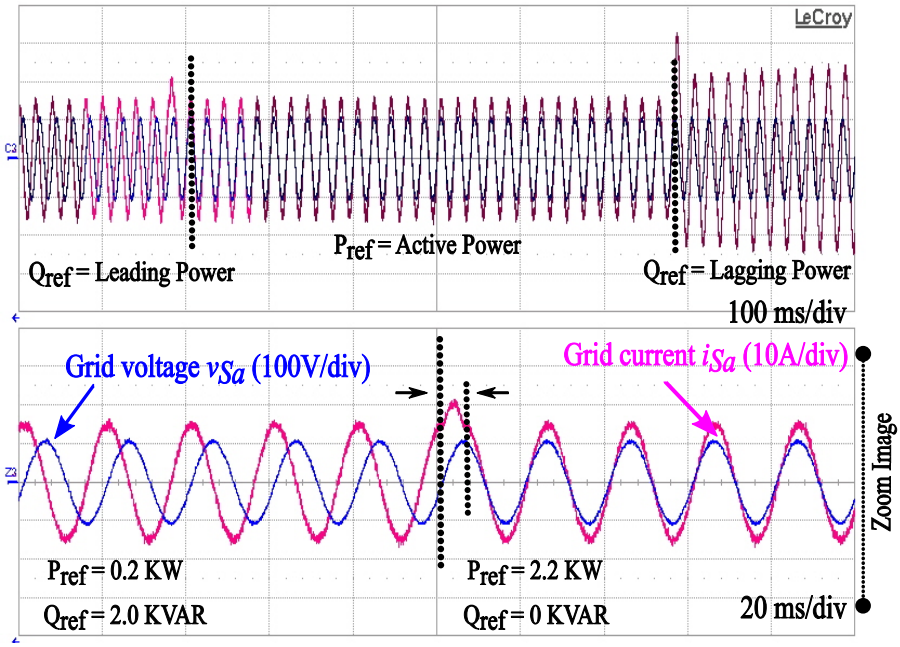


(c)

Figure 4.22: Experimental results for 2.2 kVAR leading reactive power command. (b) 2.2 KW active power command. (c) 2.2 kVAR lagging reactive power command.

In second case, the proposed APF draws 2.2 kW for a charging the DC-link capacitor without performing the reactive power support function. At this level, both the grid voltage v_{Sa} and grid current i_{Sa} are in phase (unity power factor).

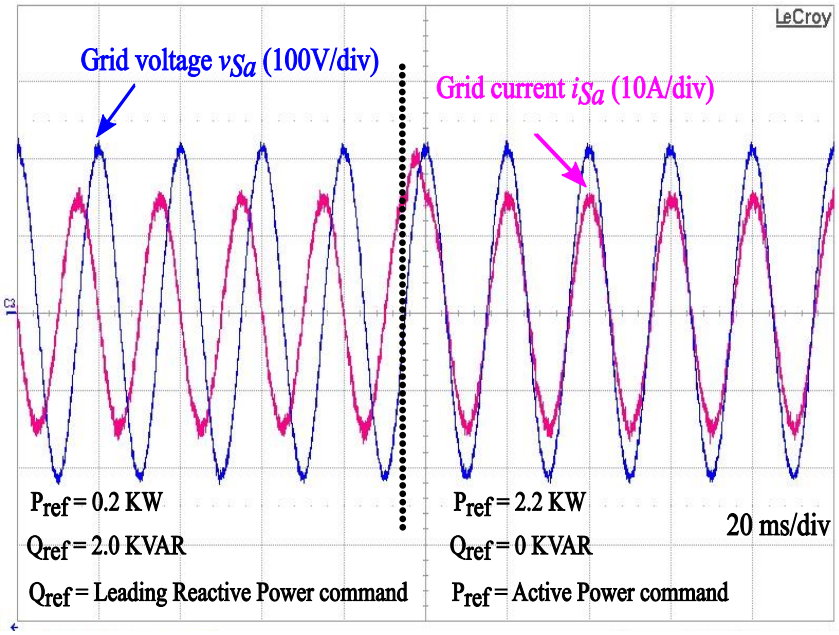


Figure 4.23: Transition to capacitive leading reactive power flow.

To demonstrate the capacitive reactive power operation of the proposed system, the grid current i_{Sa} leads the grid voltage v_{Sa} for about 90° as shown in Figure 4.23. The reactive power 2.0 kVAR injection into the grid changes the 2.2 KW power operation to leading power factor of a unity (1.0-pf) operation. For inductive lagging reactive power flow of the system, the grid current i_{Sa} lags the grid voltage V_{Sa} for about –90°, in less than two grid cycles as shown in Figure 4.24. It can be concluded from both the Figure 4.23 and Figure 4.24, that the proposed APF can effectively control the enhanced range of active and reactive power flow into the power grid system.

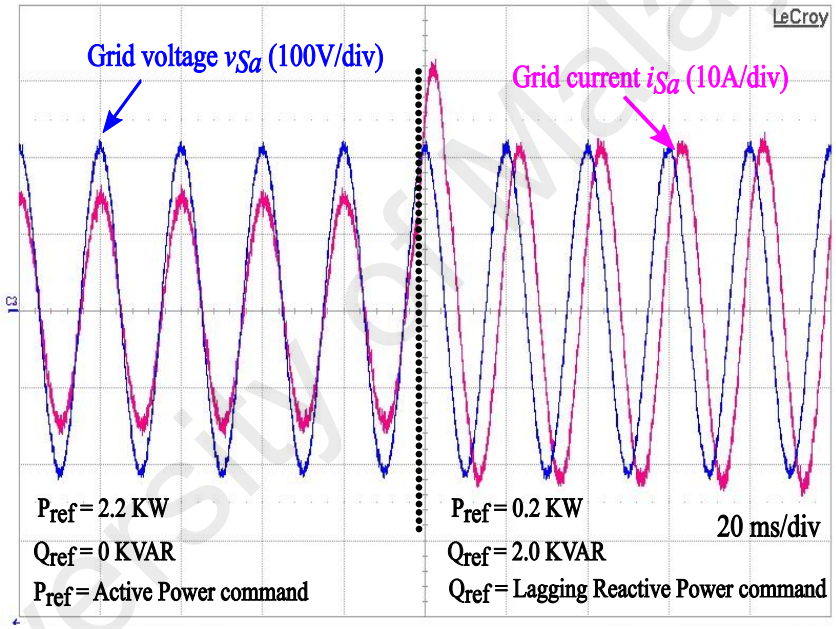


Figure 4.24: Transition to inductive lagging reactive power flow.

The experimental results show that the proposed transformerless grid-connected VSI can provide full range active and reactive power support command. The sufficient DC-link voltage level and laboratory test rig results effectively compensate the reactive power demand, current unbalance and current harmonics in addition to active power injection as depicted in Figure 4.25.

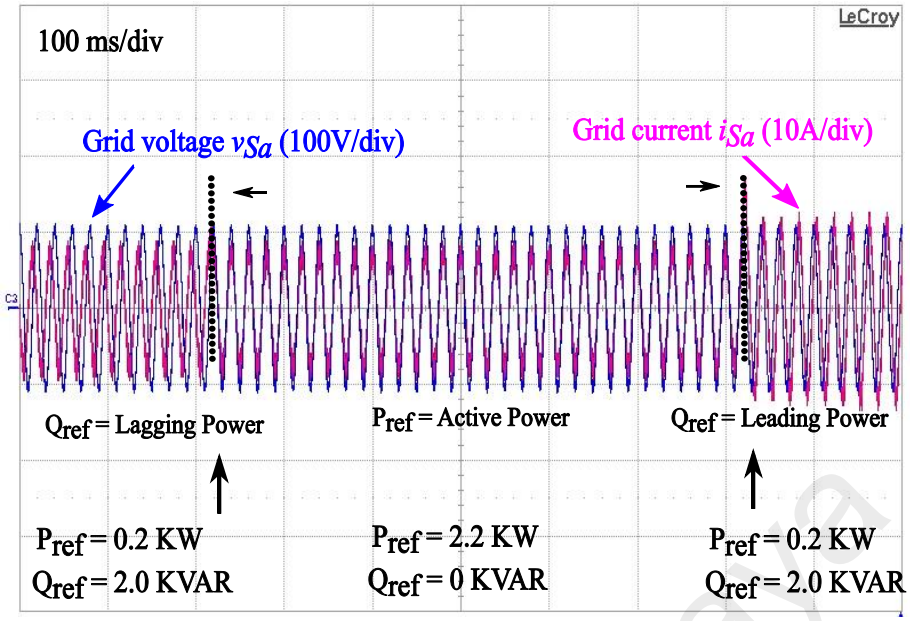


Figure 4.25: Overall transition to inductive lagging reactive power flow, active power flow, and capacitive leading reactive power flow.

4.8 Performance comparison of the proposed APF inverter

Table 4.8 and Table 4.9 compares the proposed designed inverter and capacitors with other existing topologies in terms of cost, weight, volume, number of switches, efficiency, and THD. The novel circuit presents the best reduced weight and volume compact structure compared with other topologies. The system efficiency is estimated on the number of active devices and passive components counts in the different APF topologies, under a comparative study between the APF, HAPF and proposed SAPF.

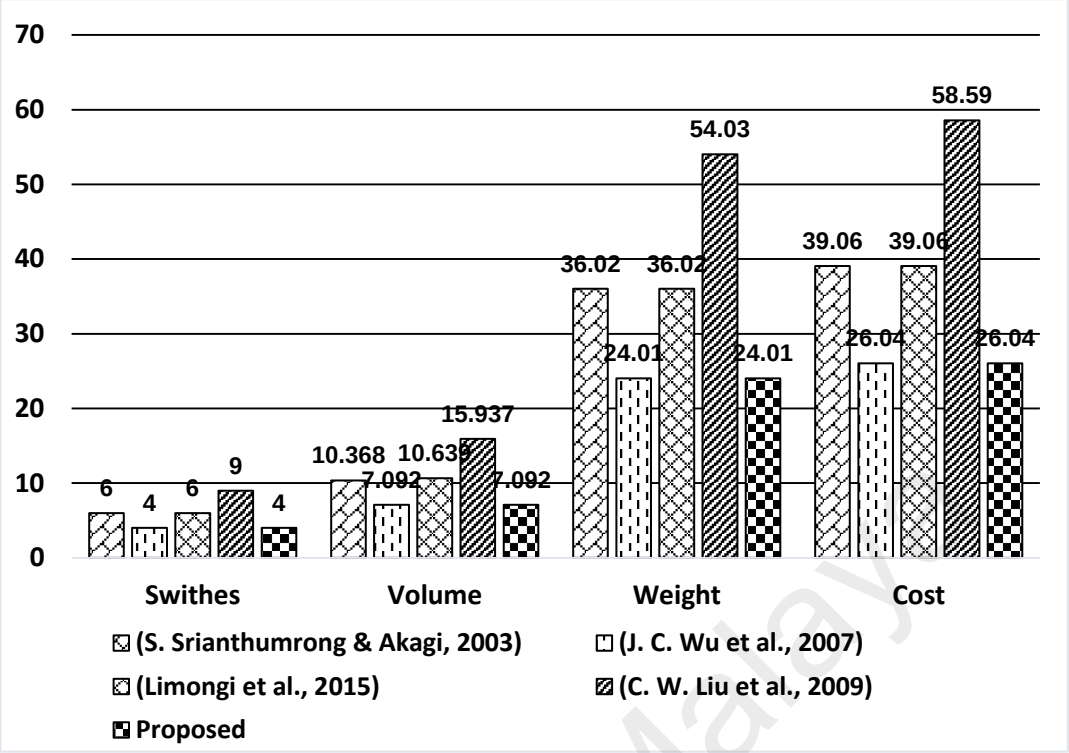
The overall reduction in weight, volume, and cost is due to the decreased amount of VSI switches and series coupling AC capacitors as illustrated in Figure 4.26 (a) (S. Srianthumrong & Akagi, 2003), (J. C. Wu et al., 2007), (Limongi et al., 2015), (C. W. Liu et al., 2009) and Figure 4.26 (b) (S. Srianthumrong & Akagi, 2003), (J. C. Wu et al., 2007).

Table 4.8: Comparison for inverter cost, weight, volume and others parameter.

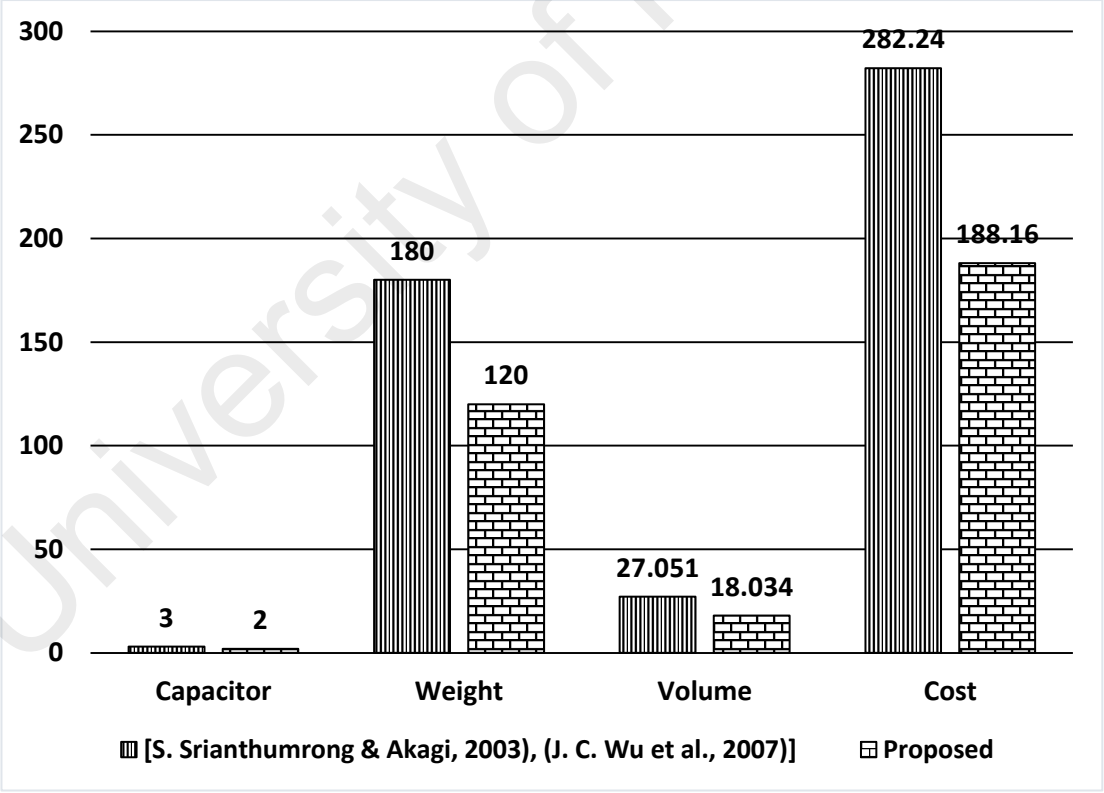
	Values				Reduction		Actual Value	
Reference	**No. of switches**	**Efficiency (%)**	**Volume (cm^3)**	**Weight (g)**	**Volume (cm^3)**	**Weight (g)**	**Cost ($)**	**THD (%)**
(S. Srianthumrong & Akagi, 2003)	6	Low	10.638	36.02	-3.546	-18	39.06	<5
(J. C. Wu et al., 2007)	4	High	7.092	24.01	0	-18	26.04	<5
(Limongi et al., 2015)	6	Medium	10.639	36.02	-3.546	-6	39.06	<5
(C. W. Liu et al., 2009)	9	low	15.957	54.03	-5.319	-30.01	58.6	<5
Proposed	**4**	**High**	**7.092**	**24.01**	**-**	**-**	**26.5**	**<5**
Type	Single Module IKW75N60T, IGBT Transistor, 600V/80A, Dimensions (21.10 x 16.13 x 5.21mm), weight (6.0042 g), volume = 1773.18703mm, 1.773(cm^3), Cost (6.51)$/each							

Table 4.9: Comparison for weight, volume and cost for capacitor.

	Values			Reduction		Actual Value
Reference	**No. of Capacitor**	**Volume (cm^3)**	**Weight (g)**	**Volume (cm^3)**	**Weight (g)**	**Cost ($)**
(S. Srianthumrong & Akagi, 2003)	3	27.051	180	-18.034	-120	282.24
(J. C. Wu et al., 2007)	3	27.051	180	-18.034	-120	282.24
Proposed	**2**	**18.034**	**120**	**9.017**	**60**	**188.16**
Type	Film Capacitor, PP (Polypropylene), 330VAC/50A, 200 µF, Dimensions (63.5 x 142mm), diameter (142mm), weight (60 g), volume = 9017mm, 9.017(cm^3), Cost (94.08)$/each					



(a)



(b)

Figure 4.26: Comparison for the switches, weight, volume and cost. (a) Inverter switches count, cost, volume and weight. (b) Capacitor count, cost, volume and weight.

4.9 Summary

In summary, an experimental 2.2 kVA power capacity APF system is installed in shunt position with the three phase utility grid and uncontrolled diode rectifiers load. This chapter explains the hardware implementation of the proposed new transformerless two-leg APF system is based on a *dSPACE* controller to carry out the experimental work for the three-phase grid connected application systems. The overall APF system performance has been analyzed, particularly during the harmonic filtering and reactive power enhancement. The feasibility of the power distribution system is improved, by eliminating the transformer and reduced power components. Comparison of the proposed system with the other previous APF topology shows considerable improvement in terms of performance, reliability, system losses, compactness and less cost of the proposed system. Experimental results of each harmonic and reactive power compensation of the APF system have been explained. The experimental and simulation results verify the feasibility of the proposed topology and its excellent performance in transient and steady states operations.

CHAPTER 5: CONCLUSIONS AND FUTURE WORK

In this chapter, conclusion of the research work is presented. Also, the future work of this study and suggestion for extension of this project has been highlighted.

5.1 Conclusions

A novel three-phase transformerless APF system has been proposed in this study. The proposed configuration uses a two-leg bridge structure and decreases the number of switching power devices in the power converter, thereby minimized the system size and cost. The feasibility of the power distribution system is improved by eliminating the transformer and power switching component to provide accurate performance, reduced volumetric size and low cost compared with other existing APF topologies. Also, it helps in reducing the switching losses of the system. A transformerless passive filters (PFs) and coupling inductors has been used at the front end of the APF inverter that increases the efficiency of the system and provides efficient PFC regulation with the power grid system. The dedicated coupling inductors based reduced power converter compensates the enhanced reactive power and APF filtering operations into three-phase grid network. However, it also controlled the constant DC-link voltage with improved power factor of unity without affecting the filtering process. The series LC PF tuned at the 5th and 7th order harmonic frequencies improves the active filtering capability and the reactive power compensation performance. The series AC coupling inductors overcome the fixed reactive power compensation caused by the defined value of the LC filter leg.

The overall APF system has been designed, implemented and the performance has been analyzed. The control algorithm ensures the regulated sinusoidal voltage, phase amplitude, and low THD in the power distribution system along with DC-link voltage control. All the design parameters have been caluclated and analyzed. The adopted modulation strategy in this study is the sinusoidal PWM (SPWM) for a proper switching

scheme for nonlinear load. The voltage control scheme is employed (PI controller) to regulate the DC-link voltage level and maintain the voltage level higher for proper reactive power compensation command. The controller operates constant and shows fast transient response during the step change nonlinear load condition. The experimental and simulation results verify the feasibility of the proposed topology as compare to conventional full-bridge topologies. Therefore, the grid current harmonics THD*i* spectrum of the proposed APF system is less than 5%, according to IEEE-519 standard. The experimental and simulation results show good dynamic and steady-state performance of the proposed topology in terms of current harmonic mitigation capability and reactive power compensation with less cost, light weight and compact structure for grid-connected power applications.

5.2 Future Work

Evaluating the observations and findings from this thesis, the future research work can be focused on the following points.

1. The novel idea of three-phase transformerless APF system can be analyzed for high power applications with low power rating of the inverter.
2. The voltage stress across the AC capacitor in phase c has been doubled than the conventional six-switched and three-leg configuration. The trade-off in proposed design is to reduce the number of passive components, therefore the doubled voltage stress can be further reduced to much lower value.
3. The control scheme adopted in this dissertation, is the conventional three-phase converter control. However, in some cases the circuit configuration is not symmetrical and unbalanced loading conditions including negative sequence and zero sequence (neutral loop 3P4W system). These harmonics effecting the control scheme, which should be consider in this dissertation.

4. The HAPF can only inject a fixed amount of reactive power due to the fixed values of the passive filters. In the reality, the load-side reactive power consumption varies from time to time, as a result, the HAPF cannot perform satisfactory dynamic reactive power compensation. In the proposed model, the reactive power compensation range using the two coupling Inductors. The two leg configuration have some limitations than the full range three legs conventional inverter scheme.
5. The proposed APF system is design and tested for the grid-connected system. In future work applications, the excessive penetration of the renewable devices in the power transmission network, creates the various power quality challenges. Therefore, the new APF model is need to be tested with the energy-fed grid interactive topologies, such as PV solar energy and Wind energy power turbine systems for harmonic mitigation and reactive power support.

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LIST OF PUBLICATIONS, PAPERS AND PATENT

1. **Tareen, W. U**, S. Mekhilef, & M. Nakaoka, "A transformerless reduced switch counts three-phase APF-assisted smart EV charger," in 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), 2017, pp. 3307-3312.

2. **Tareen, W. U**., Mekhilef, S., Seyedmahmoudian, M., & Horan, B. (2017). Active power filter (APF) for mitigation of power quality issues in grid integration of wind and photovoltaic energy conversion system. Renewable and Sustainable Energy Reviews, 70, 635-655. **(Impact factor 7.89).**

3. **Tareen, W. U**., & S. Mekhilef (2016). Transformer-less 3P3W SAPF (three-phase three-wire shunt active power filter) with line-interactive UPS (uninterruptible power supply) and battery energy storage stage. Energy, 109, 525-536. **(Impact factor 5.1).**

4. **Tareen, W. U**., & S. Mekhilef, "Three-phase Transformerless Shunt Active Power Filter with Reduced Switch Count for Harmonic Compensation in Grid-Connected Applications," *IEEE Transactions on Power Electronics*. **(In Press 2017) (Impact factor 5.19).**

5. **Tareen, W. U**., Mekhilef. Mitigation of the power quality issues due to high penetration of renewable energy sources in electric grid system using three-phase APF/STATCOM technologies: A review. Renewable and Sustainable Energy Reviews. **(Major revision 2017) (Impact factor 7.89).**

6. **File a Patent:** Tareen, W. U., & S. Mekhilef, "Transformerless Shunt Power Filter Based On Four-Switch Two-Leg Inverter For Harmonic Compensation Performance". **(2017).**