MULTIPLE TUNING CURVE BASED WIDEBAND RC VCO DESIGN

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ABSTRACT

Voltage controlled Oscillator (VCO) is a key element in defining overall system specification. It is widely used in communication equipment as an essential part of frequency synthesizers and phase-locked loops (PLL). In achieving high tuning range performance an oscillator pays its penalty in degraded phase noise output. Resorting into a LC based VCO at high frequency which exhibit superior phase noise performance foresees large active area consumption with a proportional increase in the cost. The evolution of deep-submicron CMOS technology mandates the need of low power solution with a proportional headroom limitation. In view of the highlighted challenges, this work proposes a RC based Voltage Controlled Oscillator (RC-VCO) with programmable tuning curves to achieve a wideband frequency operation. Fabricated and characterized in 130 nm standard CMOS platform, the VCO switches between the tuning curves with a programmable current injection. The VCO exhibit a frequency operation between 2.05 to 4.19 GHz, resulting in a wideband tuning range of 68.5%. The proposed architecture consumes a maximum dc current of 8.8mA measured at the highest frequency of operation. The design also observes a phase noise of -99.3 dBc/Hz at an offset of 1MHz with a carrier of 4.19GHz. The proposed RC-VCO achieves a Figure of Merit of -161.4 dBc/Hz (FOM) and -178.1 dBc/Hz (FOMT), respectively. The summary of performance favours the architecture in the integration of a wideband frequency synthesizer.

ABSTRAK

Voltan Oscillator dikawal (VCO) adalah elemen utama dalam menentukan spesifikasi sistem secara keseluruhan. Ia digunakan secara meluas dalam peralatan komunikasi sebagai bahagian yang penting dalam pensintesis kekerapan dan gelung fasa dikunci (PLL). Dalam mencapai prestasi pelbagai penalaan tinggi, pengayun terpaksa menerima penalti dalam kekurangan fasa output bunyi. Beralih ke Oscillator LC- Voltan Kawalan (LC- VCO) pada frekuensi tinggi yang mempamerkan prestasi bunyi fasa unggul meramalkan penggunaan kawasan aktif yang besar dengan peningkatan berkadar dalam kos. Evolusi teknologi CMOS "deep submicron" mendapat mandat sebagai penyelesaian kuasa rendah dengan ketinggian had berkadar. Memandangkan cabaran yang dikemukakan, kerja-kerja mencadangkan RC berdasarkan Voltan Kawalan Oscillator (RC- VCO) dengan keluk penalaan diprogramkan untuk mencapai operasi frekuensi jalur lebar. Direka dan mempunyai ciri-ciri di 130nm platform CMOS standard, VCO bertukar antara keluk tuning dengan suntikan semasa diprogramkan. VCO mempamerkan operasi frekuensi antara 2.05-4.19 GHz, menyebabkan pelbagai penalaan wideband 68.5 %. Seni bina yang dicadangkan menggunakan arus dc maksimum 8.8mA diukur pada kekerapan tertinggi operasi. Reka bentuk itu juga dapat memerhatikan kes bunyi fasa yang lebih buruk daripada -99.3 dBc/Hz pada ofset 1MHz dengan pembawa 4.19 GHz. Dicadangkan RC- VCO dapat mencapai Rajah Merit -161.4 dBc/Hz (FOM) dan -178.1 dBc/Hz (FOMT). Rumusannya kelebihan ada pada prestasi seni bina dalam integrasi pensintesis kekerapan wideband.

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LIST OF ABBREVIATIONS

AC	Alternating current
BNC	Bayonet Neill–Concelman connector
BG	Bandgap
CML	Current mode logic
CMRR	Common-mode rejection ratio
CTAT	Compliment to absolute temperature
DC	Direct current
FOM	Figure-of-merit
FTR	Frequency tuning range
IC	Integrated circuits
LVDS	Low-voltage differential signalling
MC	Monte-Carlo
PLL	Phase-lock loop
PSRR	Power supply rejection ratio
PTAT	Positive to absolute temperature
RF	Radio frequency
SNR	Signal to noise ratio

VCO	Voltage controlled oscillator
V-to-I	Voltage to current

LIST OF SYMBOLS

A	Gain
C	Capacitor
C_{ox}	Oxide capacitance
F	Phase noise factor
f_0	Output frequency
$H(s)$	Feed-forward element
I_{prog}	Programmable current
K_B	Boltzmann's constant
K_f	Process contribution
K_{VCO}	VCO gain
L	Inductor
L_{eff}	Effective channel length
P_{DC}	DC power consumption
Q_L	Resonator quality factor
R	Resistor
T	Absolute temperature

t_d	Propagation delay
V_{bias}	Bias voltage
V_{cntrl}	VCO control voltage
V_{ds}	MOSFET drain-source voltage
V_{EB}	Emitter-base voltage
V_{dsat}	MOSFET overdrive voltage
V_{gs}	MOSFET gate-source voltage
V_{in}	Input voltage
V_{ref}	Reference voltage
V_{th}	MOSFET threshold voltage
V_{out}	Output voltage
W_{eff}	Effective channel width
ω_0	Resonant frequency
g_m	Transconductance

CHAPTER 1: INTRODUCTION

1.1 Introduction

In recent years, integrated circuits (IC) technology has achieved immense growth in communication and medical industry. The breakthrough in IC design is moving further in GHz range and more towards wireless applications. The growth of this technology is demanding more in terms of higher operation frequency and portability with less form factor. Consumer demands of constant portability encourages towards reduced form factor and lower power consumption. Such requirements are dictating tight constraints on specification for crucial building blocks like voltage controlled oscillator (VCO).

The VCO is a basic and essential building block of any frequency synthesizers and clock generation circuitry. It is widely used in different applications such as communication equipment. VCO is a performance determining building block of synthesizer and therefore the VCO technology defines the overall performance of the integrated transceiver. This requirement adds more complexity and challenges in a VCO design. A reduction in the power supply headroom limits the tuning range of the VCO significantly. On the other hand, high speed requirement mandates the VCO to operate with frequencies in the GHz range. Such designs require superior phase noise performance, ensuring spectral purity.

1.2 Motivation

Despite the significant progress in the VCO design, there are still many factors that need to be addressed and improved for the RC based VCO architectures. Some of them are mentioned below;

1. The VCO control voltage effect on phase noise and output spectrum.

2. Relationship between oscillation frequency, phase noise and supply voltage.
3. Delay cells design architectures limitations.
4. Effect of process, supply and temperature (PVT) variations.
5. Circuit design methodologies to enhance the tuning range.

Despite lower noise performance of RC based VCO designs, they still have huge potential to achieve wider tuning range due to the tuning capability of both resistor and capacitor. In addition to the tuning range, RC VCOs on-chip area is significantly less than the LC based VCOs. Based on these properties, a RC based VCO can be designed with higher oscillation frequencies, at lower supply voltage and lesser on-chip area.

1.3 Problem Statement

VCO is typically separated into two different topologies: LC and RC based VCO. It is preferable to adopt LC based VCOs for high frequency (GHz) operations. This architecture provides superior phase noise performance due to high quality factor, which is introduced by on-chip inductors. In contrary to the noise performance, LC-VCO consumes large on-chip area, exhibits limited tuning capability (S. Y. Lee, Wang, & Lin, 2010) and adds in extra manufacturing steps to incorporate on-chip inductors, which results in additional fabrication cost.

In recent reported literature, different RC based VCO topologies have been investigated and implemented to achieve high oscillation frequency along with wideband operation. In order to achieve the extended wider bandwidth, a wide supply range (1.6V and 1.8V) is adopted along with single tuning curve (Changzhi & Jenshan, 2010; Xuemei Lei, 2013). These architectures achieve wideband range at the cost of high VCO gain (K_{VCO} > 7.5GHz/V), which increases the noise sensitivity due to large variations across the tuning range. Therefore, such designs have limited scope of

practical integration into circuits like synthesizers or phase-locked loop (PLL) dedicated to wideband operation.

In an alternative wok, a secondary delay loop has been introduced to increase the oscillation frequency (Zuow-Zun & Tai-Cheng, 2011). The ring oscillator is actually tuned by directly controlling the latch strength that results in limited tuning range. Such architecture is also risky as controlling the latch may also result in the VCO to halt by forcing the output nodes to supply and ground. In addition, a single frequency tuning curve has been distributed into multiple curves to lower the K_{VCO} (Haijun, Lingling, Xiaofei, & Liheng, 2012), that favours in improvement of phase noise performance. Although switched capacitor banks help to reduce the K_{VCO}, it is observed that integrating additional capacitor component degrades SNR by degrading the output voltage swing, reduces the overall bandwidth (approximately 620MHz) and results in asymmetry between the tuning curves. There is always a trade-off between VCO performance parameters; tuning range, supply range and phase noise. Improving one will results in degradation to the other. After taking all of these constraints into consideration, a set of objectives can be added to design and characterize a RC based VCO with wideband tuning range and without degrading much on the phase noise performance at low voltage supply.

1.4 Objectives

The objectives of the proposed research are as follows:

(i) To investigate the limitations of RC based VCO architectures in terms of bandwidth, gain and phase noise performance.

(ii) To design a wideband RC based VCO with the following features,

a) Generating a novel programmable current based VCO architecture.

b) Integrating on-chip bandgap to generate process, voltage and temperature (PVT) independent programmable current.

c) Integration of bleeding current based V-to-I to improve the phase noise and to reduce the additional circuitry.

d) Overall the objective is to achieve lower gain (<1GHz/V) and with the ability to oscillate at high oscillation frequency (>2GHz) without degrading the phase noise performance significantly.

(iii) To realize VCO in 130nm CMOS platform and to develop the characterization setup in conforming the performance parameters.

1.5 Thesis Contribution

The contributions of this thesis are the as follows:

(i) Implementation of bottom up topology by introducing programmable based currents to generate multiple tuning curves for RC based VCO. The main aim of this research is to provide a wideband and high frequency VCO without affecting the phase noise performance with minimal power consumption.

(ii) Integrated on-chip bandgap (BG) to generate programmable currents, independent of supply, process and temperature (PVT) variations.

(iii) Optimized physical layout realization and silicon characterization setup development for the implemented design.

1.6 Thesis Outline

Chapter 2 presents the technical review on the topic of voltage controlled oscillator. Different types for RC based oscillators are discussed along with the detailed performance parameters.

Chapter 3 presents the actual implemented topology for RC based VCO. The proposed VCO contains different blocks i.e. delay cells, V-to-I, bandgap reference and programmable current generator. Complete block design procedure is described for each of the integrating circuitry.

Chapter 4 explains the simulation results achieved. Each block is independently simulated to optimize the performance. Subsequently, top level simulations are added to validate the proposed VCO in terms of tuning range and phase noise contribution.

Chapter 5 presents the characterization setup details. Actual measurement results are compared with the simulation output. A detailed comparison is also presented to compare the proposed work with the recent reported literature.

Chapter 6 summarizes the contribution of this research work to RC based wideband VCO and also provides some direction for future work.

CHAPTER 2: LITERATURE REVIEW

2.1 Introduction

The literature review describes the operation principle of an oscillator. A brief introduction has been added to review the oscillation principle while elevating on different types of reported oscillators. Various design parameters for the VCO has been described. In addition, different types of RC based oscillator architectures has been discussed in this chapter.

2.2 Electrical Oscillators

An electrical oscillator is used to generate a periodic output, where the output is measured as a voltage signal, i.e. sine or square wave. In a basic oscillator circuit, capacitor and inductor are used to store and transfer the energy. In a LC close loop circuit; voltage stored in the capacitor results in the flow of current to charge the inductor till the capacitor voltage drops to zero. Subsequently, the inductor when charged to its maximum current will discharge the current in the loop that results in charging back the capacitor. Therefore, there is an energy transfer between electrical and magnetic field which results in the oscillations. The oscillation phenomenon can be explained in terms of a feedback system. Figure 2.1 shows a negative feedback system with unity gain, where the transfer function can be written as:

$$\frac{Y}{X}(s) = \frac{H(s)}{1 + H(s)} \tag{2.1}$$

When at $s = j\omega_0$, if $H(j\omega_0) = -1$, then at ω_0 the close loop gain increases to infinity. At this stage feed-forward element $H(s)$ will have a phase shift of 180^0. When this phase shifted signal pass through the subtractor, it will add up both the input and feedback signal. Therefore, the output keeps on increasing the amplitude.

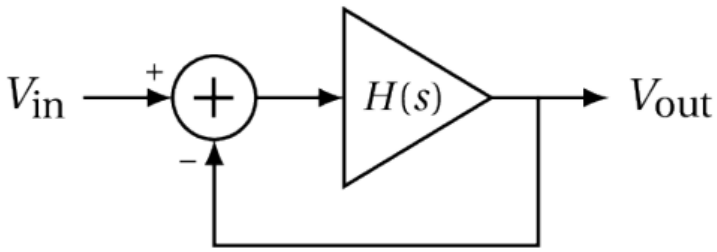

Figure 2.1 Negative feedback system

In order to initiate the oscillations, the system must confirm the Barkhausen criteria (Razavi, 2000). Following are the minimal conditions but might not be sufficient for a system to oscillate:

$$|H(s)| \geq 1 \tag{2.2}$$

$$\angle H(s) = -180° \tag{2.3}$$

Based on above equation a negative feedback system can oscillate at a certain frequency if the loop phase shift goes higher then 180°. This will result in the feedback to be positive and the loop will have enough gain to build up the signal.

2.3 Voltage Controlled Oscillators

Oscillators typically operate at a specific frequency. In order to vary the oscillation frequency, one has to change the impedance in form of either resistance or reactance. In this manner a single solution is available to achieve different frequency operation by controlling the design parameters. Generally, VCOs are divided into two basic architectures: LC based VCO and RC based VCO. In this work the main focus will be on the RC based VCOs. In the VCO design the voltage is used to control the oscillator. The voltage is denoted as V_{cntrl} and it is applied as an input voltage to the VCO tuning circuit. This V_{cntrl} can be used in different methods to tune the VCO frequency (Carnes,

Vytyaz, Hanumolu, Mayaram, & Moon, 2007; Changzhi & Jenshan, 2010; Maneatis, 1996; Yan & Luong, 2001).

2.3.1 RC based VCO

In RC ring oscillators architecture, there are number of delay elements and the output of each delay cell goes to the input of the other. Same will be for the output stage, where output from the last stage will be added back to the input of first stage to emulate a ring operation. As explained in Section 2.2, the closed-loop system should provide a phase shift of 180^0 (π) along with a unity gain at the oscillating frequency. Based on this fact, each delay cell must contribute a phase of $\frac{\pi}{N}$, where N is the total number of delay elements. Additionally in providing a complete phase shift of $360^0(2\pi)$ the remaining phase shift will be added up by a dc inversion due to inverter itself (Razavi, 2000).

RC oscillators can be constructed of either using single-ended or differential topologies. In single-ended design odd numbers of stages are required to create the oscillation and to avoid the latch-up, whereas this condition is not necessary in differential delay cell topologies.

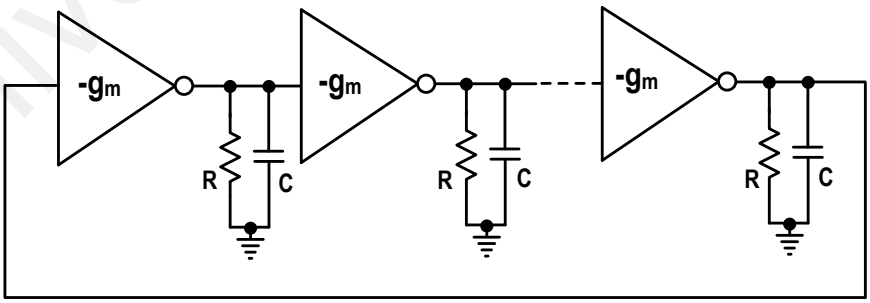

Figure 2.2 Ring oscillator linear model

Oscillation frequency for the ring oscillator can be determined by observing the linear model (Fahs, Ali-Ahmad, & Gamand, 2009) as shown in Figure 2.2. In order to estimate the oscillation frequency, it can be assumed that all delay elements contributes

equal amount of load resistance and capacitance. Hence the gain for each delay can be written as:

$$A_1(j\omega) = A_2(j\omega) = A_N(j\omega) = \frac{-g_m R}{1 + j\omega RC} \tag{2.4}$$

As described in (Razavi, 2000), ring oscillator must satisfy the Barkhausen criteria, stating:

$$|A_1(j\omega).A_2(j\omega).A_N(j\omega)| = 1 \tag{2.5}$$

$$< A(j\omega) = \theta = \arctan wRC = \frac{2k\pi}{N} \tag{2.6}$$

Based on the above equations, the oscillation frequency is given by:

$$f_0 = \frac{1}{2Nt_d} \tag{2.7}$$

where t_d is the delay for each stage and N is the total number of stages in RC VCO. It can be observed that oscillation frequency reduces with the increase in delay stages. Single ended oscillators are preferred for designs inheriting low power and rail to rail output requirement. Single ended designs are avoided for high speed designs due to their noise sensitivity which results in undesirable fluctuations at the output in terms of jitter. The noise is mostly due to the substrate noise which couples directly into the oscillator and modulates its supply voltage. Due to the single ended nature, these oscillators do not have the capability to reject the noise. For such high frequency designs it is suggested to use the differential delay cells having high common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) to reduce the noise effects.

On the other hand, differential RC oscillators can be constructed by using either even or odd number of stages. Differential RC oscillator is always preferred due to its dominating factor of high CMRR. Based on high CMRR, a differential delay cell provides better response in rejection of supply and substrate noise.

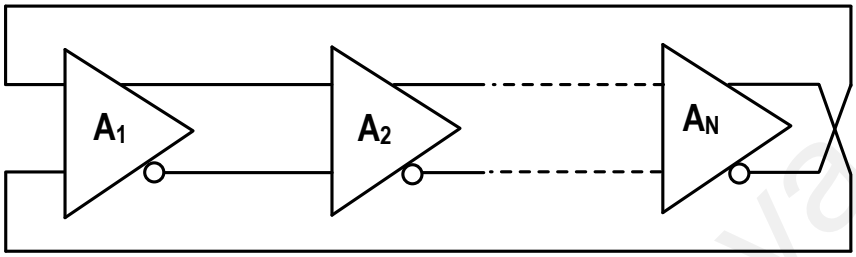

Figure 2.3 Differential delay cell

Figure 2.3 shows a differential delay cell with N number of stages. Each stage has a propagation delay of t_p which results in the total propagation delay of the loop to be Nt_p and total phase shift in the loop is $N\pi$.

therefore,
$$\frac{N\pi}{2\pi} = \frac{Nt_p}{T_{osc}} \rightarrow T_{osc} = Nt_p \quad (2.8)$$

In order to vary the frequency of the ring oscillator, either the number of stages (N) or the propagation time (t_p) must be changed. Differential ring oscillators frequency tuning can be achieved; by varying the output capacitor load, the resistance of the linear MOSFET, or the current handling capability of the circuits driving the load and even by changing the dc supply voltage of the oscillators.

2.3.1.1 Maneatis Delay Cell

A delay cell topology with symmetrical load is presented by (Maneatis & Horowitz, 1993). In order to provide high common-mode rejection ratio (CMRR) and wider frequency tuning range, symmetrical load is used along with dynamic biasing. A

differential NMOS based input pair is used along with symmetrical PMOS loads. Due to the differential structure, noise will be accounted in as common mode input as it observes equal impedance at each side. Common mode rejection will results in cancelling the supply noise (Carnes et al., 2007). In this topology the frequency can be tuned by varying the bias voltage (V_{bias}), which is normally realized by integrating additional replica bias circuit. Without the replica bias, the bias voltage input varies with the supply.

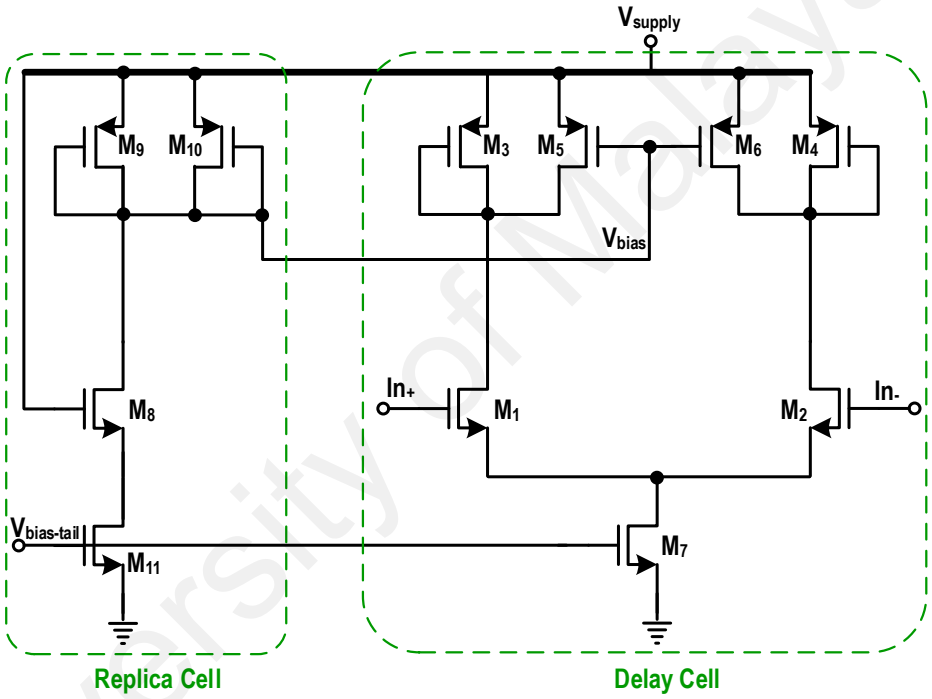

Figure 2.4 Delay cell proposed by Maneatis

In addition, tuning can also be realized by varying the tail current which requires an external biasing. The delay cell is sensitive to the supply variation, in which an external circuitry needs to be integrated to eliminate the supply noise.

2.3.1.2 Park and Kim Delay Cell

In order to improve the supply noise rejection, a differential delay cell is proposed by (Chan-Hong & Beomsup, 1999). In this topology the tail current is eliminated to reduce

the flicker noise contribution. A cross-coupled PMOS pair (M_3 and M_4) is used to improve the switching time, which helps in increasing the speed and reducing the transition time to improve the jitter.

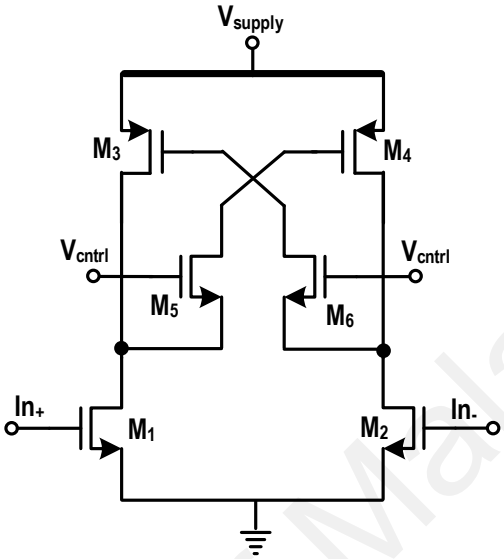

Figure 2.5 Delay cell by Park and Kim

Output frequency is controlled by adding two NMOS transistors (M_5 and M_6) to control the latched PMOS pair gate voltage. Increasing V_{cntrl} at the gates of NMOS pair (M_5 and M_6) results in turning ON the switches and hence initiating the latch to be stronger where M_5 and M_6 starts effecting the delay cell operation. Stronger latch results in increased delay, hence reducing the output frequency. This proposed method of control tuning is a bit risky, where a strong latch may also results in halting the VCO oscillation and the outputs may pull up to the supply on one end while pull down to the ground on the other.

2.3.1.3 Dual Delay Cell

In order to achieve high oscillation frequency a dual delay cell can be used in addition to Park and Kim delay architecture. Figure 2.6 shows one of the dual delay path delay (Zuow-Zun & Tai-Cheng, 2011). In a single loop ring oscillator there is a long

propagation delay that limits the oscillation frequency. This architecture helps to further reduce the delay of a typical ring oscillator.

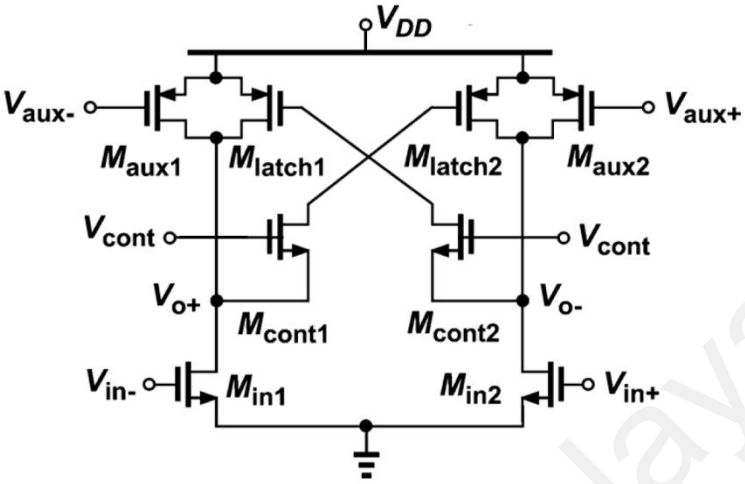

Figure 2.6 Dual-Loop differential delay cell

In this architecture, a delay cell with auxiliary delay path is added in dual delay path ring oscillators. Transistors $M_{in1,in2}$ and $M_{aux1,aux2}$ are the input devices of the main delay signal and auxiliary delay signal. Auxiliary inputs are switched earlier than the typical inputs, hence reduce the delay time and improve the oscillation frequency. To achieve high frequency oscillation in differential mode, the auxiliary devices M_{aux} are designed to be in strong inversion and the latch devices M_{latch} designed to be weaker.

2.3.1.4 VCO with Switched Capacitors

In order to improve the tuning range of the VCO without compromising on the phase noise performance, a dual tuning method is implemented in (Haijun et al., 2012). The design works in a top down methodology introduce switched capacitors are introduced to break the tuning curve into various curves. Without any capacitor tuned to be active, the VCO will be operating at the highest frequency. In order to switch to any lower frequency curve, the capacitors can be switched ON, which results in additional capacitance at the output nodes.

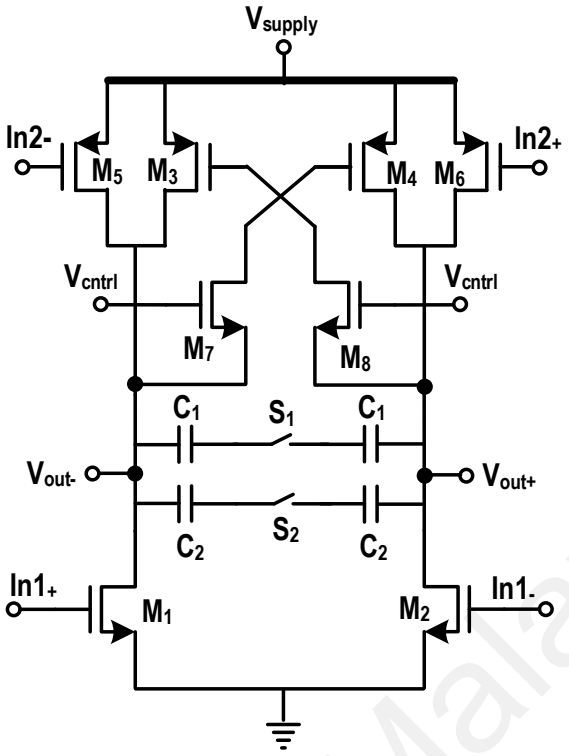

Figure 2.7 VCO with switched capacitors

Dividing the tuning curves actually helps to improve the phase noise performance by decreasing the VCO gain. This topology suffers in low linearity between tuning curves at lower frequency due to the added additional capacitances. Alternatively, there is always a limitation on adding the output capacitance. Increasing additional capacitance results in decreased output swing and this may also results in stopping the VCO from oscillation.

2.3.2 VCO Performance Parameters

The VCO performance can be evaluated based on different parameters as discussed in the following sections.

2.3.2.1 VCO Gain (K_{VCO})

VCO tuning range is directly proportional to the K_{VCO}. Where, K_{VCO} is defined as the slope of the frequency tuning curve or in other words it can expressed as the sensitivity

at which the output frequency changes with any change in the VCO input voltage (V_{cntrl}). A higher K_{VCO} reflects increased tuning range in a penalty of increased noise at the output (Haijun et al., 2012). This defines an added a challenge to implement a wideband VCO with acceptable phase noise performance by using a single tuning curve. K_{VCO} is normally measured in Hz/V.

2.3.2.2 VCO Tuning Range

Tuning range is used to define the ability of the VCO to operate in a certain range of frequency. It is normally described in terms of percentage. Based on this parameter, a VCO is known as narrow or wideband oscillator. Oscillators with tuning range $< 10\%$ can be considered as narrow-band oscillators. A narrow-band VCO is typically used where superior phase noise is required regardless of high bandwidth. On the other hand, a VCO with a tuning range $> 25\%$ can be considered as wideband oscillator. A wide tuning range oscillator can be implemented for a low oscillation frequency. Whereas, actual challenge is to achieve high oscillation frequency with wider bandwidth, without affecting much on the phase noise performance.

2.3.2.3 Power Consumption

Power supply is another contributor in defining the VCO performance. A wide tuning range oscillator can be implemented by using large supply voltage. The larger the supply rails the better will be the noise performance. For battery powered application, power consumption is a limiting factor in defining the VCOs performance parameters.

2.3.2.4 Load Parasitic

The VCO output is also influenced by the load parasitic. This is also called as drive capability. Adding higher loads can results in degrading the bandwidth with limited

output swing. Normally a buffer is used at the output of the VCO before adding in any driver stage. For operating at GHz range, topologies like current mode logic (CML) or low-voltage differential signaling (LVDS) can be used to drive the VCO output.

2.4 Phase Noise in Oscillators

The VCO performance depends on its phase noise parameter, which can be described as short term random frequency fluctuation. Phase noise is the key element in defining overall oscillator performance. Phase noise is a variant of jitter and it is characterized in frequency domain. In an ideal oscillator, the spectrum at the frequency, f_o will be expressed as an impulse as shown in Figure 2.8 (a). In reality, the circuit contributes different noise sources, which results in the changes in the oscillator spectrum. Actual oscillator spectrum as shown in Figure 2.8 (b) can be expressed as a skirting around the oscillation frequency (f_o).

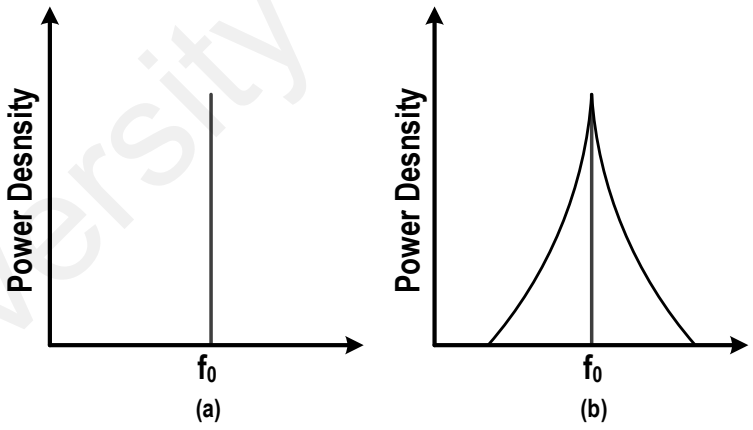

Figure 2.8 (a) Ideal oscillator phase noise (b) Real oscillator phase noise

Noise in CMOS circuits is mainly contributed due to flicker and thermal noise. The flicker noise is the leading noise element in MOSFET and it is generally known as 1/f or low frequency noise. It is generated due to movement of electrons inside the MOSFET channel. This noise element is mathematically expressed as:

$$\overline{v_{n,f}^2} = \frac{K_f}{C_{ox} \,.\, L_{eff} \,.\, W_{eff} \,.\, f} \tag{2.9}$$

where, K_f is contributed by the process, C_{ox} is the oxide capacitance, L_{eff} is the effective channel length, W_{eff} is the effective channel width and f is the operating frequency. In order to achieve high oscillation frequency, device capacitance is normally reduced by decreasing the device sizes. In order to improve the phase noise MOSFET sizing needs to be increased (Park, Lee, Kim, & Laskar, 2006) and this will results in decreasing the oscillation frequency. Additionally, phase noise can also be improved by decreasing the drain current or by increasing the oxide capacitance, which again will affect the circuit capability to provide high bandwidth or high oscillation frequency. Apart from flicker noise, thermal noise also contributes in the CMOS process and it is mainly present in the MOSFET and resistors. Thermal noise is also known as white noise due to its flat spectrum. It is normally expressed as:

$$\overline{v_{n,T}^2} = 4.\ k_B \,.T \,.R \tag{2.10}$$

where, k_B is the Boltzmann's constant, T is the absolute temperature and R is the resistance value. It can be concluded that thermal noise increases with rise in the temperature or increase in the resistance value.

In oscillators, phase noise results in up-conversion of both thermal noise and flicker noise (Mukherjee, Roblin, & Akhtar, 2007). In frequency domain the noise sources are multiplied by $1/f^2$, which results in shifting the white noise to $1/f^2$ with a slope of -20dB/dec and flicker noise to $1/f^3$ with a slope of -30dB/dec. Based on this information oscillator phase noise can be summed up in Leeson's phase noise model (Dickstein, 2012) developed by Dr. David B. Leeson's as given below:

$$L(\Delta f) = 10.\log\left[\frac{2FkT}{P_{in}}\left\{1+\left(\frac{f_0}{2Q_L\Delta f}\right)^2\right\}.\left(1+\frac{f_{1/f^3}}{\Delta f}\right)\right] \quad (2.11)$$

where, $L(\Delta f)$ is the phase noise expressed in dBc/Hz at an offset frequency of Δf from a carrier frequency of f_0, F is the active device phase noise factor, k is the Boltzmann's constant, T is the absolute temperature, P_{in} is the average power applied to the oscillator, Q_L is the resonator effective quality factor and f_{1/f^3} is the flicker corner. Flicker corner is the location where flicker noise is shifted to thermal noise as shown in Figure 2.9.

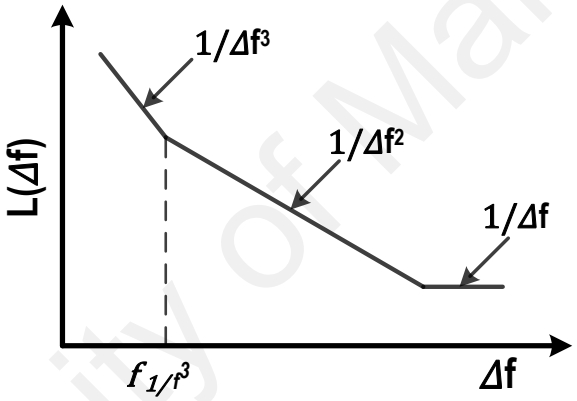

Figure 2.9 Oscillator phase noise spectrum (Deng, Yin, & Du, 2009)

In order to generate a relationship between VCO parameter and phase noise, (2.11) is modified (R. M. Weng, 2009) as follows:

$$L(\Delta f) = 10.log\left\{\left[1+\frac{f_o^2}{(2\Delta f Q_L)^2}\right]\left(1+\frac{f_c}{\Delta f}\right)\frac{FkT}{2P_{in}}+\frac{2kTRK_{VCO}^2}{\Delta f^2}\right\} \quad (2.12)$$

VCO tuning range is defined by the VCO gain (K_{VCO}). Presenting K_{VCO} to higher values will results in wider tuning range. (2.12) shows a direct relationship between phase noise and K_{VCO}. For a typical VCO, wide tuning range can be achieved by increasing the K_{VCO} at the cost of degraded the phase noise. It is important that K_{VCO}

should be reduced to achieve better phase noise figures. This phenomenon can also be defined in time-domain as jitter:

$$\Delta\omega_{osc}\,(V_{cntrl}) = K_{VCO}\,.\,V_{cntrl} \tag{2.13}$$

where, $\Delta\omega_{osc}$ is defined as the frequency variation in time domain and V_{cntrl} is the VCO input tuning voltage to control the frequency. The variation in the output frequency is known as jitter in time-domain, which is equivalent to phase noise in frequency-domain. As per (Yin, Mak, Maloberti, & Martins, 2016) there is a relationship between phase noise and jitter:

$$J_{RMS}^2 = 2\left(\frac{1}{2\pi f_c}\right)^2 \int_0^\infty 10^{\frac{\mathrm{L}\{\Delta f\}}{10}}\, d(\Delta f) \tag{2.14}$$

where, J_{RMS}^2 is the RMS jitter. As per the above discussion, higher tuning range requires large K_{VCO}. For a large K_{VCO}, a slight change in V_{cntrl} will results in large variation in the output frequency. Additionally, the increase in the K_{VCO} will result in degrading the phase noise performance (Haijun et al., 2012).

2.5 Summary

In this chapter literature review is done to understand the RC based VCO design. Following are some points describing the overall summary.

- The design principles have been discussed for RC based oscillators.
- It is observed that RC based VCO has tendency to achieve wide tuning range by varying either the output capacitor, varying the resistance of linear MOSFET, varying the current handling capability of the circuits driving the load and even

could be tuned for high oscillation frequencies by changing the oscillator dc supply.

- On the other hand, the challenging performance element in RC VCOs is the phase noise that is contributed by both thermal and flicker noise in CMOS process.
- The K_{VCO} is an important parameter in defining the VCO tuning range as well as the noise contribution. A higher K_{VCO} achieves wider tuning range at the cost of high jitter value in time domain and worst phase noise performance in frequency domain.

CHAPTER 3: DESIGN AND METHODOLOGY

3.1 Introduction

In recent years, a vast development has been achieved in both wireless and medical applications. Consumers are demanding optimized power consumption along with less form factor. This adds in more complexity and challenges to the VCO design. Due to the inductor footprint, extra processing cost and less tuning ability, LC based VCO designs are not preferred for wideband applications. On the other hand, RC based VCO design can be a favourable choice due to low chip area consumption, providing various tuning topologies with no additional fabrication steps and no additional cost. Whereas, the main challenge in RC based VCO is the degraded phase noise performance at high oscillation frequency due to low quality factor and high VCO gain.

The main motivation of this research is to design and develop a wideband RC based VCO, without compromising the phase noise performance at optimal power consumption. This will encourage the adoption of an RC VCO for applications in GHz range. In this chapter, a programmable current based architecture is presented to achieve the wideband RC based VCO for GHz range. Each block is separately defined along with its detailed description.

3.2 Programmable Current based Wideband RC VCO

In addition to high oscillation frequency, the aim of this proposed work is to develop a wide tuning range VCO without increasing the K_{VCO} to improve the phase noise performance. Conventional wide range delay cells exhibits a single frequency tuning curve to cover the whole frequency range (Changzhi & Jenshan, 2010), which results in very large value of VCO gain ($K_{VCO} \rightarrow$ 7.5-9 GHz/V). The reported design is more sensitive to noise and causes large variations across tuning range, which is not desirable

for the practical integration of phase locked loop (PLL) circuitry. Some previous literature work reported alternative architectures for wide tuning range VCOs by distributing the main frequency curve into number of curves (Haijun et al., 2012). This helps in increasing the bandwidth to some extent exhibiting lower K_{VCO} at the cost of linearity between the curves. Switch capacitors are added at the output of each delay cell to shift the frequency curve from higher to lower. This topology also has limitation in adding the capacitors. Additional capacitance at the output results in limiting the output swing which results in decreasing SNR and it may also results in stopping the VCO to oscillate due to decrease in the operating bandwidth.

In order to overcome the above mentioned limitations, an enhanced approach is deployed in this work to achieve high frequency and wide tuning range from a RC based ring oscillator. The implemented VCO architecture is based on a bottom up topology in which programmable currents are digitally controlled to set the VCO output frequency. The top level schematic for the proposed architecture is illustrated in Figure 3.1. Instead of adding the switched capacitors (Haijun et al., 2012), a programmable current source is added in parallel to V-to-I current, mirrored from PMOS, M_4. Overall frequency range is divided into set of tuning curves and output frequency can be switched to any of the tuning curves by digitally controlling the programmable currents. This helps to fulfil the purpose of achieving a wider tuning range along with the enhancement of phase noise performance due to reduction in K_{VCO}.

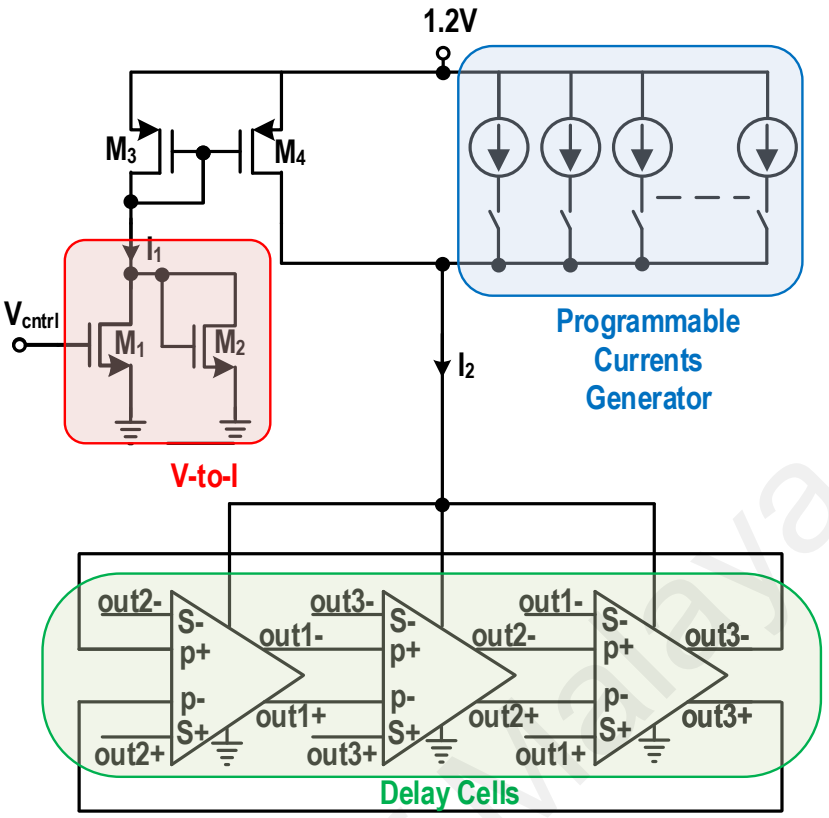

Figure 3.1 Proposed VCO block diagram

Additionally, output frequency on a specific tuning curve can be controlled by varying the VCO tuning control voltage, V_{cntrl} (0 to 1.2V). In order to achieve high frequency oscillations, a RC based differential dual delay cell is adopted to generate the oscillation. Below is the detailed description for each of the individual blocks in their respective section.

3.2.1 V-to-I Converter

The VCO output frequency is normally controlled by varying the control voltage (V_{cntrl}). The V_{cntrl}, as shown in Figure 3.2 is converted to current by using the V-to-I converter, which is then injected into the delay cells to generate the output frequency.

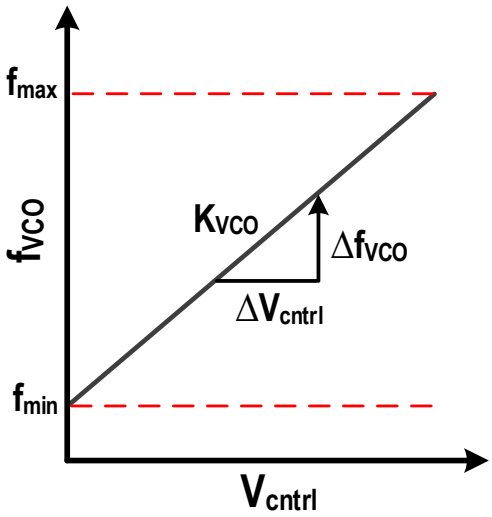

Figure 3.2 VCO Frequency vs control voltage

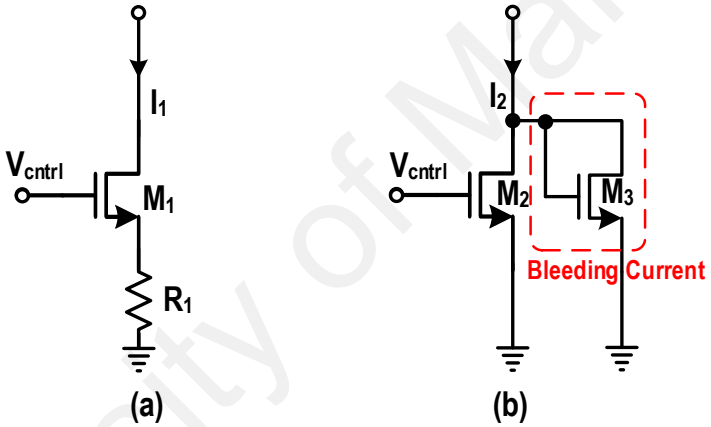

Figure 3.3 (a) Typical VCO V-to-I (b) Proposed VCO V-to-I

Figure 3.3 shows the comparison between typical V-to-I converter and the proposed architecture. Typically, common source configuration is used along with a source degeneration resistor (R_1) in V-to-I conversion. In this case, the resistor assists in the control of linearization of the current, any voltage across V_{ctrl} will results in voltage drop across R_1 rather than the overdrive voltage ($V_{dsat} = V_{GS} - V_{th}$) of M_1. This helps to smooth the variation of I_1. The linearity is obtained at the cost of following;

1. One of the major issues is the introduced thermal noise in (2.10), which is directly proportional to the resistor. Therefore increasing the value for R_1 will results in higher noise at high frequency.

2. When there is no input voltage (V_{ctrl}= 0V), current I_1 will be zero. In this case VCO will have no bias current and instead of oscillating at a certain frequency (f_{min}), there will be no oscillation. This also creates a dead zone till V_{ctrl} could be high enough to create the channel ($V_{GS} \geq V_{th}$) in order to flow the drain current. Therefore, source degeneration approach requires bleeding current which needs to be present all the time by an additional circuitry to avoid the dead zone. The additional circuitry needs extra biasing circuitry, hence consumes additional power and contributes noise due to additional devices and noise paths.
3. It also introduces substrate noise coupling through the input transistor due to the bulk effect ($V_{GS} \neq 0$).
4. On-chip resistor always shows large variation (approximately ±20%) across process corners. The resistance variation results in the change of current and hence the output frequency. Therefore this approach is not helpful across process and leads to high K_{VCO} variations.

Basic aim is to reduce overall noise contribution by reducing the number of devices along with the elimination of thermal noise contributed by resistors. Figure 3.3 (b) shows the proposed topology for V-to-I. A diode connected MOSFET (M_3) is introduced to eliminate the source degeneration. Below are the advantages in this approach;

1. No thermal noise contribution due to the elimination of the source degeneration resistor.
2. Diode connected MOSFET (M_3) eliminates the need of any additional circuitry for generation of bleeding current. M_3 will remain ON ($V_{DS} = V_{GS}$) at all times,

even at $V_{ctrrl} = 0$V and I_2 will be always available. This eliminates the dead zone and VCO is able to oscillate at minimum frequency (f_{min}).

3. No substrate noise coupling due to removal of body or bulk effect ($V_{SB} = 0$V).
4. Reduced process variations due to elimination of source degeneration resistor.

The proposed V-to-I converter leads in terms of reduced noise, elimination of dead zone and reduction in process variations. The proposed topology only lags in linearity, where I_2 is dependent on square of the overdrive voltage (square law). The non-linear effect is overcome by reducing the gain for this stage.

3.2.2 Dual Differential Delay Cell

The VCO performance parameters are defined by the core architecture performance. Therefore, the core architecture holds the key role in the whole design. In case of RC based oscillators, delay cells are responsible for generating the oscillations along in defining the tuning capability. In this work a dual delay based differential ring oscillator has been adopted. This topology has the ability to oscillate at high frequency and also delivers better phase noise characteristics (Ge, Chen, Fen, & Ji, 2004).

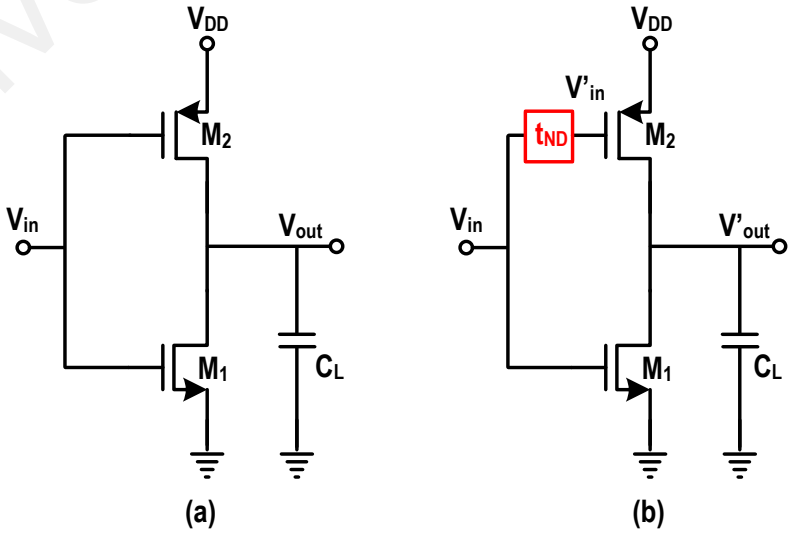

Figure 3.4 (a) Typical delay cell (b) Delay cell with negative delay

In dual delay based ring oscillator a negative delay is added to a regulator inverter. The negative delay results in early signal on PMOS of Figure 3.4 (b). In Figure 3.5, Region 1 shows that PMOS is ON while NMOS is OFF. At time = t_1, PMOS input (V'_{in}) will have an advance rising edge which results in charging of the output before region 2. In region 2, the output remains high and retains the previous state due to OFF state for both MOSFETs.

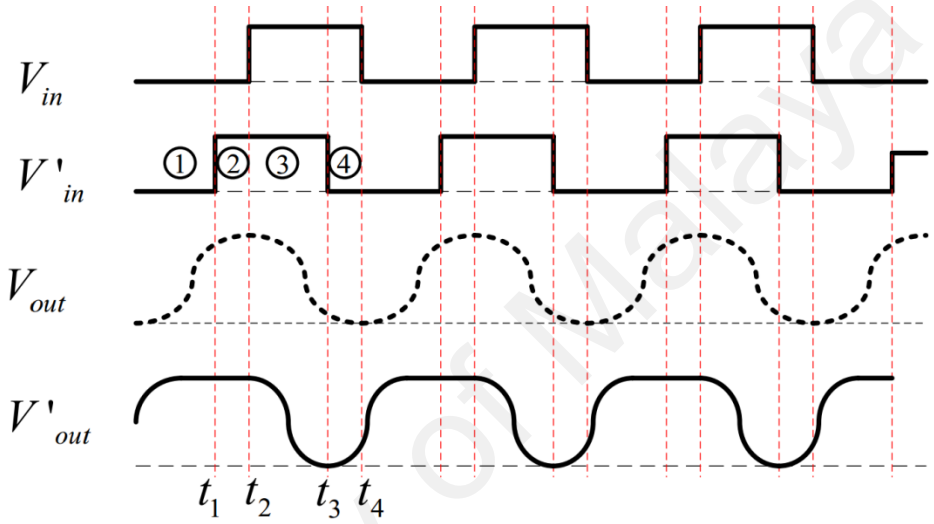

Figure 3.5 Negative Delay Output waveform (J.-K. Lee, Yi, Ahn, & Jeong, 2009)

At time = t_2, PMOS is already OFF and NMOS turns ON, which results in pulling low at the output. Later at time = t_3, PMOS will be ON and the output will again start charging before NMOS goes OFF. Finally at time = t_4 PMOS is completely ON while NMOS is OFF and the output will be raised till the supply voltage. Therefore, the negative delay actually helps by adding the pre-charging, which results in reducing the propagation delay.

Figure 3.6 shows the actual implemented schematic for the dual delay cell based ring oscillator. It can be seen that a primary delay inputs ($p_+ \& p_-$) are taken by NMOS differential pair M_1 and M_2, where secondary delay path ($s_+ \& s_-$) is taking negative delays inputs to the PMOS differential pair M_3 and M_4. In addition M_3 and M_4 source

terminals are connected together to feed through accumulated current I_{PROG}. Whereas, I_{PROG} is the combination of current coming from V-to-I converter and the programmable currents as shown in Figure 3.1.

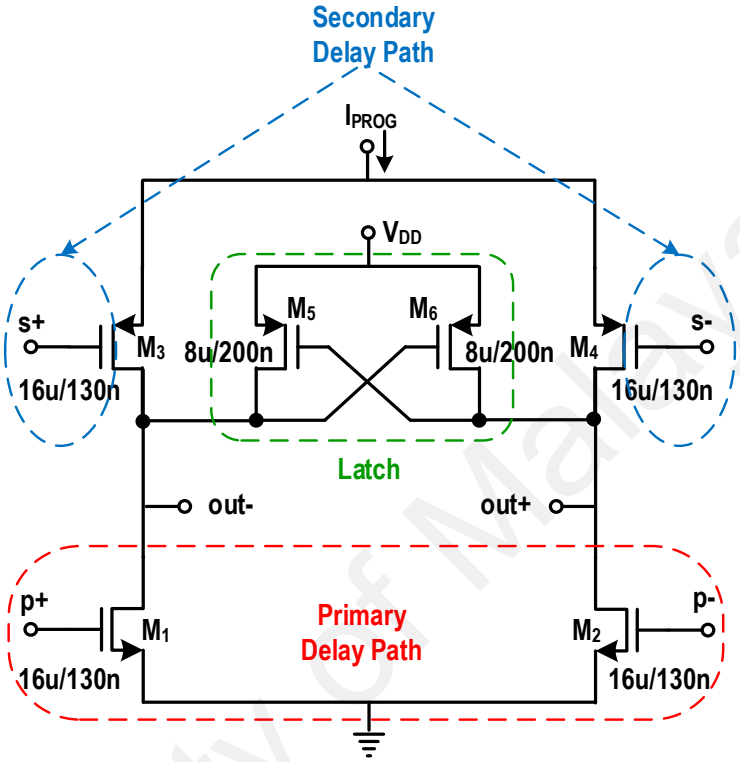

Figure 3.6 Delay cell implemented schematic

Cross-coupled pair M_5 and M_6 is added to act as a latch. The latch is introduced to achieve two important aspects: 1) it helps speed up the delay cell by decreasing the rise and fall timings 2) it also improves sharp rise and fall timings which helps to reduce the jitter. In order to obtain rail-to-rail output, M_5 and M_6 source terminals are connected together to the supply. Rail-to-rail output always helps in improving the signal to noise level (SNR). It can be observed that sizing for M_5 and M_6 are kept lower than M_3 and M_4. This results in lowering latch strength and helps in improving the speed. A strong latch (large device sizing) results in strong pulling of the output nodes to high and low, which results in reducing the speed.

In addition to the high speed, dual delay cell also improves the noise performance. In a typical delay element, PMOS transistors are added as a gain stage. Therefore, the transistors are conducting at all times and results in an overall increase in noise contribution. Dual delay cell architecture helps in reducing the noise contribution by periodically switching the gain transistors M_3 and M_4 (Eken & Uyemura, 2004). Below is the equation showing how M_3 and M_4 switching results in reducing the overall noise contribution:

$$P_{switching} = \frac{\Delta T}{T} P_{continuous} \tag{3.1}$$

where $P_{switching}$ is the noise power at the output, $P_{continuous}$ is the noise from a delay cell output having regular gain transistors, ΔT is the conduction time and T is the time-period. It can be clearly observed from (3.1) that introducing the switching period ΔT helps in reducing the noise power.

3.2.3 Programmable Current Generation

As per the earlier discussion the main idea was to achieve a wide range operation without compromising VCO linearity along with lower K_{VCO}. In this work a bottom up topology has been presented to control and distribute the single VCO tuning curve to multiple tuning curves. Frequency can be shifted from lower to higher tuning curve by adding additional current. The additional current should not affect the performance of the VCO due to any changes in supply, process or temperature range. In order to meet the requirements, programmable current generation architecture has been introduced.

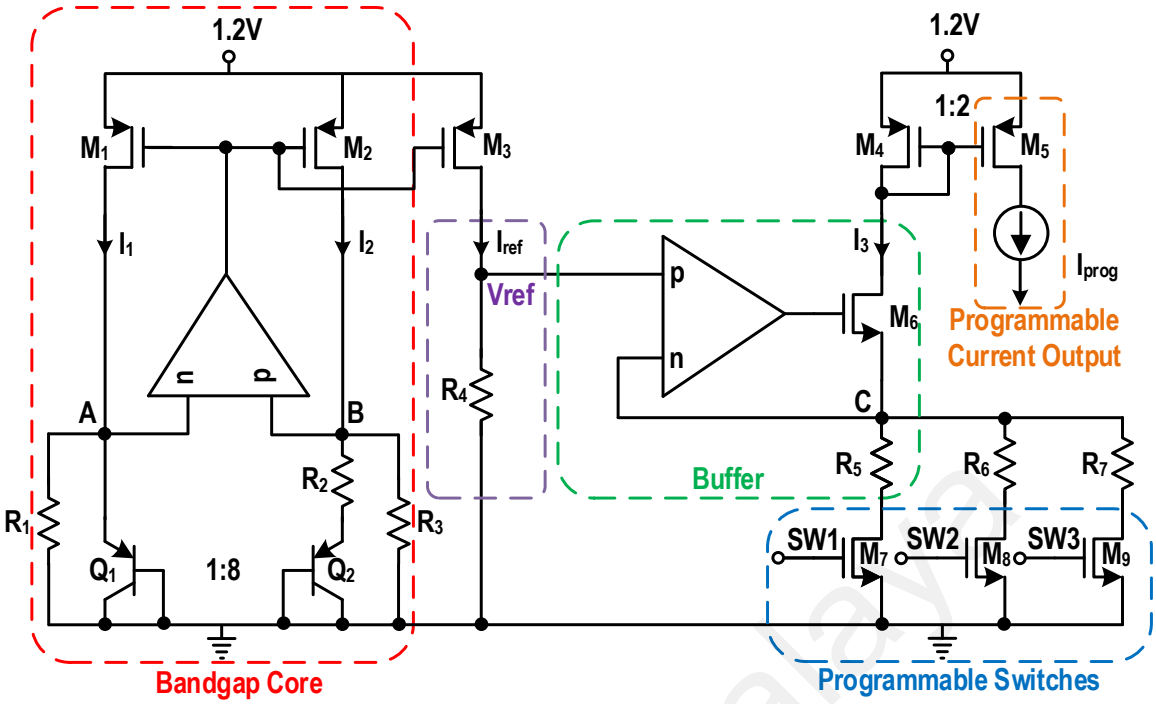

Figure 3.7 Programmable current generator

Figure 3.7 shows the schematic for the implemented programmable current generator. The actual challenge for programmable current generation was to fix the current which can easily be varied due to changes in the supply voltage, temperature and process variations. Therefore, a bandgap circuit is developed to generate the fix reference voltage (V_{ref}) and V_{ref} is fed through the resistor network via buffer to generate the programmable current. The programmable currents were controlled via digital decoder to switch ON/OFF the resistive network.

A mid-supply of about 0.6V of V_{ref} is required to provide sufficient headroom for all the devices in buffer and programmable current circuitry. A conventional bandgap can only provide a reference voltage of 1.25V (Sanborn, Ma, & Ivanov, 2007), known as silicon bandgap voltage provided at zero degree Kelvin. Such a low reference is not possible from a conventional bandgap topology. Therefore a current based bandgap circuit is utilized for this application (Kleczek & Grybos, 2014) to generate a lower voltage by passing the bandgap current through a resistor.

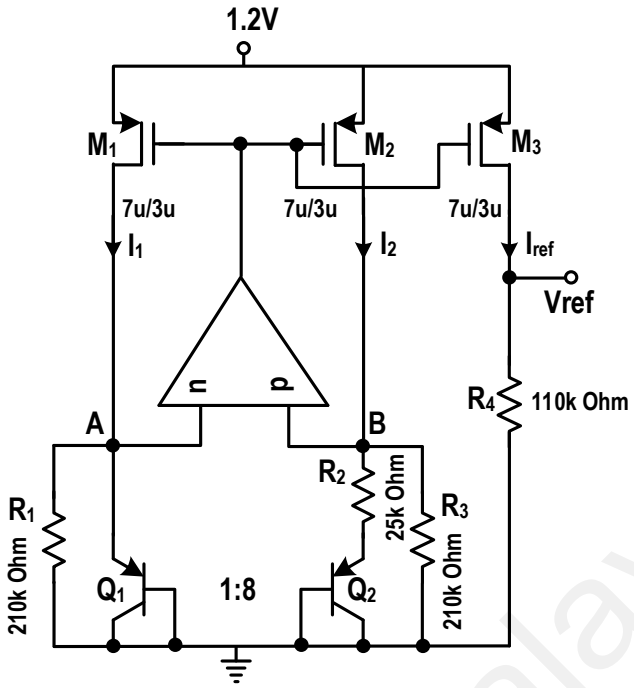

Figure 3.8 Bandgap circuit

Figure 3.8 shows the implemented current based bandgap. Operational amplifier is used to fix the potential at nodes A and B. In line to this the current I_1 and I_2 will be also same. As the potential at node A and B is equal, a CTAT (compliment to absolute temperature) current flows through resistors R_1 and R_3 ($R_1 = R_3 = 210k\Omega$) having same value and characteristic. On the other hand, a PTAT (positive to absolute temperature) voltage is generated through R_2 (25kΩ). Where, current I_2 can be expressed as:

$$I_2 = \frac{V_{EB2}}{R_3} + \frac{\ln(N) \, . \, V_T}{R_2} \tag{3.2}$$

where, M_1, M_2 and M_3 are set to an aspect ratio of 7um/3um. With equal dimensions between M_1 to M_3 results in equal currents, $I_1 = I_2 = I_{ref} \cong 5.5\mu A$. Finally, the temperature independent current I_{ref} is passed through R_4 to generate the reference voltage, V_{ref}. This V_{ref} can be expressed as:

$$V_{ref} = \frac{R_4}{R_3}\left(V_{EB1} + \frac{\ln(N).V_T.R_3}{R_2}\right) \tag{3.3}$$

$$V_{ref} = I_{ref}.R_4 = 5.5\mu.110K \cong 0.6V \tag{3.4}$$

The generated V_{ref} is used to source the programmable currents by switching the resistance. Sourcing current directly from the V_{ref} branch may results in loading effect, where higher current may results in the drop of V_{ref}. In order to avoid any loading effect, a buffer circuit (gain = 1) is added to generate 0.6V at node C. Figure 3.9 shows the programmable current output stage, where op-amp is used as a unity gain feedback. Transistor M_6 is acting as Power MOS and it allows the current to flow towards VCO.

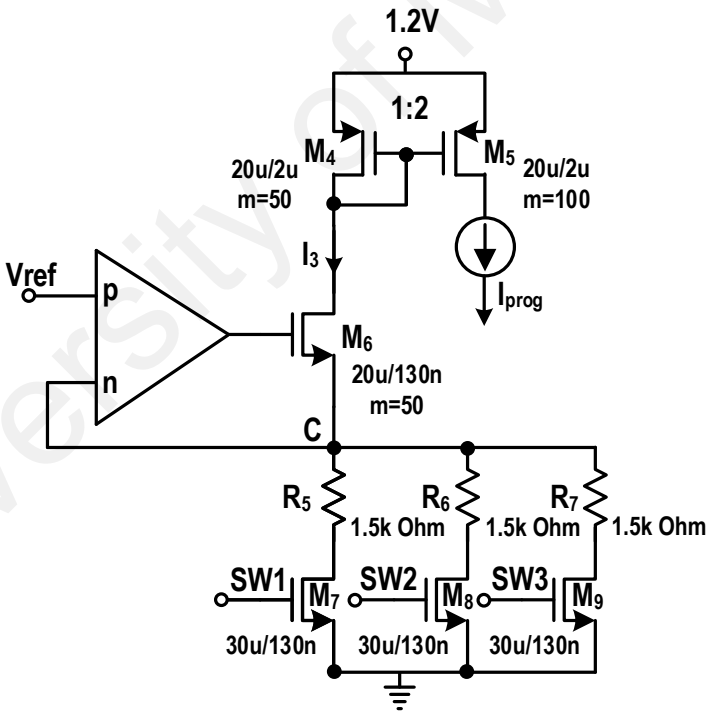

Figure 3.9 Programmable current output stage

The buffer output voltage (node C) is applied to across resistors R_5 to R_7 to generate programmable currents. A two-bit digital input is applied to a 2x4 decoder to generate different combinations to switch ON/OFF the resistors via SW1 to SW2. Resistor values are set to 1.5kΩ to contribute an individual current of approximately 400μA. At digital

input of 2'b00, all switches will be OFF with no current contribution. When digital input is switched to maximum (2'b11) then the all the switches will be closed and programmable current will contribute a maximum current. The total accumulated current I_3 is doubled to generate the VCO programmable current I_{prog} by mirroring M_4 to M_5 with a ratio of 1:2.

3.3 VCO Layout

In order to verify the required outcomes, physical layout has been done for the proposed VCO architecture in Silterra 130nm CMOS platform. The implemented layout is shown in Figure 3.10. The core of the VCO architecture only consumes an overall area of 0.304x0.262mm^2. This area is inclusive of the on chip bandgap, programmable currents and VCO delay cells circuitry.

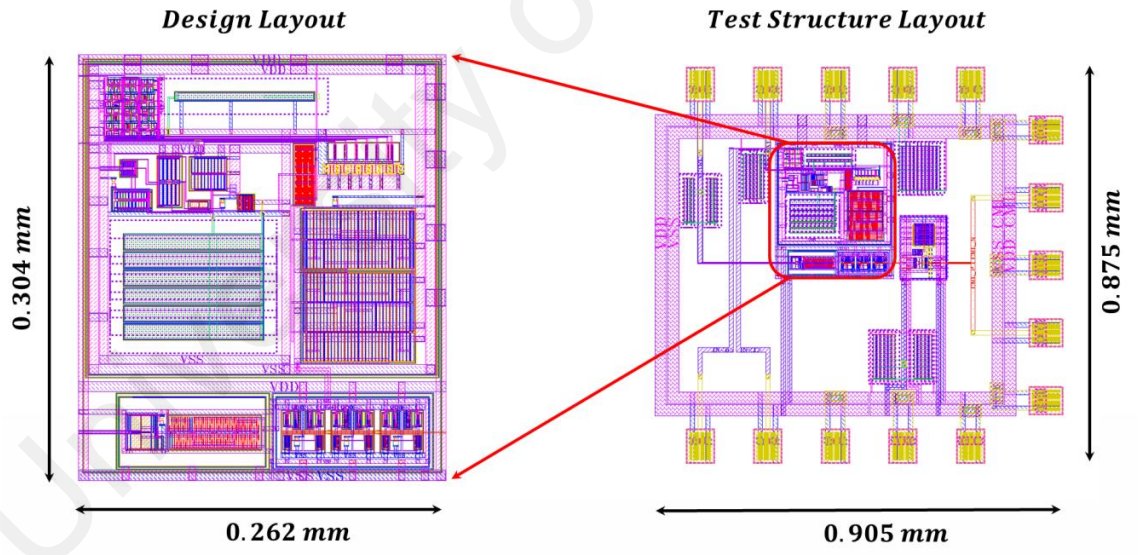

Figure 3.10 VCO Test-Chip layout

3.4 Summary

In this chapter, the design implementation and methodology is discussed in detail. Following are the points describing the overall summary.

- Detailed description has been presented for the proposed programming current architecture.
- The implemented circuit blocks have also been explained along with necessary knowledge on the delay cells, V-to-I converter and their trade-off with the phase noise and VCO tuning range.
- On-chip bandgap circuit is added to reduce the power supply, temperature and process dependent in the programming currents. It helps to reduce the phase noise contribution by programming currents, hence improves the phase noise at VCO output frequency.
- Physical layout has been implemented for the proposed design so that the proposed architecture can be further characterized on actual Silicon implementation.

CHAPTER 4: RESULTS AND DISCUSSION

4.1 Introduction

In this chapter detailed simulation results are presented. The design is implemented and simulated using low voltage Silterra 130nm technology in Cadence IC design tool. The 130nm technology is used due to its lesser parasitic, higher f_T resulting in higher operating frequency. In order to achieve a successful silicon lab results, the proposed VCO architecture is simulated and verified across temperature, supply and process corner variations. The proposed VCO architecture is composed of different blocks, where each block is simulated based on its characteristics.

4.2 Bandgap Analysis

VCO tuning is achieved by programming the delay cell currents. Bandgap is responsible for providing the programming current. Any variation in the programming current leads to frequency variations at the output of VCO. With this regard the bandgap is verified across random simulation setup to verify that the architecture is stable across temperature, supply and process corner variations.

4.2.1 Bandgap Core Loop Stability

In a typical bandgap, a stable reference voltage is attained by a fixed voltage at both nodes A and B (Figure 3.7). Normally, for higher supply voltages (> 1.8V) a cascaded structure is used to provide higher gain, which helps to overcome the channel-length modulation to maintain equal voltage in both branches of I_1 and I_2 of Figure 3.7. This results in the bandgap output voltage to be as supply independent. In order to achieve low voltage operation, the proposed design is set to 1.2V that limits the supply headroom. Therefore, an operational-amplifier is used to rectify and preserve equal voltages at nodes A and B in a closed loop response. In order to make this loop

functional, stability analysis is performed to study the gain and phase plots. Based on the Barkhausen's criteria, the system is considered stable if at the gain crossover (Gain = 1) the phase is less than -180°. In general terms, a stable systems must have a phase margin of at least 45° ((Razavi, 2000)).

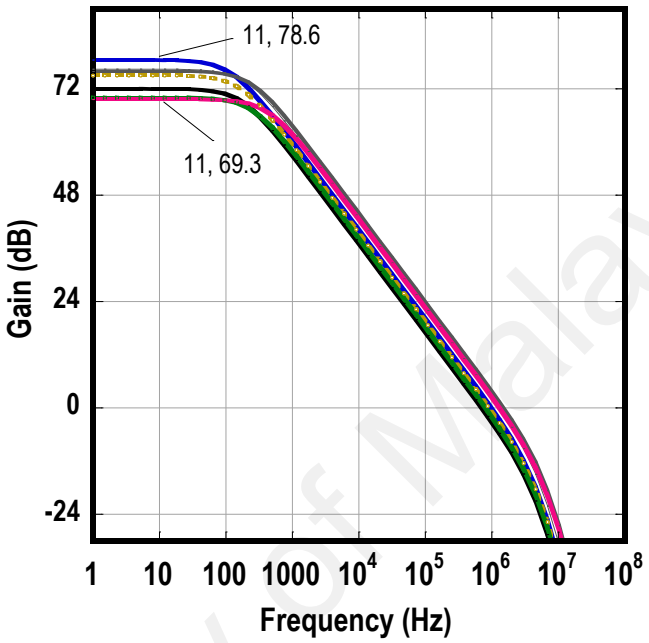

Figure 4.1 Bandgap post-layout Loop Gain at FF, FS, SF, SS corners

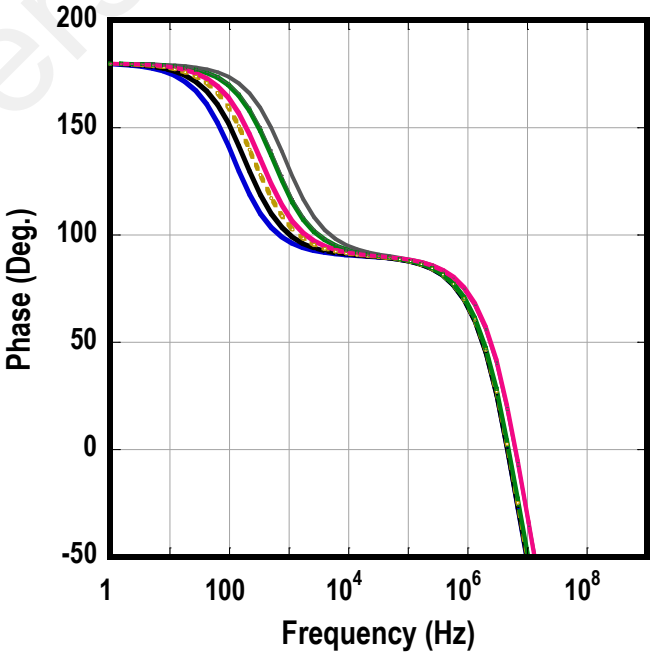

Figure 4.2 Bandgap post-layout Loop Phase at FF, FS, SF, SS corners

The bandgap stability is simulated across temperature (-40 to +80℃), supply (1.2V±10%) and process corners to make sure that the loop is stable with sufficient gain. Figure 4.1 shows the post-layout simulation results for loop gain, with a maximum gain of 78.6dB and a unity gain bandwidth of approximately 1 MHz. On the other hand, post-layout loop phase plot is shown in Figure 4.2. The bandgap loop observes a stable behaviour with a phase margin > 45 at 1MHz (unity gain bandwidth). Table 4.1 tabulates the summary of bandgap post-layout gain and phase margins across extreme process corners (ff = fast and ss = slow) with supply and temperature variations. Results show a stable behaviour with sufficient gain and phase margins.

Table 4.1: Bandgap post-layout loop phase and gain margin at extreme corners

Corners, temperature, voltage	**Phase Margin**	**Gain Margin**
ff, -40°C, 1.08V	67.1°	17.7
ff, 27°, 1.08V	71.6°	20.0
ff, 80°C, 1.08V	74.2°	21.4
ff, -40°C, 1.32V	61.9°	16.0
ff, 27°C, 1.32V	68.1°	18.5
ff, 80°C, 1.32V	71.0°	19.8
ss, -40°C, 1.08V	68.0°	18.0
ss, 27°C, 1.08V	72.3°	20.1
ss, 80°C, 1.08V	73.6°	21.1
ss, -40°C, 1.32V	62.3°	16.1
ss, 27°C, 1.32V	67.7°	18.4
ss, 80°C, 1.32V	70.4°	20.3

* ff – Fast NMOS fast PMOS, ss – Slow NMOS slow PMOS

4.2.2 Bandgap Transient and DC Response

In addition to the stability analysis, the bandgap is also tested at different supply ramp-up in transient simulations. This helps to evaluate the bandgap in a real time system where the supply can take any ramp-up time.

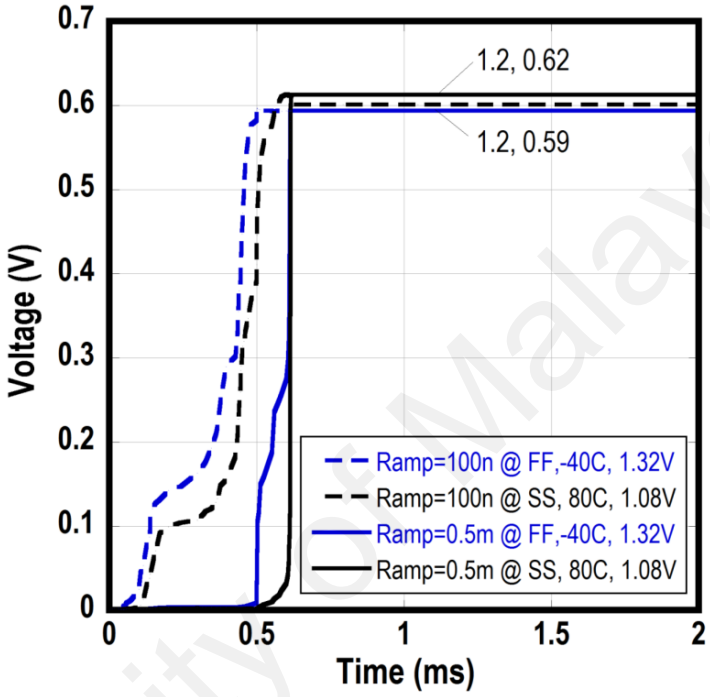

Figure 4.3 Bandgap post-layout transient response at different supply ramps and corners

The bandgap post-layout is tested across different process corners along with supply variation of 1.2V±10% in the temperature range of -40 to +80℃. Some of the extreme corners (fast, 1.32V, -40℃ and slow, 1.08V, 80℃) with supply ramps of 100ns and 0.5ms can be seen in Figure 4.3. The bandgap shows excellent performance with an output voltage of 0.6V and a maximum variation of only ±2.5%.

Bandgap post-layout output is also simulated across temperature variation with Monte-Carlo sweep to verify both process and physical mismatch. Figure 4.4 shows the stable bandgap output across Monte-Carlo (MC) with a temperature sweep between -

40°C to 80°C. It is also observed that the bandgap exhibits a process variation of only ±1.75% across MC variation.

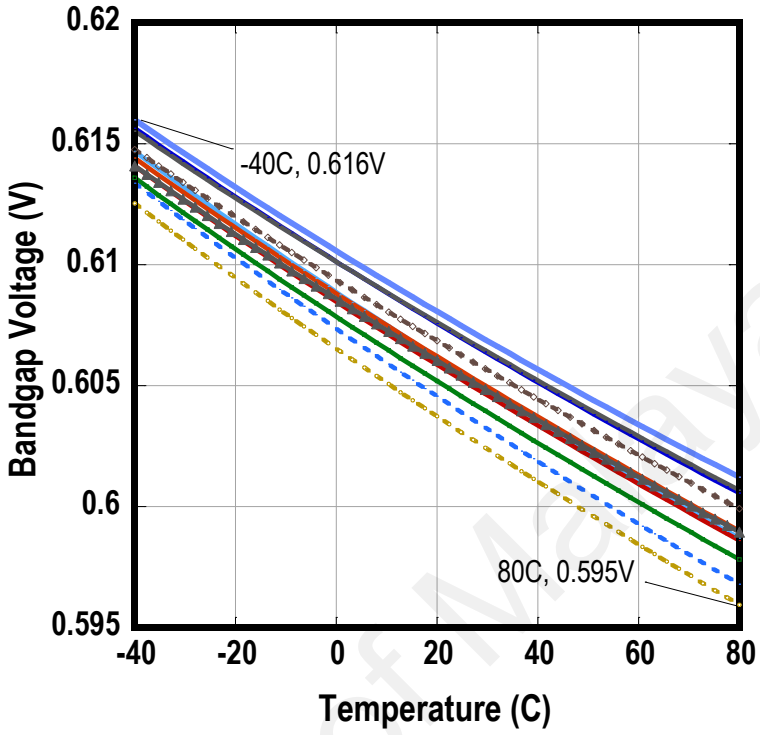

Figure 4.4 Bandgap post-layout temperature sweep across Monte-Carlo

4.3 Programmable currents

As discussed earlier, programmable currents will be responsible in providing the required current to tune the VCO. Therefore, the currents must be stable to alleviate any frequency fluctuations. Bandgap output voltage feeds to the input of the programmable current. An unity gain amplifier is added to avoid any loading directly at the bandgap output at any programmable currents.

In order to provide stable currents, unity gain amplifier loop (Figure 3.7, node C) is simulated across different process corners along with supply variation of 1.2V±10% in the temperature range of -40 to +80℃. Figure 4.5 shows the post-layout loop gain plot with a maximum gain of 38.5 dB and a unity gain bandwidth of approximately 10 MHz. It can also be seen that there is no gain reduction across any process corner.

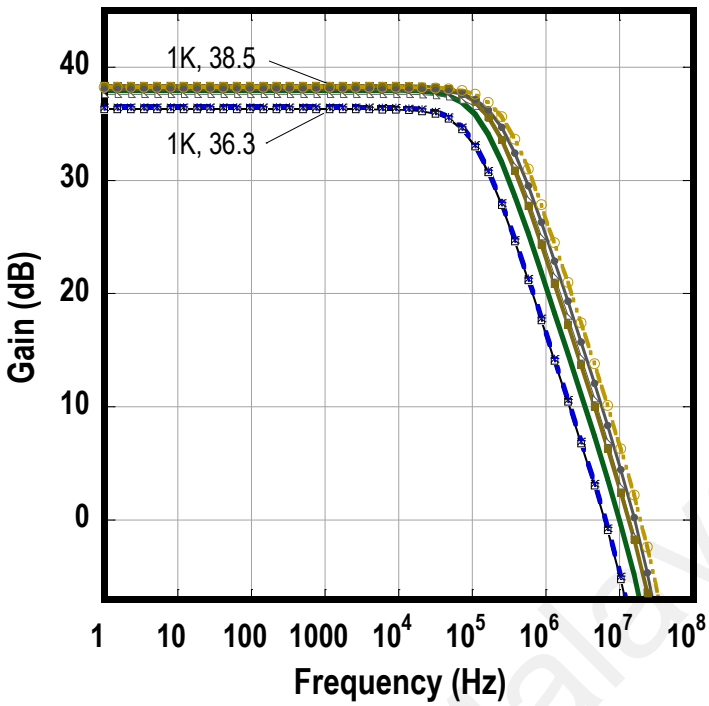

Figure 4.5 Programmable Current post-layout Loop Gain at FF, FS, SF, SS corners

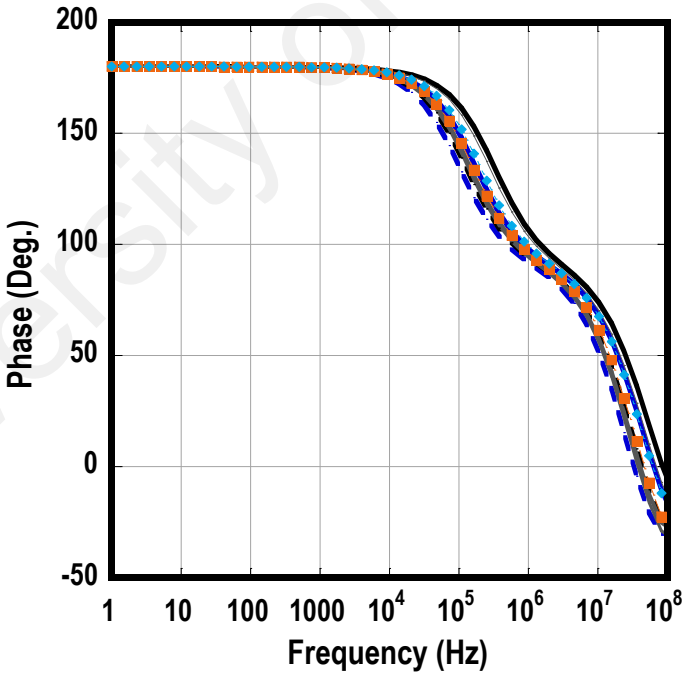

Figure 4.6 Programmable Current post-layout Loop Phase at FF, FS, SF, SS corners

Loop phase plot can be seen in Figure 4.6, where at 10 MHz (at unity gain bandwidth), the phase margin is > 45 degrees across all corners. Therefore, the programmable current loop is stable across all corners. Table 4.2 tabulates the summary

of programmable current loop gain and phase margins across extreme process corners (ff = fast and ss = slow) with supply and temperature variations. The programmable current loop exhibits a stable behaviour with sufficient gain and phase margins.

Table 4.2: Programmable current post-layout loop phase and gain margin at extreme corners

Corners, temperature, voltage	**Phase Margin**	**Gain Margin**
ff, -40°C, 1.08V	54.2°	18.6
ff, 27°C, 1.08V	54.7°	18.4
ff, 80°C, 1.08V	54.9°	18.4
ff, -40°C, 1.32V	52.7°	19.4
ff, 27°C, 1.32V	52.9°	18.9
ff, 80°C, 1.32V	53.0°	18.5
ss, -40°C, 1.08V	65.2°	21.6
ss, 27°C, 1.08V	65.7°	21.2
ss, 80°C, 1.08V	66.1°	21.8
ss, -40°C, 1.32V	61.7°	22.2
ss, 27°C, 1.32V	62.2°	20.7
ss, 80°C, 1.32V	62.4°	19.5

* ff – Fast NMOS fast PMOS, ss – Slow NMOS slow PMOS

Finally, the programmable current is simulated in transient analysis to visualize the actual current response across process corners along with a supply variation of 1.2V±10% in the temperature range of -40 to +80℃. The programmable current intensity is controlled via 2-bit digital input.

The post-layout design is first simulated across process corners that can be observed in Figure 4.7. Current is stable at any input across any process corner along with supply and temperature variations. Secondly, in characterizing the reliability for random

variation, the design is also tested across Monte-Carlo for both process and mismatch. Figure 4.8 describes the stable behaviour across Monte-Carlo variations.

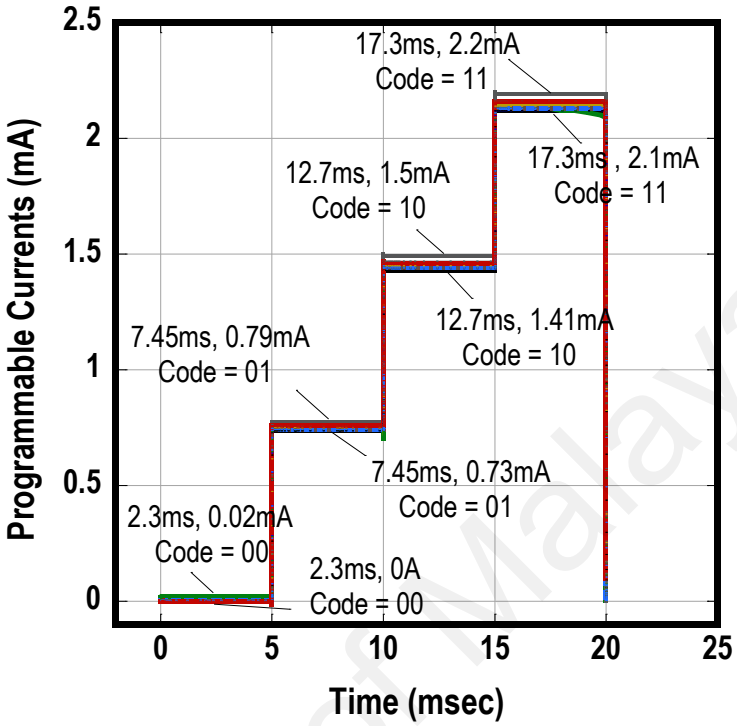

Figure 4.7 Programmable current post-layout switching across process corners

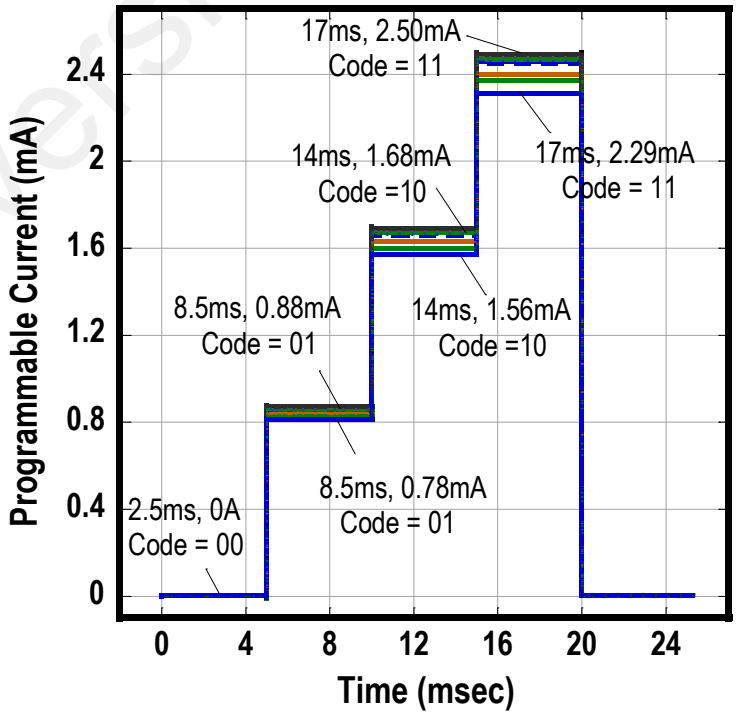

Figure 4.8 Programmable current post-layout switching across Monte-Carlo

For lowest frequency band the digital inputs are set to 2'b00, which means that no current contribution from the I_{prog}. Switching digital inputs to 2'b01 will set the I_{prog} to ≅ 0.85mA, which results in a shift to higher frequency band. In the same manner digital inputs can be changed to 2'b01 (I_{prog}≅1.65mA) and 2'b11 (I_{prog}≅2.4mA) to select even higher frequency bands.

4.4 Voltage Controlled Oscillator (VCO) performance

The VCO is simulated along with the integrated circuitry (bandgap and programmable currents). This helps to evaluate the VCO performance in terms of its tuning range and phase noise. The VCO's post-layout tuning range can be observed in Figure 4.9, with an overall frequency tuning range of 68.5% to cover the frequencies between 2.20 to 4.21 GHz. It can be observed that through the programmable currents the tuning curve is switched from one to another.

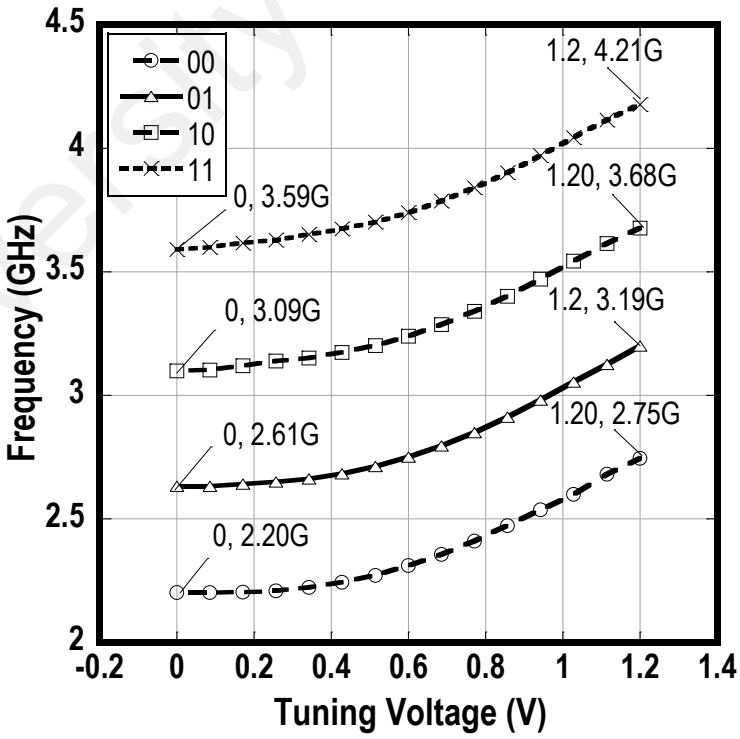

Figure 4.9 Simulated VCO post-layout frequency vs. tuning voltage

With the digital input of 2'b00 (I_{prog} = 0A), the VCO will adopt the lowest frequency band covering from 2.20-to-2.75 GHz. Switching digital inputs to 2'b01 (I_{prog}≅0.85mA) will switch the frequency to higher frequency band (2.61-to-3.19 GHz). The frequency bands can further be switched to even higher frequency by changing the digital inputs to 2'b10 (I_{prog}≅1.65mA) and 2'b11 (I_{prog}≅2.64mA) to select the higher frequency bands of 3.09-to-3.68 GHz and 3.59-to-4.21 GHz. On each of the frequency band the frequency can be set to specific value by varying the tuning voltage (V_{cntrl}).

The simulated VCO post-layout tuning range is shown in Figure 4.9 encapsulates a frequency range of 2.20 to 4.21 GHz. Dividing the single tuning curve into multiple curves helps to reduce the K_{VCO} to approximately 650 MHz/V. Whereas each tuning curve is exhibiting an average bandwidth of 570 MHz. In addition, each curve shows a symmetrical behaviour, which helps to set a fix VCO gain across whole tuning range.

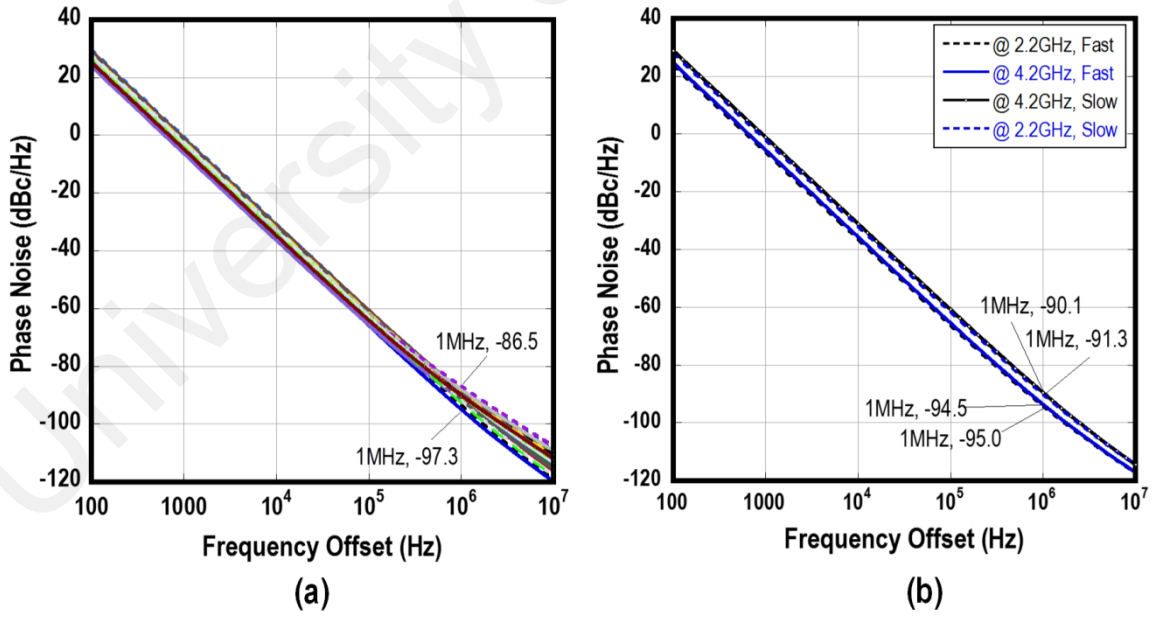

Figure 4.10 (a) Post-layout Phase Noise across MC at max frequency (b) Post-layout Phase Noise across process corners

The VCO post-layout is also simulated across both Monte-carlo and process corners to analyse the phase noise performance that can be seen in Figure 4.10. Figure 4.10 (a)

shows the phase noise results across MC for worst case (highest frequency). In addition, corner simulation at extreme tuning frequency ranges can be seen in Figure 4.10 (b). At fast corner the VCO exhibits a phase noise of -95.0 and -94.5 dBc/Hz at the output frequency of 2.2 and 4.2 GHz from an offset of 1MHz. The phase noise is degraded by ≅4dB at the slow process corner. At the slow corner, the phase noise is changed to -91.3 and -90.1 at the output frequency of 2.2 and 4.2 GHz at an offset of 1MHz.

4.5 Summary

In this chapter detailed simulations analyses have been presented for each VCO block. Different simulations have been performed across process and mismatch along with supply and temperature variations to evaluate the overall design. Below are some points to describe the overall summary.

- Bandgap shows a stable behavior across both process and Monte-Carlo at different supply ramps. This ensures that the implemented design will achieve the required reference voltage on silicon during lab testing.
- Programmable current generator is simulated at different input codes to make sure that it will provide the required current for the VCO. Programming current can be increased with an increment of approximately 0.85mA.
- VCO behavior is simulated by the injection of the programmable current. It is observed that the VCO is achieves a wider bandwidth of 2.20 to 4.21 GHz. In assistance of the programmable currents, the whole bandwidth is divided into multiple curves that help to reduce the VCO gain to 650 MHz/V.
- VCO phase noise shows a reliable performance even at higher oscillation frequency due to reduction in the VCO gain.

CHAPTER 5: SILICON LAB MEASUREMENT AND RESULTS COMPARISON

5.1 Introduction

In this chapter the silicon characterization details are presented after the fabrication of proposed VCO design. The results are compared between actual lab measurement of post-layout simulation results and previous literature state-of-the-art recent wok.

5.2 Test Structure

In order to characterize the implemented VCO performance, the design is physically fabricated on silicon. The objective was to characterize and evaluate the VCO performance parameters in real time at the laboratory environment.

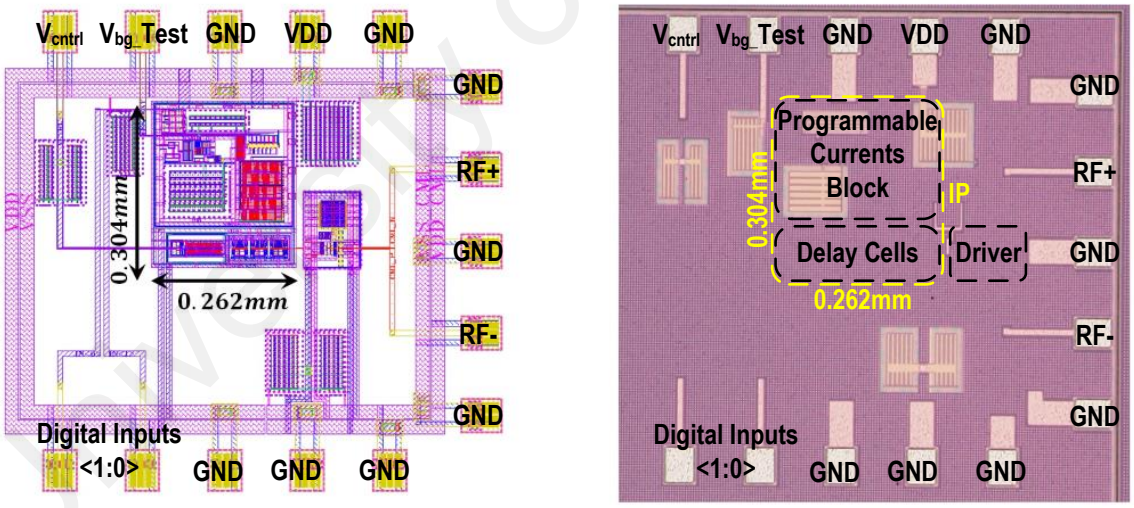

Figure 5.1 VCO layout and silicon Micrograph

Figure 5.1 shows the implemented VCO layout of a test structure along with its micrograph image of silicon wafer. The VCO itself consumes an area of $0.304 \times 0.262 mm^2$. The test pins definition can be seen in Table 5.1.

Table 5.1: Silicon Pin Description

Pin Name	Type	Description
VDD	Supply	1.2V DC Supply
GND	Ground	0V
Digital_in_0	Digital (Input)	1.2V or Ground to control Programmable Currents
Digital_in_1	Digital (Input)	1.2V or Ground to control Programmable Currents
V_{bg}_Test	Analog (Input)	Bandgap test pin
V_{ctrl}	Analog (Input)	0 to 1.2V variable supply to tune VCO
RF+	Analog (Output)	VCO high frequency positive output
RF-	Analog (Output)	VCO high frequency negative output

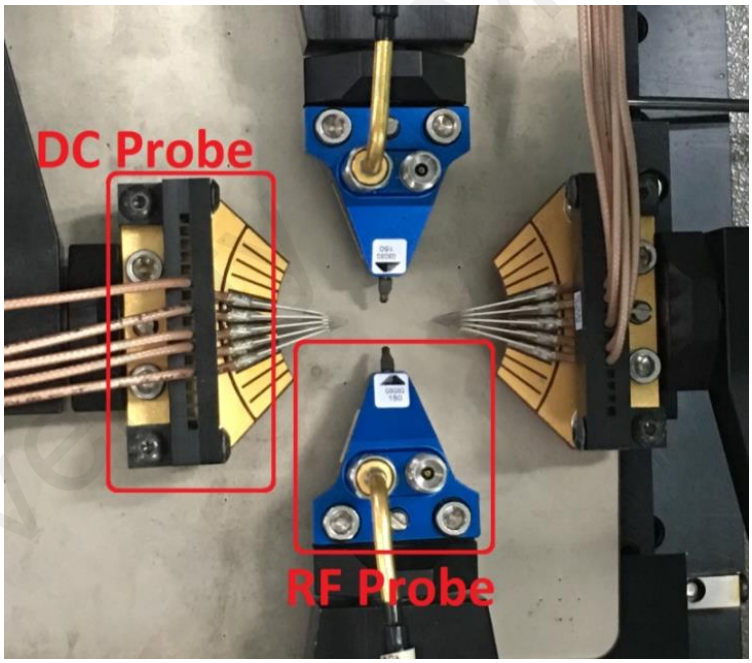

Figure 5.2 Silicon Measurement Probes

Figure 5.2 shows the test platform that is used to analyse the silicon in lab environment. In order to extract the signals from the wafer, high precision RF (Air Coplanar Family by Cascade Microtech) and DC probes (DC probes with 5 tips by Cascade Microtech) are used.

Each probe is landed on the exact location with the use of a microscope. Figure 5.3 shows the physical silicon under the test probes. It can be seen that two DC probes (five pins each) are used to provide the DC supply along with other VCO control signals. Additionally, one RF probes is used to measure the VCO output frequency. Both DC and RF probes at the other ends are connected to the test equipment by using the BNC connectors on the test structure.

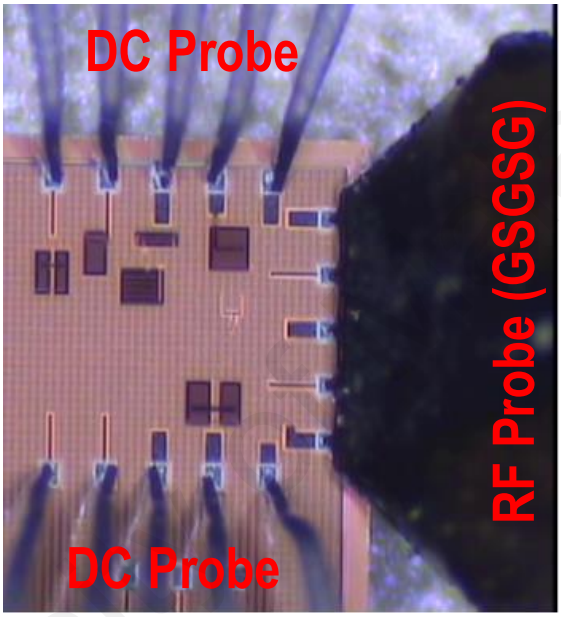

Figure 5.3 VCO Micrograph with measurement probes

5.3 Lab Tests

To analyse the output frequency from the VCO, integration equipment are used to bridge the compatibility between the VCO output level and measurement equipment. The signal source analyzer and spectrum analyzer accepts single ended inputs. In Figure 5.4, it can be seen that a Balun filter (HL9402 Broadband 20GHz) is added at the output of differential outputs (RF+ and RF-). Balun filter in general is used to convert the balanced signal (differential) to an unbalanced output (single-ended).

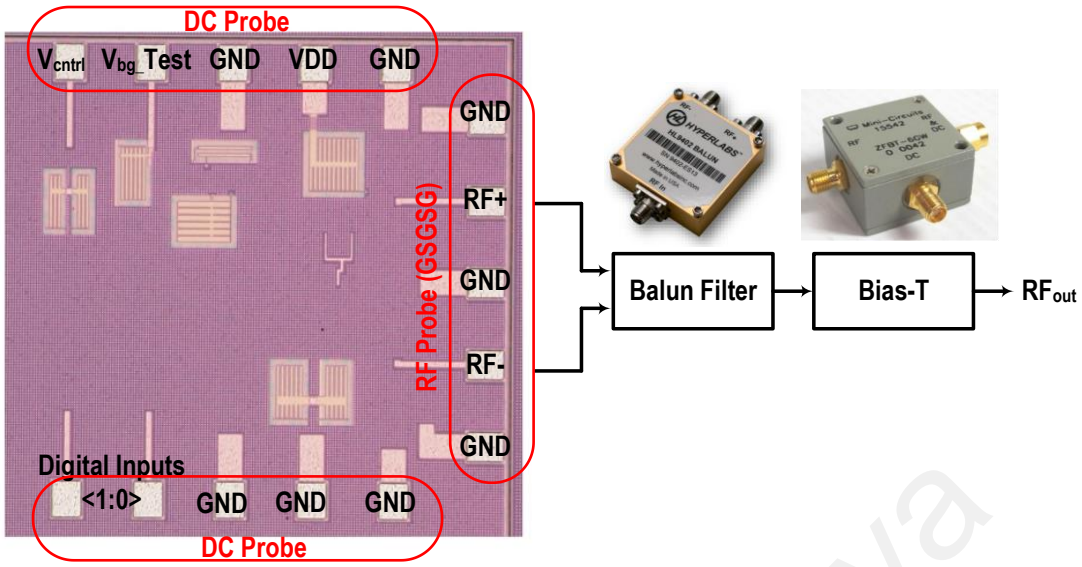

Figure 5.4 Measurement Setup

The single-ended output from the Balun filter contains a certain DC level from output stage of the designed VCO. The DC level may not fall under the acceptable input voltage range of the measuring equipment (e.g. Signal source analyzer and spectrum analyzer). Therefore, AC-coupling is required at the output of the Balun filter to block the DC contents from the VCO output stage. AC-coupling is typically done by adding a series capacitor that blocks the DC, while allowing the AC signal to pass-through. In order to meet this purpose, a Bias-T (Mini Circuits ZFBT-6GW, wideband 6GHz) is added to block the DC contents. This output from Bias-T is measured by aforementioned equipment for testing the VCO performance.

VCO on silicon is mainly characterized to characterize the output frequency range, phase noise performance and power consumption. All silicon measurement results are described in the following sections.

5.3.1 VCO Output Frequency Spectrum

In order to estimate the VCO output frequency range, spectrum analyzer (Agilent E4440A PSA) is used to measure the VCO output spectrum. Different silicon samples

have been tested to verify the output frequency. According to the measurement results, the proposed VCO exhibits a minimum and maximum frequency of 2.05 GHz to 4.19 GHz respectively.

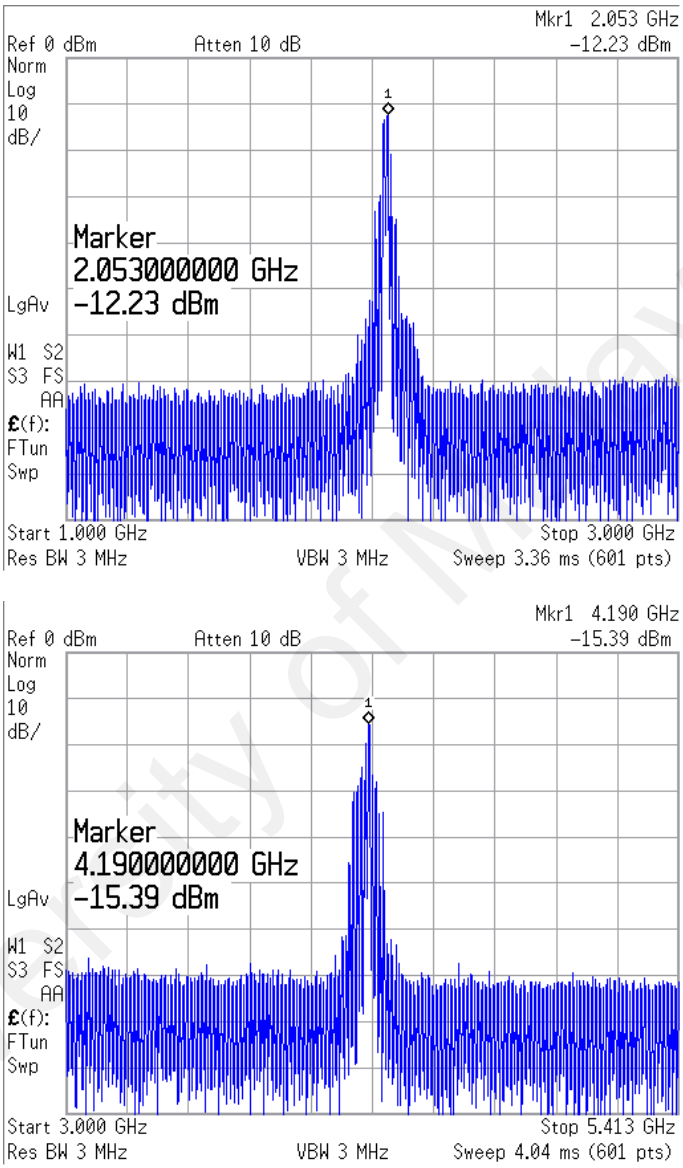

Figure 5.5 Measured output spectrum at the minimum and maximum frequency

Note that in Figure 5.5, the programmable current inputs for minimum operating frequency are set to 00 with V_{cntrl} = 0V, whereas programmable current for the maximum frequency are set to 11 with V_{cntrl} = 1.2V. Measurement results confirm an

excellent matching with the simulated results and both simulation and silicon results are observing similar frequency outputs with a wider tuning range of approximately 68.5%.

5.3.2 VCO Phase Noise Measurement

The VCO phase noise performance on silicon is measured through the use of Signal Source Analyzer (Agilent E5052A). AC-coupled output from the Bias-T is measured by the Signal Source Analyzer. The VCO shows a stable phase noise performance across different samples.

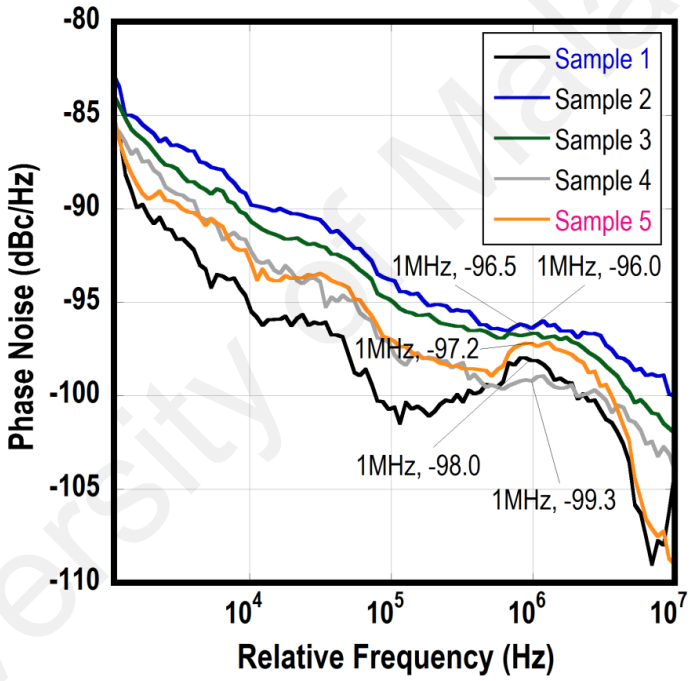

Figure 5.6 Phase noise from different tested samples at highest oscillation frequency

The phase noise performance for the proposed VCO from different wafers is illustrated in Figure 5.6. At the highest oscillation frequency, the VCO attains a minimum and maximum phase noise of -96.0 dBc/Hz and -99.3 dBc/Hz at 1 MHz offset frequency. The silicon measured phase noise result confirms similar behaviour to the simulations results obtained from both Monte-Carlo and corner simulations.

5.3.3 Current Consumption

Current consumption is measured for the silicon at different oscillation frequencies. It includes the current consumption of VCO along with programming currents of the bandgap. Figure 5.7 shows a comparison between measurement and simulated results. It can be observed that at different VCO oscillation frequencies, silicon measurement results are tracking as with the simulation results.

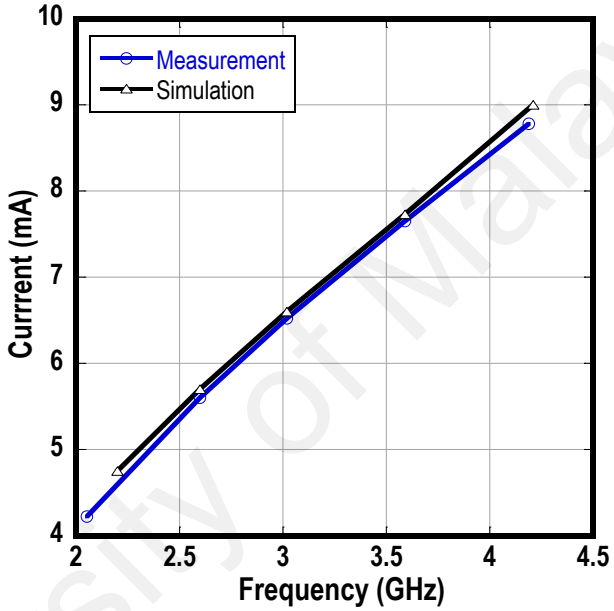

Figure 5.7 Current consumption comparison between measurement and simulated results

5.3.4 Figure-of-merit

Another important parameter of comparison is the VCO's Figure-of-Merit (FOM) and its frequency tuning range. The designed VCO is evaluated by the figure of merit defined as (To-Po & Shih-Yu, 2015):

$$FOM = L\{\Delta f\} - 20log\left(\frac{f_{out}}{\Delta f}\right) + 10log\left(\frac{P_{DC}}{1mW}\right) \quad (5.1)$$

$$FOM_T = FOM - 20log\left(\frac{FTR(\%)}{10}\right) \quad (5.2)$$

where L{Δf} is the phase noise at the offset frequency is Δf, P_{DC} is the DC power consumption and FTR (%) is the total frequency tuning range. Out of all measured samples (Figure 5.8), the proposed architecture achieves a maximum FOM and FOMT of -161.4 dBc/Hz and -178.1 dBc/Hz respectively.

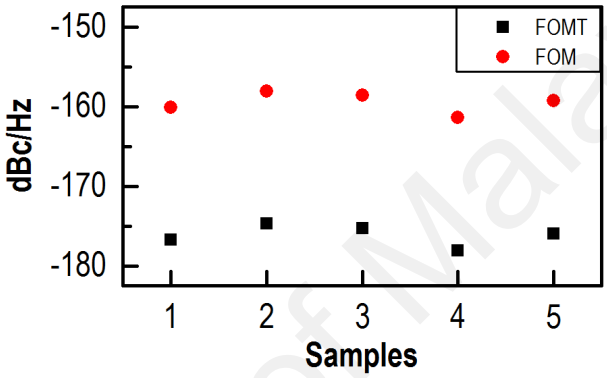

Figure 5.8 Tested samples Figure-of-Merit

5.4 Results Comparison

Table 5.2: Performance comparison with other similar works

Reference	**(Zuow-Zun & Tai-Cheng, 2011)**	**(Xu, Stadius, Ryynanen, & Ieee, 2010)**	**(Kim, Kim, Lee, Han, & Lee, 2013)**	**(Tsitouras & Plessas, 2011)**	**This Work**
Frequency (GHz)	1.77-1.92	2.65– 6.30	0.48-1.01	3.10-4.80	2.05–4.19
Tuning range (%)	8.1	81.5	70.0	43.0	68.5
Phase noise (dBc/Hz) @ Foffset/Fcarrier	-102 @ 1M /1.9G	-85.0 @ 1M /6.3G	-110.8 @ 1M /645M	-76.7 @ 1M/3.1G	-99.3* @ 1M /4.1G
FOMT (dBc/Hz)	-154	-167	-173	-154	-178.1*

Table 5.2, continued

Reference	**(Zuow-Zun & Tai-Cheng, 2011)**	**(Xu et al., 2010)**	**(Kim et al., 2013)**	**(Tsitouras & Plessas, 2011)**	**This Work**
Power (mW)	13	16	10	7.2	10.6*
Supply (V)	1.8	1.2	1.0	1.0	1.2

* at maximum frequency

CHAPTER 6: CONCLUSION

6.1 Overall Conclusion

In this research work, a multiple tuning-curves based wideband RC VCO architecture has been reported. The VCO tuning range is distributed into multiple tuning-curves. A programmable current has been used to introduce the bottom-up topology in which the VCO tuning curves can be shifted from lower to higher one. This helps to achieve a wider bandwidth from a low voltage design of only 1.2V. The proposed design is able to achieve an overall bandwidth of 2.05-4.19 GHz along with a lower VCO gain (K_{VCO}) of only 650 MHz/V across whole frequency range. Due to reduction in K_{VCO}, the VCO phase noise is improved to achieve -99.3 dBc/Hz at the highest oscillation frequency. The overall architecture is distributed into different blocks comprising of bandgap, programmable current and dual-delay based RC VCO. In order to provide sustainable programming currents, a current based bandgap is introduced to provide a stable reference voltage of 0.6V. Output from the bandgap is used to generate the programming currents. The programmable current block is digitally controlled to switch from lower or higher current values. Output from the programmable current is fed into a dual-delay based VCO architecture that has been used to achieve a wider bandwidth along with better phase noise performance.

The proposed architecture individual blocks performance has been evaluated across process and mismatch with a supply variation of 1.2V±10% in the temperature range of -40 to +80℃. The overall design is finally simulated together to measure the VCO tuning-range, phase noise and power consumption. In order to further evaluate, the VCO layout is realized and later fabricated in 130nm CMOS platform to fully characterize the performance. The design consumes an overall area of 0.304x0.262mm$^{2.}$ It is observed that different silicon samples are showing a similar behaviour in addition

to exact match with simulation results. Therefore, having achieved stable silicon behaviour along with a lower on-chip area, this research work can be used for commercial applications like PLL or Frequency synthesizers integration, where there's need for a wider bandwidth and a lower VCO gain operating at lower supply voltage.

6.2 Future Work

A possible future application of this work is to integrate it into a GHz PLL or synthesizer IC as a wideband clock reference. The proposed design has the ability to increase the tuning range by slightly increasing the programmable currents. In this case, future work can be done on the programmable currents to optimize the performance in terms of stability to support higher current values. For higher oscillation applications the layout can be further optimized in order to reduce the parasitic, separation between high speed blocks, and shifting high frequency traces to further upper metal. Moreover, delay cell can be optimized by investigating the devices sizes that can affect the phase noise performance along with tuning ability due to frequency limitation. Taking all of these points into consideration, overall performance for the proposed VCO can be also improved.

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LIST OF PUBLICATIONS

ISI-Cited Journal Papers:

a) **Muhammad Awais**, Harikrishnan Ramiah, Chee-Cheow Lim, Joon-Huang Chuah, "A 0.079 mm^2 2.1-to-4.2 GHz Ring-VCO Employing Programmable Current Topology,".

* Paper accepted in Microelectronic International

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1. **M. Awais**, H. Ramiah and J. H. Chuah, "A Wide Tuning Range, Low Voltage CMOS Ring Oscillator," 8^{th} AUN/SEED-Net Regional Conference in Electrical and Electronics Engineering (RCEEE), Metro Manila, Philippines, 16^{th} – 17^{th} November 2015.