EFFICIENCY ENHANCEMENT OF DISTRIBUTED POWER AMPLIFIER DESIGN FOR RADIO FREQUENCY COMMUNICATION SYSTEMS

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ABSTRACT

In the field of radio frequency (RF) and microwave communication system, there is an endless demand on wideband frequency operation and the amount of research work in the area of Power Amplifiers (PA) has grown as well to solve all kinds of problems. For instance, wireless portable devices have become common used in our daily life, but we often face the problem of its battery drains easily. Hence, a good design of PA can play an important role to satisfy all sorts of stringent needs. This research presents two designs of broadband distributed power amplifiers (DPAs) with different approaches. The first DPA designed using Pseudomorphic (PM) and Gallium Nitride (Xie) based with high-electron-mobility transistor (HEMT) technology as the power devices with the novel integration of broadband impedance transformer at the drain line termination. Besides, it demonstrated significant good performance over the entire bandwidth from 100 MHz to 2.4 GHz with 10 W output power performances and reaches average 35% of efficiency in 30 dB flat gains across bandwidth measured. On the other hand, the second DPA design driven by 3-stage of 10 W GaN HEMT with the gate line adjustment network and drain line tapering implementation for overall efficiency enhancement. Experimental of the prototype demonstrated output power of 41 dBm, flat gain at 12 dB, and bandwidth covering 80 MHz to 2.0 GHz with power added efficiency (PAE) 45% under 28 V drain bias. These concepts were implemented and developed in Advanced Design System (ADS) to obtain simulations and ideal performance. The research contribution has delivered bandwidth-efficiency improvements on the conventional distributed amplifier (DA) topology, battery life extension, and lower cost that is compatible with two-way radios communication applications such as Software Defined Radio (SDR). After all, this study offers practical skills and industrial realization in RF and microwave communications systems.

ABSTRAK

Dalam bidang frekuensi radio dan sistem komunikasi gelombang mikro, terdapat permintaan mengenai operasi frekuensi jalur lebar dan banyak penyelidikan dalam bidang Penguat Kuasa telah berkembang untuk menyelesaikan semua jenis masalah ini. Sebagai contoh, peranti mudah alih tanpa wayar telah menjadi kegunaan biasa dalam kehidupan seharian kita, tetapi kita sering menghadapi masalah kehabisan bateri yang mudah pada peranti tersebut. Oleh itu, reka bentuk Penguat Kuasa yang baik memainkan peranan yang penting untuk memenuhi pelbagai keperluan yang mencabar ini. Kajian ini membentangkan dua reka bentuk Penguat Kuasa jalur lebar diedarkan dengan cara yang berbeza. Bagi reka bentuk pertama, peranti kuasa Pseudomorphic (PM) dan Gallium Nitride (Xie) dengan high-electron-mbility trasistor (HEMT) teknologi telah digunakan dengan integrasi pengubalan hasil terjemahan di talian saliran akhir. Kajian ini menunjukkan prestasi yang baik ke atas lebar jalur 100 MHz hingga 2.4 GHz dengan kuasa keluaran 10 W dan mencapai purata 35% kecekapan dalam gain 30 dB merentas lebar jalur yang diukur. Selain itu, reka bentuk kedua didorong oleh tiga peringkat 10 W GaN HEMT dengan gerbang talian rangkaian pelarasan dan talian saliran tirus pelaksanaan untuk meningkatkan kecekapan seluruh sistem. Daripada kajian prototaip tersebut telah mencapai kuasa keluaran 41 dBm, gain pada 12 dB dan jalur lebar meliputi 80 MHz hingga 2.0 GHz dengan pencapaian kuasa 45% kecekapan yang setinggi mungkin. Konsep yang dicadangkan akan dibuat pengesahan uji kaji dengan simulasi dalam perisian Advanced Sistem Design. Sebagai sumbangan penyelidikan ini, kemajuan kecekapan lebar jalur telah dilakukan dan melebihi kecekapan penguat diedarkan yang konvensional, mempunyai lanjutan hayat bateri, dan kos rendah yang sesuai untuk aplikasi komunikasi radio seperti Radio Ditetapkan Perisian (SDR). Sebagai kesimpulanya, semua kajian ini menawarkan kemahiran praktikal dan kesedaran industri dalam sistem frekuensi radio dan komunikasi gelombang mikro.

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LIST OF ACRONYMS AND SYMBOLS

Acronyms:

AC	:	Alternating Current
ACPR	:	Adjacent Channel Power Ratio
ADS	:	Advanced Design System
CAD	:	Computer-Aided Design
DA	:	Distributed Amplifier
DC	:	Direct Current
DPA	:	Distributed Power Amplifier
EM	:	Electromagnetic
FET	:	Field Effect Transistor
GaAs	:	Gallium Arsenide
GaN	:	Gallium Nitride
HB	:	Harmonic Balance
HEMT	:	High Electron Mobility Transistor
LNA	:	Low Noise Amplifier
MESFET	:	Metal Semiconductor Field Effect Transistor
MMIC	:	Monolithic Microwave Integrated Circuit
PA	:	Power Amplifier
PAE	:	Power Added Efficiency, %
PCB	:	Printed Circuit Board
pHEMT	:	Pseudomorphic High Electron Mobility Transistor
PM	:	Pseudomorphic
RF	:	Radio Frequency
RFT	:	Real Frequency Technique

SRF	:	Self-Resonant Frequency
SDR	:	Software Defined Radio
TPG	:	Transducer Power Gain
UHF	:	Ultra High Frequency
VCCS	:	Voltage Controlled Current Source
VHF	:	Very High Frequency

Symbols:

A	:	Amperes
BW	:	Bandwidth
C	:	Capacitance
C_{ds}	:	Drain to source capacitance
C_{gd}	:	Gate to drain capacitance
C_{gs}	:	Gate to source capacitance
dB	:	Decibels
dBm	:	Decibels (reference to 1mW)
ε_r	:	Dielectric constant of substrate
F	:	Farads
f_c	:	Center frequency
f_o	:	Cutoff frequency
Θ_d	:	Drain line propagation delay, *ns*
G	:	Conductance
g_m	:	Transconductance, $\mho$
Hz	:	Hertz
I	:	Current, A

I_d	:	Drain current
I_{ds}	:	Drain to source current
I_{gs}	:	Gate to source current
L	:	Inductance, H
n_{opt}	:	Optimum number of section
P	:	Power
P_{out}	:	Output power, W
R	:	Resistance, Ω
RF_{in}	:	RF input
RF_{out}	:	RF output
V_{ds}	:	Drain to source voltage
V_{gs}	:	Gate to source voltage
V_{bk}	:	Breakdown voltage
V_{in}	:	Input voltage
V_k	:	Knee voltage
V_{out}	:	Output voltage
W	:	Watts
Z_L	:	Load impedance
$Z_{L,opt}$	:	Optimum load impedance
Y	:	Admittance, $\mho$
Z	:	Impedance, Ω
Z_{OT}	:	Characteristic impedance of T-section network
$Z_{O\pi}$	:	Characteristic impedance of π-section network
$Z_{u(k)}$		Impedance seen by current source in upper direction
$Z_{r(k)}$	:	Impedance seen by current source in right direction
Ω	:	Ohm

CHAPTER 1: INTRODUCTION

1.1 Research Background

There is a significant growth of the development in microwave amplifiers of radio frequency communication systems. Consequently, the demand for wider bandwidth amplifiers is drastically increasing from advanced radio equipment to deliver ever wider frequency range while maintaining stringent requirements on other design specifications such as cost, die-size and power performance. Thus, a lot of efforts spent on the theme of PA research. A new proposed of broadband high-power DA circuit topology and method to extend bandwidth and efficiency enhancement is presented in comparison to conventional DPA. A DPA is an amplifier in which a signal is amplified in parallel by a number of transconductive devices such as vacuum tubes or transistors. In this thesis, there are two designs of DPA.

For the first design, a novel integration technique of broadband impedance transformer using pHEMT and GaN HEMT is performed. By identifying the DPA's optimum impedance over the frequency range from load pull measurement technique, the impedance transformer with mixed-lumped elements via Real-Frequency Technique is designed. This proposed technique is essential to maximize DC-RF conversion to the load termination and the transformer is having advantages over size area, implementation in small form factor and low-cost approach particularly compatible for radio communications applications.

For the second design, the DPA design has involved in a control mechanism to enhance the efficiency performance by tuning the impedance at the gate termination adjustment network and applying drain line tapering topology. This 3-stage DPA system is only based on a GaN HEMT as the power device. As a result, this work has

demonstrated significant improvement in efficiency over the conventional DPA and offers wideband operation especially for communication systems of public safety agency applications.

These design and implementations made by using ADS software to run all the simulations and analysis based on the large signal model transistor design kit acquired from Cree. Moreover, OrCAD software used to design PCB layout of hardware development and several measurements carried out in Motorola Solutions laboratory in UM to test and validate the prototype of this high power and high efficiency performance power amplifier.

1.2 Problem Statement

In recent years, there is a high demand for wideband frequency operation, all kinds of PA design techniques have been proposed in research area. PA is the key component establishing the communication systems of future generation. It requires broad frequency to support high data rate and works in multiband operation within VHF and UHF up to 3 GHz. However, the conventional PA often suffers from less reliability, weak efficiency that affects power consumption especially in power amplifier class operation for class A and Class AB, bandwidth limitation and costly in manufacturing (Aridas, Yarman, & Chacko, 2014). Besides, a disadvantage often attributed to the DPA, when compared to other amplifier topologies due to its high-power consumption (Olson, Thompson, & Stengel, 2007). While part of this high-power images stems from the fact that DPA is typically optimized for maximum gain and bandwidth, automatically leading to a high-power consumption, it is true that the topology has some characteristics that limit its efficiency (Kim, Greene, & Osmus, 2014). For instance, in its basic configuration, half of the output current generated by the transistors is essentially lost. For these reasons, the

DPA is often quickly dismissed as use of low-power broadband applications such as wireless receivers.

Hence, designing a good PA that is high efficiency become contradicting requirements for the PA in radio communication systems. Where this work focuses on the efficiency enhancement of the DPA to alleviate the power consumption problems.

1.3 Research Aims

In this research work, the aim is to design a high power amplifier with distribution technique and achieve the efficiency enhancement over the conventional circuit architecture topology. The propose technique is design with GaN HEMT transistors to develop a power amplifier with output power up to 10 W and to achieve wide bandwidth up to 2.4 GHz for two-way radio applications. The final prototypes will be characterized by measurements to observe the power performances.

1.4 Research Objectives

The key of this work is to enhance the efficiency of the designated distributed power amplifier. Therefore, this study embarks on the following objectives:

1. Design of a high output power and good efficiency performance DPA with proper device selection such as Gallium Nitride based with HEMT technology.
2. To investigate and develop new technique of DPA operation bandwidth covering 100 MHz to 2.4 GHz in comparison to conventional topology.
3. To fabricate the prototype board based on industrial requirements by means of technical specifications.

1.5 Organization of Dissertation

This dissertation is framed into six chapters as follows:

Chapter 1 gives an overview, problem statement and objectives of this research.

Chapter 2 provides a history of PA designs and literature review on conventional broadband amplification design techniques to recent research contributions in communication system are covered in this chapter. The fundamental theoretical analysis on PA designs, S-parameters, classes of PA operations and GaN HEMT technology are introduced in this chapter as well.

Chapter 3 describes the flow of designing and developing DPAs by using GaN HEMT. This includes the procedure RFT employment for matching network and lumped element to distributed element conversion are presented in details. Moreover, the development of DPA prototype and details of mounting fixture are explained in here.

Chapter 4 proposes first DPA design of this thesis work with the novel integration technique of broadband impedance transformer using pHEMT and GaN HEMT. Determination of the optimum impedance and impedance transformer design principle is introduced. This design has performed good results of high output power and efficiency up to 2.4 GHz has well demonstrated with simulation and measurement results validation.

Chapter 5 discusses on the second DPA design performance employing gate line termination adjustment and tapered drain line approaches has discussed in this chapter. The conventional topology and limitation efficiency has reviewed. Lastly, the new DPA simulation and measurement results made comparison and findings throughout the design process. This design has given a good agreement on efficiency enhancement.

Finally, **Chapter 6** represents the conclusion of this thesis work, contributions and design challenges are discussed. The advance improvements are highlighted at the end of this chapter.

CHAPTER 2: LITERATURE REVIEW

2.1 History of Distributed Amplifiers

The DA is an unconventional technique that allows an amplifier designer to escape the tradeoff between gain and bandwidth. With conventional amplifiers, designer has to cascade stages, because the gain of one stage is not enough, meanwhile several stages are connected to form a transmission lines with gain effect. The gain is the sum of the gains of the stages, whereas the bandwidth of a DA is the bandwidth of each of the stages. Referring to William S. Percival who formulated the DA design as shown in Figure 2.1, the amplifier's bandwidth is primarily set by the capacitance and transconductance of the valve used, thus arriving at a circuit that achieved a gain-bandwidth product greater than that of an individual vacuum tube.

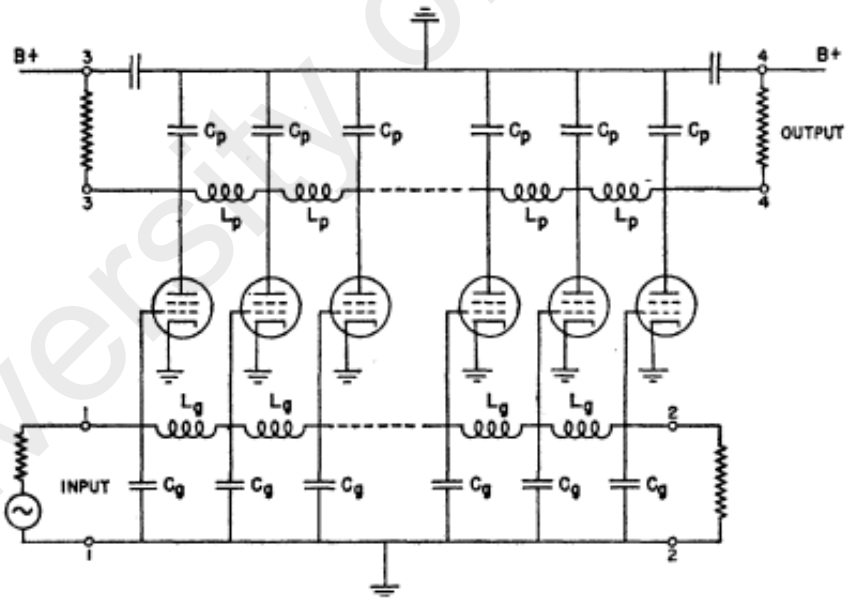


Figure 2.1: Basic structure of the DA(Percival, 1936).

Further on, the theory of DA was proved to be very useful in obtaining wider bandwidth as explained by (E. L. Ginzton, 1948), they implemented the concept of video frequencies and first published with the term of *distributed amplifier* has gained widespread awareness. In short, this DA achieved by absorbing the capacitance in an

artificial transmission line, DA becomes a broadband amplifier. Since one of the main constraints on broadband amplification is eliminated, bandwidth of the amplifier is limited only to the band of the artificial transmission line. The outlook of the first DA is as shown in Figure 2.2, where the amplifying tubes were type 807 which is the small transmitting beam-power tetrode. This DPA tube has performed a nominal gain of 11 dB with a 3 dB bandwidth of 100 KHz to 30 MHz, with the output power of 15 watts at 100 KHz.

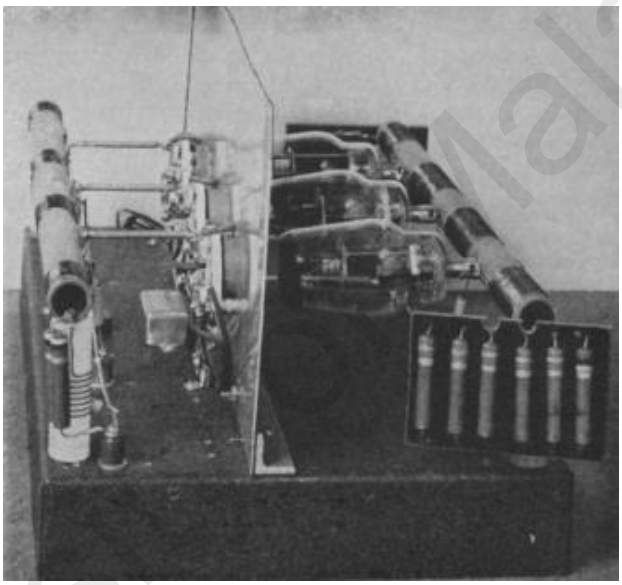


Figure 2.2: Conventional DPA tube by Copson (1950).

In the following years, the development of microwave DA has emerged from the advent of the GaAs MESFET (Niclas, Wilser, Kritzer, & Pereira, 1983). This concept was based on the idea to separate the inter electrode capacitances of the active components by means of artificial transmission lines, while adding their transconductances. Eventually a much wider bandwidth of amplification was obtained as compared to the conventional amplification systems. Besides, a monolithic GaAs MESFET amplifier were applied in pursuit of larger gain-bandwidth products (Ayasli, Mozzi, Vorhaus, Reynolds, & Pucel, 1982). Ayasli et al. showed the design formulas for gain of a traveling wave amplifier based on an approach that approximates gain and drain lines as continuous

structures. Meanwhile, (Beyer, Prasad, Becker, Nordman, & Hohenwarter) in 1984 developed a closed-form expression for gain that depend on the circuit's propagation constants and the gate circuit cutoff frequency.

After the advent of GaAs MESFET distributed amplifiers the next trend falls to the MMICs in the twentieth century. By using the non-uniform device peripheries to compensate for load line requirements of each cell position, a better result can be achieved. In Figure 2.3 shows the structure of non-uniform DPA and the non-uniform MMIC DPA (Duperrier, Campovecchio, Roussel, Lajugie, & Quere, 2001), as the impedances presented to the first cells are unrealizable and higher output power and efficiency is achievable by increasing the peripheries.

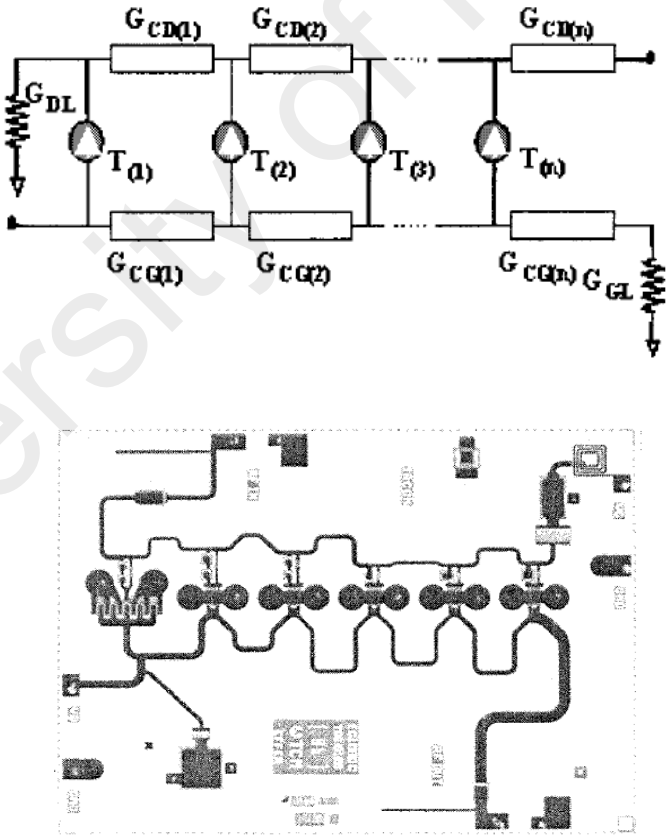


Figure 2.3: Structure of non-uniform (top) and MMIC DPA (bottom).

From this benchmark, it is based on analytical expressions of the optimum input and output artificial lines making up the non-uniform distributed architecture. In addition,

this MMIC amplifier has demonstrated 1 Watt output power with the gain of 7 dB at the minimum of 20% PAE over a multi octave frequency band. With MMIC implementation, the bandwidth can be achieved a very high frequency where in hybrid parasitics restrict the performance. GaAs is suitable due to its characteristics for monolithic fabrication. In monolithic to integrate circuit devices are mounted on single piece semiconductor material such as silicon. In addition, using specific process millions of devices are interconnected with this surface.

On the other hand, the prototype of this thesis work is produced by using hybrid method which requires very high quality substrates with active devices. The devices are interconnected with the use of bonding wires deposited on insulating substrate. For instance, hybrid circuit is coated into an epoxy material and then bonded with a dielectric substrate. The devices are made of semiconductor material such as Si, GaAs, InP. For the case of monolithic integrated circuit, all the components are formed together by various methods which include diffusion or ion implantation. While in the case of hybrid integrated circuits, interconnections are usually established by TEM mode transmission lines like microstrip lines of this research work.

Nowadays, the latest benchmarks of the DA development are the used of GaN HEMT technology, the introduction to field-plate technique to GaN HEMTs resulted in much higher breakdown voltage, higher band gaps, higher saturated electron velocity, and higher-resistivity substrates (Komiak, 2015). There are numbers of DPA design with GaN HEMT active device implementation, which provides a higher power levels over wider frequency range compared with conventional DPA uses lower power amplification and other device such as HBTs, PHEMT and MESFET. (Narendra et al., 2008) have demonstrated a 4-stage DPA with enhancement mode pHEMT technology experimentally and employing tapered drain loaded networks technique. As a result, this

DPA has achieved a high PAE of 30%, 10dB gain, low supply voltage of 4.5 V and power operation of 600mW at frequency range of 10-1800MHz. On the other hand, (Lin, Eron, & Fathy, 2009) has presented an ultra-wideband DPA using discrete GaN HEMTs that requires the utilization of large signal analysis in order to perform with high drain efficiency and output power. This paper has recommended capacitive division utilization at the gate lines and drain line tapering to improve the power performance that greater than 5 W and PAE over 27% in 20 MHz to 3 GHz wide operation bandwidth. This DPA prototype has been fabricated as shown in Figure 2.4 with hybrid PCB implementation on Rogers' RT5880 soft substrate, with a ½ oz copper cladding.

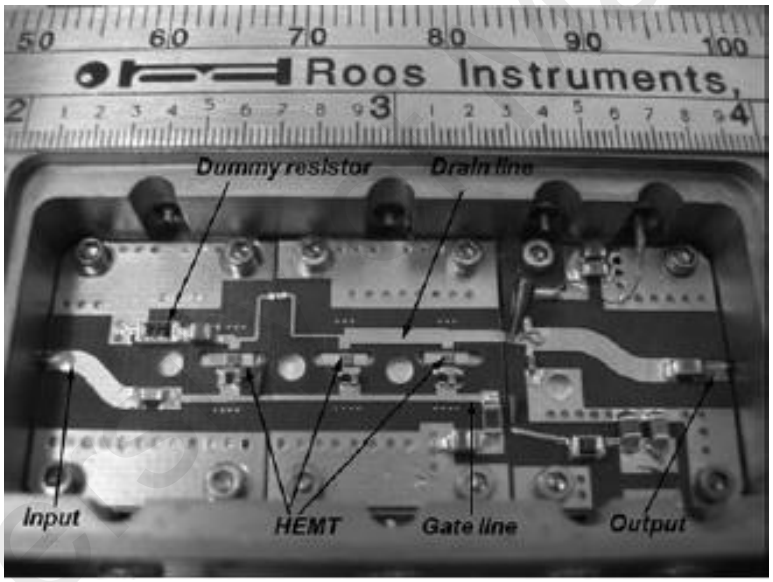


Figure 2.4: Hybrid DPA implementation with 3 -stage GaN HEMT devices.(Lin, Eron, et al., 2009)

There is several researches has shown good work for DPA design throughout the recent years has briefly summarize in Table 2.1. Nevertheless, the outcome of this thesis consists of two designs of DPA uses different techniques and device selection to investigate about the circuit architecture studies that brings better outcome in power performance. In further topic, the theory and properties of GaN HEMT will be discussed.

Table 2.1: Review of DPA performance levels.

References	Device	Fabrication	Gain [dB]	Bandwidth [MHz]	Pout [W]	PAE [%]
(Narendra et al., 2008)	LDMOS	Hybrid / Distributive	~24	10-2000	1.5	~27
(Lin, Fathy, & Eron, 2009)	GaN HEMT	Hybrid / Distributive	~11	20-3000	5	~27
(Xie, 2011)	GaN/Si HEMT	MMIC / Distributive	~10	100-2200	8.7	30-66
(Kim et al., 2014 2014)	GaN HEMT	Hybrid / Discrete	~12	100-2700	5	~40
(Andersson, 2015)	GaN HEMT	Hybrid / Distributive	7.3-12.7	900-2600	20	60-64
(Moon et al., 2016)	GaN HEMT	MMIC / Distributive	~10	100-8000	5	~35

2.1.1 Concept of Distributed Amplification

The operation of the DA can be explained by referring to Figure 2.5, where a RF signals applied to the input port of the gate line travels down the line of the termination where it is absorbed. The traveling signal is picked up by the gates of the individual transistor and transferred to the drain line of their equal transconductances, g_m. If the phase velocities on the gate and the drain lines are identical, the signals on the drain line add in the forward direction. The phase velocities between gate and drain lines can be synchronized simply by set the gate and drain line cutoff frequencies identical. Any signal which travels backward and is not entirely canceled by the out of phase additions will be absorbed by the drain line termination (Beyer et al., 1984).

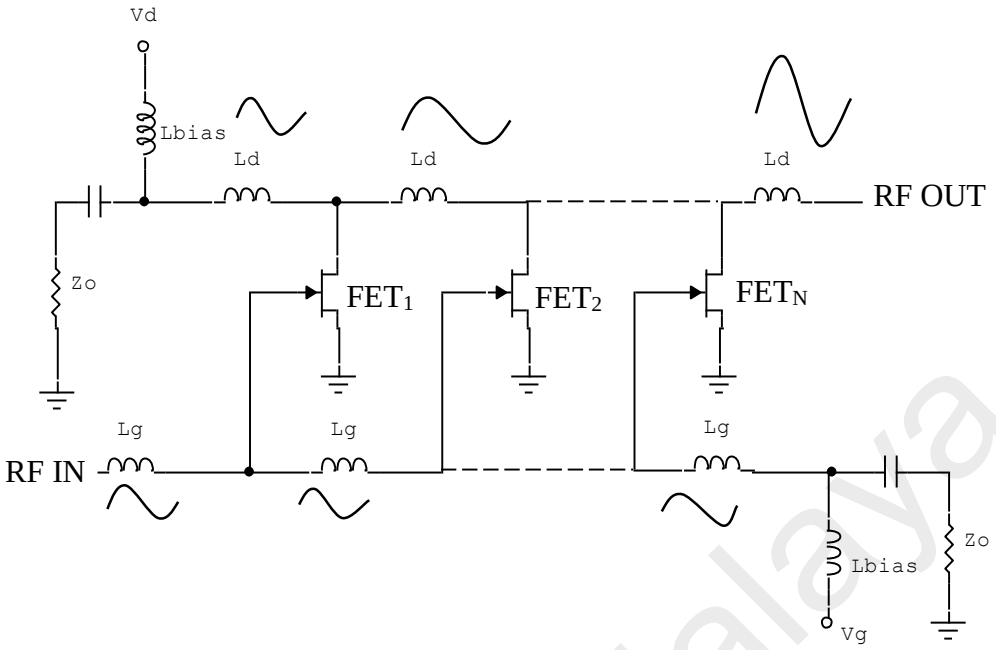


Figure 2.5: Concept of distributed amplification.

The concept of distributed amplification is based on combining the input and output capacitances of the actives device with inductors in such a way that two artificial transmission lines are obtained. The input and output capacitance of each device becomes the capacitance per unit sections for these lines (refer to Figure 2.5) and the lines are coupled by the g_m of the active device. As a result, it is possible to obtain amplification over a wider bandwidth than with conventional amplifiers. Designers have concentrated mainly on increasing the gain-bandwidth product and the gain flatness, as well as on output power capabilities.

In DA, the transmission structures employed are often analyzed as a cascade of two ports, as we will see in the following section. For the amplifiers employing transmission lines, the voltage developed along the output line tends to increase as the cutoff frequency is approached if the magnitudes of the current injected by active devices along the line remain constant.

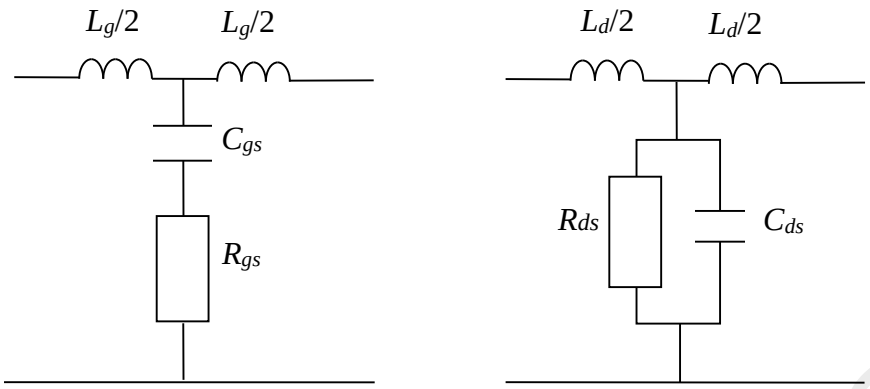
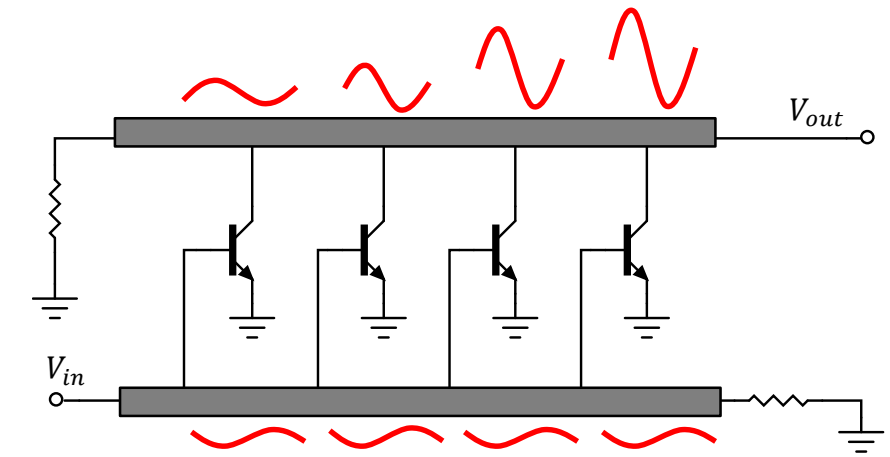


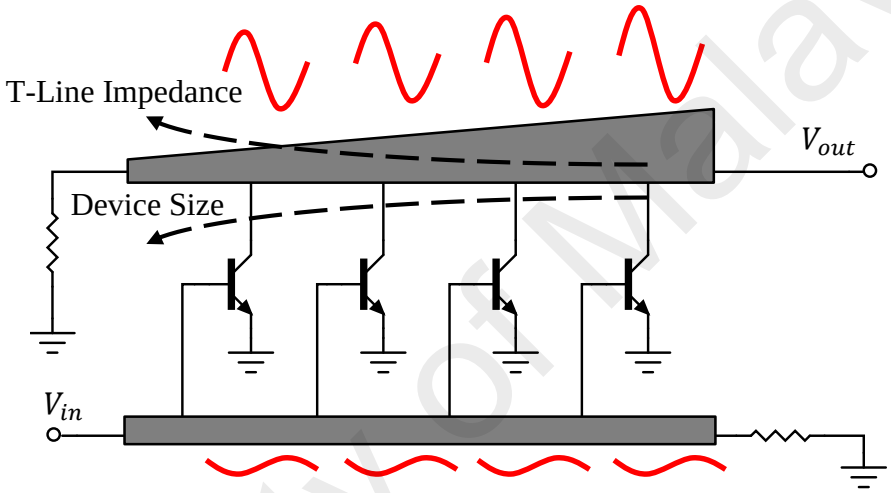
Figure 2.6: Lossless elementary section of DA, gate line (left), drain line (right).(Narendra & Grebennikov, 2015)

In a properly designed and constructed DA, the input signal passes by and is applied to the inputs of each of the stages, and is finally absorbed by a terminator, which has the characteristic impedance of the input transmission line of DA. In practice, there are several limits that apply to the DA technique. One of these is the real component of the input impedance of many amplifying devices. The real component necessarily causes energy loss in the transmission line, which limits the number of stages.

According to Chen and Niknejad (2011) the major deficiency of broadband power amplifier is their relative low efficiency. In a conventional DPA the largest voltage swings to occurs to the last stage as shown in Figure 2.7(a), and only the last stage experiences maximum allowed voltage swing when output power saturates. In Figure 2.7(b) depicted the stage-scaled structure of DA, where the preceding stages never approach maximum available voltage swings, hence, degrade the overall efficiency.



(a)



(b)

Figure 2.7: (a) Conventional DA with (b) stage-scaled DA. (Chen & Niknejad, 2011)

As a result, the output-line impedance needs to scale up from the last stage while the transistor size and bias current needs to scale down in the same direction.

2.1.2 Topologies for Broadband Amplification

In years' researchers have developed several ways to achieve broadband amplification. However, all of the topologies expanded bandwidth of operation in expense of either gain or design complexity. Some of the topologies are listed below:

- Compensating Matching Topology
- Feedback Amplifier
- Balanced Amplifier
- Distributed Amplifier (DA)

The DA topology is an attractive candidate for the SDR Transmitter applications (Narendra et al., 2008; Narendra et al., 2012; Narendra et al., 2010). In conventional DAs however, the current combining efficiency at the drain line is typically poor, due to current splitting on the drain line into two branches, forming two waves travelling one towards the load and the other toward the dummy terminations. The tapered drain line DA eliminates the drain line reverse wave adopting a suitable tapering of the drain line impedance (Olson et al., 2007). The DFDA topology, proposed in (Botterill & Aitchison, 1994), allows an efficient power combining with the load termination. Similar technique, by adding Lange couplers or Wilkinson combiners at the input and output of the DA to improve output power, gain and PAE, was demonstrated by (D'Agostino & Paoloni, 1994). A compact DFDA with single-ended termination was shown in (Eccleston, 2005) demonstrating a practical realization with meandered artificial transmission lines loaded with short-circuits stubs.

Therefore, in this research, a new design of distributed power amplifier based with GaN HEMT is proposed. Moreover, the remarkable bandwidth-efficiency improvements to the conventional DA were implemented. The proposed concept will be experimentally validating with the simulations and board fabrication done, to provide an output power of

more than 10 W over the frequency bandwidth of 2.4 GHz and the gain of 10 dB with a PAE over 40%. The concept requires a small size area and low cost, which is practical and compact implementation for RF and microwave communications.

2.1.3 Limitation on Broadband Amplification

The amplifier behaviour is very limited by the gain-bandwidth product for an active device, especially capacitance parameters. When the bandwidth is extended, the gain will be reduced; eventually cascade of amplifying stages becomes not effective as the gain reaching unity. Besides, as the outputs are combined from several shunt-connected power transistors, the resulting power-output is increases and causes no enhancement in the gain-bandwidth product. Therefore, the basic concept of distributed amplification is applied to design an arrangement in such a way that the currents from the output of several active devices are superimposed and does not accumulate the effects of input and output shunt capacitances.

DAs operation is well described as traveling-wave tube amplifiers patented by Percival in 1937. It consists of two transmission lines represented by series-inductive elements connecting with number of active devices at the input and output of adjacent gain stages, causes capacitances to be isolated, where the output currents are combining with an additive fashion. As a result, the interlaying series inductors and shunt capacitances at the gate and drain line, creates two artificial transmission lines. The distributed nature of the capacitance allows the amplifier's bandwidth extension, while the gain of the DA is emerging as additive patterns is comparatively low.

In early days of amplifiers, tubes are used in order to amplify RF signals. Nowadays microwave amplification depends mainly on microwave transistors. Although the transistor became the major element in amplifiers, it has limitations on broadband

operation due to its inherent characteristics. These characteristics bring up frequency dependent behavior, some of which may be listed as:

- Magnitude of S_{21}(gain) decreases with frequency at a rate of 6 dB/octave. Phase of S_{21}also changes from frequency.
- Both magnitude and phase of S_{12}(isolation) changes from frequency. Together with the change of S_{21}, this variation can cause stability issues for broadband operation.
- S_{11}(input return loss) and S_{22}(output return loss) are also frequency dependent which makes impedance matching problematic.

In order to design a proper constant gain amplifier, the limitations mentioned above should be eliminated.

2.2 Gain-Bandwidth Product

The gain-bandwidth product is the product of the gain and the bandwidth of an amplifier which describes the operational amplifier gain behavior with frequency, in any point of the frequency response, is a constant. The bandwidth can be obtained with the following formula:

$$Bandwidth[Hz] = \frac{Gain\ Bandwidth\ Product\ [Hz]}{Closed\ Loop\ Gain, Av} \tag{2.1}$$

Gain and bandwidth products of an amplifier stage limited by intrinsic parameters to the active device employed, expanding the bandwidth will give rise to a reduction in the gain (Gassmann, 2007; Narendra et al., 2012; Narendra et al., 2010).

As the gain is made close to unity, it becomes inefficient to cascade amplifier stages. On the other hand, combining the outputs from a number of active devices in parallel will increase the output power but will produce no improvement in the gain

bandwidth product (Wong, 1993). In Figure 2.8 illustrated this concept by considering a simple transistor combined with coupling circuit.

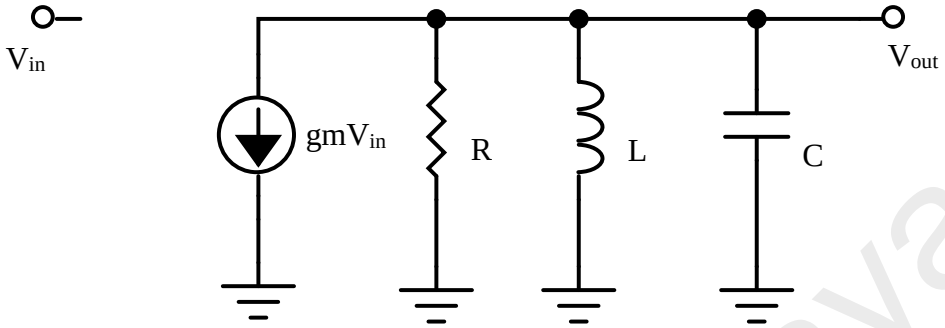


Figure 2.8: Simple bandpass amplifier structure.

The transfer function of the above circuit can be obtained as:

$$A_v(\omega) = \frac{-g_m}{1 + jQ\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)} \tag{2.2}$$

Where $\omega_0 = \frac{1}{\sqrt{LC}}$ and $Q = \omega_0 RC$, Q is the quality factor of a resonant circuit.

The maximum gain occurs at middle band and is given by $g_m R$. The -3 dB bandwidth B is given by $\frac{1}{2\pi RC}$. Hence the gain-bandwidth product is

$$A_{v0}B = \frac{g_m}{2\pi C} \tag{2.3}$$

From equation (2.3) the maximum gain-bandwidth product of a given active device will be obtaining if the capacitance is close to the intrinsic contribution to the input and output capacitance of the active device.

2.3 Image Impedance Method

The image parameter method applied to DA since it consists of a cascade of identical two-port networks forming an artificial transmission line. The analysis can be conveniently accomplished using the ABCD parameters, because the overall ABCD matrix is the product of those of the cascaded two-ports (Wong, 1993) as shown in Figure 2.9.

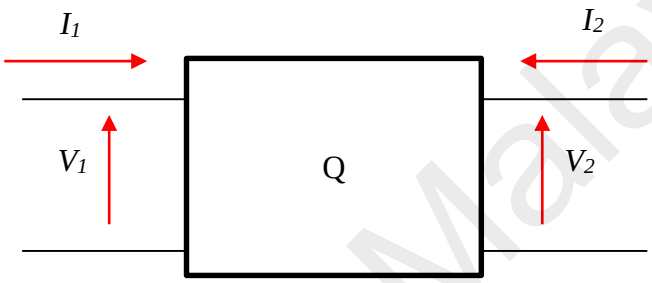


Figure 2.9: A two-port network.

When considering signal transmission and impedance matching in cascaded two-ports, each two-port should operate in the appropriate impedance terminations so that the maximum power transfer takes place over the prescribed bandwidth. Such condition can be met by terminating the two-port with a pair of impedances known as image impedances so that the impedance appears the same when one looks into either direction of each port as shown in Figure 2.10.

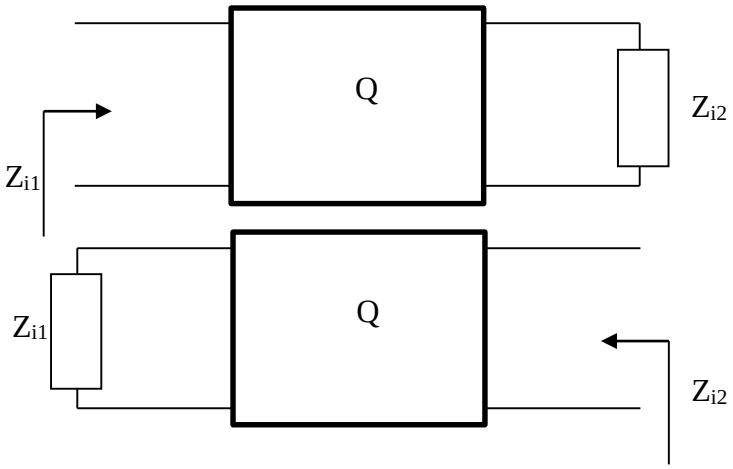


Figure 2.10: A two-port network terminated by its image impedance.

The impedances as Z_{i1} and Z_{i2} can be expressed as

$$Z_{i1} = \sqrt{Z_{SC1}Z_{OC1}} = \sqrt{\frac{B}{D}\frac{A}{C}} \tag{2.4}$$

$$Z_{i2} = \sqrt{Z_{SC2}Z_{OC2}} = \sqrt{\frac{B}{A}\frac{D}{C}} \tag{2.5}$$

Where Z_{sc} and Z_{oc} represent the impedances appearing at port 1 and port 2, short circuit and open circuit respectively. If the network is symmetrical, Z_{i1} and Z_{i2} become identical, and the characteristic impedance are denoted as Z_0.

2.4 Theoretical Analysis of Distributed Amplification

In this section the literature on DA theoretical analysis method will be presented. The circuit networks design and simulations will be done by using Keysight's Advanced Design System (ADS) 2012.08 software which delivers new capabilities that improve productivity and efficiency for all applications it supports and breakthrough technologies applicable to GaAs, GaN and silicon RF power-amplifier multichip module design.

As beginning of the understanding of the electrical performance of the topologies, the circuit analysis shall be started with a simplified basic FET (Field Effect Transistor) model. The intrinsic elements g_m, C_{gs}, C_{gd}, C_{ds}, R_{gs}, and R_{ds} of the small-signal FET model shown in Figure 2.11 are extracted by means of device modeling. For simplicity, as a zero-order analysis, the feedback capacitance C_{gd} can be neglected. It is convenient to investigate gate and drain lines independently to understand its performance over the frequency range.

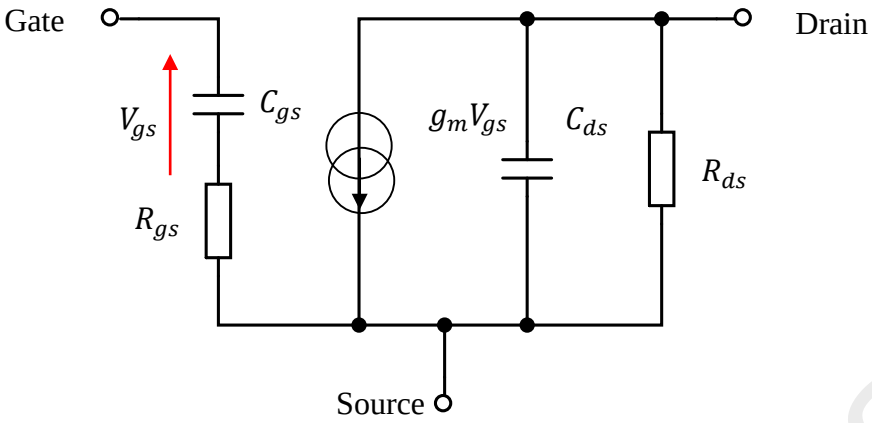


Figure 2.11: Simplified small-signal circuit model of a transistor.

2.4.1 Distributed Amplifier with Periodically Loaded Transmission Lines

According to (Ayasli et al., 1982), a distributed amplifier with periodically loaded transmission lines was first proposed. By considering the unilateral figure of the FET, the above circuit can be separated out two sections each, for gate and drain lines, as shown in Figures 2.12 and 2.13. Hence, the circuit can be analyzed separately. The gate and drain lines are connected to the coupling through the current source *Idn = gmVcn*. Figure 2.12 (b) and 2.13 (b) shows a single unit cell of gate and drain lines respectively.

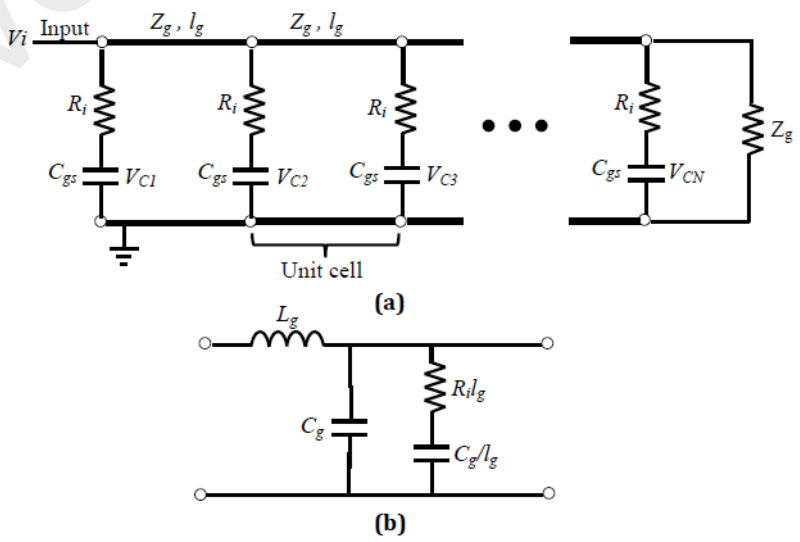


Figure 2.12: Equivalent circuit (a) and single unit cell (b) of gate line.

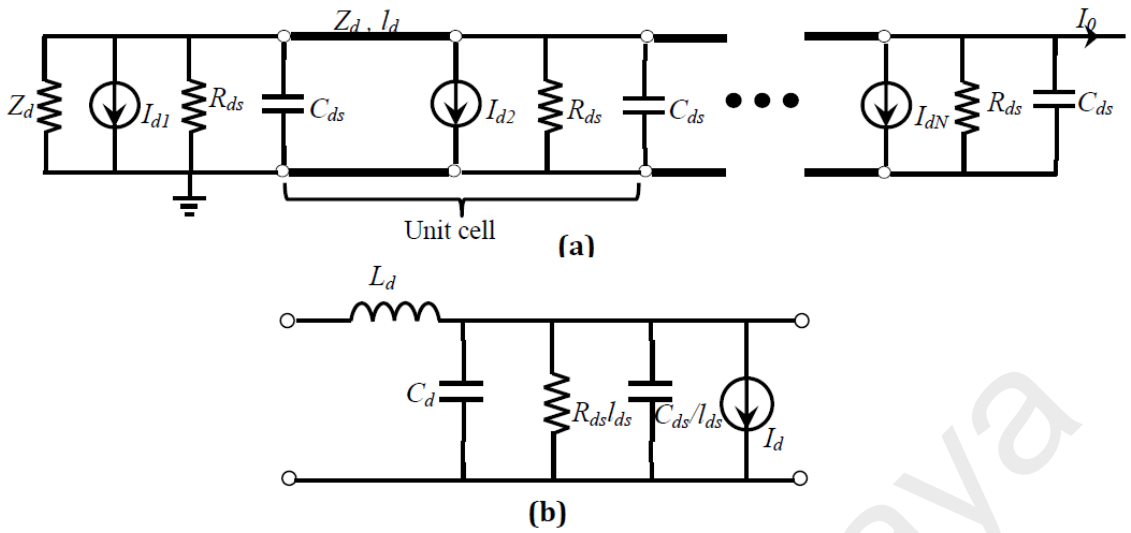


Figure 2.13: Equivalent circuit (a) and single unit cell (b) of drain line.

Lg and *Cg* are the per unit inductance and capacitance of the gate transmission lines. *Rilg* and *Cgs/lg* are the per unit length loading due to the FET input resistance *Ri* and gate to source capacitance *Cgs*. Similarly, *Ld* and *Cd* are the inductance and capacitance per unit length of the drain line and *Rdsld* and *Cds/ld* are the per unit length loading due to the FET output resistance *Rd* and drain to source capacitance *Cds*.

Since the transmission line properties change due to the FET input and output capacitances, we need to obtain the characteristic impedance of the modified lines. For the gate line, the series and parallel admittance per unit length are given by

$$Z = j\omega L_g \tag{2.6}$$

$$Y = j\omega C_g + \left[R_i l_g + \frac{1}{j\omega C_{gs}/l_g}\right] \tag{2.7}$$

$$\Rightarrow Y = j\omega C_g + \frac{j\omega C_{gs}/l_g}{1 + j\omega C_{gs} R_i} \tag{2.8}$$

Where *Z* is the series impedance and *Y* is the shunt admittance. Next, using transmission line theory, characteristic impedance of the gate line is obtained as

$$Z_g = \sqrt{\frac{Z}{Y}} = \sqrt{j\omega L_g \left\{j\omega C_g + \frac{j\omega C_{gs}/l_g}{1 + j\omega C_{gs} R_i}\right\}^{-1}}$$

$$Z_g = \sqrt{\frac{L_g}{C_g + C_{gs}/l_g}}, \quad R_i \approx 0 \tag{2.9}$$

In the above calculation, we have assumed that the loss due to the resistance *Ri*is negligible. By definition, the propagation constant of the transmission line is given by

$$\gamma_g = \alpha_g + j\beta_g = \sqrt{ZY} \tag{2.10}$$

Where, α_g is the gate line attenuation constant and β_g is the phase shift per section of the gate line. A similar analysis is used to obtain the characteristic impedance and propagation constant of the drain line. Hence, the series impedance Z and shunt admittance Y of the drain line are found as:

$$Z = j\omega L_d \tag{2.11}$$

$$Y = \frac{1}{R_{ds} l_d} + j\omega \left(C_d + \frac{C_{ds}}{l_d} \right) \tag{2.12}$$

Next, the characteristic impedance of the drain line is found as:

$$Z_d = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{L_d}{C_d + C_{ds}/l_d}} \tag{2.13}$$

And by using the small loss approximation, the propagation constant can be calculated as:

$$\gamma_d = \alpha_d + j\beta_d = \sqrt{ZY} \tag{2.14}$$

Besides, for the ideal lossless case, the expression of the gain is found as

$$G = \frac{g_m^2 Z_g Z_d N^2}{4} \tag{2.15}$$

Furthermore, amplified signals at the beginning of the drain line decay exponentially. However, increase from the number of sections N is not enough to compensate for an exponential decay of signals. Therefore, we cannot increase the number of sections in a distributed amplifier indefinitely for a real lossy case, which

implies that there is an optimum number for *N* for a given FET. Hence, to obtain the optimum N, N_{opt}, the equation is given as:

$$N_{opt} = \frac{\ln(\frac{\alpha_g l_g}{\alpha_d l_d})}{\alpha_g l_g - \alpha_d l_d} \tag{2.16}$$

2.4.2 Analysis on Periodically Loaded Transmission Lines

As given in (Beyer et al., 1984), the device is considered unilateral, that is, *Cgd* (the gate-to drain capacitance) is neglected. The equivalent gate and drain transmission lines are shown in Figures 2.14(a) and (b). In the analysis, the lines are assumed to be terminated by their image impedances at both ends. With the unilateral device model employed, the two transmission lines are non-reciprocally coupled with the action of the transconductance *gm*.

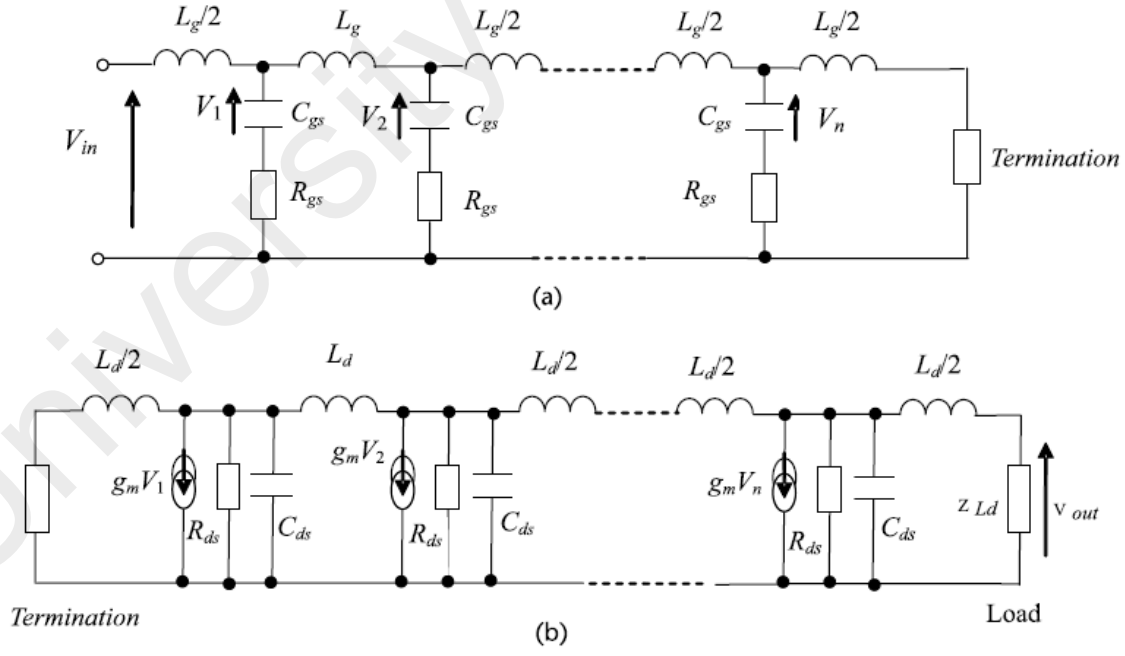


Figure 2.14: (a) Gate transmission line and (b) drain transmission line.

Hence, current delivered to the load of the amplifier is given by

$$I_0 = \frac{1}{2} g_m e^{-\frac{\theta_d}{2}} \left[\sum_{k=1}^{n} V_{ck} e^{-(n-k)\theta_d} \right] \tag{2.17}$$

Where, V_{ck} is the voltage across the gate-to-source capacitance of the k_{th} FET,

$\theta_d = A_d + j\varphi_d$ is the propagation constant of the drain line, A_d and $j\varphi_d$ are the attenuation and the phase shift per section of the drain line respectively, n is the number of FETs in the amplifier. Next, the V_{ck} is expressed in terms of the voltage at the gate terminal of the k^{th} FET and is given as:

$$V_{ck} = \frac{V_i e^{-\frac{(2k-1)\theta_g}{2} - j\tan^{-1}(\frac{\omega}{\omega_g})}}{\left[1 + (\frac{\omega}{\omega_g})^2\right]^{1/2} \left[1 - (\frac{\omega}{\omega_c})^2\right]^{1/2}} \tag{2.18}$$

Where, V_i is the input voltage of the amplifier,

$\theta_g = A_g + j\varphi_g$ is the propagation function of the gate line,

A_g and φ_g are the attenuation and the phase shift per section of the gate line respectively,

$\omega_g = 1/R_t C_{gs}$ is the radian gate line cut-off frequency and

$\omega_c = 2\pi f_c$ is the radian cut-off frequency of the lines.

The most commonly used definition of power transducer gains is the so-called transducer gain G_T defined as

$$G_T = \frac{P_{load}}{P_{av}} \tag{2.19}$$

where P_{load} is the power delivered to the load by the amplifier, and P_{av} is the power available from the source. The latter is the same as the power delivered to the amplifier input by the source of the condition that the amplifier input impedance is conjugating matched to the source impedance.

2.5 Scattering Parameters

S-parameters refer to the scattering parameters. It is an essential part of high-frequency design, which describes the electrical behavior of linear electrical networks when undergoing various steady state stimuli by signals. S-parameters and distributed models provide a means of measuring, describing, and characterizing circuit elements when traditional lump equivalent circuit models cannot predict circuit behavior to the desired level of accuracy. The important topic in here is that how much the gain loss that can be achieved. In Figure 2.15 shows the two-port network. For the S-parameter subscripts "ij", j is the input port, and "i" are the output port. Thus, S_{11} refers to the ratio of signal that reflects on port 1 for a signal incident on port 1.

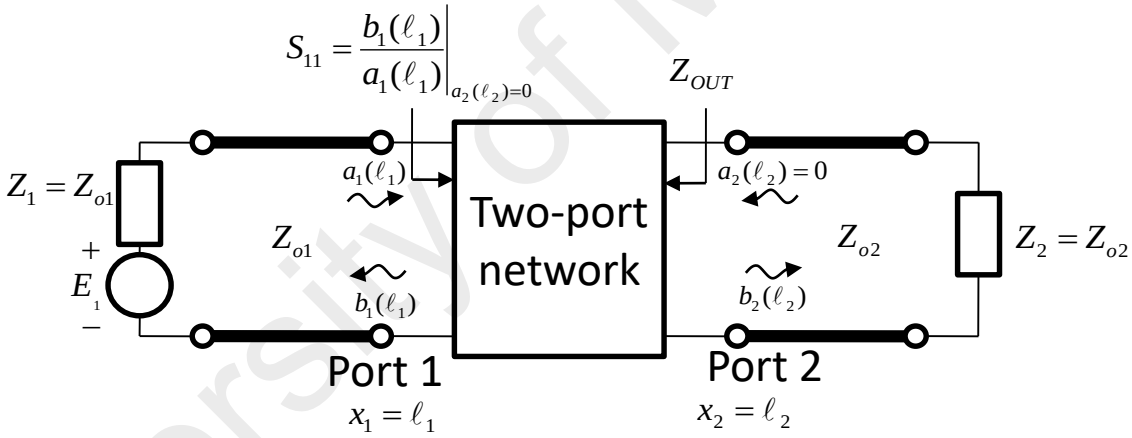


Figure 2.15: Incident and reflected waves in a two-port network.

Besides, S-parameters describe the response to a n-port network of voltage signals at each port. If we assume that each port is terminated in impedance Z_0, the four S-parameters of the 2-port can be defined as followed:

$$S_{11} = \frac{b_1}{a_1}\Big|_{a_2=0} \tag{2.20}$$

$$S_{12} = \frac{b_1}{a_2}\Big|_{a_1=0} \tag{2.21}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \tag{2.22}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \tag{2.23}$$

Where the meanings of the S-parameters are:

- S_{11} = Input port voltage reflection coefficient.
- S_{12} = Reverse voltage gain.
- S_{21} = Forwards voltage gain.
- S_{22} = Output port voltage reflection coefficient

In other words, S-parameters represent the small signal network analysis which acts as the device characterization technique where the measurements are done under small signal power conditions. Under small signal are considered signals that are small enough not to drive the device into saturation and thus have only liner effect on the device. The basic purpose of these measurements is presenting the effects of RF energy flow through devices. For any two-port device, such as GaN HEMT based distributed amplifier, the scattering matrix will fully describe the device performance.

2.6 Classes of Amplifier

Power Amplifiers are generally divided into two main categories: linear and non-linear amplifiers. These two categorized amplifiers can be distinguished because of their linearity, efficiency and circuit topologies. Linear amplifiers tend to preserve the waveform shape of the input signal at the output, while nonlinear amplifiers have inevitable distortion in the signal and are suitable for constant envelope signals such as FM, CW. Amplifier classes have unique bias levels for their objectives and has their own trade-offs. The most common linear amplifier classes are A, B, AB; while class A being the most linear of all amplifier types. The main nonlinear amplifier classes are C, D, E, F, G, H and S. Some linear PA class theories and the reduced conduction angles analyses are discussed further down.

2.6.1 Class A

In this class, the transistor is biased in the exact mid-point of the linear range so that the current at the output flows during the entire cycle of the input signal, and the drive signal is kept within certain values so that the transistor will not fall into cutoff or saturation region thus conduction angle of the transistor being 360 ˚. Since the transistor always conducts, there is no necessity for turn-on region, resulting of improved charging storage. Class A amplifiers also extend to have a better high frequency performance compared to other type of power amplifiers and less evident high-order harmonics as it is shown later in this thesis. The quiescent point of this class is shown at the Figure 2.16 below and the amplifier clearly operates in the linear region, so the signal distorted minimally. Because the efficiency of this class is 50% theoretically, the class A power amplifiers are mainly used in applications for low-power levels, requiring high gain. Hence, class A amplifier will have major effect on high power applications for its power consuming property. This is the main disadvantage of this type amplifier, as it costs

significantly more to generate power supply at high power levels. On the other hand, these types of amplifiers are the most linear and the least complex compared to other type of power amplifiers.

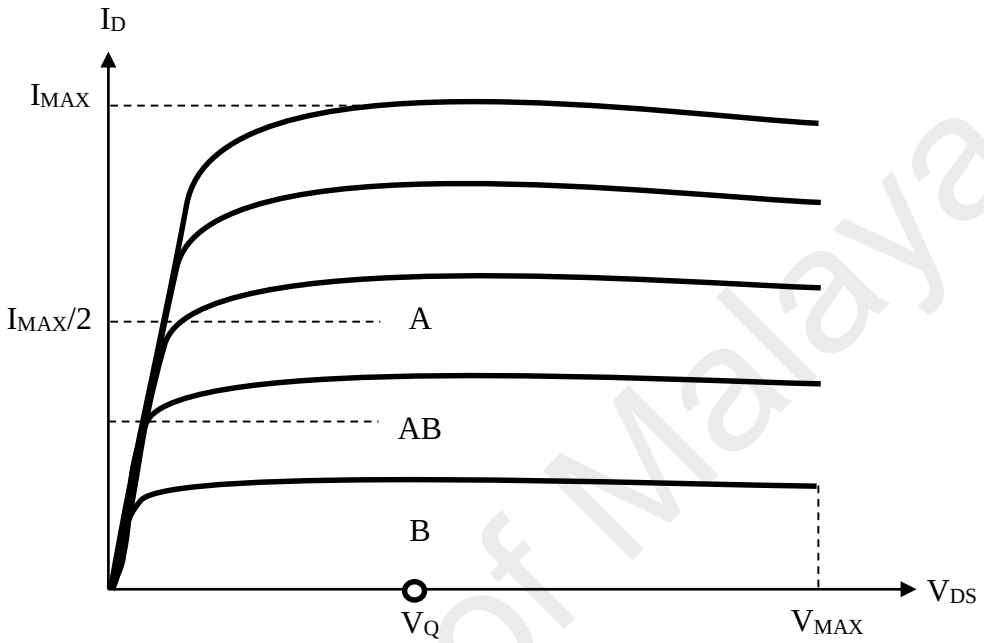


Figure 2.16: Bias points for common PA modes.

2.6.2 Reduced Conduction Angle Analysis

Conduction angle is defined as the fraction of the wave period in which the given active device is conducting, knowing the fact that a full cycle of a sinusoidal waveform can be considered as 360˚. For instance, in Class-A PAs this angle is 360 ˚ as explained before, since the transistor is conducting during the entire cycle. For basic reference, bias points and corresponding conduction angles for common PA modes are given in Table 2.2.

On the other hand, reducing the conduction angle, one can predict useful improvement in efficiency and the concept behind this process is analyzed using figure

2.16. For this analysis, it is illustrated that the conduction angle can be reduced by moving the device bias point toward cut-off from Class-A condition shown in Table 2.2.

Table 2.2: Reduced Conduction Angle for some PA modes

Mode	Bias Point	Quiescent Point	Conduction Angle
A	0.5	0.5	2π
B	0	0	π
AB	0-0.5	0-0.5	$\pi - 2\pi$
C	<0	0	$0 - \pi$

Looking at this figure, an adequate portion of RF drives will cause the input voltage fall below the threshold voltage which is given as in this figure and as a result of this some part of the current is cut off. In order for the current to be able to swing up to maximum saturation point (I_{MAX}), RF drives level must be increased in relation to Class-A condition and the device is assumed to be transconductive. The quiescent voltage point of this process is depicted in figure 2.17 below as V_q.

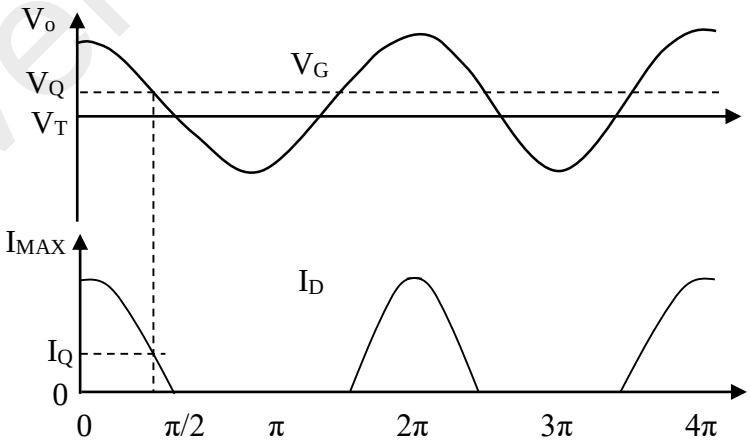


Figure 2.17: Reduced conduction angle waveforms.

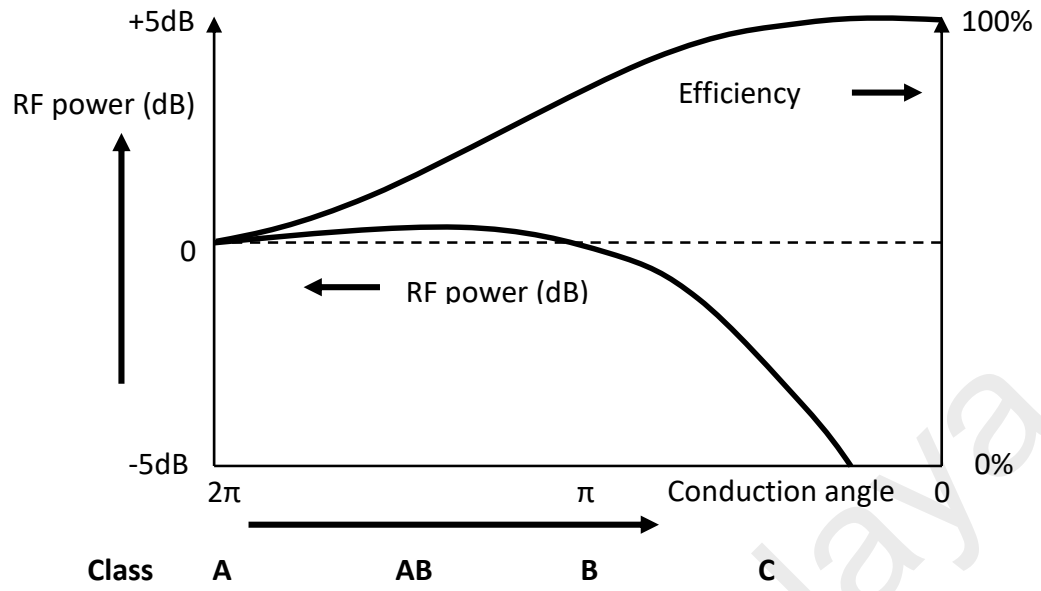


Figure 2.18: Efficiency as a function of conduction angle.

As it is clearly seen in the Figure 2.18, reducing conduction angle gives better efficiency, which is defined as the ratio of fundamental output power to the DC supply power. For instance, efficiency for a class A power amplifier is at 50%, while it increases substantially to reducing conduction angle and reaches to 78.5% for a class B amplifier.

2.6.3 Class B

In class B amplifiers, the conduction angle are 180˚, meaning the transistor conducts either positive or negative half cycle of the input signal, independent of drive level. Analogously, DC bias applied to device determines the class operation; quiescent point at cutoff for this class is shown in figure 2.19. The device is assumed to be linear beyond threshold voltage and harmonics are short at the output, hence fundamental load is resistive according to the assumptions while defining class B amplifier. For an ideal case of class B PA, the efficiency is improved on 78.5% compared to class A, however the trade-off for this improvement is less linearity, since class B amplifier have harmonic contents in the amplified signal.

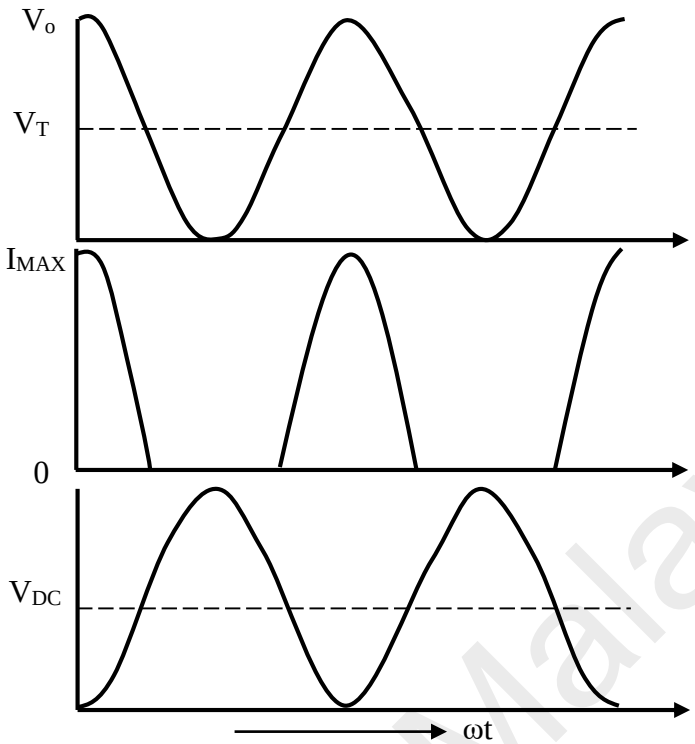


Figure 2.19: Class B Waveforms.

2.6.4 Class AB

A class AB amplifier is a nonlinear amplifier, a compromise between class B and class A regarding to efficiency and linearity parameters and operates between two edges defined for these two amplifiers. For ideal case, an operating class AB mode is biased to a quiescent point, which is in the region between the cutoff point and the bias point of class A. It has a quiescent drain current of between 0.1 and 0.2. Efficiency is improved compared to class A PA, but still less than 78.5% by virtue of conduction angle in this class is between 180 and 360. Unlike class B amplifier, the conduction angle for a class AB amplifier being a function of drive level results from distortion of amplitude modulated signals at their peak power level. Applications of class-AB often utilize wider dynamic range than the two linear PA discussed above. The reason is in fact the diversity of source that causes the gain compression in these mentioned PAs.

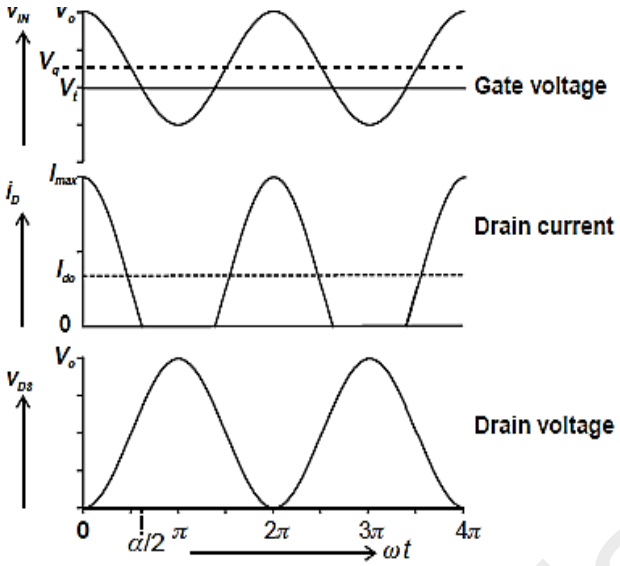


Figure 2.20: Class AB Waveforms.

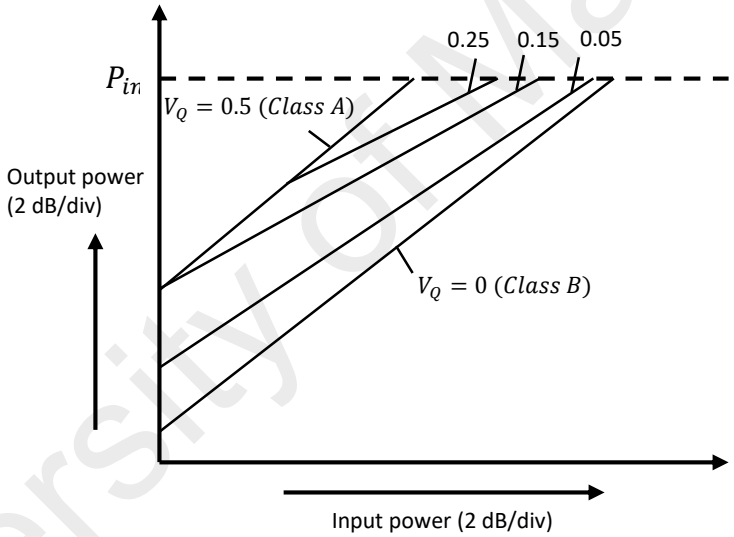


Figure 2.21: Class AB gain characteristics.

For further linearity observation a figure of linearity for different PA modes, which obviously indicates the gain compression for class-AB mode, is given above in Figure 2.21. This gain compression, however, arises from a different source than a class A amplifier which experiences this reduction of gain in saturation region. As a design criterion, quiescent bias voltages of 0.25, 0.15 and 0.05 in the figure correspond to class AB condition. As it is shown in figures above, for class AB waveforms, truncated input signal causes odd degree harmonics which is not a desirable effect in power amplifier design.

2.7 RF Power GaN HEMT

Figure 2.22: Actual component of GaN HEMT. (CREE, 2006-2007)

Due to high bandgap, GaN HEMT device is selected as a power device. The device from CREE Inc. (part number of CGH40010F) depicted in Figure 2.2. Cree's CGH40010 operating on 28 volt rails, offers V_{bk} of ~100 V with 50 Ω condition, which found to be suitable for a variety of RF communication applications. GaN HEMTs offers high efficiency, high gain and wide bandwidth capabilities making the CGH40010 ideal for linear and compressed amplifier circuits. However, they are many GaN devices available from other device manufacturers such as Nitronix, Fujitsu, NXP, Triquint, etc.

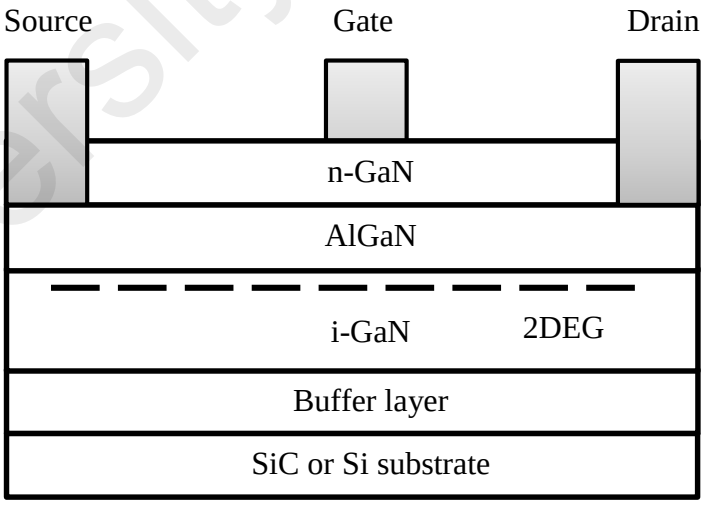


Figure 2.23: GaN HEMT basic configuration.

In Figure 2.23 shows the basic configuration of GaN HEMT. The silicon-doped aluminium gallium nitride (AlGaN) is grown top of GaN, which means AlGaN has an even higher energy gap than GaN. The silicon impurities donate electrons to the crystal

that tend to accumulate in the regions of the lowest potential. This forms a sheet of electrons, which constitutes a two-dimensional electron gas (2DEG). The 2DEG can be contacted with source and drain metals and the depletion region modulated with a gate contact to realize transistor action (Giorgi, 2008).

The enhanced equivalent circuit of a high-power GaN HEMT device can include the delay network to describe the high-frequency delay effects, the source spreading resistance to describe influence of the device channels into the increase in magnitude of S_{21} with frequency, and the electrothermal elements to estimate channel temperature rise due to power dissipation. However, it is the most important to proper evaluating the main nonlinear intrinsic elements of the device equivalent circuit, while the extrinsic linear elements, whose effects are not so significant especially at lower frequencies, can be included within the distributed circuit parameters. In table 2.3 shows the comparison between the properties of Gallium Nitride to other semiconductor materials. In addition, GaN based HEMTs had certain unique properties that make them well suited for high frequency, high power applications(Rajkumar Santhakumar, 2010). These are:

1) **High breakdown voltage**. The wide band gap of GaN, about 3.4 eV, results in a much higher breakdown field strength (>3.3 MV/cm) when compared to other semiconductors. This in turn results in high breakdown voltages for GaN HEMTs. Hence, these transistors can be biased at higher drain-source voltages. For power amplifiers, this usually results in easier impedance match to 50 Ω.

2) **High electron sheet charge densities**. The ability of GaN to form a heterojunction with materials like AlxGa1-xN and the presence of strong polarization fields (spontaneous and piezoelectric) results in a 2DEG at the interface without the need for external doping. The sheet charge densities thus obtained are much larger than in hetero-

junctions in other semiconductors. At the same time, due to the absence of dopants, high mobility can be maintained. The high sheet charge results in high output current.

3) **High saturation/peak electron velocities**. The electron velocities in GaN are comparable to or better than other semiconductors. However, the electron mobility is not as high as in some other semiconductors like GaAs. This problem can be overcome by designing devices with short gate lengths so that the electric field is kept high. This should make the device performance more dependent on saturation velocity rather than mobility.

4) **High thermal conductivity**. Inherently, GaN exhibits better thermal conductivity than GaAs or InP. However, free-standing GaN substrates were not available at the time of this work. The substrate of choice to grow the GaN epitaxial layers was 4H-SiC. In addition to having a good lattice match to GaN, SiC shows almost three times higher thermal conductivity than GaN. Hence, GaN-on-SiC offers a very high thermal conductivity material system and is well suited to build power amplifiers

Table 2.3: Comparison of gallium nitride to other semiconductor materials properties.(Runton, Trabert, Shealy, & Vetury, 2013)

Semiconductor Material	**GaN**	**4H-SiC**	**GaAs**	**InP**	**Si**
Bandgap [eV]	3.39	3.23	1.42	1.34	1.12
Breakdown Field Strength [MV/cm]	3.3-5.0	3.0-5.0	0.4	0.5	0.3
Saturated Electron Velocity [cm/s)	1.3	2.0	1.3	1.0	1.0
Peak Electron Velocity [cm/s)	2.5	2.0	2.1	2.5	1.0
Electron Mobility [cm^2/Vs)	1000	900	8500	5400	1400
Thermal Conductivity [W/cm^{o}C]	1.3	3.7	0.55	0.68	1.3
Dielectric Constant	8.9	9.7	12.9	12.5	11.7

2.8 Summary of Literature Review

In this chapter, the literature review of distributed power amplifier design work has been presented. By critically analyzing various works, there have been raised several issues of concern regarding broadband amplification limitations and novelty in DPA design for radio frequency communication applications. Therefore, some of the performances such as power, noise and stability, are discussed and theoretical expressions are formulated based on previous research work. Keysight's ADS 2012 software simulator is used to obtain insight of the transistor intrinsic parasitic that affect the DPA performance and design for the impedance termination adjustment. The termination adjustment is expected to provide a relevant improvement in comparison to the conventional DA topology and demonstrates the effectiveness of the topology. In addition, with the unique properties of GaN HEMT power transistor device, it acts as an essence for the DPA designs which is well suited for high frequency and high power RF communications applications.

CHAPTER 3: METHODOLOGY

3.1 Project Overview

This chapter discusses the design methodology of a conventional DPA and a modified DPA with GaN HEMT which including distributed amplifiers topology, software simulations and theoretical analysis. In detail, the process of designing GaN HEMT bias network, gate line adjustment network, drain line tapering method, Real Frequency Technique RFT for input matching network and prototype development with fabrication process are presented in this chapter. In Figure 3.1 shows the research flowchart that carried out throughout the design and development process.

At the beginning of this research studies, several research works have been reviewed and summarized in chapter 2 to gain knowledge on the invention of PA as well as how does the design should evolve. The basic principle of DPA design has been studied in-depth and investigated the design concepts and limitations for degree of enhancement. Next, several theoretical analysis has been carried out, such as the circuit architecture, image impedance technique, M-derived network, S-parameters analysis and device selections.

Advanced Design System (ADS) is a useful software tools that provides an integrated design environment to construct RF network and perform ideal results for the simulations. This software is produced by Keysignt EEsof EDA, a division of Keysight Technology. The design process is divided into two design and both are distributed PA. For the first DPA design, the optimum impedance need to be determined and load pull measurement technique is used to verify the best impedance for the whole DPA system. Followed by the integration of impedance transformer by using Real Frequency Technique in the MATLAB environment is developed. This impedance transformer is

integrated at the drain line of DPA, where MATLAB is used to produce a proper network according to circuitry parameters and characteristic of power transistor used.

Besides, the conventional DPA with very basic schematic of DPA is constructed and the values of lumped elements is calculated according to number of stage used. In second design, the conventional DPA is modified with phase adjustment and drain line tapering implementation. The phase coherency has been analyzed with theoretical aspects and the gate line impedance has been adjusted accordingly to enhance the conventional performances. Drain line tapering with non-uniform impedance values is produced to boost the overall efficiency. Based on the impedance adjustment at the gate line of DPA, optimum impedance at the input source is obtained. Eventually, these values are used to build the new input matching network by using RFT in MATLAB environment.

On top of that, the new DPA design is simulated with the mentioned techniques and optimize until the results achieve the design specifications. Else amendment for DPA circuit architecture need to be done. After several simulations carried out, the best performance result is chosen for prototype fabrication. The prototype board is developed with practical industrial realization in OrCAD software which is used to design PCB board. Firstly, the lumped elements are converted to microstrip transmission line in ADS to observe the ideal performances. Secondly, the board layout is designed in OrCAD environment and send for fabrication. OrCAD is a PCB layout design software tool to create schematics and electronic prints for manufacturing PCB from Oregon company. Thirdly, the fabricated board is assembled with surface mounted devices, and carry out troubleshooting on connections before going to next step. Finally, the prototype board is validated with measurement equipment, such as spectrum analyzer to obtain state-of art performances.

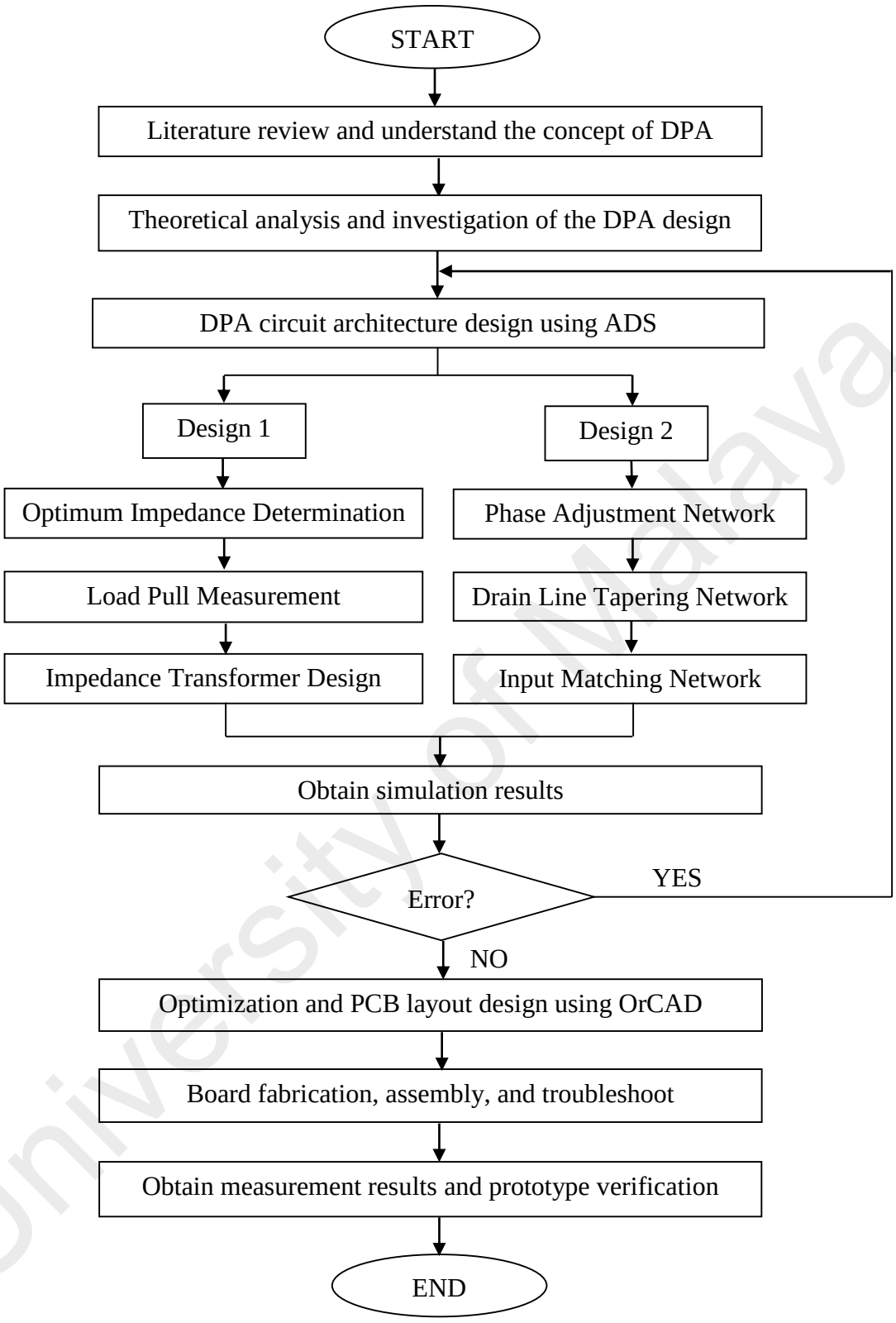


Figure 3.1: Project flow chart for distributed amplifier design.

Table 3.1: DPA designs specifications.

	Design 1	**Design 2**
Bandwidth [MHz]	100-2400	80-2000 (ISM band)
Output Power [Watt]	≥10	≥10
Class of Operations	Class A	Class AB
Power Added Efficiency (PAE) [%]	>30%	>40%
Gain [dB]	≥30 dB flat gain	≥10 dB flat gain
DC Supply [V]	28	28
Device Technology	• **pHEMT** (ATF 54143 and ATF511P8 from Avago) + • **GaN HEMT** (CGH40010F from CREE)	• **GaN HEMT** (CGH40010F from CREE)
Design Tools	• ADS • CAD simulator • MATLAB • CST • OrCAD Cadance	• ADS • MATLAB • OrCAD Cadance
Applications	SDR	LTE, and UHF radios

3.2 GaN HEMT Bias Characteristics

A Class AB type of biasing was chosen to get a compromise between linearity and efficiency while maintaining a high output power. For CREE CGH40010F transistor gate bias voltage = -3 V and voltage sweep from -3 to 1.5 V with 100 mV step. A current versus voltage characteristic of transistor graph is plotted and the test bench in ADS is carried out as below. VGS = - 2.8 V was found to be good point to bias the transistor with regard to class AB operation in chapter 2. Bias point in result of drain current of IDS=154 mA voltage swing from 5 V to 28 V and IDSmax=1049 mA.

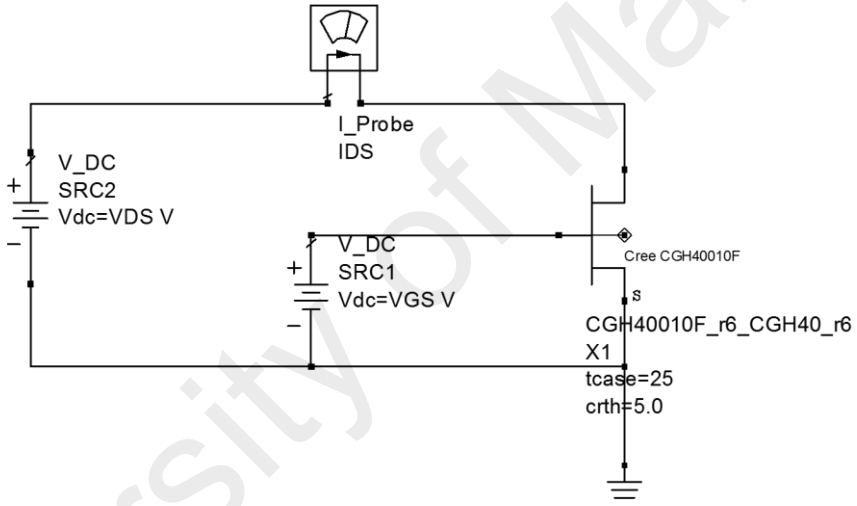


Figure 3.2: Schematic of GaN HEMT bias characteristic for bias point selection.

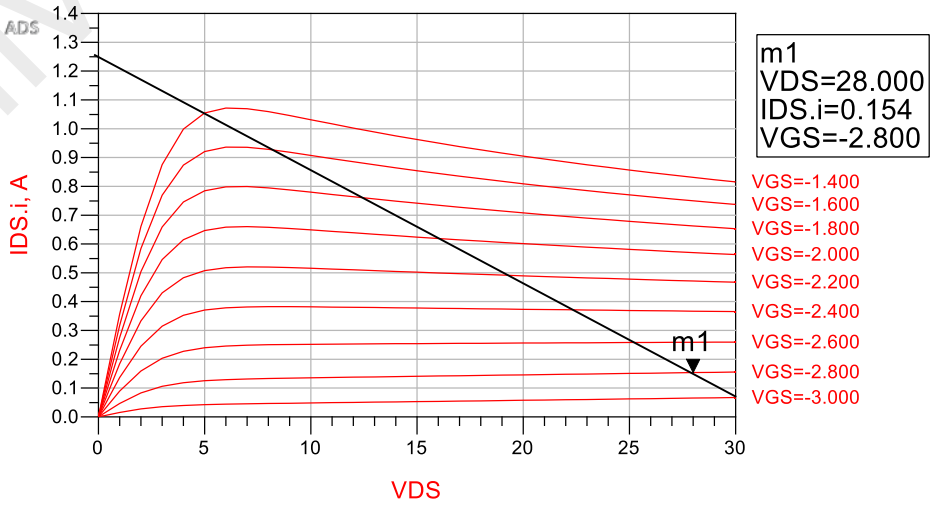


Figure 3.3: IV curves simulation results.

3.3 Image Parameters

The image impedance method is applied at the gate line of distributed amplifier. It consists of a cascade of identical two-port networks forming an artificial transmission line as mentioned earlier in chapter 2. To achieve an impedance match over a broad range, the load and source impedance must be transformed into image impedance. Else the gain response will not be flat as a function of frequency. The following equations represent T-network and π-network:

$$Z_{OT} = \sqrt{\frac{L}{C}\left(1 - \frac{\omega^2}{{\omega_c}^2}\right)} \tag{3.1}$$

$$Z_{O\pi} = \sqrt{\frac{L}{C}\left(1 - \frac{\omega^2}{{\omega_c}^2}\right)^{-1}} \tag{3.2}$$

Where the cut-off frequency is given by,

$$\omega_c = \frac{2}{\sqrt{LC}} \tag{3.3}$$

In this research the characteristic impedance Zo is fixed at 50 Ohm, therefore the cut-off frequency can be calculated by using the following equation:

$$f_c = \frac{1}{\pi \cdot C \cdot Z_o} \tag{3.4}$$

For this research, the cut-off frequency at 1.5 GHz has chosen for the overall system, while for the lumped elements as 1.63 pF and 4.08 nH respectively. This is due to the selected cut-off frequency has given the maximum gain and power efficiency for 3-stage DPA. However, by adding more stages into the DPA will cause the gain

decreases. This is due to the capacitance is proportional to the dimension of the transistors and gate of DPA, there is a trade-off between gain and bandwidth in DPA design.

3.4 M-Derived

The purpose of using m-derived is to improve the matching network at gate line and drain line of the distributed amplifier. In addition, it gives a sharper cut-off at the edges of the passband and a better impedance characteristic. It is placed at both ends of the gate and drain line termination. The parameter m known as the midpoint impedance, which means the mid-series section is derived by cutting through the middle of the series impedance Z and results in a T section. In a low-pass filter, a clearly defined cut-off frequency followed by a high attenuation is needed. It is not practicable to obtain either of these conditions by wiring appropriate prototype constant-k sections in cascade. In summary, using m-derived band pass filers, the attenuation will increase close to cut-off frequency. Besides, the characteristic impedance is made constant over the pass band of m-derived half sections (m=0.6). Lastly, the f_o is the geometric mean of frequencies of peak attenuation and cut-off frequencies as well. In Figure 3.4 depicted the schematic of gate line network with m-derived attachment.

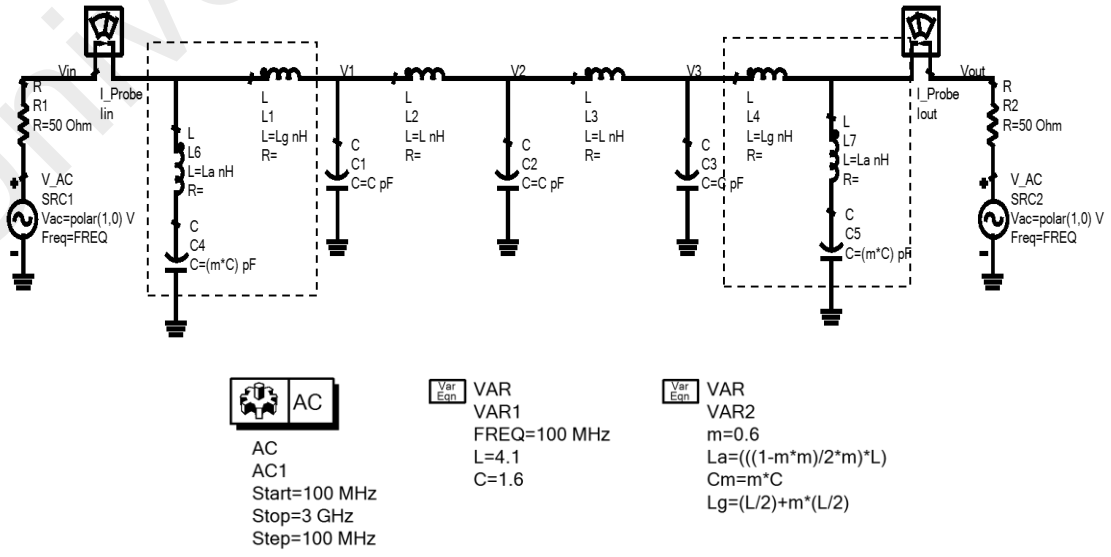


Figure 3.4: Gate line network with m-derived.

3.5 S-Parameter Simulations

In order to design the input matching at the gate line network, Smith Chart utility in ADS was used with load and source reflection coefficient values for simultaneous conjugate matching which was achieved from the design guide simulation results and schematic of gate line network as shown in following figures.

As in Figure 3.5 illustrates the bandwidth from 100 MHz to 1.5 GHz able to maintain at 50 Ω for 3-stage gate line network, with the input impedance values in 50.987-j10.304 Ω at 1.5 GHz beyond that frequency the impedance values is not stable. With the S-parameter simulation, the gate line network was placed 50 Ω terminations at both end ports as shown in Figure 3.6.

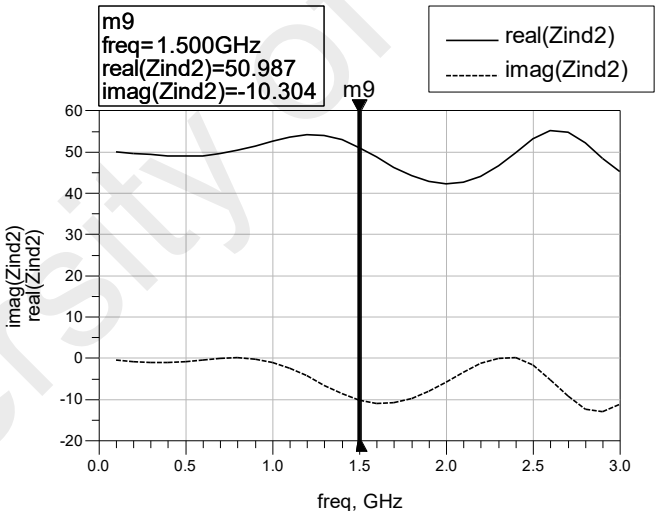


Figure 3.5: Simulation result for input impedance in 3-stage gate line network.

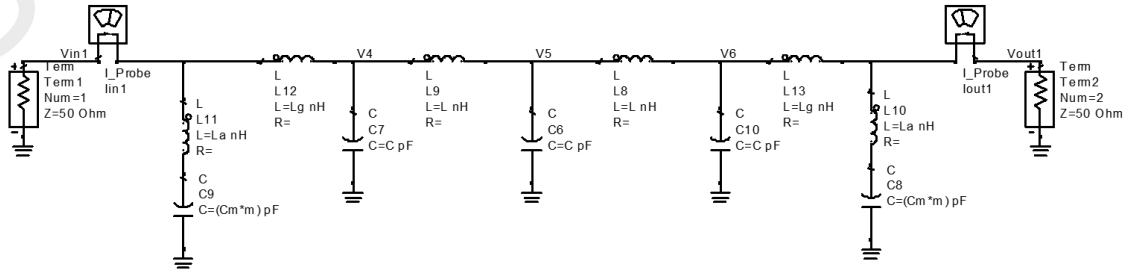


Figure 3.6: S-parameter simulation test on gate line impedance.

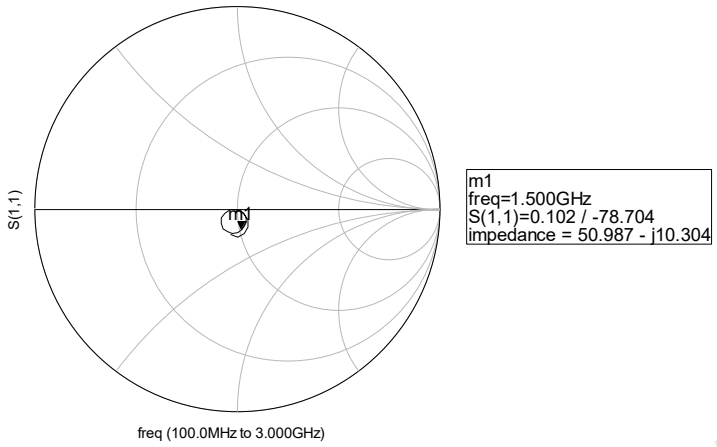


Figure 3.7: Smith chart shows the similar results for Figure 3.6 circuitry.

Based on the simulated results from S-parameter, it is an evident to show that the matching circuit works in S-parameter as compared to AC simulation circuit. Both S-parameter and AC simulations obtained the similar results of impedance value at frequency up to 1.5 GHz while maintain at 50ohm.

The required bandwidth to be achieved has been set 100 MHz to 3.0 GHz initially, after several changes of the impedance values, the value of S11 and S22 has shown a significant degradation at higher frequency due to the characteristic of transistor, therefore other parameters such as capacitances and inductances need to be tuned to obtain an optimum result as discuss in Chapter 4 and 5.

3.6 Impedance Matching

In order to maximize the delivery to the load, impedance matching is playing a crucial role. The ideal condition is to achieve no reflection and allow the entire electrical signal to be transmitted. When the electrical signal propagates in the circuit, a portion of this signal will be reflected at the interface between the sections with different impedances. Therefore, the optimum value of load impedance Z_L needed to be determine, this is where the power delivered to the load is maximized.

Theoretically, the power delivered to the load can be defined as

$$P = \frac{1}{2} V_{in}^2 Re\left(\frac{1}{Z_L}\right) = \frac{1}{2} V_S^2 \left|\frac{Z_L}{Z_S + Z_L}\right|^2 Re\left(\frac{1}{Z_L}\right) \quad (3.5)$$

At the fundamental aspect, Figure 3.8 has shown the matching circuit arrangement. For a single stage PA at Figure 3.8 (a), the matching circuit connected between the source and the input of an active device. In Figure 3.8 (b) the matching circuit is connected between the output of an active device with the load. In the distributed stage, the load represents an input circuit for the next stage. Hence, the matching circuit is connected between the output of the active device of the preceding amplifier stage and the input of the active device of the succeeding stage of the power amplifier as in Figure 3.8 (c).

Ultimately, the load immittance W_L is transferred to the optimum device of output immittance W_{out}, to maximize the efficiency and output power based on supply voltage, the saturation voltage of the transistor and class of operation selected. W_S is referred to the source immittance, where the term *immittance* was introduced by Bode to refer to a complex number, which may be either the impedance or admittance of a system.

The matching circuits have to construct to realize the required voltage and current wave forms at the device output, to provide the stable operating conditions and meet the PA amplitude and phase characteristics requirements. Note that the losses in the matching circuit must be as small as possible to deliver the output power to the load with maximum efficiency.

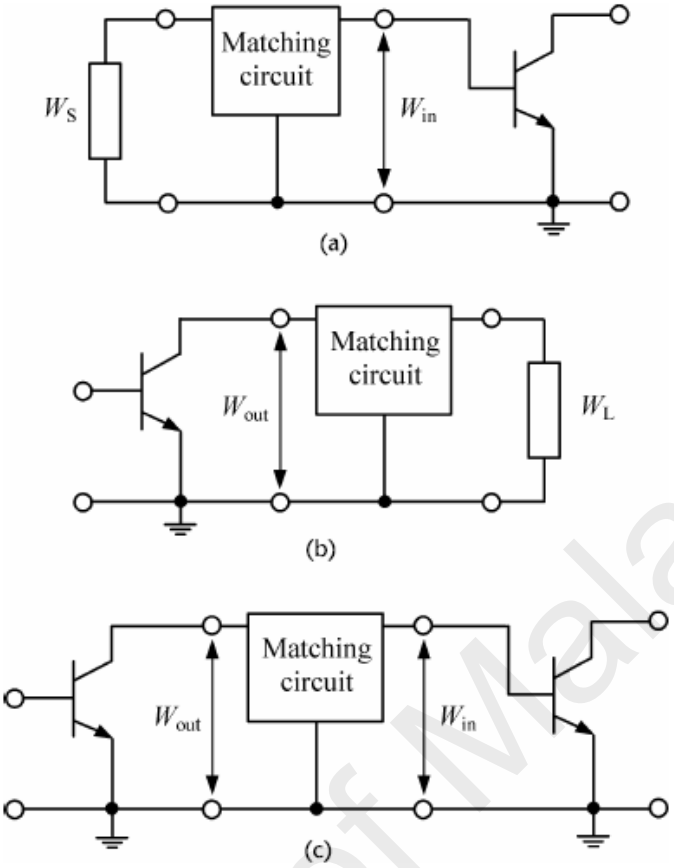


Figure 3.8: The matching circuit arrangement with active devices.

Besides, in figure 3.9 represent the single stage gate line network. This work is focusing on the bandwidth-efficiency enhancement of conventional DPA. Beyer et al. claimed that the gate line attenuation is more sensitive to the frequency response in drain line attenuation. Hence, the concept provides the optimum impedance at both ends of DPA gate line to extend the bandwidth response. Based on the single stage matching network, the simulated result has shown 50 Ω impedances matching up to 600 MHz, beyond that frequency, the impedance value is declining at higher frequency as shown in Figure 3.10.

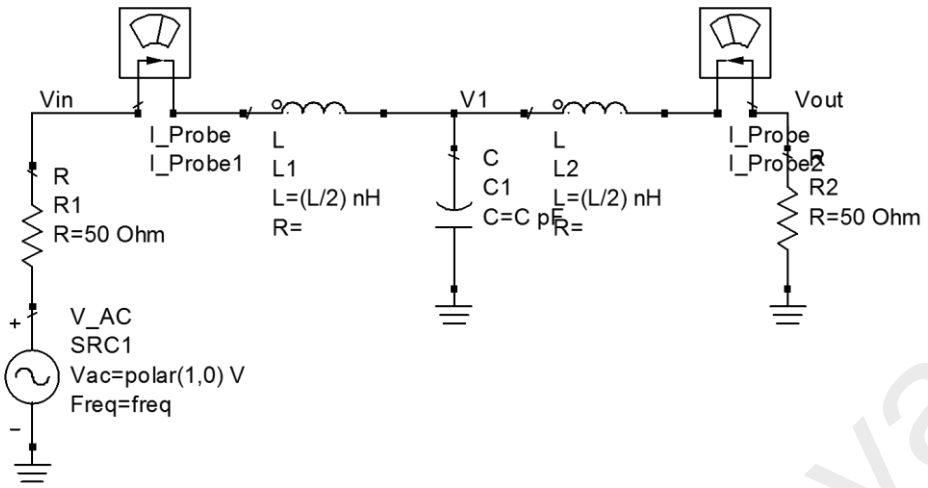


Figure 3.9: Matching circuit for single stage gate line network in ADS.

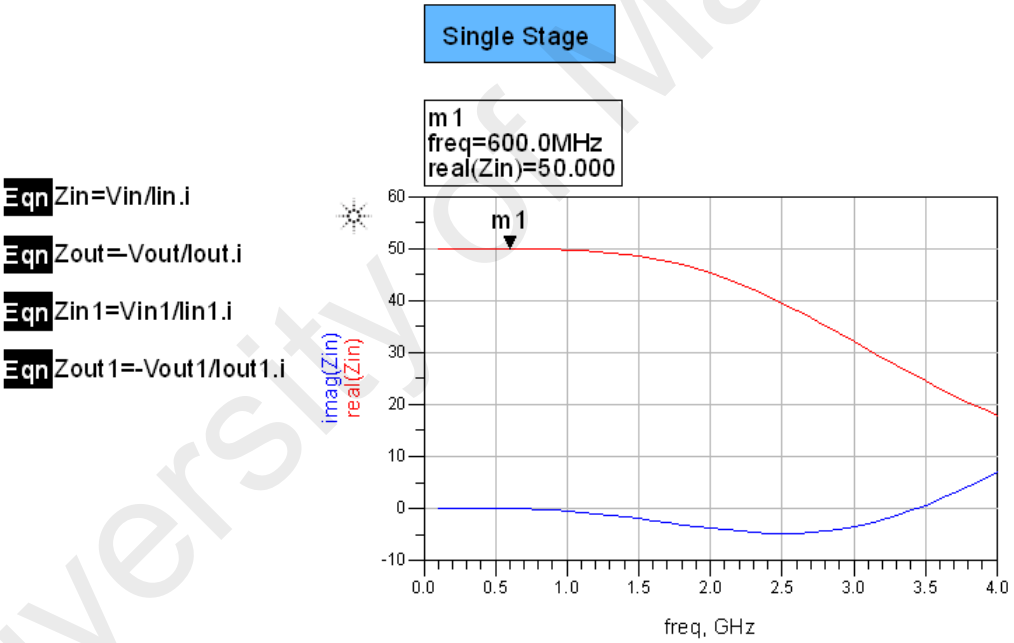


Figure 3.10: Circuit matching of single stage PA in ADS simulation.

As in Figure 3.11, 3-stage gate line is constructed in order to obtain bandwidth extension with traveling wave topology. The both end of the gate line is terminated with impedance source and the impedance load for further adjustment, where the output of impedance matching has been simulated as depicted in Figure 3.12.

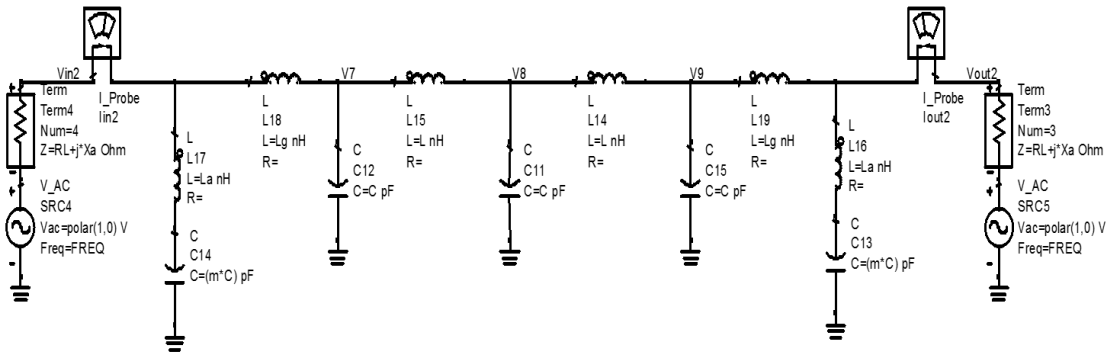


Figure 3.11: Gate line network of a 3-stage PA.

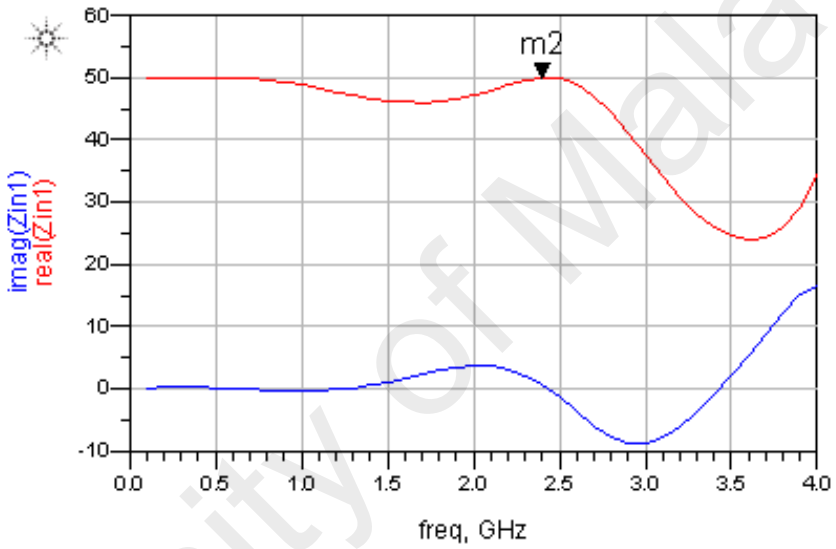


Figure 3.12: Circuit output matching of 3-stage PA in ADS simulation.

For 3-stage gate line, the bandwidth of the input impedance is improved compared to single stage gate line. Bandwidth extended from 600 MHz to 2.5 GHz, which is close to 50 Ω match. As in Chapter 4 and 5, the complete 3-stage DPA matching is constructed with desired bandwidth and simulations is done in ADS for further analysis.

3.7 Design of Input Matching Network via RFT

In this work, the input matching network is designed by employing RFT on the MATLAB environment. This state-of-art approaches such as RFT stands for Real Frequency Technique, which was initially invented by Professor H.J. Carlin of Cornell

University over the last 3 decades. This technique has provided excellent solutions to construct power transfer networks for many applications. Moreover, the RFT has been enhanced by Professor Yarman as the most suitable one to design matching networks and microwave amplifiers for antennas.

Hence, a developed homemade design tool by Professor Yarman on MATLAB utilizing Levenberg-Marquard non-linear optimization algorithm is applied in this research. For single matching problems, RFT generates the lossless equalizer [E] in terms of its back-end reflection coefficient $E_{11}(p) = \frac{h(p)}{g(p)}$. g(p) represents the Hurwitz denominator that can be generated from numerator polynomial h(p) in order to construct scattering parameter of [E]. Hence conventional impedance or admittance parameter does not apply in this case. From the engineering point of view, it is very practical to choose the transmission zeros at DC and infinity. [E] is assumed to be a least phase structure to ensure that the realization of equalizer without coupled coils other than impedance level transformer. The equation below shows the Belevitch form of real normalized scattering parameters of [E].

$$E_{11}(p) = \frac{h(p)}{g(p)} = \frac{h_n p^n + h_{n-1} p^{n-1} + \cdots + h_1 p + h_o}{g_n p^n + g_{n-1} p^{n-1} + \cdots + g_1 p + g_o} \tag{3.9}$$

Note that the integer, n represents the total number of reactance elements. For transforming resistance R_1 and R_2, an ideal input matching network must have a flat TPG at $T_o < -1$ over the operating frequency.

There are few input parameters that needed to be determined in the MATLAB function isqnonlin to construct the structure of input matching network. The MATLAB functions “Isqnonlin.m” is a nonlinear leas square optimization routine which employs

Levenberg-Marquard minimization technique. As in Table 3.2 shows the description of each input parameters that involved in the MATLAB command prompt.

Table 3.2: The input parameters required in MATLAB command prompt.

Input parameters	**Description**	**Input for this work**
f_o	Normalized Frequency	2400 MHz
T_o	Desired flat gain level	0.9 dB
ntr	Control flag for equalizer design. ntr =1 means ideal transformer included; ntr = 0 means no ideal transformer.	0
k	Order of transmission zeros in DC	0
h = [h_n, h_{n-1}, h_{n-2} .... h_o]	Input coefficients for h to determine the elements of matching circuits	[1 1 0 0 1 1 1]
wlow	Low frequency end of the optimization	100 MHz
whigh	High Frequency end of the optimization	2400 MHz
N_opt	Total number of sampling points within optimization	80

The resulting circuit diagram is shown in Chapter 4 and 5 for both DPA designs. After we obtained the input matching network from MATLAB, the Transducer Power Gain (TPG) graph is synthesized to observe the matching circuit's performance. TPG act as the initial guess technique of RFT in MATLAB, this result is then verify again using ADS simulations before producing the prototype board.

3.8 Transmission Line: Microstrip

In this project, the microstrip transmission lines was implied to the DPA system. It consists of a grounded metallization surface covers at bottom of dielectric substrate, height between the trace and reference plane "*h*", the dielectric constant "ε_r" of the material used, a conductive strip of width "*W*" and thickness of the trace "*t*", as shown in the Figure 3.13. Microstrip is frequently used in microwave transmission line, especially for microwave integrated circuits and MMICs. The major advantage of microstrip over stripline are that all active components can be mounted on top of the board. The disadvantages are that when high isolation is required such as in a filter or switch, some external shielding may have to be considered. Given the chance, microstrip circuits can radiate, causing unintended circuit response. A minor issue with microstrip is that it is dispersive, meaning that signals of different frequencies travel at slightly different speeds. Microstrip does not support a TEM mode, because of its filling factor. For coupled lines, the even and odd modes will not have the same phase velocity. However, the open structured microstrip has a major fabrication advantages compared to stripline and coplanar waveguide because of the interconnection, adjustments and simplicity of practical realization.

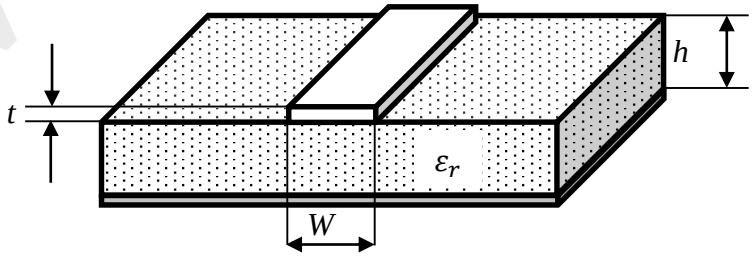


Figure 3.13: Structure of the microstrip line.

Any circuit trace on the PCB has characteristic impedance Zo associated with it. When designing microstrip components, calculating microstrip impedance is more significant. The characteristic impedance Z_0 of a lossless microstrip line can be calculated by the equation as below:

$$Z_0 = \left(\frac{120\pi}{\sqrt{\varepsilon_r}}\right)\left(\frac{h}{W}\right)\left(\frac{1}{1 + 1.735\varepsilon_r^{-0.0724}\left(\frac{W}{h}\right)^{-0.836}}\right) \tag{3.10}$$

Based on this equation, one can compute the opposition to alternating current based on the input values of trace width, thickness, dielectric thickness and dielectric constant. For this project, the characteristic impedance of a microstrip line with zero strip thickness as a function of the normalized strip width *W/h* for $\varepsilon_r = 3.66$ is displayed in Figure 3.14. The mathematics used represented a good closed form approximation for the line impedances between 50 to 166 ohms. Hence, the strip thickness when conducting any design for microstrip line has to take into account.

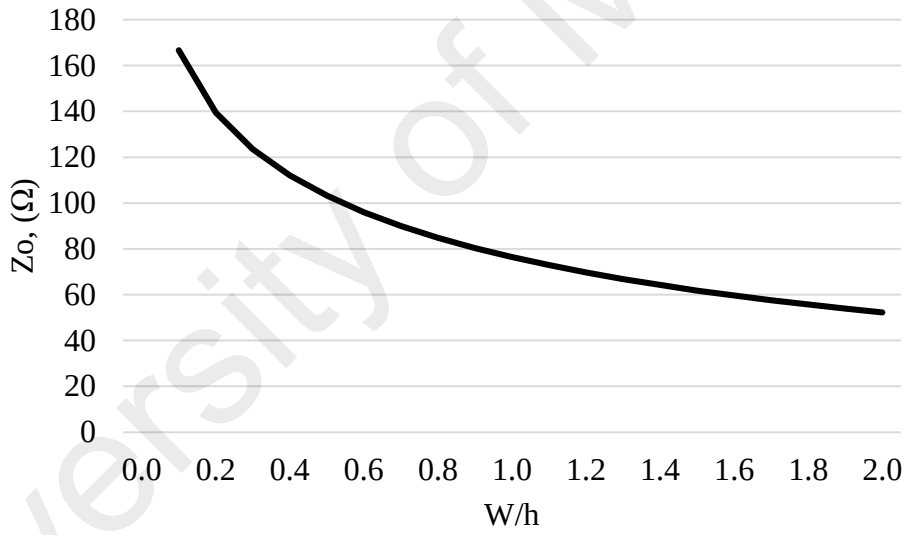


Figure 3.14: Characteristic impedance *Zo* versus *W/h*.

Nonetheless, the Keysight ADS's LineCalc tool has alleviated the mathematical with more accurate calculation to obtain the width and length of the microstrip. In the next topic, the method of lumped inductor to microstrip conversion will be discussed.

3.8.1 Lumped inductor to Microstrip

Lumped inductors act as the energy storage in magnetic field that can be implemented using many different configurations such as spiral. Due to the inductors that applied in ADS simulation does not realized in the actual PCB board, hence the lumped elements is replaced to distributed elements. In Figure 3.15 shows the schematic of a microstrip line connected to 50 Ω termination with S-parameters simulation in ADS software.

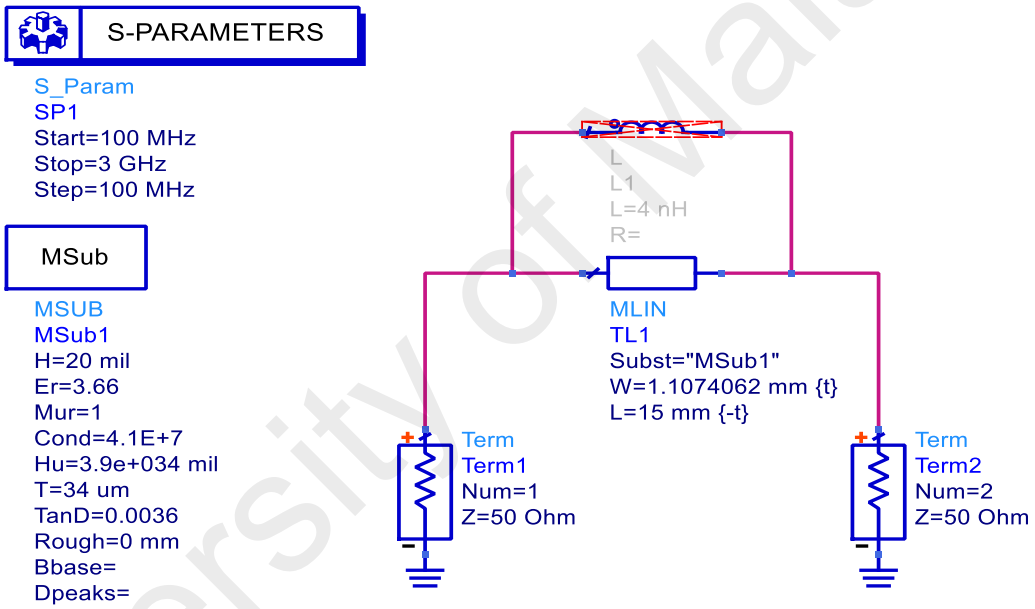


Figure 3.15: Schematic of inductance to microstrip conversion.

Next is to determine the material of PCB used for the research. Rogers 4350B is selected (Rogers, 2015) and substrate parameters in Table 3.4 need to identify based on its datasheet as input parameters in LineCalc tools as shown in Figure 3.16.

In the component parameters, the desired frequency is set to 2.4 GHz. The purpose of using LineCalc tool is to synthesize the physical property such as width, W and length, L of a microstrip line depend on the input of electrical parameters.

Table 3.3: Parameters of ROGERS 4350B Laminate.

Parameter	Value
Substrate thickness	0.508mm
Relative dielectric constant	3.66
Relative permeability	1
Conductor conductivity	4.1×10^7 Siemens/meter
Dielectric loss tangent	0.0034

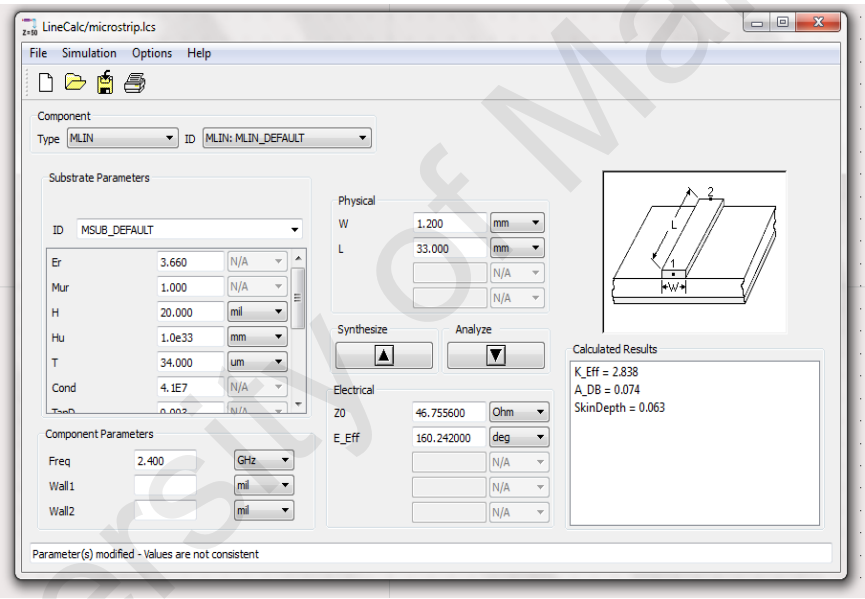


Figure 3.16: LineCalc tools interface in ADS.

Therefore, the electrical parameters have to be determined with the aid of reactance of an inductor formula as followed:

$$X = 2\pi f L \tag{3.11}$$

Where *f* represents the design frequency and L is the inductance in a network. Besides, the reactance of inductor can also be expressed in terms of characteristic impedance Z_o and electrical length Θ,

$$X = Z_o sin\theta, \;\; \theta < 45° \tag{3.12}$$

The lossless matched transmission line with an electrical length Θ less than 45°. In Figure 3.17, the input matching network for the system is constructed in ADS. Circled in red represents the lumped inductor that need to be replace with microstrip line. Whereas in Table 3.5, represent the calculations of lumped elements to microstrip line conversion at gate line input matching network according to equation (3.11) and (3.12) respectively.

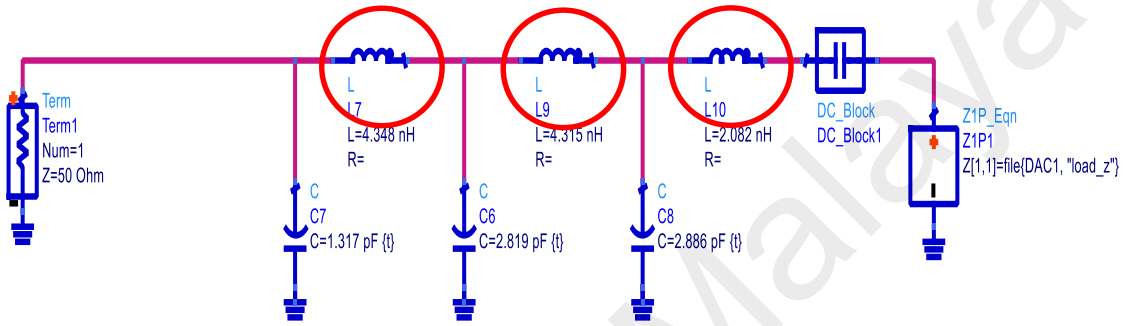


Figure 3.17: Input matching network.

Table 3.4: Electrical parameters determination.

Inductance, L (nH)	2.082	4.315	4.348
Upper band Frequency, f (GHz)	2.40	2.40	2.40
Reactance, X_L (Ω)	31.40	65.08	65.57
Length, θ(°)	42	42	42.0844
$sin\ \theta$	0.6691	0.6691	0.6702
Z_o(Ω)	46.93	97.26	74.89

The value of characteristic impedance Z_o and electrical length Θ is obtained and synthesize in the LineCalc tools in order to acquire the value of L and W of a microstrip line. The schematic is simulated with the input value of L and W to obtain inductance

values that are close to the actual design value as shown in Figure 3.18. The deviation can be optimizing by the adjusting the variable of Z_o and Θ.

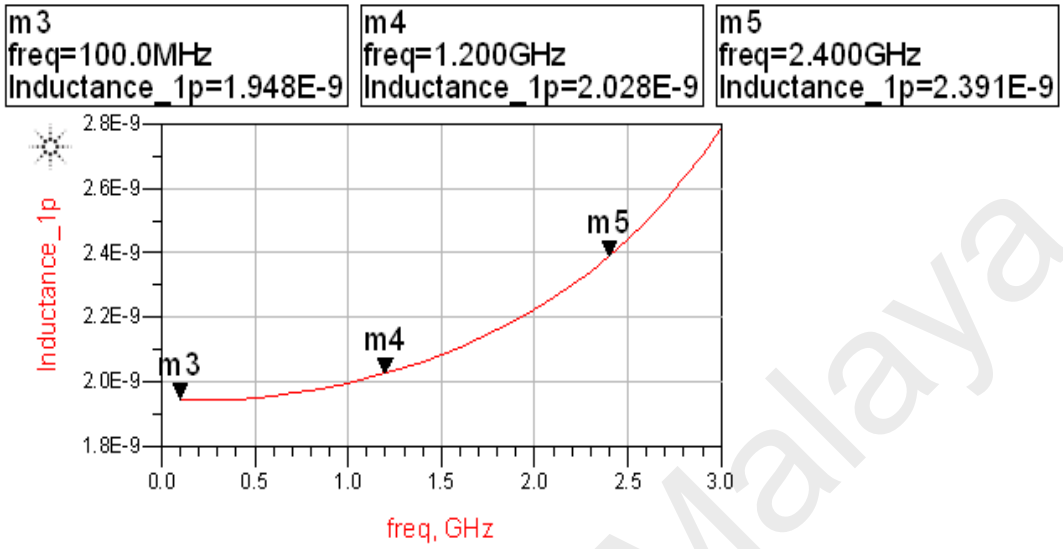


Figure 3.18: Microstrip conversion for actual inductor 2.082nH.

In Figure 3.18 has delivered the least deviation for actual value of inductor 2.082 nH from the simulation. The same procedure is repeated for other value of inductor conversion to microstrip line. Ultimately, all the lumped inductor is replaced with the microstrip line as shown in Figure 3.19.

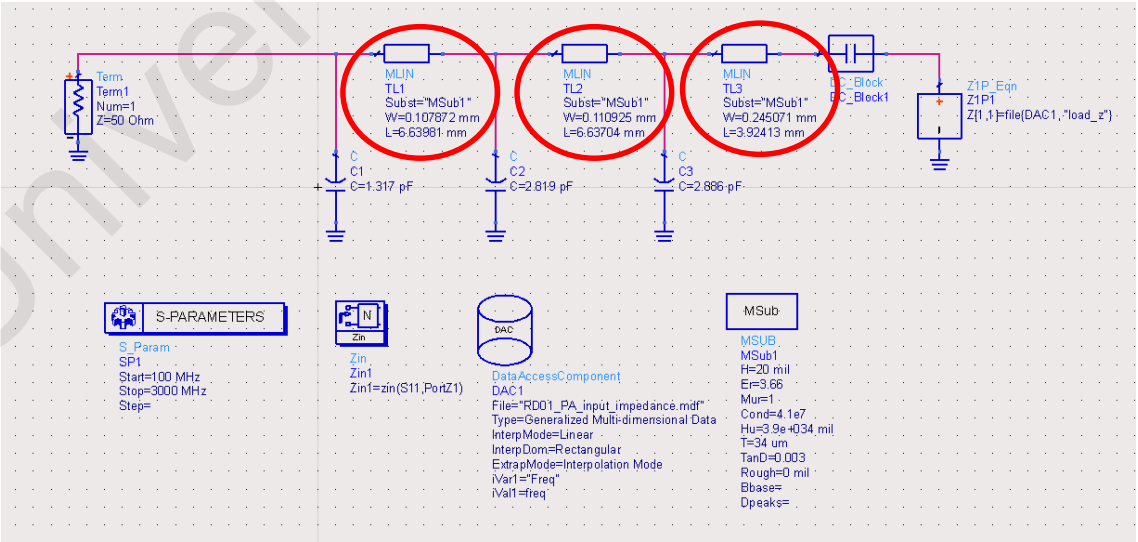


Figure 3.19: Lumped Inductor replaced with microstrip in ADS.

3.8.2 Capacitor conversion with industrial realization

Capacitor are lumped elements that store electrical energy in an electric field between two plate or electrodes when a voltage is applied across them. The circuit of an ideal value capacitor with the industrial capacitor model is constructed as in Figure 3.20, and there are both connected to a 50 Ω termination.

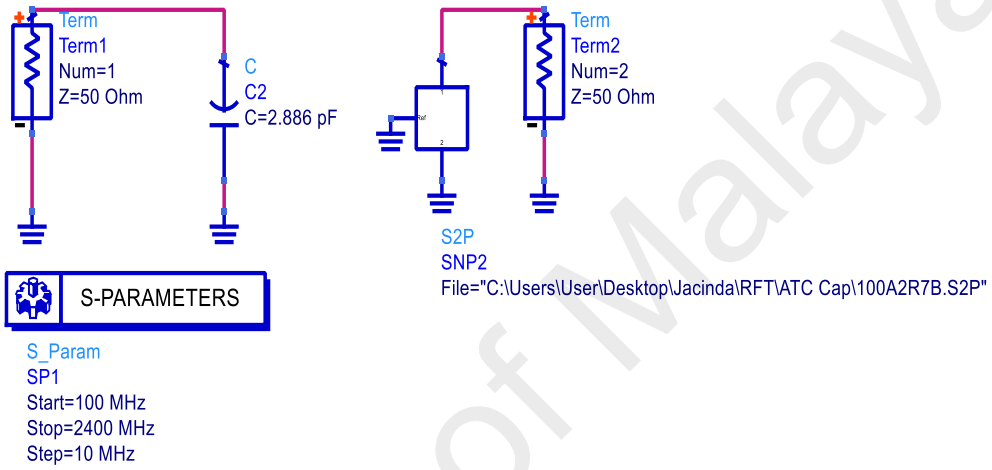


Figure 3.20: Circuit diagram of ideal capacitor and an industrial capacitor ATC 100A model. (Corp., 1996)

The model of industrial capacitor that implement in this work is ATC 100A series capacitor from American Technical Ceramic Corp. which is a surface mounted device that has the most versatile high Q, and high self-resonant multilayer capacitor. Typically function as bypass, coupling, tuning, feedback, impedance matching and DC blocking. In order to run in ADS simulation, the source file of the capacitor model is required and insert them according to the part number of the capacitor. The 2-port S-parameter component S2P is used as function of data extraction from the industrial capacitor model. Hence, the value that are closed to the value of ideal capacitor are chosen.

The capacitors that constructed at the DPA matching network has to be replaced by the actual capacitor value as shown in Figure 3.21. Based on the simulation in Figure 3.22, it represents the results of actual ATC capacitor model with 2.7 pF performs in ADS.

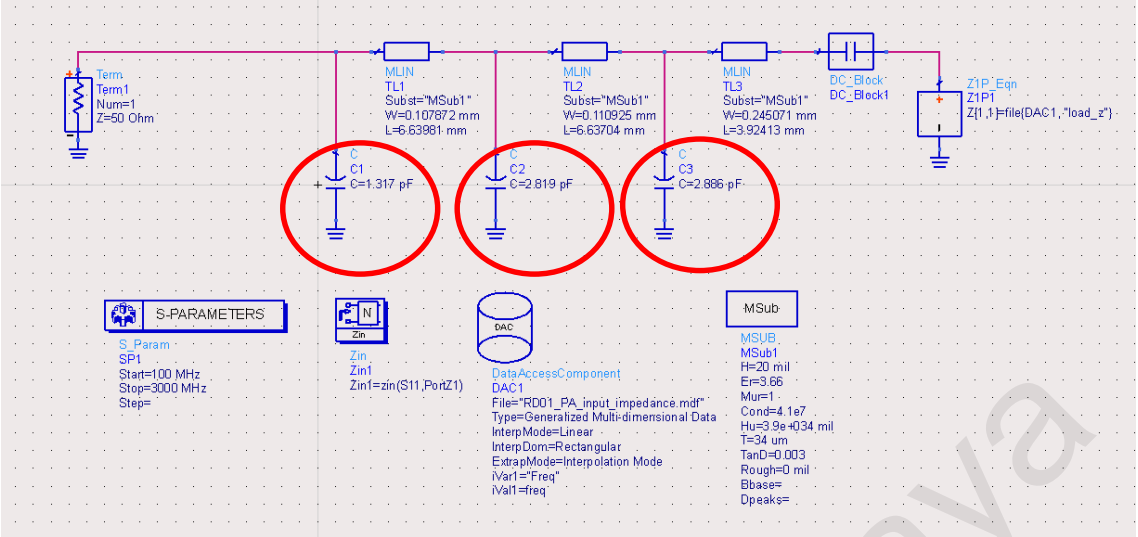


Figure 3.21: Lumped capacitor that need to be replaced with industrial capacitor.

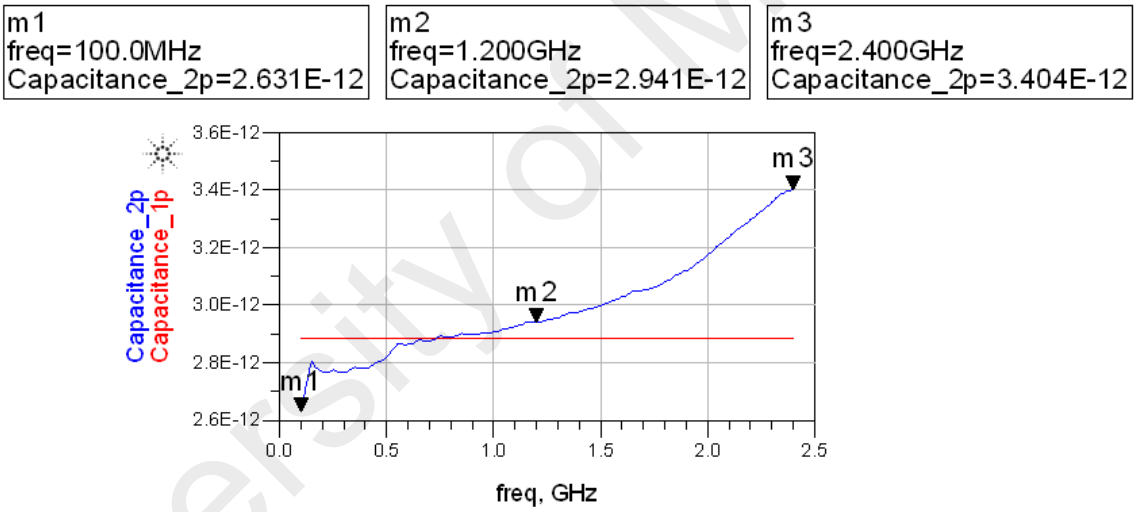


Figure 3.22: Simulation result for ATC capacitor 2.7pF over operating frequency.

For instance, the real capacitor at 2.7 pF is chosen to replace the 2.886 pF ideal capacitor. According to the simulation result, the deviation between the real capacitor with the simulated value is significant. Therefore, it is crucial to select the suitable real capacitor that are closely matched with the ideal capacitor value in order to maintain the overall performance while implement in prototype board.

This lumped inductor and capacitor conversion technique has employ in overall system of the DPA. In figure 3.23, the capacitors in the input matching network has successfully converted to the ATC model capacitor to carry on the simulation of DPA.

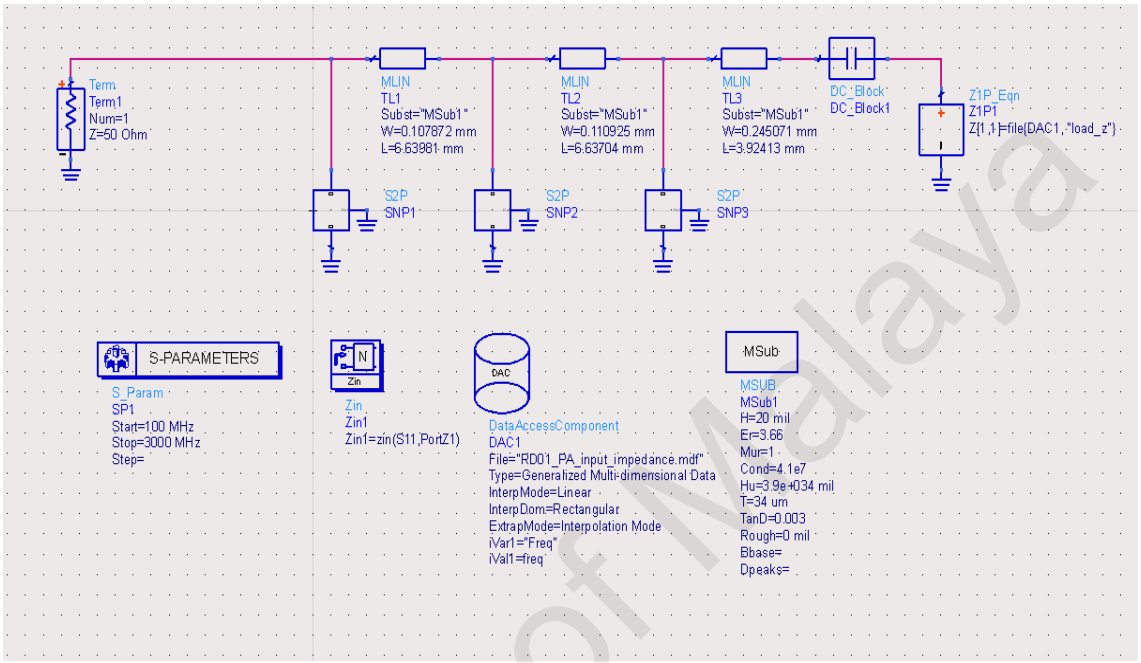


Figure 3.23: Ideal capacitor to industrial capacitor conversion.

3.9 Prototype Development and Fabrication

After the simulated circuit is done, a physical prototype was then fabricated to investigate the circuit performance. Initially, the schematic of PCB is construct by using OrCAD 10.5 Capture CIS. Then each of the layout footprint is drawn in OrCAD layout according to the actual size of component used in this research, for instance, the ATC 100A series capacitor pads with size 0603, followed by the pads of RF choke, transistors, chip resistor, SMA connectors, DC connectors, chip inductors are drawn as in Figure 3.24. Besides that, there are existing libraries and footprints of component that can be used in OrCAD software as well.

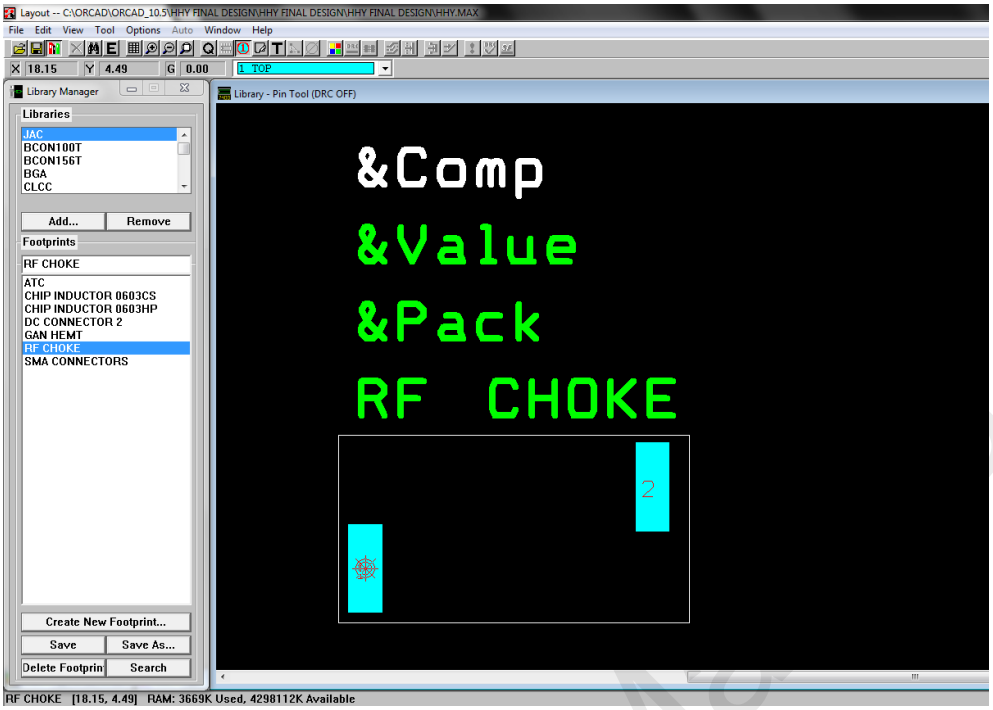


Figure 3.24: Layout footprint of Coilcraft RF Choke device drawn in OrCAD.

After created all the actual component pads, a netlist from capture is imported to generate the PCB layout. All the component pads are arranged accordingly in OrCAD layout. Prototype boards for both designs in this research are fabricated by using Rogers' 4350B laminates with two layers PCB material, which has a dielectric constant ε_r of 3.66, a thickness *h* of 0.508 mm and 2 oz. of standard copper cladding. These prototype boards are fabricated in Circuit Image System Inc. The first layer of PCB is used for RF and DC routing, where all the component placement take place on top of the layer. Whereas, the second layer is the solid bottom ground. These prototypes have an open grounding area with adequate via holes, DC and RF routing that are well isolated. The via holes are connected from the first layer to the second layer, and the grounding screws thread are contacted to the heat sink to provide a better grounding to the device, especially at higher frequency.

After the final layout of the design is done, the OrCAD gerber file is generated and send to Circuit Image company for fabrication. Once fabrication is done, we need to

proceed to the soldering work on the prototype board. One of the most difficult component to solder is the transistors that mounted on PCB. The transistors are not encouraging to be soldered in traditional way since the package is DFN type with no leads to apply solder to. A small amount of solder paste was applied to the copper pads of the transistor footprint and began solder and placed the transistor precisely on the board.

On the other hand, the DC drain biasing terminals are bypassed to ground with multiple chip capacitor, they are 100 pF, 33 nF and 10 μF as a precaution of low frequency oscillation. Whereas the DC blocking capacitors used in this DPA is 33 pF (ATC 100A series capacitor), where the operating frequency must be less than SRF capacitor, hence the higher SRF than 2.4 GHz operating frequency the better blocking.

In the meantime, the DC drain line is then connected to the wideband bias choke 4310LC provided by Coilcraft Inc.. This RF choke is used to block the high frequency AC while passing lower frequency or DC. Note that, at high frequency the inductor becomes a high impedance element that can be used for RF isolation. Without this RF choke, the efficiency of PA can diminish and signal loss occur, as well as RF noise can interfere with other parts of the circuit. The RF choke selection is based on finding an inductor whose SRF is near to the frequency where choking is needed. As for the DC gate line, the high-Q chip inductor of 220nH is used as DC feeding for the DPA system. The SRF must be lower than operating frequency to avoid AC and DC interference.

3.9.1 Mounting Fixture

A mounting fixture for the both designs was manufactured using 7 mm thick aluminum see Figure 3.25 and Figure 3.26 for more details. This mounting fixture also called “heat sink” is used to conduct heat away from the board.

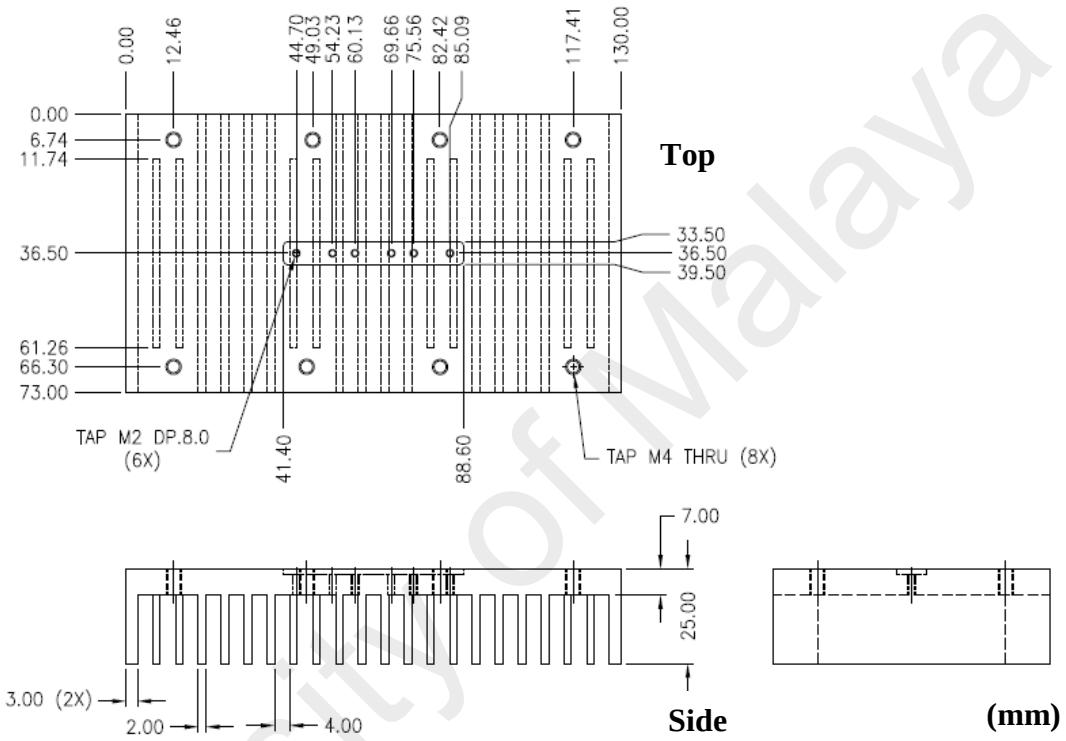


Figure 3.25: Sketching of the aluminum heat sink used to secure the PCB.

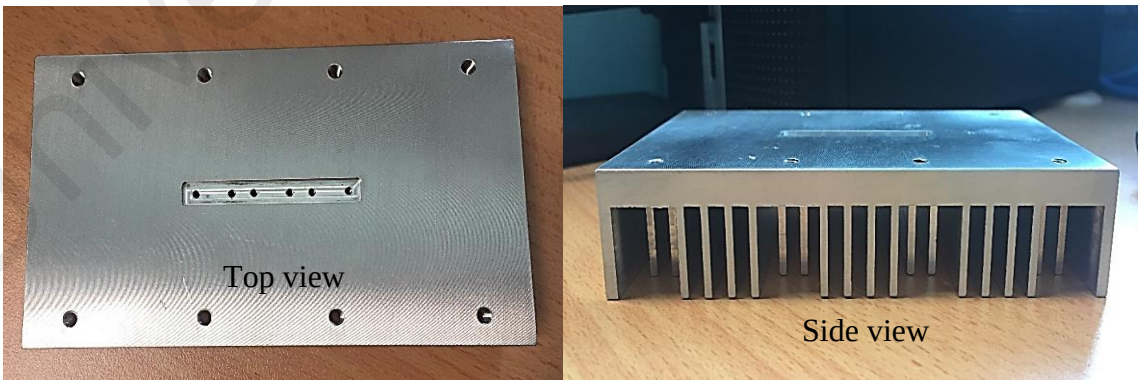


Figure 3.26: Top and side view of an aluminum mounting fixture that manufactured by Brusia Engineering Sdn. Bhd.

The heat sinking properties of the mounting fixture should allow the circuit to operate within safe temperature levels. For a GaN power transistor, a grounded fixture is attached at the bottom layer of PCB via indium foil and multiple screws. This indium foils are provided by Indium Corporation as free samples for this design. It gives a very good electrical and thermal conductivity of 0.34 W/cm at 85 ^{o}C. The foil part number is IN52-48SN with 0.004-in. thickness. Added that, high power DPA requires higher power dissipation, hence indium foil has better heat released as compared to aluminum and copper foil.

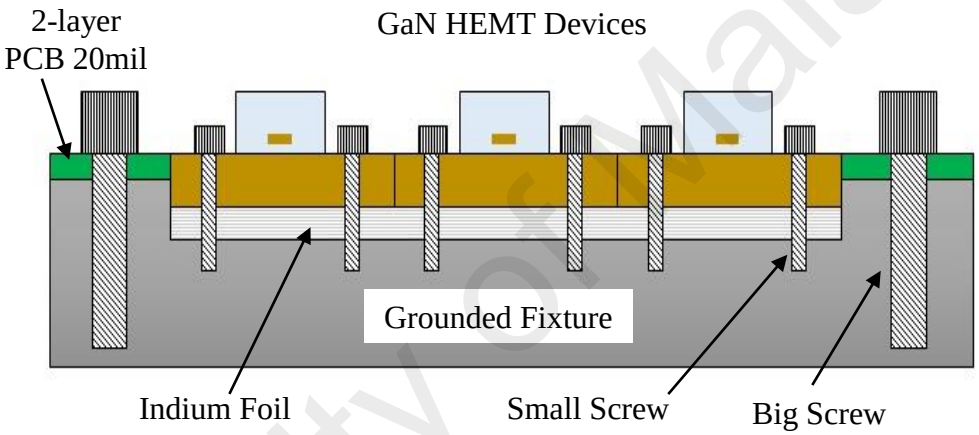


Figure 3.27: Cross-sectional diagram of a GaN HEMT devices on 3-stage DPA.

A cross-sectional diagram of the GaN HEMT devices, indium foil, 2-layer PCB and the mounting fixture with screws are depicted in Figure 3.27. The bigger screw is used to hold the grounded heat sink whereas the smaller screw is to mount the GaN HEMT devices to the fixture.

CHAPTER 4: DPA WITH IMPEDANCE TRANSFORMER INTERGRATION

4.1 Introduction

The demanding radio applications such as software defined radio (SDR) at working frequency up to 2 GHz in (Narendra et al., 2012; Y.Peng, 2011) uses DPA strategies with high efficiency often faced DC-RF energy conversion weaken as the frequency increases towards device cut-off, this is cause of the loading effect of the high power transistors. However, these amplifiers do not achieve the output power greater than 10 W(Palombini, 2013; Zhou, Roy, & Amaya, 2013). The vectorially combined DPAs in (Narendra et al., 2012) has exhibited the best performance in output power-gain response at operating bandwidth 0.04 GHz to 2 GHz. Whereas the work in (Andersson, 2015) has demonstrated output power greater than 43 dBm and more than 45 % efficiency with extending bandwidth up to 2 GHz.

Nonetheless, device selection is important for the DPA development. In current trend of DPA design, GaN HEMT devices has involved in various microwave applications due to their high power density, which is very much applicable for this work. As GaAs pHEMT devices has a super lattice structure for high efficiency power amplification to further inhibit substrate conduction (K. Joshin, 2014).

In this chapter, a new design technique of broadband amplifier is integrated with the broadband impedance transformer. An approach to maximize output power and efficiency from DPA with load pull measurement is discussed and with a novel broadband impedance transformer employing RFT for practical and compact design solution of radio communications (100-2400 MHz) applications is introduced.

4.2 Optimum Impedance Determination of DPA

Impedance determination at the drain line transmission is imperative for the maximum output power achievement. In this section, the method to determine optimum impedance is described in details. At the drain line of the DPA, the current source from each of the active devices is loaded by its optimum load impedance represented by $R_{opt}(\omega)$. The current sources from each section are combined to a single load in order to achieve the peak excursion of RF voltage and current swing. Added that, it is leading in the Class A amplifier operation as V_{max} and I_{max} (Cripps, 2006). However, the optimum power performance is represented as Z_L as shown in Figure 4.1.

To fulfill the manner as mentioned above, the optimum virtual impedances $Z_u(k)$ and $Z_r(k)$ are flows in two directions (K. Joshin, 2014) where k refers to the total section of DPA i.e. $k = 1, 2, 3, \ldots n$. The generalized design equation can be derived from Fig. 1 as

$$Z_{u(k)} = \left(\frac{I_1}{I_k} + \frac{I_2}{I_k} + \frac{I_3}{I_k} + .. + \frac{I_n}{I_k}\right)(R_{opt,1} // R_{opt,2} // .. // R_{opt,k} // R_L) \tag{4.1}$$

where I_k serve as the magnitude of the complex current sources and in-phase combining is considered. The impedance at n stages with identical power transistor can be close to R_{opt} with valid Z_L termination and written as

$$Z_u(1) = Z_u(2) = Z_u(3) \approx R_{opt} // Z_L \tag{4.2}$$

Whereas the impedance at the drain transmission line $Z_r(k)$ must be synthesized to load each device generator by its optimum $R_{opt,k}(\omega)$. Hence, it is important to analyze the fundamental value and initial guess of the $R_{opt,1}$ and Z_L in order to acquire the load pull simulations and measurements of the single device. In this situation, CAD simulator is used to ease the design process with an optimizer assisting the transistor model with an ideal current source and parallel high impedance. The design approach utilized vectorially combine current sources with load pull determination (B. S. Yarman, Jun. 2010), as the

phase is synchronized between the current source and the transmission line delay. The $Z_r(k)$ are coordinated at each junction of the device peripheries, where the current is combine in the additive patterns as depicted in Figure 4.1.

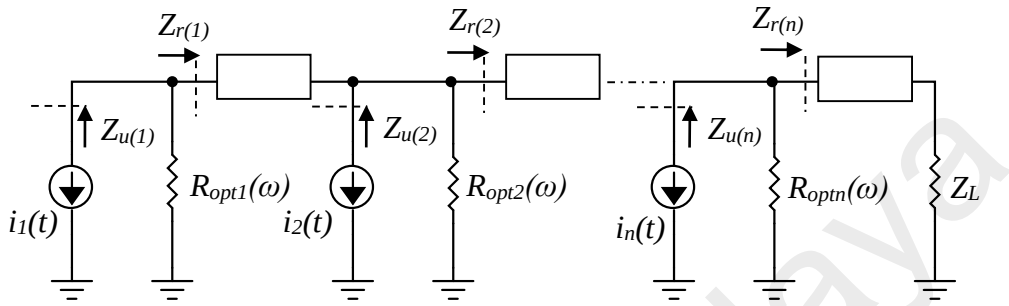


Figure 4.1: Optimum load impedance $R_{opt,k}(\omega)$ loaded at each of device generator at drain line.

In Figure 4.1, the schematic shows the optimum load impedance from each device generator at the drain line, and exhibits frequency-dependent behavior. Hence, the selected power transistor (CGH40010F) with $R_{opt}(\omega) \approx 40\ \Omega$ is acquired at the average value across the bandwidth. The optimum number of devices used in this DPA design is $n = 3$, where $Z_r(1) \approx 40\ \Omega$, and $Z_r(2) \approx Z_r(3) \approx Z_L$ are optimized in CAD simulator, for optimum power performance up to 2 GHz the recommended Z_L is 12 Ω (Narendra et al., 2010).

Nevertheless, with load pull measurement technique shown in Figure 4.2, the optimum load pull measurement of the Z_L at 1 GHz as reference frequency the optimum power performance such as output power and PAE is achieved at ~12 Ω region in measured level. The load pull impedance determination with the bandwidth of 100 MHz to 2500 MHz is listed as shown in the Table 4.1. As indicated the impedances has minimum reactance value (or can be neglected for sake of simplicity) and the real part can be approximated to 12 Ω in function of wide frequency. Good correlation (between

simulations CAD versus load pull measurement) of the load impedance data is established.

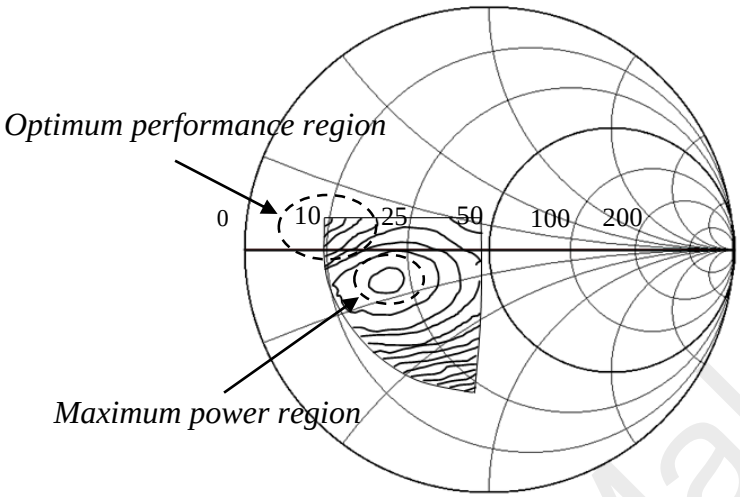


Figure 4.2: The measured results of load pull impedance contour at 1GHz. For an optimum power performance, we obtained 12 Ω approximately.

Table 4.1: Load pull impedance determination for the 3-stage DPA

Frequency, *f* **(MHz)**	**Impedance, *Z*** **(Ω)**	**Power, *P*** **(dBm)**	**Efficiency, *η*** **(%)**
100	12 + j1.8	42.3	44.6
500	12 + j4.3	41.8	44.2
1000	11.4 + j2.3	41.5	43.8
1500	12.3 + j2.3	41.3	40.5
2000	12.4 – j1.4	38.8	34.5
2500	12.7 – j3.2	24.5	31.8

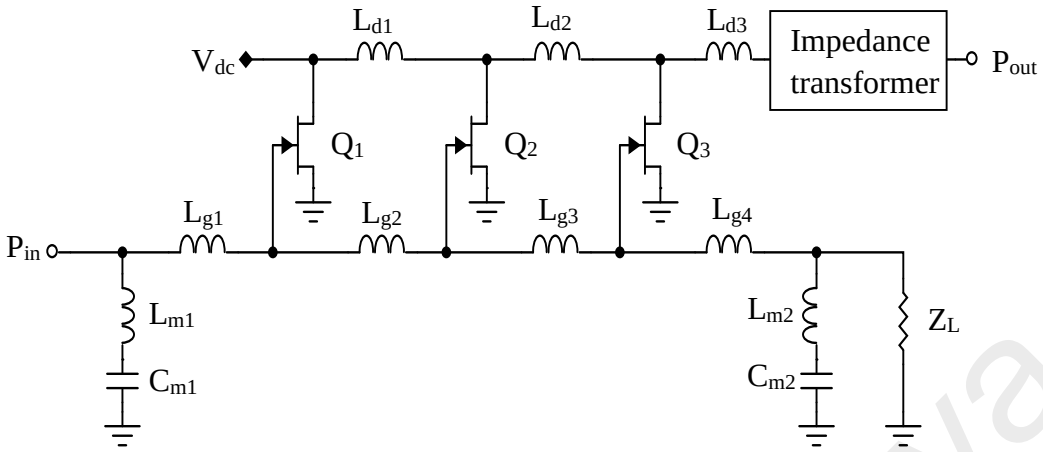


Figure 4.3: Simplified circuit diagram of the DPA with integration of the proposed impedance transformer.

In the following section, a novel technique to design broadband impedance transformer is discussed. This is a method of transforming optimum impedance of the 3-stage DPA 12 Ω to 50 Ω termination over the wide band operation. Simplified design of the 3-stage high power DPA with broadband impedance transformer is given in Figure 4.3 above.

4.3 Impedance Transformer Design Principle

In this section, a general principle of transformer design is discussed. Our design opt over a range of 100 MHz to 2400MHz to transform 12 Ω to 50 Ω. Hence, several design methods (Dennler, Schwantuschke, Quay, & Ambacher, 2012; Wang, Fischer, Oever, Korden, & Weigel, 2011) are explored, such as design with the multiple power modes and ultra-wideband power transfer networks. However, these occupying big size area; employing distributed elements and no freedom to optimize in board level. Thence, this work utilizing the mixed-lumped element to enable smaller area consumption of the board and lower cost product implementation.

The RFT is employed to solve the analytic problems in DPA design. Especially to simplify the process of loss less two-ports construction for a preassigned gain

performance (Aridas, Yarman, & Chacko, 2014; Carlin, Apr. 1977; Dai et al., 2015; H. J. C. a. B. S. Yarman, Jan. 1983; S. Yarman, 1982.). The impedance transformer network is express in terms of its Darlington's driving point impedance

$$Z_B(p) = \frac{N(p)}{D(p)} \tag{4.3}$$

where $p = \sigma + j\omega$ is the complex variable.

and in general, any real positive real impedance can be expressed as

$$Z_B(p) = Z_M(p) + Z_F(p) \tag{4.4}$$

In this representation, $Z_M(p)$ is a minimum reactance function which is free of Right Half Plane (RHP) and on the $j\omega$ axis it is expressed as

$$Z_M(j\omega) = R_M(\omega^2) + jX_M(\omega) \tag{4.5}$$

. Whereas the $Z_F(j\omega)$ represents a Foster function which is selected as

$$Z_F(j\omega) = jX_F(\omega) \tag{4.6}$$

Such that $X_F(\omega) = -\frac{1}{C_{n+1}\cdot\omega}$. Typically, C_{n+1} is necessary to perform as a DC block capacitor that placed along with the impedance transformer to block the DC signal over the wide frequency range.

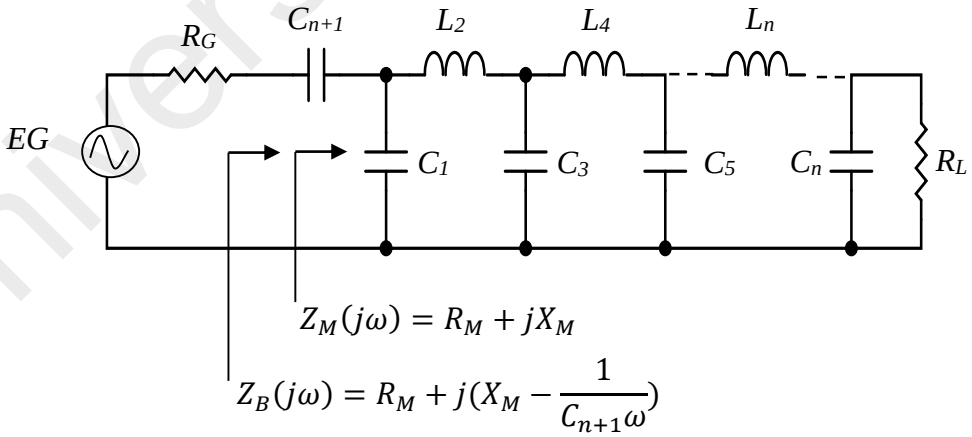


Figure 4.4: Circuit Topology which is dictated by the real part of the positive real impedance Z_B.

The optimization of the impedance transformer is based on transducer power gain (TPG) is given by

$$TPG(\omega) = \frac{4R_M R_L}{(R_M + R_L)2 + (X_M + X_F + X_L)^2}. \quad (4.7)$$

The frequency band is determined as $B(\omega) = \omega_2 - \omega_1$ over a specified angular frequency, ideally, $TPG(\omega) = 1$, otherwise it is zero. Thus, within the passband, let us define an error function $\varepsilon(\omega)$ such that over the band of operation $\omega_1 \leq \omega \leq \omega_2$,

$$\varepsilon(\omega) = (R_M - R_L)^2 + (X_M + X_F + X_L)^2 \geq 0. \quad (4.8)$$

Synthesis of (9) yields a low pass *LC* ladder as shown in Figure 4.4. It is noted that the *LC* ladder starts with a shunt capacitor C_1 since $Z_M(p)$ is a minimum reactants function. Relying on the value of integer "*n*", the last component was either a capacitor C_n ("*n*" = odd case) or an inductor L_n ("*n*" = even case).

Actual frequencies may be normalized with respect to upper edge of the frequency pass band. Hence, f_o is selected as f_o = 2.4 GHz. After the optimization, the polynomials $a(p) = [a_1\ a_2\ a_3\ a_n\ a_{n+1}]$ and $b(p) = [b_1\ b_2\ b_3\ b_n\ b_{n+1}]$ are determined. Then, $Z_M(p) = a(p)/b(p)$ is synthesized and eventually, resulting transducer power gain (TPG) in dB and the impedance transformer circuit with optimized element values are printed as a loss less *LC* ladder in unit termination. The admittance $Y_M(p)$ is given as

$$Y_M(p) = C_1 p + \cfrac{1}{L_2 p + \cfrac{1}{C_3 p + \cfrac{1}{L_4 p + \cfrac{1}{C_5 p + 1}}}}, \quad (4.9)$$

with C_1 = 0.6061; L_2 = 0.7029; C_3 = 2.870; L_4 = 1.165e; C_5 = 1.549e; R_L = 1.00.

Actual capacitors are given by $C_{iA} = C_{iN}/2\pi f_o R_o$; similarly, actual inductors are given by $L_{iA} = L_{iN}R_o/2\pi f_o$ where C_{iN} and L_{iN} represent the normalized values of capacitors

and inductors respectively. Normalization numbers are specified as $R_o = 50\ \Omega$ and $f_o = 2.4$ GHz.

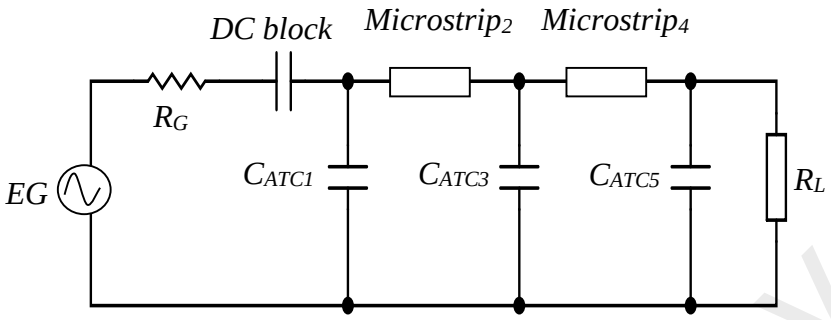


Figure 4.5: Circuit with practical implementation of micropstrip transmission line, high Q capacitors and DC block.

The inductors which obtained from the optimization above are realized with microstrip transmission line, where the signal and ground currents are on the same layer. The conversion of inductance to microstrip transmission line process is synthesized with the concern of printed circuit board (PCB) properties such as the dielectric substrate thickness, copper trace thickness, and signal trace of width. Moreover, the attenuation of the line and characteristic impedance also take into conversion consideration. Besides, the capacitors (ATC 100A series high Q) are used to enable board level optimization. The resulting circuit diagram with practical implementation as mentioned above has depicted in Figure 4.5.

The following section has shown the comparison of TPG performance between ideal and practical cases in Figure 4.6. The TPG results of the practical design are acceptable over the entire frequency range significantly and the result has shown reasonable agreement with the ideal result.

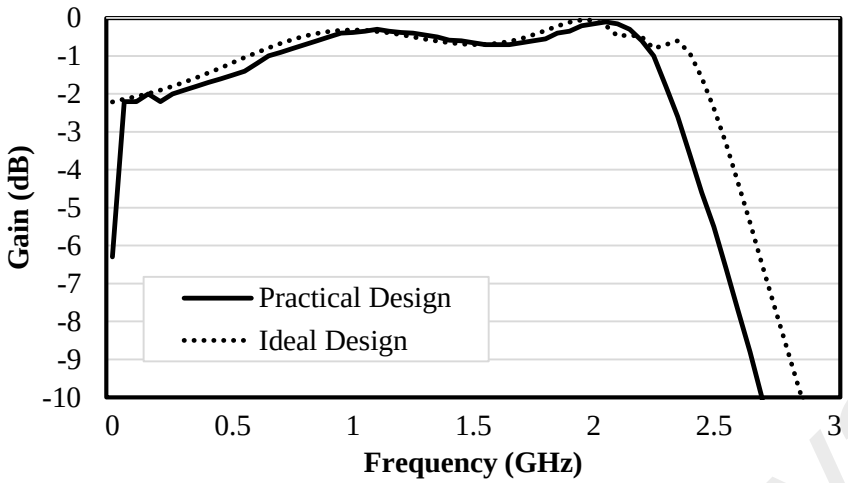


Figure 4.6: TPG results over the wide frequency operation range for practical and ideal design respectively.

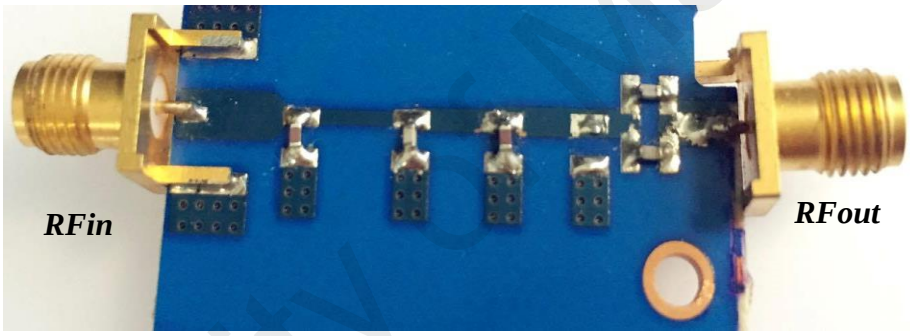


Figure 4.7: Prototype board of the impedance transformer.

In order to experimentally validate the impedance transformer and the board level, the prototype board was designed and fabricated as shown in Figure 4.7. The size of the broadband impedance transformer is 37 mm x 21 mm, where the inductors were realized by using high characteristic impedance transmission line trace on board as microstrip line with top metal thickness of 2 oz with gold plating for high power manipulation precondition beyond 30 W. PCB (standard RO4350B laminates) with dielectric constant (3.66), and the board thickness (0.762 mm) is used in this work. For getting better accuracy of the design, inductors were modelled by employing the computer simulation technology (CST), in which PCB properties were included. With CST platform, it enables the optimization of Q-factor and inductance values to produce flat gain response over the band of interest.

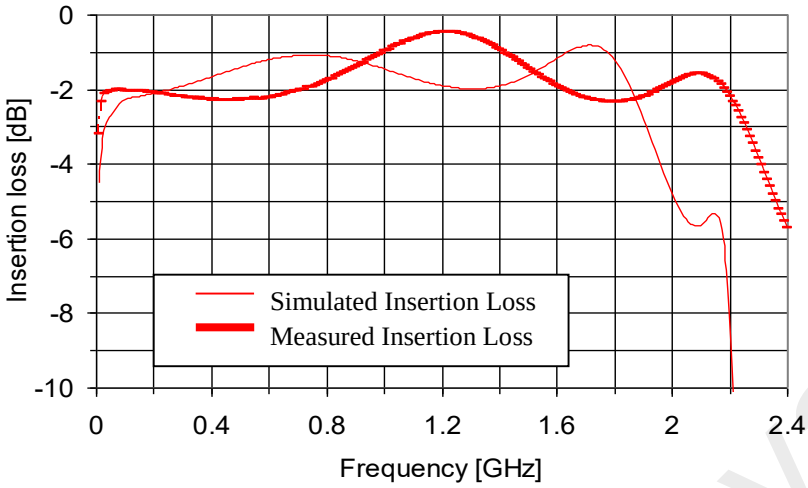


Figure 4.8: Insertion loss graph in dB depicted the simulated vs. measured performance of the broadband impedance transformer.

In Figure 4.8 the graph corresponds the loss of signal power in a transmission line. This insertion loss is simulated with the microstrip and discrete high Q capacitors, whereas the measured result is to measure TPG response in dB. In case of extra loss, the insertion loss is defined to be positive, for the simulated result shows ideal performance up to 2.2 GHz with low intrinsic loss, for measured result illustrated some extra loss at 1.2 GHz but bandwidth is up to 2.4 GHz however the overall insertion loss showing good correlation. All the above computations were done using CST platform and interfaced with network analyzer. According to the measured TPG in the pass band, there is -1.1dB gain with ±0.9 dB fluctuations. Hence, the measurement performance indicated good trend with the simulation results this is due to further optimization has been carried out during measurement process with realization of microstrip line. Additionally, the usage of discrete lump inductors has insignificant change to the gain performance within the pass band, nonetheless, suppresses the harmonics in the stop band as they should do. The measured result is done comparison with the lumped transmission line as illustrated by the simulated results.

4.4 Measurement Results of Full DPA Line Up

As in Figure 4.9 illustrates the design circuit of the novel DPA approach with non-uniform gate line, where the two non-identical high- f_t transistors (ATF54143 and ATF511P8 from Avago Inc.) are cascaded to the GaN transistor (CGH40010F from CREE Inc.) and with inter-stage tapered impedance (Narendra & Grebennikov, 2015).

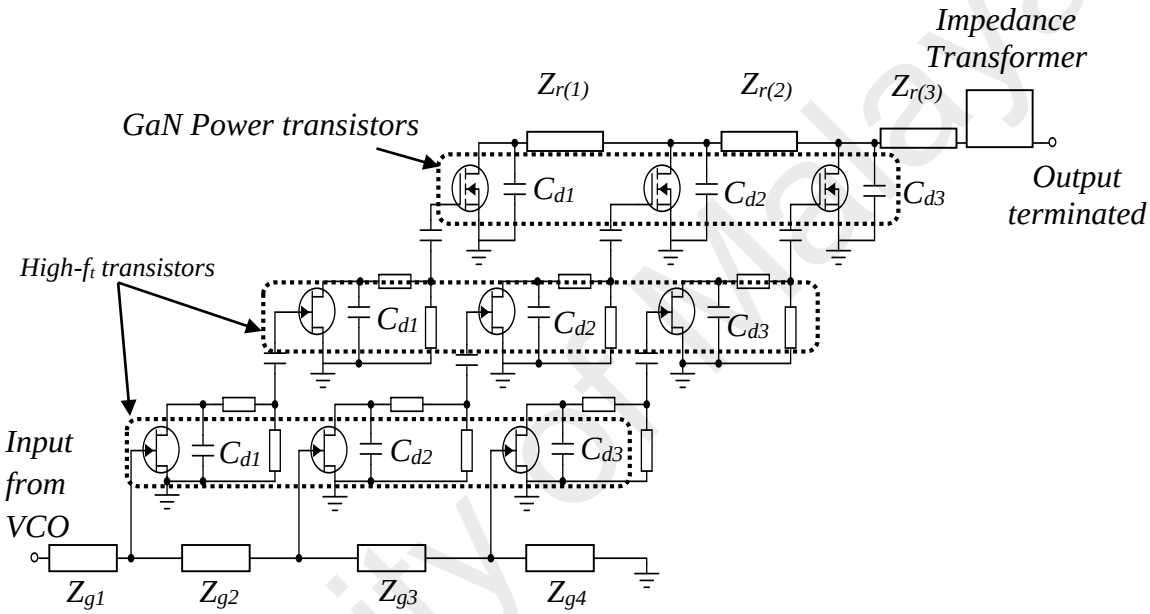


Figure 4.9: New DPA design schematic with non-uniform gate line is adopted.

The prototype board of full DPA design with integration of the impedance transformer was developed and fabricated as shown in Figure 4.10. Refer to Figure 4.10 the total board size is 87.5mm x 95mm uses the similar PCB properties as the broadband transformer impedance highlighted in previous section. This board working best over high frequency operations, therefore the adequate via-holes, diameter size and the spacing between them is taking into consideration to deliver a good electrical grounding for the shunt capacitors. The diameter size of the via-holes was created in 0.5mm with the gap of 1mm between holes, which enables the surface mounted device's grounding from the top layer connect to the bottom layer. Open grounding area with via-hole and DC/RF

routing is well isolated in PCB for minimum spurious. The screws diameter of 4.5mm is mounted to support grounded heat-sink chassis.

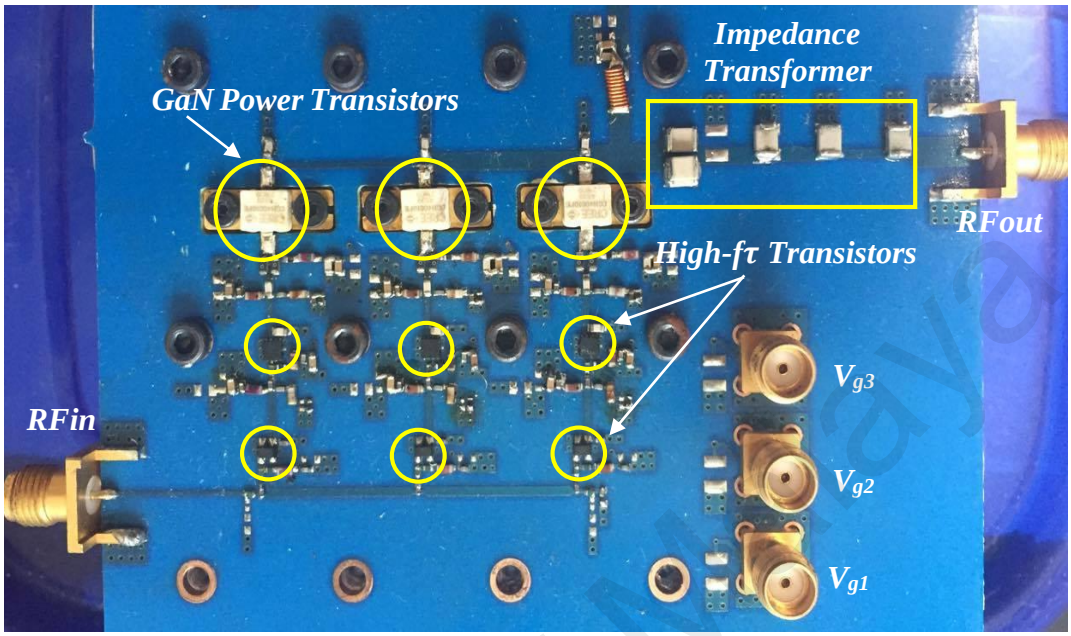


Figure 4.10: Actual prototype board of the full DPA line up.

By looking into the lumped transmission line in Figure 4.10, it's been realized from the inductance of the gate and drain lines with the assistance of full wave EM (electromagnetic) simulator. On the other hand, the DC gate biasing terminals are bypassed to the ground with multiple chip capacitors 100pF, 33nF and 10uF respectively for each of the power transistor. At the final stage there is high Q air-wound coil used as the RF choke, inevitably it has the ability to perform at high frequencies and they are free from energy losses. Whereas for the DC feed lines, the high Q chip inductors are applied for first and second stage respectively to block the AC while allowing DC to pass. The voltage supply to the high-f_t transistors is 5.5 V and 28V for the GaN power transistors. As a results, the high-f_t transistors are biased with I_{dq}=34 mA (20% I_{dss}) and I_{dq}=93 mA (14% I_{dss}), while the GaN power transistor with I_{dq}=278 mA (4% I_{dss}). The input drive throughout the measurement is fixed to ~3 dBm from the voltage-controlled oscillator.

The high-f_t transistor being lower input parasitic capacitance C_{gs} is connected to the gate line. Certainly this minimizes the loading behaviour at the input gate line. Such

a high gain at frequency up to 2.4 GHz (Cripps, 2006), enables the DPA to directly connected to the VCO. However, the effective input capacitance of the first high-f_t transistor C_{in} and effective output capacitance of the power transistor C_{out} are important to define f_c. C_{in} of the first high-f_t transistor and C_{out} of the power transistor are lower than 3 pF, which provides a 2.2 GHz with a 50 Ω load. Accordingly, effective gate and drain line elements, i.e. L_i, are synthesized by means of (9) to achieve the desired f_c.

$$f_c = \frac{1}{\pi\sqrt{L_i C_{opt,i}}} \quad . \tag{4.10}$$

Measurement characterization of the power performance including output power and gain are recorded experimentally, refer to Figure 4.11. Approximately 10 W output power and gain of 30 dB are achieved across the bandwidth. PAE about average 35 % and DC current of 1.3 A at average are obtained over the entire frequency range.

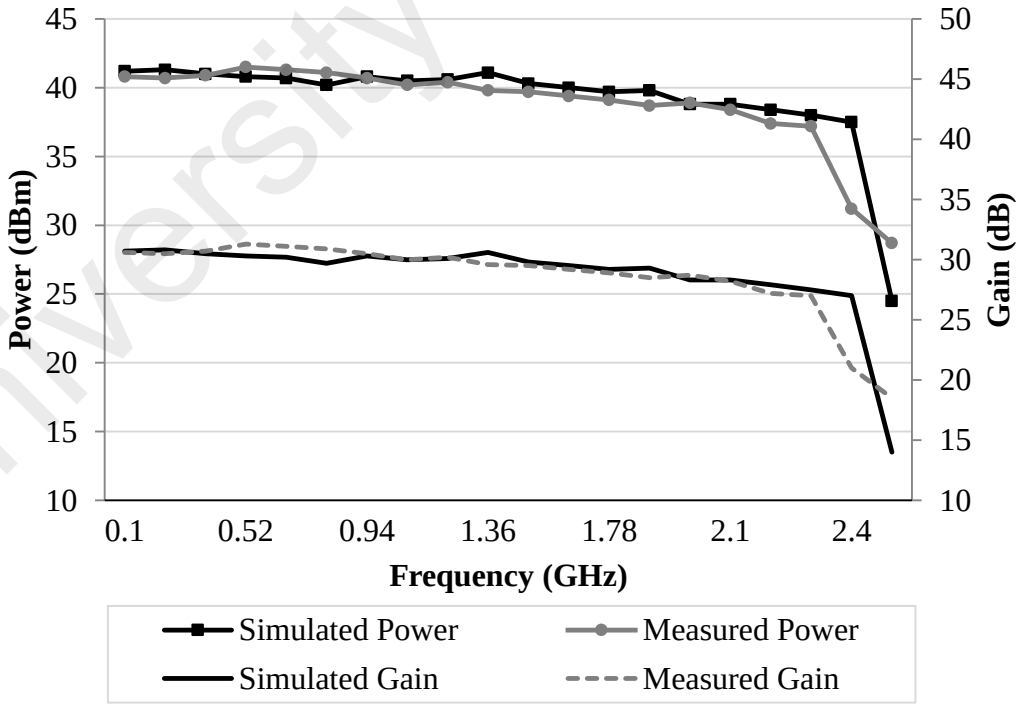


Figure 4.11: Measured vs. simulated of the power performance (output power and gain) of the DPA topology over the entire bandwidth.

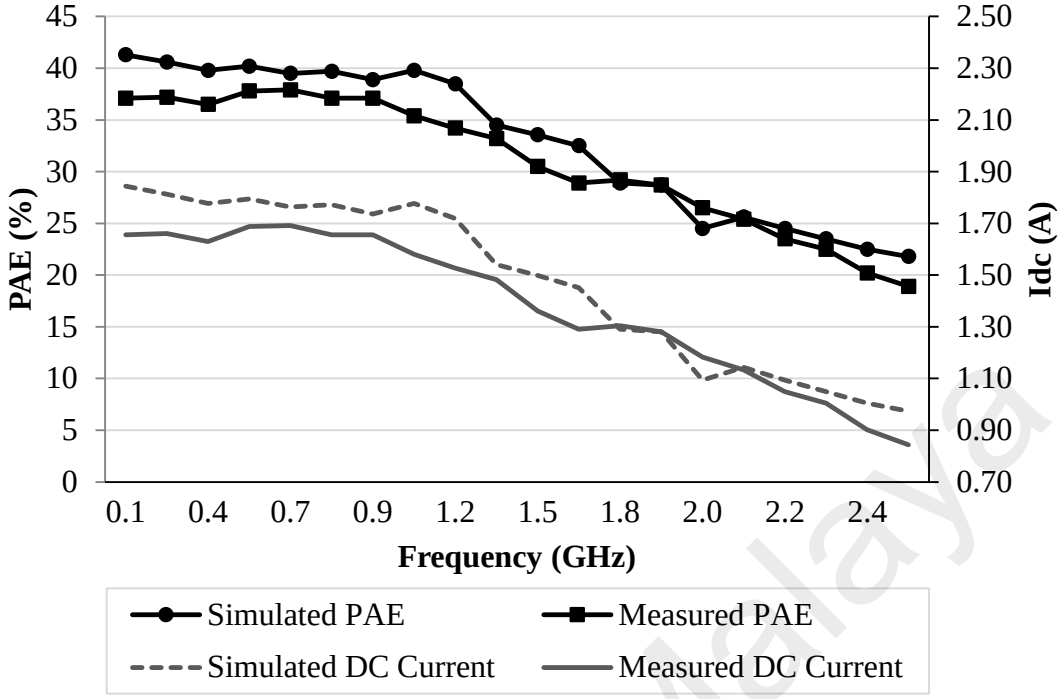


Figure 4.12: Measured vs. simulated efficiency and total DC current of the DPA topology over the entire bandwidth.

This work demonstrated good performance such as output power and efficiency up to 2.4 GHz which is an attractive for two-way mobile communication systems such as SDR applications.

Table 4.2: Comparison of State-of-Art performance.

References	Device Technology	Bandwidth [GHz]	Gain [dB]	Pout [dBm]	PAE [%]
(Lin, Fathy, et al., 2009)	GaN HEMT	0.02 – 3.5	13.4	37	27
(Narendra et al., 2012)	pHEMT + GaN HEMT	0.04 – 2.0	33	41	35
(Kim et al., 2014)	GaN HEMT	0.1 – 2.7	12	37	40
(Mughal, Kashif, Cheema, Imran, & Azam, 2015)	GaN HEMT	0.15 – 0.5	2.5	37	67
This work	**pHEMT + GaN HEMT**	**0.1 – 2.4**	**30**	**40**	**35**

The summary of the DPAs power performance up to 2 – 3 GHz frequency is tabulated in Table 4.1 and compared with the recent advanced DPA works. Other research works with distributive power amplifier approaches can be found in references. Meanwhile, a greater output power and higher efficiency were developed by (Narendra et al., 2012). In addition, this implementation of the hybrid PCB has higher power capability, lower cost and faster turnaround, which is suitable for low-frequency operation and higher current applications. However, this work has achieved higher output power with extended bandwidth and low cost implementation technology.

CHAPTER 5: DPA GATE LINE IMPEDANCE ADJUSTMENT

5.1 Introduction

In this chapter, the performance of second DPA design with gate line termination adjustment network and tapered drain line approach has been discussed. The reviews from the conventional DPA topology and the limitation on its efficiency has been analyzed as design guideline. In the last three decades, (Ayasli et al., 1982) have published design formulas for the gain of traveling-wave amplifier based on an approach that approximates gate and drain lines as continuous structure. Besides, (Beyer et al., 1984) have created a closed-form expression for the gain efficiency that relying on the cut off frequency at the gate line and the schematic propagation constants. According to (Olson et al., 2007) this research shows the drain line tapering method has erased the reverse signal at the drain line and obtains suitable characteristic impedance. Similarly, (Gassmann, 2007) has applied tapering drain line concept and demonstrated an amplifier having the output power and gain of 5.5 W and 7 dB respectively. The circuit was operating in the frequency range from 2 GHz to 15 GHz.

Nowadays, the latest benchmarks of the DPA development is the usage of GaN HEMT technology, the introduction of field-plate technique to GaN HEMTs resulted in lower parasitic capacitances and other benefits as presented by many past researchers (D. G. Tas, 2012; R. Santhakumar et al., 2011; van Raay et al., 2015). Therefore, the impact of this thesis is to enhance the efficiency as high as possible and meet the optimum performance in the wide-band at the range of 100 MHz to 2.4 GHz based with GaN HEMT technology.

Lastly, the new design of 3-stage DPA has been experimentally validated at simulation and measurement level. The results comparison and findings has been made

throughout the design process and has given a good agreement on efficiency enhancement.

5.2 Review of Conventional Topology and the Limitation on Efficiency

Firstly, the conventional distributed amplifier constructed in ADS as shown in Figure 5.1. This conventional DPA is drove by three units of power transistor device with GaN HEMT technology. Impedance matching and m-derived were used and it is mentioned in Chapter 3 to compute the overall system and each of the lumped elements in the circuit can be tune accordingly to obtain a better performance for overall system. The nonlinear analysis such as harmonic balance of the DPA making use of the non-linear active device model and passive components models is performed.

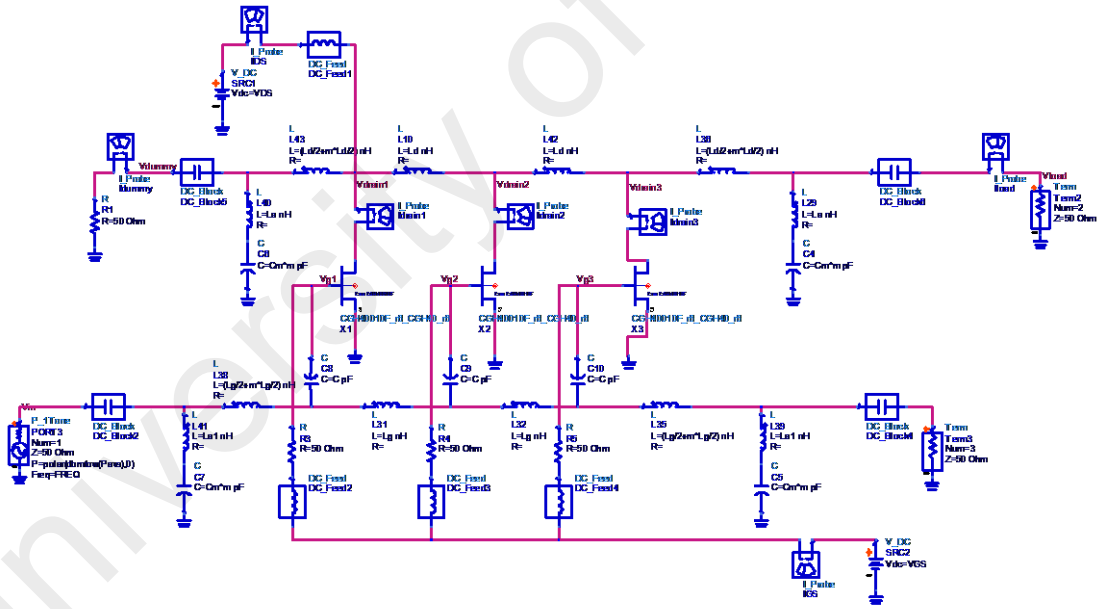


Figure 5.1: Schematic of conventional 3-stage DPA in ADS.

As the power performance of this conventional DPA (refer to Figure 5.2 and Figure 5.3), the output power of ~10 W, gain of 10 ± 1 dB, and PAE of average 30 % are achieved in the frequency range of 100 MHz to 2.7 GHz, beyond 2.5 GHz the output power is dropped tremendously which does not fit to 10 W (40 dBm) applications. The

DC biasing scheme for this conventional DPA was set at VGS = - 2.4 V, and VDS = 28 V and same Pavs = 29 dBm is applied.

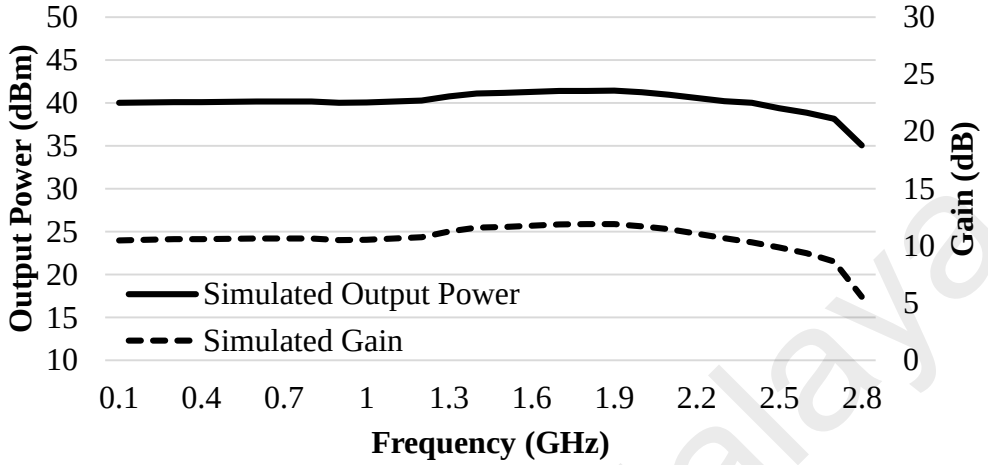


Figure 5.2: Simulated power performance (output power and gain) of the convention DPA topology over the entire bandwidth.

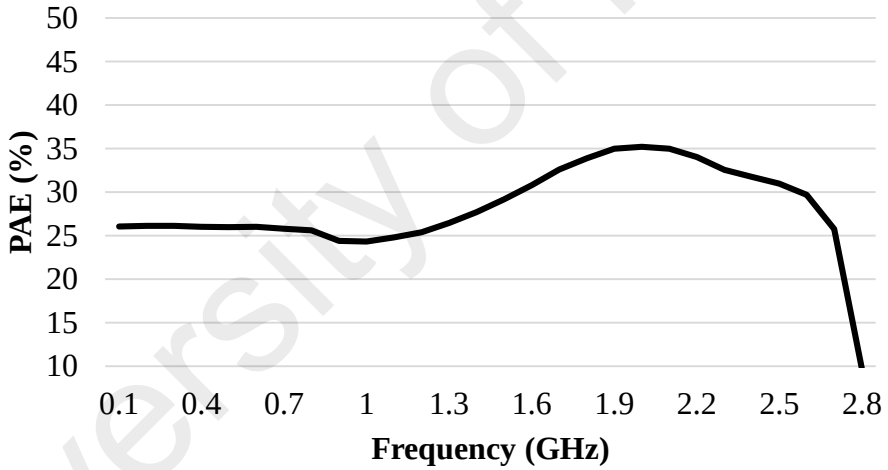


Figure 5.3: Simulated power efficiency of the conventional DPA topology.

As a guideline from the conventional DPA topology, the overall system has been modified for further enhancement on the power efficiency while maintaining in flat gain and broadband by implement the impedance termination adjustment network topology and drain line tapering method.

5.3 Gate Line Impedance Adjustment Network Topology

As we understand from previous sub-topic, the need to improve efficiency is essential, whereby we look into gate line impedance adjustment which new in principle. Gate line of a DPA act as back bone for the whole system. In previous topic, a conventional 50 Ω gate line network is constructed from the impedance matching and M-derived. Why 50 Ω? The 50 Ω is basically conventional standards. This standard is a great compromise between minimum loss and maximum power handling, for air-dielectric coax during World War II work on radar. The impedance of coax for a given outer diameter and dielectric is solely a function of the diameter of the inner conductor and the dielectric constant of the filler material:

$$Z_o = \frac{138}{\sqrt{\varepsilon_R}} \log\left(\frac{D}{d}\right) \tag{5.1}$$

Based on this equation, the loss versus characteristic impedance graph is plotted in Figure 5.4 (a). Assuming $\varepsilon_R = 1$ for any cable as air dielectric, the minimum insertion loss obtained at around 77 Ω. In Figure 5.4 (b) shows 30 Ω is the best peak power handling.

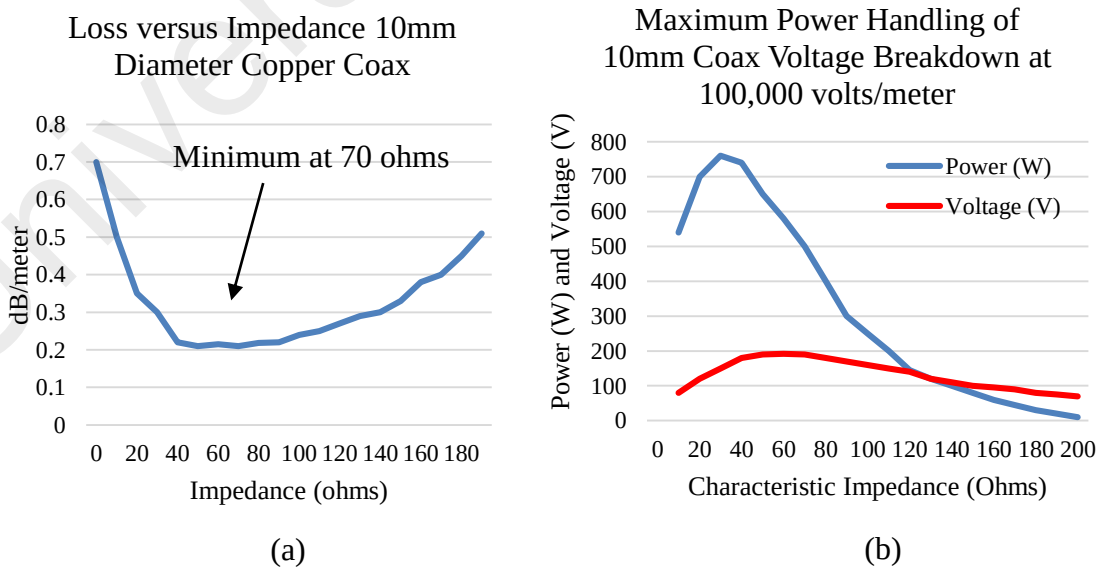


Figure 5.4: Graph of insertion loss (a) and power handling (b) versus characteristic impedance of a 10 mm diameter coax. (A. S. Gilmour, 1930)

As information, (A. S. Gilmour, 1930) claims that the peak power handling for air coax is limited by voltage breakdown as opposed to hearing effects which limit the average power handling. The arithmetic mean between 30 Ω as the best power handling, and 77 Ω has the lowest loss, the geometric mean is 48 Ω. Thus, the choice of 50 Ω is a compromise between power handling capability and signal loss per unit length, for air dielectric.

In Figure 5.5 represent the gate line adjustment network for this research. In conventional DPA, the impedance at the source and load was match with 50 Ω. Hence, we are trying to play tune of the impedances other than 50 Ω at the gate line to enhance power efficiency towards the drain, while the drain line we were applying drain line tapering method to boost more on the efficiency.

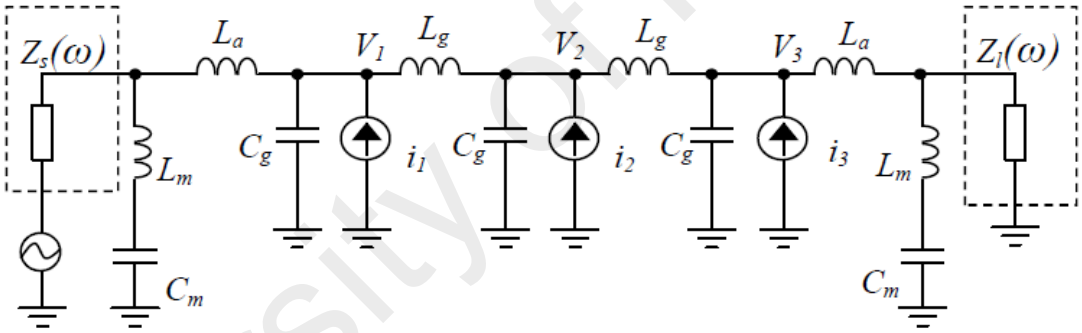


Figure 5.5: Gate line adjustment network.

This gate line is designed to acquire the behavior of the voltage gate as a function of frequency. The magnitude and phase will be analyzed in different value of impedance set. The purpose is to improve the gain efficiency by adjusting the impedance value at the both end ports while maintaining the structure of the circuit. Based on Figure. 5.5, Z_s represents the impedances at the source termination and Z_l as load termination which can be defined as the "equivalent Thevenin impedances".

$$Z_S(\omega) = R_S(\omega) \tag{5.2}$$

$$Z_l(\omega) = R_L(\omega) + jX_L(\omega) \tag{5.3}$$

The voltage V_n , n = 1,2,and 3 can be expressed as:

$$V_n = \frac{V_s}{\frac{R_l(\omega)+jX_l(\omega)}{Z_s\left(\frac{\omega}{\omega_c}\right)}+1} \tag{5.4}$$

The (ω/ω_c) is the normalized frequency, and the selection of the different set of impedances are in such a way that optimum $X_l(\omega)$ can be numerically determined for various $R_l(\omega)$ values. The input current i_n of each transistor at the gate line is injects with $g_m V_{gs}$ where V_{gs} refers to the source from the gate voltage.

The theory behind this gate line adjustment network is based on the phase coherent effects. Due to the fact that the phase delay changes with frequency, it is difficult to achieve the phase coherency for optimum current combining at each junction as shown in Figure 5.6. The further the location of the current source that closer to the load termination, the earlier the power degraded with respect to frequency, and at a certain frequency it absorbs power from the line such as negative impedance. The power delivery by each GaN device follows the real part of impedance. So, there is a strong peaking occurred at the closer the signal to ω_c, especially at the first and the last section.

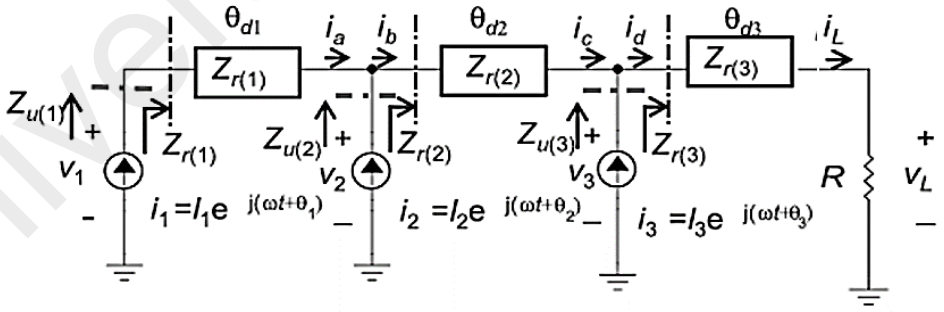


Figure 5.6: Phase coherency for optimum current combining at each junction.

(Narendra et al., 2008) emphasized that by using a nonuniform gate line design the phase velocity synchronization between gate and drain line can be achieved. A simple adjustment at the gate line impedances offers an efficiency enhancement, and the gate line termination load R are adaptively reduced at the simulation level. From the

simulation studies, the fact that gate line attenuation is more sensitive to frequency than the drain line attenuation is investigated, and the drain line attenuation does not vanish in the low frequency limit, unlike attenuation in the gate line. Therefore, the frequency response of the DPA can be expected to be predominantly controlled by the attenuation on the gate line.

5.4 Drain Line Tapering Effects

In order to compensate the results from the gate line impedance adjustment to allow FETs in the distributed network to drive unequally, the equal drive to each section of transistor can be restored by increasing the characteristic impedance of the gate line in a systematically tapered manner from the input to load termination. In a manner analogous to gate voltage equalization, the voltage at the drains of all the FETs can be made the same by tapering the drain line impedances, but alternate the impedances decreasing along the line toward the output load termination.

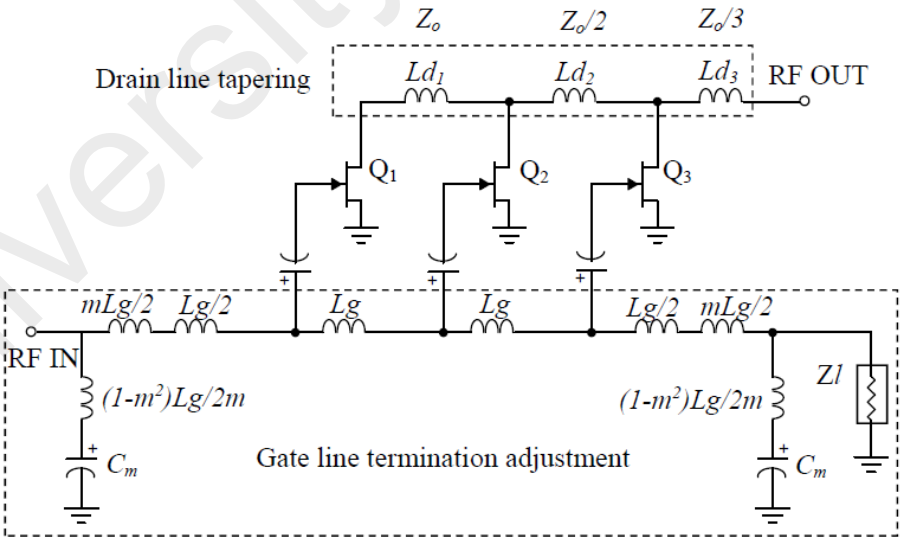


Figure 5.7: Gate line termination adjustment network with tapered drain line.

As mentioned in Chapter 2, tapered drain line of DPA eliminates the drain line reverse wave adopting a suitable tapering of the drain line impedance. The power

efficiency of the amplifier can be improved at the drain side by applying a tapered drain line technique which is significantly improved as compared to the conventional DPA topology.

The circuit diagram in Figure 5.7 illustrate that the first GaN device feeds a section with characteristic impedance Z_o, follow by second device feeds with $Z_o/2$ and last section with $Z_o/3$. With such attempts, the total GaN device output current at the drain line is force to feed in the forward direction only, whereas the reverse current will be canceled due to the reflection from the change of impedance at each section as described in Figure 5.8. Hence, the maximum output power is achieved from each cell of a GaN device.

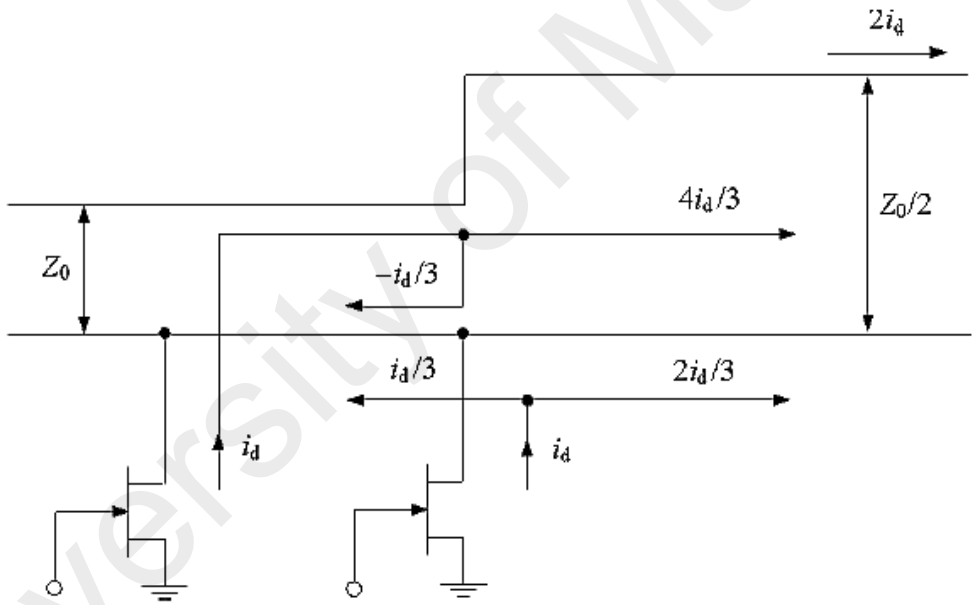


Figure 5.8: Current distribution in drain line tapering network.

The entire current of the GaN devices may effectively use in the load without the necessity of half the drain current flowing into the load and half drain current flowing into the reverse termination. Besides, the uniform current is hard to achieve in practical due to the unequal drive voltage on the gate line and the GaN device process variation, and there exists a small range of useful realizable impedances for microstrip line practical implementation.

5.5 Synthesize Input Matching Network employing RFT

As mentioned in Chapter 3, the detail review of matching network determination using RFT has been discussed. The input matching network for the 3-stage DPA is constructed with MATLAB function and obtained the value of inductance and capacitance for the matching as shown in Table 5.1.

Table 5.1: Optimized element values from MATLAB input matching network.

Element	Values
L_1	2.082 nH
L_2	4.315 nH
L_3	4.348 nH
C_1	2.886 pF
C_2	2.819 pF
C_3	1.317 pF
R_S	30 Ω

The transducer power gain performance is depicted in Figure 5.9. From TPG graph, the result obtained is satisfying, as the value of TPG is within the range of 0 to -1 dB. Added that, the similar input matching network in MATLAB is then transferred to ADS software as shown in Figure 5.10. The S-parameter simulation is carried out in the form of smith chart to observe the impedance of the network transform from 50 Ω to 30 Ω and TPG performance in ADS that illustrated in Figure 5.11.

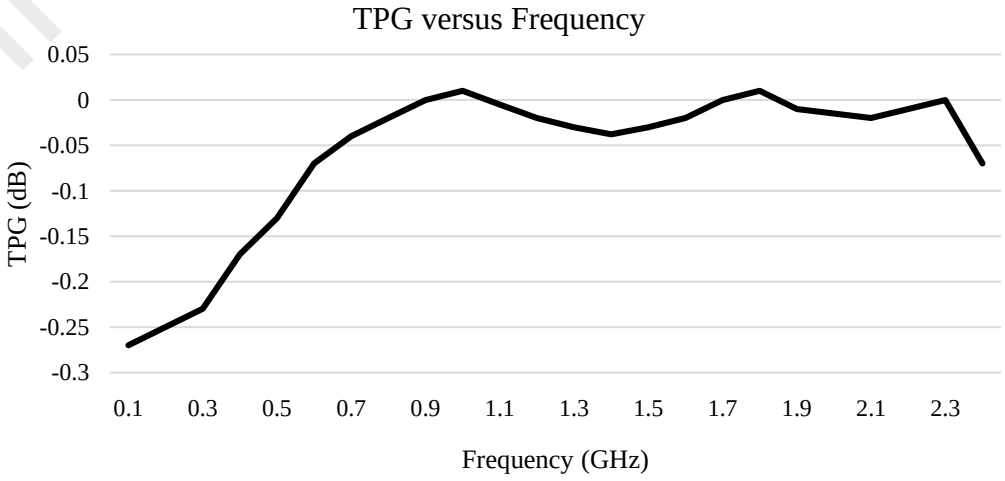


Figure 5.9: Result of TPG versus frequency for input matching network.

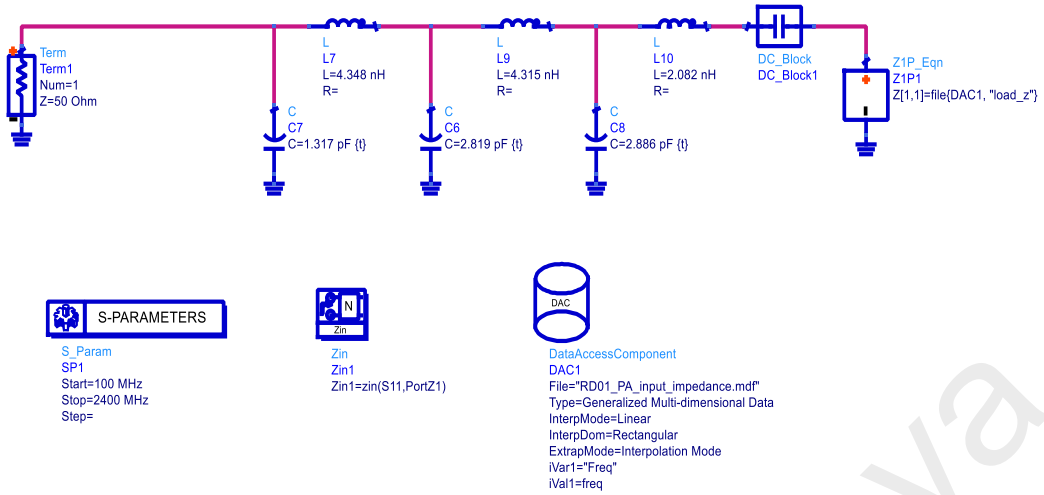


Figure 5.10: MATLAB input matching network constructed in ADS.

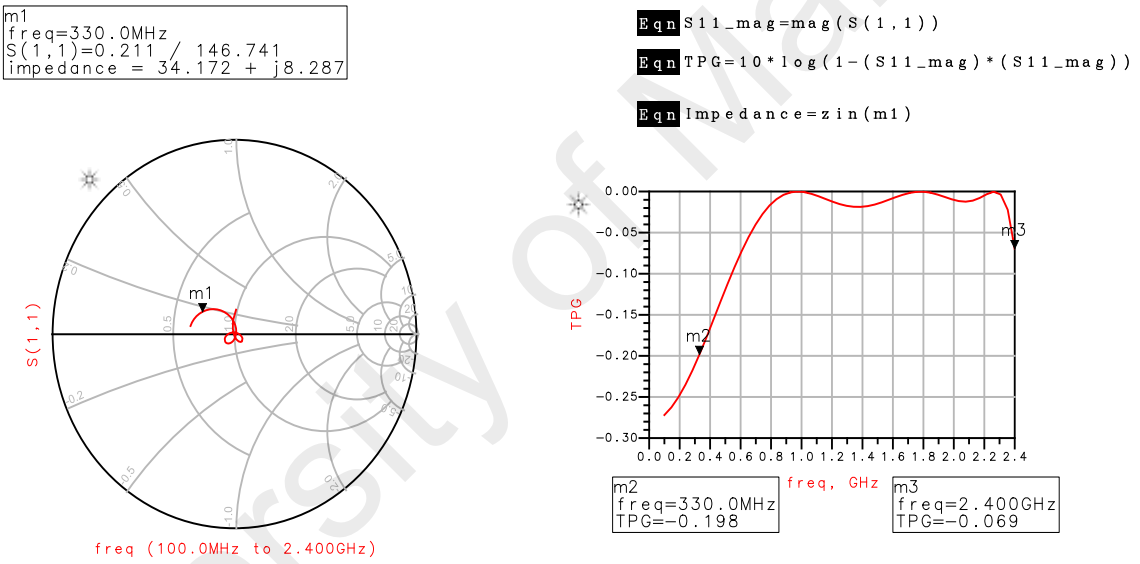


Figure 5.11: Input matching network simulation result in ADS.

In the above simulations are the crucial steps of the RFT. The simulation result obtained in ADS is very close to the MATLAB result. Where the impedance obtained after MATLAB optimization is 34.172 + j8.287 Ω that are close to 30 Ω. The overall performance still can be optimized from different parameters such as the value of capacitor, gate line impedance adjustment, and tapered drain line.

5.6 Measurement Results of 3-stage DPA

Ultimately, the gate line impedance adjustment network has implemented to the DPA circuit architecture, followed by the tapered drain line method and input matching network via RFT, the final schematic of modified 3-stage DPA is constructed in OrCAD software as depicted in Figure 5.12.

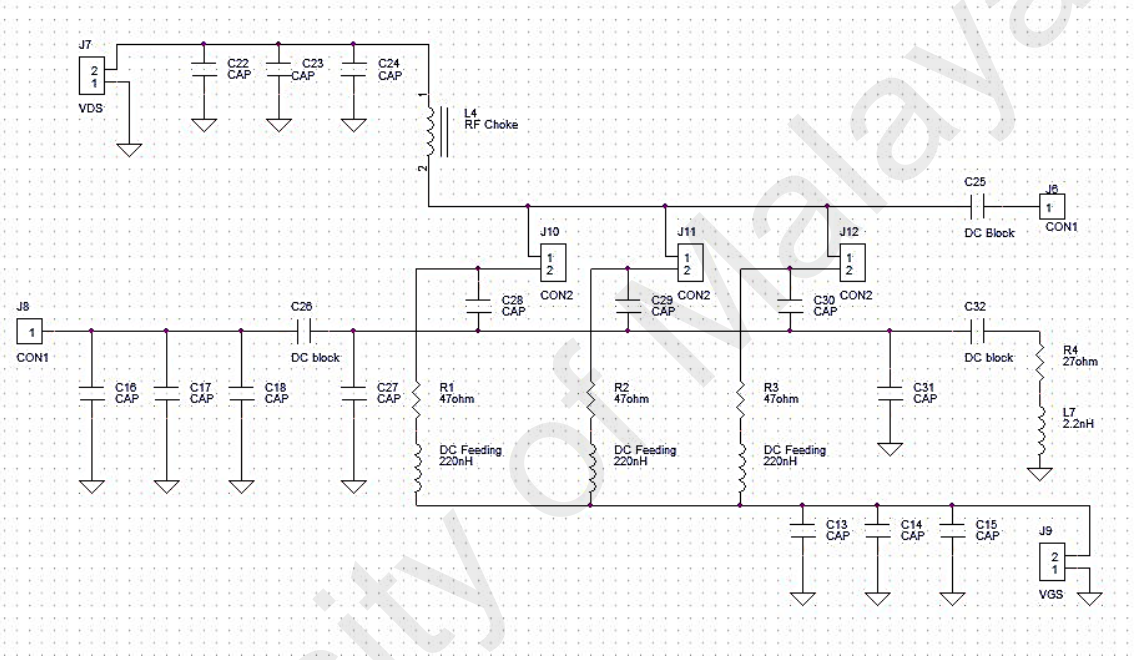


Figure 5.12 Schematic of modified 3-stage DPA that constructed using OrCAD 10.5 Capture CIS before converted to PCB layout.

This schematic has simulated in ADS software to observe and optimize the overall performance. The state-of-art power performance is achieved according to two-way radio communication standards. In Figure 5.13 shows the circuit constructed in ADS software, the 3-stage DPA is developed with microstrip implementation with industrial capacitors insertion (ATC 100A series capacitor).

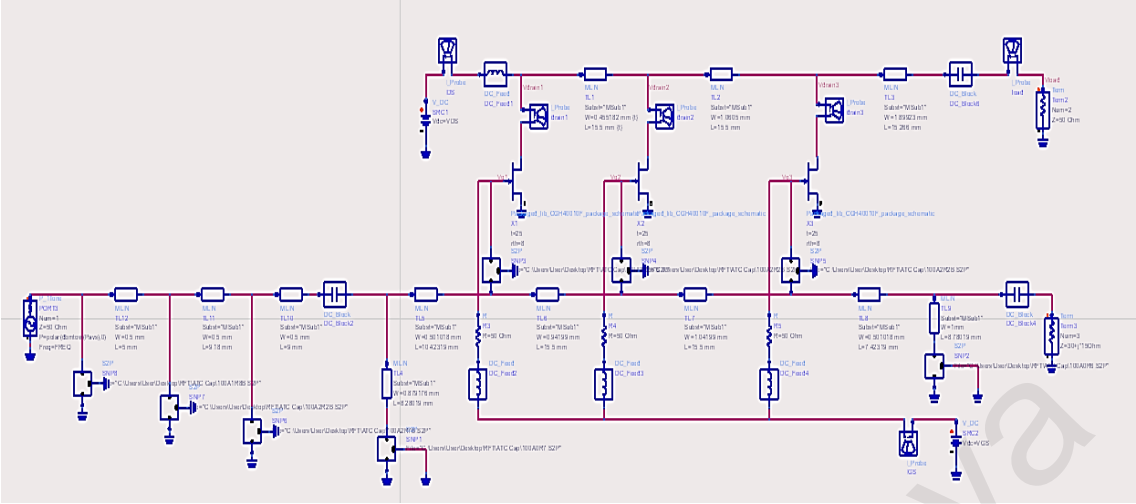


Figure 5.13: Circuit level schematic of 3-stage DPA system with microstrip implementation in ADS software simulation.

As in Figure 5.14, 5.15 and 5.16 represents the ADS optimized and simulated performance of the conventional and modified DPA before proceed to prototype fabrication. The DC biasing scheme at the same condition for both design, VGS = -2.96 V, VDS = 28 V at P_{in} = 29 dBm is applied. In Figure 5.14 display the flat gain of 10 ± 1 dB for both designs and the output power of modified DPA is slightly higher than the conventional at 40 ± 2 dBm, which is about 10 W of high output power in Figure 5.15. For the power efficiency of modified DPA has significantly growing almost 20% but majority 10% enhancement across the bandwidth (0.1 GHz to 2.7 GHz) can be observed in Figure 5.16 compared to conventional topology. Beyond 2.7 GHz the performance is degraded, however the result has achieved the design specification in ISM band. Practically, the operate bandwidth is narrower by using CST software. In order to simulate in CST software, the board's s-parameter measurement need to be extracted and transfer it to CST software to obtained an accurate realized DPA simulation data that are close to the experimental data. Due to the lack of software licensing, this design was simulated in ADS software only. However, this simulated results have given a good agreement on the methods applied with respect to conventional technique.

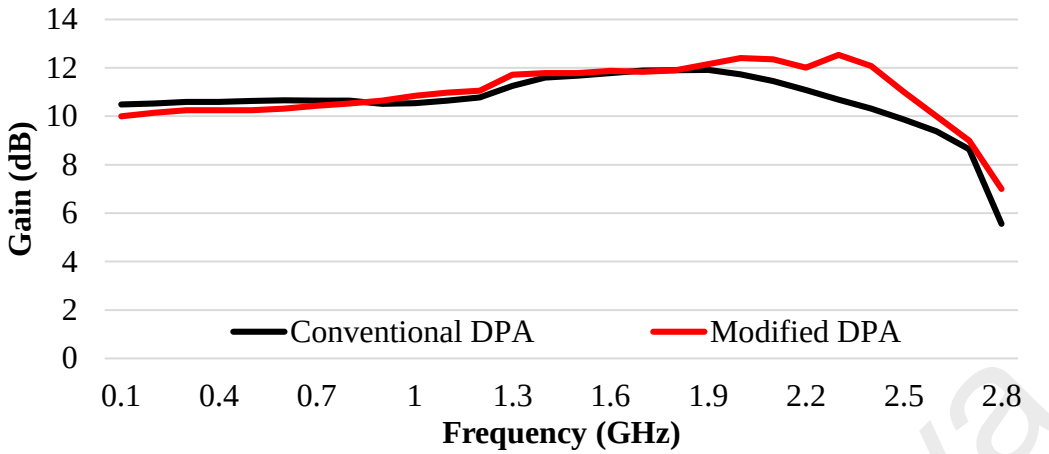


Figure 5.14: Simulated gain of conventional versus modified DPA.

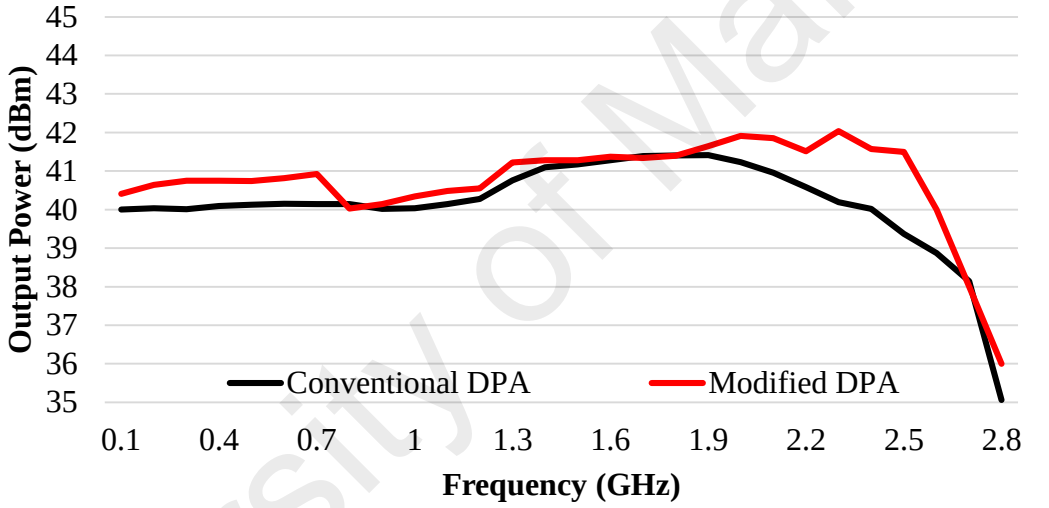


Figure 5.15: Simulated output power of conventional versus modified DPA.

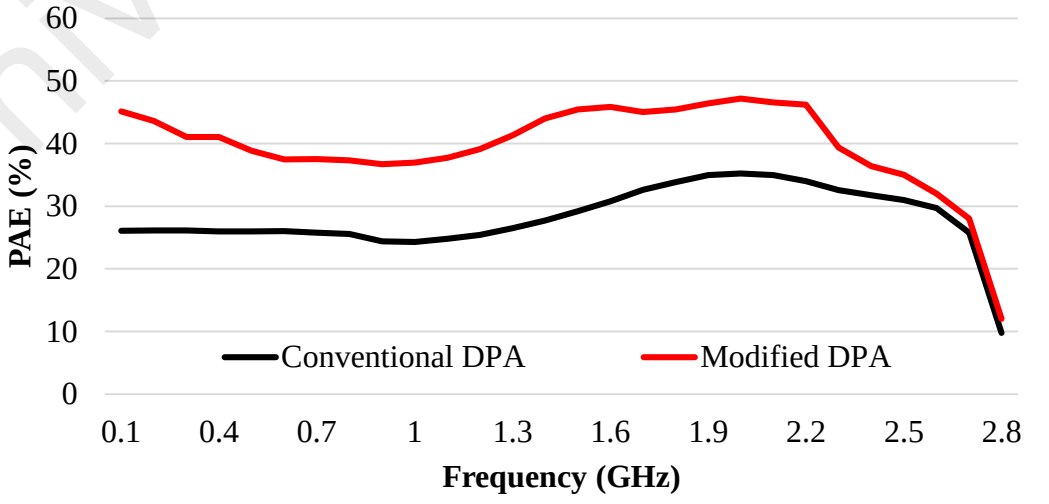


Figure 5.16: Simulated PAE of conventional versus modified DPA design.

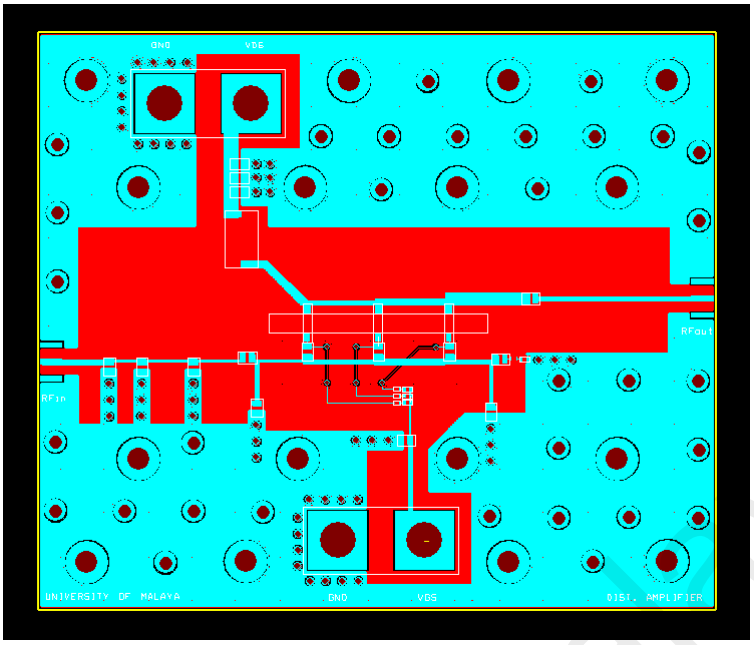


Figure 5.17: Final layout of the 3-stage DPA design used for fabrication.

Next, we proceed to the prototype layout drawing and fabrication in order to validate the circuit design experimentally. The total layout dimension is 148.2 mm x 126 mm as shown in Figure 5.17. The blue colored areas represent copper with solder mask protecting trace against oxidation, red is the second layer with bare substrate, lastly the maroon represents plated through holes. Finally, the fabrication is done in Figure 5.18.

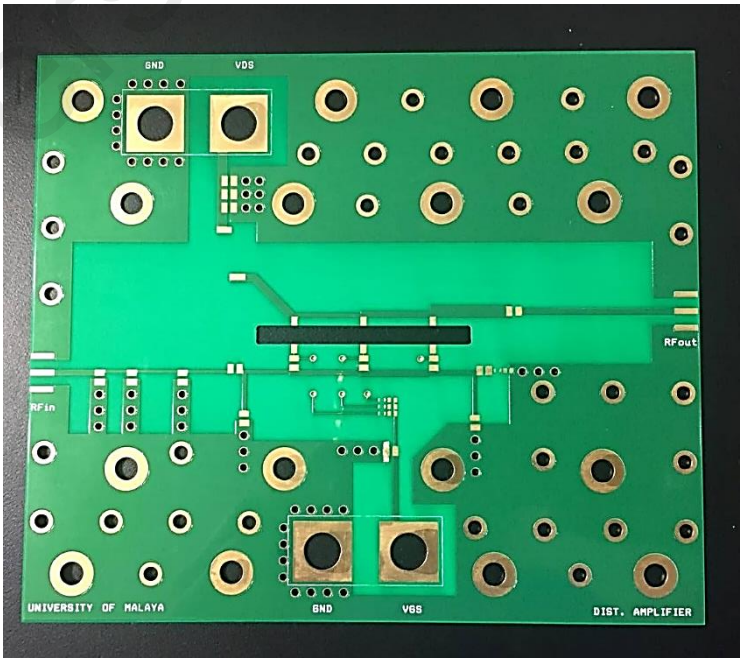


Figure 5.18: Prototype board fabricated for final 3-stage DPA.

Eventually, all the components are soldered on the prototype board as shown in Figure 5.19 and ready for power measurement and board testing. The overview of the test setup used during the power measurements can be viewed in Figure 5.20.

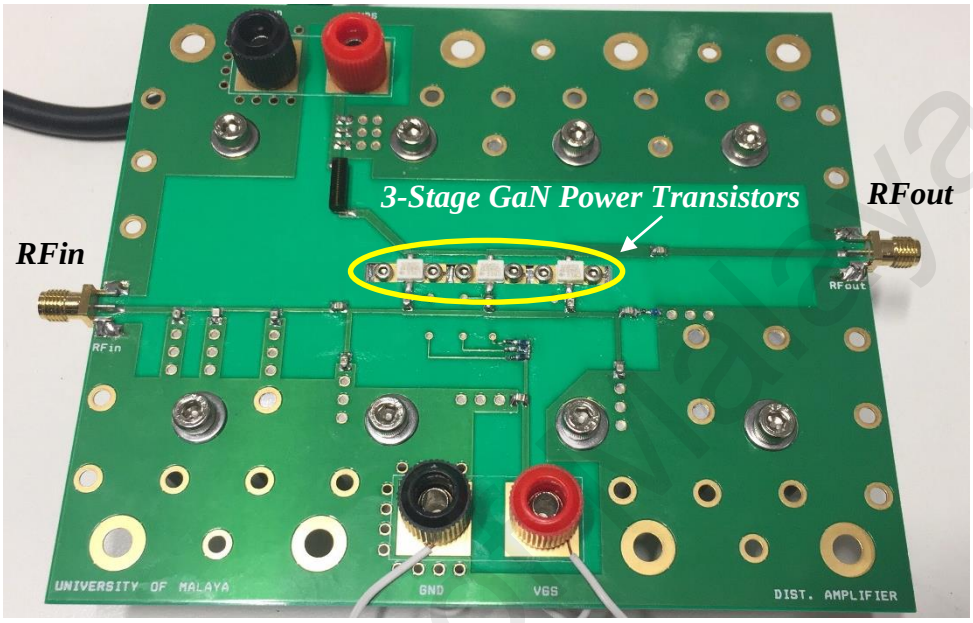


Figure 5.19: Realised 3-stage DPA prototype.

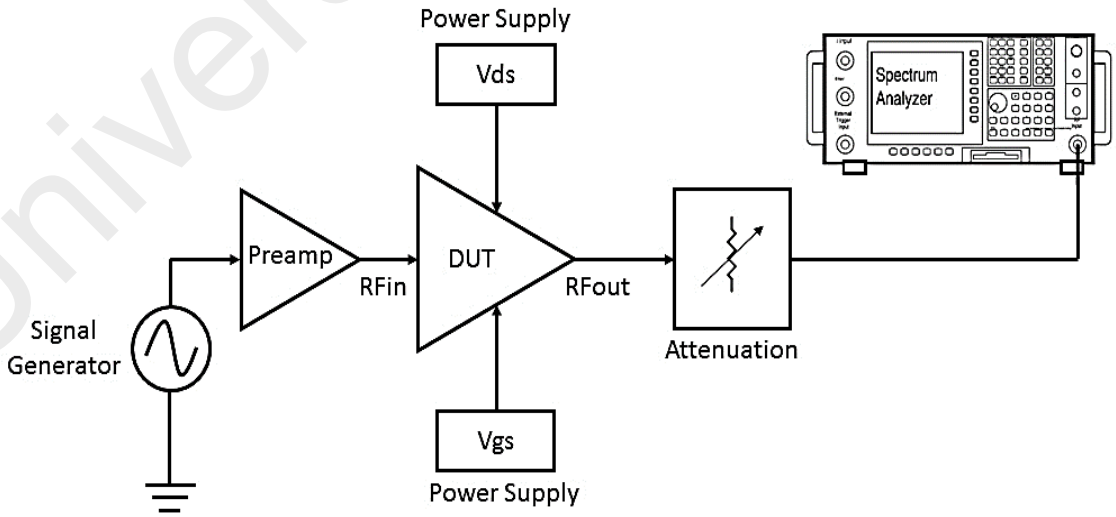


Figure 5.20: Overview of measurement setup for DPA power performance.

At first, the safety precautions need to be done before carry out experiment, as prevention is better than cure. In this case Electrostatic Discharge (ESD) precautions are needed, by wearing a protective the outer garments, and put ESD mat under the device under test, as the GaN HEMT transistor is a ESD sensitive materials and would cause damage if not handling in a proper way.

An actual measurement setup for the DPA prototype board is shown in Figure 5.21. The stability of the realized DPA prototype was tested and successfully passed the test by using a spectrum analyzer. Then power measurements across the desired bandwidth of 100 MHz to 2.4 GHz were performed with a RF input signal provided to the DPA RF input to keep the average power low and to reduce the thermal stress on the transistors. During the measurement, an RF signal generator created the high frequency input signal with an output signal of 25 dBm, as compared to simulation level, this signal generator has its limit to generate output signal, therefore a preamplifier is needed to boost the input signal before it reached the amplifier under test.

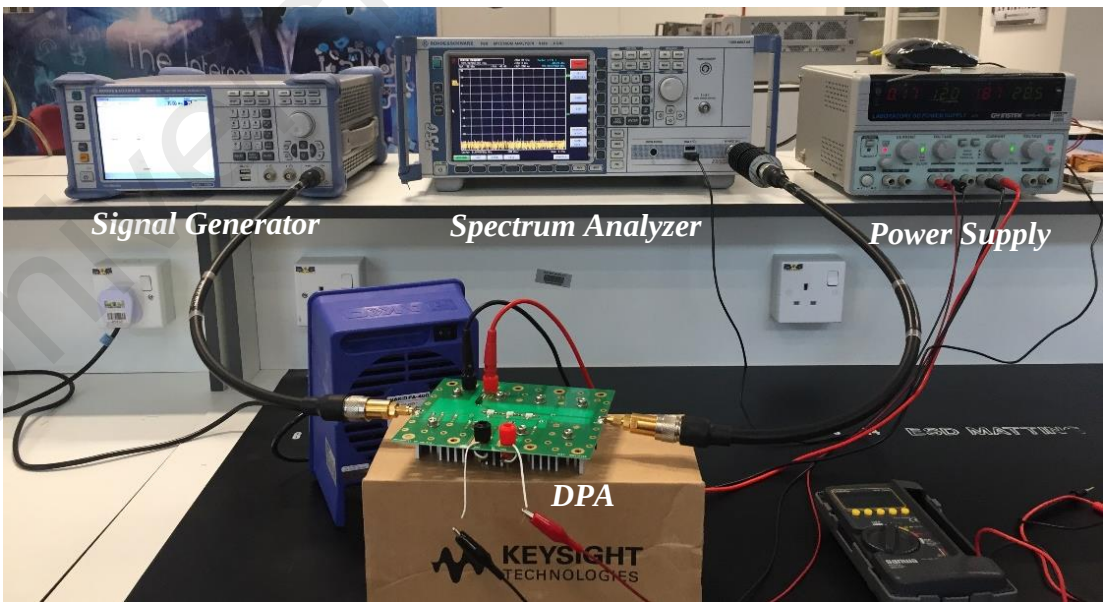


Figure 5.21: Actual measurement setup for DPA prototype board with measurement equipment available in Motorola Lab, UM.

Besides, the 30 dB loss attenuator were used to limit the output power of the DPA and protect the following instrument from over high power levels. A spectrum analyzer from Rohde & Schwarz company, was set to measure with zero span at the frequency of the input signal and the measurement marker is placed at the top of the pulse. An average of 100 samples were taken to smooth out the displayed power level. The entire setup was then switched on during a time period before the actual measurements were performed to enable all components to warm up and stabilize.

The output power was measured and the supplied DC current to the DPA was measured as well from the DC power supply. After that, the power efficiency was calculated from these measurements by the equation as follows:

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \times 100\% \tag{5.5}$$

The measured output power, gain and efficiency of the DPA versus frequency with the simulated results are plotted in following Figures 5.22 and 5.23. The measured output power is rated at 40 dBm along the frequency, but it was degraded drastically beyond 2 GHz and same situation goes to the measured gain performance as observed in Figure 5.22. This may be due to the grounding effect of GaN device that will affects the performance in higher frequency. The GaN HEMT power transistor is a very sensitive device, the grounding part is attached with the indium foil to support the board thermal for a better heat transfer. Besides, in this measurement the simulation result is obtained from ideal performance value in ADS with microstip realization, but in practically, they are easily affected by other parameters such as the arrangement of elements on board, the length and width of the microstrip, lacking of via holes and list goes on. Whereas the measured efficiency versus frequency at P_{in} = 28 dBm in Figure 5.23, has peaked slightly above 45% which is considered close to the simulation results and bandwidth covering

100 MHz to 2 GHz. The DC current of 0.9 A at average are obtained over the entire frequency range.

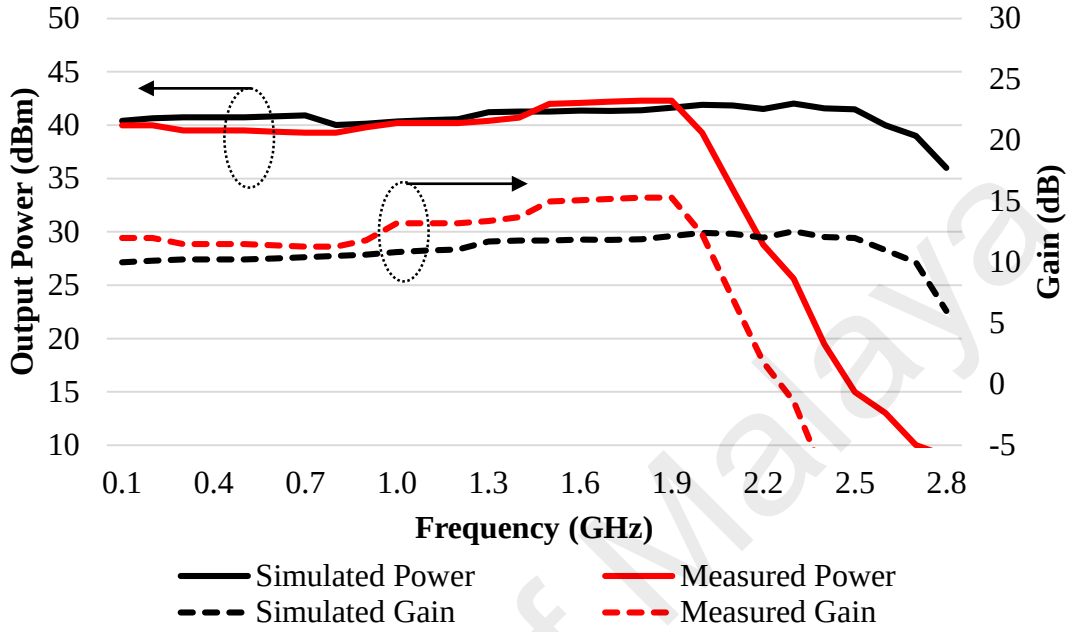


Figure 5.22: Measured vs. simulated of the power performance (output power and gain) of the DPA topology over the entire bandwidth.

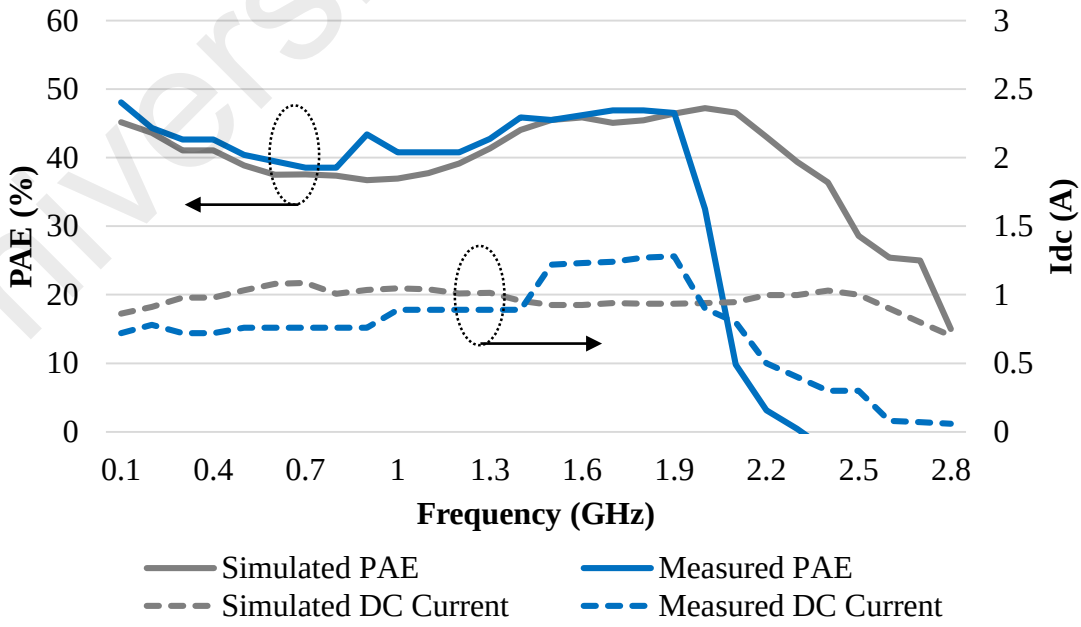


Figure 5.23: Measured vs. simulated efficiency and total DC current of the DPA topology over the entire bandwidth.

In this research, these measurement results had carried out optimization and troubleshooting on the DPA board. The recorded results are the best measurement level chosen. However, there is a good correlation between simulation and measurement results of DPA design and achieved state-of-art performance according to author's knowledge.

In fact, in comparison with the state of the art for GaN HEMT distributed amplifiers reported in Table 5.2. The presented gate line phase adjustment technique has delivered the lowest bandwidth, higher gain and power among the reported GaN HEMT DPAs.

Table 5.2: Comparison of State-of-Art Performances.

References	Device Technology	Bandwidth [GHz]	Gain [dB]	Pout [W]	PAE [%]
(Ulusoy et al., 2014)	GaN HEMT	0.4 – 8.0	11	12	18 – 45
(Kim et al., 2014)	GaN HEMT	0.1 – 2.7	12	5	40
(Andersson, 2015)	GaN HEMT	0.9 – 2.6	10	20	60 – 64
(Moon et al., 2016)	GaN HEMT	0.1 – 8.0	7.3-12.7	5	35
This Work	**GaN HEMT**	**0.08 – 2.0**	**12**	**12.6**	**32 – 47**

CHAPTER 6: DISCUSSION AND CONCLUSION

6.1 Conclusion

As a conclusion, a comprehensive study of circuit topologies for broadband, efficient, high power distributed power amplifiers was completed. This thesis has contributed a significant improvement in efficiency over the conventional DPA based on the novel integration technique of broadband impedance transformer and gate line impedance adjustment method. The fabrication of the prototype has performed as planned. The performance of the designed amplifier compared to the commercial reference amplifier offered twice the output power, but within a slightly narrower bandwidth as compared to MMIC technology. The sized of the fabricated amplifiers were rather large compared to commercial amplifier block, but the expenses are much lower. These types of power amplifiers are very important to design RF communication systems, for example LTE, Bluetooth, two-way radio mobile applications and etc. They required wideband operation, high efficiency and low power consumption. Thus, this research is very interesting and it can be taken further for the advancement of PA to improve market-oriented product nowadays.

6.2 Future Work

This thesis research has developed two circuit configurations of distributed power amplifiers. The first design was working with the aid from Motorola Solutions, that employed a novel integration technique of broadband impedance transformer by using pHEMT and GaN HEMT as power transistor of the DPA system. The key point of this design is to maximize DC - RF conversion to the load termination that addressed on impedance transformer design using RFT. This prototype board with impedance transformer integration is having advantages over size area, implementation in small form

factor and low cost approach particularly compatible for radio communications applications. However, this work can be further improving in terms of fabrications with monolithic instead of hybrid. As monolithic material can achieve very wide bandwidth which is suitable for ultra wide band applications enhancement such as 4G and 5G network applications. Besides, the amplifier class A operation has the limitation on giving higher efficiency over 30 %, it has a major drawback in that it is inherently inefficient due to its constant operation in the active region which forces it to dissipate power even where there is no or just a small input signal.

For the second design exhibited in Chapter 5, a conventional DPA is designed in ADS simulation as the guideline to improve the overall network, however the same power transistor GaN HEMT are used for both cases in conventional and modified DPA respectively. In the conventional DPA system has presented a very fundamental impedance matching network based on theoretical calculation on the lump inductors and capacitors. Whereas the modified DPA was designed in order to prove the impedance adjustment technique at the gate line able to enhance the overall efficiency. A comparison between simulation and measurement results were made in Chapter 5, in order to validate the prototype board. Yet, the simulation results are the ideal goals throughout this research, due to some loss, components selection and circuitry errors the measurement does not achieved a 100% perfect result, but the fabricated DPA still managed to gives good agreement for this research work. This design can be further improving especially in the analysis on phase coherent studies at the gate line of DPA as this is the novel technique that can be further investigate on theoretical aspect.

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LIST OF PUBLICATIONS AND PAPERS PRESENTED

Conference Paper

1. **H. Hui Yan**, K. Narendra and T. A. Latef, "**Efficiency Enhancement for Distributed Power Amplifier with GaN HEMT Technology**", *IEEE Asia-Pacific Conference on Applied Electromagnetics (APACE) Langkawi, Kedah, Malaysia*, 11-13 December 2016.

ISI Journal

1. K. Narendra, **H. Hui Yan**, B.S. Yarman and T. A. Latef, "**Distributed Power Amplifier with Novel Integration Technique of Broadband Impedance Transformer using pHEMT and GaN HEMT**", *IET Microwaves, Antennas & Propagation*, 8 February 2017. DOI: 10.1049/iet-map.2016.0934 (ISI-Cited Publication)

2. **H. Hui Yan**, K. Narendra and T. A. Latef, "**Broadband GaN HEMT Distributed Power Amplifier Design with Phase Adjustment**", *Microwave and Optical Technology Letters, June 2017.* (Submitted journal)