DESIGN OF AN ULTRA WIDEBAND LOW NOISE AMPLIFIER FOR COGNITIVE RADIO APPLICATIONS

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2017

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DISSERTATION SUBMITTED IN FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE OF MASTER OF ENGINEERING SCIENCE

FACULTY OF ENGINEERING
UNIVERSITY OF MALAYA
KUALA LUMPUR

2017

UNIVERSITY OF MALAYA

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Registration/Matric No: KGA130060

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Title of Dissertation: DESIGN OF ULTRA WIDEBAND LOW NOISE AMPLIFIER FOR COGNITIVE RADIO APPLICATION

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ABSTRACT

Since the release of 3.1 GHz – 10.6 GHz bandwidth for unlicensed radios operation in 2002 and allowing unlicensed radios to operate in the TV white space, ultra-wideband communication has become more favorable due to its high data transfer rate. However, in order to avoid unlicensed radios to interfere with underutilized licensed radios, a software has to be developed to monitor the spectrum frequency. Cognitive radios (CR) are introduced in 2000 to overcome the spectrum crowding and underutilization issues due to the increase amount of communication systems and static frequency allocation by Federal Communications Commission (FCC). CR is a hardware driven software communication system that continuously monitors the RF spectrum to determine the available band for unlicensed users, react by changing its operating frequency band and upon request from licensed user, withdraw from the frequency band without causing interference to other users. An ultra-wideband low noise amplifier (LNA) ranging from 50 MHz – 10 GHz frequency adapting resistive feedback and self-biasing techniques is designed to fulfill the requirement of CR front end transceiver. By using common source topology, the proposed LNA is able to achieve an ultra-wideband frequency response in gain and noise figure performance. Measured results show that the input and output matching are better than -10 dB with a gain of 10.32 to 13.28 dB, noise figure of 3.29 to 6 dB with a third-order intercept point ranging from -3.2 to +6 dBm in a frequency span from 50 MHz to 10 GHz using standard CMOS 0.13µm platform. The designed architecture occupies 0.77 mm^2 chip area and consumes 31.2 mW of DC power from 1.2V DC supply headroom power supply.

ABSTRAK

Sejak pembebasan bandwidth dari 3.1 GHz – 10.6 GHz untuk operasi radio tidak berlesen dan membenarkan radio tidak berlesen untuk beroperasi di dalam jalur TV, ultra jalur lebar komunikasi telah digalakkan kerana kadar pemindahan data yang tinggi. Walau bagaimanapun, untuk mengelakkan radio tidak berlesen daripada menggangu dengan radio berlesen yang tidak digunakan sepenuhnya, satu perisian perlu ditubuhkan untuk mengawasi spektrum frekuensi. Kognitif radio (CR) diperkenalkan pada tahun 2000 untuk mengatasi masalah kesesakan dan kekurangan penggunaan spektrum disebabkan oleh penambahan sistem komunikasi dan peruntukan frekuensi static oleh Federal Communications Commission (FCC). CR ialah sistem komunikasi dimana perkakasan didorongi oleh perisian yang sentiasa memperhatikan spektrum RF untuk menentukan ketersediaan spektrum untuk pengguna tidak berlesen, bertidak dengan mengubah frekuensi operasi dan atas permintaan pengguna berlesen, menarik balik dari jalur frekuensi tanpa menyebabkan kegangguan terhadap pengguna lain. Satu ultra jalur lebar penguat hinggar rendah (LNA) yang berfungsi antara 50 MHz – 10 GHz yang menggunakan teknik-teknik rintangan suap-balik dan pincangan-diri telah direkabentuk untuk memenuhi keperluan CR front-end transceiver. Dengan menggunakan topologi common source, LNA yang dicadangkan dapat mencapai ultra jalur lebar frekuensi tindak balas dalam gandaan dan angka hingar. Hasil ukuran menunjukkan input dan output padanan lebih baik daripada -10 dB dengan gandaan dari 10.32 hingga 13.28 dB, angka hingar dari 3.29 hingga 6 dB dengan pintasian titik masukan tertib ketiga (IIP3) dari -3.2 hingga +6 dBm dalam jarak frekuensi dari 50 MHz hingga 10 GHz dengan menggunakan piawai CMOS 0.13 μm platform. Rekabentuk ini menggunakan 0.77 mm^2 keluasan cip dan menggunakan 31.2 mW DC kuasa dari 1.2V DC kuasa bekalan.

ACKNOWLEDGEMENTS

First of all, I would like to thank my supervisor, Assoc. Prof. Ir. Dr. Harikrishnan Ramiah for supporting and guiding me throughout my Master study in University Malaya. Moreover, I am grateful that he provided a comfortable research environment with good facilities and resources for research purposes.

Secondly, I would like to accredit Silterra Malaysia Sdn. Bhd. for technical assistance and advice provided in fabricating the designed chip. Additionally, I would like to acknowledge the Collaborative μElectronic Design Excellence Centre (CEDEC) for providing technical support and equipment for chip measurement. I would also like to thank the friendly staffs of CEDEC in helping me in measurement process. Next, I am grateful that UM High Impact Research Grant has provided me financial support throughout my years of study.

I would also like to thank my colleagues for their encouragement, technical support and ideas in circuit design and journal publishing. I also appreciate the help and support by undergraduate students.

Lastly, I would like to express gratitude to my family members and friends for their understanding and support during my post-graduation study.

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LIST OF SYMBOLS AND ABBREVIATIONS

BJT	:	Bipolar Junction Transistor
BW	:	Bandwidth
CMOS	:	Complementary Metal Oxide Semiconductor
CR	:	Cognitive Radio
dB	:	Decibel
dBm	:	Decibel with respect to 1 mW
DC	:	Direct Current
DRC	:	Design Rule Check
DUT	:	Device Under Test
F	:	Noise Factor
FCC	:	Federal Communications Commission
FOM	:	Figure of Merit
GaAs	:	Gallium Arsenide
GSG	:	Ground-Signal-Ground
GSGSG	:	Ground-Signal-Ground-Signal-Ground
IIP3	:	Third-Order Intercept Point
IM	:	Intermodulation
IM3	:	Third-Order Intermodulation Product
K_f	:	Stability Factor
LNA	:	Low Noise Amplifier
LVS	:	Layout Versus Schematic
MOSFET	:	Metal Oxide Semiconductor Field Effect Transistor
NF	:	Noise Figure
NFA	:	Noise Figure Analyzer

NMOS	:	N-channel MOSFET
P1dB	:	1 dB Compression Point
PA	:	Parameter Analyzer
PEX	:	Parasitic Extraction
PMOS	:	P-channel MOSFET
PSA	:	Power Spectrum Analyzer
PSG	:	Power Spectrum Generator
PVT	:	Process, Voltage, and Temperature
QAM	:	Quadrature Amplitude Modulation
Q-Factor	:	Quality Factor
RF	:	Radio Frequency
S-Parameters	:	Scattering Parameters
SGS	:	Signal-Ground-Signal
SiGe	:	Silicon Germanium
SoC	:	System-on-Chip
SOLT	:	Short-Open-Load-Through
SNR	:	Signal to Noise Ratio
THD	:	Total Harmonic Distortion
TV	:	Television
VNA	:	Vector Network Analyzer
C_{gd}	:	Gate-Drain Parasitic Capacitance
C_{gs}	:	Gate-Source Parasitic Capacitance
C_{ox}	:	Oxide Capacitance
g_{d0}	:	Drain-Source Transconductance In Triode Region
g_m	:	Transconductance
g_{mb}	:	Backgate Transconductance

f	:	Frequency
k	:	Boltzmann's Constant
K	:	Process-Dependent Constant
L	:	Length of MOSFET
R	:	Resistance
r_o	:	Channel Length Effect Resistance
S11	:	Input Port Voltage Reflection Coefficient
S12	:	Reverse Voltage Gain
S21	:	Forward Voltage Gain
S22	:	Output Port Voltage Reflection Coefficient
T	:	Absolute Temperature in Kelvin
V_{TH}	:	Threshold Voltage of Transistor
V_{TO}	:	Threshold Voltage of Transistor Without Body Bias
W	:	Total Width of The MOSFET
Ω	:	Resistance
λ	:	Channel Length Modulation Effect Coefficient
μ_n	:	Electron mobility
ϕF	:	Surface Potential
ω	:	Frequency in rad/s
γ	:	Channel Noise Coefficient

CHAPTER 1:

INTRODUCTION

1.1 Motivation

In recent years, wireless communication has grown rapidly and solutions are needed to address the issues of spectrum crowding and underutilization due to static frequency allocation (Lunden, Koivunen, & Poor, 2015; Velempini, Moyo, & Dlodlo, 2012). Since Federal Communications Commission (FCC) has released the frequency band from 3.1 GHz to 10.6 GHz in 2002 for unlicensed radios application and allowing unlicensed radios to utilize TV white space, ultra-wideband communication appears to be the solution for high speed data transfer and spectrum crowding (Kalteh, Fallahi, & Roozbahani, 2008; Leib, Frei, & Menzel, 2009).

In order to prevent interference between unlicensed radios with licensed radios, FCC has set the maximum allowable signal transfer power of unlicensed radios to be much lower than licensed radios so that both radios can co-exist in the same spectrum. However, to avoid spectrum crowding, ultra-wideband communication system should have the ability to switch to other available frequency band and therefore gave birth to the idea of cognitive radio (Haykin, 2005). Cognitive radio is a dynamic spectrum access communication system that is capable of monitoring the frequency spectrum and allocate available frequency band to unlicensed users without causing interference to other users (Mitola & Maguire, 1999). Upon request from licensed user, cognitive radio would withdraw the unlicensed user from the current frequency band and place them to another available band again without causing interference (Wang & Liu, 2011).

Although the cognitive radio is still in research stage and the operating bandwidth is yet to be finalized, the requirement of an ultra-wideband front end transceiver is inevitable (Razavi, 2010; Shim, Yang, & Jeong, 2013). The requirement of a low noise amplifier

(LNA) is extremely important due to its integration after antenna which has strict specifications to follow. An ultra-wideband LNA should have properties such as wideband input and output matching, low and flat noise performance with high and flat gain performance (Chirala, Huynh, Nguyen, & Guan, 2011; Ren-Chieh, Kuo-Liang, & Huei, 2003). Additionally, the LNA needs to inherit decent linearity to amplify the signal without distortion.

Conventional wireless transceiver uses bulky passive components to implement the circuit in printed circuit board. However, with the advancement in semiconductor technology, the size of the circuit has greatly reduced. Semiconductors technologies such as SiGe, GaAs, Bipolar Junction Transistor (BJT) and Complementary Metal Oxide Semiconductor (CMOS) has been used to realize RF design for many years with CMOS being the most favorable (Abidi et al., 1997). CMOS size has been reduced significantly over the years due to the scaling of CMOS length. Moreover, the introduction of on-chip passive components has made system-on-chip (SoC) possible and cost effective which makes CMOS appealing to manufacturers (Brackenbury, Plana, & Pepper, 2010). However, due to the inferior performance of CMOS with lossy substrate, designing circuit in CMOS platform has always been a challenge (Suet Fong & Mayaram, 1999; H. H. Wu et al., 2007). The design of LNA utilizing CMOS platform oversees challenges such as noise from substrate and lower transconductance with higher noise figure compare to other semiconductor counterparts. The scaling of CMOS proportionally reduces the operating voltage which makes low power application possible at the cost of lower linearity.

Over the years, researcher have come up with plenty of topologies and circuit designs to overcome the effect of CMOS inferior performance (W.-K. Chen, 2009; Lu & Xia, 2008; Papananos, 2013; Namrata Yadav, Abhishek Pandey, & Vijay Nath, 2016). By

introducing ultra-wideband property into the design, more considerations are required to design the circuit. However, the benefits of ultra-wideband communication system has motivated researchers to continue the quest for solution.

1.2 Objective

- To investigate and design ultra-wideband low noise amplifier for cognitive radio applications.
- To realize and verify the physical silicon footprint of the proposed LNA.
- To measure the fabricated low noise amplifier and verify the simulation data with measurement data.

1.3 Scope of project

The scope of this project encapsulates the design of schematic and layout of the ultra-wideband LNA based on mathematical verification and the characterization of the fabricated chip. Due to the extended bandwidth of the LNA, the RF signal requires cascading through two stage of amplifications to achieve the desired gain and noise performance. To achieve ultra-wideband input and output matching, resistive feedback, pi-matching, and resistive termination techniques are investigated. Integration of resistors requires extended optimization to achieve the desired trade-off between bandwidth, and gain and noise performance. The complete design flow from front-end to back-end involves the use of Cadence Spectre-RF simulation tools along with Mentor Calibre verification. Several test and measurement equipment such as Vector Network Analyzer (VNA), Power Spectrum Analyzer (PSA), Power Spectrum Generator (PSG), Noise Figure Analyzer (NFA) and Parameter Analyzer (PA) are employed to extract the measured results.

1.4 Dissertation Structure

This dissertation is divided into five chapters as follows. Chapter 1 describes the motivation and objective of this project. Chapter 2 explains on the specifications related to in LNA design. In this chapter, some reported circuit topologies and techniques are explained and their advantages and disadvantages are listed out. Chapter 3 introduces the design methodology of the proposed ultra-wideband LNA. Chapter 4 presents the simulation and measurement results of the proposed LNA. Subsequently, the measurement results are compared with recent reported LNA solution. Chapter 5 shows the conclusion of the project along with future work and possible improvement to the proposed LNA.

CHAPTER 2:

LITERATURE REVIEW ON LNA

2.1 LNA Specifications

Few important specifications are considered in the LNA design and will be discussed in this chapter. This chapter is divided into LNA specifications and topology consideration.

2.1.1 Impedance Matching

Input and output impedance matching are essential in LNA design as it is important to deliver maximum power to the LNA circuit as well as to assure that maximum power is delivered to the subsequent stage of the transceiver (Pramod, Kumaraswamy, & Praveen, 2013). Moreover, a well-matched circuit has little to none reflection of RF signal as well as standing wave. In RF communication, the standard impedance matching is 50 ohms and is measured through S-parameters analysis (Ling, Zhigong, & Jianjun, 2005). Unlike conventional narrowband LNA which has a minimum peaking response in desired frequency, ultra-wideband LNA has few minimum peaks but generally with a response of less than -10 dB in the entire band of operation. In ultra-wideband LNA design, input and output impedance matching are usually taken -10 dB as a benchmark because it translates to about 10% of signal reflection in power. Figure 2-1 is illustrated to further understand how the two-port network S-parameters works (Razavi, 2012).

Figure 2-1: Model of S-parameters two-port network.

In Figure 2-1, a_1 and a_2 are signals injected to the two-port network while b_1 and b_2 are signals rejected from the two-port network. To determine S-parameters, only one signal is injected at a time. For simplicity, left hand side of the two-port network is regarded as input while right hand side of the two-port network is regarded as output. In order to determine the input port voltage reflection coefficient, S11 signal a_1 is injected to the input port of the two-port network and the reflected signal b_1 is measured. The ratio of b_1/ a_1 is then expressed in dB20 and denoted as S11 and it is inversely proportional to input return loss where a low input reflection coefficient which implies a high return loss. For output port voltage reflection coefficient S22, a_2 is injected into the output port of the two-port network and the reflected signal b_2 is measured. The ratio of a_2/b_2 is then expressed in dB20 and indicated as S22 which inversely proportional to output return loss. Note that if the input and output impedance are well-matched, S-parameters can be expressed as both power and voltage components. Conventional narrowband LNA can achieve excellent S11 and S22 performance by implementing external matching circuit such as filter and the design parameters can be determined by using Smith's Chart (Floyd, Mehta, Gamero, & Kenneth, 1999; Liang-Hung, Hsieh-Hung, & Yu-Shun, 2005). However, ultra-wideband matching is more complex than narrowband matching because a wide range of frequency matching needs to meet the specification. Some of the examples of ultra-wideband input matching techniques are $1/g_m$ matching, resistive feedback matching, π-matching/filter, and inductive source degeneration matching. For output matching, buffer circuit and resistive termination are the most common technique. Impedance matching is essential in determining the stability of the LNA and some of the trade-offs of obtain impedance matching are gain, power consumption and chip size.

2.1.2 Gain

For receiver, RF signal that is picked up by the antenna is usually very weak due to attenuation and path loss (Cordeiro, Challapali, Birru, & Sai, 2005). Therefore, LNA

would have to provide enough signal gain in order to amplify the signal to a certain level before its data can be retrieved. Gain of the LNA is determined by S21 of the S-parameters and sometimes it is known as forward voltage gain. Referring to Figure 2-1, gain of the S-parameter is obtained by measuring the input signal $\boldsymbol{a_1}$ injected to the two-port network and the output signal $\boldsymbol{b_2}$ exiting the two-port network. The ratio of $\boldsymbol{b_2/a_1}$ is then expressed in dB20 and denoted as S21. S21 usually is expressed as voltage gain and under well-matched input impedance condition, it can be viewed as power gain. In communication system, LNA gain is usually in the range of 10 dB up to 30 dB depending on the application it is targeted upon. A very high forward gain may result in compression on signal which lowers the 1 dB compression point, P1dB and also the input referred third-order intercept point, IIP3. Furthermore, high forward gain resulted from higher transconductance would increase the total power consumption and decrease the LNA stability (Toby Kwok-Kei, Kin-Chung, Dongsheng, & Luong, 2000). However, a LNA that has insignificant gain would results in high noise and renders the signal to be undetectable. Over the years, some circuit design techniques have been adapted to improve the gain of the LNA such as g_m-boosting technique, current-reuse/inverter technique, cross-couple technique and inductor peaking.

2.1.3 Reverse Voltage Gain

Reverse isolation is a measurement of how well a circuit in preventing leakage of signal from output back to the input and it is inversely proportional to reverse voltage gain. The lower the reverse voltage gain implies the better the reverse isolation. A high reverse voltage gain may result in instability of the circuit (Zhuo et al., 2005). Referring to Figure 2-1, in order to measure reverse voltage gain, output signal $\boldsymbol{a_2}$ is injected at the output port of the two-port network and the signal exiting the input port $\boldsymbol{b_1}$ is recorded. The ratio of $\boldsymbol{b_1/a_2}$ is then expressed in dB20 and denoted as S12. To avoid confusion, a better S12 performance implies that the reverse voltage gain is small. The choice of the

topology in designing LNA affects greatly the S12 performance. Common source topology has worse S12 performance compared to common gate topology due to the presence of gate-drain parasitic capacitance, C_{gd} between input and output path in common source topology (Bevilacqua & Niknejad, 2004). Moreover, in layout, the additional parasitic capacitance that is present between input and output path would worsen the S12 performance. To improve S12 performance, input signal can be cascaded into two or three stages of LNA at the cost of increased power consumption (Janssens, Crols, & Steyaert, 1998). Moreover, output impedance matching is essential in improving S12 performance. A lower output reflection coefficient, S22 results in higher output return loss thus minimizes the reflected signal power which will be leaking back to the input. Finally, in layout design, huge and long metal layers with different metal layers crossing each other should be avoided in the possibility to reduce the parasitic capacitance.

2.1.4 Noise Figure

In wireless communication, it is inevitable that the desired RF signal is coupled with noise picked up from surrounding while in transmission. However, in LNA design it is assumed that the external noise is only the 50 ohms thermal noise from antenna. One of the objectives in designing LNA is to amplify the desired signal with minimum addition of noise from the circuit. This is because LNA is positioned as the first block of the communication system after antenna an according to Friis formula for noise,

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \ldots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}} \qquad (2\text{-}1)$$

where F_1 represent the noise of the first block LNA, the total system noise is highly affected by LNA noise contribution and later blocks contribute insignificant effective

noise if the gain of LNA is high. Therefore, it is crucial that LNA has high gain to suppress the noise contribution of following stages.

2.1.4.1 Thermal Noise

Thermal noise is generated by thermal agitation of the charge carriers inside the conductor regardless of any applied voltage and the thermal noise equation is given as,

$$\overline{V_n^2} = 4kTR \tag{2-2}$$

where $\overline{V_n^2}$ is the noise voltage mean square per hertz of bandwidth, k is the Boltzmann's constant, T is the absolute temperature in Kelvin, and R is the resistance (Sarpeshkar, Delbruck, & Mead, 1993). (2-2) sometimes is multiplied with bandwidth to obtain the total noise voltage of the spectrum. Although noise can be modeled as voltage noise or current noise, but for simplicity only voltage noise will be shown throughout the noise analysis. In ultra-wideband LNA design, incorporating resistors into the architecture is inevitable in order to obtain flat performance. Hence, in ultra-wideband LNA design, the average noise figure is higher than the narrowband LNA.

2.1.4.2 MOSFET Channel Thermal Noise

When MOSFET operates in saturation mode, there exist an inverse resistive channel between the drain and the source (Antonopoulos et al., 2013). Since the channel is resistive therefore it is considered as a contribution of thermal noise. MOSFET channel thermal voltage noise can be derived as,

$$\bar{V}_n^2 = \frac{4kT\gamma}{g_{d0}} \tag{2-3}$$

where γ is the channel noise coefficient which depends on channel length and its bias conditions, and g_{d0} is the drain-source conductance in the triode region. The value of γ is

2/3 for long channel and much larger for short channel (Chih-Hung & Deen, 2002). However, MOSFET channel noise can be reduced by implementing noise-cancelling technique and increasing the number of finger of the MOSFET (Zhang, Li, Moody, Xue, & Ren, 2014).

2.1.4.3 Flicker Noise

Flicker noise is only dominant at low frequency region. The equation of flicker noise is given as,

$$\overline{V_n^2} = \frac{K}{WLC_{ox}} \frac{1}{f} \tag{2-4}$$

where, K is the process-dependent constant and in most of the case PMOS has a smaller value of K than NMOS, W is the width of the transistor, L is the length of the transistor, C_{ox} is the oxide capacitance, and f is the frequency (Aoki & Shimasue, 2001). Although flicker noise is not dominant in cognitive radio application, but it is close to the $1/f$ corner frequency. As stated in (Razavi, 2012), with today's technology the corner frequency might be located at tenths or even hundreds of megahertz. Although MOSFET has other noises such as gate noise and gate-induced noise current at high frequency, but the noise contribution is negligible and is ignored in this analysis.

2.1.5 Linearity

One of the requirements of LNA is to amplify RF signal linearly. When the input signal is small, the signal would be amplified linearly at the output. However, when input signal gradually increases, nonlinearity behavior becomes more apparent at the output signal (Jian-Yu & Shuenn-Yuh, 2007). There are few scenarios such as harmonic distortion, device compression and intermodulation which will result in nonlinearity and distortion in LNA. The input/output characteristic of a memoryless LNA can be approximated by Taylor series expansion in time domain as,

$$y(t) \approx \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{2-5}$$

where *x(t)* and *y(t)* are the input and output function in time domain respectively, $\alpha_1 = g_m$, $\alpha_2 = \frac{1}{2} g'_m$ and $\alpha_3 = \frac{1}{6} g''_m$. Here, α_1 is the transconductance or sometimes referred as small signal gain of the LNA. If the function of *x(t)* is given as,

$$x(t) = A\cos\omega t \tag{2-6}$$

then, (2-5) can be expanded as,

$$\begin{aligned} y(t) &= \alpha_1 A\cos\omega t + \alpha_2 A^2\cos^2\omega t + \alpha_3 A^3\cos^3\omega t \\ &= \alpha_1 A\cos\omega t + \frac{\alpha_2 A^2}{2}(1+\cos 2\omega t) + \frac{\alpha_3 A^3}{4}(3\cos\omega t + \cos 3\omega t) \\ &= \frac{\alpha_2 A^2}{2} + (\alpha_1 A + \frac{3\alpha_3 A^3}{4})\cos\omega t + \frac{\alpha_2 A^2}{2}\cos 2\omega t + \frac{\alpha_3 A^3}{4}\cos 3\omega t \end{aligned} \tag{2-7}$$

In (2-7), the first term is the dc offset which result from second-order nonlinearity, the second term is the fundamental frequency, third term is the second-order harmonic, and the forth term is the third-order harmonic. From (2-7), second and third-order harmonics amplitude increases with the power of two and three which indicates that at certain point, the harmonics would have a larger amplitude than fundamental frequency which results in significant nonlinearity.

2.1.5.1 Harmonic Distortion

From (2-7), when a sinusoid is applied to a nonlinear device, the output has frequency components that are integer multiples of the input signal which is the harmonics. In narrowband communication systems, harmonic distortion measurement is not a good way to indicate the effect of nonlinearity. For example, if a narrowband LNA operates in 2.4 GHz, its second-order harmonic would be in 4.8 GHz which would be filtered out or attenuated due to the narrowband characteristic of the LNA. In comparison to ultra-

wideband LNA, 4.8 GHz still falls under the operating frequency. However, before the harmonic's amplitude reaches comparable level with fundamental frequency, another nonlinearity effect takes place which is the signal compression and will be discussed later. To calculate each order of harmonic distortion, the amplitude of the harmonic is divided by the amplitude of fundamental frequency and expressed in db20. The equations can be approximated as (Leung, 2011),

$$HD_2 \cong \left| \frac{\frac{1}{2}\alpha_2 A^2}{\alpha_1 A + \frac{3\alpha_3 A^3}{4}} \right| \cong \frac{1}{2}\left|\frac{\alpha_2}{\alpha_1}\right| A \tag{2-8}$$

$$HD_3 \cong \left| \frac{\frac{1}{4}\alpha_3 A^3}{\alpha_1 A + \frac{3\alpha_3 A^3}{4}} \right| \cong \frac{1}{4}\left|\frac{\alpha_3}{\alpha_1}\right| A^2 \tag{2-9}$$

and the total harmonic distortion (THD) can be calculated as,

$$THD = \frac{\sqrt{HD_2^2 + HD_3^2 + HD_4^2 + \ldots}}{V_{fund}} \tag{2-10}$$

where V_{fund} is the fundamental signal in voltage.

2.1.5.2 1 dB Compression Point (P1dB)

Small signal gain of the LNA is obtained by assuming harmonics are negligible. Referring to (2-7), fundamental frequency has two terms which are $\alpha_1 A$ and $\frac{3\alpha_3 A^3}{4}$ due to third-order harmonic and the latter varies greatly with amplitude. If α_1 and α_3 are both positive value, then fundamental frequency would expand indefinitely. However, most of the RF circuits has opposite signs for α_1 and α_3 which results in compression when amplitude of the signal increases. P1dB is determined when the input signal level causes

the gain to drop by 1 dB or when the output signal level is amplified 1 dB lesser than it is supposed to amplify. By equating the compressed gain due to third-order harmonic to 1 dB less than the ideal gain without harmonic, P1dB can be written as,

$$20\log\left|\alpha_1 + \frac{3}{4}\alpha_3 A^2_{in,1\,dB}\right| = 20\log|\alpha_1| - 1dB \tag{2-11}$$

$$A_{in,1\,dB} = \sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2-12}$$

P1dB indicates 10% gain compression and is widely used to determine the linearity of the circuit although there are other cases that would cause nonlinearity. If a signal is not amplitude modulated, then the compression of signal has no significant effect to the data but if a signal is amplitude modulated, then the compressed signal would result in loss of data. However, in order to transmit large data, RF signals are usually modulated with more than one modulation such as quadrature amplitude modulation (QAM) where amplitude modulation and phase modulation takes place.

2.1.5.3 Desensitization and cross modulation

When RF signal is detected along with a large interferer, the receiver is largely blocked by the interferer (Gu, 2005). One of the applications that uses large interferer to desensitize the receiver is signal jammer or blocker. Another effect of RF signal coupled with large interferer in nonlinear system is the cross modulation effect. When a larger interferer with amplitude modulation is coupled with RF signal, the modulation would transfer from the interferer to the signal. However, if the interferer is phase modulated, the modulation would not transfer to the signal in memoryless nonlinear system.

2.1.5.4 Input third-order-intercept point (IIP3)

IIP3 is the measurement for intermodulation effect when RF signal is received together with two same amplitude interferers with frequency separation from 10 kHz up to few megahertz. Intermodulation (IM) arises from the mixing of the two interferers that generate intermodulation products at the output. Assuming two interferers with frequency ω_1 and ω_2 detected as input into a nonlinear receiver, the IM products at output is shown in Figure 2-2.

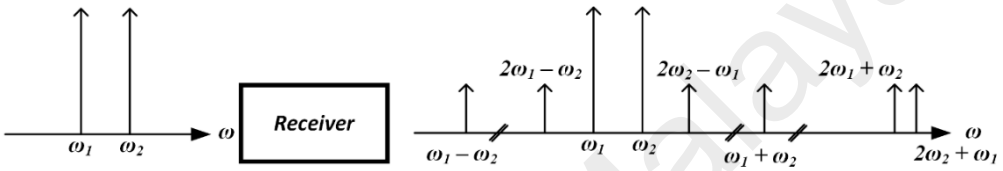


Figure 2-2: Two tone signals with intermodulation products.

In Figure 2-2**,** third-order IM products $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ falls closely to the desired outputs ω_1 and ω_2 which makes the detection of desired signal difficult. In some cases, third-order IM products might fall exactly on top of the desired outputs and corrupt the signal. The input of the receiver accompanies with two interferers is given as,

$$x(t) = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t \tag{2-13}$$

hence, the output of the receiver due to nonlinearity effect on the two interferers can be written as,

$$\begin{aligned} y(\mathrm{t}) = {} & \alpha_1 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t) + \alpha_2 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^2 \\ & + \alpha_3 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^3 \end{aligned} \tag{2-14}$$

By expanding (2-14)**,** and omiting the dc terms, harmonics and second-order IM products which are located far away from the desired signal, the third-order IM products, IM_3 can be expressed as,

$$2\omega_1 \pm \omega_2 = \frac{3\alpha_3 A_1^2 A_2}{4}\cos(2\omega_1 + \omega_2)t + \frac{3\alpha_3 A_1^2 A_2}{4}\cos(2\omega_1 - \omega_2)t \quad (2\text{-}15)$$

$$2\omega_2 \pm \omega_1 = \frac{3\alpha_3 A_1 A_2^2}{4}\cos(2\omega_2 + \omega_1)t + \frac{3\alpha_3 A_1 A_2^2}{4}\cos(2\omega_2 - \omega_1)t \quad (2\text{-}16)$$

and for two tone signals with equal amplitude, $A_1 = A_2 = A$, the amplitude of each IM_3 products can be simplified as,

$$IM_3 = \frac{3}{4}\alpha_3 A^3 \quad (2\text{-}17)$$

On the other hand, fundamental frequencies at the output of a nonlinear receiver can be expressed as,

$$\omega_1 = (\alpha_1 A_1 + \frac{3}{4}\alpha_3 A_1^3 + \frac{3}{2}\alpha_3 A_1 A_2^2)\cos\omega_1 t \quad (2\text{-}18)$$

$$\omega_2 = (\alpha_1 A_2 + \frac{3}{4}\alpha_3 A_2^3 + \frac{3}{2}\alpha_3 A_2 A_1^2)\cos\omega_2 t \quad (2\text{-}19)$$

where the first term is the ideal fundamental frequency gain and second along with the third terms are third-order harmonics due to nonlinearity of the receiver and varies greatly with amplitude (Leung, 2011). When the amplitude of the two-tone signal is small, the first term of (2-18) and (2-19) is much larger than second and third terms. As explained in the appreciation of P1dB, most of the RF circuits have compressive gain which results in compression of the fundamental frequency. The point of 1 dB gain compression of the fundamental frequency can reach before IIP3 point and it is also true for the opposite for some special cases. In order to find the IIP3, the amplitude of ideal fundamental frequency is made equal to the amplitude of IM_3 and can be expressed as,

$$\left|\alpha_1 A_{IIP3}\right| = \left|\frac{3}{4}\alpha_3 A_{IIP3}^3\right| \tag{2-20}$$

$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2-21}$$

and from (2-12), IIP3 and P1dB can expressed as,

$$\frac{A_{IIP3}}{A_{in,1\,dB}} = \frac{\sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}}{\sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|}} = \sqrt{\frac{4}{0.435}} \approx 9.6\,dB \tag{2-22}$$

(2-22) shows that IIP3 is around 9.6 dB greater than P1dB which implies that the signals are compressed before reaching IIP3 point. In simulation and measurement, the curve of IIP3 is extrapolated to obtain the IIP3 point by assuming the fundamental and IM product increase linearly when two tone signals power increase. This assumption will be demonstrated in Chapter 4.

2.1.6 Stability Factor

Since LNA design involves active device, the stability of the circuit is important. If an amplifier is unstable, the amplifier would oscillate and distort the desired signal. The Rollet's stability factor can be expressed as (Marzuki, 2011),

$$K = \frac{1-\left|S11\right|^2-\left|S22\right|^2+\left|\Delta\right|^2}{2\left|S21\cdot S12\right|} \tag{2-23}$$
$$\Delta = S11\cdot S22 - S12\cdot S21$$

where S11, S22, S12, and S21 are the scattering parameters for two-port network. A stability factor of greater than 1 would deem the circuit to be unconditionally stable.

2.2 LNA Topologies

Prior in exploring the topologies of the LNA, it is important to determine whether the circuit design should be single-ended or differential. Single-ended LNA implies that the LNA has only one input port and one output port while differential LNA implies that there are two input ports and two output port with which input signals out of phase to each other (Chang-Wan, Min-Suk, Phan Tuan, Hoon-Tae, & Sang-Gug, 2005; Xiaoling & K. K, 2005). Single-ended LNA is easier to implement because on-chip or off-chip balun is not required to provide the out of phase signals. Passive off-chip or active on-chip balun can be adapted into the circuit design to generate out of phase signals but comes in a disadvantage such as insertion loss, unbalanced amplitude and phase of the balun, and additional noise to the circuit (Yoon et al., 1999). Moreover, according to (2-1), in order to achieve high gain and low noise in receiver block, it is preferable to implement a differential mixer than differential LNA. On the other hand, differential LNA consumes double the DC power compare to single-ended LNA with larger chip area, and introduces complexity into the circuit design.

Differential LNA has the advantages of rejecting common-mode noise, power noise, second-order intermodulation products and to improve the dynamic range. This is because common-mode noise which is coupled together with differential inputs and power noise which is generated due to fluctuation of power supply are out of phase to each other at the output port balun which would potentially cancel out each other.

In order to achieve ultra-wideband performance, LNA design would require more than a single stage of amplification. Since input matching is important in LNA design in order to minimize input reflection coefficient, the first stage amplification of the LNA design should be chosen diligently. Figure 2-3 and Figure 2-4 shows the common gate amplifier and common source amplifier in a single stage. Common gate LNA has the advantage of

ultra-wideband input matching due to its input impedance looking up from the source terminal which is equal to (Sanghyun, Woonyun, Chang-Ho, Kyutae, & Laskar, 2009),

$$Z_{in} = \frac{1}{g_m} \| \frac{1}{g_{mb}} \tag{2-24}$$

where g_m is the gate transconductance and g_{mb} is the backgate transconductance. Backgate transconductance arises due to the source terminal of common gate LNA is no longer at same potential with backgate. This is usually true in ultra-wideband LNA design because R_1 is required to incorporate in the source terminal in Figure 2.3 to prevent direct short of input signal to the ground and the incorporation of resistor R_1 would create voltage drop across the source terminal which in turn results in backgate transconductance. In most of the cases, $g_m >> g_{mb}$ and therefore the input matching is more dependant on g_m. By carefully tuning the gate bias voltage and CMOS width, the common gate Z_{in} can be made equal to 50 ohms or 20 mS of transconductance. Although common gate LNA can achieve input matching without additional matching circuit or technique, but the temperature and process dependency of g_m would jeopardize the input matching easily. Moreover, as frequency increases, gate source capacitance, C_{gs} which is in parallel with Z_{in} deteriorates the input matching. Common gate LNA also has lower gain to noise ratio than common source LNA due to its restriction in transconductance (David J Allstot, Li, & Shekhar, 2004). The noise factor equation for common gate LNA by assuming $g_m R_S = 1$ can be simplified as (Chih-Fan & Shen-Iuan, 2005),

$$F = 1 + \frac{\gamma}{\alpha} + \frac{4R_S}{R_D} \tag{2-25}$$

where $\alpha = \frac{g_{d0}}{g_m}$ and g_{d0} is the drain-source conductance in triode region. By assuming $\frac{\gamma}{\alpha} = 1.33$ and $R_D >> R_S$ which results to a noise figure of almost 4 dB. Usually common gate LNA is accompanied with a noise-cancelling stage due to its poor noise performance (Bruccoleri, Klumperink, & Nauta, 2002; W. H. Chen, Liu, Zdravko, & Niknejad, 2008).

Another downside of common gate LNA is that it requires additional resistor at the source terminal compared to a common source LNA which result in lower voltage swing due to voltage headroom consumption of the resistor (Ansari & Yavari, 2011).

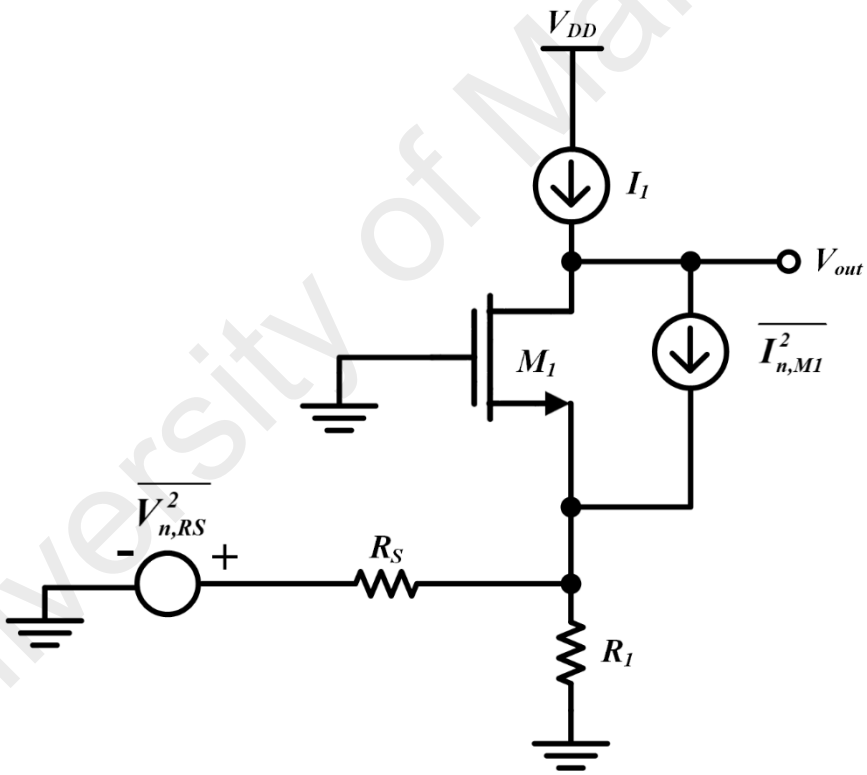


Figure 2-3: Common gate amplifier.

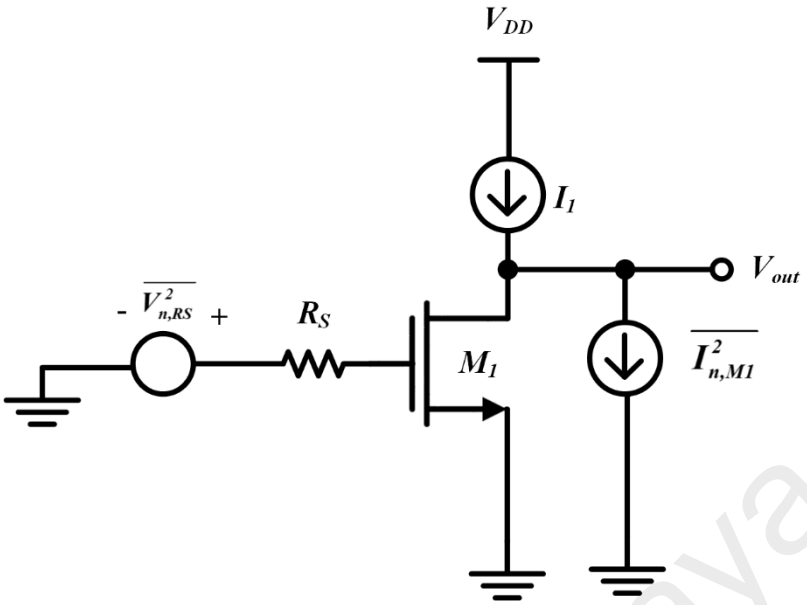


Figure 2-4: Common source amplifier.

On the other hand, common source LNA has to integrate external matching circuit in order to achieve ultra-wideband matching as the input signal is connected directly to the gate terminal of the LNA which has high impedance (D. J. Allstot, Xiaoyong, & Shekhar, 2004). Filter circuit, shunt resistive feedback and inverter circuit are some of the input matching techniques that can be used in common source LNA to achieve ultra-wideband matching. However, since there is no restriction on the transconductance, gain and noise performance of the common source LNA is typical much superior than common gate LNA (Im, Nam, Kim, & Lee, 2009; N. Yadav, A. Pandey, & V. Nath, 2016).

There's an alternative methodology to implement ultra-wideband LNA by cascading several stage of common source amplifier which known as a distributed LNA (Ballweber, Gupta, & Allstot, 2000; Chirala et al., 2011; Hee-Tae & Allstot, 2002). However, relatively large chip area and power consumption compare to common source LNA or common gate LNA has made this design not favorable for ultra-wideband design. After the first stage of the ultra-wideband LNA is determined, the input matching technique can then be specified.

2.2.1 Input Matching Techniques

As mentioned earlier, input matching is essential in LNA design and the techniques of input matching will be discussed subsequently.

2.2.1.1 Resistive Termination

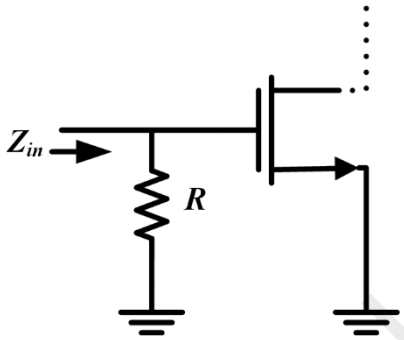


Figure 2-5: 50 ohms resistive termination.

Figure 2-5 shows a 50 ohms resistive termination matching in order to achieve maximum power transfer. The resistor itself will contribute to thermal noise which will increase the amplifier's noise figure (Vishwakarma, Sungyong, & Youngjoong, 2004). Moreover, the low resistance path due to resistive termination will cause leakage of the signal to ground and further attenuate the signal. Resistive termination input matching technique is not favorable for ultra-wideband application.

2.2.1.2 Shunt-series resistive feedback

Shunt-series resistive feedback is one of the common input matching techniques in common source LNA (H. K. Chen, Chang, Juang, & Lu, 2007). As shown in Figure 2-6 is the shunt-series resistive feedback technique with R_F the feedback resistor and R_D the load resistor at drain terminal. Sometimes the feedback R_F is series-connected with an on-chip capacitor to isolated DC and signal component when DC biasing is not the same for gate and drain and sometimes it is diode-connected as shown in Figure 2-6.

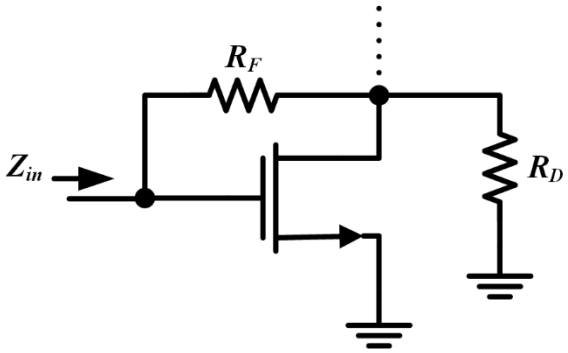


Figure 2-6: Shunt-series resistive feedback technique.

By ignoring the effect of C_{gs} and by connecting a voltage source V_x with current I_x on gate terminal, the effective resistance, R_{eff} looking into Z_{in} can be derived as,

$$\frac{V_X}{I_X} = R_{eff} = \frac{R_F + R_D}{1 + g_m R_D} \approx \frac{R_F + R_D}{1 + A_V} \tag{2-26}$$

where $A_v = g_m R_D$ is the voltage gain of the LNA. By carefully selecting the parameters, R_{eff} can be made equal to 50 ohms. However, this technique needs a sacrifice in gain and noise performance as the feedback path reduce the effective gain and thermal noise contribution by the resistor nevertheless it is one of the suitable technique for ultra-wideband input matching.

2.2.1.3 Inductive Source Degeneration

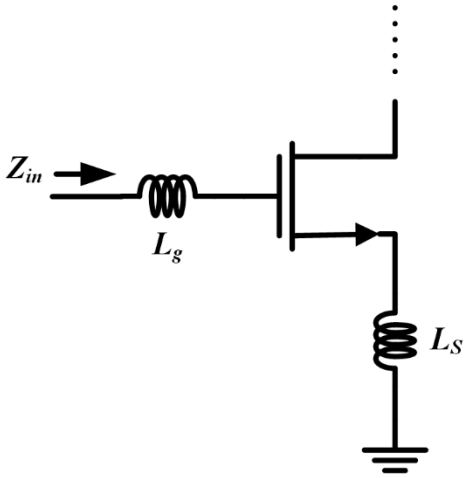


Figure 2-7: Inductive source degeneration technique.

As shown in Figure 2-7, two on-chip inductors L_g and L_s is connected to the gate and source terminal respectively. Since inductor does not consume voltage headroom, this technique allows stacking of MOSFET in order to achieve current reuse topology and higher gain performance (Andreani & Sjoland, 2001; Shaeffer & Lee, 1997). The input impedance looking into gate terminal can be derived as,

$$Z_{in} = sL_g + sL_s + \frac{1}{sC_{gs}} + \frac{g_m L_S}{C_{gs}} \tag{2-27}$$

The first three terms of (2-27) is the imaginary part of the input impedance and can be made equal to zero and the last term is the real part of the input impedance and again can be made equal to 50 ohms. This technique does not incorporate any resistor into the design other than the parasitic resistance in inductors which is negligible therefore it does not contribute to the total noise in the circuit. An on-chip capacitor C_{gs} can be connected between gate and source terminal to add a degree of freedom into the circuit design. The trade-off of using this technique is that the inductor requires a large chip area consumption therefore increases the cost of production. Although this technique achieves input

matching and good gain and noise performance but the narrowband response of inductor renders this technique suitable for narrowband LNA design only.

2.2.1.4 Filter Matching

Input matching can be achieved by using filter circuitry. Second and higher order filter can be incorporated in the circuit design in order to pass a certain desired frequencies and block unwanted frequencies (Ismail & Abidi, 2004). However, on-chip filters usually occupy large amount of physical area due to the size of the capacitors and inductors used in the filter are relatively larger than other on-chip components and the non-ideality of the filter would result in signal attenuation.

2.2.2 Output Matching Techniques

It is important to ensure that the insertion loss of the input as well as the output is low in order to minimize signal reflection and voltage standing wave. Resistive termination at the output matching and buffer circuit integration are by far the most common output matching techniques in LNA design.

2.2.2.1 Resistive Termination

Although resistive termination matching is not common in input matching, but it is widely used in output matching together with a final stage common source topology.

As shown in Figure 2-8, a resistor is connected at the drain terminal of the final stage LNA. V_{out} is connected to the next stage of the transceiver which is potentially a mixer and should be input matched. At low frequency, resistor R is parallel with a large MOSFET output resistance r_o and a large gate-drain parasitic capacitance, C_{gd}. Output resistance r_o arises due to channel length modulation and can be derived as,

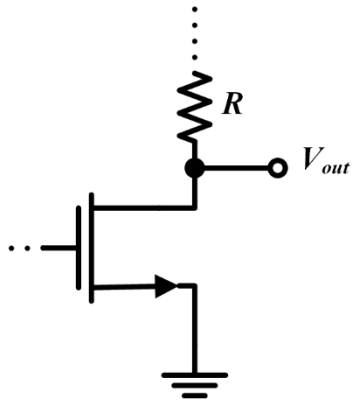


Figure 2-8: Output resistive termination technique.

$$
\begin{aligned}
i_D &= K(V_{GS} - V_t)^2(1 + \lambda V_{DS}) \\
i_d &= \frac{d\, i_D}{d\, V_{DS}} \mid \mathrm{V}_{ds} \\
&= \lambda K(V_{GS} - V_t)^2 V_{ds} \\
&= \frac{V_{ds}}{r_o} \\
r_o &= \frac{1}{\lambda K(V_{GS} - V_t)^2} = \frac{1}{\lambda I_D}
\end{aligned}
\tag{2-28}
$$

where $V_{GS} - V_{TH}$ is the overdrive voltage, $K = ½\ \mu_n C_{ox}(W/L)$ is the MOSFET physical parameters, $1 + \lambda V_{DS}$ is the channel length modulation effect and r_o value is large in the entire frequency range. Therefore, in low frequency the effective impedance at the output is resistor R. However, as the frequency increases the impedance, C_{gd} decreases and the output impedance is now C_{gd} parallel with R. To compensate this detrimental effect, an on-chip inductor is usually placed series with R to resonate with C_{gd} at high frequency to create a minimum peak in output matching response.

2.2.2.2 Buffer Circuit

As an alternative of using passive component to achieve output matching, MOSFET can be used as a source follower to provide output matching. Common drain amplifier or source follower has high input impedance and low output impedance which makes it suitable to drive mixer which is required to have 50 ohms input impedance as well as to

act as a voltage buffer (Reiha & Long, 2007). Source follower topology is shown in Figure 2-9 with M_1 act as common drain amplifier and M_2 is used to isolate the signal from ground connection because the impedance looking down from M_1 is r_o as explained in output resistive termination.

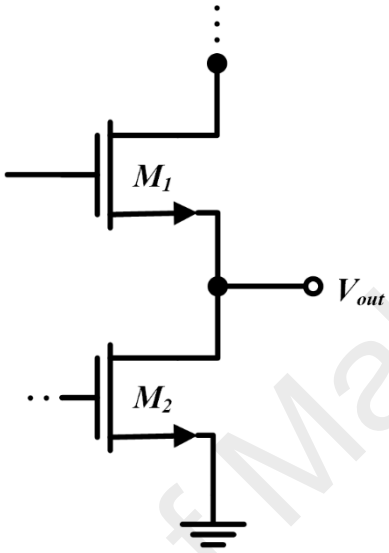


Figure 2-9: Source follower topology.

The output impedance of M_1 is roughly equal to $1/g_m$ which can be set to 50 ohms. The drawback of buffer circuit is in the less than unity voltage gain and the additional power consumption resulting out of the integration.

2.2.3 Gain Enhancement Stage

As the first RF block in the wireless communication, LNA must have sufficient gain in order to amplify weak RF signal. A typical gain of more than 10 dB is required in LNA design which translates to around 10 times amplification. LNA design sometimes necessitate the sacrifice of gain and noise performance obtain matching and low power consumption. However, there are several techniques to enhance the gain of the LNA and suppress the noise.

2.2.3.1 Stacking Cascode Common Gate Topology

Figure 2-10 describes the stacking of cascode common gate gain topology. Common gate M_1 acts as first stage amplification with input matching and M_2 acts as gain enhancement stage. L_1 and C_1 acts as filter circuit to ground output signal of M_1 from entering source terminal of M_2. On the other hand, C_2 is integrated to the circuit to act as ac-coupling capacitor. Since the current flows in the same path for a stacking cascode topology, the total power consumption is the same as in absence of M_2 and sometimes known as current reuse stage (Lee, Park, Chang, & Yun, 2012). However, since M_2 consume voltage headroom V_{DS} and therefore it would reduce the dynamic range of the LNA. Due to the scaling of MOSFET which limits the voltage headroom supply, stacking topology becomes more complicated to bias and sustain in saturation especially in ultra-wideband design since resistors are also incorporated in the design which further consumes more voltage headroom.

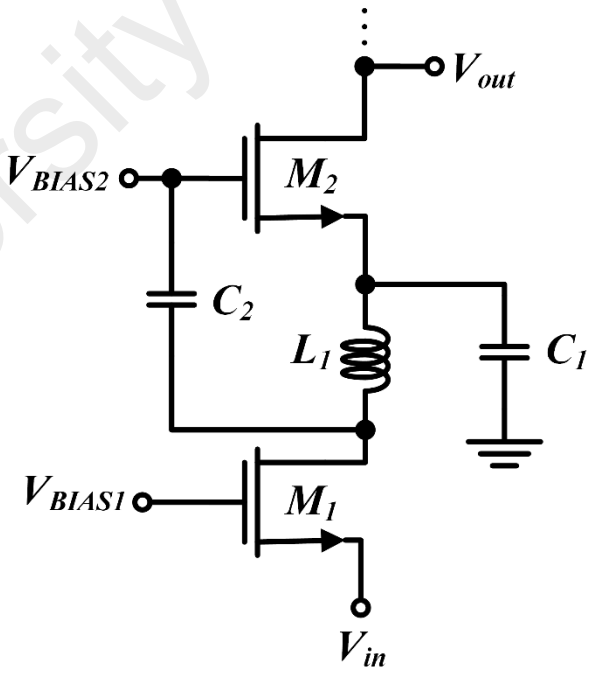


Figure 2-10: Stacking cascode common gate topology.

The effective transconductance of this topology is roughly g_{m1} multiplied by g_{m2} where g_{m1} and g_{m2} are the transconductance of each MOSFETs respectively which results in higher gain.

2.2.3.2 Stacking Cascode Common Source Topology

Similarly, common source stage can be stacked with another common gate stage to improve the LNA gain (Choong-Yul & Sang-Gug, 2003). The circuit in stacking cascode common source topology is shown in Figure 2-11.

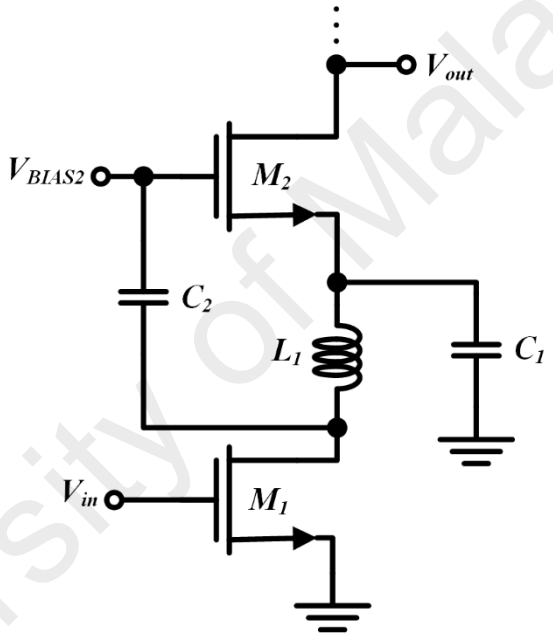


Figure 2-11: Stacking cascode common source topology.

Unlike stacking cascode common gate amplifier, the stacking of cascode common source amplifier has no restriction in M_1 transconductance which result in higher overall gain. Stacking cascode topology also provide another advantage which is an improvement in reverse isolation because the output signal is isolated by M_2 output impedance. There is another topology that is based on cascode architecture but with a lower requirement in voltage headroom supply which is the folded cascode LNA topology. The required voltage supply for folded cascade topology is only V_{DS} instead of $2V_{DS}$ as in stacking cascade topology, the voltage supply can be as low as 0.4 V.

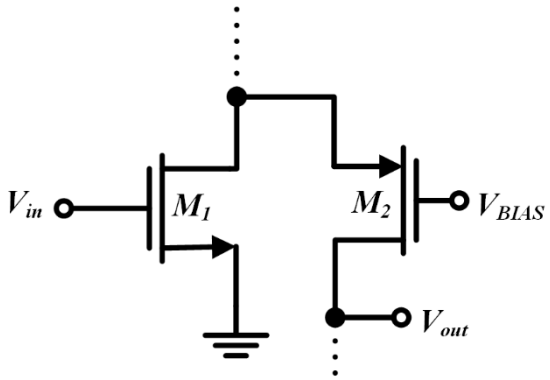


Figure 2-12: Folded cascode topology

Figure 2-12 shows the folded cascode LNA topology and instead of stacking the PMOS M_2 on top of M_1 to realize the inverter circuit, M_2 is folded to allow ultra-low voltage supply application (Tae-Sung & Byung-Sung, 2006).

2.2.3.3 Inverter Circuit

An alternative topology which also uses current-reuse technique is the inverter circuit as shown in Figure 2-13. Instead of stacking M_1 with another NMOS, inverter circuit uses a PMOS to stack with M_1 (Bruccoleri, Klumperink, & Nauta, 2004). Since the current flows through the same path and therefore the total power consumption is deemed to be the same. By using PMOS, DC-biasing of M_2 can be lowered down and can be biased with the same DC source of M_1. Unlike stacking cascode common source and common gate topology, the RF signal is injected in both of the MOSFET gate terminal. Since both the NMOS and PMOS act as common source amplifiers, the outputs at V_{out} are in same phase which would combine constructively and increase the total signal power. The effective transconductance of the inverter at V_{out} is equal to $g_{mn} + g_{mp}$ where g_{mn} and g_{mp} are the transonductance of NMOS and PMOS respectively. Usually, the inverter circuit is connected with a feedback resistor between the drain and gate of the NMOS to provide input matching. Sometimes an inductor is integrated between the gate of M_1 and M_2 to resonate with the parasitic capacitance as well as forming the pi-matching network.

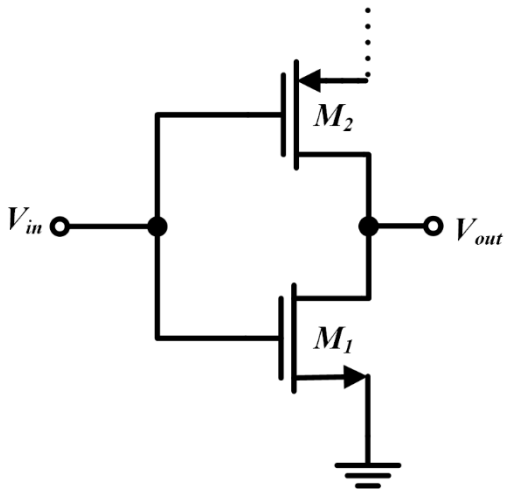


Figure 2-13: Inverter circuit.

2.2.3.4 Cross-Coupled Topology

The elaborate discussion of gain enhancement covers only on single-ended LNA. Alternatively, the LNA gain boosting could be achieved by adapting differential inputs which is a cross-coupled LNA as shown in Figure 2-14.

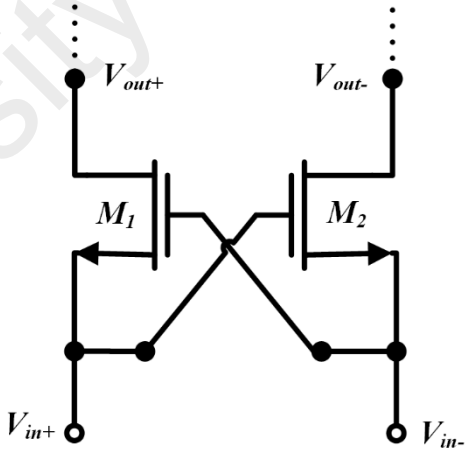


Figure 2-14: Cross coupled differential LNA.

Two MOSFETs M_1 and M_2 are connected between one source terminal to another gate terminal. V_{in+} flows into the non-inverting source terminal of M_1 but into the inverting gate terminal of M_2 and similarly, V_{in-} flows into the non-inverting source terminal of M_2 but into the inverting gate terminal of M_1. At the output of M_1, input V_{in+} is amplified by

the gain, A_{V1} and combine constructively with V_{in-} inverted signal. On the other hand, at the output of M_2, input V_{in-} is amplified by the gain, A_{V2} and combine constructively with V_{in+} inverted signal. The output signals can be expressed as,

$$\begin{aligned} V_{in+} &= -V_{in-} \\ V_{out+} &= V_{in+}A_{V1} - V_{in-}A_{V1} = 2V_{in+}A_{V1} \\ V_{out-} &= V_{in-}A_{V2} - V_{in+}A_{V2} = 2V_{in-}A_{V2} \end{aligned} \tag{2-29}$$

where V_{out+} and V_{out-} would be connected to the balun to initiate phase inversion and again to combine constructively. However, the disadvantages for cross-coupled differential LNA are high power consumption and it requires baluns to implement the circuit (Amer, Hegazi, & Ragai, 2007).

2.2.3.5 Cascade LNA Topology

In line with the scaling down of MOSFET in recent years, the allowable voltage headroom for MOSFET has been lowered. In order to achieve ultra-low voltage operation, the available voltage headroom supply could scale down to 0.4 V. Therefore, stacking cascode topology is not favorable in ultra-low voltage application. To achieve higher gain, LNA is cascaded for few stages to increase its total gain (Lin, Hsu, Jin, & Chan, 2007).

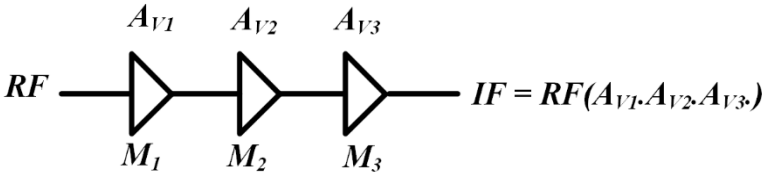


Figure 2-15: Cascade LNA topology to achieve higher gain.

Cascade LNA topology incorporates three stages of amplification is shown in Figure 2-15. The output is simply the multiplication of RF signal by the three stages of gain A_{V1}, A_{V2} and A_{V3}. However, the total power consumption of cascade LNA topology is the

summation of all currents flowing through each MOSFET multiplied by the voltage headroom supply and potentially the power consumption could be high.

Scaling down of MOSFET also introduces another design challenge which is the lowered allowable gate voltage bias. If the allowable voltage headroom supply, V_{DD} is 0.4 V then the highest gate voltage bias is also 0.4 V. Moreover, some CMOS platform has high threshold voltage, V_{TH} which makes the overdrive voltage, V_{GS} - V_{TH} smaller. Smaller overdrive voltage would result in weak inversion layer in MOSFET and reduces the gain and increases the noise of the amplifier significantly. To rectify this issue, forward body bias technique is introduced to lower down the threshold voltage and in turn to increase the overdrive voltage (Wu, Huang, Wong, & Wang, 2007). Threshold voltage equation of a NMOS device can be expressed as,

$$V_{TN} = V_{TO} + \gamma(\sqrt{|V_{SB} + 2\Phi_F|} - \sqrt{|2\Phi_F|} \quad (2\text{-}30)$$

where V_{TN} is the NMOS threshold voltage with the present of body bias, V_{SB} is the source-to-body voltage bias, V_{TO} is the threshold voltage without body bias, and Φ_F is the surface potential. From (2-30), in the present of forward body bias voltage, threshold voltage of NMOS device can be reduced. However, forward body bias voltage should not exceed a diode turn on voltage 0.7 V to avoid latch up of the device.

2.2.4 Noise-Cancelling Stage

If common gate amplifier is chosen as the first stage of the LNA, poor gain and noise performance of the common gate amplifier must be rectified. Figure 2-16 shows a common gate noise-cancelling stage where $V_{n1,in}$ is the M_1 input channel noise voltage and $V_{n1,out}$ is the output channel noise voltage.

M_1 channel noise can be model as a series noise voltage source connected to M_1 gate terminal. The channel noise is inverted in node *Y* but maintains its phase in node *X*. The

noise voltages then are channelled to M_2 and M_3 where both of the noise voltages will be amplified and inverted again and is maintained out of phase to each other. The noise voltages will combine destructively at the output and effectively cancels the M_1 channel noise. On the other hand, RF signals maintain its phase at node *X* and *Y* and both are in phase at node B and C which will combine constructively at the output. By using this technique, gain and noise performance of the LNA can be improved simultaneously (Blaakmeer, Klumperink, Leenaerts, & Nauta, 2008). M_2 can be replaced with a PMOS to achieve current reuse topology but at the penalty of limited voltage headroom available at the output. However, for ultra-wideband application, M_3 parasitic feedback path, C_{gd3} would jeopardize the performance of the circuit and requires plenty of optimization.

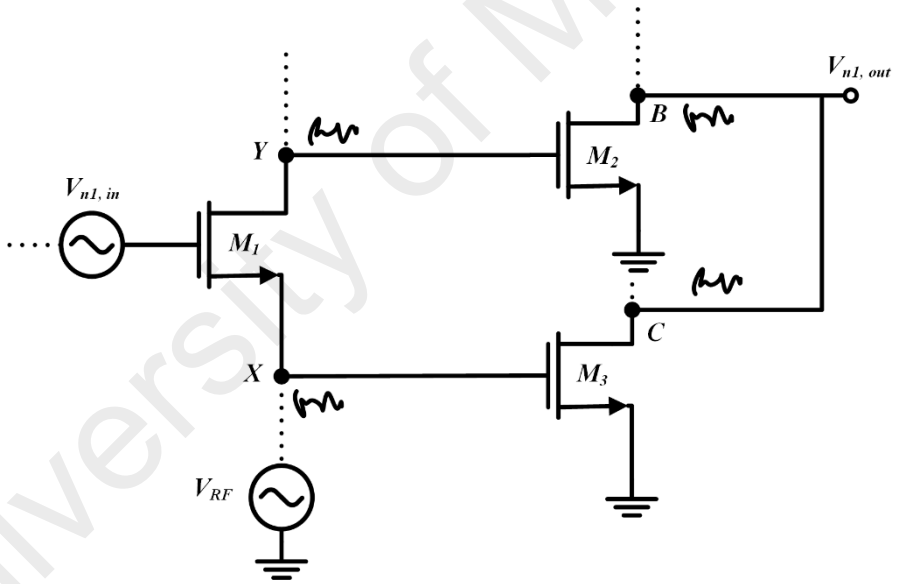


Figure Error! No text of specified style in document.**-16: Common gate noise-cancelling stage.**

Table 2-1 and Table 2-2 are included to summarize the discussed topologies and designs as well as the comparison of other reported works.

Table 2-1: Summary of the discussed topologies and designs.	
Topologies/Design	**Description**
Amplifier Type	
Single-ended LNA	Does not require balun. No insertion loss, additional noise to the circuit. Less power consumption.
Differential LNA	Ability to reject common-mode noise, power noise, second-order intermodulation products and improve dynamic range. Requires on-chip or off-chip balun which complicates the design and worsen noise, power, and insertion loss performance.
Common gate LNA	Ultra-wideband input matching without external matching circuit. Heavily depend on temperature and process. Lower gain to noise ratio due to restriction on transconductance.

Common source LNA	Requires additional input matching circuit. Better gain and noise performance.
Distributed LNA	Large chip area and power consumption. Flat gain and noise performance.
Input Matching	
Resistive termination	Easiest to implement. Large thermal noise and signal leakage.
Shunt-series resistive feedback	Lower gain and noise performance. Requires only extra resistor.
Inductive source degeneration	Large chip area due to large inductor. Narrowband response.
Filter matching	Requires many circuit components which makes the chip area large. Signal attenuation due to non-ideality of the filter.
Output Matching	
Resistive termination	Easy to implement. Requires inductor to neutralize the effect of parasitic capacitance.

Buffer	Less than unity gain. Requires tuning of the circuit.
Circuit Design	
Stacking cascade common gate	Same power consumption. High gain but lower dynamic range. Voltage headroom consumption. Great reverse isolation.
Stacking cascode common source	Same power consumption. Higher gain but lower dynamic range. Voltage headroom consumption. Good reverse isolation.
Folded cascode	Lower voltage supply. Requires PMOS which has worse noise and gain performance.
Inverter circuit	Same power consumption. Easy to implement input matching. High gain but lower dynamic range. Voltage headroom consumption.
Cross-coupled	Higher gain but requires differential inputs.

	Insertion loss, noise, and power contribution by balun.
Cascade LNA	Lower voltage supply. High gain but high power consumption. Better dynamic range compared to cascode LNA.
Noise-cancelling stage	Improve noise performance. Requires tuning of the circuit. Extra circuit components.

Table 2-2: Summary of the comparison between proposed LNA and reported works.	
Comparison between other reported LNA	Description
Proposed LNA	Largest bandwidth and highest IIP3 performance compare to other design. Utilized noise-cancelling and pi-matching network to improve noise and input matching performance. Relatively higher power consumption due to large bandwidth.
(Chung, Lee, Jeong, Yoon, & Kim, 2015)	Utilized inverter and feedback resistor to achieve input matching. CMOS parallel push-pull concept to achieve high IIP3 performance. Relatively smaller bandwidth.
(Bagga et al., 2014)	Utilized double-loop transformer feedback to achieve high gain and matching performance.

	Relatively lower power consumption but worse IIP3 performance due to high gain.
(Li, Feng, & Li, 2017)	Utilized $1/g_m$ input matching network, cascade and cascode method to achieve high gain. Worsen noise performance due to common gate amplifier as first stage of amplification. Buffer circuit as output matching network.
(Taibi, Trabelsi, Slimane, Saadi, & Belaroussi, 2017)	Utilized inductive source degeneration and buffer method to achieve input and output matching. Common source cascode with common gate as first stage amplification and cascade with another common source to achieve high gain performance. High gain performance worsen IIP3 performance.
(Razavi, 2010)	Utilized resistive feedback and resistive termination method to achieve input and output matching.

	Signal is cascaded by two common source amplifiers to achieve high gain performance. Included to the comparison due to its targeted applications is same with the proposed LNA.

CHAPTER 3:

CMOS LNA FOR COGNITIVE RADIO DESIGN

3.1 Design Consideration

With the depth of review in numerous reported ultra-wideband LNA design, the advantages and disadvantages of all the possible architecture are listed and considered. First of all, since cognitive radio has bandwidth of tenths of megahertz to ten gigahertz, power consumption of the LNA is usually sacrificed to obtain ultra-wideband performance with optimized noise, gain and matching. Therefore, in choosing between single-ended and differential LNA topology, single-ended LNA topology outshine the differential LNA topology simply because in single-ended LNA topology power consumption is half of the differential LNA. Moreover, differential LNA requires passive or active baluns at the input and output port which would increase the noise of the circuit. Hence, it is more suitable to implement differential solution at the mixer than in LNA.

In deciding for the first stage of the LNA, common source topology has more advantages than common gate topology. Although common gate topology has self-matching property, but the poor gain and noise response requires g_m-boosting and noise-cancellation technique to improve the gain and noise performance which in turn increases the total power consumption and complexity of the circuit. Besides, common gate self-matching is easily affected by process, voltage and temperature (PVT) variation and would add into the risk factor of fabricating the chip if input matching is just below -10 dB. On the other hand, although common source topology has no inherit self-matching property, but this setback can be easily solved by incorporating resistive feedback technique into the design. Furthermore, resistor is more reliable in PVT variation.

Resistors are incorporated into the circuit design in order to achieve ultra-wideband response in gain and noise and the resistors would consume voltage headroom which

results in lower dynamic range and linearity. If common gate topology is implemented as the first stage of the LNA, two resistors are required to be integrated at the drain and source of the common gate amplifier and therefore reduces the dynamic range and linearity drastically. In comparison, common source topology only requires one resistor connected to the drain of the amplifier and results in higher dynamic range and linearity. To further improve the dynamic range and linearity, stacking amplifier topology is avoided but a cascade topology is adapted into the design. Finally, peaking inductors are incorporated in the design to improve the LNA performance at high frequencies.

3.2 Proposed LNA Architecture

Accounting for the design restriction, the proposed LNA architecture is realized in 0.13 μm standard CMOS technology. The proposed LNA architecture uses cascade topology is shown in Figure 3-1. The proposed LNA is divided into two stages in which the first stage is the input matching and gain stage while the second stage is the output matching and gain enhancement stage. In Figure 3-1, RF and IF is input and output respectively whereas C_1 and C_2 are both off-chip ac-coupling capacitors. Inductors L_{D1}, L_{D2}, and L_{D3} are peaking inductors that are incorporated into the design to compensate the effect of parasitic capacitances. R_{D1}, R_{D2}, and R_{D3} are used to provide the DC bias for MOSFET's gates as well as to set the gain of the LNA. By using self-bias method, the need of current mirror is alleviated and the chip area of the LNA can be made smaller without the presence of on-chip ac-coupling capacitor. R_F is the feedback resistor to provide the 50 ohms input matching. L_G is used to resonate with M_1 and M_2 gate parasitic capacitances and to form a π-matching network. The π-matching network provides another minimum peak in high frequency in order to improve the input matching. The substrate and deep N-well of all the MOSFETs are tied to ground and VDD respectively to avoid substrate/well conduction. An inductor can be placed in between output of first stage and input of second stage to resonate with M_3 gate capacitance but the integration

of an inductor would make the number of inductors uneven and increase the overall chip area.

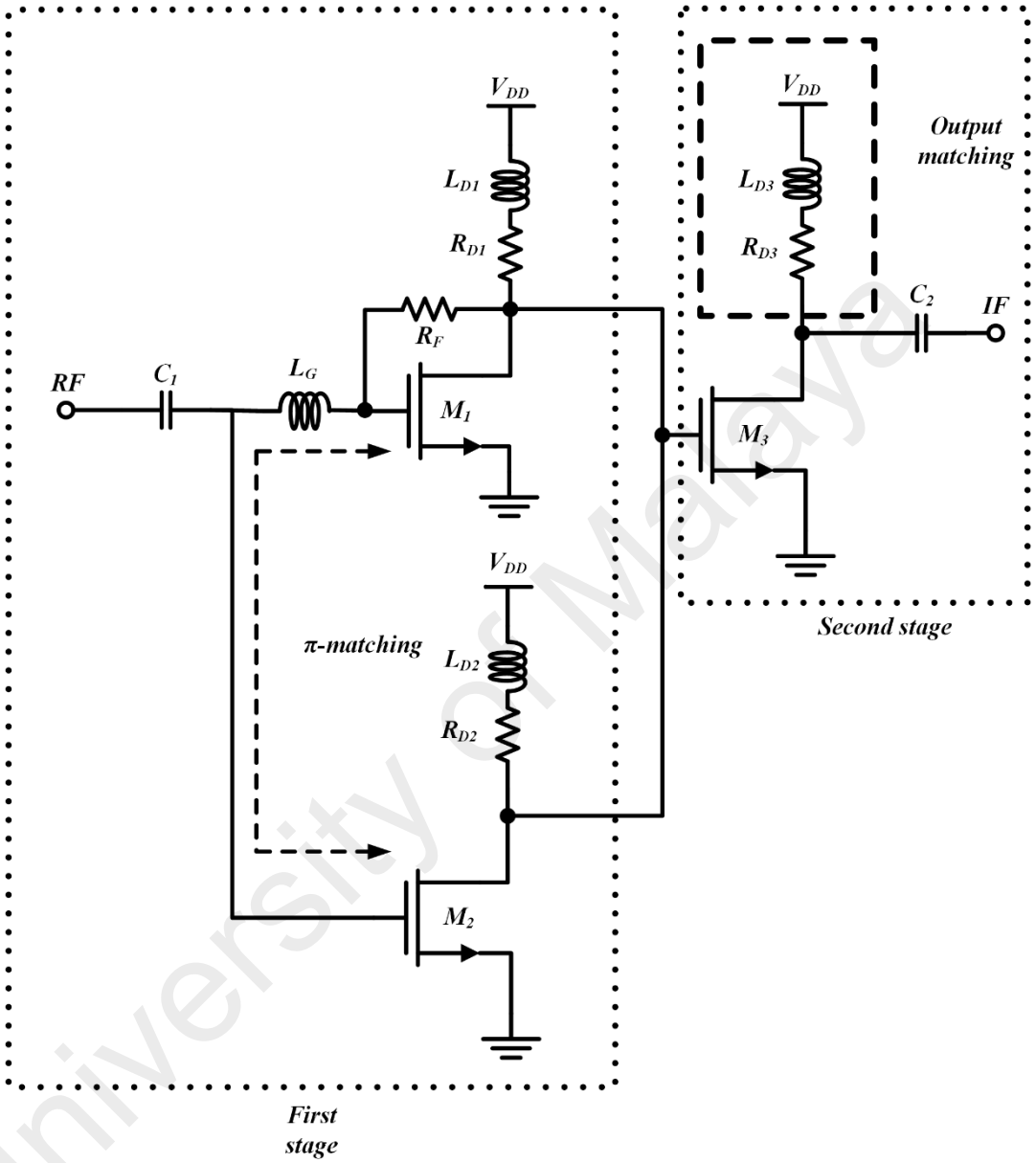


Figure 3-1: Proposed LNA architecture.

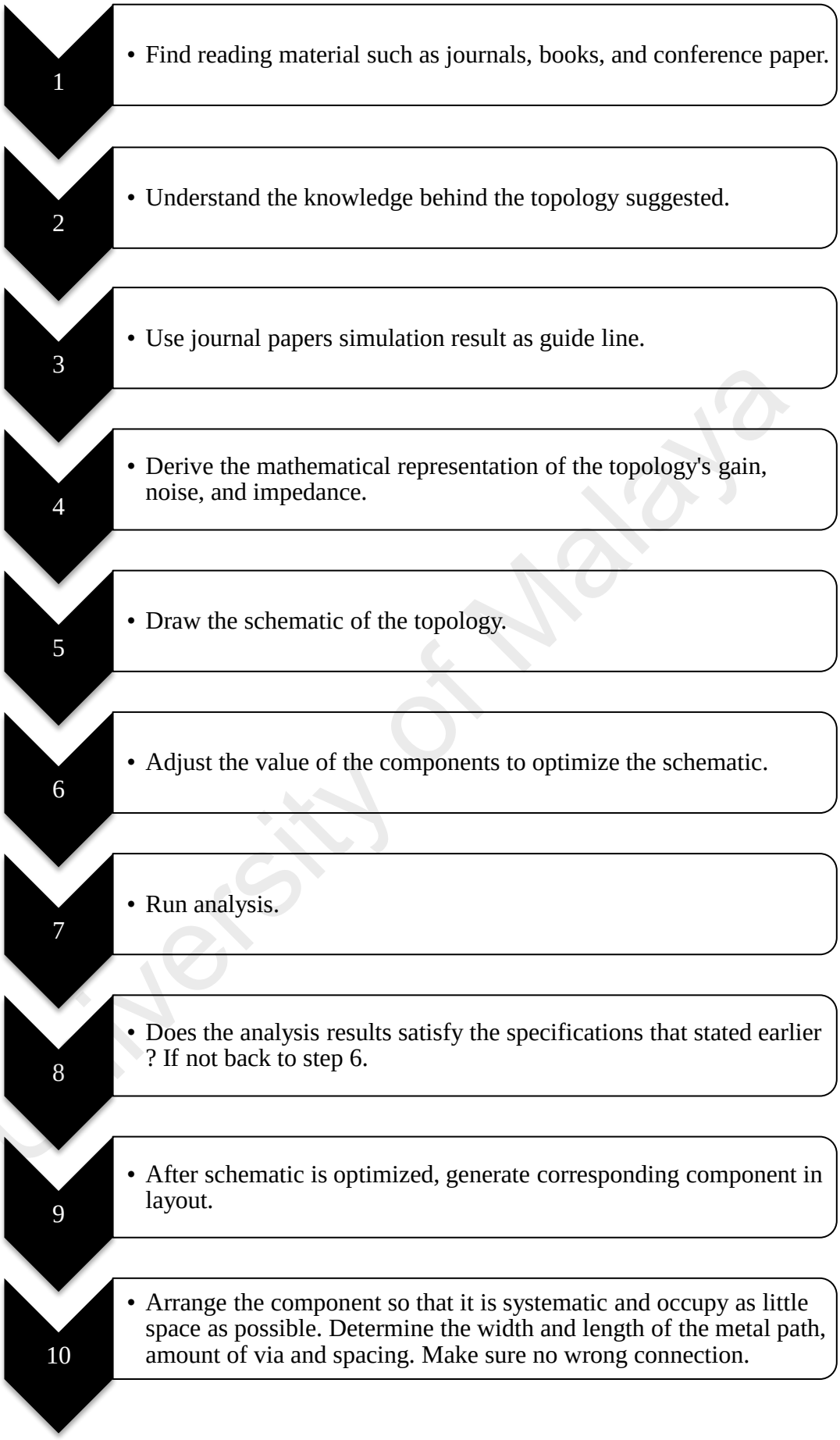
At the first stage, RF signal is split into two paths and amplified by M_1 and M_2 respectively. Since M_1 and M_2 outputs are in same phase, the RF signals would combine constructively at the output. M_1 can be replaced with a PMOS to establish the inverter topology to reduce power consumption with a penalty of reduced dynamic range and linearity of the circuit. The difference in C_{gs} value of NMOS and PMOS would complicate

the realization of π-matching network and self-bias method. M_1 and M_2 outputs are then cascaded into second stage common source amplifier to further improve the gain of the circuit. The values for all the components shown in Figure 3-1 are listed in Table 3-1.

Table 3-1: Circuit component values of the proposed LNA.

Parameters	Design Values
$\left(\frac{W}{L}\right)_{M_1}, \left(\frac{W}{L}\right)_{M_2}$	96 µm/ 0.13 µm
$\left(\frac{W}{L}\right)_{M_3}$	134 µm/ 0.13 µm
L_{D1}, L_{D2}	3.5 nH
L_G	0.85 nH
L_{D3}	0.75 nH
R_F	280 Ω
R_{D1}, R_{D2}	70 Ω
R_{D3}	25 Ω
C_1, C_2	1 uF

The size of M_1 and M_2 are made equal to obtain same C_{gs} values to establish π-matching network. Total width of the MOSFET W, is given as, W = (number of finger)*(finger width)*(multiplier). Number of finger is increased to highest to achieve the lowest noise figure. All the on-chip resistors are paralleled to achieve at least 500 ohms of resistance in each resistor to reduce the effect of process variation. However, there are some parasitic capacitance in each resistor and would add up when the resistors are in parallel which results in degradation on the LNA performance. Fortunately, these parasitic capacitance can be countered by adjusting the value of peaking inductors. Flow chart of the design and measurement process is simplified and shown in Figure 3-2.



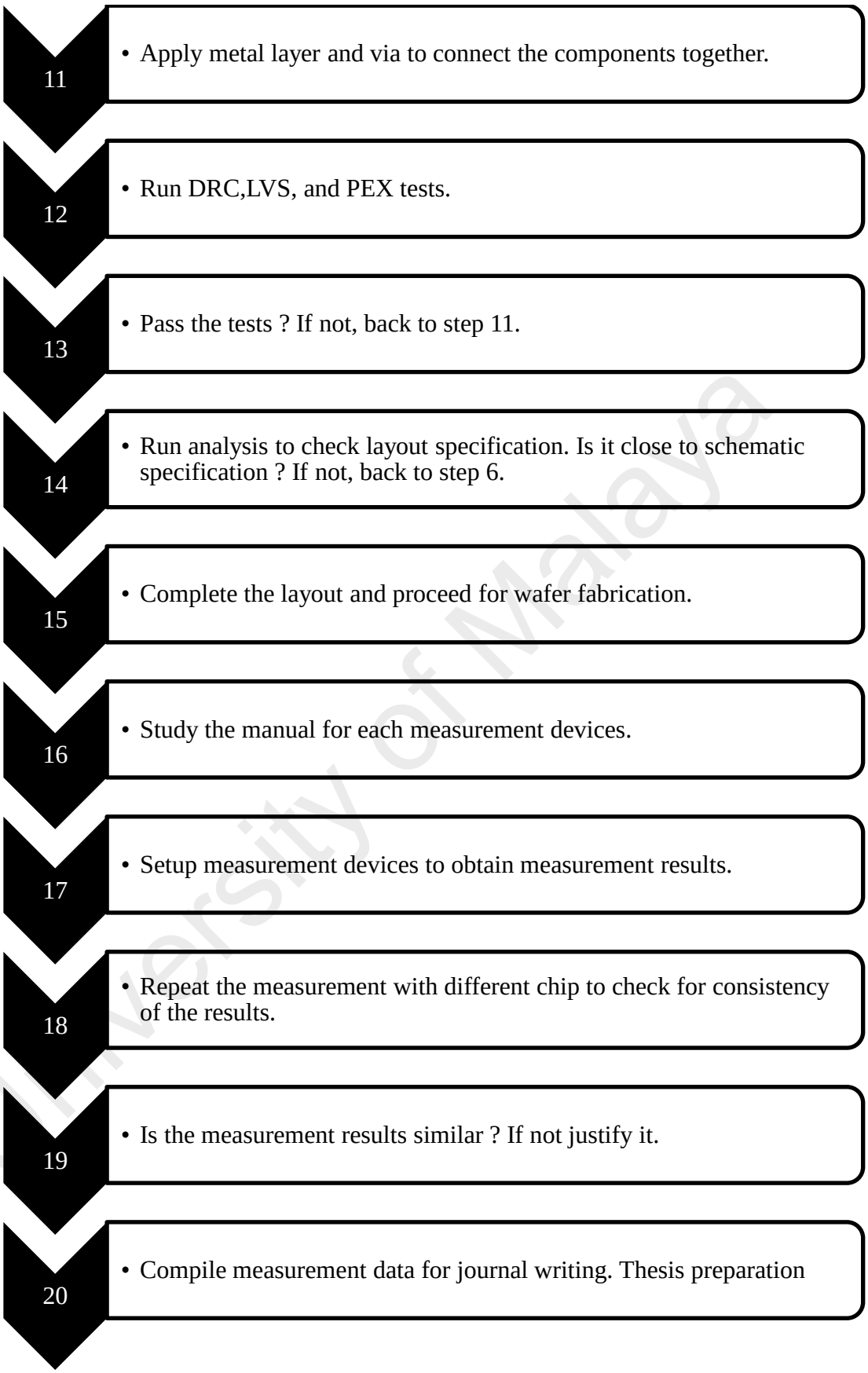


Figure 3-2: Flow chart of the design and measurement process.

3.3 Proposed LNA Circuit Analysis

In this section, input and output matching analysis, small signal gain analysis and noise analysis of the proposed LNA will be discussed.

3.3.1 Input and Output Matching Analysis

The proposed LNA uses resistive feedback technique to achieve ultra-wideband input matching. Since M_1 and M_2 are identical in parameters, therefore the small signal analysis of M_1 is sufficient. The equivalent small signal model of M_1 is shown in Figure 3-3.

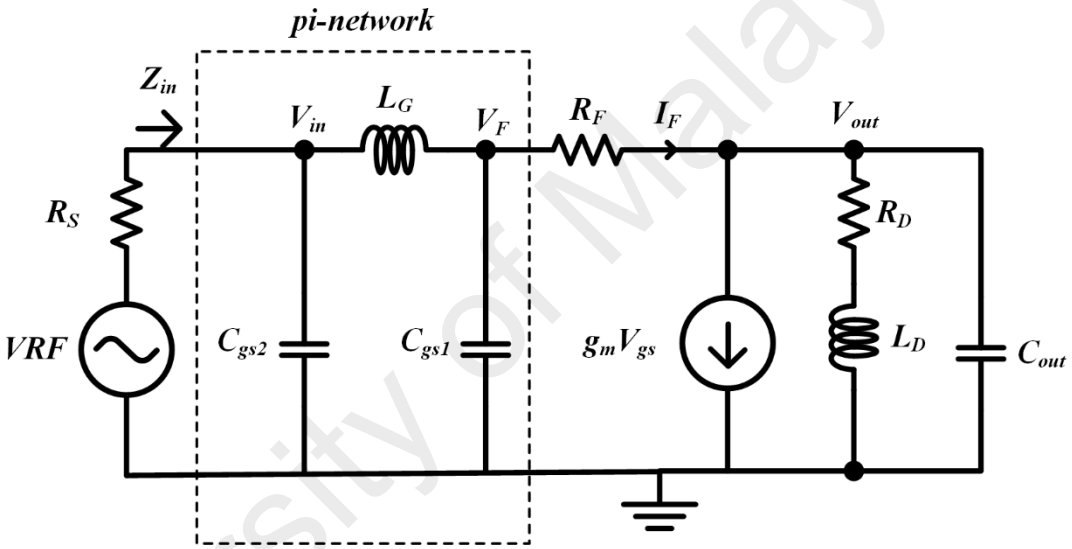


Figure 3-3: Equivalent small signal model of input matching.

At low frequency, C_{gs1} and C_{gs2} can be considered as open circuit and L_G as a short. Therefore, in low frequency the pi-network can be ignored. If the impedance looking in from V_F node is equal to R_S then V_F = ½ V_{RF} and good impedance matching can be achieved with maximum power transfer and minimum insertion loss. To compute the equivalent impedance looking in V_F node, assuming that a voltage source V_S is connected parallel with V_F which gives $V_S = V_F$ and has a current I_S. The equivalent impedance $Z_{eq} = V_S/I_S$ can be derived as follow,

$$\frac{V_S}{I_S} = Z_{eq} = \frac{R_F + Z_D}{1 + g_m Z_D} \approx \frac{R_F + R_D}{1 + g_m R_D} \approx R_{eq} \tag{3-1}$$

where $Z_D = (R_D + sL_D) \,||\, 1/sC_{out}$ *and* $R_D + sL_D = (R_{D1} + sL_{D1}) \,||\, (R_{D2} + sL_{D2})$. C_{out} is the total parasitic capacitance at the output of M_1 which consists of C_{gd1}, C_{gd2}, and C_{gs3}. From (3-1), Z_{eq} can be made equal to 50 ohms by carefully selecting the parameters. As the frequency increases, C_{gs} of the MOSFET reduces and impedance Z_{in} looking in from node V_{in} is no longer equal to Z_{eq} and this would result in deterioration of the input reflection S11. A filter circuit can be implemented by utilizing C_{gs} and adapting on-chip inductor and capacitor to introduce another minimum peak at high frequency to maintain the input matching. In this proposed LNA, another identical MOSFET, M_2 is used to provide the necessary component to establish π-matching network together with inductor L_G. The advantages of using MOSFET over on-chip capacitor are MOSFET can provide higher gain and it has smaller size compare to an on-chip capacitor. However, the disadvantage of incorporating M_2 into the design is the increase in power consumption. Assuming the high frequency operation, L_D resonate with C_{out} so that $Z_{eq} = R_{eq}$, the high frequency input impedance can be derived as,

$$Z_{in} = \frac{s^2 L_G C_X R_{eq} + sL_G + R_{eq}}{s^3 C_X{}^2 L_G R_{eq} + s^2 C_X L_G + 2sC_X R_{eq} + 1} \tag{3-2}$$

where $C_X = C_{gs1} = C_{gs2}$. By substitute Z_{in} to R_S, the roots of Z_{in} can be determined as,

$$\omega_1 = 0 \tag{3-3}$$

$$\omega_2 = \sqrt{\frac{L_G - 2C_X R_X{}^2}{C_X{}^2 L_G R_X{}^2}} \tag{3-4}$$

where $R_X = R_S = R_{eq}$. (3-2) will be verified in simulation and measurement result. The effect of M_2 and L_G to form pi-matching network will be discussed in simulation result.

Resistive termination method is adapted into the LNA output to achieve output impedance matching. At low frequency, the output impedance is simply the resistance value of R_{D3} coupled with parasitic resistance at the output. However, in high frequency, parasitic capacitance at the output of M_3 changes the output impedance and hence peaking inductor L_{D3} is incorporated at the output to maintain the performance of output reflection S22. Output impedance can be simplified as $(R_{D3} + sL_{D3}) \parallel 1/sC_{out3}$ where sC_{out3} is the output parasitic capacitance at M_3 which consist of C_{gd3} and the input capacitance of the next stage. Output impedance can be derived as,

$$Z_{out} = \frac{R_{D3} + sL_{D3}}{s^2 C_{out3} L_{D3} + sC_{out3} R_{D3} + 1} \tag{3-5}$$

By incorporating peaking inductor in the output network, it introduces a real root in Z_{out} which would result in a minimum peak in S22. The peaking inductor value is chosen deliberately to result in a minimum peak in the center of the bandwidth and will be verified in the simulation result.

3.3.2 Gain Analysis

The proposed LNA uses two common source amplifiers as first stage of amplification. The output signal of both common source amplifier is combined constructively and results in higher gain. The first stage output is then cascaded to second stage amplifier for further amplification. Assuming an input matched condition, $R_S = R_{eq}$ and therefore $V_F = ½\ V_{RF}$, the gain of M_1 can be expressed as,

$$\frac{V_{out,1}}{V_{RF}} = -\frac{1}{2}(g_{m1} - \frac{1}{R_F})(Z_D \parallel R_F) \tag{3-6}$$

where $V_{out,1}$ is the output voltage of M_1. Since M_1 and M_2 parameters are identical, therefore $g_{m1} = g_{m2} = g_{mx}$ and $Z_{D1} = Z_{D2} = Z_{DX}$, the total gain of the proposed LNA, V_{total} can be derived as,

$$\frac{V_{total}}{V_{RF}} = (g_{mx} - \frac{1}{R_F})(Z_{DX} \parallel R_F) g_{m3} Z_{D3} \tag{3-7}$$

The total gain of the proposed LNA can be made higher by increasing the transconductance of the MOSFETs and resistance of R_F. However, higher transconductance leads to higher power consumption and R_F has little degree of freedom to adjust as it is tied closely with input matching. On the other hand, increase of Z_{DX} and Z_{D3} able to improve the gain but the former is used to bias the gate of the MOSFETs and the parameters must be adjusted diligently while the latter is used to provide output matching. The effect of M_2 in improving the gain will be shown in Chapter 4.

3.3.3 Noise Analysis

Noise factor of a system is measured by signal to noise ratio of input and output and the equation is given as,

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{3-8}$$

where SNR_{in} is the ratio of input signal to noise of R_S and SNR_{out} is the ratio of output signal to noise of R_S and additional noise from LNA circuit itself. SNR_{in}, SNR_{out} and F can be rewritten as,

$$SNR_{in} = \frac{S_{in}}{N_{in}} \tag{3-9}$$

$$SNR_{out} = \frac{G_{LNA} \cdot S_{in}}{G_{LNA} \cdot N_{in} + N_{LNA}} \tag{3-10}$$

$$F = \frac{\frac{S_{in}}{N_{in}}}{\frac{G_{LNA} \cdot S_{in}}{G_{LNA} \cdot N_{in} + N_{LNA}}} = 1 + \frac{N_{LNA}}{G_{LNA} \cdot N_{in}} \tag{3-11}$$

where G is the gain of the LNA. Noise figure is defined as noise factor in dB and can be expressed as,

$$NF = 10\log(F) = 10\log\left(\frac{SNR_{in}}{SNR_{out}}\right) = 10\log(1 + \frac{N_{LNA}}{G_{LNA} \cdot N_{in}}) \tag{3-12}$$

From (3-12), in order to obtain low noise figure, high gain and low internal LNA noise is required. Referring to Figure 3-1, the components that contribute significantly to noise figure are the channel noise of M_1, M_2, and M_3 and thermal noise of R_D and R_F where $R_D = R_{D1} = R_{D2}$. By viewing noise components of the LNA as noise voltage, the noise figure of each components can be obtained by taking the ratio of each component's output noise voltage to the amplified input noise voltage. (3-12) can be rewritten as,

$$NF = 10\log(1 + \frac{F_{R_F}}{F_N} + \frac{2F_{M_1}}{F_N} + \frac{F_{M_3}}{F_N} + \frac{2F_{R_D}}{F_N}) \tag{3-13}$$

where $F_N = (G_{LNA})(N_{in})$ and all the noise components can be derived as,

$$\begin{aligned} F_{R_F} &= \frac{4kTR_F(g_{m3}Z_{D3})^2}{4kTR_s\left[(g_{mx} - \frac{1}{R_F})(Z_{DX} \parallel R_F)(g_{m3}Z_{D3})\right]^2} \\ &= \frac{R_F}{R_S[(g_{mx} - \frac{1}{R_F})(Z_{DX} \parallel R_F)]^2} \end{aligned} \tag{3-14}$$

$$
\begin{aligned}
F_{M_1} &= F_{M_2}, \\
&= \frac{4kT\frac{\gamma}{\alpha}g_{mx}(g_{m3}Z_{D3}Z_{DX})^2}{4kTR_s[(g_{mx}-\frac{1}{R_F})(Z_{DX}\parallel R_F)(g_{m3}Z_{D3})]^2} \\
&= \frac{\gamma}{\alpha}\frac{g_{mx}Z_{DX}{}^2}{R_s[(g_{mx}-\frac{1}{R_F})(Z_{DX}\parallel R_F)]^2}
\end{aligned}
\tag{3-15}
$$

$$
\begin{aligned}
F_{M_3} &= \frac{4kT\frac{\gamma}{\alpha}g_{m3}(Z_{D3})^2}{4kTR_s[(g_{mx}-\frac{1}{R_F})(Z_{DX}\parallel R_F)(g_{m3}Z_{D3})]^2} \\
&= \frac{\gamma}{\alpha}\frac{1}{g_{m3}R_s[(g_{mx}-\frac{1}{R_F})(Z_{DX}\parallel R_F)]^2}
\end{aligned}
\tag{3-16}
$$

$$
\begin{aligned}
F_{R_D} &= \frac{4kTR_D(g_{m3}Z_{D3})^2}{4kTR_S[(g_{mx}-\frac{1}{R_F})(Z_{DX}\parallel R_F)(g_{m3}Z_{D3})]^2} \\
&= \frac{R_D}{R_s}\frac{1}{[(g_{mx}-\frac{1}{R_F})(Z_{DX}\parallel R_F)]^2}
\end{aligned}
\tag{3-17}
$$

where k is the Boltzmann constant, T is the temperature in Kelvin, γ is the channel noise coefficient, $\alpha = g_{d0}/g_m$ and g_{d0} is the drain-source conductance in triode region. From (3-14) to (3-17), it is shown that the total noise figure can be reduced by increasing the transconductance with a drawback of increase in power consumption. M_1 and M_2 has the same noise figure as both have equal physical and operational parameters. On the other hand, the proposed LNA has the noise-cancelling topology suggested in (Razavi, 2012). In order to achieve lower noise figure, M_2 is also used as inverting amplifier to cancel the noise of M_1 as shown in Figure 3-4.

Noise current of M_1 at node Y flows through R_F and R_S and has a voltage of V_X at node X. Noise current at node Y and X is in phase but it is inverted by M_2 and recombine at

node *Y*. The inverted noise current of M_2 will combine destructively with the noise current component of M_1 and hence noise current of M_1 can be cancelled out. The noise voltage at V_Y and V_X ratio can be expressed as,

$$\frac{V_Y - V_X}{R_F} = \frac{V_X}{R_S}$$
$$\frac{V_Y}{V_X} = 1 + \frac{R_F}{R_S} \tag{3-18}$$

Therefore, in order to cancel the noise at node *Y*, A_1 gain is chosen as $1 + R_F/R_S$. The effect of M_2 in lowering the total noise of the LNA will be shown in simulation verification.

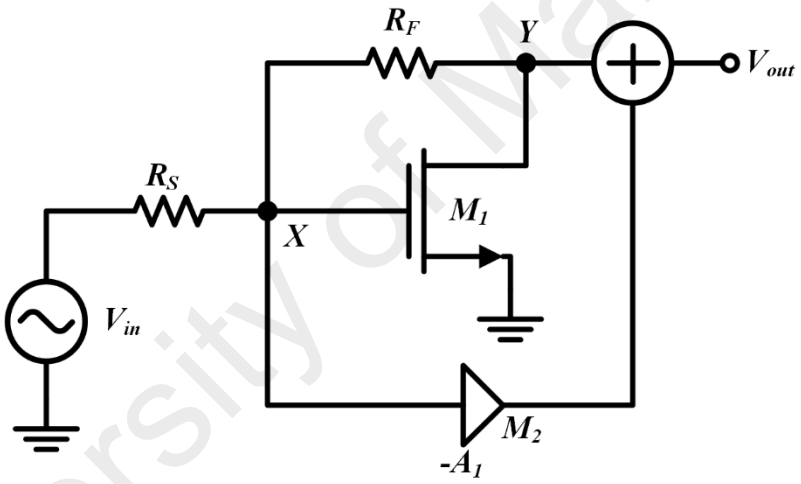


Figure 3-4: Noise-cancelling method of the proposed LNA.

3.4 Measurement Devices Analysis

The measurement devices included vector network analyzer (VNA), power signal generator (PSG), power signal analyzer (PSA), noise figure analyzer (NFA), and parameter analyzer (PA). The specifications of the devices will be discussed and their functions are explained.

3.4.1 Vector Network Analyzer

VNA as shown in Figure 3-5 has an operating frequency range from 45 MHz to 50 GHz and the model name is Agilent E8364B. The dynamic range of VNA is 104 dB. In order to obtain accurate results, VNA has to be calibrated. VNA is calibrated by connecting the input and output together via a load test and the discrepancy caused by ac-coupling capacitors as well as input and output cables can be eliminated. The calibrated VNA should show 0 dB of input and output matching response together with minimum reading of forward voltage and reverse voltage gain. VNA is used to measure S-parameters and P1dB of the device and it has 50 ohms input and output impedance.

Figure 3-5: Vector network analyzer that was used in measurement setup.

3.4.2 Power Signal Generator

PSG as shown in Figure 3-6 has an operating frequency range of 250 kHz to 26.5 GHz and the model name is Agilent E8267D. It has an output impedance of 50 ohms which implies that the proposed LNA should match the impedance of the PSG to reduce the reflection of the input power signal. The maximum output power is 20 dBm which is sufficient to measure IIP3 response of the proposed LNA. The PSG is capable of generating two-tone signal as output which eliminate the need of power combiner and two unit of PSG.

Figure 3-6: Power signal generator that was used in measurement setup.

3.4.3 Power Signal Analyzer

PSA as shown in Figure 3-7 has an operating frequency range of 3 Hz to 26.5 GHz and the model name is Agilent E4440A. It has input impedance of 50 ohms which implies that the proposed LNA should match the impedance of the PSA to reduce the reflection of the output power signal. The maximum input power is 30 dBm which is sufficient to measure the IIP3 response of the proposed LNA.

Figure 3-7: Power signal analyzer that was used in measurement setup.

3.4.4 Noise Figure Analyzer

NFA as shown in Figure 3-8 has an operating frequency of 10 MHz to 26.5 GHz and the model name is Agilent N8975A. It has input impedance of 50 ohms which implies that the proposed LNA should match the impedance of the NFA to obtain accurate noise figure response. Since the NFA has < 12 dB instrument noise figure from the frequency

range of 3 GHz to 13.2 GHz at the temperature of 20 to 26 degree Celcius, it has to be calibrated to eliminate the instrument noise figure. An external amplifier is recommended to further suppress the instrument noise figure.

Figure 3-8: Noise figure analyzer that was used in measurement setup.

3.4.5 Parameter Analyzer

PA as shown in Figure 3-9 has the function of providing ± 200 V and ± 1 A which is sufficient to power on the proposed LNA. The model name is Agilent 4156C and with 1 femtoamp and 0.2 microvolt measurement resolution.

Figure 3-9: Parameter Analyzer that was used in measurement setup.

CHAPTER 4:

SIMULATION AND MEASUREMENT ANALYSIS

4.1 Simulation Result

After rigorous optimization of the proposed circuit, the desired performances have been achieved. The layout of the proposed LNA is drawn and verified. To optimize the layout of the proposed LNA to achieve minimum possible chip area, tests such as design rule check (DRC), layout versus schematic test (LVS), and parasitic extraction test (PEX) are carried out to check on any design rule violation, discrepancy between layout and schematic, and in verifying the parasitic capacitance and resistance that are contributed due to the metal paths.

4.1.1 Layout

Figure 4-1 shows the layout of the proposed LNA. The left hand side of the layout is the RF input bondpads with the configuration of GSG with each bondpad separation of 150 µm to fulfill the fabrication requirement and the right hand side of the layout is the IF output bondpads with the same configuration as the input. Located at the bottom of the layout is the DC supply with the configuration of Signal-Ground-Signal (SGS). The active area of proposed LNA is shielded with double guard rings with one terminal connected to VDD and another terminal connected to ground. Both of the guard rings separation is small to intentionally create large parasitic capacitance in order to short any surrounding noise and power supply noise to the ground. The layout including bondpads has an area of 0.77 mm^2 and the active area of the proposed LNA consumes an area of 0.33 mm^2. In the schematic design, no on-chip capacitor used in between input path and output path. However, when layout is drawn, there is a large void around the IF path. In order to reduce the void, dummy on-chip capacitors are inserted into the layout with one

terminal connected to VDD and another terminal connected to ground. It serves the same purpose as the guarding to short any surrounding noise to the ground.

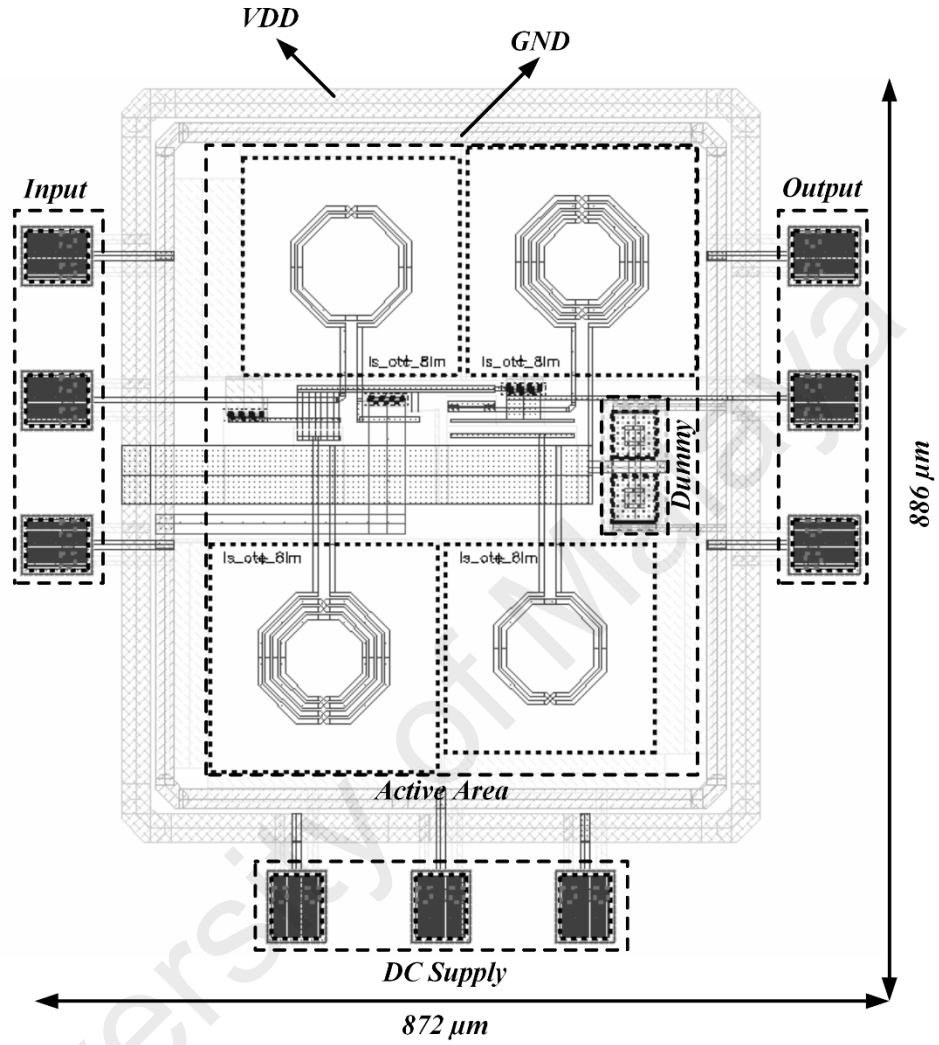


Figure 4-1: Layout of the proposed LNA.

4.1.2 Input and Output Matching

Figure 4-2 shows the simulated S11 plot of the proposed LNA with and without incorporating π-matching network. For the S11 curve with π-matching network, it can be observed that there are two minimum peaks which are at near zero frequency and at around 7 GHz. The simulation result confirms with the (3-2) and obtains a S11 response of below -10 dB for the entire band of operation. On the other hand, if the proposed LNA is implemented without incorporating a π-matching network or a second/third-order filter, the S11 response exceeds -10 dB at the frequency above 7 GHz and reach as high as -7.3

dB at 10 GHz. Such input matching response would result in large insertion power loss and result in weak amplified signal.

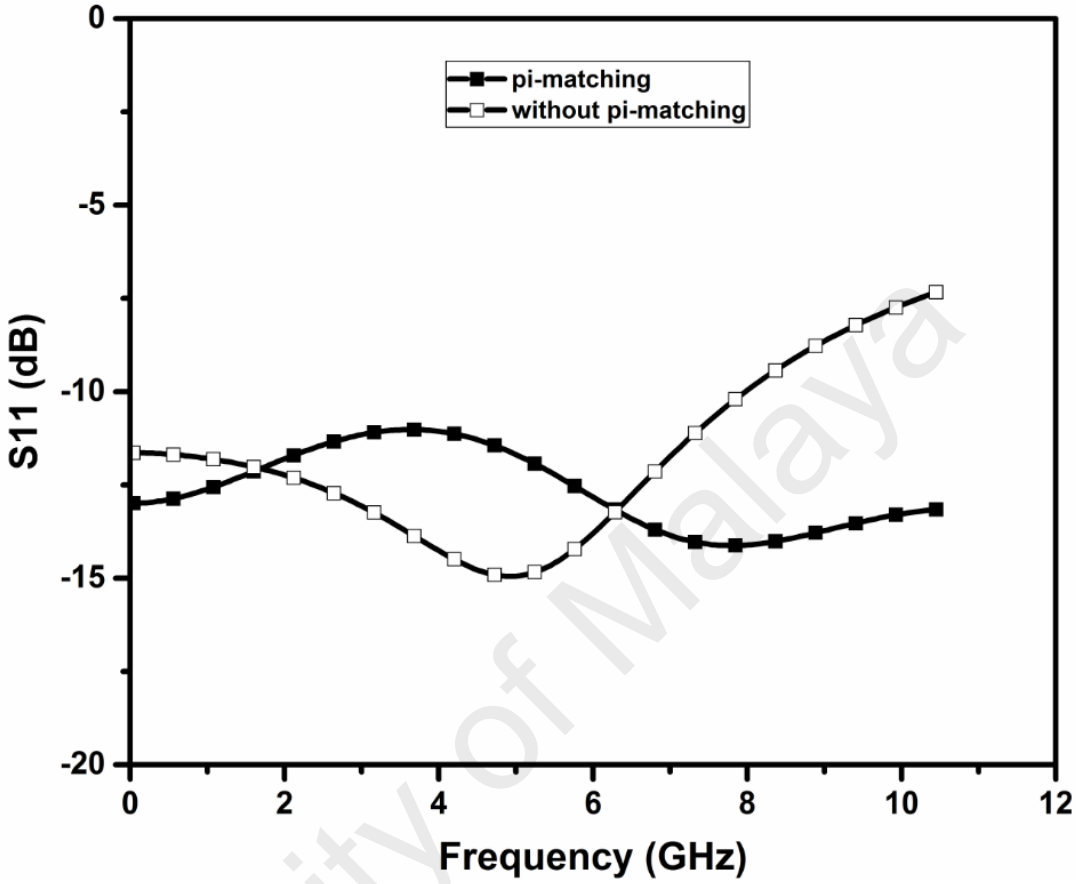


Figure 4-2: Simulated input matching response, S11 of the proposed LNA.

Figure 4-3 shows the simulated output matching response, S22 with and without peaking inductor L_{D3}. With the presence of peaking inductor, S22 response achieve better than -10 dB of output matching in the entire band of operation. The incorporation of peaking inductor introduces a minimum peak at around 6 GHz as proven in (3-5). On the other hand, if the proposed LNA is implemented without the output peaking inductor, the S22 response would rise to above -10 dB for the entire band of operation and reach to a maximum of -5.5 dB. Such a response would result in large output reflection coefficient and reduce the available signal power at the output port. The incorporation of peaking inductor into the design has successfully minimize the effect of parasitic capacitance at the output port. The proposed LNA peaking inductors have low Q-factor to minimize the layout area and to widen the peaking response.

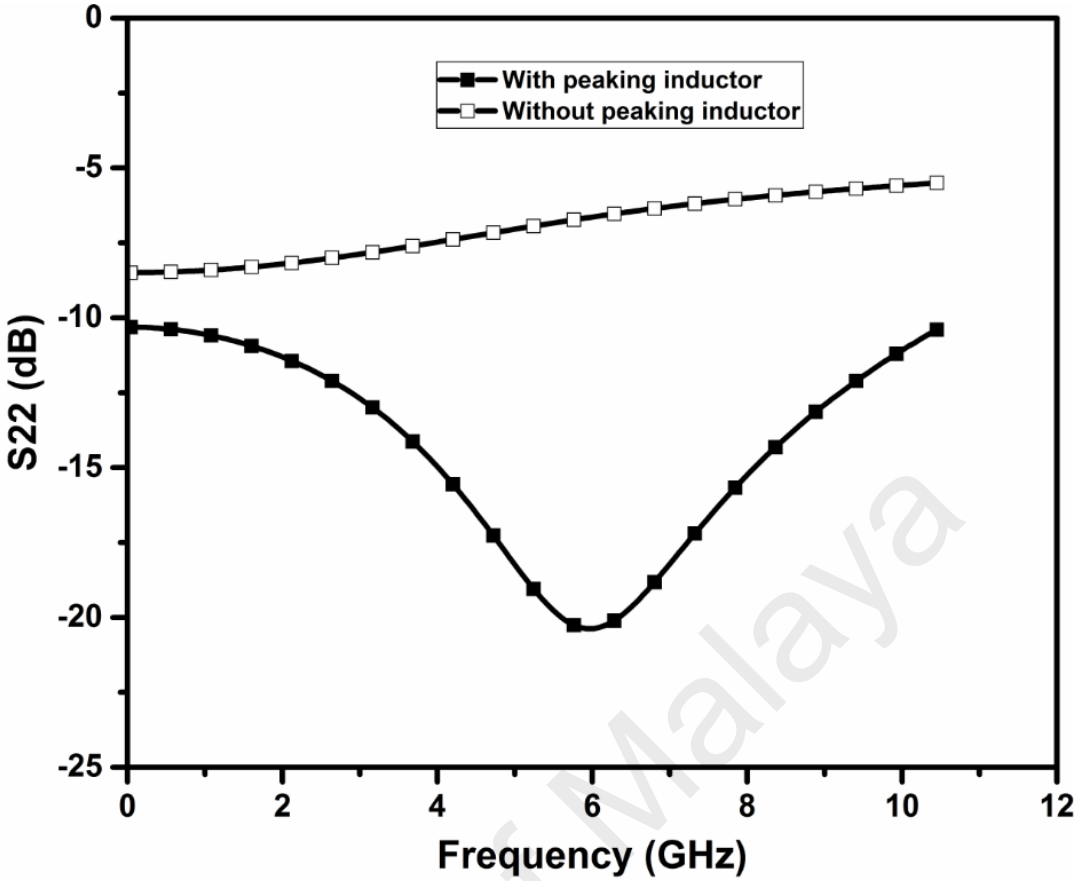


Figure 4-3: Simulated output matching response, S22 of the proposed LNA.

4.1.3 Gain

Figure 4-4 shows the simulated LNA gain response, S21 with and without M_2 amplifier stage. Higher gain response can be observed when M_2 is ON and the LNA achieves gain higher than 11.8 dB with a maximum of 15.6 dB. The gain difference between M_2 ON and M_2 OFF is small due to the mismatch of signal phases at output of M_1 and M_2 that caused by the feedback resistor, R_F and L_G. Nevertheless, the gain of the LNA is improved by using M_2 to establish π-matching network instead of using lossy on-chip capacitor. Additionally, incorporation of M_2 also helps to achieve input matching and noise reduction.

Figure 4-5 shows the simulated LNA gain response, S21 with and without peaking inductors L_{D1}, L_{D2}, and L_{D3}. The gain of the LNA in high frequency is largely improved by using peaking inductors. On the other hand, the gain of the LNA without peaking

inductors plunges below 10 dB after 3.5 GHz and continues to decrease until 4 dB at 10 GHz. Peaking inductors method is sometimes referred as bandwidth extension method.

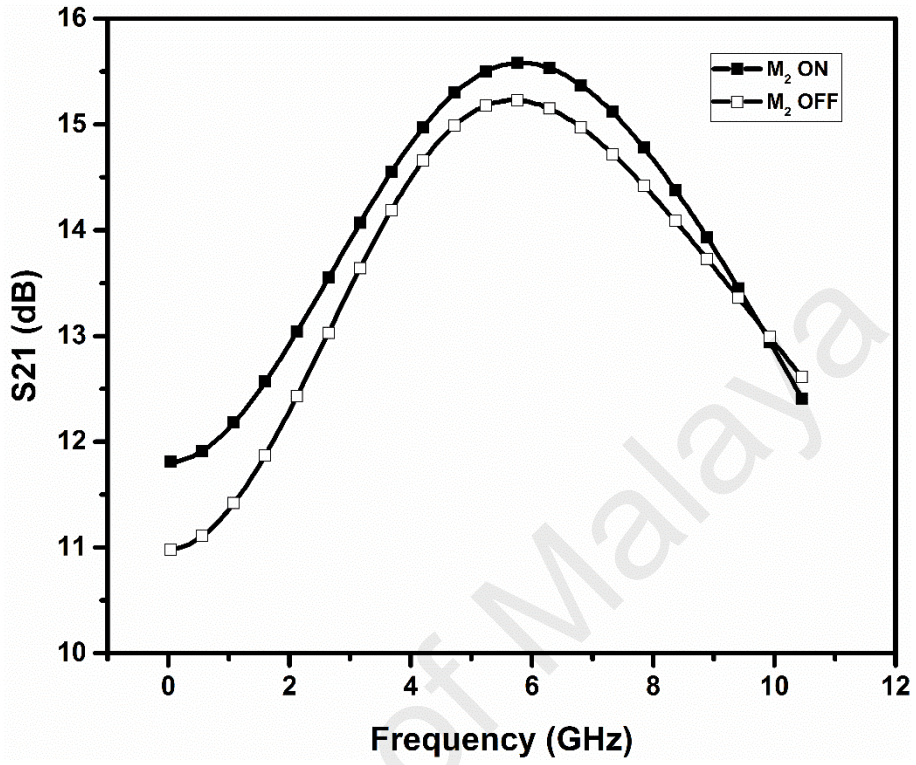


Figure 4-4: Simulated forward voltage gain response, S21 of the proposed LNA with and without M_2.

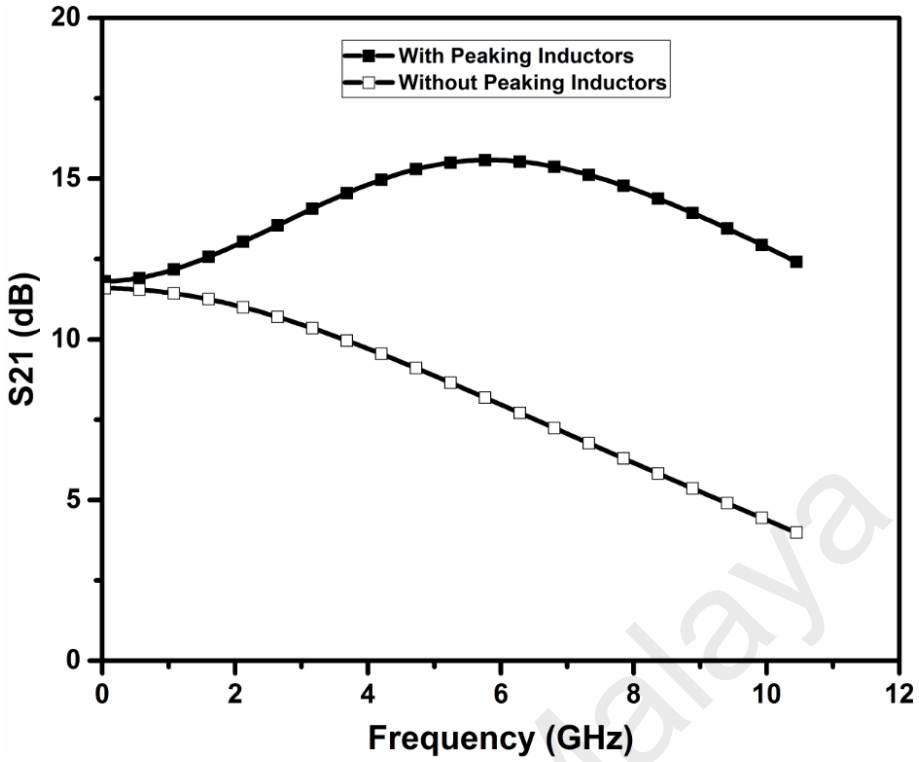


Figure 4-5: Simulated forward voltage gain response, S21 of the proposed LNA with and without peaking inductors.

4.1.4 Reverse Isolation

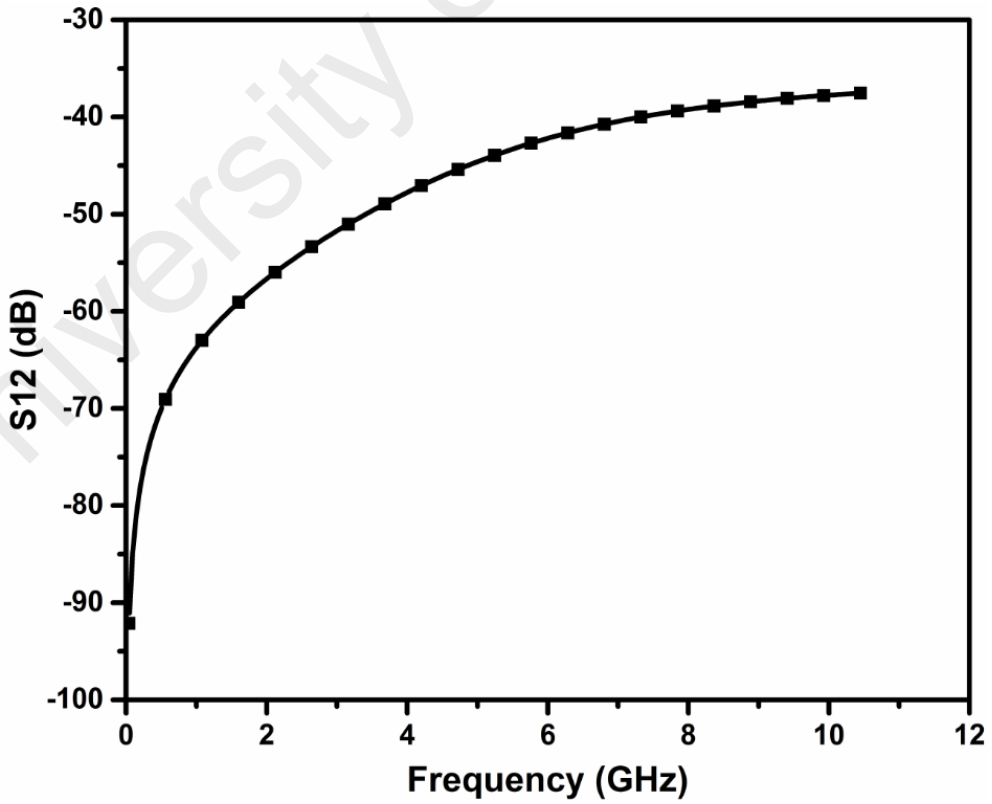


Figure 4-6: Simulated reverse voltage gain response, S12 of the proposed LNA.

Figure 4-6 shows the simulated reverse voltage gain response, S12 of the proposed LNA. The proposed LNA shows low reverse voltage gain or in other words good reverse isolation in low frequency. The low frequency reverse voltage gain is observe to be as low as -92 dB. As mentioned in Chapter 2, common source amplifier has lower reverse isolation than common gate amplifier due to the existence of C_{gd} path between the input and output port. When the frequency increases, the impedance of the parasitic capacitance C_{gd} decreases and results in higher reverse voltage gain, *S12*. The reverse voltage gain reaches as high as -37 dB at 10 GHz. However, by expressing the reverse voltage gain in power percentage, it can be shown that the reverse voltage gain is negligible if compare to the total output power. Such a small amount of power leakage deemed to be harmless to the circuit design.

4.1.5 Noise Figure

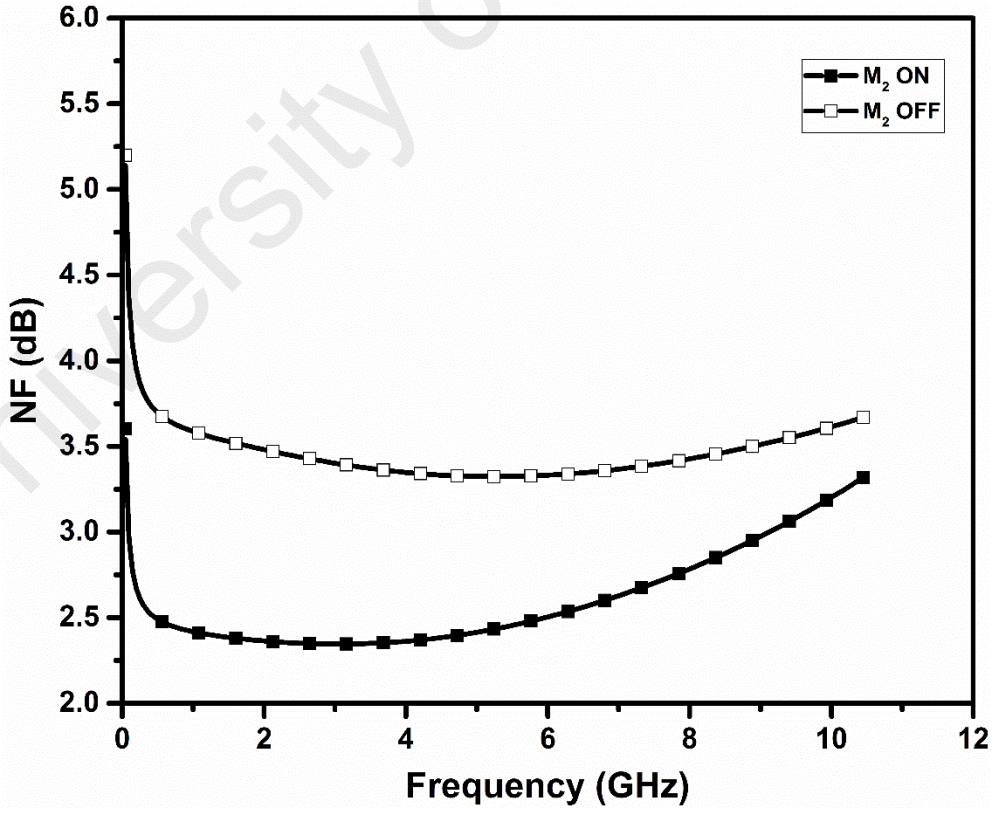


Figure 4-7: Simulated noise figure of the proposed LNA.

Figure 4-7 shows the simulated noise figure response of the proposed LNA with and without M_2 turned ON. The noise figure response shows huge improvement when M_2 is

ON. This agrees with the explanation in Chapter 3 that the noise voltage of M_1 can be cancelled off by using the topology shown in Figure 3-3. By implementing M_2 as inverting amplifier to inverse the phase of the noise voltage of M_1, the noise figure of the proposed LNA reaches as low as 2.35 dB at around 2.5 GHz and is maintained below 3.2 dB in the entire band of operation. On the other hand, when M_2 is OFF, the minimum noise figure increases to 3.33 dB and reaches as high as 5 dB. Flicker noise of the proposed LNA starts to dominate the total noise figure at frequency below 100 MHz. Although channel noise and thermal noise can be reduced by increasing the gain of the circuit, the flicker noise is not affected by the increment of gain as shown in (2-4). However, by incorporating noise-cancelling technique into the design, the flicker noise can be effectively reduced or cancelled.

4.1.6 IIP3 and P1dB

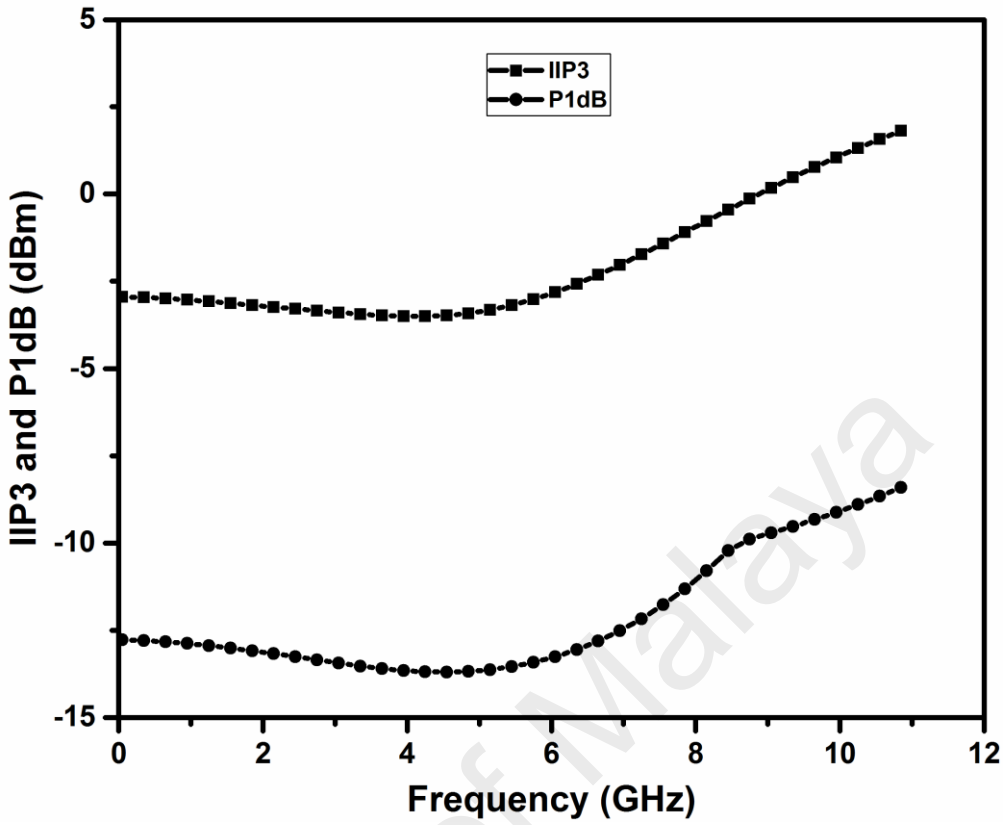


Figure 4-8: Simulated input third-order-intercept point, IIP3 and 1 dB compression point, P1dB of the proposed LNA.

Figure 4-8 shows the IIP3 and P1dB response of the proposed LNA. P1dB is the measurement of the 1 dB compression of signal and the proposed LNA achieve -13.7 to -8.4 dBm of P1dB response. Such P1dB response is capable in amplifying most of the standard wireless signals without experiencing much signal compression. For example, wireless network for 802.11 variants has a minimum received signal and maximum received signal of -100 dBm and -10 dBm respectively and operates at around -50 dBm range and hence all the input range of the wireless signal can be amplified without much compression. On the other hand, the proposed LNA achieves IIP3 ranging from -3.5 to 1.8 dBm which is around 9.6 dB higher than P1dB. However, before the LNA experience IM_3 intermodulation effect, the output signal has already exceeded the compression point.

P1dB response is simulated by gradually increase the input power and IIP3 response is simulated by using two-tone-test with frequency separation of 1 MHz.

4.1.7 Stability Factor

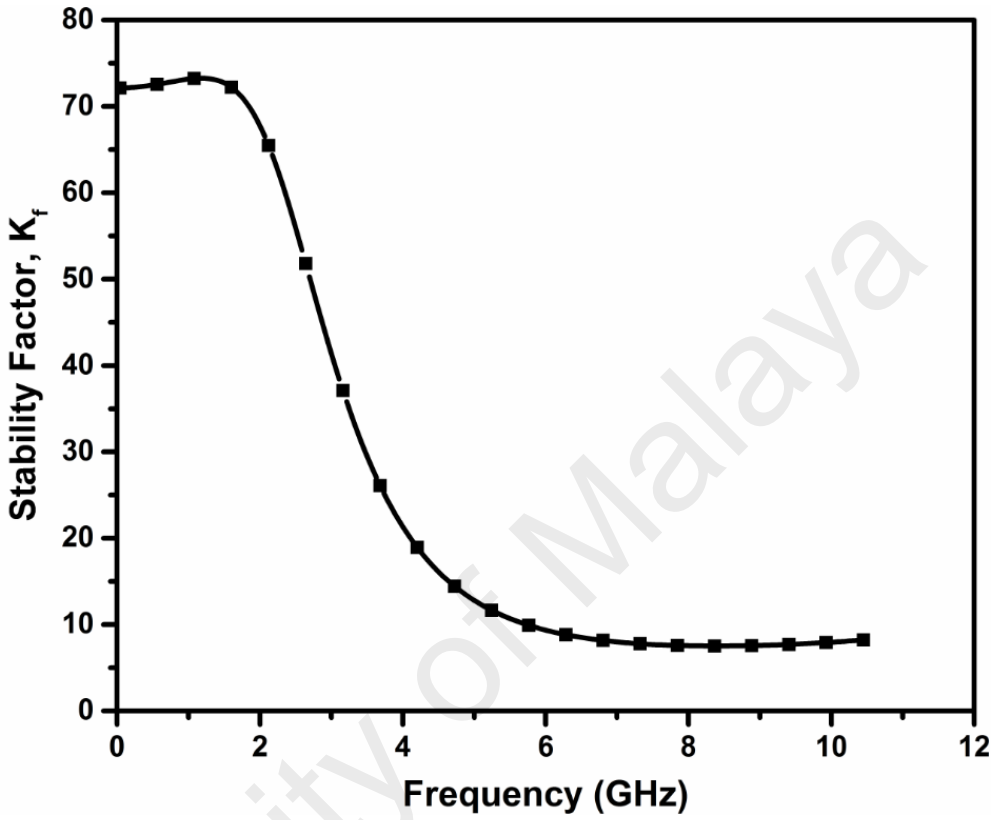


Figure 4-9: Simulated stability factor of the proposed LNA.

Figure 4-9 shows the simulated stability factor of the proposed LNA generated by CAD tool. The LNA achieves a stability factor, $K_f > 1$ and is unconditionally stable for the entire band of operation. However, the software generated stability factor includes other algorithm which is not included in hand calculation by using (2-23). Moreover, in measurement results, only S-parameters can be measured directly using VNA. Therefore, in the discussion of stability factor in measurement results, only hand calculation results based on S-parameters and (2-23) will be presented.

4.1.8 Summary of Post-Layout Simulation Results

In previous sections, pre-layout simulation results are presented mainly to demonstrate the difference without incorporating π-matching, M_2, and peaking inductors. After the

schematic is finalized, layout of the proposed LNA is drawn and simulations for post-layout are carried out.

In this section, the summary of the post-layout simulation will be presented.

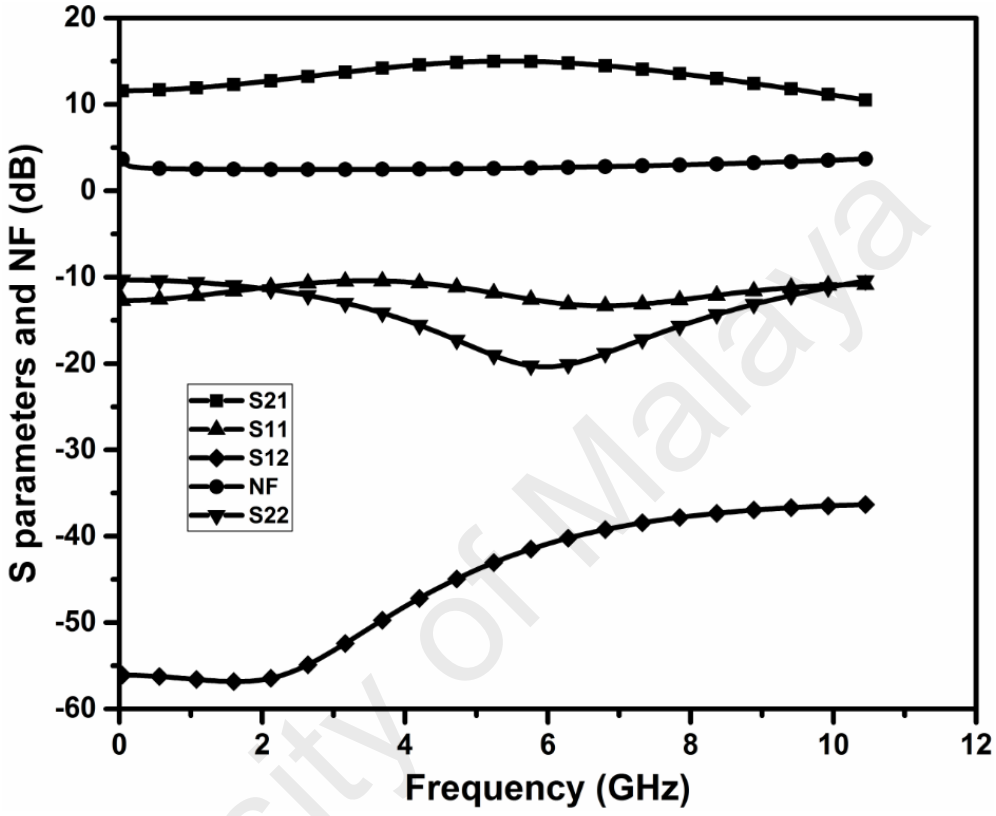


Figure 4-10: RC-extracted simulation of S-parameters and NF.

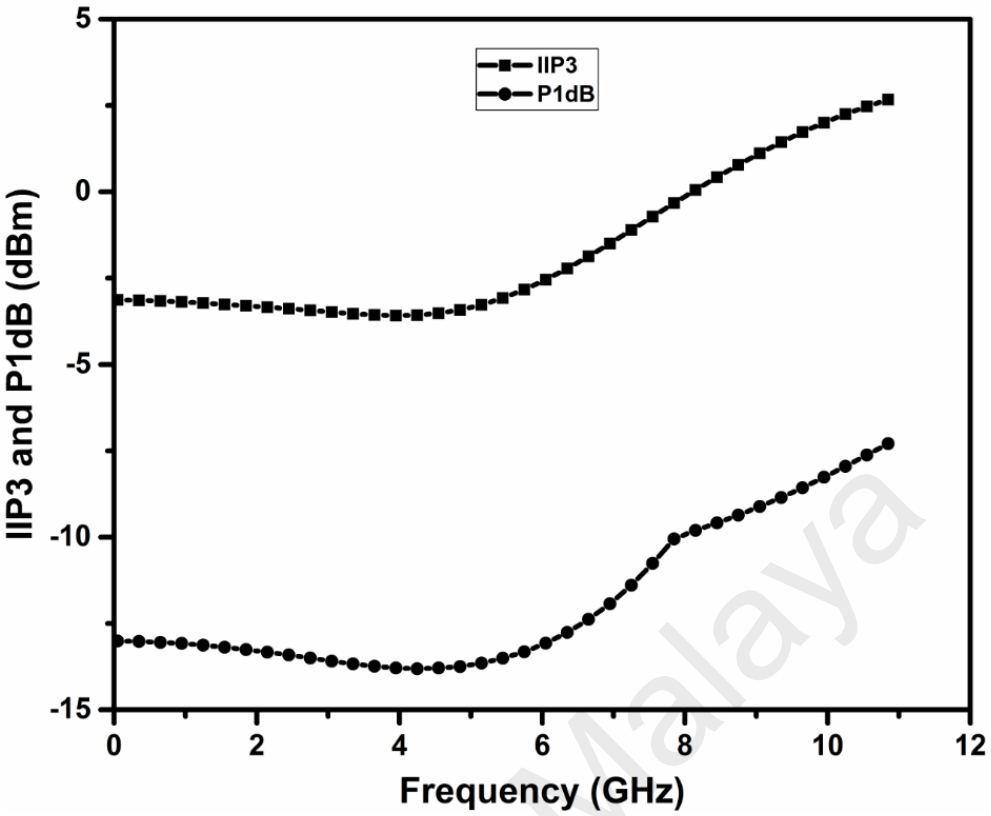


Figure 4-11: RC-extracted simulation of 1 dB compression point, P1dB and input third-order-intercept point IIP3.

Figure 4-10 and 4-11 show the RC-extracted post-layout simulation results of S-parameter, noise figure, P1dB and IIP3. The post-layout performance of the proposed LNA is tabulated in Table 4-1.

Table 4-1: Post-layout simulation results of the proposed LNA.

Performance Parameter	Results
S21 (dB)	13 ± 2
S12 (dB)	< -36
S11 (dB)	< -10.4
S22 (dB)	< -10.3
NF (dB)	3.01 ± 0.54
Power (mW)	35.4
Voltage (V)	1.2
Bandwidth (GHz)	0.05 - 10
IIP3 (dBm)	-0.75 ± 2.75
Size (mm^2)	0.77

There are slight differences between pre-layout simulation and post-layout simulation due to the added parasitic capacitance and resistance from the layout interconnection. However, the differences are in an acceptable range with minimal discrepancy.

4.2 Measurement Result

Figure 4-12 shows all the measurement equipment used in characterizing the device under test (DUT). First of all, the connection of the DC probe to the parameter analyzer (PA) should be established. The PA is remotely controlled by the computer and since there are only two DC supply in the proposed LNA, hence only two cables are needed to establish the connection. PA is used to supply V_{DD} to the chip or device under test (DUT) and to monitor the total current flowing through the circuit. From the observation, the total power consumption of the chip can be determined by basic mathematical computation.

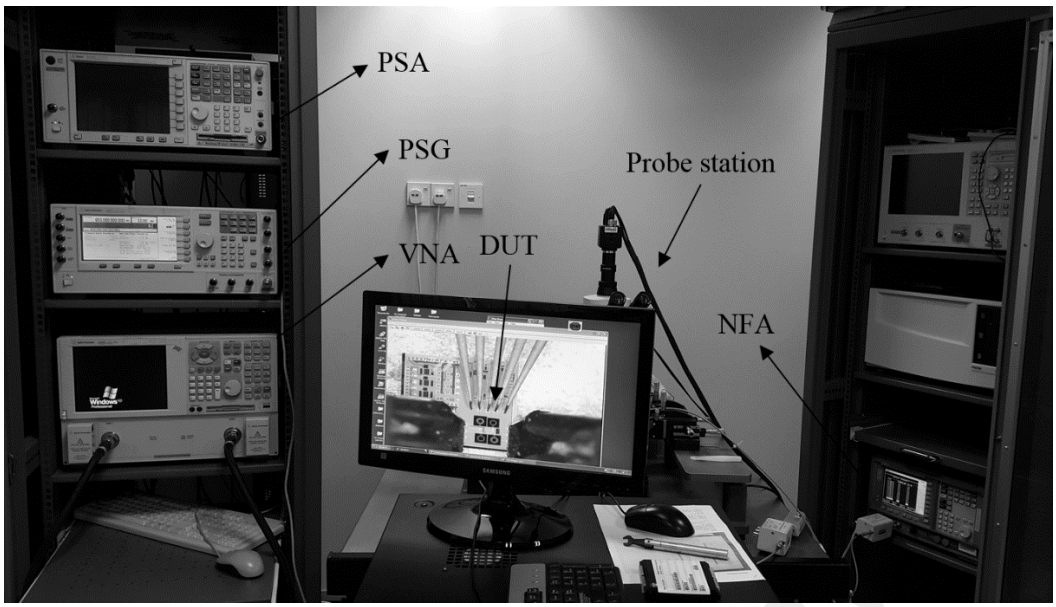


Figure 4-12: Test setup in wafer probing of the DUT.

After the setup of PA is finalized, input port of the VNA is connected to the probe and output port of the Vector Network Analyzer (VNA) is connected to the IF probe and remotely controlled by the terminal. VNA is capable of obtaining the S-parameters and P1dB of the DUT by stepping up the input power gradually. The DUT is placed on the probe station as shown in Figure 4-13.

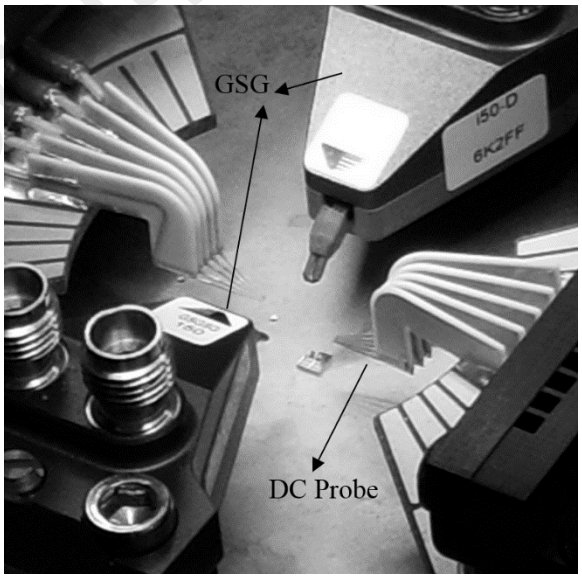


Figure 4-13: Alignment of the probe tips respective to the DUT.

4.2.1 Power Consumption

After the probe tips are placed, PA is turned ON by feeding a voltage of 1.2 V to the DUT. The total current flowing through the DUT is observed and the sample which has the closest DC characteristic is compared to the post-layout simulation is selected for further reliable characterization. The closest sample to the post-layout DC characteristic draws 26 mA of DC current and consumed total power of 31.2 mW. Meanwhile, in post-layout simulation, 29.5 mA of DC current and total power of 35.4 mW is consumed by the chip. It is believed that the DC characteristic differences between the DUT and post-layout simulation is caused by process variation and in turn affects the self-bias gate voltage. It is to be expected that the gain and noise performance would degrade due to the lower gate voltage.

4.2.2 S-parameters

The VNA is used to sweep the S-parameters from 40 MHz to 10.5 GHz by using 201 number of step size to synchronize with the available number of step size in noise figure analyzer (NFA). The measured S-parameters results are shown in Figure 4-14 and 4-15.

4.2.2.1 Measured and simulated S11 and S22

Upon obtaining the measured S-parameters, the results are then compared with RC-extracted simulated S-parameters. Figure 4-14 shows the comparison between simulated and measured S11 and S22 results of the proposed LNA. The simulated and measured results shows a similarity in the curves and agrees well with each other. The measured S11 and S22 seems to be not affected by the difference in DC biasing. This would not be the case for common gate amplifier with $1/g_m$ input matching because it depends heavily on DC bias to determine its transconductance. Measured S11 shows two minimum peak that are in near zero frequency and around 7 GHz. The consistency of the data between measured and simulated S11 shows that resistive feedback technique is unaffected by

process variation and shift of DC bias. On the other hand, measured S22 shows a shifted minimum peak compared to the simulated S22 probably due to the parasitic capacitance or process variation that causes the change in the inductor value and in turn shifted the minimum peaking frequency. Nevertheless, the measured S11 and S22 both achieves less than -10 dB of matching response in the entire band of operation.

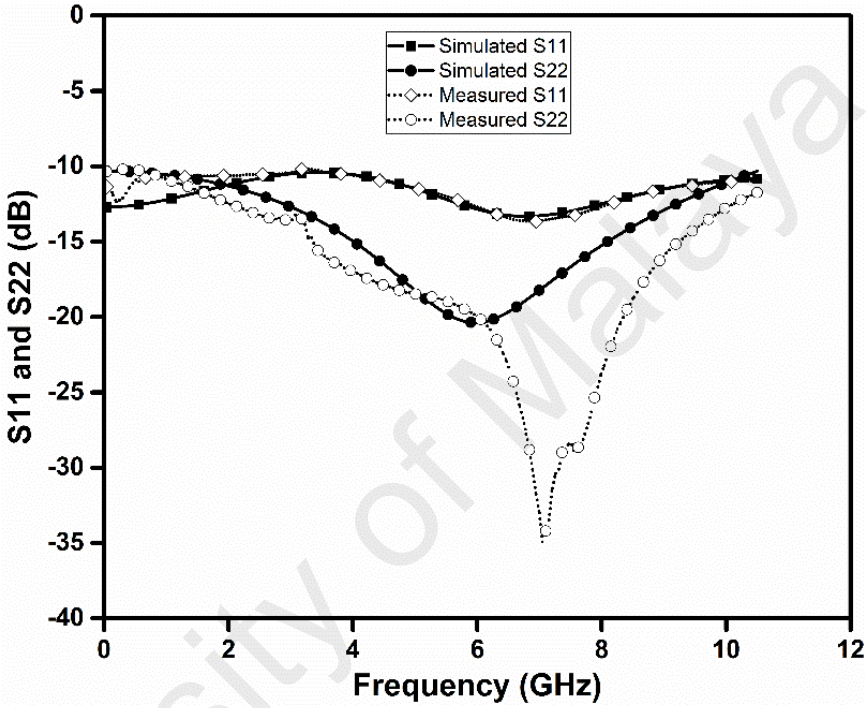


Figure 4-14: Measured and simulated input and output matching response, S11 and S22 of the proposed LNA.

4.2.2.2 Measured and simulated S21 and S12

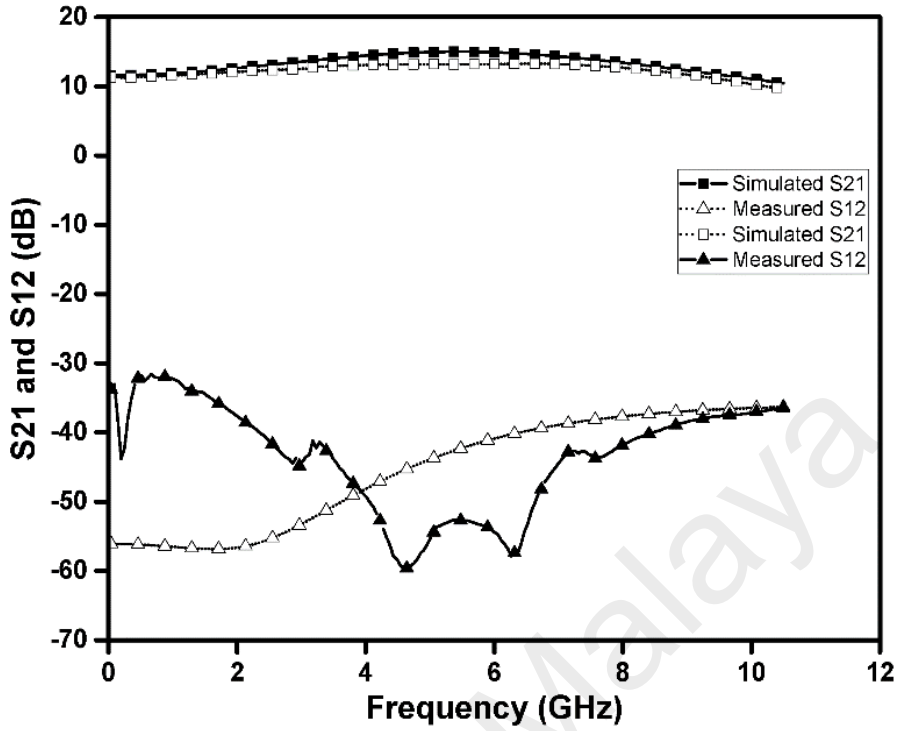


Figure 4-15: Measured and simulated forward voltage gain and reverse voltage gain response, S21 and S12 of the proposed LNA.

Figure 4-15 shows the measured and simulated S21 and S12 of the proposed LNA. The measured S21 shows similar curve as the simulated S21 but with lower gain due to the lowered DC bias. However, the measured S21 manage to maintain above 10 dB of gain with a range from 10.32 to 13.28 dB in the entire band of operation. The proposed peaking inductor technique proves to be effective in extending the bandwidth as well as boosting the gain at high frequency. The measured S12 shows unexpected result as the reverse voltage gain increases to around -31 dB at low frequency. The result is unexpected because at low frequency, impedance of parasitic capacitance is very large that it would block the signal and reduce the reverse voltage gain significantly. Moreover, the cascade stage would further reduces the feedback of output to the input. It is believed that process variation has contributed the shift of S12 performance. However, measured S12 performance is still acceptable because -31 dB of reverse voltage gain is negligible.

4.2.3 Noise Figure

In the characterization of the NF, the noise source is connected directly from input to output of NFA to calibrate out the noise source. However, the noise generated by the DC blocks, cables, and probe tips is not able to be calibrated. In order to cancel out the noise generated by those components and to obtain the actual DUT noise figure, the noise and gain of each components are measured using NFA. Then by using Friis's equation in (2-1), it can be rewritten as,

$$\frac{(F_{TOTAL} - F_1)(G_1 G_2) + 1 - F_3}{G_2} + 1 = F_2 \qquad (4\text{-}1)$$

where F_{TOTAL} is the total noise figure measured by NFA without calibrating DC-blocks and cables, F_1 is the measured noise of DC-block and cable at the input, F_2 is the DUT noise, F_3 is the measured noise of DC-block and cable at the output, G_1 is the measured gain of DC-block and cable at the input, and G_2 is the measured gain of DUT. G_2 can be replaced by VNA measured S21 if the circuit is well matched. Finally, the measured noise and gain of all the components are substituted into (4-1) to compute the actual noise figure of DUT.

Figure 4-16 shows the measured and simulated noise figure of the proposed LNA where the measured noise figure is approximated with a fitting curve. The measured noise figure of the proposed LNA has a range of 3.29 dB to 6 dB in the entire band of operation. The difference in measured and simulated noise figure are caused by the shifted DC-bias point which results in lower gain and higher noise and the unavailability of amplifier to suppress the NFA noise in high frequency. Although the DC-blocks and cables are able to be measured and calibrated using (4-1), but the probe tips is not calibrated out, resulting in an additive noise contribution.

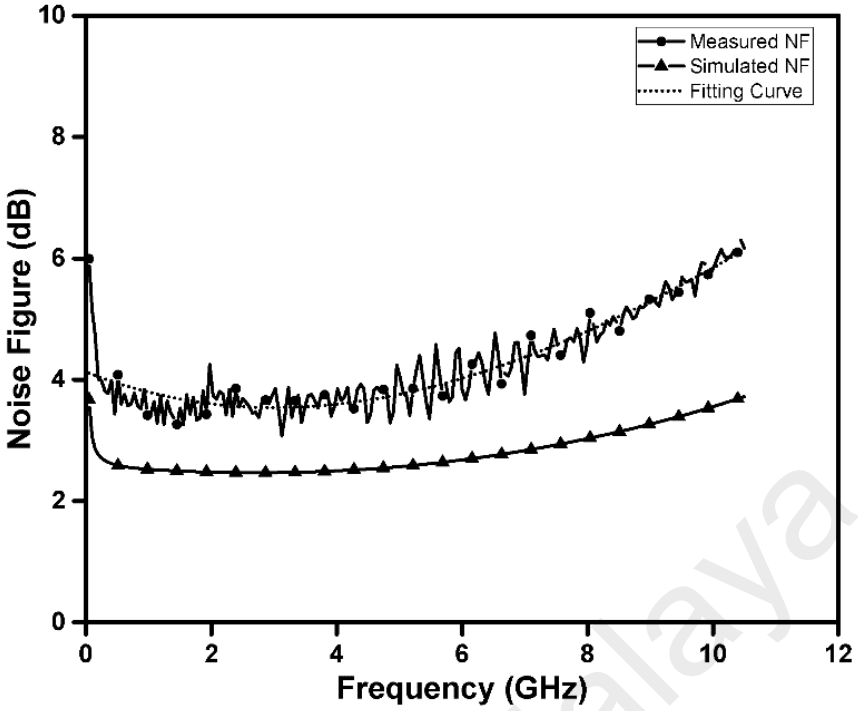


Figure 4-16: Measured and simulated noise figure of the proposed LNA.

4.2.4 P1dB and IIP3

As highlighted, VNA is capable of linearly stepping the input power to compute the P1dB. The input power of the VNA is increased gradually from -27 dBm to 5 dBm with center frequency of 5 GHz. The proposed LNA maintained its gain but gradually reduced as the signal power approach P1dB point. The P1dB point is then determined by observing 1 dB drop of gain and the measurement is repeated in another frequency.

For IIP3 measurement, the DC block and cable loss of the input and output port is measured using power signal generator (PSG) and power signal analyzer (PSA). The loss of DC block and cable is obtained and the data is adapted in computing the IIP3. At the PSG, two tone setting is enabled with 1 MHz frequency separation and the output is examined using PSA.

As observed in the Figure 4-17, two equal amplitude signals or two tone signals can be observed in the PSA. Finally, the input port of the DUT is connected to PSG and output port of the DUT is connected to PSA to observe the nonlinearity effect. Fundamental two tone signals can be observed in Figure 4-17 which are at 5 GHz and 5.001 GHz

frequencies and accompanied by third-order intermodulation signals as well as firth order intermodulation signals. The two tone signals amplitude is increased gradually from -25 dBm till 5 dBm and the output is recorded with only third-order intermodulation signals component taken into account. The actual signal power that is received by the DUT is determined by incorporating the PSG signal power and deducting the input port DC block and cable loss while the actual signal power that is delivered by the DUT is determined by accounting the PSA measured signal power and added with the output port DC block and cable loss.

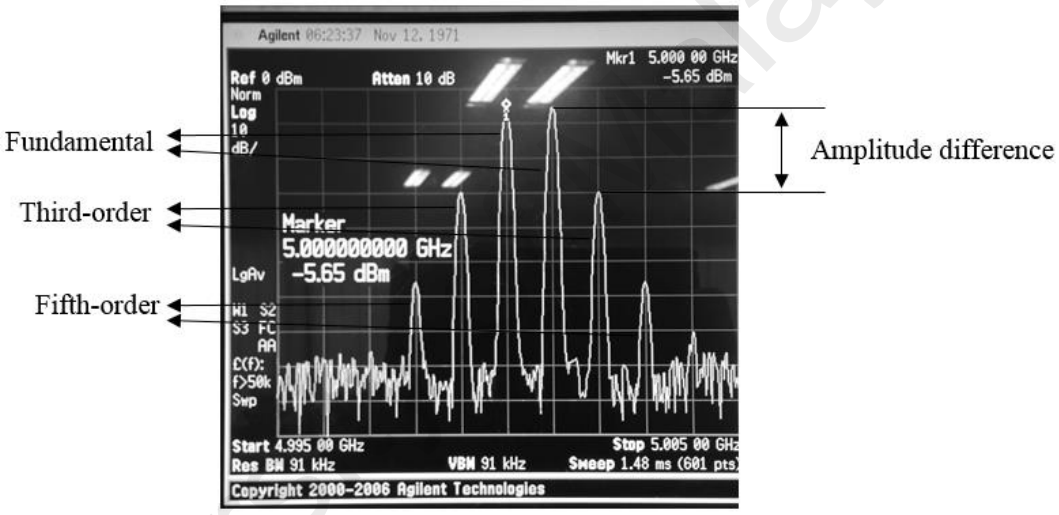


Figure 4-17: Screenshot of IIP3 test.

An example of the IIP3 plot at 50 MHz is shown in Figure 4-18. As can be observed in Figure 4-18, both fundamental and third-order intermodulation signals undergo compression before it reaches the IIP3 point. This is to be expected since the P1dB point is around 10 dB smaller than IIP3 point. By assuming the output signal is linear without affected by compression, the fundamental and third-order intermodulation signals can be extrapolated to locate the IIP3 point as shown in Figure 4-18. The characterization is repeated for other frequencies and the results are plotted as shown in Figure 4-19. It can be observed that in Figure 4-19, the performance of the measured IIP3 and P1dB is generally better than the simulated IIP3 and P1dB respectively. This is due to the overall

gain reduction of the fabricated DUT. The measured IIP3 ranges from -3.2 to +6 dBm in the entire band of operation.

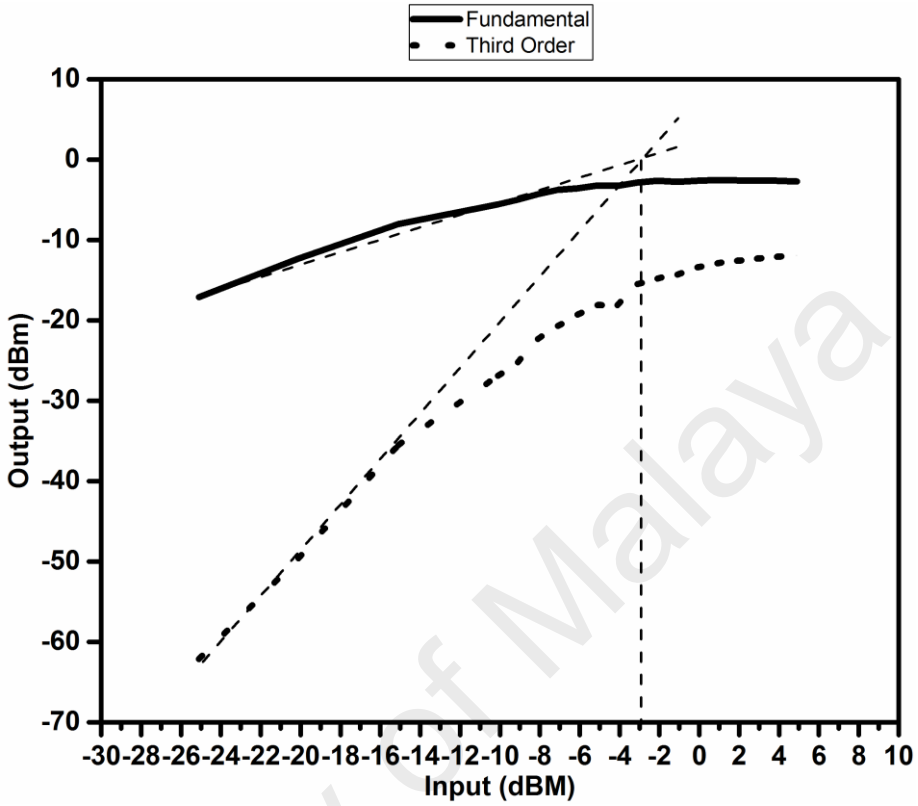


Figure 4-18: Input third-order-intercept point, IIP3 plot after manual calibration.

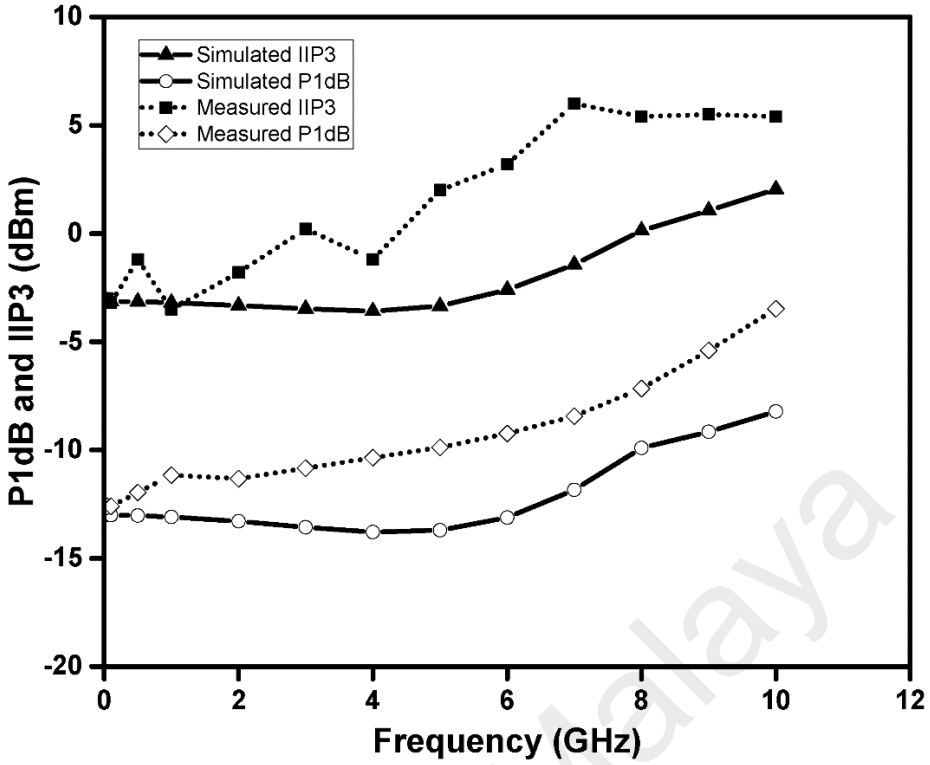


Figure 4-19: Measured and simulated input third-order-intercept point, IIP3 and 1 dB compression point, P1dB of the proposed LNA.

4.2.5 Stability Factor

In the CAD tool simulation, stability factor of the circuit is determined not only by considering S-parameters but also other parameters as well. In measurement, the stability factor cannot be obtained directly from the equipment and only the S-parameters data is obtainable. Therefore, the stability factor of the LNA is determined manually by using a simpler model which is highlighted in (2-23). The stability factor of the proposed LNA is shown in Figure 4-20.

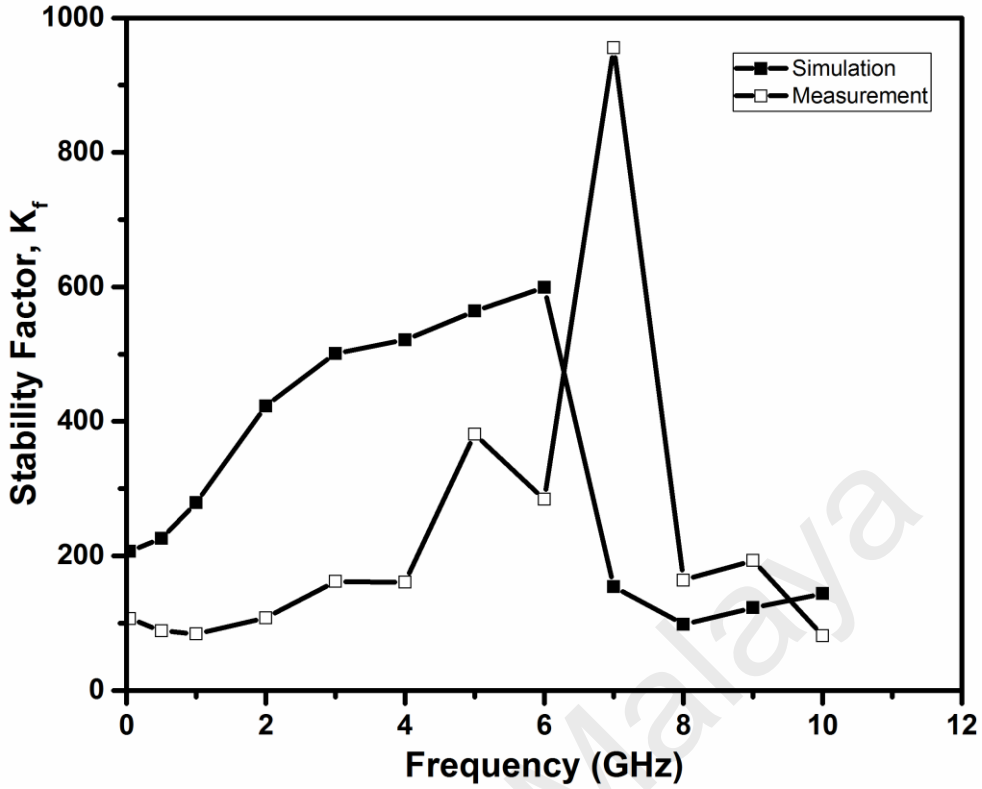


Figure 4-20: Simulated and measured stability factor of the proposed LNA.

In Figure 4-20, it can be observed that the simplified stability factor for both simulated and measured results is larger than one and the proposed LNA is deemed to be stable.

4.2.6 Chip Microscopic View

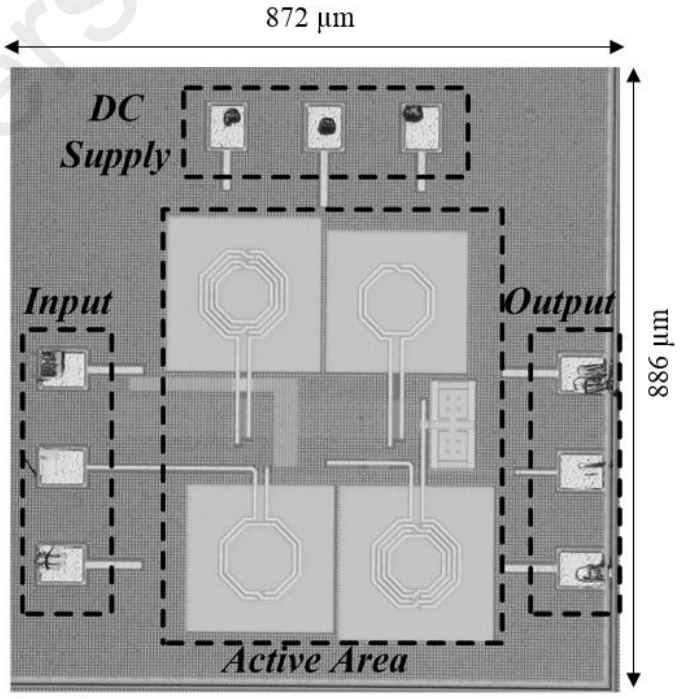


Figure 4-21: Screenshot of the proposed LNA chip microscopic view.

Figure 4-21 shows the microscopic view of the proposed LNA fabricated in a standard 0.13 µm CMOS process. The proposed LNA occupies total area of 0.77 mm^2 including bondpads and 0.33 mm^2 of active area.

4.3 Results Comparison and Discussion

The simulated and measured results are summarized in Table 4-2.

Table 4-2: Simulated and measured performance summary of the proposed LNA.

Specifications	Simulated	Measured
S11 (dB)	<-10	<-10
S22 (dB)	<-10	<-10
S21 (dB)	11 ~ 15	10.32 ~ 13.28
S12 (dB)	<-36	<-33
NF (dB)	2.47 ~ 3.55	3.29 ~ 6
P1dB (dBm)	-13 ~ -8.2	-12.6 ~ -3.48
IIP3 (dBm)	-3.5 ~ +2	-3.2 ~ +6
K_f (unitless)	>1	>1
Power (mW)	35.4	31.2
BW (GHz)	0.05 ~ 10	0.05 ~ 10

From Table 4-2, it is described that the measured input and output matching response of the LNA has similar performance compare to simulated result. This confirms with the statement in Chapter 3.1 where resistive feedback and resistive termination techniques are less affected by PVT variation. This would be a different case if common gate $1/g_m$ matching and buffer circuit is implemented as both the circuit implementation depend heavily on g_m. There is a maximum of 12.5% difference in S21 response mainly due to the shifted DC bias point. The penalty of lowered gain would results in higher noise figure but with lower power consumption as seen in Table 4-2. A decrease of 4.2 mW of power

consumption is observed due to the PVT variation. The increase in measured noise figure is also due to the inaccuracy and insensitivity of the NFA. NFA unable to cancel out the noise from noise source in frequencies higher than 3 GHz due to the lack of amplifier and result in nonzero noise after calibration. The inability of the NFA to directly measure the DUT noise figure also requires de-embedded method to obtain the real DUT noise figure. Although the noise of DC blocks and cables can be deducted but the noise of the probe tips is unable to measure and therefore is included into the noise of DUT being measured. Since linearity is inversely proportional to gain and lower gain would indirectly improve the P1dB and IIP3, an excellent IIP3 response of as high as +6 dBm is observed in the measured result. Nevertheless, the proposed LNA is deemed to be stable with the stability factor greater than unity in the entire band of operation.

To compare the proposed LNA with other recently reported works, figure of merit (FOM) system is adapted as a standard to determine the performance of the proposed LNA and other reported works (Chiou & Chou, 2013). The LNA performance such as gain, noise figure, linearity, bandwidth of operation and power consumption are taken into consideration. The modified FOM can be expressed as,

$$FOM = 10\log\left[\frac{10^{(S21_{\max}/20)} \cdot 10^{(IIP3_{\max}/10)}}{10^{NF_{\min}/10} \cdot P_d} \cdot \frac{f_H - f_L}{\sqrt{f_H \cdot f_L}}\right] \quad (4\text{-}2)$$

where $S21_{max}$ is the maximum gain, $IIP3_{max}$ is the maximum input third-order-intercept point, NF_{min} is the minimum noise figure, P_d is the power consumption in Watts and f_H and f_L are maximum operating frequency and minimum operating frequency in GHz respectively. The proposed LNA has the highest *FOM* compare to other reported works because of its superior IIP3 performance and relatively wide bandwidth. The performance of the proposed LNA compare to other reported works is summarized in Table 4-3.

Reported LNA (1) has similar performance as the proposed LNA with lower power consumption and noise figure but with a narrower bandwidth. Bagga, (2), (3) have lower FOM than 20 due to narrower bandwidth and worse IIP3 performance due to high gain. Finally, Razavi is compared with the proposed LNA due to the LNA is targeted for cognitive radio applications.

Table 4-3: Performance comparison with other reported works.

Performance Parameters	This Work	(Chung, Lee, Jeong, Yoon, & Kim, 2015)	(Bagga et al., 2014)	(Li, Feng, & Li, 2017)	(Taibi, Trabelsi, Slimane, Saadi, & Belaroussi, 2017)	(Razavi, 2010)
Voltage (V)	1.2	1.2	0.8	1.2	1.8	-
Power (mW)	31.2	20.8	9.6	8.5	16.5	22
BW (GHz)	0.05-10	0.1-1.6	3.5-9.25	3-12.3	3.2-10.64	0.05-10
S11 (dB)	<-10	<-8	<-8	<-11	<-7.5	-
S22 (dB)	<-10	<-12	-	-	<-15	-
$S21_{max}$ (dB)	13.28	13	18	15	17	20
S12 (dB)	<-33	-	<-20	-	-	-
$IIP3_{max}$ (dBm)	+6	+5.5	-12	-7	-9	-7
NF_{min} (dB)	3.29	2.1	1.6	4	2.5	2.9
Area (mm^2)	0.77	-	0.56	0.86	-	-
Process (µm)	0.13	0.065	0.09	0.13	0.18	0.065
FOM	35.9	32.5	15.6	19	15.9	28.2

This work appreciates the significance of input and output matching and achieves at least < -10 dB input and output response in the entire band of operation. In typical case, LNA is followed by mixer which eliminate the need of output matching circuit. However, since the proposed LNA is measured as a standalone solution, thus output matching

circuit is mandatory for measurement purposes. Adapting resistors into the architecture are inevitable to obtain a flat response on S-parameters from tens of megahertz to 10 GHz. To compensate for the additional noise and voltage headroom consumption from resistors, higher voltage supply and power consumption are required. This justifies the reason most of the ultra-wideband LNAs with respectable noise and gain response have high power consumption.

CHAPTER 5: CONCLUSIONS AND FUTURE WORKS

5.1 Summary and Conclusions

In this dissertation, the design of ultra-wideband LNA for cognitive radio application is presented. The proposed LNA was designed and fabricated in 0.13 µm standard CMOS technology. The measurement results are generally in agreement with the post-layout simulation results.

The proposed LNA adapted resistive feedback topology and together with π-matching network to achieve ultra-wideband input matching. For the output matching, 50 ohms resistive termination technique is adapted into the design to achieve maximum power transfer and gain enhancement. RF signal is cascaded over two stages of amplification to achieve adequate gain. Peaking inductors are incorporated into the design to extend the bandwidth of the LNA with reasonable trade-off in chip size. The proposed LNA adapts self-bias technique to provide gate voltage for the circuit and avoided the use of biasing circuit and on-chip capacitor.

In conclusion, a resistive feedback self-biased ultra-wideband LNA was designed and fabricated with the aid of standard 0.13 µm CMOS technology. It is observed that the gain of the LNA is 11.8 ± 1.48 dB and the reverse isolation is better than -33 dB in the entire band of operation. This work observes better than -10 dB of input and output matching with a noise figure of 3.29 to 6 dB. The maximum P1dB and IIP3 are -3.48 dBm and +6 dBm respectively. The total power consumption of the device is 31.2 mW with 1.2 V of supply headroom. The device occupies 0.77 mm^2 of physical area which includes the bondpads and 0.33 mm^2 with only active area.

5.2 Future Works

The proposed LNA can be adjusted carefully using ac-analysis to make sure the output signal phase of M_1 and M_2 are equal in order to acquire higher gain. If the output signals phase is equal and channel noise signal of M_1 is exactly out of phase at the output of M_1 and M_2, the noise performance of the LNA will be further improved.

On the other hand, M_2 can be removed to reduce the power consumption but with the cost of higher noise figure. In order to further improve the gain of the LNA, the circuit can be cascaded with another gain stage but with the drawback of lower linearity.

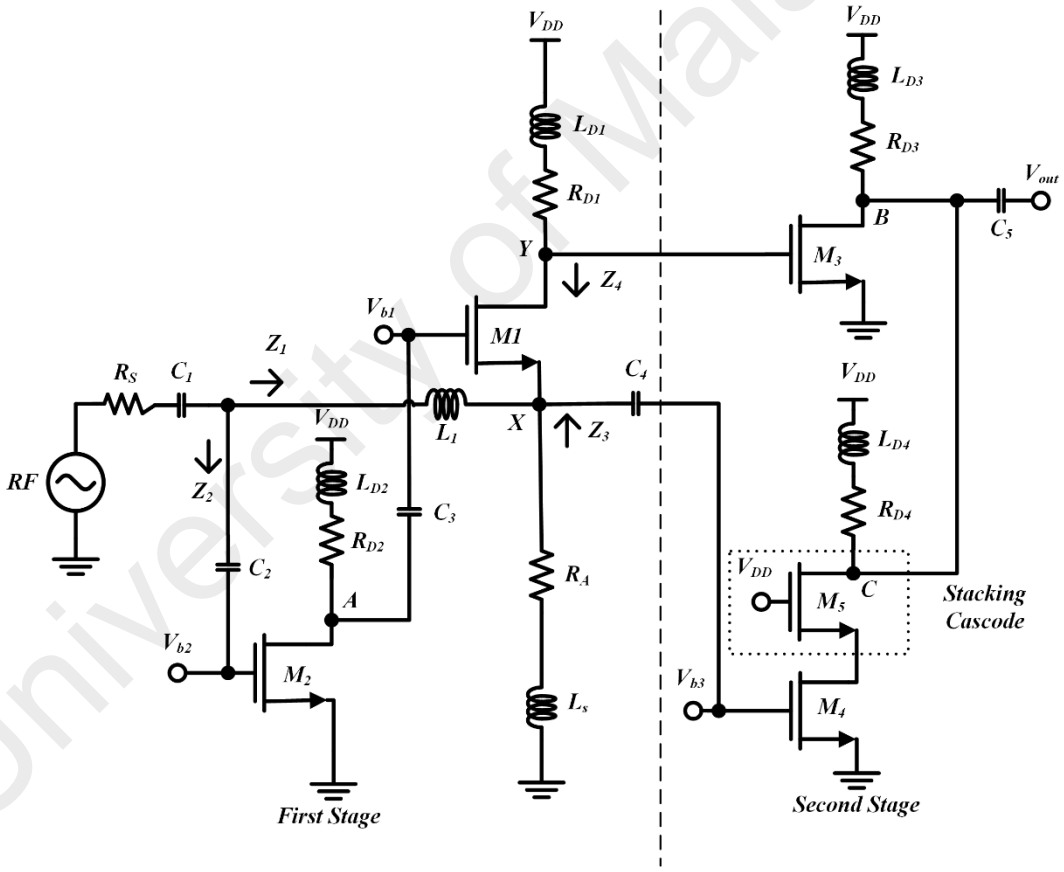
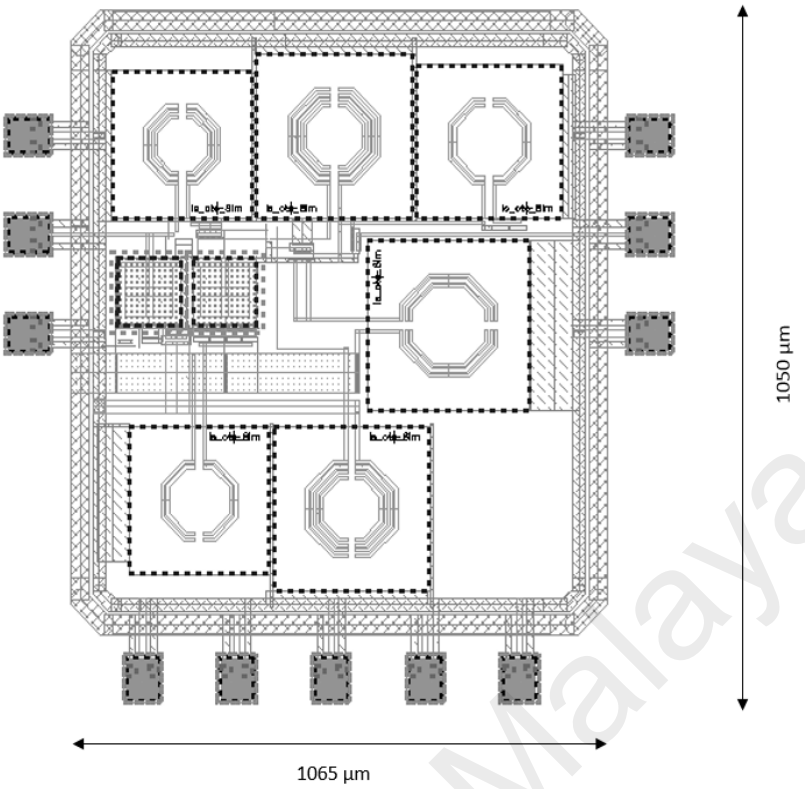


Figure 5-1: Improvised LNA design 1 with g_m-boosting and noise cancelling techniques for cognitive radio application



Specification	Example 1 LNA
S11 (dB)	<-10
S22 (dB)	<-7.2
S12 (dB)	<-38
$S21_{max}$ (dB)	13.0
NF_{min} (dB)	3
$IIP3_{max}$ (dBm)	-5.3
Power (mW)	24.2
BW (GHz)	0.05 – 10
Area (mm^2)	1.12
Voltage (V)	1
Process (µm)	0.13

Figure 5-2: Layout view and post-layout simulation results of improvised LNA design 1.

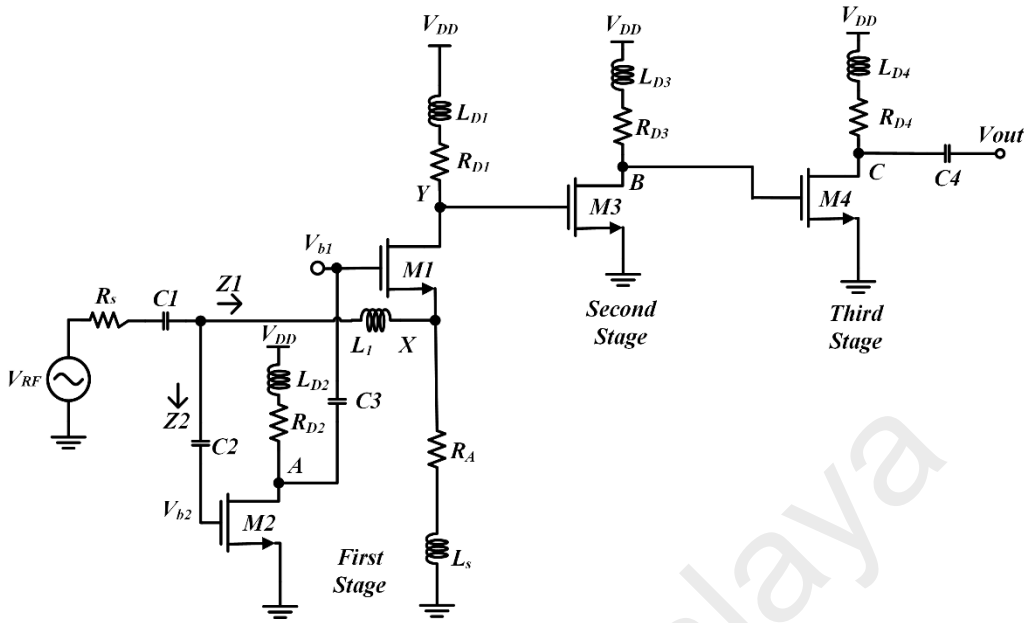
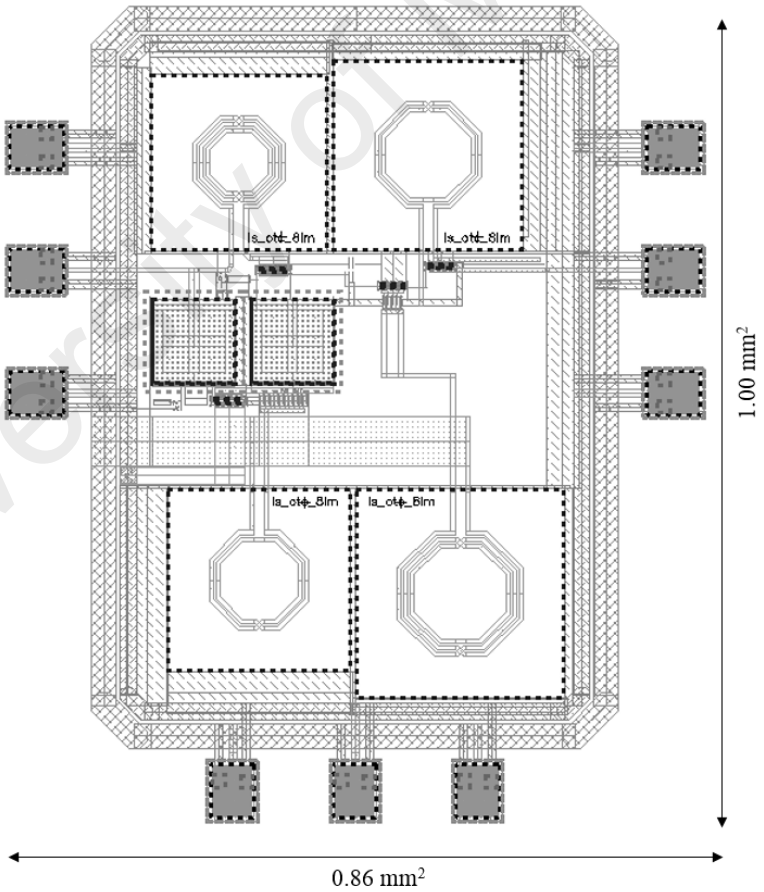


Figure 5-3: Improvised LNA design 2 with g_m-boosting technique with three stage cascade amplification for cognitive radio application.



Specification	Example 2 LNA
S11 (dB)	<-10.9
S22 (dB)	<-13.4
S12 (dB0	<-47
$S21_{max}$ (dB)	19.2
NF_{min} (dB)	3.7
$IIP3_{max}$ (dBm)	- 10.4
Power (mW)	21.4
BW (GHz)	0.05 – 10
Area (mm^2)	0.86
Voltage (V)	1
Process (µm)	0.13

Figure 5-4: Layout view and post-layout simulation results of improvised LNA design 2.

Figure 5-1 to 5-4 show two examples of possible LNA design for cognitive radio application. Both of the designs results are up to post-layout simulation. Figure 5.1 adapted noise-cancelling and g_m-boosting to improve the gain and noise performance and a stacking cascade stage to improve the reverse isolation. Figure 5.3 adapted g_m-boosting technique and is cascaded over three stages of amplification to achieve very high gain but has a higher noise performance due to lack of noise-cancelling stage. Both of the circuits adapted common gate $1/g_m$ matching and the performance of $1/g_m$ matching due to PVT variation only can be determined after fabrication.

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LIST OF PUBLICATIONS AND PAPERS PRESENTED

Conference paper:

Tey, Y. Y., & Ramiah, H. (2015). "A High Gain and Low Noise Common Source Amplifier for Cognitive Radio Application," *IEEE International RF and Microwave Conference (RFM 2015)*.

Journal paper:

Y. Y. Tey, H. Ramiah & N. M. Noh, "A 50 MHz ~ 10 GHz, 3.3 dB NF, +6 dBm IIP3 Resistive Feedback Common Source Amplifier for Cognitive Radio Application," *Microelectronics Journal*.

Y.Y. Tey, H. Ramiah & N. M. Noh, "Design of Low Noise, Flat Gain CMOS Based Ultra-wideband Low Noise Amplifier for Cognitive Radio Application," *IETE Journal of Research*.