PERFORMANCE EVALUATION OF A THREE-PHASE NINE LEVEL VOLTAGE SOURCE CONVERTER USING SELECTIVE HARMONIC ELIMINATION TECHNIQUE

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ABSTRACT

Multi-level converters are attracting research interest; this is because of their tremendous positive contribution they are making in the medium power industries. The converter has put hope in the minds of power electronic engineers that a time will come when it will break a record by providing an efficient means of utilizing the abundant renewable energy resources.

This research report aims at ultimately producing an optimized 3 phase nine level multilevel voltage source inverter for renewable energy sources which reduces the size of the converter by using a single dc source as an input to generate a nine level 3-phase output voltage waveform which is nearly sinusoids.

The circuit comprises of three sets of parallel connected cascaded configurations powered using a single source (photovoltaic, battery, wind etc.). The cascaded configuration composed of two parallel connected modules that are connected to a specially made transformer having to independent primaries and series connected secondary sides with 1:1 turns ratio.

Selective harmonic elimination method is used to eliminate the lower other odd harmonics. This is achieved by controlling the fundamental component at certain pre-determined point per quarter wave cycle. In this thesis, a 3-phase five level converter with (3/9) distribution ratio was designed and simulated. The converter was able to eliminate eleven lower order non-triplen harmonics. This shows how SHE can improve the performance of a converter without the need for additional components.

The results obtained yield a positive outcome, giving the converter an upper hand over it counterparts and the possibility of taking the lead in renewable energy applications.

ABSTRAK

Penukar pelbagai peringkat menarik minat penyelidikan; ini disebabkan oleh sumbangan positif yang besar yang mereka buat dalam industri tenaga sederhana. Penukar telah meletakkan harapan di dalam minda jurutera elektronik kuasa bahawa masa akan datang apabila ia akan memecahkan rekod dengan menyediakan cara yang efisien menggunakan sumber tenaga yang boleh diperbaharui yang banyak.

Laporan penyelidikan ini bertujuan untuk menghasilkan penghasilan sumber voltan bertingkat 3 tahap yang dioptimumkan untuk sumber tenaga boleh diperbaharui yang mengurangkan saiz penukar dengan menggunakan satu sumber dc tunggal sebagai input untuk menghasilkan sembilan aras voltan keluaran voltan keluaran 3 tahap hampir sinusoid. Litar terdiri daripada tiga set konfigurasi yang diselaraskan selari dengan menggunakan satu sumber (fotovoltaik, bateri, angin dll). Konfigurasi cascaded terdiri daripada dua modul yang berkaitan selari yang disambungkan kepada transformator yang dibuat khas untuk main independen dan siri bersambung yang bersambung dengan nisbah 1: 1 berubah. Kaedah penyingkiran harmonik terpilih digunakan untuk menghilangkan harmonik ganjil yang lebih rendah. Ini dicapai dengan mengawal komponen asas pada titik tertentu yang ditentukan sebelum kitaran gelombang suku tahunan. Dalam tesis ini, penukar lima tahap 3 fasa dengan nisbah taburan (3/9) telah direka dan disimulasikan. Penukar mampu menghapuskan sebelas perintah harmonik bukan triplen yang lebih rendah. Ini menunjukkan bagaimana SHE dapat meningkatkan prestasi penukar tanpa memerlukan komponen tambahan.

Hasilnya menghasilkan hasil yang positif, memberikan penukar satu tangan lebih tinggi ke atasnya dan kemungkinan mengambil petunjuk dalam aplikasi tenaga boleh diperbaharui..

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS AND ABBREVIATIONS

V	:	Volt
VSI	:	Voltage Source Inverter.
THD	:	Total Harmonic Distortion.
MLDCL	:	Multilevel DC Link
MIT	:	Multilevel Inverter Topology
FFT	:	Fast Fourier Transform
CHB	:	Cascaded H-bridge

LIST OF APPENDICES

CHAPTER 1: INTRODUCTION

1.1 Background on the research topic

Over dependency on fossil fuels as the major source of energy poses a serious threat to the continued existence of life in our dear planet "Earth". The number of greenhouse gases emitted to the atmosphere on daily bases as the result of energy generation and industrial utilization are quite alarming. Fossils exploration and processing results in the serious environmental pollution (both land and water), which entails affects the natural structures and habitat living in them. As the result of the aforementioned problem, scientist have focused their attention and resources towards finding an alternative and sustainable means of energy generation that has zero or minimum environmental de-gradational effects compared to the conventional fossil fuels (Lazarus, et al., 1993). To this effect, a lot of power electronic converters were designed and have already been placed at various distributed generation (DG) and grid-connected networks (Alepuz, et al., 2006).

The need for an alternative means of energy generation that is more suitable and friendly to our environment has been the cardinal point of this research. In addition to the greenhouse gas effect, the deflation rate of the existing fossils reserves is quite alarming. hence, there is the need to get a more reliable alternative source of energy. Based on this, there is the need to improve the existing means of energy transformation/conversion. This can be achieved by inventing a new and better converter topology, improving the efficiency and performance of the existing ones by reducing the inverter output THD

Multi-level converters over the last decade have become an interesting research area for many power electronic engineers and scientist. This could be mainly due to its high power handling capability making it suitable for both medium and high power industrial

applications across the world. To increase such power and voltage ratings, we increase the number of inverter levels by adding more switching device in each phase (Rashid, 2006). There have been a lot of modulation technique due to the need and importance of removal of harmonics in the output voltage. In addition to its high power handling capability, it also produces a better output voltage waveform closer to sinusoidal, with low output harmonic distortions and reduced switching stress dv/dt on the power electronic switching devices (Manjrekar,2002). These features have remarkably put it on top of it conventional counterpart (Bernet, 2005).

Multi-level converters can be categorized into three main topologies namely Flying Capacitors (FC), Neutral Point (NPC) /Diode Clamped and Cascaded H-bridge (CHB) (Lai & Peng, 1993). They are brought into existence in order to increase the system output power and at the same time provide solutions to the inability of the ordinary conventional inverters to withstand high switching frequency, high voltage and current stress which cumulatively lead to poor efficiency and induces electromagnetic- interference (EMI) in the system (Kang, Park, & Kim, 2004).

In their topology, a number of low voltage devices were arranged in such a way to share the voltage/current stress across them and this is successfully achieved by employing proper switching sequence of the switches. An important advantage of multi-level configuration is that without the need to increase the frequency of switching or output power, the harmonics in the output waveform is reduced. The name multi-level begins from three levels and increases thereby reducing the total harmonic distortion. Voltage problems, clamping requirements, expenses, and other constraints limits the number of achievable. Switching strategy plays a significant role in the performance of an inverter, because it has link with the harmonic content of the inverter output voltage. That is why power electronic scientist have suggested innovative techniques to minimize

harmonic distortions in the converter output. Numerous modulation methods like Sinusoidal Pulse Width Modulation Techniques (SPWM), Space Vector Modulation Technique (SVM) and Optimized Harmonic Stepped Waveform Technique (OHSW) are embraced. (Suresh, 2016) in his paper presented a review on selective harmonic elimination PWM strategy and the different optimization algorithm techniques

The SPWM and SVM techniques were designed to operate at a high switching frequency which results in a reduction of the output filter size and increased device switching stress/ heat loss. OHSW technique operates the power devices at a low frequency, exerting less switching stress on them, making them to dissipate less amount of heat. The reduced switching frequency results in increased output harmonic distortion, which warrants the need for large sized filter. To realize a smaller size filter using this techniques, the dominant low frequency harmonics needs to be shifted further to a high frequency through the use of step modulation and multiple level inverter, these results in increased inverter price and circuit complexity. To address this problem, a different approach was introduced, were by notches are superimposed on the output waveform at a predetermined angle, this pushed the low order dominant harmonics to a higher frequency, so that they can be easily eliminated using a small sized filter (Bernet, Krug, Fazel, & Jalili, 2005). This new approach is called Selective Harmonic Elimination Method or pre-calculated modulation technique. It was first proposed by Patel at et al. (Hoft, 1973). This is a non-carrier based technique because it only requires some pre-calculated angles that are stored in a lookup table (memory) (N. Chiasson, 2003). These angles are generated by finding Fourier series expansion of the voltage equation, which happens to be a non-linear trace-dental equation as shown below:

$$\boldsymbol{H_n = \left\{\frac{4E}{n\pi}\left\{(-i)^N\left(1 + 2\sum_{k=1}^{N}(-1)^K \cos(na_K)\right)\right\}\right.} \textbf{ for odd and even } \boldsymbol{n} \quad \ldots\ldots\ldots\ldots\ldots \textbf{1.1}$$

Based on the odd quarter wave symmetry theory, the DC components and even harmonics will cancel out will be left with the fundamental and odd harmonic components (Brendan Peter McGrath, 2002). The fundamental component is equated to a constant value which is determined by the selected modulation index, and the odd harmonics are equated to zero. The generated equations have no direct solution. Hence, numerical techniques which involve iterative procedures as in Newton Raphson method, a mathematical resultant method which uses the concept of polynomials, optimization techniques or Hybrid genetic algorithm (Ozpineci, Tolbert, & Chiasson, 2004) are used to approximate the switching angles. Selective harmonic elimination method has drastically reduced switching loss, filter size, price, and complexity of the entire circuit, which form the reason why it has been extended to high power multi-level converters (Manjrekar, 1993). The number of achievable voltage level is only limited by voltage unbalance problems, voltage clamping requirements, circuit layout, packaging constraint, and cost.

A recent inverter was introduced into the system which has 3^n steps, where n is the number of cascaded H-bridges. The said configuration/ topology operates by summing up or subtracting the transformer secondary output voltages. It also has the ability to produce more output voltage steps without the need for additional components. The drawback of this method is the system bulkiness, which is as the result of the low-frequency transformer.

To mitigate the said problem, a new technique was developed that generates $3^{(n-1)}$ +2 output voltage levels. The converter topology uses three (3) full-bridge units with each operated with a unique control strategy. Two of the unit modules were switched at low frequency which realizes a normal square output voltage steps at the fundamental frequency, whereas the last unit is operated at a much faster frequency, hence, producing

some notches that are superimposed on the fundamental, making it to look more like a sinusoidal waveform. (Bernet, 2006). This approach produces a better output with less harmonic distortions compared to the earlier mentioned converter topologies. Unlike the previous techniques, more voltage levels can be generated without incorporating additional components (Bernet, Krug, Fazel, & Jalili, 2005). The high frequency of operation results in a reduction in the transformer size, hence reducing the overall system size and cost. The disadvantage of this topology is it generates higher harmonics when operated on a light load

This project simulates a nine-level three phase multi-level voltage source converter that is suitable for renewable energy applications. In this work, a modified h-bridge converter topology and cascaded multi-winding transformer are used to generate a nine level 3-phase sinusoidal waveform with reduced device count when compared with the conventional nine level h-bridge topology. For the switching function, an optimized selective harmonic elimination technique is used to find the optimum switching angles. The proposed topology will be simulated using PSIM software. The performance of the proposed topology with regards total harmonic distortion (THD) and efficiency is compared against the conventional three-phase nine level topology.

1.2 Aim and objectives of study

1.2.1 Aim

The research work aims at ultimately producing an optimized 3 phase nine level multilevel voltage source inverter for renewable energy sources.

1.2.2 Objectives

The following are the sets of objectives:

1. Simulating a three-phase nine level output voltage source converter.

2. To employ selective harmonic elimination method to eliminate (n-1) non- triplen lower order harmonics.
3. To compare the proposed topology performance with that of a conventional nine level H-bridge converter

1.3 Conceptual Framework

As outlined in figure 1.1 multilevel converter is broadly classified into two major categories based on the nature of input source. Hence, this research will base its work on voltage source converters (VSI). Under VSI, we will specifically look at a three-phase Cascaded H-Bridge Multi-level converters with single equal DC source.

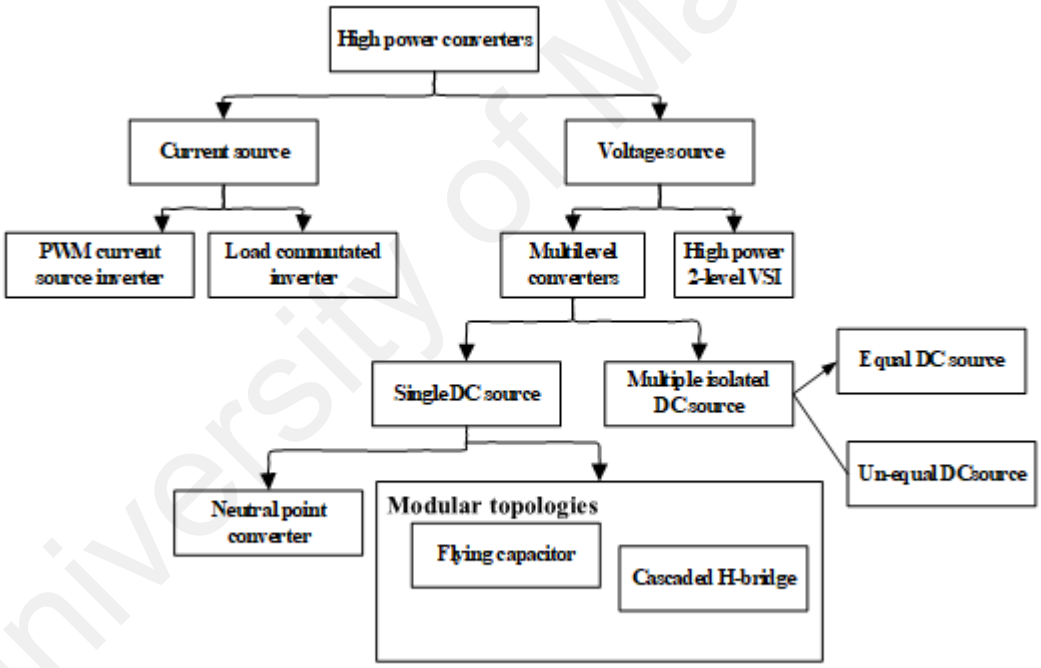

Figure 1.1: Multilevel converter classifications

Cascaded H-bridge multi-level converter uses the minimum number of power electronic components for a given output level (Jih-Sheng, 1996) compared to other converter topologies. This makes it dissipate less heat and hence the cooling system reduces which translates to a smaller size and lightweight. These properties gave the room

to incorporate a specially designed transformer at the converter output. In addition, the topology also has the following advantages as well (Lazarus, et al., 1993).

1. There is an automatic voltage sharing across the switches in a module due to the usage of the independent voltage source. Therefore, reduces restriction in the switching sequence.
2. The converter produces more output voltage levels, adding smaller voltage steps to the load and less harmonic distortion for a given switching frequency.
3. Its modular nature makes its production, maintenance and redundancy integration much easier.
4. Higher voltage level can be achieved by series-connecting more H-bridges.

Secondly, the research reduces the heat generated due to uneven switching stress distribution across the switches, as well as heat due to lower order harmonics. This will be done by using hybrid genetic algorithms to solve the non-linear transcendental equations (i.e. eqn. (1.1)...(1.4) derived using Selective Harmonic Elimination methods SHE-PWM. SHE-PWM is one of the promising converter modulation techniques that is used to generate non-linear transcendental, whose solutions provide an optimized switching angles.

$$\cos(\alpha_1) - \cos(\alpha_2) + \cos(\alpha_3) - \ldots\ldots + \cos(\alpha_{11}) - \cos(\alpha_{12}) = \frac{M\pi}{4} \quad \text{---1.1}$$

$$\cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) - \ldots\ldots + \cos(5\alpha_{11}) - \cos(5\alpha_{12}) = 0 \quad \text{---1.2}$$

:

:

$$\cos(37\alpha_1) - \cos(37\alpha_2) + \cos(37\alpha_3) - \ldots + \cos(37\alpha_{11}) - \cos(37\alpha_{12}) = 0 \quad \ldots 1.3$$

α_K Denotes the switching angles and most satisfies the relationship,

K= 1, 2…N

$$\alpha_1 < \alpha_2 < \ldots\ldots < \alpha_N < \frac{\pi}{2} \quad \text{----------1.4}$$

With an appropriate choice of switching angles and proper utilization of switching freedom, the inverter total harmonic distortion (THD) level at the output will reduce, hence eliminating the heat generated by harmonics. This, in general, reduces the overall system size and increases system efficiency.

CHAPTER 2: LITERATURE REVIEW

2.1 Introduction

This chapter reviews the past and present technological transformation that has taken place in the field of power converters and their modulation strategy

2.2 Multi-level Voltage Source Converters

As previously stated, quite a number of multi-level converter topologies have been mentioned in several kinds of literature. (Sadigh, 2015). In this paper, the three most mentioned topologies are looked into. The high voltage capability, fewer harmonics in the output waveform and higher efficiency are some of the advantages that made multilevel voltage source noteworthy (M. Aleenejad, 2014).

A common drawback to the multilevel inverters is its complexity and cost due to the need for more number of power switches (SurinKhomfoi and L. M. Tolbert, 2007).

Some main features that make a multilevel converters include:

a) Common mode voltage
b) Input current
c) Output voltage waveform
d) Switching frequency.

Figure 2.1 shows classification of the converter.

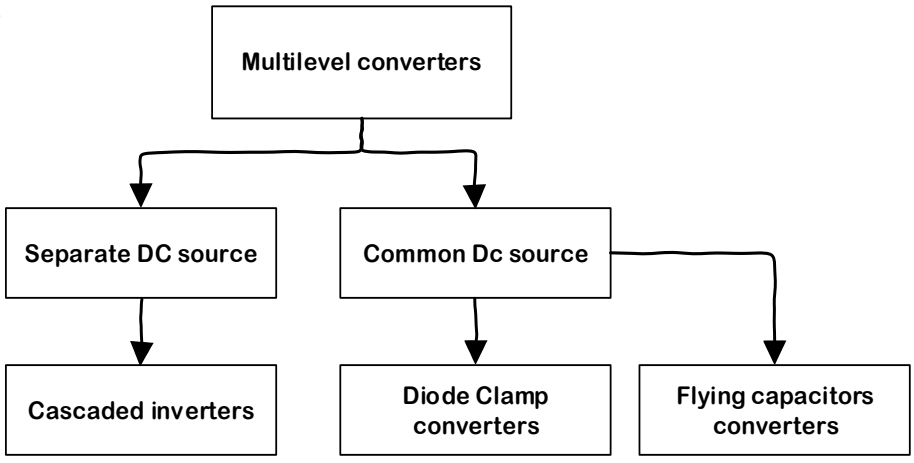

Figure 2.1: Multilevel converter topology (Anjali Krishna R, 2016)

Over the past years, so many multilevel inverter topologies have been proposed. (Rashid, 2006)

The predominant Multi-Level Converter topologies are:

1. Diode Clamped.
2. Flying Capacitor.
3. Cascaded H-Bridge.

2.2.1 Diode Clamped Topology

Diode clamp multi-level converter topology is an advancement of a three-level Neutral point inverter invented in the early 80's (JosÉ Rodrigue, 2009). Later in the 1990s, the number of steps was increased up to six levels. (N.S. Choi, 1991).

Clamping diodes are used in this type of converter to reduce the device voltage stress. An m_d level diode clamped converter needs $(2m_d - 2)$switching device, needs $(m_d - 1)$ input voltage source and $(m_d - 1)$ $(m_d - 2)$ number of diodes with a voltage Vdc across the diodes and switch (Anjali Krishna R, 2016) . Figure 2.2 shows single phase 5-level diode clamp converter. It comprises of four series connected capacitors in parallel with the Dc bus. The Dc bus input voltage V_{dc} is shared equally across the four capacitors, each having $\frac{V_{dc}}{4}$ across it. The output voltage step is determined by the number of series connected capacitors. For M steps diode clamp inverter, there are M-1 series connected DC bus capacitors. The clamping diodes have different voltage ratings depending on its position in the circuit. From figure 2 below, diode D3 should at least be able to block $\frac{3V_{dc}}{4}$ voltages were D1 will only block $\frac{V_{dc}}{4}$ (M.D. Manjrekar, 2000).

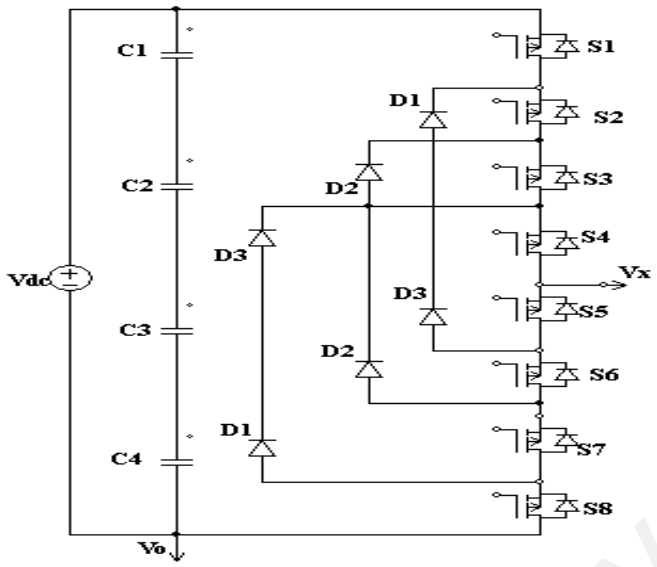

Figure 2.2: 5-level diode clamp converter

Table 2.1 below shows the possible output voltage steps between point Vx and Vo, with their allowable switching combination. Logic state1 and 0 corresponds to the switch On and Off states.

Table 2.1: Diode clamped Voltages with the corresponding switching combination

Voltage	Switching States							
V_{ox}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
V_1=0	0	0	0	0	1	1	1	`1
$V_2 = \frac{V_{dc}}{4}$	0	0	0	1	1	1	1	0
$V_3 = \frac{V_{dc}}{2}$	0	0	1	1	1	1	0	0
$V_4 = \frac{3V_{dc}}{4}$	0	1	1	1	1	0	0	0
$V_5 = V_{dc}$	1	1	1	1	0	0	0	0

From the table, it can be seen that switch (S_1, S5), (S_2, S6), (S_3, S7) and (S_4, S8) are operated complementary and in a sequential switching pattern. Each of the switching devices should at least be able to block $\frac{V_{dc}}{4}$ voltage level. The clamping diodes blocks

unequal reverse voltage. For instance, when the converter output voltage is at $V_1 = 0$, all the lower arm switches are said to be at On state, in this case D3 has to block $\frac{3V_{dc}}{4}$, D2 blocks $\frac{V_{dc}}{2}$, and D1 will block $\frac{V_{dc}}{4}$. In a situation where a converter is to be designed with the same rated diodes, then for a Dn-1 positioned diode, n-1 series connected diodes will be required to block $(n-1)\frac{V_{dc}}{n}$ reverse voltage (M.D. Manjrekar, 2000). Below is the list of advantages and disadvantages of diode clamped converter topology (Krug et al, 2007)

2.2.1.1 Advantages

1. It requires single isolated Dc supply; this warrants the possibility of having a back-to-back connection.
2. The dc bank capacitors can be charged simultaneously.
3. It provides a better efficiency when operated at fundamental switching frequency

2.2.1.2 Disadvantages

1. The number of clamping diodes increases with increase in voltage level. This brought about the additional cost and circuit complexity, especially in higher steps converters.
2. Unequal switching stress across the switching device, i.e. inner switches conduct for a short time compared with the inner switches.
3. Not suitable for redundancy

2.2.2 Flying Capacitor Topology

Flying capacitor (FC) is another converter topology that was invented in the early 90's by Maynard et al (Meynard & Foch, 2002). Its circuit connection is similar to that of a diode clamp, only that in this case capacitors were placed instead of diodes.

An m level diode clamped converter needs $(2m-2)$switching device and needs$(m-1)$ number of capacitors with a voltage Vdc across the `capacitors and switch (Anjali Krishna R, 2016).

Figure 2.3 shows its 3 phase circuit connection. The topology comprises of a ladder-like arranged dc link capacitors, each having a different voltage rating. The voltage difference between two adjacent capacitors determines the amplitude value of each step. To generate M-level phase voltage steps at Vxo, M-1 capacitors need to be connected serially at the dc-bus. The line voltage Vxy, in this case, will be (2M -1) levels.

One of the benefits of flying capacitor over diode clamp is its redundancy property. It can generate a particular output voltage using multiple switching sequences. Table 2 shows the possible switching combinations of a six-level output voltage waveform. For an M-level flying capacitor converter designed with equally rated capacitors, the number of phase capacitors can be found using the expression ((M-1) (M-2))/2 (JosRodrigue, 2009)

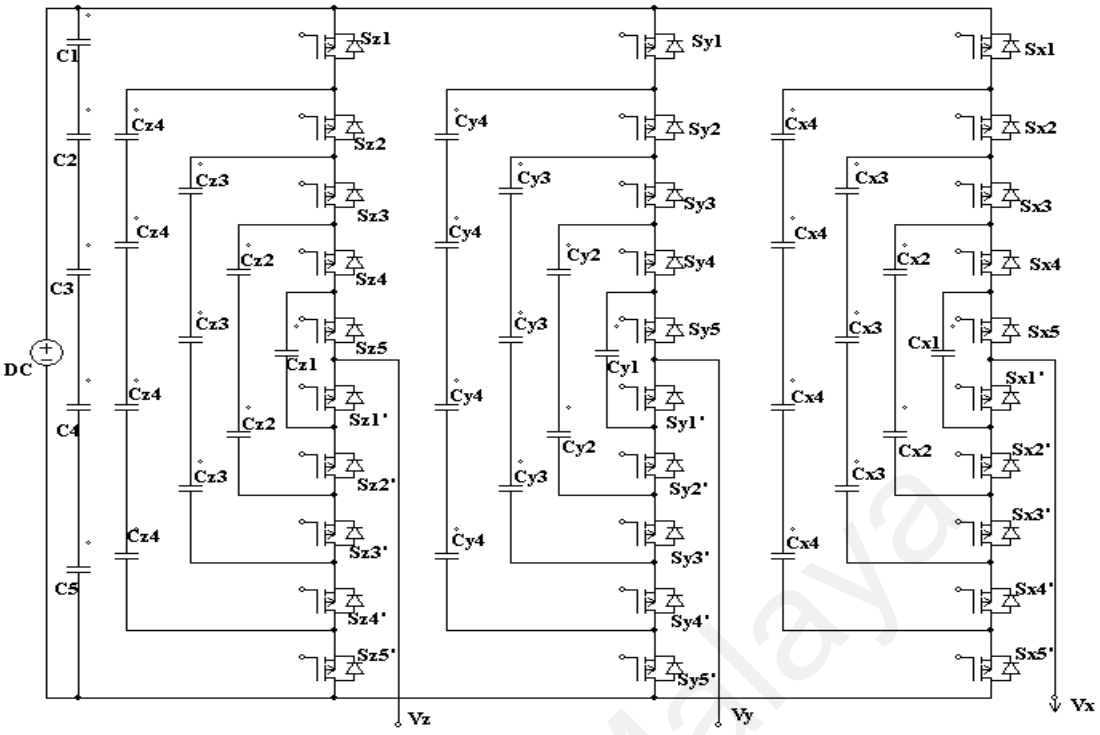

Figure 2.3: Five-Level Flying Capacitor Multi-level converter (Anjali Krishna R, 2016)

Table 2.2: Flying capacitor Multi-level converter possible switching combinations

Voltage	Switching States									
V_{ox}	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x1}'	S_{x2}'	S_{x3}'	S_{x4}'	S_{x5}'
5 V_{dc}(0 Alternative switching signal)										
$5V_{dc}$	1	1	1	1	1	0	0	0	0	0
$4V_{dc}(4-Alternative\ switching\ signal)$										
$5V_{dc}-V_{dc}$	1	1	1	1	0	0	0	0	0	1
$4V_{dc}$	0	1	1	1	1	1	0	0	0	0
$5V_{dc}-4V_{dc}+3V_{dc}$	1	0	1	1	1	0	1	0	0	0
$5V_{dc}-3V_{dc}+2V_{dc}$	1	1	0	1	1	0	0	1	0	0
$5V_{dc}-2V_{dc}=V_{dc}$	1	1	1	0	1	0	0	0	1	0
$3V_{dc}(5-Alternative\ swtching\ signals)$										
$5V_{dc}-2V_{dc}$	1	1	1	0	0	0	0	0	1	1
$4V_{dc}-V_{dc}$	0	1	1	1	0	1	0	0	0	1
$3V_{dc}$	0	0	1	1	1	1	1	0	0	0
$5V_{dc}-4V_{dc}+3V_{dc}-V_{dc}$	1	0	1	1	0	0	1	0	0	1
$5V_{dc}-3V_{dc}+V_{dc}$	1	1	0	0	1	0	0	1	1	0
$4V_{dc}-2V_{dc}+V_{dc}$	0	1	1	0	1	1	0	0	1	0
$2V_{dc}(6-ALternative\ switching\ signal)$										
$5V_{dc}-3V_{dc}$	1	1	0	0	0	0	0	1	1	1
$5V_{dc}-4V_{dc}+V_{dc}$	1	0	0	0	1	0	1	1	1	0
$4V_{dc}-2V_{dc}$	0	1	1	0	0	1	0	0	1	1
$4V_{dc}-3V_{dc}+V_{dc}$	0	1	0	0	1	1	0	1	1	0
$3V_{dc}-V_{dc}$	0	0	1	1	0	1	1	0	0	1
$3V_{dc}-2V_{dc}+V_{dc}$	0	0	1	0	1	1	1	0	1	0
$2V_{dc}$	0	0	0	1	1	1	1	1	0	0
$V_{dc}(4-alternative\ switching\ signal)$										
$5V_{dc}-4V_{dc}$	1	0	0	0	0	0	1	1	1	1
$4V_{dc}-3V_{dc}$	0	1	0	0	0	1	0	1	1	1
$3V_{dc}-2V_{dc}$	0	0	1	0	0	1	1	0	1	1
$2V_{dc}-V_{dc}$	0	0	0	1	0	1	1	1	0	1
V_{dc}	0	0	0	0	1	1	1	1	1	0
$0V_{dc}(0-Alternative\ switching\ signal)$										
$0V_{dc}$	0	0	0	0	0	1	1	1	1	1

The merits and de-merits of the multi-level flying capacitor are stated as follows (JosÉ Rodrigue, 20 October 2009).

2.2.2.1 Advantages

1. High-value capacitors can serve as a backup during a power failure and voltage sagging.

2. The topology allows the possibility of switching redundancy, which results in voltage stress balancing across the capacitors.

3. Allows the control flow of real and reactive power.

4. It requires single isolated dc supply voltage source.

2.2.2.2 Disadvantages

The number of capacitors is determined by the inverter output level. This makes the circuit looks bulky and difficult to package.

2. A complex control mechanism that requires feedback is involved. This is to maintain voltage across the capacitors.

3. The converter has poor efficiency due to high switching losses.

2.2.3 Cascaded H-bridge Topology

A cascaded H-bridge is a promising converter topology made up of series a connected H-bridge inverter module. (M. Malinowski, 2010) Figure 2.4 shows a single phase 5-level circuit configuration of the inverter. The circuit comprises of four full bridge modules with each having its own independent dc supply. The nine-level voltage steps are generated by adding up the individual output voltages generated by each module. By employing a systematic switching function on the switches, each of the H-bridge cells can synthesize three different voltage levels, positive (+E), zero (0) and negative (-E)

(Rodriguez, Lai, & Peng, 2002). The sequence of phase voltage steps is expressed in a unique and distinctive pattern from the earlier mentioned topologies. In this case, it is express as N= 2Pdc+1, where Pdc stands for the number of independent dc source

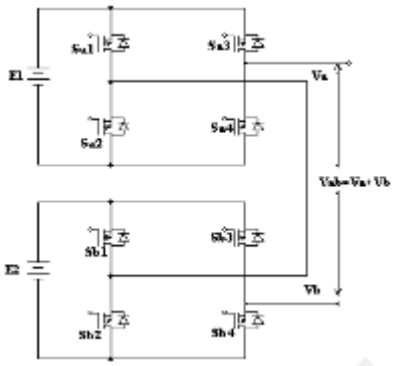

Figure 2.4: Single phase 5-level Cascaded H-bridge Converter

From the figure above, switch Sa1 and Sa2' are called the converter leg and are always operated complimentary to avoid short-circuiting the supply. The five-level switching sequences and their corresponding output voltage is given in table 2.3 below

Table 2.3: The five-level Cascaded H-bridge Converter switching sequences

Voltage	Switching States							
V_{ab}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
V_1=-2E	0	1	1	0	0	1	1	`0
$V_2 = -E$	0	1	1	0	0	1	0	1
V_3 =0	0	0	0	0	0	0	0	0
$V_4 = +E$	1	0	0	1	1	0	1	0
$V_5 = +2E$	1	0	0	1	0	0	0	1

Out of the three mentioned topologies in this paper, cascaded H-bridge topology uses the least number of power electronic components.

The advantages and disadvantages of this topology can be summarized as follows (Rodriguez, et al, 2002).

2.2.3.1 Advantages

1. There is an automatic voltage sharing across the switches in a module due to the usage of the independent voltage source. Therefore, reduces restriction in the switching sequence.
2. The converter produces more output voltage levels, providing a smooth and steady voltage change across the load, resulting in less THD for a particular operating frequency.
3. It modular nature makes its production, maintenance and redundancy integration much easier.
4. Higher voltage level can be achieved by series-connecting more H-bridges

2.2.3.2 Disadvantages

1. The need for separate independent dc supply by each of the H-bridge modules. This, therefore, increases the device cost and size

2.3 Three phase Hybrid inverters

Since this project is working on a modified three-phase inverter topology, it became pertinent after discussing the basic topologies to also review and report three-phase hybrid topologies along with their switching operational principles.

2.3.1 Three phase Multi-level DC link inverter topology

In an inverter circuit proposed by Rao et al(2013), the associated gate drive circuitry was reduced as it utilizes fewer switches in contrast to the 36 switches in the conventional three phase cascaded inverter topology. For m number of voltage level, MLDCL requires m+3 active switches per phase, which is half the number of switches and clamping diode required in diode clamped topology and in addition, half the voltage capacitor and clamping capacitors needed in flying capacitor topology.

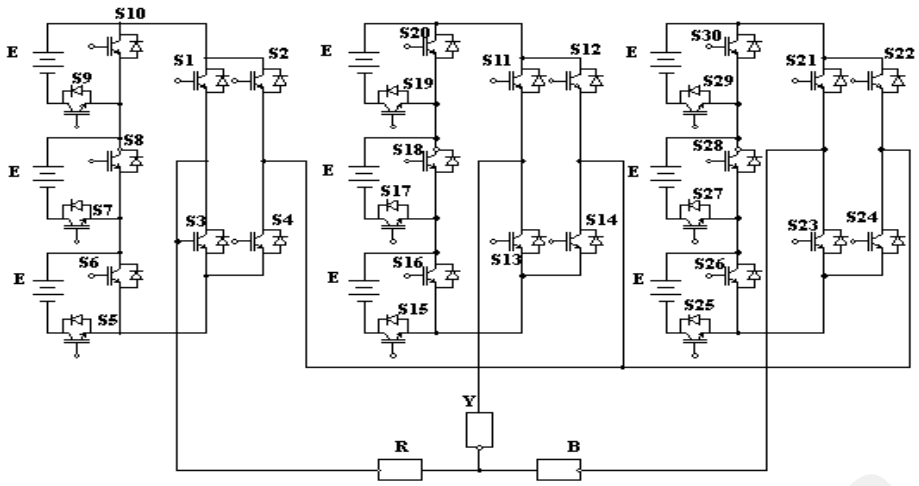

Figure 2.5: Three phase Multilevel DC link inverter topology

Figure 2.5 above shows the circuitry of the proposed hybrid MLDCL converter.

Sub-harmonic and modified space vector pulse width modulation are the techniques used in the proposed topology, table 2.4 below shows the switching state for the proposed single phase and the respective generated voltage.

Table 2.4: switching States for a single phase seven level MLDCL inverter

V_0	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
0	1	0	0	1	0	1	0	1	0	1
E	1	0	0	1	0	1	0	1	1	0
2E	1	0	0	1	0	1	1	0	1	0
3E	1	0	0	1	1	0	1	0	1	0
-E	0	1	1	0	0	1	0	1	1	0
-2E	0	1	1	0	0	1	1	0	1	0
-3E	0	1	1	0	1	0	1	0	1	0

2.3.2 Three phase reduced switch Multilevel Inverter Topology

This proposed topology produces a seven-level output voltage that is almost sinusoidal waveform thereby reducing lower order harmonics. The converter uses three H-bridge modules with one module per phase with 3 additional connected switches that allow the possibility of achieving the desired seven level waveform. There are a total of 21 switches and nine dc sources with three per phase. In order to determine the switching angles for

generating a fundamental output voltage, it uses fundamental switching scheme. Below is the circuit of a 3-phase 21 switch MLI (Gobinath.K, 2013)

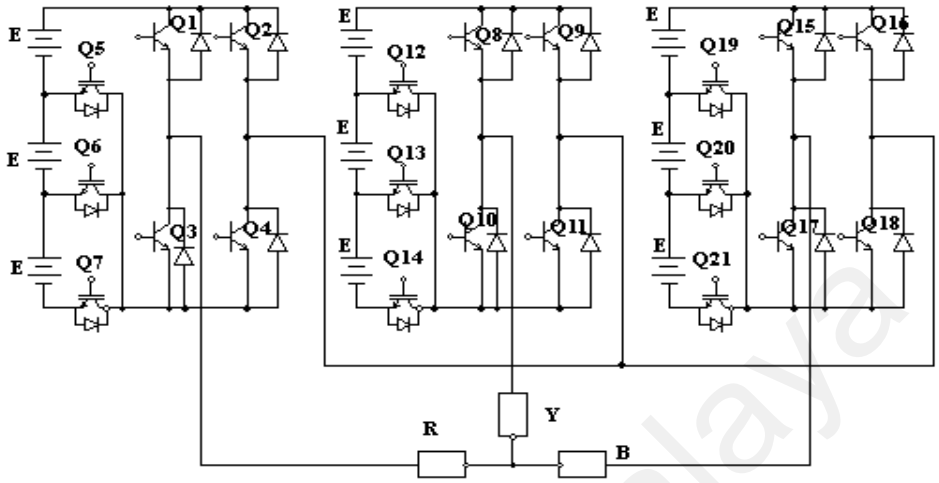

Figure 2.6: Three phase seven level Multilevel Inverter (Gobinath.K, 2013)

This proposed topology has three operating modes namely: Powering Mode, Free-wheeling mode and regenerating mode.

For the powering mode, the polarities for load current and voltage are the same. In the free-wheeling operating mode, one of the main switches is off and passage of the load current is due to load inductance. Whereas in regenerating Mode the stored energy in load inductance to be feedback to the source, the load current has to be positive during the negative half cycle and negative for the positive half cycle. (Gobinath.K, 2013)

Table 2.5: the Switching States for Three-phase seven level Multilevel Inverter

Switches in ON states	Output voltage [$V_{ao}(t)$]	States
S_1, Q_4	$-V_{DC}, 1$	1
S_3, Q_3	$V_{DC}, 4$	2
S_2, Q_4	$-(V_{DC}, 1 + V_{DC}, 2)$	3
S_2, Q_3	$V_{DC}, 3 + V_{DC}, 4$	4
S_3, Q_4	$-(V_{DC}, 1 + V_{DC}, 2 + V_{DC}, 3)$	5
S_1, Q_3	$V_{DC}, 2 + V_{DC}, 3 + V_{DC}, 4$	6
Q_1, Q_4	$-(V_{DC}, 1 + V_{DC}, 2 + V_{DC}, 3 + V_{DC}, 4)$	7
Q_2, Q_3	$V_{DC}, 1 + V_{DC}, 2 + V_{DC}, 3 + V_{DC}, 4$	8
Q_1, Q_3	0	9
Q_2, Q_4	0	10

2.3.3 Reverse Voltage Multilevel Inverter Topology(MIT)

Najafi, (2012) proposed a new MIT which has two functionalities. The first part utilizes high-frequency switches for the generation of level states, and the second part employs low frequency for the generation of the polarity of the output voltage. Therefore, these two high and low frequencies produce the required output voltage. The circuit diagram is shown in figure 2.7 below

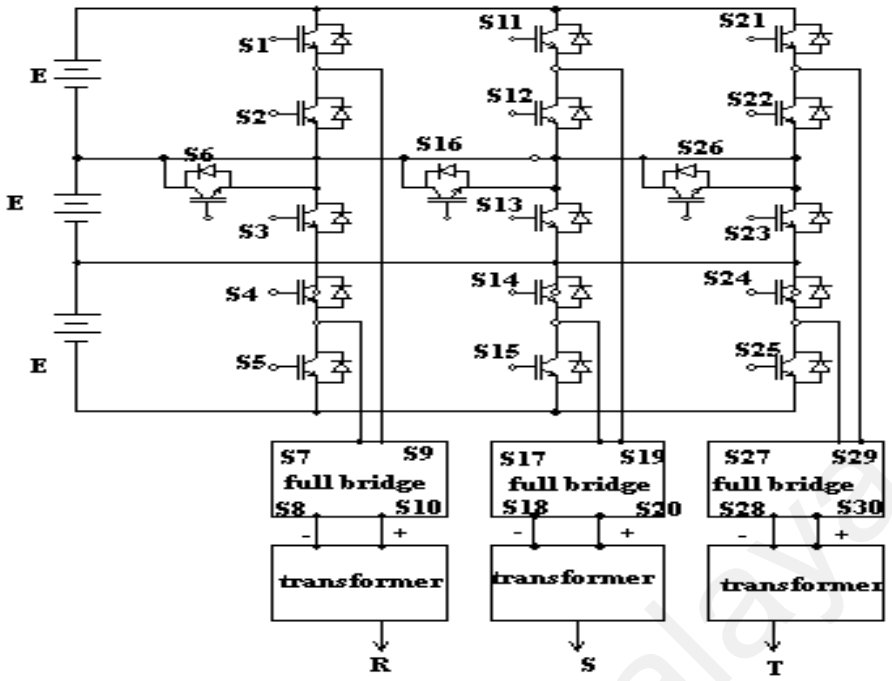

Figure 2.7: Reverse Voltage Multilevel Inverter Topology (Ehsan Najafi, 2012)

To generation a seven-level output voltage, two different topologies are integrated per phase which requires a total of 10 switches per phase. In the topology, the required non-polarized output waveform levels are generated by the upper six switches while generation of polarity is done by the lower 4 switches in the full bridge circuits. Duplicating the middle stage increases the output voltage level. As seen from the circuitry, to generate a particularly desired polarity, the output voltage is the input to the full bridge converter with the converter output fed into the primary of a transformer whose secondary is arranged in the delta and to the three-phase system.

2.3.4 Three phase Asymmetrical Cascaded Multilevel Inverter Topology

The converter is called asymmetrical cascaded MLIT due to its unequal magnitude of the input DC sources. This MLI topology can be integrated with renewable energy

sources as it requires a lesser number of DC sources (H. Belkamel, 2013). Figure 2.8 shows the circuit diagram of the asymmetrical cascaded topology

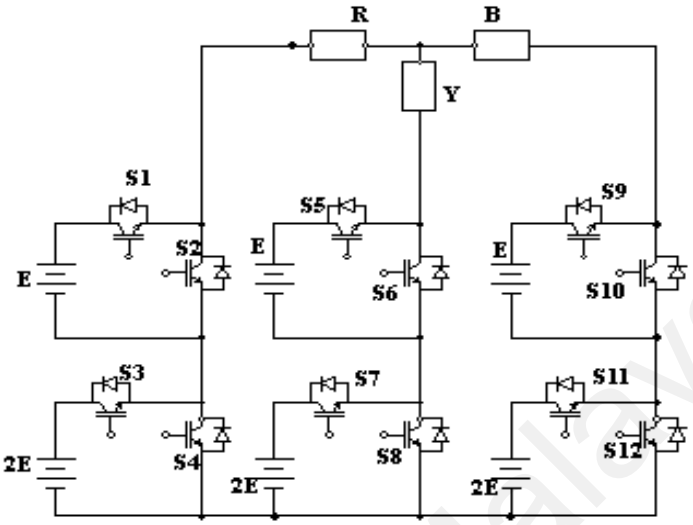

Figure 2.8: Three phase Asymmetrical Cascaded Multilevel Inverter Topology

The zero and E-level output voltage level are generated using with two switches and a single DC source. In order not to short-circuit the DC source, the switches s1 and s2 are operated in a complementary manner. The two DC sources and four switches of each phase of the proposed topology forms a module structure. Three basic unit can be added based on the required output voltage levels. It generates the pulse modulation signals through comparing of the reference sine wave with the carrier wave thereby generating pulse signals A1, A2, A3. Applying logical operations to these pulse signals as in equation 2.1 to 2.4 yields Z1, Z2, Z3 and Z4 respectively.

$$\boldsymbol{Z1 = (\overline{A2}\ X\ A3) + A1} \qquad \textbf{2.1}$$

$$\boldsymbol{Z2 = (\overline{A1}\ X\ A2) + \overline{A3}} \qquad \textbf{2.2}$$

$$\boldsymbol{Z3 = (\overline{A1}\ X\ A2) + A1} \qquad \textbf{2.3}$$

$$\boldsymbol{Z4 = (\overline{A2}\ X\ A3) + A3} \qquad \textbf{2.4}$$

Where ‘X’ and ‘+’ stands for logical operations of AND and OR respectively.

2.3.5 Three-phase Symmetrical Multilevel Inverter Topology

This is another proposed modular 3-phase symmetrical topology is proposed which produces 3-phase output voltage level using 12 switches (Ahmed Salem, 2015). Each phase comprises a battery and two switches in series and parallel respectively. Both switches connected to the battering are operated in complementary to each other. Increasing the number of phase elements(components) increases the number of the voltage level.

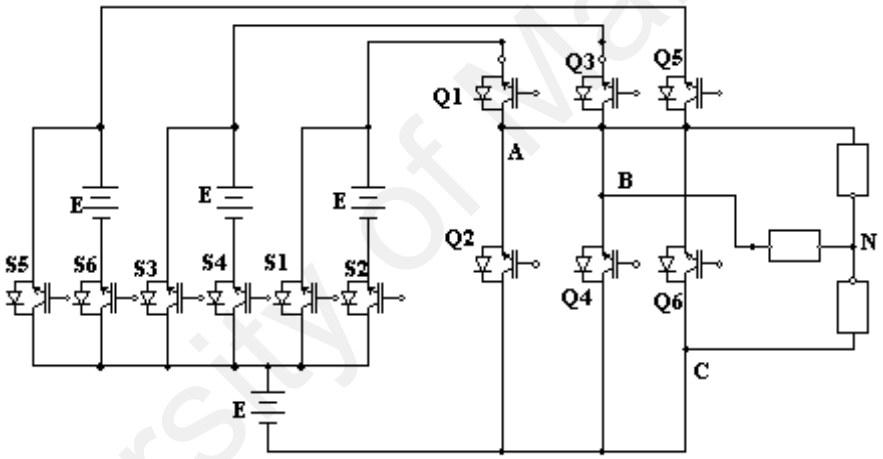

Figure 2.9: Three-phase Symmetrical Multilevel Inverter Topology (Ahmed Salem, 2015)

Equation 2.5 to 2.8 shows an expression of this topology that outlines the relationship between the number of cells, poles, levels, power electronic switches, and phase.

$$NPole = Ncell + 2 \quad (2.5)$$

$$Mlevel = 2Ncell + 3 \quad (2.6)$$

$$Nsw = 3(2Ncell + 2) \quad (2.7)$$

$$Nps = 3Ncell + 1 \quad (2.8)$$

Where NPole =number of poles

Mlevel = number of levels

New =number of power switches

Nps=number of power electronic switches

Ncell=number of cells.

2.3.6 Five-level three-phase cascaded hybrid multilevel inverter

Thongprasri, (2011) proposed a three-phase cascaded hybrid multilevel inverter which is made up of a combination of a 3-phase inverter in series with an H-bridge inverter with each having a separate dc power source. Uses multi-carrier based modulation sub-harmonic pulse width modulation (MC-SH PWM) FPGA board to generate produce the control signal. Figure 2.10 below shows the 3-phase topology of the proposed multilevel inverter

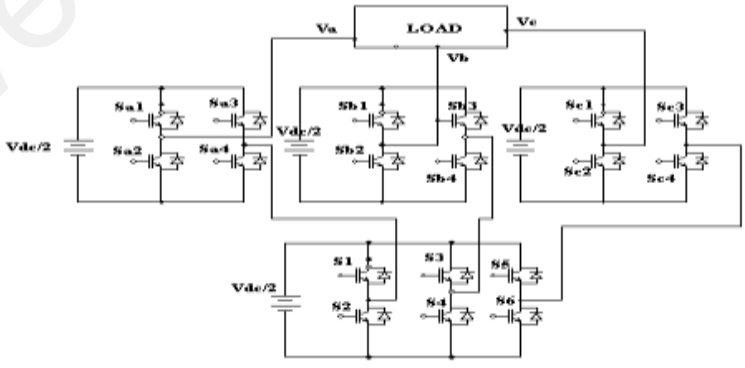

Figure 2.10: Five-level three-phase cascaded hybrid multilevel inverter

The tested the proposed topology using 3 different types of the load; 18W fluorescent lamp- ballast, RL, and 1HP 3-phase induction motor; without filtering. The single phase topology is shown below in figure 2.11

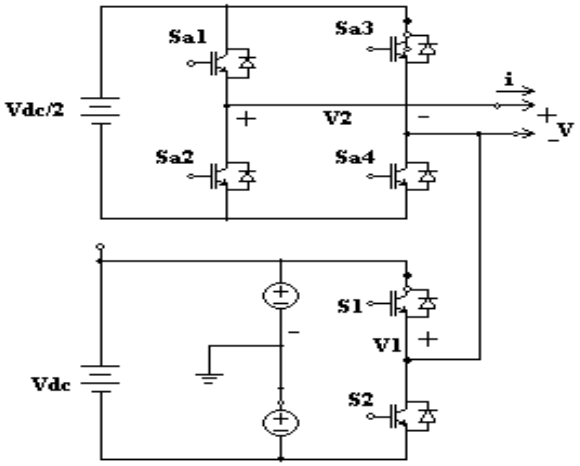

Figure 2.11: Single phase topology of the hybrid multilevel inverter

2.4 Converter Terminology, Assessment parameters, and reduced count topologies

Here, some commonly used terminologies in the field of multi-level power converters are highlighted and some converter assessment parameters are mentioned.

2.4.1 Multilevel Inverter Terminologies

1. Reduced Device Count Multilevel Inverter (RDC-MLI) Topologies refers to the topology in which for a given number of phase level the number of controlled switching devices is reduced.
2. Total voltage blocking capability: Refers to the maximum amount of reverse voltage the converter switches are capable of blocking. (J. Ebrahimi, 2012).
3. Symmetric and asymmetric source configuration: the term ‘symmetric’ in an MLI refers to when the voltages of the input dc level are equal, otherwise it is termed ‘asymmetric’ (Babaei, 2008). Binary and trinary are the two most known asymmetric source configuration. In the former, the voltage level values are in a geometric progression with a factor if ‘2’, and a factor of ‘3’for the later configuration. To synthesize more output level using the same number of power switches, an asymmetric source configuration is used. Numerous

researchers have produced other asymmetric source configuration (S. Daher, 2008)

4. Even power distribution: also known as “charge balance control” or “equal load sharing” (C.-C. Hua, 2009). When each input source of a multilevel conversion provides equal power to the load, such “power distribution” within the sources is said to be ‘even’. In some literatures, it is called “charge balance control” or “equal load sharing”.
5. Level- Generation and Polarity-Generation: MLI generates s stepped output waveform by controlling the dc input source in such a way that it adds up and subtracts to produce a level waveform. The generated output composed of both positive and negative polarities, allowing the realization of an alternating signal with positive and negative half cycle. The MLI converter switches in polarity generation circuit has to be able to withstand the operating voltage
6. Fundamental Frequency Switching: the switching frequency, current and blocking voltage are proportional to the switching losses in a converter (M. F. Kangarlu and E. Babaei, 2013). In order to minimize the switching loss, the MLI is operated at low frequency, which is usually called fundamental frequency while reserving the output quality.

2.4.2 Assessment Parameters

The general rule for assessing the performance of an inverter topology is based on:

1. Blocking voltage of the converter
2. Total number of power switch
3. Controllability of the topology
4. Ability to employ asymmetric voltage ratios

2.5 Comparison of the Hybridized three phase multilevel inverter topologies

With the aim of keeping the THD within the standard limit and lesser device count, researchers have proposed different control strategies. Table 2.6 shows the Comparison of some of the proposed three-phase topologies based on modulation techniques, number of diodes and switches, DC source and percentage of THD in the output.

Table 2.6: Comparison of Classical Topologies and reduced device count Topologies

S/N	Author	Topology	N_s	N_d	N_c	N_{dc}	N_t	Modulation technique	THD
1	Martins et al.,(2006)	Bi-directional switched inverter	6	0	2	1	0	PWM	25
2	Malinowski et al., (2010)	Conventional Cascaded H-bridge	36	0	0	9	0	Sub-Harmonic PWM	10.78
								Modified Space vector PWM	8.79
3	Thongprasri , (2011)	Hybrid MLI	18	0	2	4	0	Multilevel Carrier SHPWM	15.6
4	Najafi et al.,(2012)	Reverse Multilevel	30	0	0	3	3	Phase Deposition SPWM	3.85
5	Rao et al., (2013)	Multi-level DC link inverter	30	0	0	9	0	Sub-harmonic PWM	9.02
								Modified space vector	6.84
6	Gobinath et al.,(2013)	Reduced switch modified Multilevel Inverter	21	0	0	9	0	Selective harmonic Elimination	7.8
7	Belkamel et al.,(2013)	Asymmetrical MLVI	12	0	0	6	0	SPWM	25.609
8	Salem et al.,(2015)	Symmetrical MLVI	12	0	0	4	0	Low frequency Modulation	16.88
								Single carrier SPWM	34.83
								Two carrier SPWM	35.35

2.6 Multi-level Converters Modulation Techniques

Due to the rapid advancements in the field of power electronics and the tremendous breakthrough and confidence posed by multi-level converter technology, researchers are exploring every aspect of it, with aim of improving its overall performance. With the

subsequent invention and modification of topologies, the need for new and compatible modulation techniques to suit the new topologies can never be overemphasized, this is the reason why modulation technique is trending in the field of power electronics (Rodriguez, Lai, & Peng, 2002). The ever-rising complication of power control systems as the result of additional auxiliaries, the need to reduce switching losses and stress on individual power switches, have facilitated significantly in the advancement so far recorded in the field of modulation techniques (Li et al, 2002). Several techniques have been developed with each having its merits, de-merits and preferential area of application. Figure 2.11 shows the various classifications of multi-level converter modulation techniques. From the figure, it can be seen that the techniques are categorized into two broader groups based on their domain operation. These are the state space vector techniques and the voltage level based approach (Bernet, 2006). The former operates based on the voltage space vectors while the latter operates on voltage level over a period of time

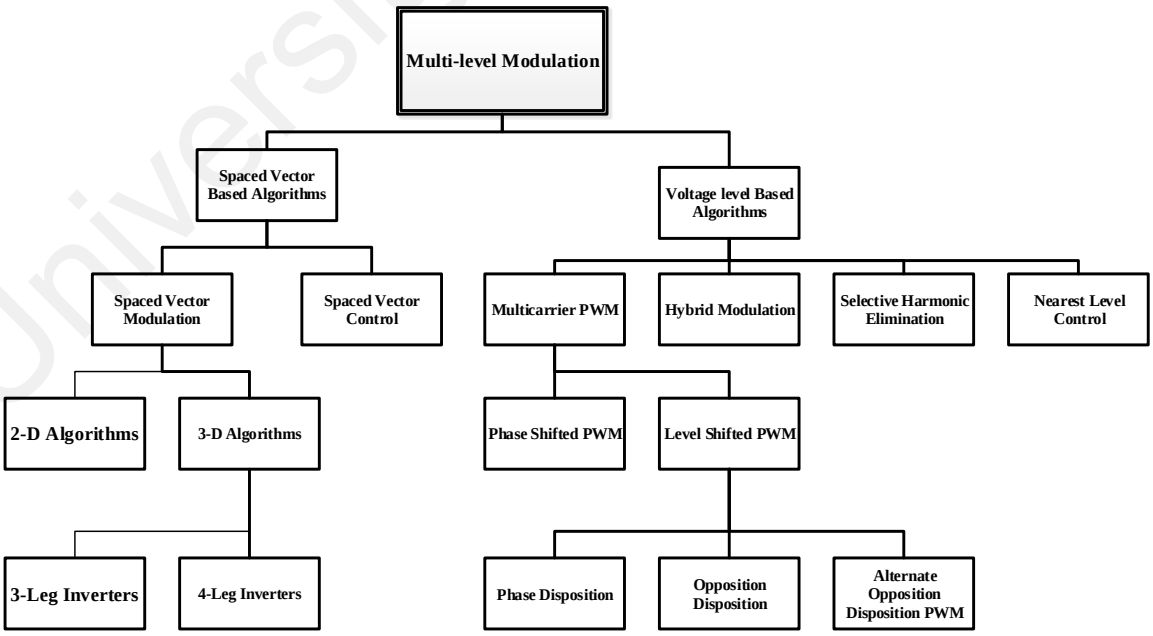

Figure 2.12: List of Multi-Level Converter Modulation techniques

2.6.1 Carrier Based Pulse Width Modulation

The early PWM techniques were transformed and upgraded to be applied to the current multi-level topologies. The new technique, unlike the conventional counterparts, produces the control signal using multiple carrier signals, hence called multi-level PWM (Brendan Peter McGrath, 2002). FC and CHB topologies can both be configured in modular form, hence giving the leverage of each module to be modulated independently using bipolar and unipolar sinusoidal carrier PWM, this amount to equal power distribution in the module cells. An N cell of FC and CHB will require (180°)/N and (36°)/N carrier phase shift respectively to generates a low harmonic distorted multi-level voltage waveform (Bornhardt, 06 August 2002). This technique is denoted as Multi-Level Phase Shift Sinusoidal Pulse Width Modulation (MPSSPWM). Its major advantage is its ability to suppress the harmonics at the inputs of CHB's converters and also it has the capability to provide a balanced dc voltage in FC converter topologies. A new different approach called Level Shift Pulse width modulation (LSPWM) was introduced, it requires superimposing two carrier signals on each other. This technique is further sub-classified into 3 categories namely Alternate phase opposition (APOD), Phase opposition disposition (POD-PWM) and Phase disposition (PD) on the bases of the spatial orientation of the carrier signal (Brendan Peter McGrath, 2002).

2.6.2 Space Vector Modulation (SVM)

This technique involves comparison of converter gating signal with the vector representation of a sinusoidal reference (V_{ref}), where by an exact replica of the reference voltage is reproduced at the converter output (Bornhardt, 06 August 2002). SVM technique is currently been applied on various converter topologies, resulting in the development of new algorithms that suits the existing topologies, this can be seen in the

variously reported literature. The reported techniques are application specifics that are designed to work on a fixed converter output steps. The higher the output steps, the more complex the control algorithms and the mathematical computations. The drawback poised by the complex algorithms and rigorous computations was later addressed in subsequent literatures (Celanovic & Boroyevich, 2002) . Franquelo et al in his article "Space vector modulation technique for multi-level converters", proposed a new algorithm that uses simple computational procedures to produce a reference value close to the state vector, hence eliminating the need for lookup tables. In addition to reducing tedious computations, it also disputes the notion that says the more the output steps the more the computational complexity. In another literature, a new 2 Dimensional SVM technique was presented in (Bernet, 2006). The technique is suitable for application in 3-phase balanced system where all triple harmonics have canceled. A more sophisticated algorithm that warrants an online vector calculation was presented in (Prats, et al., 2004), it is called 3 Dimensional algorithms because it is an upgraded version of the earlier discussed 2D, it has further minimized mathematical computations and eliminate the links between circuit complexity and converter output step. This technique is applicable to both balanced and unbalanced systems (Prats, et al., 2004).

2.6.3 Selective Harmonic Elimination Method (SHE-PWM)

Another name given to this modulation technique is offline or pre-calculated modulation technique. It was first proposed by Patel at et al. (Hoft, 1973). This is a non-carrier based technique because it only requires some pre-calculated angles that are stored in a lookup table (memory) (Z. Du, 2006). These angles are generated by first finding the Fourier expansion of the voltage waveform, which happens to be a non-linear trace-dental equation.

Based on the odd quarter wave symmetry theory, the dc components and even harmonics will cancel out will be left with the fundamental and odd harmonic components (Menzies & Zhuang, 2002). The fundamental component is equated to a constant value which is determined by the selected modulation index, and the odd harmonics are equated to zero. The generated equations have no direct solution. Hence, numerical techniques which involve iterative procedures as in Newton Raphson method (Ozpineci, Tolbert, & Chiasson, 2004). the mathematical resultant method which uses the concept of polynomials, optimization techniques or Hybrid genetic algorithm (Chiasson, 2003) are capable of providing approximate values of the angles. SHE method has drastically reduced switching loss, which is the reason why it has been extended to high power multi-level converters (Z. Du, 2006).

Its drawback is its restrictions to open loop systems and the complexity in finding the switching angles for a higher number of steps. These limitations resulted in the invention of other low switching loss techniques with feedbacks that are suitable for higher level applications (Bernet, 2006).

2.6.4 Sinusoidal PWM (S-PWM):

This technique works based on the comparison of a referenced sinusoidal wave and a triangular carrier wave. The output voltage waveform is formed as a result of the gating signal been fed into the inverter switches. These gating pulses are formed when the reference wave is larger than the carrier waves as depicted in the figure below. (S. K.Peddapelli, 2014)

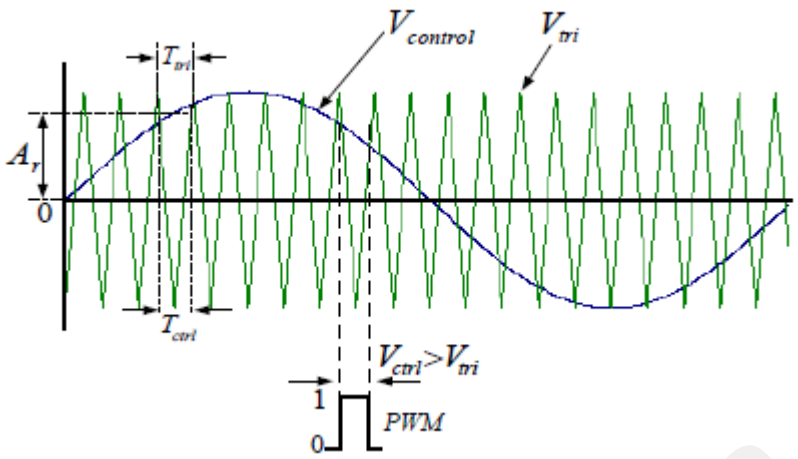

Figure 2.13: Sinusoidal PWM

2.6.5 Phase Disposition (PD) PWM:

This technique enhances output voltage of a multi-level converter by optimally suppressing the output harmonics. Hence, minimizing the distortion level in the voltage waveform. It employs several optimization techniques, the likes of gradient optimization algorithms. (G. T. Son, 2014)

2.6.6 Staircase Modulation

The staircase modulation method is most suitable for elimination of device stresses and switching losses in higher voltage and power energy conversion. It does so by determining the optimal primary values of the switching angles. Particle Swarm optimizing algorithm can be utilized in solving the transcendental equations, because it makes the switching angle solution converges at the global minimal (K. Shen, 2014)

2.6.7 Stepped Modulation

Here, the modulating signal is a stepped wave which is divided into intervals with each interval controlled separately to minimized specific harmonics. Converters controlled

using this technique has less distortion compared to the conventional PWM modulation method. (S. K.Peddapelli, 2014)

2.7 Application of Multi-Level Converters:

As earlier stated, multi-level converters positive properties make it famous and attractive to high power medium voltage industries. A number of publications were made on the industrial application of multi-level converters especially the one found in high power ac drives systems like electric trains, power generation stations, crane conveyors and refineries (Rodriguez, et al, 2002). Figure 2.14 below summarizes the various areas of multi-level converter applications.

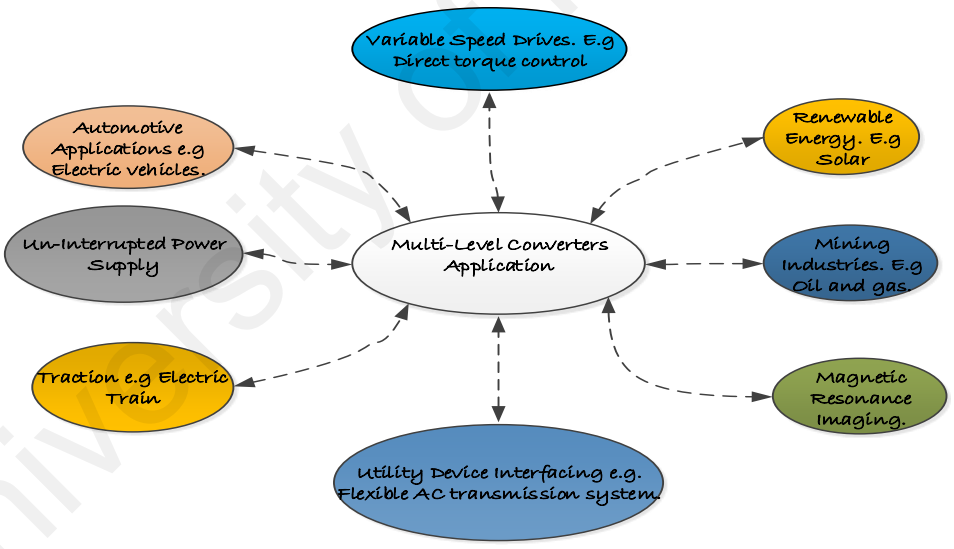

Figure 2.14: Multilevel Converter Applications

It's worth mentioning that most of the stated converter topologies can be used in any of the stated applications, though some specific topologies appear to be more efficient and reliable in some specific area of application (Rodriguez et al 2002). A High Voltage DC transmission system with only one Modular Multi-Level Converters converter and a diode rectifier which has a short-term energy storage capability and low cost. (Jie Guo, 2016).

An approach and improvement were made on the existing multi-level inverter used for electric vehicles. It is designed such that the switching devices isolate the connected low battery of the power system. This method makes the electric vehicles wiring system to be done exposed, which makes the entire system safe and easily accessible.

2.8 Conclusion

This chapter presented a comprehensive discussion on the multilevel converter. Emphasis is given to the three major converter topologies: Diode Clamped, Flying Capacitor, and Cascaded H-Bridge where their operational characteristic, advantages, and disadvantages were presented. Some of the latest proposed three-phase multilevel inverter topologies based on their applications, layouts, switching operation, modulation techniques, have been reviewed in this paper. These topologies have the merits of lower total harmonic distortion, reduced number of switches as compared to the conventional multilevel inverter topologies. A brief comparison of these topologies is also carried out. Also, different modulation techniques such as the multilevel converter carrier base PWM, Space vector Modulation Techniques (SVM), and Selective Harmonic Elimination method (SHE-PWM) are reviewed. Finally, the applications of multilevel converters are highlighted. There are literatures on numerous multilevel converters technology. The presence of various different literatures is due to the fact that there is no one topology of multilevel converter that has all the solutions when looked in terms of simplicity and performance

CHAPTER 3: DESIGN METHODS AND IMPLEMENTATION

3.1 Introduction

The aim of this chapter is to outline the necessary design method and procedures involved in the course of conducting this project. The block diagram in figure 3.1 below represents the whole system. It is categorized into three sub-sections namely Power circuits, gate drive circuits, and the control circuits. The power circuits section comprises of the Dc Power supply, Cascaded H-bridge modules, Isolation transformers and the load. The Gate drive circuit comprises a gate drives IC and its external auxiliaries. While the control circuits contain a peripherals interface controller (PIC) and its external connections. Even though the project is based on simulations but each of the sub-block diagrams will be discussed in detail to enable and ease its practical implementation.

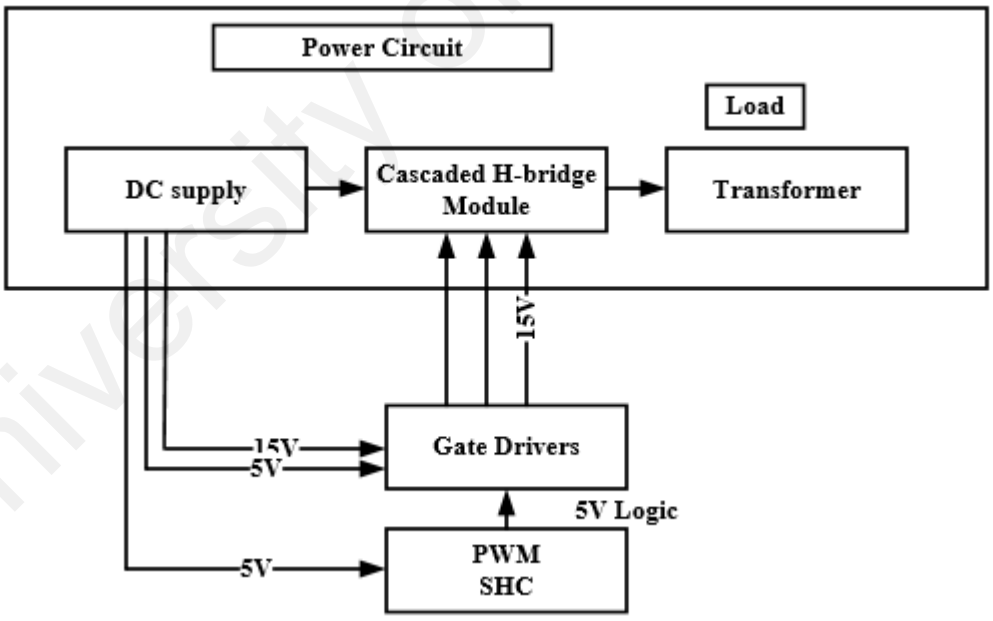

Figure 3.1: system block diagram

3.2 Power Circuits

3.2.1 Direct current (dc) power supply

In the simulation, a 30 Volts DC power supply is used as the power source to the circuit electronic components. But when implementing the circuit, a laboratory Dc supply can be used. The device should be capable of supplying three isolated outputs. The ground terminal should be isolated, because of the floating point requirement. From the block diagram above, it can be seen that one of the terminals was connected to the Cascaded H-bridge modules. This is the single dc supply terminal used as input to the two converter modules. The 15v terminal was connected to the IGBT driver Vcc terminal, while the 5v terminal is to be connected to the driver supply logic level Vdd and the PIC microcontroller Vcc supply pin. In reality, a photovoltaic wind or battery cell could be used to power the system. Also worth mentioning is the device power handling capability. The power supply used should be able to supply the system requirement power.

3.2.2 Cascaded H-bridge Modules

Even though this topology has been described in the literature section, but still there is the need to further explain it at this stage. The cascaded H-bridge converter is the topology used in this thesis. It is a three-phase circuit consisting of two parallel connected H-bridge modules per phase. The uniqueness of this topology is that all the 3-phases are fed through a single DC source supply. Each of the modules has four semiconductor switches and is configured such that it can generate a quasi-square voltage waveform (+E, 0, -E) at its output terminal. Figure 3.2 below shows the three-phase topology connection. E denotes the main dc source from the power supply unit. S_1,S_2,….S_{24} are the semiconductor

switches.G_1, G_2,…, G_{49}, represent the gating signals used for controlling the IGBT on and off state.

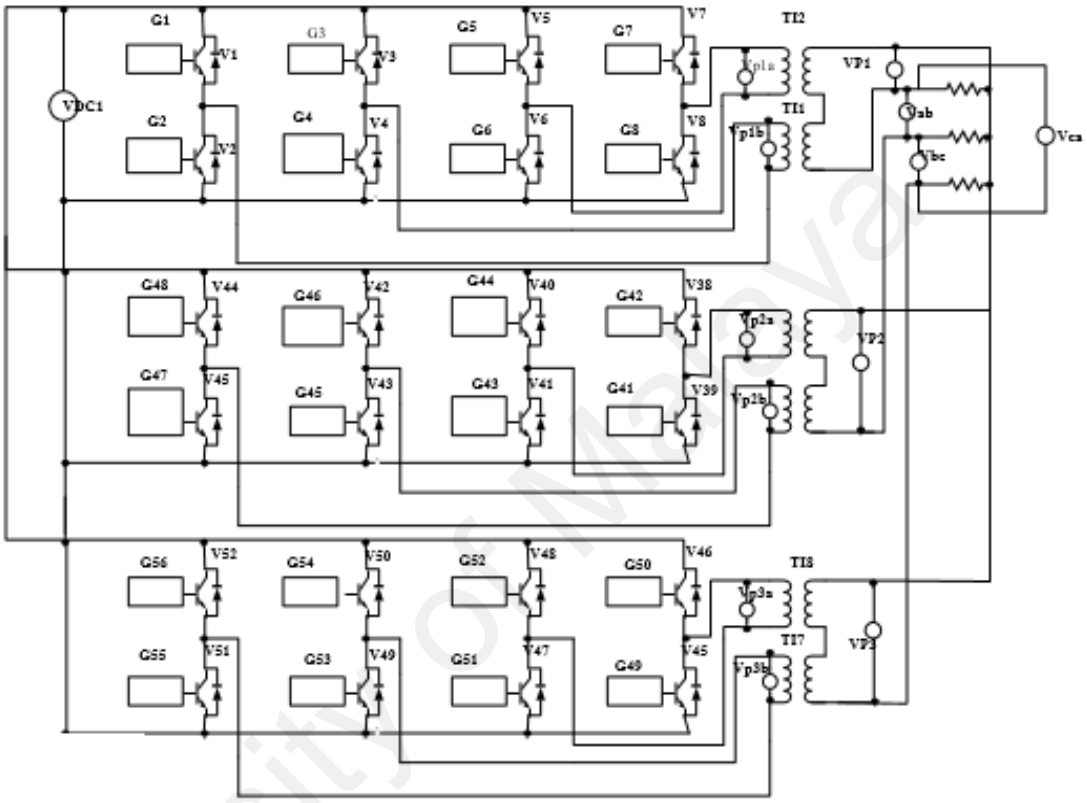

Figure 3.2: The three-phase H-bridge connection

3.2.3 Power Electronic Switch

The switch used in this thesis are insulated gate bipolar junction transistor IGBT. It was selected because of its high current and voltage rating, high switching speed, low switching loss, short circuit withstand capability and easily driven gate-emitter junction. These positive features put it on top of the other transistor switches (BJT, MOSFET) specifically in the area of power electronics. When selecting a specific IGBT for a project, consideration should be given to the device operating voltage and current, device switching speed, gate threshold voltage level and short circuit withstanding period. All these were chosen to satisfy the project design specifications.

3.2.4 Isolation Transformers

The proposed circuit as seen from the circuit configuration should have three specially designed transformers, with each per phase. The transformers should be customized such that it has two independent input primaries and two series connected secondary side all having 1:1 turns ratio producing an output voltage across the load given by equation(3.1) and (3.2) below. The essence of the transformer is to allow switching control freedom because, without the transformer in place, certain switching combinations will result in short-circuiting the source. The transformer also provides isolation and the winding reactance to some extent serves as a filter.

$$V_{out} = V_1 + V_2 \qquad 3.1$$

$$\frac{V_p}{V_s} = \frac{N_p}{N_s} \qquad 3.2$$

3.2.5 The Load

There are various types of loads, but in this thesis, we consider only resistive loads in the simulation. Various loads are considered in order to measure the converter.

For the experimental, a decade resistance box can be used as the load in the system. It is a device that contains inbuilt discrete resistance. A value of a resistance is dialed in by positioning the mechanical performance and efficiency adjuster to one of the discrete values offered by the box.

3.2.6 Switching angles analysis

The modulation technique employed on any kind of converter topology plays a major role in determining the properties of its output waveform (Chiasson, et al, 2003).

As mentioned in the thesis objective, Selective harmonic elimination method is the modulation technique to be used in generating the nine levels output voltage. Therefore, the switching angles need to be carefully chosen such that the lower order odd non-triplen harmonics are eliminated. The triplen will cancel out of the line voltage. This technique apart from producing an output with a lower total harmonic distortion THD it also reduces the amount of Electro-Magnetic Interference EMI and switching losses caused by high switching frequency modulation techniques.

To have an idea of how the angles should be. A rough sketch of the 5 levels single-phase waveform was made using arbitrary values of switching angles. Figure 3.3 depicts a rough sketch of the targeted five levels waveform with the assumption that it is an odd quarter wave symmetry

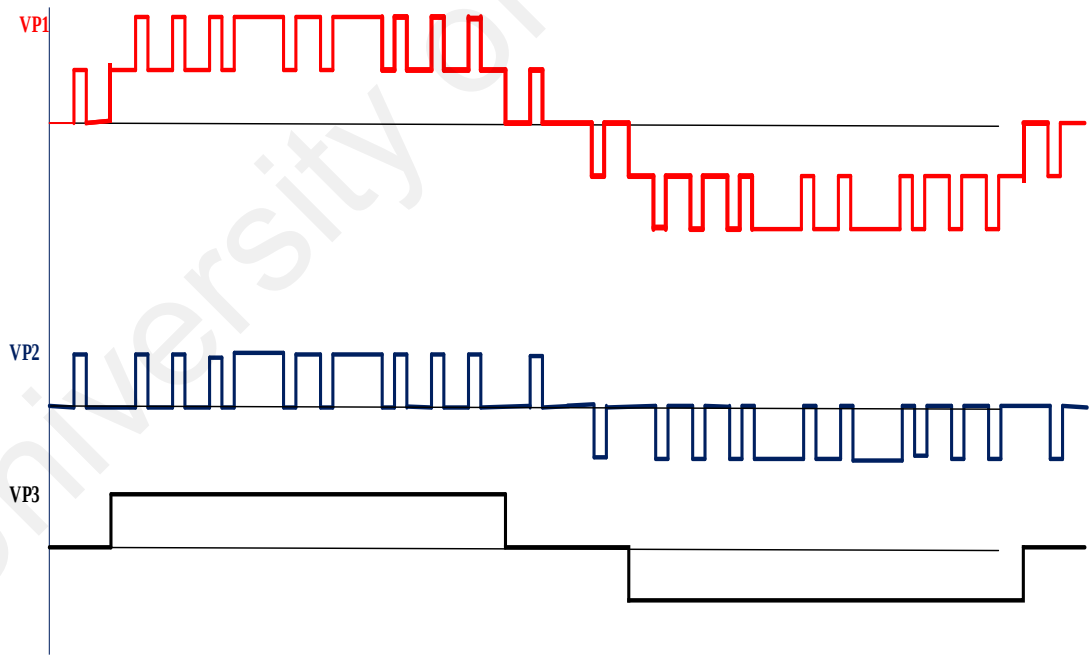

Figure 3.3: Single phase 5 levels waveform

For a single phase odd quarter waveform, both the dc and even harmonic components tend to cancel out, only the fundamental and odd harmonic components will remain. The triple harmonics will be eliminated in the line voltage. In order to eliminate the targeted harmonics, the fundamental component needs to be symmetrically controlled

both during the positive and negative half cycle at certainly specified angles. With this operation, lower order odd harmonics (N-1) will be eliminated (where N is the number of switching angle) (Chiasson, et al, 2003). Therefore, $5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th}, 23^{rd}, 25^{th}, 29^{th}, 31^{st}, 35^{th}$ order harmonics will all be eliminated in this case.

Based on the quarter wave symmetry, the Fourier series expansion of the five levels waveform in figure 3.3 above is given by (Z. Du, 2006),

$$\boldsymbol{V_{out}(wt) = \sum_{n=1}^{\infty} a_n \ \sin(nwt)} \qquad \textbf{……..3.1}$$

Where

$$\boldsymbol{a_n = \frac{4E}{n\pi}\sum_{K=1}^{N}(-1)^{K+1}\cos(n\alpha_K)} \qquad \textbf{…….3.2}$$

$$\boldsymbol{for\ odd\ values\ of\ n}$$

$$\boldsymbol{b_n = 0} \qquad \textbf{…… 3.3}$$

$$for\ all\ value\ of\ n$$

α_K Denotes the switching angles and most satisfies the relationship,

$$\boldsymbol{\alpha_1 < \alpha_2 < \ldots\ldots < \alpha_N < \frac{\pi}{2}} \qquad \textbf{……. 3.4}$$

E is the value of the dc supply voltage,

N is the switching angles per quarter wave

n is the odd harmonic order,

w is the angular frequency,

t is time.

Simplifying equation (3.5)and (3.6) the amplitude of the fundamental and odd harmonic components of the nine levels waveform in figure 3.3 above are calculated and represented by the non-linear transcendental equations (3.9) and (3.8)below:

$$\boldsymbol{h_1 = \frac{4*E}{\pi}\{\cos(\alpha_1) - \cos(\alpha_2) + \ldots\ldots \pm \cos(\alpha_{12})\}} \qquad \textbf{3.5}$$

$$\boldsymbol{h_n = \frac{4*E}{n\pi}\{\cos(n\alpha_1) - \cos(n\alpha_2) + \ldots\ldots \pm \cos(n\alpha_{12})\}} \qquad \textbf{3.6}$$

The amplitude of the fundamental component is controlled by the modulation index (M) and is given by the expression

$$\text{Modulation Index (M)} = \frac{h_1}{E} \qquad \textbf{3.7}$$

For all n =

While M=0 for all n ≠ 1

Therefore, using equations(3.8)(3.9) and(3.10), the transcendental equations can be expressed as:

$$\boldsymbol{\cos(\alpha_1) - \cos(\alpha_2) + \ldots\ldots + \cos(\alpha_{11}) - \cos(\alpha_{12}) = \frac{M\pi}{4}} \qquad \textbf{3.8}$$

$$\boldsymbol{\cos(5\alpha_1) - \cos(5\alpha_2) + \ldots\ldots + \cos(5\alpha_{11}) - \cos(5\alpha_{12}) = 0} \qquad \textbf{3.9}$$

$$\vdots$$

$$\boldsymbol{\cos(35\alpha_1) - \cos(35\alpha_2) + \ldots\ldots + \cos(35\alpha_{11}) - \cos(35\alpha_{12}) = 0} \qquad \textbf{3.10}$$

The above non-linear transcendental equations are solved to find the approximate close value of the switching angles, capable of eliminating the converter highlighted harmonics. Due to the non-linearity of the equations, it is not possible to find the solution using ordinary mathematical methods. Therefore, the genetic optimization algorithms

presented was used to find the solution of the 12 switching angles. The technique uses different values of modulation index (M) to find the solutions of the switching angles $\alpha_1, \alpha_2, \ldots, \alpha_{12}$.

The angles at modulation index (M) = 3.3 were considered in this thesis. Using the quarter wave symmetry properties, the remaining corresponding angles for both positive and negative axes were calculated.

3.2.7 Terminal voltage analysis:

Figure 3.4 and 3.5 shows the targeted output voltage waveform at the terminals of a single phase module 1 and 2 with their gating signals. The generated voltages were then passed through isolation transformers with 1:1 winding ratio in order to produce their sum at the secondary sides across the load as shown in figure 3.3 above. In order to generate the voltage waveform, a gating signal of each of the switches' needs to be generated based on the computed switching angles. The gating signals were then transformed into the binary sequence, where the 5V high was taken as logic 1 and 0V low was represented by logic 0. The IGBT's conduction states during the positive and negative half cycle in both H-bridges are given in Table 3.1 below

Table 3.1: IGBT conducting states

Voltage	Switching States							
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$+0$	1	0	1	0	1	0	1	0
$+E$	1	0	0	1	1	0	0	1
-0	0	1	0	1	0	1	0	1
$-E$	0	1	1	0	0	1	1	0

In any H-bridge module, switches on the same leg are always operated complementarily to avoid short-circuiting the dc source.

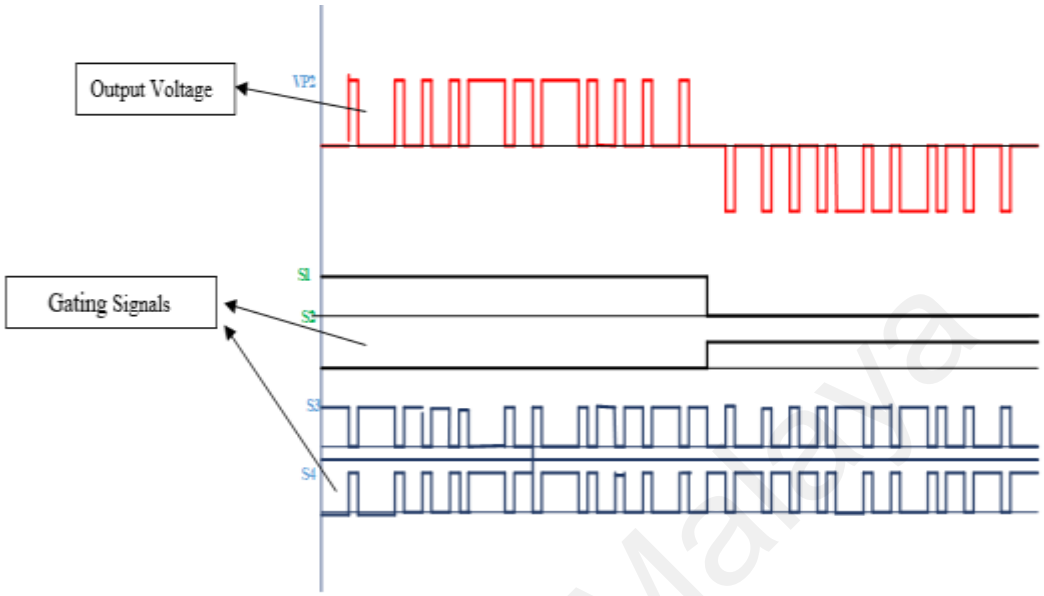

Figure 3.4: H-bridge Module 1 terminal voltage (V1) and gating signals

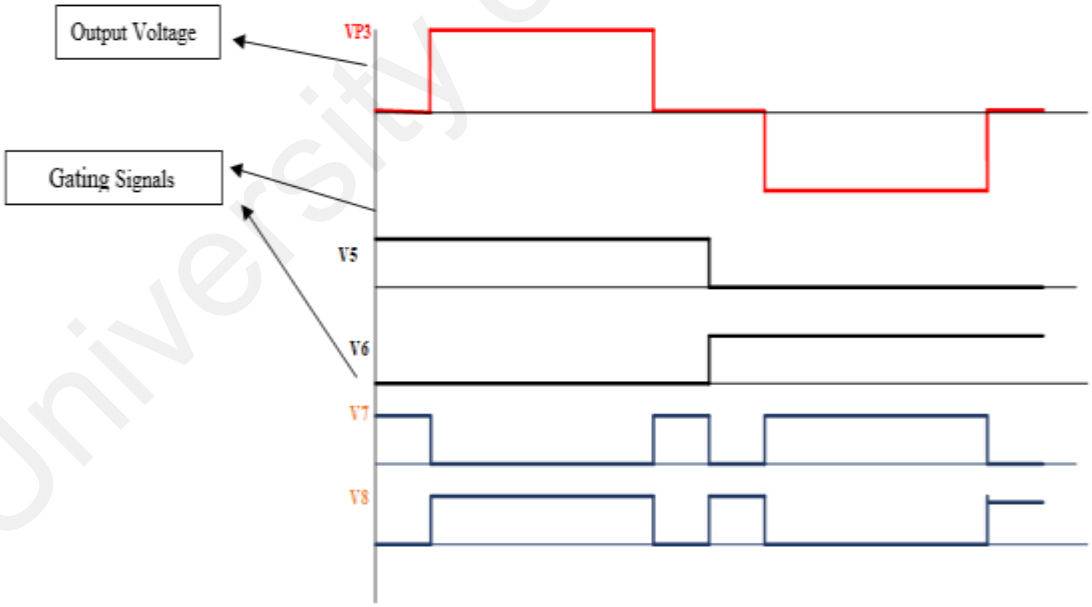

Figure 3.5: H-bridge Module 2 terminal voltage (V2) and gating signals.

3.2.8 Gate Driver Circuit.

Even though the thesis is based on simulations, but it will be better to outline how the system will be implemented practically. The voltage level of the switching signals

generated by the Micro-controller is not enough to drive the gate of the IGBT's. This results in the need for another circuit that can amplify the signal level to the required magnitude. Therefore, a gate driver is needed for the ON and OFF of the IGBT. There are several gate drivers in the market but let's consider a common one that has a simple configuration (IR2110). In this project, twelve IR2110 are needed to serve this purpose.

CHAPTER 4: RESULT AND DISCUSSION

4.1 Design Verification Using PSIM Software

In an effort to verify the proposed nine level waveform design procedures performed in the previous section, the circuit in figure 3.2 was set up in PSIM software. The circuit was then simulated using the calculated switching angles for two reference points M= 3.3 with switching angle distribution ratio of 3/9. The converter is a three-phase, so triple harmonics needs not to be considered. There are 12 switching points per quarter cycle. Therefore, based on the selective harmonic elimination theory (N-1) (Chiasson, et al, 2003), both the two cases can eliminate 11 lower order odd harmonics, if the fundamental component is properly switched at the pre-calculated angles given in table 4.1, 4.2 and 4.3.

4.2 Switching Angles

Tables 4.1, 4.2 and 4.3 below show the calculated values of the switching angles for phase 1, 2 and 3 respectively which were found using the method proposed in (Dahida, 2008) and completed based on the quarter wave symmetry theory.

Table 4.1: Phase 1 switching angles five level Voltage level 3/9

s/n	0-90	Actual time (s)`	90-180	Actual time (s)`	180-270	Actual time (s)`	270-360	Actual time (s)`
1	13.40246	0.000744581	166.5975	0.009255	193.4025	0.010745	346.5975	0.019255
2	15.67567	0.000870871	164.3243	0.009129	195.6757	0.010871	344.3243	0.019129
3	19.61681	0.001089823	160.3832	0.00891	199.6168	0.01109	340.3832	0.01891
4	35.50001	0.001972223	144.5	0.008028	215.5	0.011972	324.5	0.018028
5	37.80673	0.002100374	142.1933	0.0079	217.8067	0.0121	322.1933	0.0179
6	46.26136	0.002570076	133.7386	0.00743	226.2614	0.01257	313.7386	0.01743
7	48.24797	0.002680443	131.752	0.00732	228.248	0.01268	311.752	0.01732
8	54.85481	0.003047489	125.1452	0.006953	234.8548	0.013047	305.1452	0.016953
9	58.37752	0.003243196	121.6225	0.006757	238.3775	0.013243	301.6225	0.016757
10	61.01313	0.003389618	118.9869	0.00661	241.0131	0.01339	298.9869	0.01661
11	83.87128	0.004659516	96.12872	0.00534	263.8713	0.01466	276.1287	0.01534
12	86.0193	0.00477885	93.9807	0.005221	266.0193	0.014779	273.9807	0.015221
13	90	0.005	180	0.01	270	0.015	360	0.02

Table 4.2: Phase 2 switching angles five level Voltage level 3/9

s/n	0-90	Actual time (s)	90-180	Actual time (s)	180-270	Actual time (s)	279-360	Actual time (s)
1	133.40246	0.007411248	286.5975	0.015921667	313.403	0.017411667	466.5975	0.025921667
2	135.67567	0.007537538	284.3243	0.015795667	315.676	0.017537667	464.3243	0.025795667
3	139.61681	0.00775649	280.3832	0.015576667	319.617	0.017756667	460.3832	0.025576667
4	155.50001	0.00863889	264.5	0.014694667	335.5	0.018638667	444.5	0.024694667
5	157.80673	0.008767041	262.1933	0.014566667	337.807	0.018766667	442.1933	0.024566667
6	166.26136	0.009236743	253.7386	0.014096667	346.261	0.019236667	433.7386	0.024096667
7	168.24797	0.00934711	251.752	0.013986667	348.248	0.019346667	431.752	0.023986667
8	174.85481	0.009714156	245.1452	0.013619667	354.855	0.019713667	425.1452	0.023619667
9	178.37752	0.009909863	241.6225	0.013423667	358.378	0.019909667	421.6225	0.023423667
10	181.01313	0.010056285	238.9869	0.013276667	361.013	0.020056667	418.9869	0.023276667
11	203.87128	0.011326183	216.1287	0.012006667	383.871	0.021326667	396.1287	0.022006667
12	206.0193	0.011445517	213.9807	0.011887667	386.019	0.021445667	393.9807	0.021887667
13	210	0.011666667	300	0.016666667	390	0.021666667	480	0.026666667

Table 4.3: Phase 3 switching angles five level Voltage level 3/9

s/n	0-90	Actual time (s)	90-180	Actual time (s)	180-270	Actual time (s)	279-360	Actual time (s)
1	253.40246	0.014077914	406.5975	0.022588333	433.403	0.02407833	586.5975	0.032588333
2	255.67567	0.014204204	404.3243	0.022462333	435.676	0.02420433	584.3243	0.032462333
3	259.61681	0.014423156	400.3832	0.022243333	439.617	0.02442333	580.3832	0.032243333
4	275.50001	0.015305556	384.5	0.021361333	455.5	0.02530533	564.5	0.031361333
5	277.80673	0.015433707	382.1933	0.021233333	457.807	0.02543333	562.1933	0.031233333
6	286.26136	0.015903409	373.7386	0.020763333	466.261	0.02590333	553.7386	0.030763333
7	288.24797	0.016013776	371.752	0.020653333	468.248	0.02601333	551.752	0.030653333
8	294.85481	0.016380822	365.1452	0.020286333	474.855	0.02638033	545.1452	0.030286333
9	298.37752	0.016576529	361.6225	0.020090333	478.378	0.02657633	541.6225	0.030090333
10	301.01313	0.016722951	358.9869	0.019943333	481.013	0.02672333	538.9869	0.029943333
11	323.87128	0.017992849	336.1287	0.018673333	503.871	0.02799333	516.1287	0.028673333
12	326.0193	0.018112183	333.9807	0.018554333	506.019	0.02811233	513.9807	0.028554333
13	330	0.018333333	420	0.023333333	510	0.02833333	600	0.033333333

4.3 Simulation result

4.3.1 Terminal Voltage

The presented topology terminal voltage waveforms V1 and V2 are shown in Figure 4.1 and 4.2 respectively. Both voltage waveforms look the same as the pattern presented in chapter three. The gating signals also tally with the voltage switching combination presented.

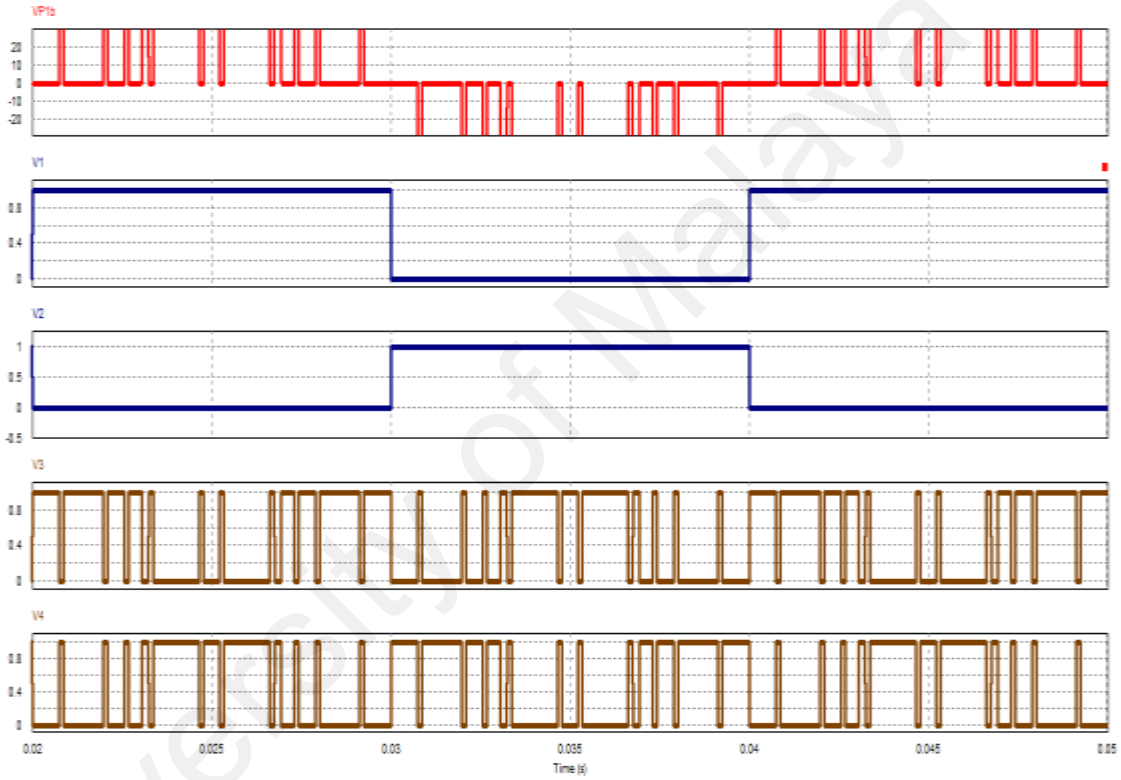

Figure 4.1: Simulated output voltage for module1 (V1).

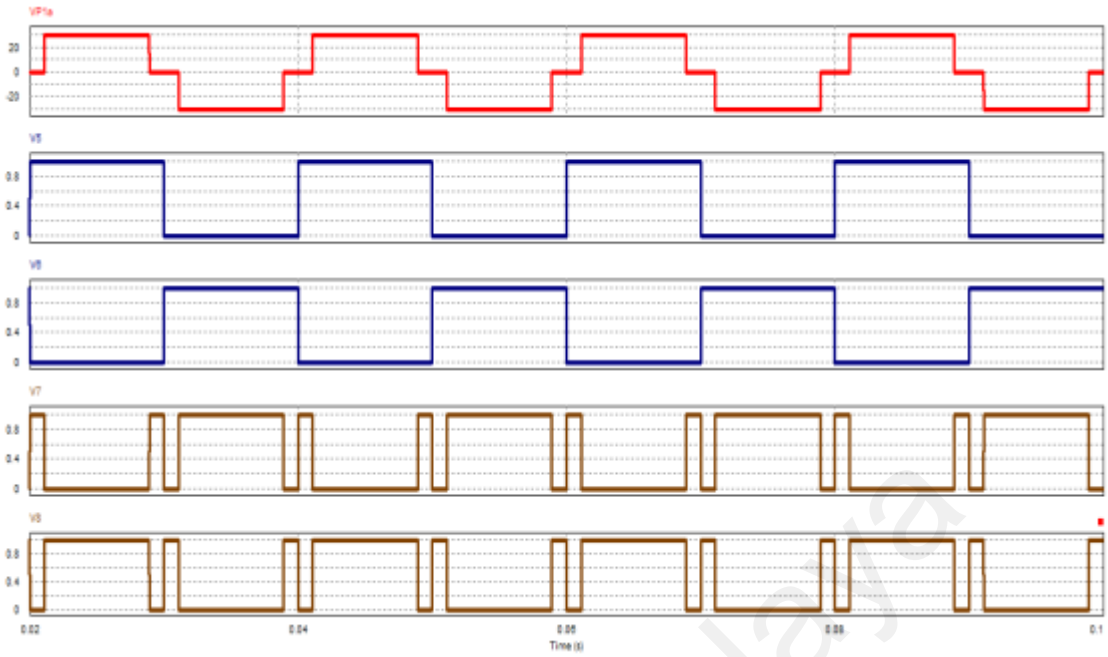

Figure 4.2: Simulated output voltage for bridge module2 (V2).

4.3.2 Summation of the two voltages

Figure 4.3. 4.4 and 4.5 show the summation of the two voltages Vp1a and Vp1b, Vp2a and Vp2b, and Vp3a and Vp3b at the secondary side of two isolation transformers with turn's ratios respectively. It can be seen that the two waves add up to produce a five-level fundamental component that is controlled at certain pre-determined angles per quarter cycle, therefore satisfying the angle distribution

ratio

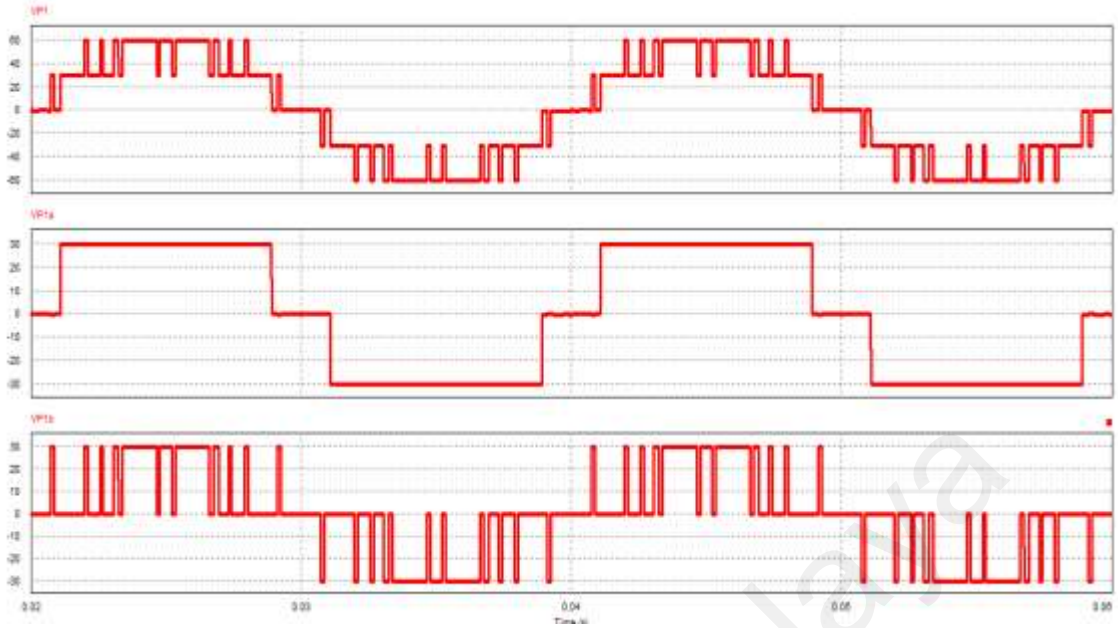

Figure 4.3: Summation of the two-phase voltages Vp_{1a} and $Vp1_b$

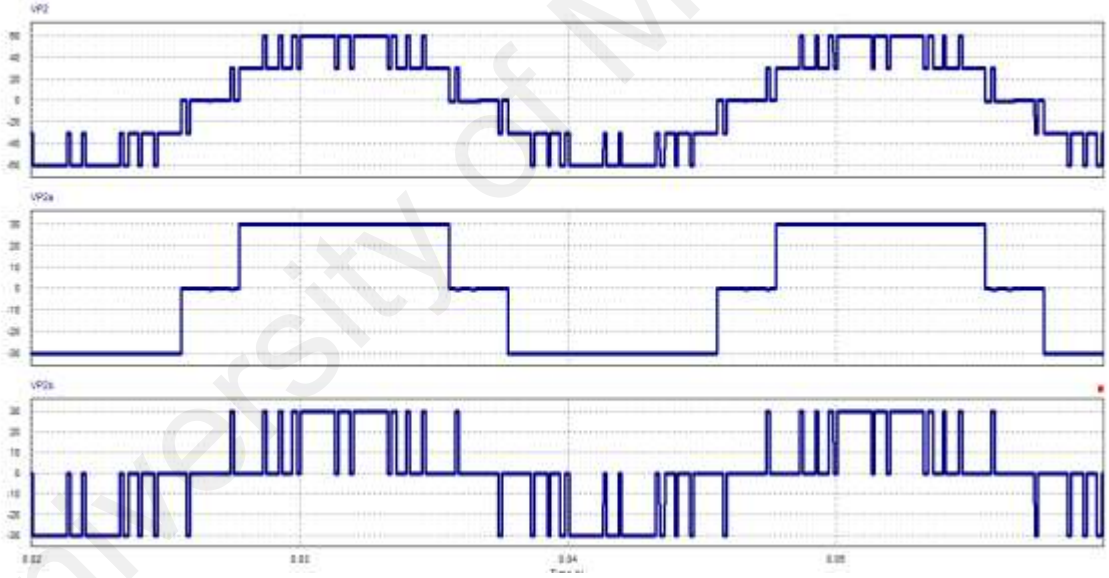

Figure 4.4: Summation of the two-phase voltages Vp2a and $Vp2_b$

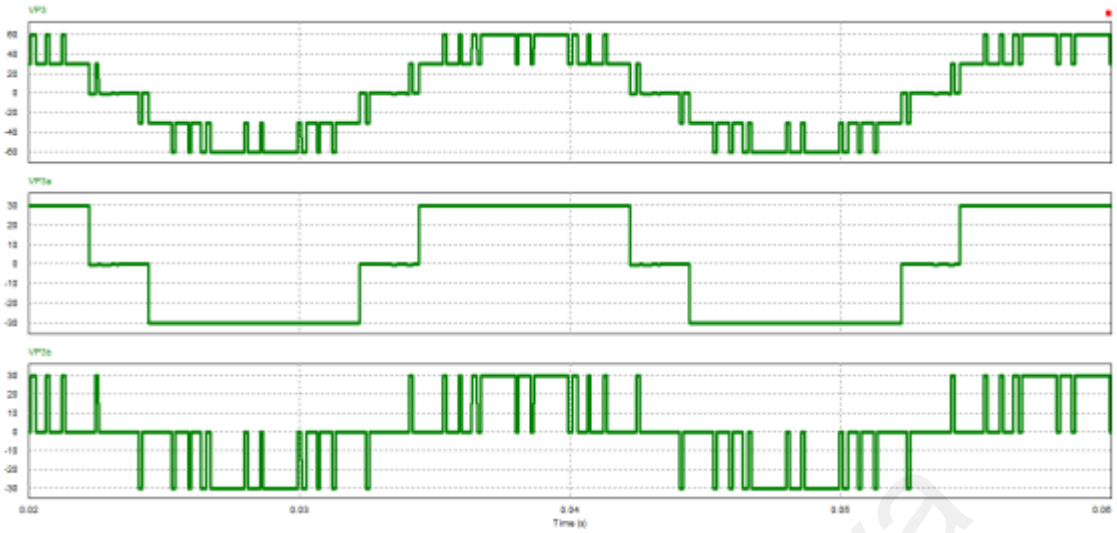

Figure 4.5: Summation of the two-phase voltages Vp3a and Vp3b

4.3.3 Nine level Phase and line Voltages waveforms

Figure 4.6 below shows the voltages VP1, VP2 and VP3 for the phases 1, 2 and 3 respectively whereas figure 4.7 shows the line voltages for the corresponding phases.

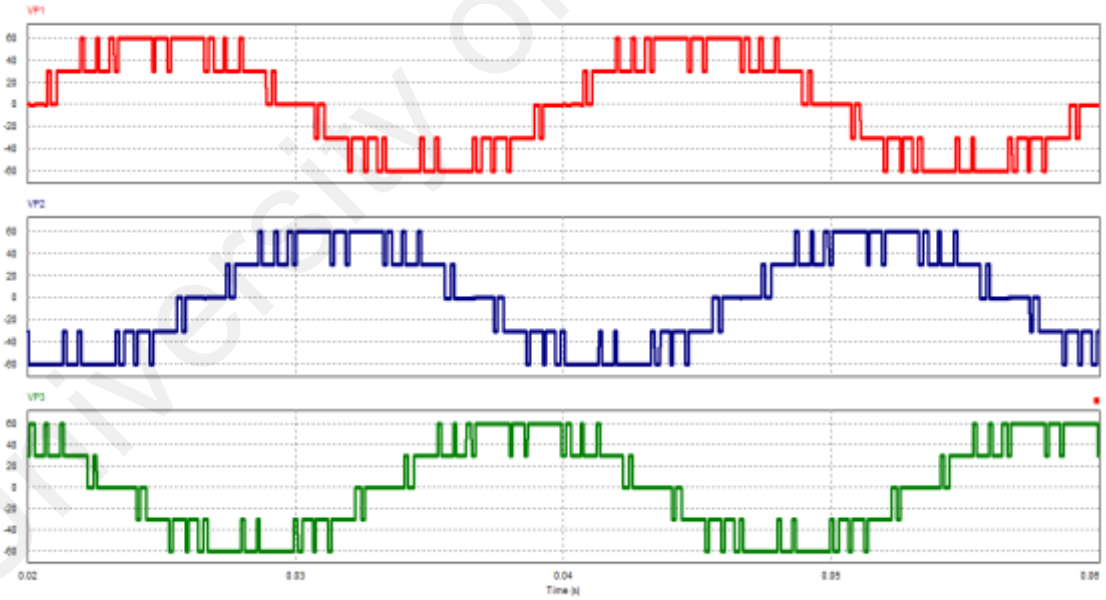

Figure 4.6: phase voltage waveform

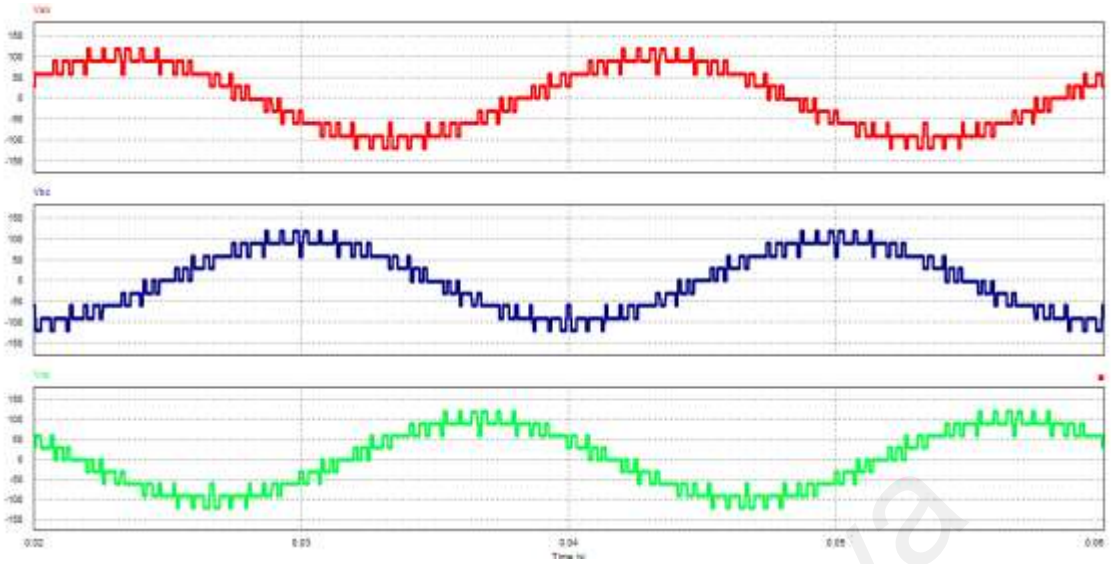

Figure 4.7: line to line voltage waveforms

4.3.4 Proposed topology three phase 9-level waveform

Figure 4.8 below shows the simulated output of the proposed 3-phase waveform

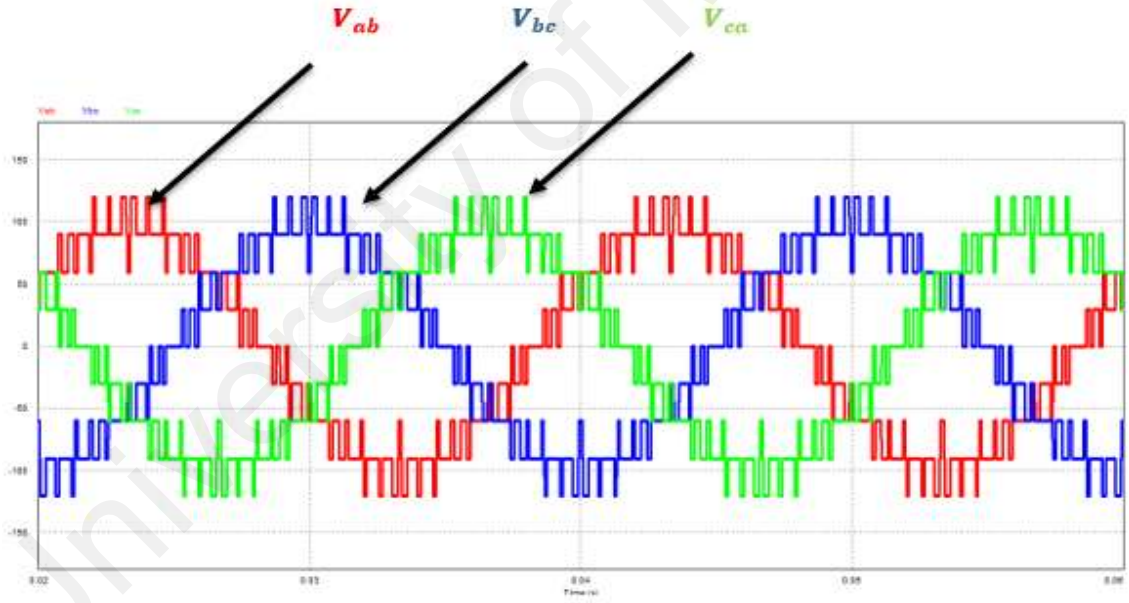

Figure 4.8: proposed topology line voltage waveform

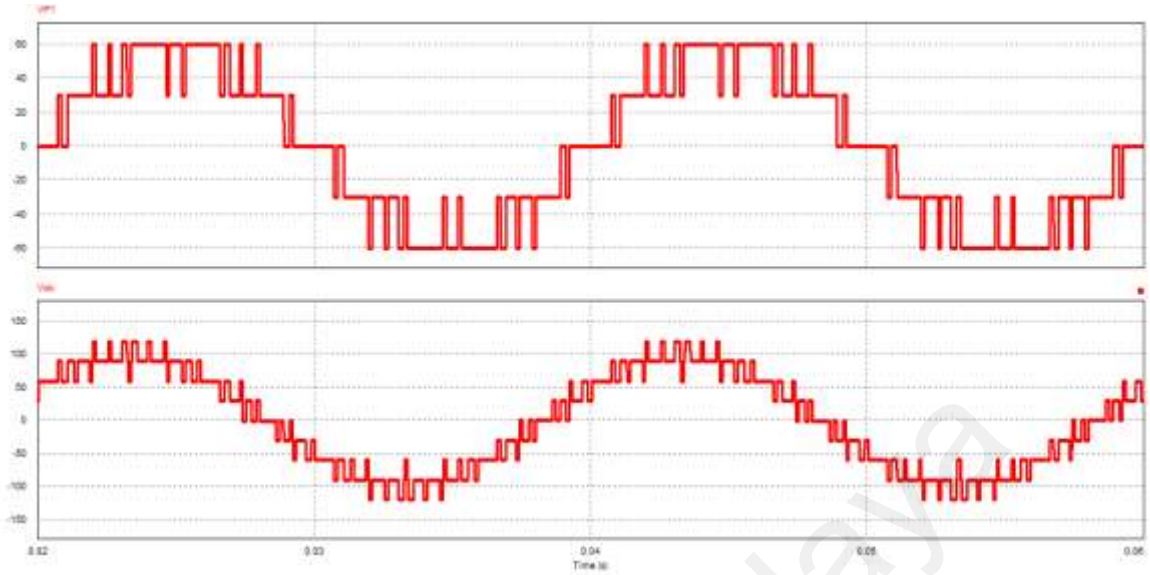

Figure 4.9: Phase and line voltage waveform

Figure 4.9 above shows the proposed topology simulated phase and line terminal voltage waveforms respectively.

To illustrate the difference between the proposed topology waveform and the classical cascaded H-bridge, a nine-level circuit was also simulated, and the waveform is shown in Figure 4.10 below.

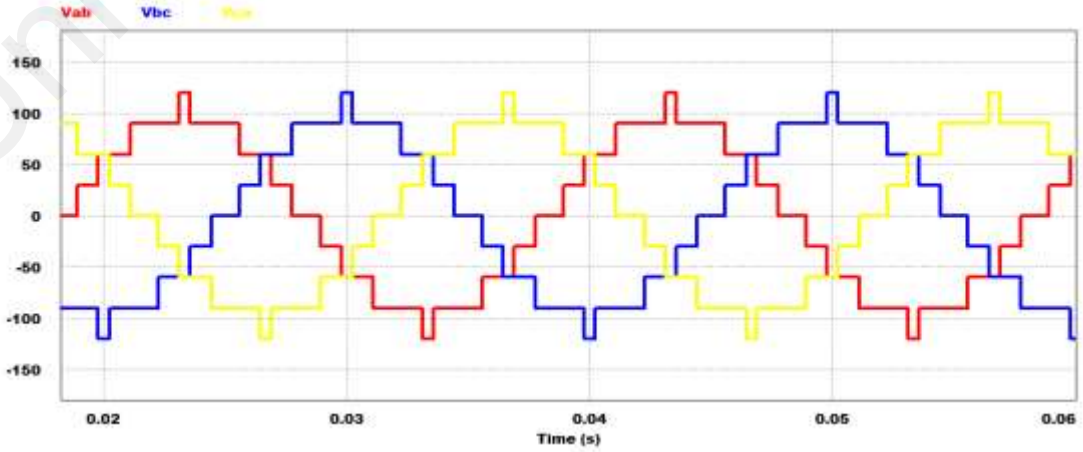

Figure 4.10: conventional CHB topology line voltage waveform

4.3.5 Output voltage Harmonic Contents

Figure 4.11 and 4.12 is the FFT spectrum of the Nine level waveform with 3/9 distribution ratio. From the spectrum of 4.11, it appears that all the 11 non triplen selected lower order harmonics were suppressed or completely eliminated, only the triplen (3^{rd}, 9^{th} etc.) remains. It can as well be seen from 4.12 which is the line-to-line voltage. It can be seen that all the harmonics that lies within the 35^{th} order harmonics are eliminated. Hence, complying with the SHE-theorem of eliminating (N-1) odd non-triplen. Figure 4.13 is the FFT of a conventional nine-level cascaded H-bridge topology. Clearly, the lower order odd harmonics (3^{rd}, 5^{th} ....etc) are only suppressed not eliminated, not as in the case of our proposed topology.

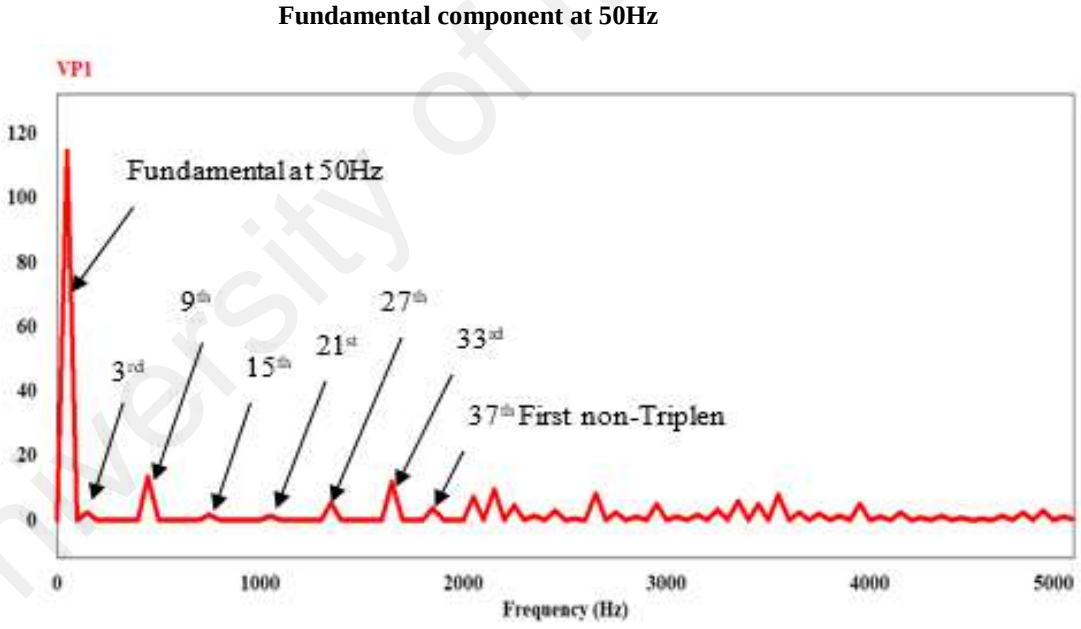

Figure 4.11: FFT of phase voltage for Proposed topology

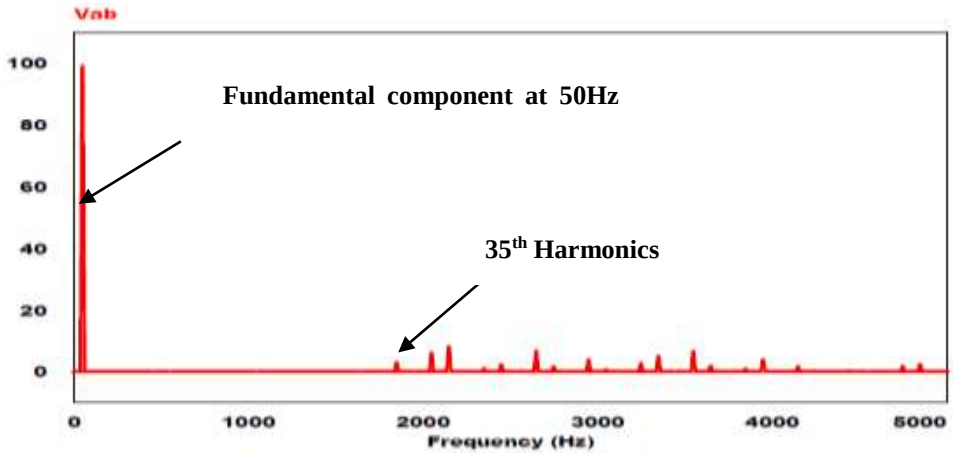

Figure 4.12: FFT of line voltage for proposed

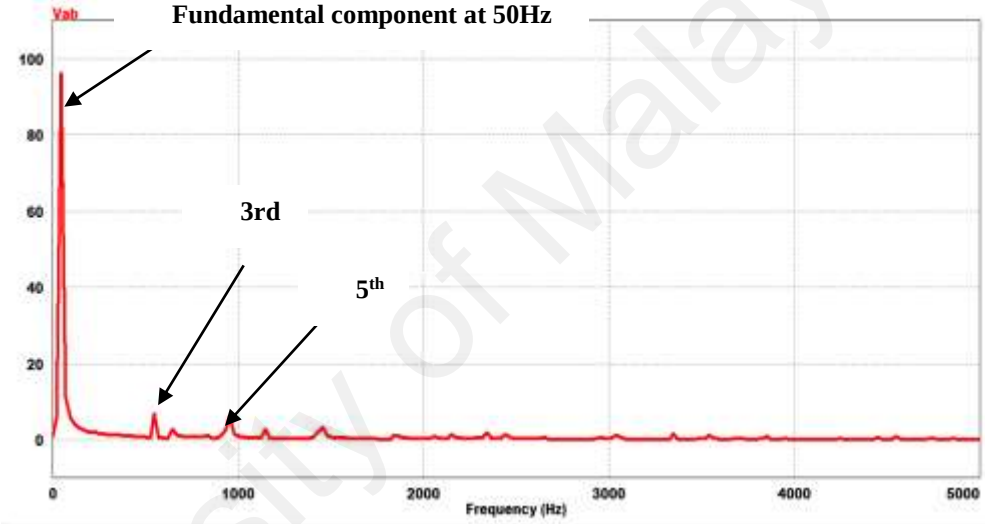

Figure 4.13: FFT for conventional CHB topology line voltage

4.3.6 Finding the Total harmonic distortion THD:

The total harmonic distortion will be evaluated and compared in both the conventional and proposed topology. Using equation 4.1 the exact amount of harmonic distortion present in a signal can only be calculated over an infinite range, which is practically impossible. Therefore, a range of harmonics needs to be specified; first consideration will be made within the range of the eliminated harmonics.

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \times 100 \qquad \text{..... 4.1}$$

In the above equation, V_1 is the fundamental component; V_n is voltage amplitude of the nth order odd harmonic.

The formula in equation 4.1 was programmed in excel to compute the total harmonic distortion level. The circuit is simulated with a number of resistors from 10Ω to 10000kΩ in random step. Based on the plot, it can be deduced that THD increases with increase in load. Which also means the higher the power delivered to the load, the lower the harmonic contents.

Where P is the power delivered to the load, E is the voltage across the load and R_l is the load resistance.

For 3/9 and M= 3.3

Figures 4.14 shows the relationship between the total harmonic distortions considered over the 100th harmonics and the output power of the two nine-level converter topologies. From the plot, the THDs of both converters decrease with increasing output power, especially in the proposed case by looking at its sharp negative gradient. From the graph, the THD of the proposed topology considered within the 100th harmonic has satisfies the IEEE standard of 5%. It is quite low (0.0432%), hence the circuit only requires a small low pass filter. While the conventional topology has a higher value of THD, which is above the minimum allowable distortions. Therefore a filter is needed to meet up the requirement.

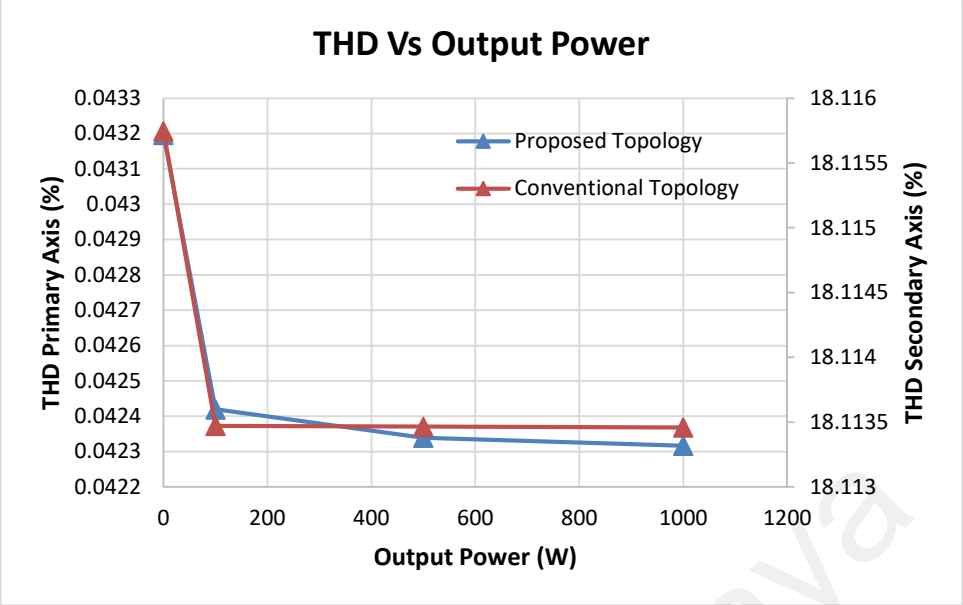

Figure 4.14: THD comparison

Figure 4.15 shows the efficiency comparison plot of the two converters. Both converters dissipate similar behaviors. At minimum or no-load both converters have very poor efficiency. However, efficiency improves and reaches a steady state when the load increases. This finding concludes that the proposed topology has better operational efficiency than the conventional one.

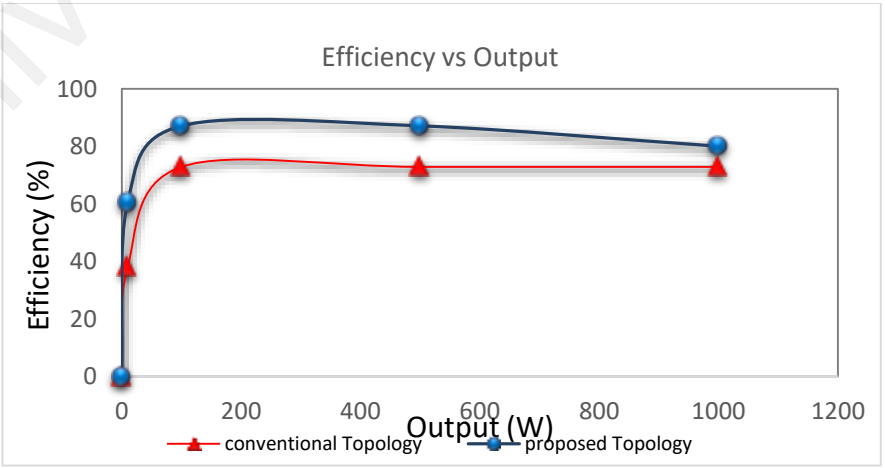

Figure 4.15: Efficiency comparison

CHAPTER 5: CONCLUSION AND RECOMMENDATION

5.1 Conclusion

A multi-level 3-phase nine level converter with (3/9) distribution ratio using cascaded H-bridge topology with a single dc input source and an Isolation transformer has been designed and simulated in this thesis.

The reported converter addresses the issue of using multiple independents dc-link sources to synthesize multi-level output voltage waveforms and it also reduces the number of transformers compared to ordinary conventional multi-level converter generating the same number of voltage levels. These features make the converter to be compact in size, less complex and reduced cost of production and maintenance. The converter was able to eliminate eleven lower order non-triplen harmonics. This shows how SHE can improve the performance of a converter without the need for additional components.

Based on the simulation results obtained for both cases, it appears that SHE has the ability to eliminate selected harmonics by chopping of the fundamental component a number of times at certain pre-determined angles. It, therefore, eliminates harmonics without increased in switching frequency. While for out of range it can be achieved by using a small size low pass filter to further eliminate the higher order harmonics.

Hence, based on the results obtained, it can be concluded that all the aims and objectives have been achieved within the limit of simulation and computational error.

5.2 Future Recommendations

1- The first area of future work is to implement the control algorithm on a digital signal processor DSP. This is to provide a better switching speed.
2- Increasing the converter level by either connecting additional H-bridge module or using transformers with a different turn's ratio.
3- Construct a low pass filter to further improve the converter output, to satisfy the IEEE 5% THD.
4- Distribute the IGBT switching stress by utilizing the redundant switching combinations.

5- Study the converter output harmonic properties using;
   a- A load different from the resistor. i.e. Inductive, capacitive or combination.
   b- Different modulation technique.

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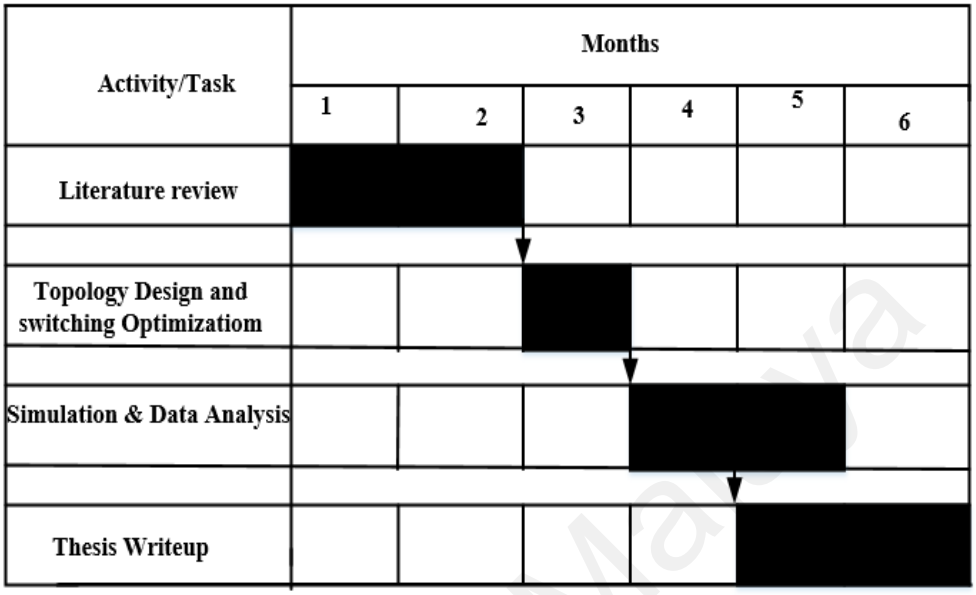
APPENDIX

5.3 Appendix A: Work schedule



Work schedule

5.4 Appendix B: List of items for the project.

S/N	Equipment/Software Tool/Components	Quantity	Estimated Cost (RM)
1.	Matlab/PSIM software	------	Free (Available in Lab)