AN EFFECTIVE ISLANDING DETECTION METHOD FOR PHOTOVOLTAIC GRID CONNECTED INVERTER

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FACULTY OF ENGINEERING
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ABSTRACT

Presently, available international standard related to anti-islanding requirements on medium and low grid connected system required that voltage utility distribution network should be automatically disconnected from the distribution grid when the circuit breaker supplying the feeder connected to the distribution generation trips. Islanding is undesired because it may endanger maintenance service workers and damage load equipment through unsynchronized re-closure. In principle, the main idea of islanding is monitoring the changes in the output parameter of the inverters or other system parameters in indicating islanding.

This thesis presented a low cost and effective passive anti-islanding detection method for single-phase photovoltaic grid-connected inverters. An analog circuit for over/under voltage protection is developed to ensure fast detection and no delay to system. An under-/over frequency circuit is also developed, for accurate and fast frequency detection with minimal external components. A new algorithm is developed in a low cost $PIC18F4550$. An improved disconnection time in the proposed method compared with that in the previously developed method is an attractive solution for single phase grid connected inverters.

The low cost, effective and minimal external component count are the advantages. A prototype is developed and tested to demonstrate the performance and feasibility of the proposed method. The test was conducted on different combination of resistive, capacitive and inductive loads. The experiment results verified that the proposed anti-islanding detection method is able to detect islanding operation effectively under various load types, inverter output powers and quality factors.

ABSTRAK

Standard antarabangsa yang berkaitan dengan syarat anti-pemulauan bagi sistem fasa terhubung grid sederhana dan kecil memerlukan voltan jaringan distribusi dengan automatik terputus daripada grid apabila litar pemutus yang menghubungkan grid dan distribusi generasi telah terbuka.

Fenomena pemulauan adalah tidak diingini kerana ianya boleh membahayakan pekerja semasa proses pembaik pulihan serta boleh menyumbang kepada kerosakan kepada alat. Secara prinsip, konsep utama proses pemulauan adalah untuk mengamati sebarang perubahan pada hasil akhir sesebuah alat penyonsang.

Thesis ini mengkaji dan mengusulkan satu anti-pemulauan pasif yang efektif dan menjimatkan kos untuk mengesan fenomena pemulauan. Litar analog telah dicipta untuk mengawal proses kekurangan atau kelebihan voltan bagi memastikan pengesanan yang pantas tanpa menyumbangkan sebarang kelewatan kepada sistem. Seterusnya adalah litar yang telah dicipta untuk mengawal proses kekurangan atau kelebihan frekuensi bagi memastikan kepersisan dan kelajuan frekuensi deteksi dengan bilangan komponen yang minimal. Algoritma yang diusulkan adalah menggunakan *PIC*184550. Penurunan drastik pada pemutusan masa dalam kaedah yang diusulkan jika dibandingkan dengan kaedah sebelum ini telah menjadi solusi yang menarik bagi sistem penyongsang satu fasa terhubung grid.

Murah, efektif dengan komponen yang minimum adalah kekuatan kepada kaedah ini. Prototaip dibina untuk menguji keupayaan kaedah yang diusul. Eksperimen telah di jalankan pada pelbagai kombinasi beban rintangan, kapasitif dan induktif. Hasil eksperimen membuktikan bahawa kaedah pasif anti-pemulauan yg digunakan mampu mengesan fenomena pemulauan secara efektif dibawah pengaruh beban yang berlainan, kuasa akhir sistem penyongsang dan faktor kualiti.

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LIST OF SYMBOLS

C	Capacitance
f	Grid Frequency
$I_{n,a}$	Negative Sequence Current
L	Inductance
m_f	Modulation Frequency
OV/UV	Over/Under Voltage
OF/UF	Over/Under Frequency
PCC	Point of Common Coupling
Q_f	Quality Factor
R	Resistor
RMS	Root Mean Square
SNR	Signal to Noise Ratio
$THD_{avg,t}$	Average of Total Harmonic Distortion of Phase-A Current
V	Grid Voltage
$V_{avg,t}$	Average Voltage of a Line to Line Voltage
$VU_{avg,t}$	Average Voltage of 3 Phase Voltages
V_{load}	Load Voltage
Vs_{min}	Minimum Pre-Set Voltage Value
Vs_{max}	Maximum Pre-Set Voltage Value
Vs_{maxU}	A Set Point to Detect Islanding with RPS
V_{PCC}	Voltage at Point of Common Coupling
Z_{PCC}	Impedance at Point of Common Coupling
Z_{load}	Impedance of the Load

LIST OF ABBREVIATIONS

AFD	Active Frequency Drift
APS	Active Phase Shift
DG	Distributed Generation
DT	Decision Tree
DFT	Digital Fourier Transformation
DWT	Discrete Wavelet Transform
FES	Fuzzy Expert System
FGNW	Fast Gauss-Newton
IM	Impedance Measurement
IGBT	Insulated Gate Bipolar Transistor
LED	Light-Emitting Diode
LPS	Load Parameter Space
MPPT	Maximum Power Point Tracking
NDZ	None Detection Zone
PI	Proportional Integrator
PV	Photovoltaic
PLL	Phase Locked Loop
PJD	Phase Jump Detection
PWM	Pulse Width Modulation
PMS	Power Mismatch Space
PLCC	Power Line Carrier Communication
R	Receiver
RPS	Real Power Shift

ROCOF	Rate of Change of Frequency
ROCOP	Rate of Change of Power Output
RPEED	Reactive Power Export Error Detection
SFS	Sandia Frequency Shift
SMS	Sliding Mode Frequency Shift
SPD	Signal Produced by Disconnect
SCADA	Supervisory Control and Data Acquisition
T	Transmitter
THD	Total of Harmonics Distortion
UTSP	Unified Three Phase Signal Processor
VSC	Voltage Source Converter

CHAPTER 1

Introduction

1.1 Introduction

Renewable energy has been intensively developed over the past decade. It produces lower pollution than fossil fuels and nuclear generation systems (Yu, Matsui, & Yu, 2010). The new paradigm of distributed generation (DG) thus increases in technical importance and increases profits globally (Chowdhury, Chowdhury, & Crossley, 2009). In principle, DG is a small-scale generation unit installed to the load and connected to the grid, for selling or buying of energy. DG most important consideration is islanding (Yu et al., 2010), which, as specified in (*IEEE Recommended Practice for Utility Interface of Photovoltaic (PV) Systems*, 2000), is the condition when "a portion of utility system that contains both load and distributed resources remains energized while it is isolated from the remainder of the utility system". Such an undesired event could be due to circuit tripping, accidental disconnection of the utility through equipment failure, human error, disconnection for maintenance services, or network reconfiguration (which is uncommon) (Chowdhury et al., 2009; Yu et al., 2010). Integrating DG into utility is a major concern. One problem is that DG may accidentally continue to supply the local load demand when the networks are already isolated from the main system. Successful detection of the islanding is an ongoing challenge to many researchers because existing methods are still not entirely satisfactory (Yip et al., 2010).

Methods of islanding prevention have been studied. Figure 1.1 is a graph of IEEE conferences and journals published on anti-islanding, between 1989 and 2012. From 2002 onwards, it shows that there are an increased of interest on islanding detection.

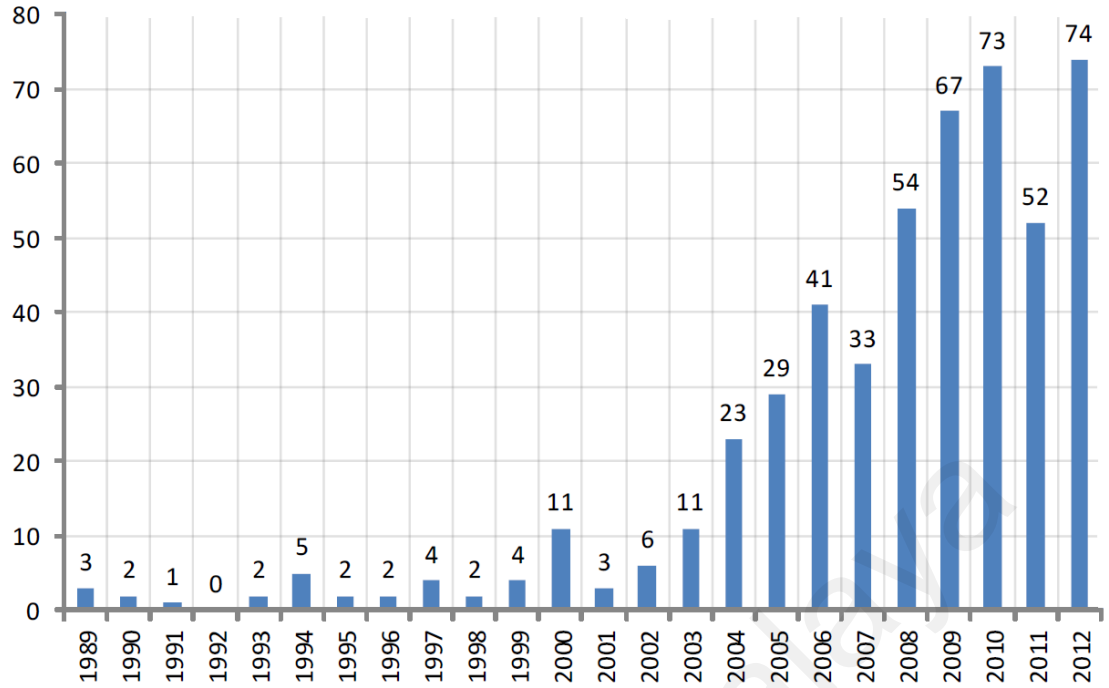


Figure 1.1: Papers related to anti-islanding, 1989-2012

The 1989-2012 conferences and journals present two types of anti islanding methods: local, or remote. The local methods are either passive or active as shown in Figure 1.2.

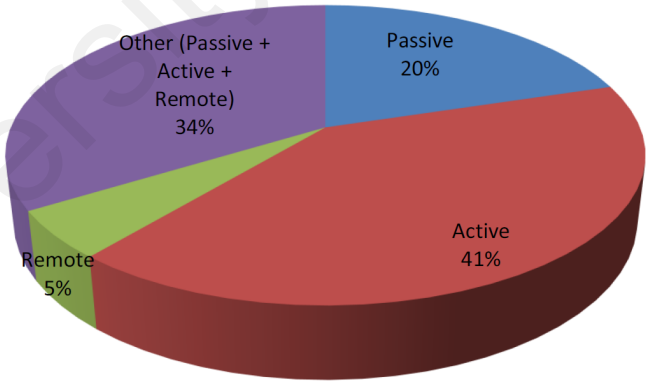


Figure 1.2: Types of islanding detection, 1989-2012

Passive islanding detection relies on changes to electrical parameters to determine whether islanding had occurred (Chiang, Jou, Wu, Wu, & Feng, 2010). These methods were the first to be developed. As technology progressed, more papers discussed active methods, whose development aimed to overcome the limits of passive methods. Remote methods are more reliable but are neither more cost-effective nor simpler to implement

than passive or active methods (Kunte & Wenzhong, 2008). Chapter 3 gives examples of passive, active, and remote detection methods. They each have advantages and drawbacks when applied.

High demand for the "perfect" method led to much research on wavelet-based islanding detection. Wavelet-based method detects islanding through local measurements of PCC voltage and current signals, just as in passive methods. It is able to evaluate the high-frequency components injected by inverter, just as in active methods (Pigazo, Moreno, Liserre, & Dell'Aquila, 2007). Its main advantage is its sensitivity to signal irregularities such as those in islanding condition (Ray, Kishor, & Mohanty, 2010).

Two factors in understanding of anti-islanding requirements are: the established standards for grid-connected systems (which address issues of islanding and the procedure for testing and qualifying a DG system) (Chiang et al., 2010), and NDZ (the zone in which an islanding detection method would fail to operate on time, and an evaluating criterium for islanding detection methods).

This thesis proposes a low cost and effective passive islanding detection method for single-phase photovoltaic grid-connected inverters. An analog circuit for over/under voltage protection was developed to precisely ensure a very fast detection without adding any delay to the system. An under/over frequency circuit was also developed, for accurate and fast frequency detection with minimal external components. A new algorithm was developed in a low-cost PIC18F4550, integrating the circuits with the existing inverter control system. The drastically improved disconnection time in the proposed method compared with that in the previously developed method is an attractive solution for single phase grid connected inverters. The low cost, effective and minimal external component count are the proposed method's advantages. A prototype was developed and tested to demonstrate the performance and feasibility of the proposed method. The experiment results verified that the proposed islanding detection method able to detect islanding operation effectively

under various load types, inverter output powers and quality factors.

1.2 Research Objectives

The objectives of this work are:

a) To develop new hardware prototype design of the under/over voltage circuit and under/over frequency circuit.

b) To develop the islanding control method and the algorithm using PIC18F4550.

c) To calculate the frequency values and control the voltage and frequency limitation of the single phase grid connected PV inverter.

d) To verify the proposed method with islanding test under different RLC load with different quality factors and inverter output powers.

e) To implement the proposed passive islanding method in the single phase grid connected PV inverter and further reduce disconnection time between inverter and the grid.

1.3 Thesis Structure

Chapter 2 describes the types of PV system, solar PV cell, PV output characteristics, PV advantages and disadvantages, inverter for PV system and single phase grid connected inverters.

Chapter 3 presents a literature review on anti-islanding standards, none detection zone, islanding detection methods which include passive islanding, active islanding and remote techniques. This chapter also describes the principle of detection method and wavelet as a new approach for islanding detection.

Chapter 4 presents the hardware and software development and implementation, which comprises of hardware and software configuration of the proposed low cost passive

method for islanding detection of single phase grid connected PV inverter (the under/over voltage circuit and under/over frequency circuits). The proposed islanding control algorithm is implemented in PIC18F4550.

Chapter 5 presents the simulation and experiment results for the proposed passive islanding method under various load types, inverter output powers and quality factors. This chapter also provides a comparison between the proposed and the past method that has been implemented before in the single phase grid connected PV inverter. The comparison table that summarizes disconnection times between the two methods is also provided.

Chapter 6 concludes with a summary, a listing of the author's contributions and recommendations for possible future work.

CHAPTER 2

PV Generation System and Grid-Connected PV Inverters

2.1 Introduction

Nowadays photovoltaic and solar thermal systems are the most common technologies for utilising solar energy. One of the important factors for an economically practical performance of solar energy systems is the availability of solar energy on ground surface that can be transformed into heat or electricity (other than operation costs, installation costs and lifetime of system components) (Angelis-Dimakis et al., 2011).

Photovoltaic conversion use solar panels to convert sunlight into electricity without any interference from heat engine. The biggest benefits of the photovoltaic devices are their construction as stand-alone systems to give outputs from microwatts to megawatts and simple to design requiring very little maintenance. For this reason, they are used for power source, water pumping, remote buildings, solar home systems, communications, satellites and space vehicles, weather instrument, and for even megawatt scale power plants. With such a huge range of applications, the request for photovoltaic is rising every year (Parida, Iniyan, & Goic, 2011).

This chapter presents types of PV system, solar PV cell, PV output characteristic, advantages and disadvantages of PV system, inverter for PV system and single phase grid connected inverters.

2.2 Types of PV System

Photovoltaic systems are grouped according to their component configurations, the connection of the equipment to other power sources and electrical loads and their functional and operational requirements. The two main classifications are grid-connected and

stand-alone systems (See Figure 2.1). Photovoltaic systems can be designed to supply DC and/or AC supply, can be connected with other energy sources and energy storage systems and can operate interconnected with or without the grid.

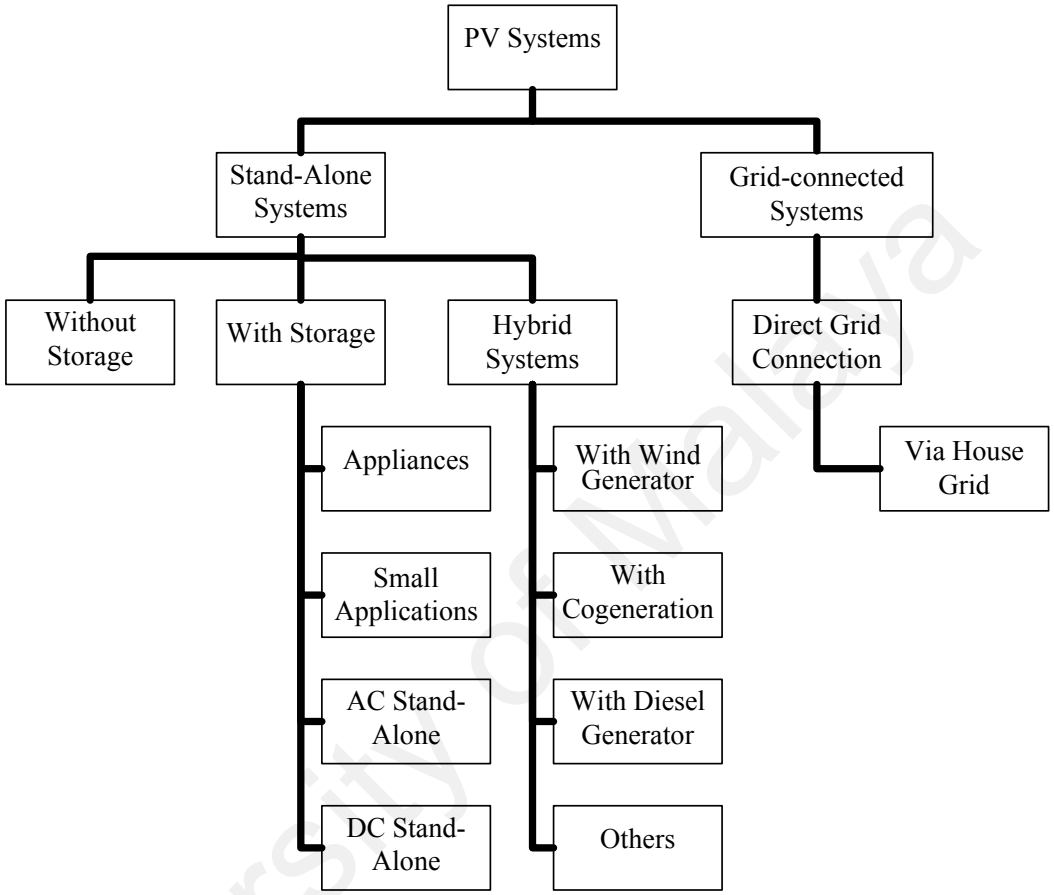


Figure 2.1: PV system configurations

The stand-alone or off-grid systems generate power independently of the utility grid. Generally stand-alone is sized and designed to supply certain DC and/or AC electrical loads throughout the day with no additional supplement source. This system may or may not use energy storage as a backup system. The simplest form of a stand-alone solar system is a direct-coupled system where the DC output of a solar panel is directly connected to a DC load as in Figure 2.2. In direct-coupled systems, there is no electrical energy storage (batteries), the load only operates during daylight hours, making these designs appropriate for regular applications such as water pumps, ventilation fans and small cir-

culation pumps for solar thermal water heating systems. The crucial part of designing well-performing direct-coupled system is matching the impedance of the electrical load with the maximum power output of the PV array. For certain loads, a maximum power point tracker (MPPT) (a type of electronic DC-DC converter) is used between the array and load to better utilize the available array maximum power output. Most of stand-alone PV systems used batteries for energy storage. Stand-alone are suitable for locations where the grid cannot break through and there is no other source of energy (See Figure 2.3). Stand-alone systems are the most cost-effective choice for applications far from the grid; hence they control the majority of photovoltaic installations in remote regions of the world. Examples are remote stations and lighthouses, military applications or auxiliary power units for emergency services and manufacturing facilities using delicate electronics. The disadvantages of stand-alone systems are the excess battery costs, finite capacity and low capacity factor to keep electricity forcing to throw away the extra energy produced (Kaundinya, Balachandra, & Ravindranath, 2009).

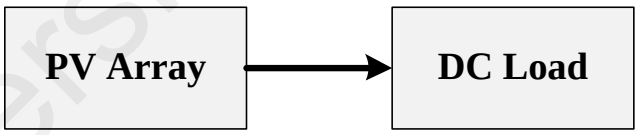


Figure 2.2: Direct coupled PV system (www.fsec.ucf.edu)

Grid-connected PV systems (utility-interactive) are designed to function in parallel with the electricity distribution system. The main unit in grid-connected PV systems is the inverter or power conditioning unit (PCU). The inverter converts the DC power from the solar array into AC power (following the voltage and power quality requirements of the utility grid), and when the utility grid is disconnected, it will automatically stops supplying power to the grid. At night and during other periods when the electrical loads are larger than the PV system output, the balance of power needed by the loads is received

from the grid. This safety feature is a must in all grid-connected PV systems to ensure that the PV system will not continue to function and feed back into the utility grid when the grid is disconnected for service or repair as in Figure 2.4.

The term hybrid energy system (HES) is a stand-alone energy system, which combines renewable and conventional energy sources with lead-acid batteries for power conditioning equipment, chemical storage and a controller. The controller and power conditioning units are used to sustain the grid quality power (Nema, Nema, & Rangnekar, 2009). In this type of system, the battery bank is firstly recharged by the solar system and when insufficient, the generator takes place (See Figure 2.5).

The flexibility of PV allows applications in sizes starting from a few watts to several megawatts. PV systems are categorized as follows (based on the power output rating):

1. Very small systems (< 5W) with or without energy storage, mainly for electronics user.

2. Small systems (5W- 1 kW) with or without energy storage, for cathodic protection of pipelines, navigational aids and signalling, remote communication systems, desalinization systems, micro irrigation and remote instrument packages.

3. Kilowatt-size systems (1 kW to a few 10s of kW) with or without energy storage for single family residences, rural power systems, purification systems, water pumping and for remote security applications. These systems can be either stand-alone or grid-connected.

4. Intermediate-scale systems (10s of kW to 100s of kW), mostly worked with grid support. For example, distribution system support and remote transmitters.

5. Large-scale systems (1 MW or larger) connected to utility grids mainly for industrial, grid power generation and commercial (Ramakumar & Bigger, 1993)

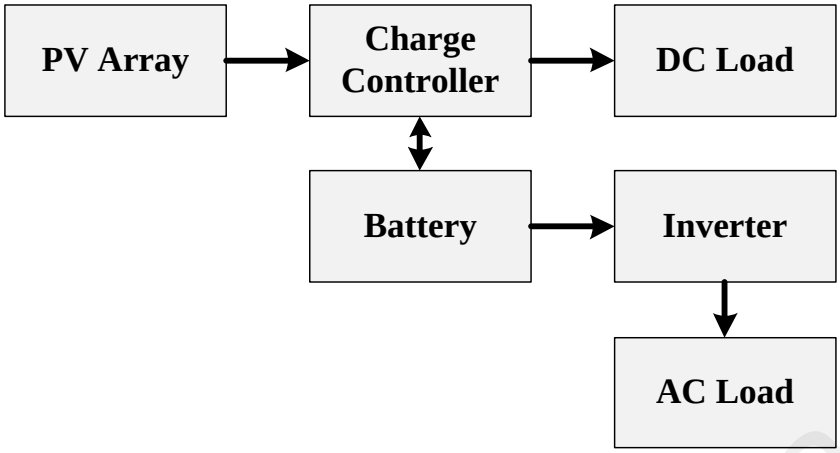


Figure 2.3: Diagram of stand-alone PV system with battery storage powering DC and AC loads (www.fsec.ucf.edu)

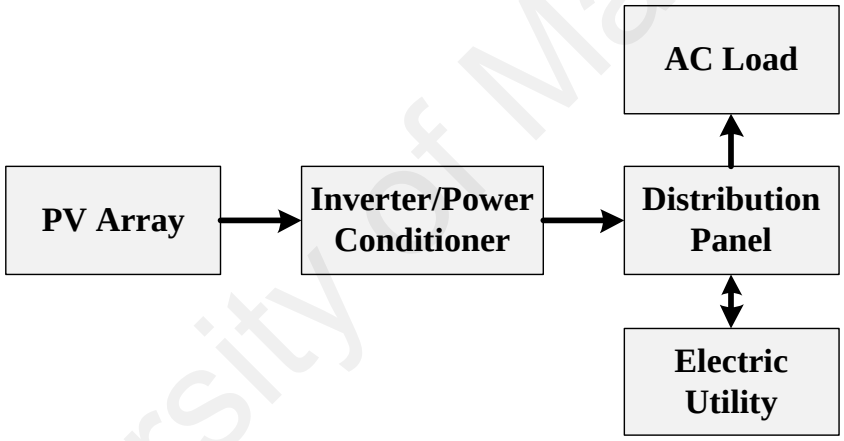


Figure 2.4: Diagram of grid-connected photovoltaic system (www.fsec.ucf.edu)

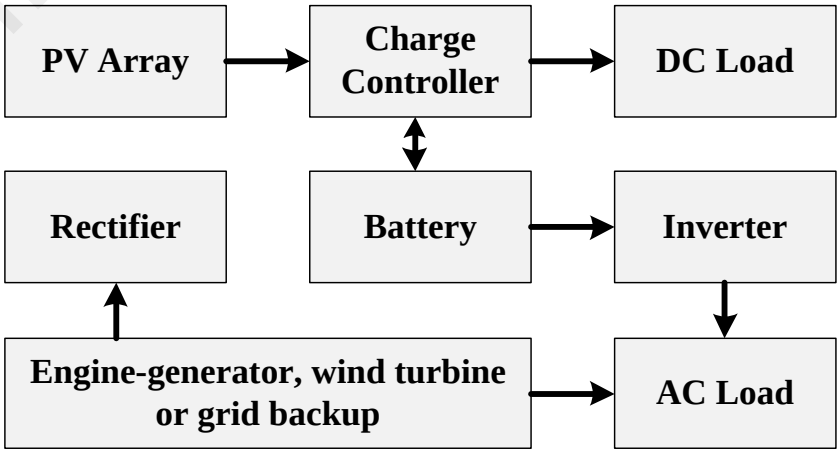


Figure 2.5: Schematic diagram of a hybrid PV system incorporating a PV array and additional power supply backup (www.fsec.ucf.edu)

2.3 Solar PV Cell

A solar cell is a tool producing electrical energy directly from solar energy. The basic tool requirement of a solar cell is an electronic asymmetry, such as a p-n junction. When illuminated, photo generated electron-hole pairs (EHP) are produced all over the solar cell. If the cell is connected to a load, current will flow from one region of the cell, through the load, and back to the other region of the cell (Lee, Chen, Allen, Rohatgi, & Arya, 1995).

Figure 2.6 shows the work flow of a PV cell. When solar cell exposed to light, the cell produces charge carrier known as electrons and holes. The internal field generated by junction separates some of positive charges (holes) from negative charges (electrons). Holes are swept into positive (p-layer) and electrons are swept into negative (n-layer). An external circuit provides the necessary path for free electrons to pass through the load to recombine with positive holes. Hence under illumination, current is formed from the cells.

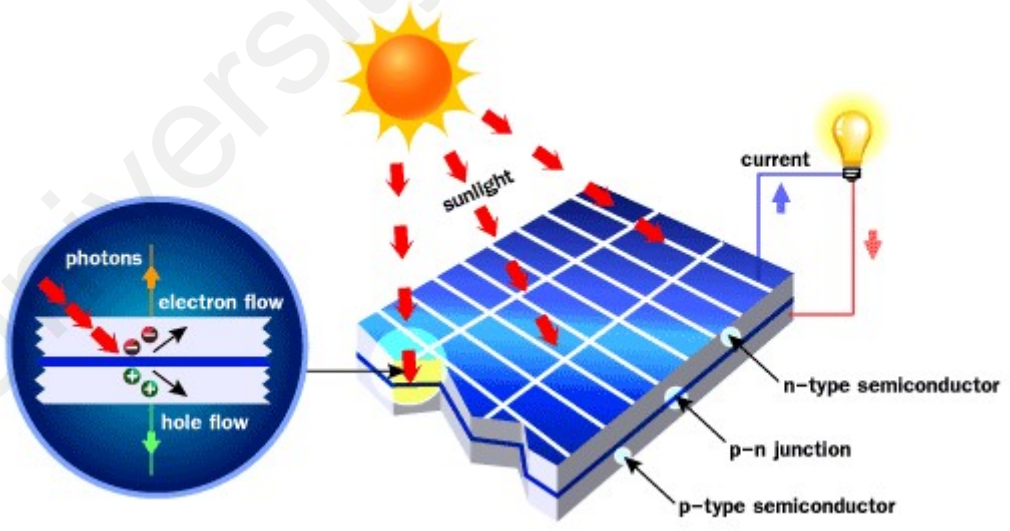


Figure 2.6: Work flow of a PV cell (www.pvsolarchina.com)

As shown in Figure 2.7 in order to produce higher currents, voltages and power levels, photovoltaic cells are connected electrically in series and/or parallel circuits. Photovoltaic modules are the essential structure blocks of PV systems and consist of PV cell

circuits sealed in an environmentally protective laminate. Photovoltaic panels consist of one or more PV modules combined together. A photovoltaic array is known as the complete power-generating unit, consisting of any number of PV modules and panels. Based on current or voltage requirement, PV arrays are connected in a lot of ways: If the PV arrays are connected in parallel, the output current will increase. If the PV arrays are connected in series, the output voltage will increase.

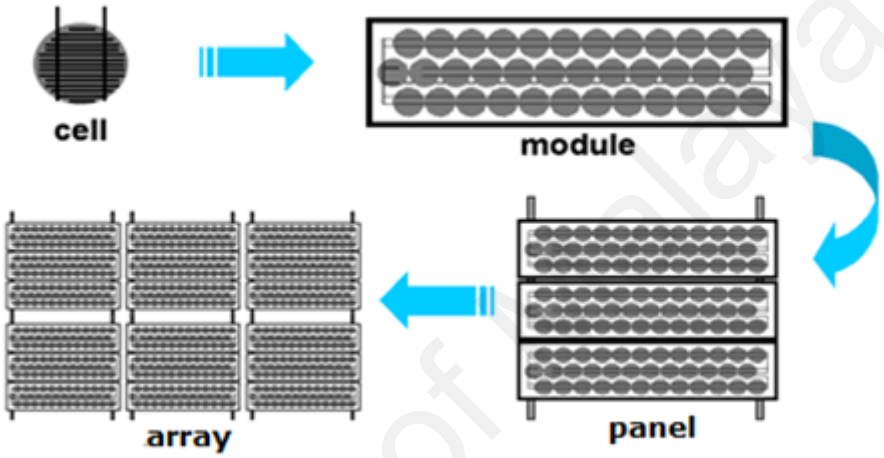


Figure 2.7: Transformation process from a single cell into an array (www.fsec.ucf.edu)

There are a lot of types of solar cells available on the market. All of them have the same electric current generation principles, but different approaches used to produce the structures in order to reduce the cost of production. All of these approaches involve a trade-off between lower manufacturing costs versus lower efficiency in conversion process. Based on the manufacturing technology and the semiconductor, there are four major cell types:

- Monocrystalline Silicon – This type of solar cell uses a single layer of silicon. It is highly efficient (15-18%) but the most expensive because of the long, expensive process of creating silicon crystals and the high grade of silicon used.

- Polycrystalline Silicon – Liquid silicon is poured into blocks that are subsequently sawed into plates, producing polycrystalline silicon cells. This method produces

some degree of degradation to the silicon crystals which make them less efficient (12-14%). However, it is easier and cheaper to manufacture (Rath, 2003).

- Amorphous Silicon – Since Amorphous silicon (a-Si) PV module or thin-film silicon PV module absorbs light more effectively than crystalline silicon PV module, it can be made thinner. It is suitable for any applications that low cost is important and high efficiency is not required. The typical efficiency of amorphous silicon PV module is around 6%.

- Hybrid Silicon PV Module: A mixture of single crystalline silicon with thin layers of amorphous silicon gives better sensitivity to indirect light or lower light levels. The Hybrid silicon PV module has highest level of conversion efficiency which is about 17%.

Even though there are differences in manufacturing cost and efficiency, each type of solar cell has its own advantages compared to another over its application suitability. Other way of looking at solar cells is in terms of the types of materials they are made of. Silicon is the most regularly used semiconductor, but a number of other materials can be used as well. These include copper gallium indium diselenide (CIGS), and cadmium telluride materials. Efficiencies between of 18% - 24% have been achieved in the current generation of solar cells. However major advances in efficiency have also been made on the new cells (more than 20% efficiency) and some laboratory prototypes are getting as high as 30% efficiency. A lot of exciting and promising possibilities are emerging on new PV cells with high potential for lower cost and moderate efficiencies (Deb, 2000).

2.4 PV Output Characteristics

The energy conversion capability at the existing conditions of temperature and irradiance (light level) is described through the I-V (current-voltage) curve of a PV string

(or module). Theoretically, the curve is the combinations of current and voltage at which the string could be 'loaded' or operated (if the irradiance and cell temperature could be held constant). Figure 2.8 shows a typical I-V curve, the power-voltage or P-V curve, and main points on these curves (Nguyen, 2008).

Based on Figure 2.8, the span of the I-V curve ranges from the short circuit current (I_{sc}) at zero volts, to zero current at the open circuit voltage (V_{oc}). The maximum power point (I_{mp}, V_{mp}) (at the 'knee' of a normal I-V curve) is the point where the array produces maximum electrical power. In a PV system, the job of the inverter is to continuously change the load in order to hunt the specific point on the I-V curve at which the array as a whole generates the maximum DC power.

At voltages below V_{mp}, the flow of electrical charge (solar-generated) to the external load is relatively free of output voltage. This behavior starts to change near the knee of the curve. As the voltage further increase, there will be an increasing percentage of the charges recombine within the solar cells rather than flowing out through the load. At V_{oc}, all of the charges recombine internally. The (I,V) point at which the product of current and voltage reaches its maximum value is called the maximum power point (located at the knee of the curve) (Corporation, March 1, 2011).

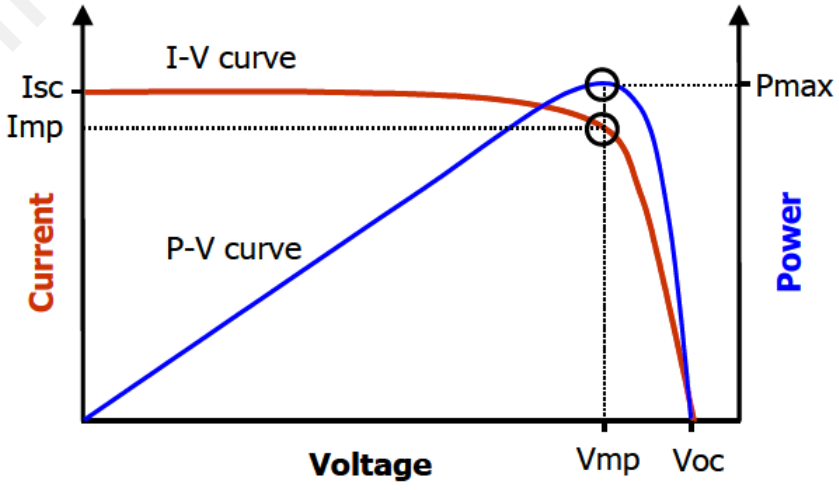


Figure 2.8: The I-V and P-V curves of a photovoltaic device. The P-V curve is calculated from the measured I-V curve

Figure 2.9 (Kyocera, 2008) shows output current I influenced by change in insulation S, while output voltage V is almost constant. In contrast, for changes in temperature, voltage seems to vary widely but current is constant (See Figure 2.10) (Kyocera, 2008).

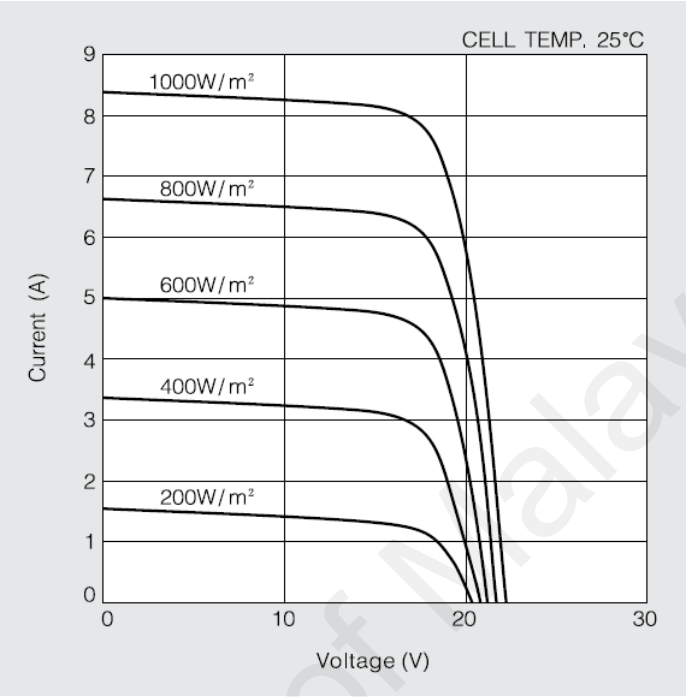


Figure 2.9: I-V characteristics of a PV cell array for various values of irradiance S at 25^{o}C, for KD135GX-LPU (Kyocera, 2008)

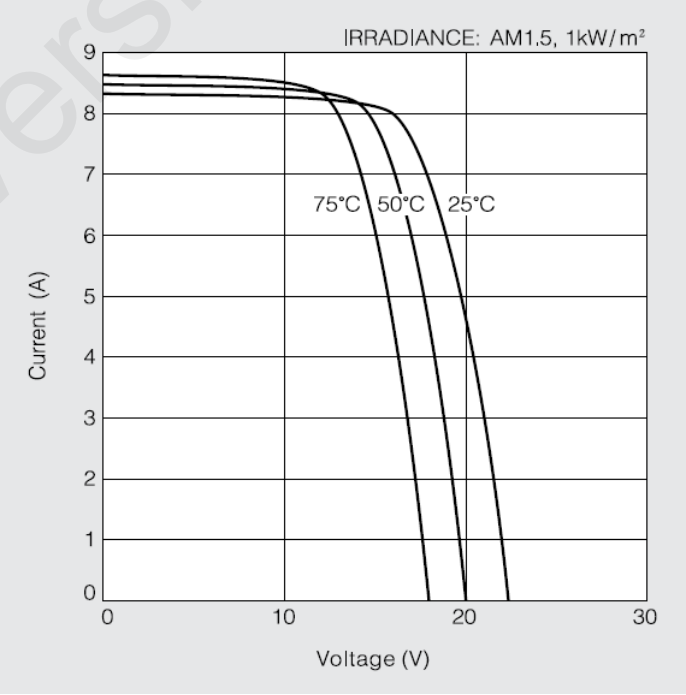


Figure 2.10: I-V characteristics of a PV Cell array for various values of temperature T at 1000W/m^2 irradiance, for KD135GX-LPU (Kyocera, 2008)

2.5 PV Advantages and Disadvantages

The non-existence of recurring fuel costs; and uncertainty of escalation in conventional fuel costs makes the renewable technologies increasingly attractive. PV has demonstrated low operation and maintenance (O&M) costs as compared to many conventional technologies. Photovoltaic systems have a lot of advantages compared to conventional power-generating technologies. PV systems can be used for either centralized or distributed power generation, and can be designed for a lot of applications and operational requirements. PV systems are modular, have no moving parts, easily expandable and even transportable in some cases. The attractive qualities of PV systems are the environmental compatibility, energy independence, free fuel (sunlight), and no noise or pollution is formed from operating PV systems. Generally, PV systems that are well designed and properly installed have long service lifetimes and require very minimal maintenance. Nowadays, the disadvantage for the technology is the high cost of PV modules and equipment (as compared to conventional energy sources). Thus, the economic value of PV systems is realized over many years. The surface area requirements for PV arrays may be a limiting factor for some of the cases. Surface area requirements for PV array installations are from 8 to 12 m^2 (86 to 129 ft^2) per kilowatt of installed peak array capacity. This is because of the diffuse nature of sunlight and the existing sunlight to electrical energy conversion efficiencies of photovoltaic devices.

2.6 Inverter for PV system

The core component in a grid connected PV system is the inverter (Calais, Agelidis, & Meinhardt, 1999) which transforms into AC power (following the requirements of grid voltage and grid power quality) from DC power produced by the PV array. A standard grid connected PV inverter has MPPT and current control algorithms to ensure a successful power delivery from the PV system to the utility grid (Krismadinata, 2012).

Normally, the grid system is known as AC voltage source of infinite capacity, while the output of grid-connected inverter system can be controlled as voltage or current source. For the case of PV grid-connected inverter system designed as a current-source system, grid-connected system is actually a parallel connection of AC current source and voltage source. The output power factor can be assured one by controlling the phase synchronization between grid voltage and current of the grid-connected inverter system. Meanwhile, for the case of the output of the grid-connected inverter system controlled as a VAC, the PV grid-connected system and the grid are actually two AC voltage sources in parallel operation. At the same time, to guarantee stable operation of the grid-connected inverter system, the amplitudes and the phases of the output voltage of the inverter must be strictly controlled. Because of the slow response of phase-locked loop and difficulty in controlling the output voltage, circumfluence may occur between the utility and the grid-connected inverter system, resulting to unstable running or even failure of the system. The control mode of voltage source input, and current source output is used in the design of photovoltaic grid-connected inverter (Zhou, Tong, Mao, & Gao, 2010). Generally, an inverter has to fulfil these functions in order to inject energy from a PV array into the utility grid:

1. generates sinusoidal current waveform
2. low total harmonic distortion
3. regulated voltage as specify by power utility: single phase $230 \pm 10\%$; three phase $415 \pm 10\%$
4. synchronised with line frequency $50Hz \pm 2\%$
5. Operates at near unity power factor.

The way these functions are sequenced within an inverter design determines the choice of semiconductors and passive components and therefore their losses, sizes and prices (Calais, Myrzik, Spooner, & Agelidis, 2002). In principal, a step up converter boosts the PV array's generated voltage to a suitable and fixed high level DC voltage. PV Array voltages changes with weather, but constant DC bus voltage is controlled by the converter's controller. The high DC bus voltage is converted to AC by a bridge inverter's circuit (See Figure 2.12). This bridge generates sinusoidal current. A grid connected inverter comprises of bridge inverters which consist of semiconductor switches that control pulse width in creating the sine wave. The common types of semiconductor switches used are (Krismadinata, 2012):

1. MOSFET – Metal Oxide Semiconductor Field Effect Transistors. These switches can be switched at very high frequency but it is not stable enough for bigger power inverters. The typical handling power is less that 1kW power.

2. IGBT – Insulated Gate Bipolar Transistor. This switch is being used in almost all grid connected inverters with the exceeding 1kW of power.

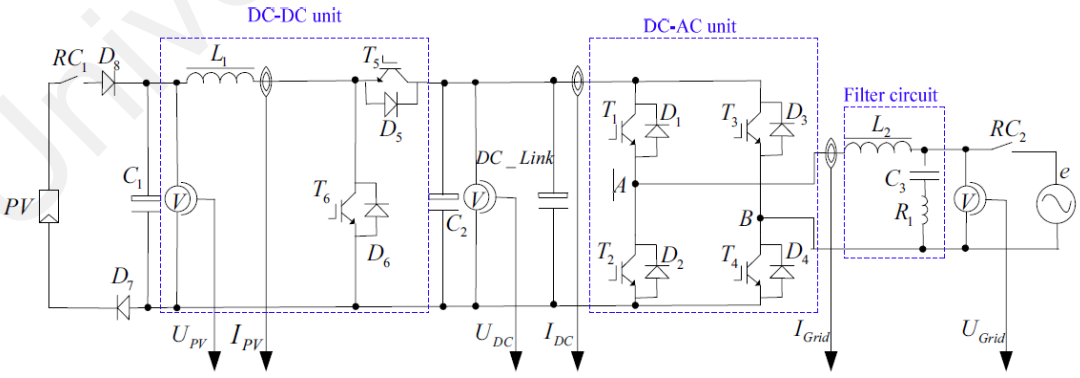


Figure 2.11: General main circuit block diagram (Zhou, et al., 2010)

Rapid switching for creating sine waves caused interference thus required filtering in order to comply with the electromagnetic- interference guidelines of many countries.

The main circuit block diagram of the PV grid-connected system is shown in Figure 2.11 which includes:

1. DC-DC unit: It is used to achieve boost and Maximum Power Point Tracking (MPPT). Boost-chopper is used to increase the output voltage of the PV array to 400V. MPPT (to guarantee that solar panels always operate at maximum power point) has to control the solar cell operating voltage by regulating the duty cycle of the boost based on the V-I characteristics of solar cells.

2. DC-AC unit: The full-bridge topology is used and the power factor is assured one by controlling the output current of the unit to be in phase with the grid voltage.

3. Filter circuit: AC-side filter is adopted to filter AC side current harmonics to guarantee the quality of grid current (Zhou et al., 2010).

2.7 Single phase grid connected inverters

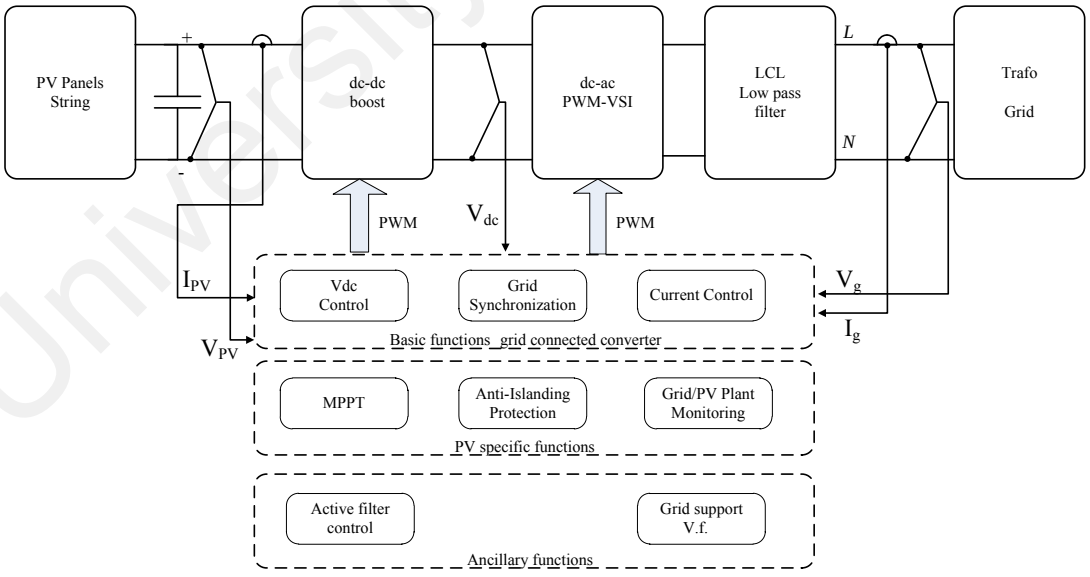


Figure 2.12: Block diagram of a single-phase grid connected PV inverter

Block diagram of the single-phase grid connected PV inverter used in this project is shown in Figure 2.12. The single phase grid connected inverter consists of PV Arrays,

DC-DC boost converter connected to two capacitors in series which functions as maximum power point (MPP) tracker, four switching devices (illustrated as ideal switches) connected in the form of a full bridge configuration (S1-S4), filter inductor (L_f) which used to filter the current injected to the grid. The power generated by the system is delivered directly to the grid. Since voltage of the grid is uncontrollable, the simplest way of controlling the operation system is through controlling the current that is flowing into the grid. The injected current must be sinusoidal with low harmonic distortion (Rahim, Chaniago, & Selvaraj, 2011).

CHAPTER 3

Islanding Detection Methods for PV Grid-Connected Inverter

3.1 Introduction

The "island" condition is a situation where the inverter still continues to supply power to the network even when the grid is no longer present. Island condition can be dangerous and can cause damage of the equipments, failure of automatic reclosing systems, damage of the inverter and safety concern of the workers. Due to the above reasons the inverter must be equipped with anti-islanding detection and protection to avoid the island condition. In grid-connected PV inverters, the methods of islanding detection fall into 3 categories: passive islanding, active islanding, and remote islanding.

3.1.1 Passive Islanding

Passive islanding techniques rely on parameter thresholds. Their advantages are easy implementation (controller not required), no degradation of the PV inverter power quality, and inexpensiveness. Their primary drawbacks are a relatively large None Detection Zone (NDZ) and their ineffectiveness in multi-inverter systems (Syamsuddin, Rahim, Krismadinata, & Selvaraj, 2009; H. Zeineldin & Kirtley, 2009). The most commonly used passive islanding detection techniques are over/under voltage and over/under frequency (OV/UV & OF/UF), phase jump detection (PJD), voltage harmonic monitoring, current harmonic monitoring, rate of change of power output (ROCOP), and rate of change of frequency (ROCOF). The following are important requirements and descriptions on how most of them work:

3.1.1 (a) Over/under voltage and over/under frequency (OVP/UVP and OFP/UFP)

This basic method is based on setting a threshold value for voltage and frequency at the point of common coupling (PCC). Basically, there will be disconnection in the circuit if the value of voltage or frequency is not within the standard limits. Most of the standards usually have their own normal voltage/frequency ranges. Note that the protection method is implemented in software, typically, rather than in actual relays. At PCC,

$$\triangle P = P_{Load} - P_{PV}, \tag{3.1}$$

$$\triangle Q = Q_{Load} - Q_{PV} \tag{3.2}$$

The system basically depends on $\triangle P$ and $\triangle Q$ just before the grid disconnects, to form an island. If $\triangle P \neq 0$, the amplitude at PCC will change, OVP/UVP detects the change, disconnecting the inverter. If $\triangle Q \neq 0$, the load voltage will show a sudden phase shift, leading to a change in the frequency of the inverter output current. OFP/UFP will detect this change and disconnect the inverter. The main advantage of this method to researchers of islanding detection is its low cost (T5-09, 2002; Yu et al., 2010). Other advantages of this method are their easy implementation (no additional controller) and no degradation of PV inverter power quality. Hence the proposed method is not only easy to implement (by using analog circuit), increased effectiveness for islanding detection (being compared with the existing algorithm which used digital concept and added delay to the system) and with a very low cost needed. Fulfilling to what the industry need especially for industrial product which is to lower the cost of the existing product and at the same time increased the effectiveness of the product.

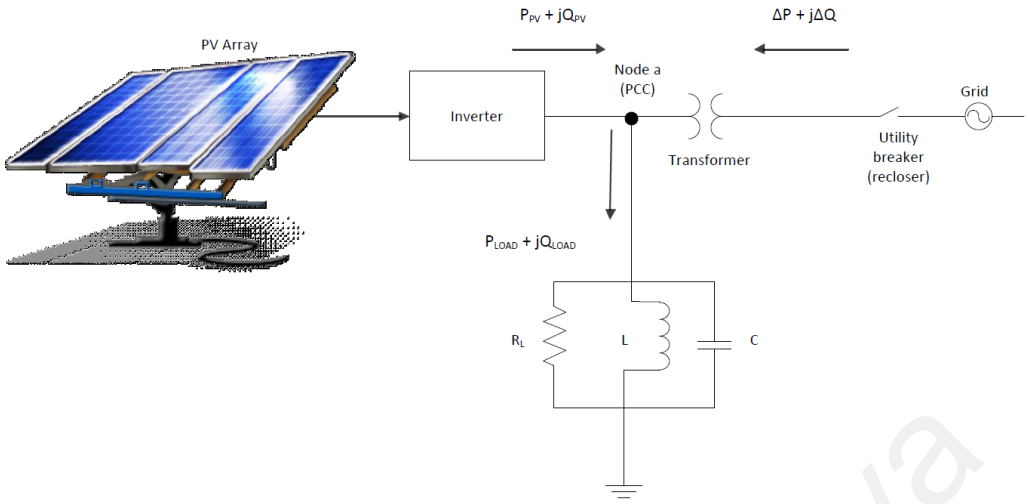


Figure 3.1: PV System/Utility Feeder Configuration, with definitions for power flow and terms (T5-09, 2002)

3.1.1 (b) Phase Jump Detection

Phase jump detection is a method capable of deactivating the inverter if there is a phase difference detected between the inverter output voltage and the inverter output current, such as during islanding. Its main advantage is its effectiveness, even with multiple inverters. Still, the threshold value must be chosen correctly to provide reliable islanding detection without any frequency nuisance trips. Below is the equation for phase-jump algorithm (3.3) (Llaria, Curea, Jiménez, & Camblong, 2011; T5-09, 2002; Yu et al., 2010):

$$\arctan\left(\frac{\frac{\triangle Q}{P}}{1+\frac{\triangle P}{P}}\right) \leq \vartheta_{threshold} \tag{3.3}$$

3.1.1 (c) Monitoring of voltage and current harmonics

This method proposes two parameters for islanding detection: THD and the main harmonics (3^{rd}, 5^{th}, and 7^{th}) of the PCC voltage. If these values exceed a specific limit, the inverter shuts down. During normal operation, the PCC voltage equals the grid voltage, hence the distortion is usually negligible ($THD \approx 0$). During islanding, two mechanisms

can cause the harmonics at PCC to increase:

1. Current harmonics produced by the PV inverter are transmitted to the load,

2. Magnetic hysteresis and other non-linearities in the transformer cause high distortion to the voltage response, increasing THD.

The effectiveness of this method does not temper much in multiple inverter configurations, but it still has that problem of not having an ideal tripping threshold for reliable islanding protection. This method may also fail with high value of Q. A typical condition for a grid-connected PV inverter is that its THD must not exceed 5% of its full rated current. Values of the harmonic limits of the test voltage according to AS4777.2-2005 are as listed in Table 3.1 (De Mango, Liserre, Aquila, & Pigazo, 2006; Dr. Robert H. Wills, 1994; Ranade, Prasad, Omick, & Kazda, 1989; T5-09, 2002; Yu et al., 2010).

Table 3.1: Harmonic limits of the test voltage ("Grid Connection of Energy Systems via Inverters - Part 2: Inverter requirements," 2005; "Grid Connection of Energy Systems via Inverters - Part 3: Grid protection requirements.," 2005)

Harmonics order number	3	5	7	9	11	13
Limit based on percentage of fundamental	4%	2%	1.5%	0.6%	0.1%	0.1%

3.1.1 (d) Rate of change of frequency (ROCOF)

When the grid supply is lost, the system comprising inverter and load becomes islanded. There is thus a power imbalance, which causes transient in the islanded system, and the frequency slowly changes. This change (df/dt) is measured over a few cycles, usually 2-50 cycles. If the change rate exceeds the pre-set value, the inverter shuts down. A ROCOF relay monitors the voltage waveform and trips up the circuit breaker when frequency change rate exceeds the threshold for longer than the preset time-delay. In small and medium DG units, a trip setting of $0.3Hz/sec$ has been found to be the optimum value, with $0.3s - 0.7s$ operating time. With extreme frequency changes, the tripping

time could be set to less than four or five cycles (Freitas, Wilsun, Affonso, & Zhenyu, 2005; Redfern, Usta, & Fielding, 1993).

3.1.1 (e) Rate of change of power output (ROCOP)

As grid loss generally produces load change, monitoring of the changes in the DG power output provides direct detection of islanding. This method monitors all the changes in the power output and integrates those changes over a defined sample period. Tripping occurs when the signal exceeds the trip settings. The method can quickly detect unsynchronized reconnection of the utility supply to a power island containing the DG unit (Redfern et al., 1993).

3.1.2 Active Islanding

Active techniques inject a small disturbance at the PV inverter output for islanding detection. Their main advantage is relatively smaller NDZ than that in passive methods. Their main drawbacks are the possibility of deteriorating output power quality destabilizing the PV inverter, and the need (usually) for additional controllers increasing complexity (Syamsuddin et al., 2009; H. Zeineldin & Kirtley, 2009). Existing active techniques are given next.

3.1.2 (a) Impedance measurement (IM)

This method detects islanding through inverter output impedance changes, caused by loss of the main power. It has many weaknesses, especially the reduced effectiveness as the number of inverters connected to the grid increases (unless all the inverters are somehow synchronized). Another is the necessity to set an impedance threshold to signal that the mains is connected (this requires an exact value of the grid impedance, usually very small). (O'Kane & Fox, 1997) showed indirect method used to measure impedance by introducing a small high-frequency (HF) signal as input to a voltage divider and con-

nected to the mains through a coupling capacitor. The voltage divider circuit changes the output voltage, from which islanding can be detected. All the weaknesses of this method have led some to conclude that it is sometimes impractical (Mohamad, Mokhlis, Bakar, & Ping, 2011; O'Kane & Fox, 1997).

3.1.2 (b) Sliding mode frequency shift (SMS) or active phase shift (APS)

The slide (or slip) mode frequency shift uses positive feedback to the phase of the voltage at PCC to shift the phase (and hence the short-term frequency). (Smith, Onions, & Infield, 2000) proved the method's robustness through a SPICE-based model simulation. Usually, DG operates at unity power factor, so the phase angle between the PCC voltage and the inverter output current is controlled at zero. In SMS method, the current-voltage phase angle is made to be a function of the frequency of the PCC voltage. Usually this method will be implemented through the use of an input filter to the PLL. The authors of reference (Lopes & Huili, 2006) proved that in the Q_f versus f_0 space, this method can be designed to ensure islanding detection in an RLC load with a small quality factor, but as the load quality factor increases, the method's effectiveness decreases (Lopes & Huili, 2006; Smith et al., 2000).

3.1.2 (c) Sandia frequency shift (SFS) or active frequency drift with positive feedback

This method is the accelerated version of active frequency drift (AFD). It uses positive feedback to prevent islanding. With connection to the grid, it tries to amplify small changes in frequency but the stability of the grid prevents it. When the grid disconnects, changes to the frequency produce a phase error. The process continues until the frequency exceeds the threshold of OF or UF. To implement positive feedback, the "chopping fraction" is defined as:

$$C_f = C_{f0} + K\left(f_a - f_{grid}\right) \tag{3.4}$$

With C_{f0} the chopping fraction when there is no frequency error, K the accelerating constant that does not change direction, f_a the measured frequency of the voltage at PCC, and f_{grid} the grid frequency. SFS method is known as one of the active methods that have small NDZ. It depends on its parameters C_{f0} and K. (H. H. Zeineldin & Kennedy, 2009) showed that the performance of this method depends on the parameter K. Simulation results show that the mathematical formula derived to optimally set this parameter is highly effective and able to eliminate NDZ. In (H. H. Zeineldin & Conti, 2011), the same author tested this method with multiple DGs and validated it through simulation results (T5-09, 2002; H. H. Zeineldin & Conti, 2011;H. H. Zeineldin & Kennedy, 2009).

3.1.2 (d) Reactive power export error detection (RPEED)

An RPEED relay combined with a DG control system generate a level of reactive power flow in the inter-tie between the DG and the grid. Islanding is detected through relay tripping, once the grid connection is lost. The relay tripping is triggered by the error existed between the setting and the actual reactive power being exported for a time period longer than the pre-set value. The operating time for this method is typically 2 to 5 seconds; it is thus suitable only as backup protection. It nevertheless is considered more effective than passive method, especially for small-load changes or no-load changes during off-grid (Chowdhury et al., 2009; Mohamad et al., 2011).

3.1.3 Remote techniques

Remote islanding detection techniques are based on the communication between the utility and the PV inverter unit (Syamsuddin et al., 2009) .This technique does not have NDZ and does not degrade the PV inverter power quality. In multi-inverter systems it is effective but expensive to implement (especially in small systems) and has a complicated communication technique.

3.1.3 (a) Power line carrier communication (PLCC)

In principle, this method uses a low-energy communication signal along the power line. A transmitter (T) is placed near the grid protection switch, and a receiver (R) is installed at the PCC as shown in Figure 3.2. Without islanding, a low energetic signal is transmitted to the receiver. During islanding, communication stops the data transmission, ordering the inverter to trip. This scheme has been proven to be very effective in multiple-DG configurations. Several properties must be complied with by the transmitter signal to ensure smooth islanding detection. Firstly, the signal must be sent continuously, then the signal frequency must be low because of transformer inductance (which acts as a low-pass filter), and lastly the signal must able to travel from the grid to the load (De Mango, Liserre, & Aquila, 2006; Kunte & Wenzhong, 2008; Llaria et al., 2011).

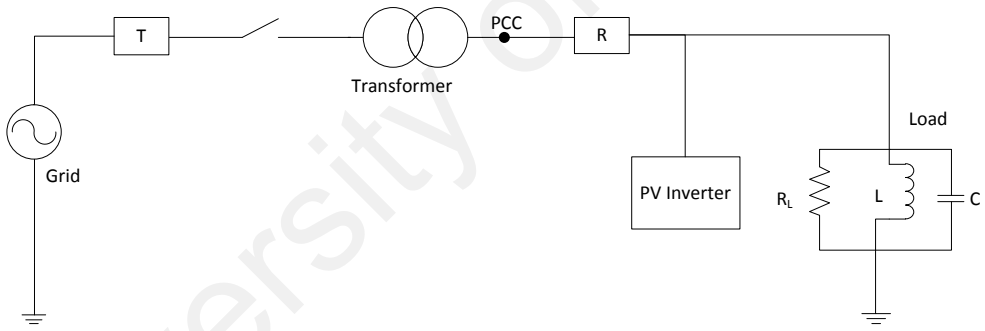


Figure 3.2: Anti-islanding method based on PLCC with transmitter (T) and receiver (R) (De Mango, Liserre, & Aquila, 2006)

3.1.3 (b) Signal produced by disconnect (SPD)

This method is similar to PLCC. The only difference is the type of transmission used (microwave link, telephone link, or others). Its switch state is directly communicated to the DG. Its strengths are additional supervision and full control of both the grid and the DG. Its drawbacks, however, include relative expensiveness, also possible/significant licensing and design complications (Yu et al., 2010).

3.1.3 (c) Supervisory Control and Data Acquisition (SCADA)

A supervisory control and data acquisition (SCADA) system monitors the auxiliary contacts on all utility circuit breakers that are liable to check the conditions of islanded operation. Upon islanding, a series of alarm is activated and the corresponding circuit breaker is tripped. This method is highly effective in detecting islanding, but it is too expensive and requires many sensors. Its drawback is that it is rather slow, especially when the system is busy (with disturbances) (Funabashi, Koyanagi, & Yokoyama, 2003; Strath, 2005).

3.2 Anti-islanding standards

Among the popular reference standards for islanding include IEEE 929-2000, IEC 62116, IEE 1547, VDE 0126-1-1, and AS 4777.3-2005. These standards have been fully utilized to help the researchers in designing their product.

Table 3.2 shows all the standards as having their own Q value, islanding disconnection time, frequency and voltage operation range (Yu et al., 2010). According to IEEE929-2000 standard, Q is:

$$Q = \tan\left(arccosine\left[pf\right]\right) \tag{3.5}$$

The selected Q of 2.5 equals to 0.37 power factor. As power factor increases, Q decreases. The test requirement that Q=2.5 is equal to lines with uncorrected power factors from 0.37 to unity; this seems to reasonably cover all distribution line configurations (*IEEE Recommended Practice for Utility Interface of Photovoltaic (PV) Systems*, 2000). Japan standard proposes that Q equals 0 and that rotating machinery is added during islanding test (Yu et al., 2010). Besides Q, islanding disconnection time is also crucial. The German VDE 0126-1-1 has the strictest disconnection time limit: below 0.2 seconds. Normal frequency and voltage range also are important to islanding detection. Australian standard AS 4777.3-2005 requires that nominal frequency and voltage range be set by

Table 3.2: Reference standards for anti-islanding (Yu, et al., 2010)

	Quality factor, Q_f	Required islanding detection time, t	Normal frequency range, f (nominal frequency f_0)	Normal voltage range, V (% of nominal voltage V_0)
IEC 62116	1	$t < 2s$	$(f_0 - 1.5Hz) \leq f$ and $f \leq (f_0 + 1.5Hz)$	$85\% \leq V \leq 115\%$
IEEE 1547	1	$t < 2s$	$59.3Hz \leq f \leq 60.5Hz$	$88\% \leq V \leq 110\%$
IEEE 929-2000	2.5	$t < 2s$	$59.3Hz \leq f \leq 60.5Hz$	$88\% \leq V \leq 110\%$
Japanese standard	0 (+rotating machinery)	Passive : $t < 0.5s$ Active : $0.5s < t < 1s$	Setting value	Setting value
Korean Standard	1	$t < 0.5s$	$59.3Hz \leq f \leq 60.5Hz$	$88\% \leq V \leq 110\%$
VDE 0126-1-1	2	$t < 0.2s$	$47.5Hz \leq f \leq 50.2Hz$	$80\% \leq V \leq 115\%$
AS 4777.3-2005	1	$t < 2s$	Setting value	Setting value

manufacturer. Steps to obtaining trip values are: (1) determination of under/over voltage and under/over frequency values through gradual increase or decrease of voltage and frequency until the device tested (the inverter) disconnects from the variable ac supply, and (2) reading of the over/under voltage or over/under frequency values at which disconnection occurred. A criteria of acceptance for over/under voltage is that the value at step (2) should equal an under-voltage set point of ±5V; for frequency, the value should equal an under-frequency set point of ±0.1Hz (*Grid Connection of Energy Systems via Inverters - Part 2: Inverter requirements*, 2005; *Grid Connection of Energy Systems via Inverters - Part 3: Grid protection requirements.*, 2005).

Figure 3.3 shows a typical anti-islanding test circuit for PV grid-connected inverter as outlined by IEEE 929-2000.

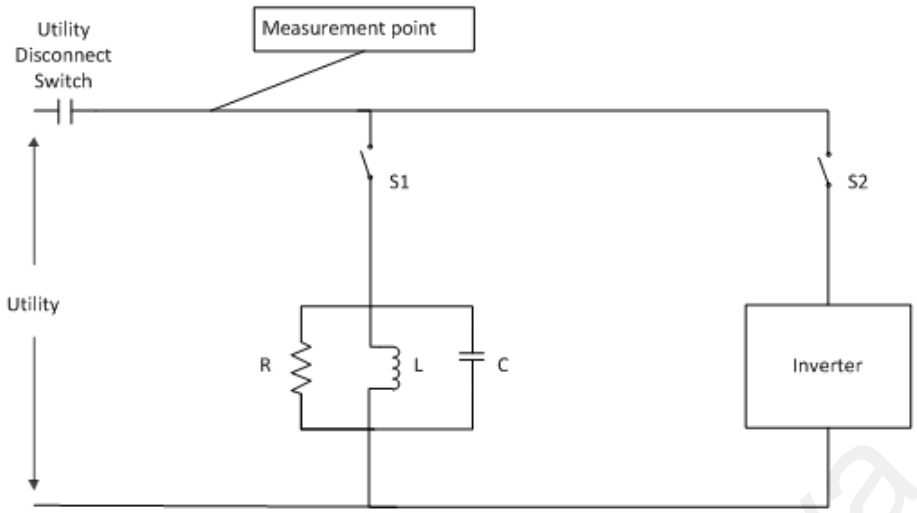


Figure 3.3: Anti-islanding test circuit ("IEEE Recommended Practice for Utility Interface of Photovoltaic (PV) Systems," 2000)

3.3 None Detection Zone (NDZ)

NDZ enables determination of the best method, which is the one with the smallest NDZ area (Ropp et al., 2000). (H. Zeineldin & Kirtley, 2009) proved that passive islanding has larger NDZ than does active islanding. NDZ can be detected/analyzed 2 ways, either by load parameter space (LPS) or by power mismatch space (PMS) (Yu et al., 2010).

- LPS is suitable for islanding detection that is based on frequency drifting (Yong-zheng Zhang & Lopes, 2007). LPS or RLC load space, predicts NDZ through zero phase error (called phase criteria) between the PV output current and the terminal voltage. Through the phase criteria, NDZ can be mapped out to normalized C_{norm} against load inductance (L). This method can predict the NDZ location for each method but not the method's disconnection time. Ropp et al. proved that the worst case of islanding detection involves loads that have high Q factor (Ropp et al., 2000).(See Table 3.3)

Table 3.3: Phase criteria for several islanding prevention methods (Ropp, et al., 2000)

Islanding prevention scheme	Phase criterion	How to use phase criterion (P.C.)
OFR/UFR	$\tan^{-1}\left[R\left(\omega C-\frac{1}{\omega L}\right)\right]=0$ $\Downarrow$ $\omega C-\frac{1}{\omega L}=0$	If ω at which the P.C. is satisfied lies within OFR/UFR trip limits, the RLC load is inside the NDZ
PJD	$\tan^{-1}\left[R\left(\omega_0 C-\frac{1}{\omega_0 L}\right)\right]\leq\phi_{th}$	If the P.C. is satisfied at ω_0 (line frequency), the RLC load is inside the NDZ
SMS	$\tan^{-1}\left[R\left(\omega C-\frac{1}{\omega L}\right)\right]=-\arg\left[\left(G(j\omega)\right)\right]$	If ω at which the P.C. is satisfied lies within OFR/UFR trip limits, the RLC load is inside the NDZ
AFD	$\tan^{-1}\left[R\left(\omega C-\frac{1}{\omega L}\right)\right]=-\frac{\pi c f}{2}$	If ω at which the P.C. is satisfied lies within OFR/UFR trip limits, the RLC load is inside the NDZ
SFS	$\tan^{-1}\left[R\left(\omega C-\frac{1}{\omega L}\right)\right]=-\frac{\pi(cf_{k-1}+K\Delta\omega)}{2}$	If ω at which the P.C. is satisfied lies within OFR/UFR trip limits, the RLC load is inside the NDZ

- PMS exploits the power mismatch in R, L, and C. The power mismatch is controlled by the grid, but when the grid is disconnected, the power mismatch increases, putting the voltage and frequency out of its nominal value (Zhihong, Kolwalkar, Yu, Pengwei, & Reigh, 2004).

$$\left(\frac{V}{V_{max}}\right)^2-1\leq\frac{\Delta P}{P}\leq\left(\frac{V}{V_{min}}\right)^2-1 \tag{3.6}$$

$$Q_f\left[1-\left(\frac{f}{f_{min}}\right)^2\right]\leq\frac{\Delta Q}{P}\leq Q_f\left[1-\left(\frac{f}{f_{max}}\right)^2\right] \tag{3.7}$$

As outlined by IEEE 929-2000, where $V_{max}=110\%$, $V_{min}=88\%$, $f_{max}=60.5Hz$, $f_{min}=59.3Hz$, and $Q_f=2.5$. The equation can be derived as:

$$-17.36\%\leq\frac{\Delta P}{P}\leq 29.13\% \tag{3.8}$$

$$-5.94\% \leq \frac{\Delta Q}{P} \leq 4.11\% \tag{3.9}$$

From 3.8 and 3.9, Zhihong Ye et al. proved that if the active power and reactive power mismatches are within the specified range, the operating frequency and voltage will remain inside the nominal range, making islanding detection impossible. From both the equations, NDZ area can be mapped as in Figure 3.4 (Eltawil & Zhao, 2010); (Ropp et al., 2000); (T5-09, 2002). This paper also highlights that each Q will have its own NDZ, and the smaller the Q_f , the smaller the NDZ (Zhihong et al., 2004).

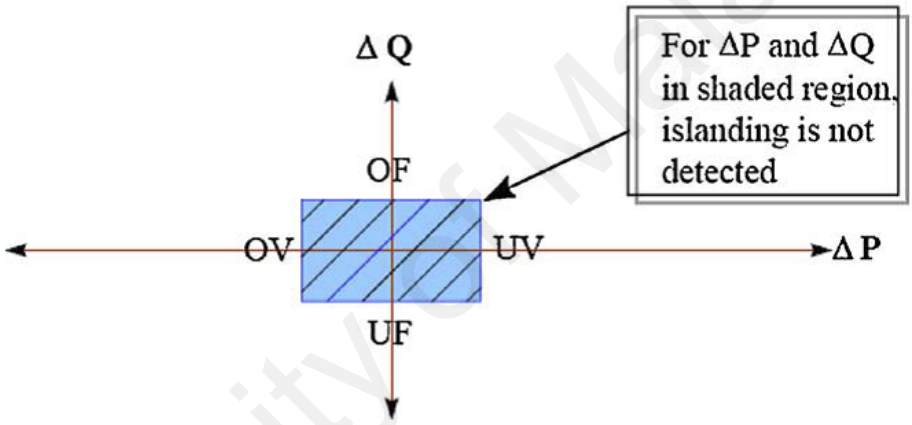


Figure 3.4: NDZ mapping in ΔP versus ΔQ space for OUV and OUF (Eltawil & Zhao, 2010; Ropp, et al., 2000; T5-09, 2002)

Many papers have published ways to eliminate or reduce NDZ. Behrooz Bahrani et al. (Bahrani, Karimi, & Iravani, 2011) validated their NDZ-eliminating approach in an active islanding method. They analytically analyzed and proved that the method has an NDZ in LPS owing to the effect of unbalanced three-phase RLC load. Basically, active islanding method injects a negative sequence current as a disturbance signal to a DG system. Islanding is detected through the corresponding negative sequence voltage at PCC.

NDZ is eliminated by a slight modification to the control algorithm; the phase angle of the injected negative-sequence current $I_{n,a}$ is technically changed periodically between

zero and π. The modification uses a periodic pulse as the reference signal of the negative-sequence current controller. Note that the paper also tested and evaluated the islanding method on various types of two-DG configurations.

H.H. Zeineldin et al. (H. Zeineldin & Kirtley, 2009) proposed a simple passive islanding technique with negligible NDZ. They proposed a simple OV/UV method that detects voltage deviation upon islanding. They also verified and concluded that different values of reference power expressed as a function of voltage will reduce or increase NDZ. The PSCAD/EMTDC simulation result of (H. Zeineldin & Kirtley, 2009) proved that the use of power voltage expression with positive slope reduces NDZ. They also verified that setting the slope of the power voltage expression tangential to the active power output results in negligible NDZ. The mathematical operation developed can be simply implemented in the control algorithm. Future work may include experiment result supporting the existing simulation result.

3.4 Principle of detection method

A good islanding detection method ensures reliable detection. This section elaborates on the principle of the islanding detection methods commonly used now: detection of THD or harmonics, frequency of PCC voltage, changes to the grid impedance, power variation, voltage at PCC, wavelet detection, even combinations of several detection methods into one. The followings are the summary of the works done based on the above mentioned ways of islanding detection:

3.4.1 Detection of THD or harmonics

(Jae-Hyung, Jun-Gu, Young-Hyok, Yong-Chae, & Chung-Yuen, 2011) proposed a system that injects the output current with a ninth harmonic component that is less than the pre-defined standard into the grid. Goertzel algorithm is then used to detect the ninth harmonic component of the V_{PCC}. The Goertzel algorithm is a kind of discrete Fourier

transformation that extracts from the input signal, the phase and magnitude of the desired frequency. When islanding occurs, $V_{PCC}$and V_{load} become equal, and hence, so do Z_{PCC} and Z_{load}. The proposed method detects the magnitude of the ninth harmonic and stops the system within two periods due to the appearance of the injected ninth harmonic current in the V_{PCC}. The advantage of this technique is that any order of the harmonic (third, fifth, and seventh), or two or more harmonics side by side, can be chosen.

The authors from the reference (Liserre, Pigazo, Dell'Aquila, & Moreno, 2006) have validated the islanding detection capability of their proposed method (which modifies a three-phase system through use of resonant controllers to make it suitable for single-phase systems, and uses a grid voltage sensorless algorithm). In principle, grid voltage sensorless method compares the predicted voltage with the real ones. The voltage is predicted by assuming that the grid is present, and that when the grid is missing, the algorithm will suffer a transient that is stronger (case of DG system power equaling load power) than that of a system adopting grid voltage measurement. The authors developed the Kalman filter (KF) algorithm to detect this transient. The system detects islanding by comparing the estimated grid voltage with the measured grid voltage through the energy associated with each of the harmonic error. The method was successfully tested with real grid conditions and nonlinear load.

3.4.2 Detection of frequency

Two examples from passive islanding detection based on frequency detection are basic OF/UF and ROCOF. Frequency change rate is one of the common methods used in the United Kingdom and Europe (Soo-Hyoung & Jung-Wook, 2009). (Syamsuddin et al., 2009) proposed basic passive islanding detection through TMS320F2812 DSP, for OF/UF; the frequency is calculated from the instantaneous voltage value from the first zero crossing until the third. DSP increases the counter value while reading the voltage

value for N sampling time. The frequency data are then stored in the memory register and compared with the pre-set threshold value in the islanding detection algorithms. If the memory's data exceed the pre-set threshold value, the DSP sends a signal to turn off the relay that disconnects the system.

An active islanding method that also uses frequency to detect islanding is Active Frequency Drift (AFD). It varies the output current frequency through positive feedback. It injects a current with slightly distorted frequency into the PCC. Upon grid disconnection, the phase error between the PCC voltage and the inverter current is detected by the inverter, which then tries to compensate by increasing the frequency of the injected current until it exceeds the OF/FU limits. Its performance is poor, however, and a suitable chopping fraction (cf) value to meet the harmonic limits is hard to choose. Hence, a novel AFD method (Jung, Choi, & Yu, 2007) with a periodic chopping fraction that deviates from the frequency instantly from nominal is proposed. Another problem in conventional AFD method is the amount of THD injected into the grid. THD usually defines the NDZ of a method. Ahmad Yafaoui et al. (Yafaoui, Bin, & Kouro, 2012) proposed an improved AFD method that can detect islanding with less THD compare to the conventional AFD. Simulation and experiment results show the proposed method to produce 30% less THD in the current waveform. The proposed method is based on a different current distortion injection waveform. The RMS value and the Fourier series coefficient of the proposed current waveform are obtained and used to derive analytically some of the operational characteristic of the method.

Wen-Jung et al. (Chiang et al., 2010) proposed an active islanding method incorporated into the control of a grid-connected inverter that acts as a virtual resistor (Chiang et al., 2010) or virtual capacitor (Chiang, Jou, & Wu, 2012). For virtual-resistor operation, the frequency is slightly higher (80Hz) or lower (50Hz) than the grid voltage frequency (60Hz). For virtual-capacitor operation, the frequency is slightly lower than the grid volt-

age frequency. Neither the virtual resistor function nor the virtual capacitor function is activated when the grid is connected. With grid loss, the grid-connected inverter acts as a virtual resistor or a virtual capacitor. Islanding is thus detected from variations in the local load voltage amplitude and frequency. Analysis and experiment results verified that the proposed method can effectively detect islanding with various load types and quality factors. Figure 3.5 is a diagram of the control used in (Chiang et al., 2012; Chiang et al., 2010). The grid-connected inverter is controlled by the current-mode controller. The controller output is sent to a PWM circuit to generate the proposed PWM signals.

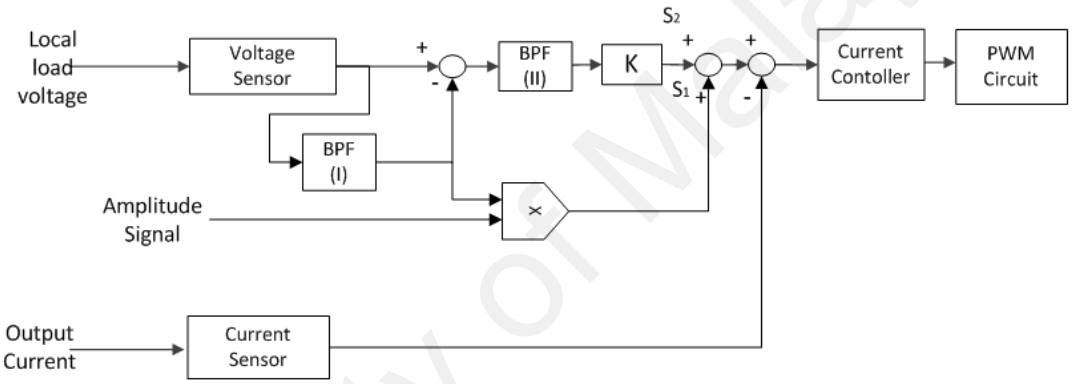


Figure 3.5: Control of the grid-connected inverter as virtual resistor or virtual capacitor (Chiang, et al., 2012; Chiang, et al., 2010)

3.4.3 Detection of impedance

Because of the small NDZ, impedance monitoring became one of the most popular methods researched for active islanding detection. There is an initiative by researchers in developing an active method that introduces fewer disturbances to the DG system. An example is the method developed by M. Cionbotaru et al. (Ciobotaru, Agelidis, & Teodorescu, 2008) which is based on phased-locked loop (PLL) controller and grid impedance changes. (Hamzeh, Farhangi, & Farhangi, 2008) also proposed an active method; it combines PI and predictive controllers to generate the reference current and the inter-harmonic current for injection into the DG system. The authors adopted DFT algorithm to finally

estimate the grid impedance for islanding detection.

Soo-Hyoung Lee et al. (Soo-Hyoung & Jung-Wook, 2009) reported the development of a passive method to determine islanding through impedance detection that uses the switching frequency of a PWM inverter. The authors proved that impedance during islanding is much larger than that in pre-islanding. The proposed modulation frequency (mf) is 21-330, with the usual switching frequency being 1260Hz- 20 kHz. The idea is that islanding can be detected through variation in impedance with respect to inverter switching modulation. (Soo-Hyoung & Jung-Wook, 2009) concluded that this method:

a) has zero NDZ;

b) does not cause any intended changes in reactive power or harmonics variation to the DG system as do other active methods;

c) is successful in detecting islanding in single and multiple grid-connected DG systems as proven by PSCAD/EMTDC simulation in (Soo-Hyoung & Jung-Wook, 2009) (within 20ms).

David Diaz Reigosa et al. (Reigosa, Briz, Blanco, Garcia, & Guerrero, 2011; Reigosa, Briz, Charro, Garcia, & Guerrero, 2012) proposed a new active method that measures the high-frequency impedance of the grid. This method injects a high-frequency signal for islanding detection of microgrids. It relies on variations in the high-frequency impedance measured, obtained from the output current estimated and the output voltage measured, of the LCL filter, through complex-vector filters. This method detects islanding in the range of a few milliseconds.

3.4.4 Detection of power variation

Many anti-islanding detection methods degrade power quality. One literature suggests that high power quality can be obtained with high islanding-detection capability

(Yu, Matsui, So, & Yu, 2008). The technique uses effective power variation, a periodic increase or decrease of the inverter output current magnitude. Such variation keeps the total average real power from the PV to be constant without affecting the maximum power point tracking (MPPT) function of the PV inverter. Results of the proposed method show the reference current varying proportionally with deviations in the inverter output voltage after islanding. If the inverter output voltage varies largely, AFD method will be activated for a limited period to detect islanding. Positive and negative chopping fractions were used here to improve transient response.

Jun Zhang et al. (Jun et al., 2013) proposed an improved islanding method that is based on intermittent bilateral (IB) reactive power variation (RPV). The variation scheme proposed for this method is the setting of the reactive power reference. The proposed method monitors system frequency and determines islanding once the frequency runs out of the normal range. It detects and controls the inverter output reactive power to the required variation. This technique has been validated by a three-phase grid-connected inverter with 6kW active power. The experiment results show the intermittent bilateral reactive power variation (IBRPV) method capable of eliminating NDZ in less than 2s.

In (Cardenas & Agbossou, 2012), an active islanding detection algorithm proposed by the same author in (Cardenas, Agbossou, & Doumbia, 2009) was validated for multi-inverter system configurations. The proposed algorithm is based on positive voltage feed-back. The rms voltage measured at PCC is taken as feedback variable V_{rms}. Variations of V_{rms} are then used to generate a limited active power perturbation (ΔP). Synchronization of DG units is not required because all the units use the same variable (V_{rms}) to generate their local anti-islanding protection. The experiment results verified that islanding could be confirmed within 250ms on 60Hz utility voltage.

3.4.5 Detection of negative sequence voltage at PCC

Behrooz Bahrani et al. (Bahrani et al., 2011) proposed an active islanding method in which a negative-sequence current controller injects a disturbance signal of negative-sequence current. With grid connection, the injected negative-sequence current flows to the grid. Without grid, the injected negative-sequence current flows to the load, unbalancing the PCC voltage. The magnitude of the corresponding negative-sequence voltage at PCC is used to detect islanding; if it exceeds the threshold, the system is islanded.

Houshang Karimi et al. (Karimi, Yazdani, & Iravani, 2008) also proposed similar active islanding detection, which injects a small negative-sequence current through a 3-phase VSC controller and detecting the corresponding negative-sequence voltage at PCC through a UTSP (which basically is a modified PLL, is more immune to noise, so is reliable for detection of small magnitude negative-sequence voltage). The UTSP introduced also precisely detects negative-sequence voltage even when the signal is polluted with a 30dB signal-to-noise ratio (SNR) Gaussian white noise. PSCAD/EMTDC simulation shows the proposed islanding detection method able to detect islanding within 60ms (3.5 cycles) under UL1741 test conditions.

Another active islanding method, developed by B. Indu Rani et al. (Indu Rani, Srikanth, Saravana Ilango, & Nagamani, 2013), monitors PCC voltage. It depends on changes to the magnitude of the injected current. The current is perturbed by reducing the magnitude of the reference current to 80% of I_{ref}, for 2 cycles. As only the current magnitude reduces, the perturbation does not affect power quality as do other active islanding techniques. When the grid disconnects, the PCC voltage change exceeds the allowable range, and islanding is detected. The simulation was on MATLAB/Simulink, and the algorithm was implemented on ALTERA CYCLONE FPGA. The detection time for the worst case in the proposed method was 400ms.

P.K. Dash et al. (Dash, Padhee, & Panigrahi, 2012) proposed a new time-frequency approach for power island detection in DG systems. It uses a hybrid of a fast variant of the S-Transform (ST) algorithm and an FES. The negative sequence voltage and current signals from the DG system are obtained through the fast ST. These features are then used as inputs to the FES to detect islanding.

3.4.6 Wavelet transformation

Many papers have been recently published on wavelet-based islanding detection. This method is basically a passive method; it does not introduce any disturbances to the system. It will eliminate NDZ without any disturbances that can deteriorate output power quality.

Discrete Wavelet Transform (DWT) is a signal processing tool that can be used when time-varying harmonics must be evaluated, and, as in islanding detection, time localization is required (Hanif, Dwivedi, Basu, & Gaughan, 2010). Use of DWT enables a signal's decomposition into several signals of different frequency bands, called wavelet coefficients.

The wavelet coefficient for voltage or frequency signal is compared with the preset threshold value. If the relevant wavelet coefficient remains above the preset threshold value for a time longer than the pre-set time threshold, islanding will be detected. The pre-set threshold value shall be determined through the simulation and experiment result.

(Arachchige & Rajapakse, 2011) investigated an intelligent method that is based on the wavelet coefficients of transient signals. A trained DT classifier that uses the energy associated with the wavelet coefficients is the islanding detector. The proposed method always responded in less than 24ms every time islanding occurred.

(Shariatinasab & Akbari, 2010) introduced islanding detection that is based on wavelet packet transform. It uses only the local measurement of voltage and current at PCC. In

(Morsi, Diduch, & Chang, 2010), this method detected islanding only by evaluating the current signal at PCC. Its primary advantages are its suitability for use in multiple-DG configurations and its ability to detect islanding within less than one third of a cycle, i.e., 5.5ms, for a 60Hz grid frequency.

The first paper published on wavelet-based islanding detection algorithm was by Alberto Pigazo et al. (Pigazo, Liserre, Mastromauro, Moreno, & Dell'Aquila, 2009; Pigazo et al., 2007), in 2007. They proposed a detection method that takes advantage of the time and frequency localization of the DWT, which is applied to the high-frequency components introduced by the distributed power generation system inverter at the PCC. It is considered a passive method because its ability to detect islanding is based on the voltage and current signals at PCC.

In (Ray, Kishor, & Mohanty, 2012), Prakash K. Ray et al. compared WT with ST through the extracted features for islanding detection in hybrid DGs. The hybrid system consists of DG resources such as PV, fuel cell, and wind energy connected to the grid. The method uses the negative sequence component of the voltage signal in islanding detection. The results showed ST to be more advantageous than WT.

As a conclusion, wavelet-based detection is a passive technique that performs as good as an active technique, and is no doubt the new future technique for anti-islanding (Hanif, Basu, & Gaughan, 2011).

3.4.7 Combination of detection methods

There has also been much effort into combining the various methods. It considers the advantages of each method and combines them for best results. The following are several combination islanding detection methods.

a) Combination of voltage amplitude and frequency at the PCC: This method injects a disturbance signal through either the direct axis (d-axis) or the quadrate axis (q-

axis) current controllers of the interface VSC. Signal injection through the d-axis controller will modulate the amplitude of the voltage at PCC. Meanwhile, signal injection through the q-axis controller will cause frequency deviation at PCC during islanding. This method can detect islanding as fast as 33.3ms (Hernandez-Gonzalez & Iravani, 2006). Waleed K.A. Najy et al.(Najy, Zeineldin, Alaboudy, & Wei Lee, 2011) have also proposed an accurate and efficient passive method that uses PCC voltage and frequency as islanding indicators. The proposed method was tested on various disturbances such as active and reactive power mismatches with constant RLC loads, dynamic loads during islanding, and fault disturbances under fully loaded and lightly loaded systems conditions. It can differentiate between islanding and non-islanding for closely matched load-DG rating, reducing the NDZ of the OV/UV and OF/UF methods.

b) Combination of rate of voltage change (passive method) and real power shift (active method): if an average rate of voltage change (passive technique) cannot justify between islanding and other events in the system, a real power shift (active technique) will be activated to change the real DG power. According to the algorithm, voltage are measured and compared between V_{smin} and V_{smax} values. If the value lies between V_{smin} and V_{smax} , RPS is activated, which increases or decreases the real power generation on one of the DGs. The second stage of the algorithm compares values with V_{smaxU} (a set point to detect islanding). Islanding is detected when the values match the V_{smaxU}. The main advantages of this method are that it eliminates the need for disturbance injection (unlike any other active methods) and efficiently detects islanding. The proposed method has been validated in a distribution network in Aalborg, Denmark (Mahat, Zhe, & Bak-Jensen, 2009).

c) Combination of voltage unbalance and current THD: both are the parameters for

detecting islanding especially in the case of small changes in the load for DG. Three parameters are monitored for the final decision on islanding detection. At every sampling time, this method calculates the average voltage of 3-phase VUavg,t, the THDavg,t average of the phase-A current, and the average voltage $V_{avg,t}$ of the line-to-line voltage. For large variations of DG load, the proposed method easily detects islanding through the $V_{avg,t}$ values, whereas for little variations, it checks the other monitoring parameters ($THD_{avg,t}$ and $VU_{avg,t}$). The proposed method has been validated on several distribution network conditions and is expected to be an effective islanding detection method for industrial fields (Sung-Il & Kwang-Ho, 2004).

d) Combination of frequency, voltage magnitude, phase change, THD, various sequence voltage, current and power: Maldhar Padhee et al.(Padhee, Dash, Krishnanand, & Rout, 2012) proposed the simulation of a novel islanding technique that uses features estimated by a novel FGNW algorithm. A certainty-factor-based FES is then constructed by using the most significant features obtained through the FGNW algorithm to differentiate between islanding and non-islanding (only the parameters that exhibit significant deviations are chosen as inputs for the FES). The simulation results show the proposed method able to detect islanding in less than one cycle.

3.5 Summaries of Hybrid Method

The limits and the implementation procedure of the methods must be known before making any comparisons. All the methods discussed may have the following limits:

a) Reduced power quality and system instability (owing to positive feedback)

b) NDZ

c) False operation or ineffectiveness (in multiple-DG configurations)

d) High implementation costs.

Those limits cause active islanding detection to be more focused on. Still, despite the lower reliability of passive methods, they are sometimes combined with active methods to increase effectiveness.

Existing method are still lacking (most of them make use of active methods) because active techniques inject a small disturbance at the PV inverter output to detect islanding. Their main drawbacks are the possibly deteriorated output power quality causing instability to the PV inverter and normally require additional controllers which increased the complexity of the method. These drawbacks bring too many issues especially in current industrial state where cost and effectiveness play an important role to the product developed. Hence the choice of method that will be used in this research will focus on increasing the effectiveness for islanding detection (speed of detection), easy implementation and with a very low cost needed.

Table 3.4: Comparison of the principle methods for islanding

Principle Method of Detection	Classification	Speed of Detection / Run-On time	NDZ
Harmonics/ THD	Active method (Jae-Hyung et al., 2011) (Goertzel algorithm)	0.4 seconds	None
	Passive method (Liserre et al., 2006) (Grid voltage sensorless)	45ms	None
Frequency	Passive method (Syamsuddin et al., 2009) (OF/UF)	Within 2 seconds	Large
	Active method (Jung et al., 2007) (a novel AFD)	Within 2 seconds	Exist but less than conventional AFD method
	Active method (Chiang et al., 2010) (virtual resistor method)	39ms (with Q=2.5)	None
	Active method (Chiang et al., 2012) (virtual capacitor method)	51ms (with Q=2.5)	None
	Active method (Yafaoui et al., 2012) (improved AFD)	Within 2 seconds	Very small

continued on the next page

Changes of impedance	Passive method (Soo-Hyoung & Jung-Wook, 2009) (switching frequency)	20ms	None
	Active method (Ciobotaru et al., 2008) (PLL)	0.95 seconds	None
	Active method (Hamzeh et al., 2008) (PI & predictive controller)	0.77 seconds	Very small
	Active method (Reigosa et al., 2011; Reigosa et al., 2012) (high frequency signal injection)	A few milliseconds	None
Power variation	Power variation Active method (Yu et al., 2008) (effective power variation with AFD)	0.3 second (with Q=2.5)	None
	(reactive power variation) (Jun et al., 2013)	Less than 2 seconds	None
	Active methods(Cardenas & Agbossou, 2012; Cardenas et al., 2009) (voltage positive feedback)	250ms	None
Negative sequence voltage at PCC	Active method (Bahrani et al., 2011) (injecting a disturbance signal of negative-sequence current)	120ms	None
	Active method (Karimi et al., 2008) (injecting a disturbance signal of negative-sequence current)	60ms (3.5cycles)	None
	Active method(Indu Rani et al., 2013) (reducing the magnitude of the injected current)	400ms	Very small
	Passive method (Dash et al., 2012) (Fuzzy & S-Transform)	Less than 20ms (less than 1 cycle)	Very small

continued on the next page

Wavelet	Passive method (Hanif et al., 2010) (wavelet)	50ms (2.5 cycles)	Almost zero
	Passive method (Arachchige & Rajapakse, 2011) (wavelet coefficients of transient signals)	24ms	None
	Passive method (Shariatinasab & Akbari, 2010) (Discrete Wavelet Transform)	5.5ms (for 60Hz)	None
	Passive method (Morsi et al., 2010) (Wavelet packet transform)	Very small	None
	Passive method (Pigazo et al., 2009) (Discrete Wavelet Transform)	Less than 20ms (less than 1 cycle)	None
	Passive method (Ray et al., 2012) (Wavelet transform & S-Transform method)	Very small	None
Combination	Active method (Hernandez-Gonzalez & Iravani, 2006) (Combination of voltage amplitude and frequency at the PCC)	33.3ms	Very small
	Passive method (Najy et al., 2011) (Combination of voltage amplitude and frequency)	150ms	Very small
	Active & passive method (Mahat et al., 2009) Combination of a rate of voltage change (passive) and real power shift (active)	Within 2 seconds	small
	Passive method (Sung-Il & Kwang-Ho, 2004) (Combination of voltage unbalance and total harmonic distortion of current)	Within 2 seconds	None
	Passive method (Padhee et al., 2012) (Fast Gauss Newton Algorithm)	Under 20ms (under 1 cycle)	Very small

CHAPTER 4

Hardware & Software Development

4.1 Introduction

A PIC18F4550 microcontroller based islanding detection (as in Figure 4.1) for single phase grid connected PV inverter developed is low cost and effective with 3 inputs channels designed for voltage and frequency data collection. Generally, PIC18F4550 provides 40 general purposes of I/O pins, they are Port A (RA0 ... RA5), Port B (RB0 ... RB7), Port C (RC0... RC7), Port D (RD0... RD7) and Port E (RE0... RE3). Port A, Port B and Port E also serve as analog inputs to the ADC. Furthermore, this microcontroller is a very high performance microcontroller, embedded with enhanced flash and is a USB microcontroller with nano Watt technology. The special PIC18F4550 features are listed in Appendix C.

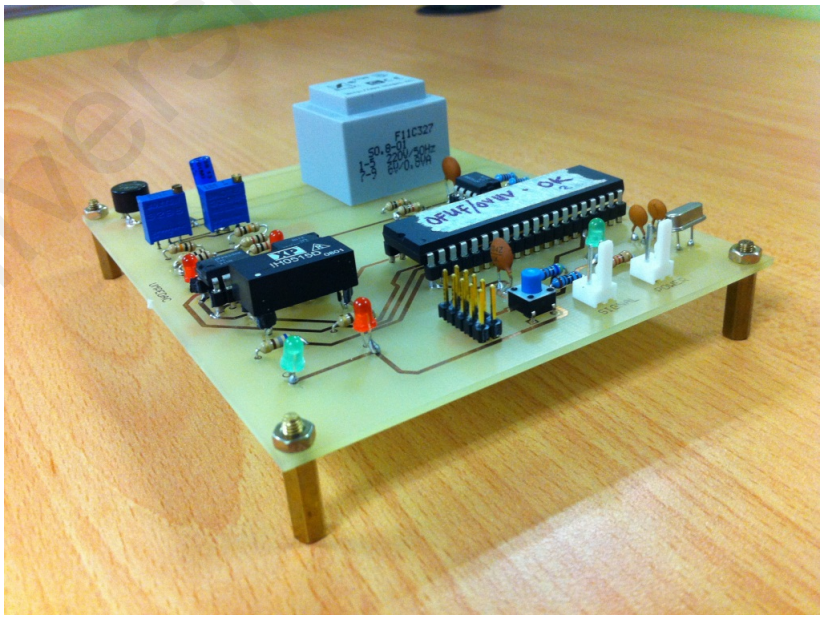


Figure 4.1: Photo of PIC18F4550

4.2 Overall block diagram of the grid-connected PV inverter with the proposed method

Figure 4.2 is the block diagram of the grid-connected PV inverter system with PIC 18F4550 microcontroller for islanding detection integrated with the main controller for the inverter system. In this work, the proposed low cost and effective passive method is developed using microcontroller PIC18F4550. The controller handles the proposed passive islanding of under/over voltage and under/over frequency detection before the signals are sent to the main controller of the single-phase grid-connected inverter.

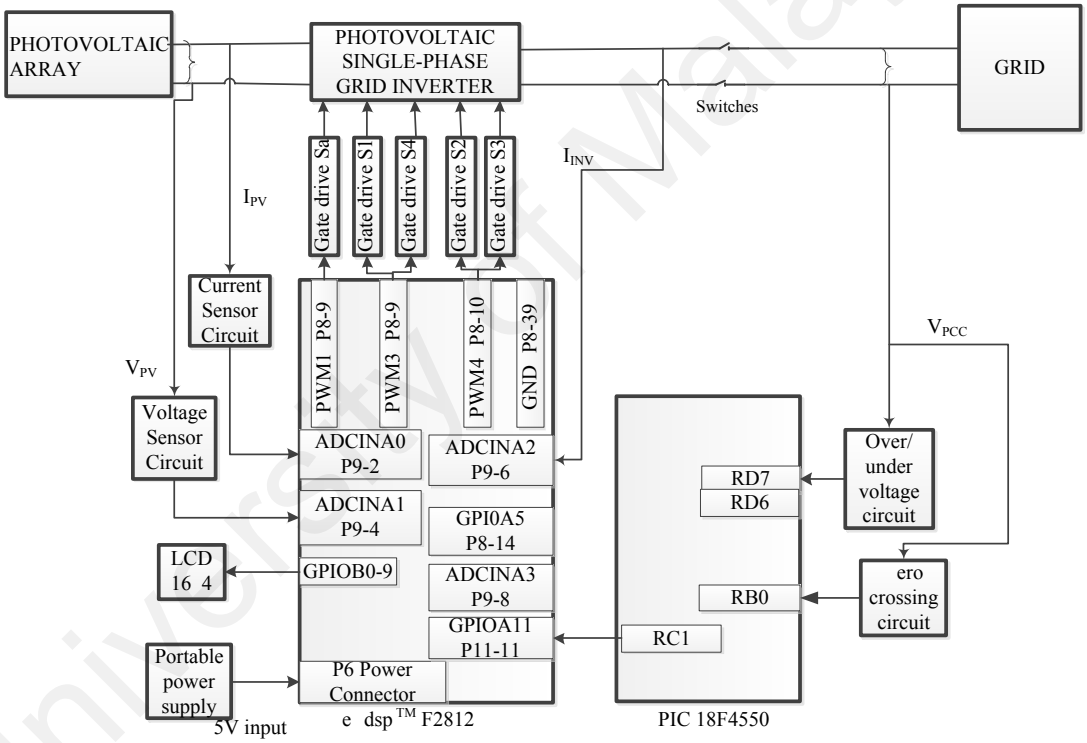


Figure 4.2: The grid-connected PV inverter system with PIC 18F4550 microcontroller

The proposed method takes the grid voltage to the under/over voltage circuit and send the signals as input to PIC18F4550 for under/over voltage detection. For under/over frequency, the proposed method detects zero crossing detection pulses and sends the signal as interrupt input to PIC18F4550. These signals are used as conditional detection in the developed islanding detection algorithm. The islanding detection algorithm output

from PIC18F4550 is input to the main inverter controller through GPI0A11, the input then used as a signal to turn off the relay, disconnecting the inverter from the grid.

4.3 Microcontroller PIC18F4550 with the proposed method

Figure 4.3 shows the hardware details of the proposed circuit connection using Proteus ISIS schematic simulation. The under/over voltage and under/over frequency circuits connect directly to the microcontroller. Reset system which consists of a reset button, a 4.7$k\Omega$ resistor and a 47pF capacitor is also included in this circuit. For faster performance, a 20MHz crystal is used as oscillator. In this work, RB0 was the interrupt input INT0 and connected to a zero crossing circuit. RD7 and RD6 were inputs to the under-/over voltage analog circuit. Pull-up resistors were turned on at Port D to ensure a 5V limit. All in Port C were used as outputs.

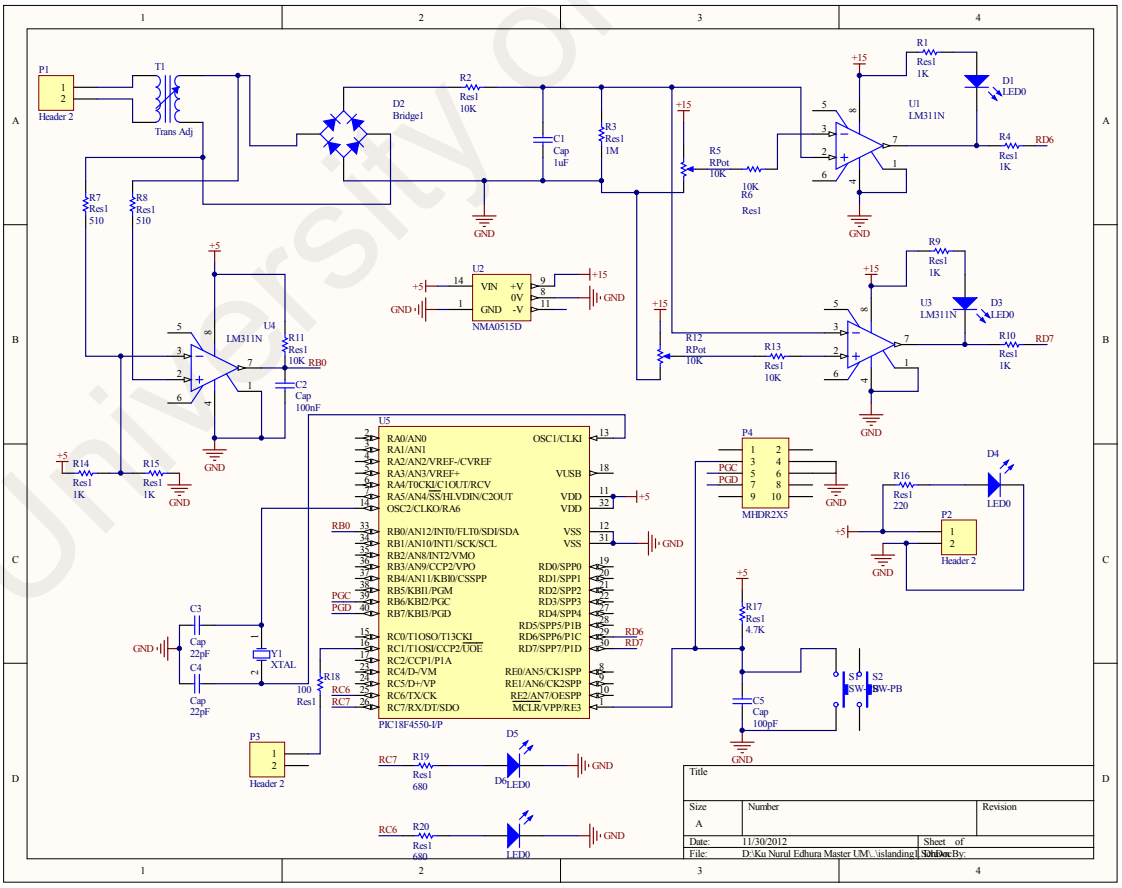


Figure 4.3: PIC 18F4550 Microcontroller with the proposed method

4.4 The proposed under voltage and over voltage circuit

Figure 4.4 shows the under and over voltage circuit of the proposed method.

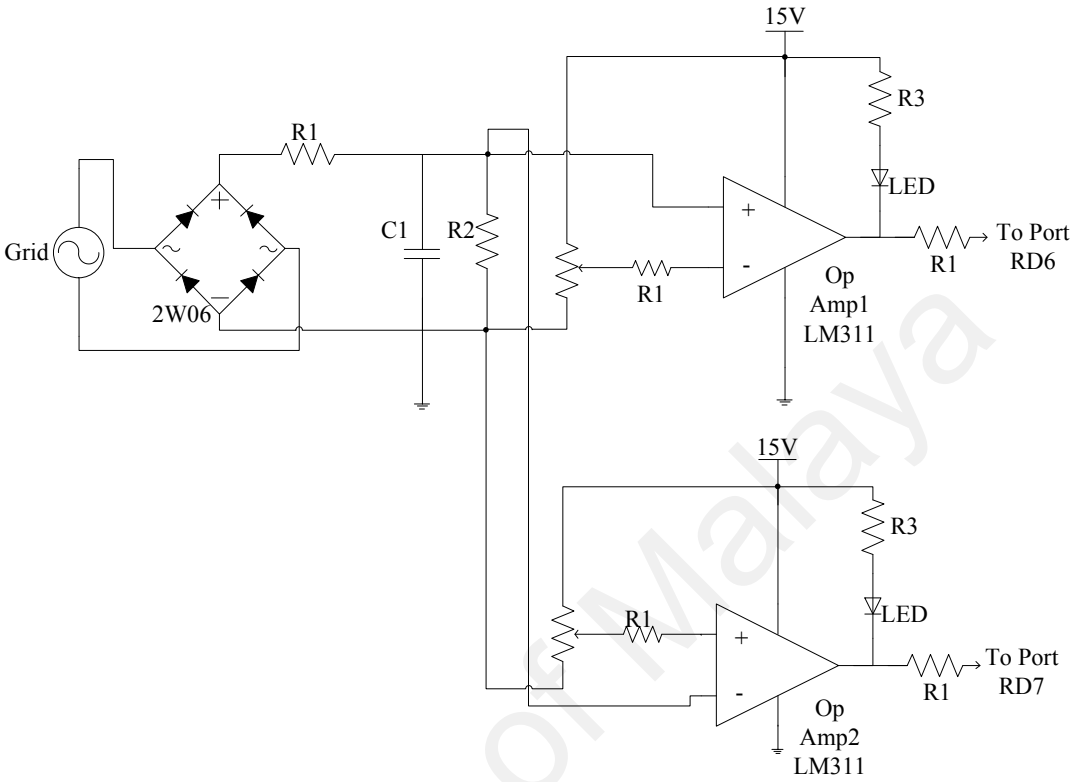


Figure 4.4: Under and over voltage circuit

PIC18F4550 was designed to read analog signals between 0V and 5V, hence the under/over voltage circuit was designed not to exceed that range. In this work, a 240V-6V transformer was connected to the utility source. A rectifier transforms the lower AC voltage into DC. Through the addition of resistor R2 parallel with capacitor C1, this circuit can convert a high voltage signal into a very stable low DC voltage signal. The stable DC signal then act as input to the under-voltage circuit which used the OpAmp1. A $10k\Omega$ potentiometer is used as tuner for reference voltage V_{ref1}. The value of the reference voltage V_{ref1} is being set according to the normal voltage range as per AS 4777.3-2005 standard. The DC voltage and reference voltage V_{ref1} are compared, with OpAmp1 acting as comparator. OpAmp1 output is fed to RD6 as input signal to the microcontroller. The same concept is applied to the over voltage circuit, except that the location of the reference

voltage is now at the positive side of OpAmp2 and the stable DC voltage now connects to the negative input of OpAmp2. This circuit was developed for accurate and fast detection of under/over voltage without continuous calculation of the grid voltage RMS as in the past method. Not only does detection become very fast, there is no added delay. Figure 4.5 shows the operating condition of the grid connected PV inverter at 240V RMS and 50Hz $\pm$ 2% frequency.

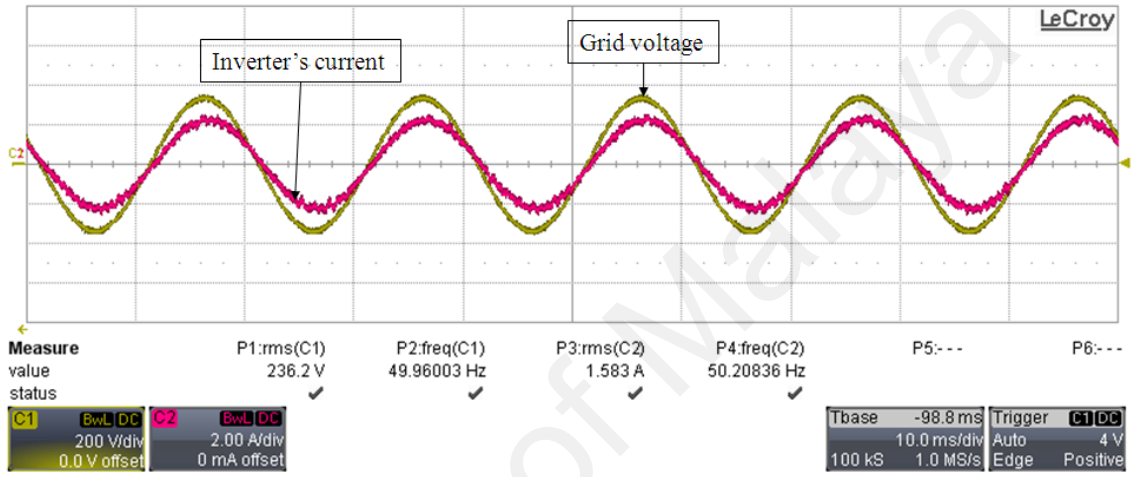


Figure 4.5: Normal condition at 240V and 50Hz: (C1) Grid voltage and (C2) Inverter's current

Figure 4.6 and Figure 4.7 show the under and over voltage islanding, condition where relays disconnect the inverter from the grid. For under voltage, the voltage is 228.6V RMS(The box in Figure4.6 and Figure 4.7 shows value of the grid voltage (RMS) before the inverter is disconnected). Meanwhile, for over voltage the voltage is 245.3V RMS (see Figure 4.7). In both condition, the frequency is maintained at 50Hz $\pm$ 2%.

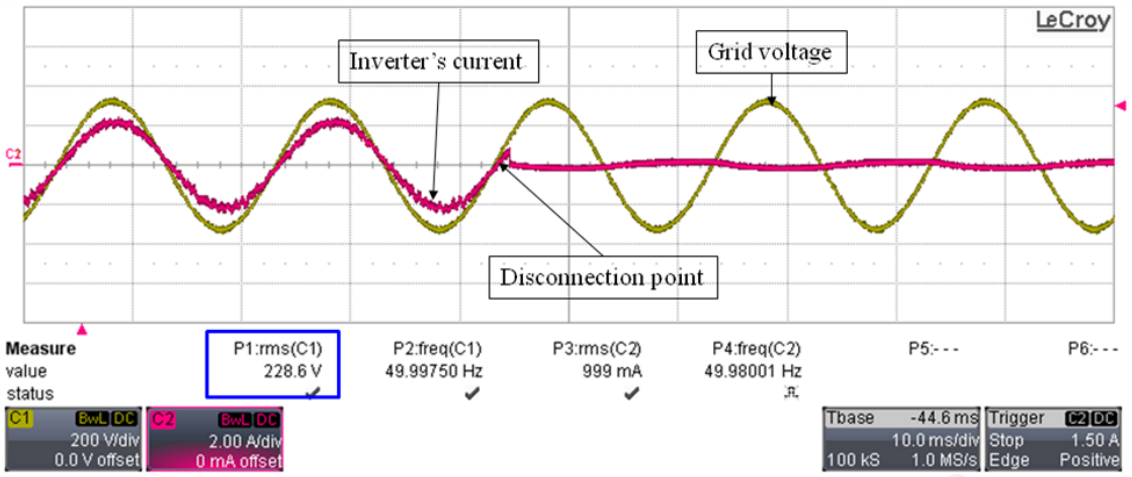


Figure 4.6: Under voltage islanding: (C1) Grid voltage and (C2) Inverter's current

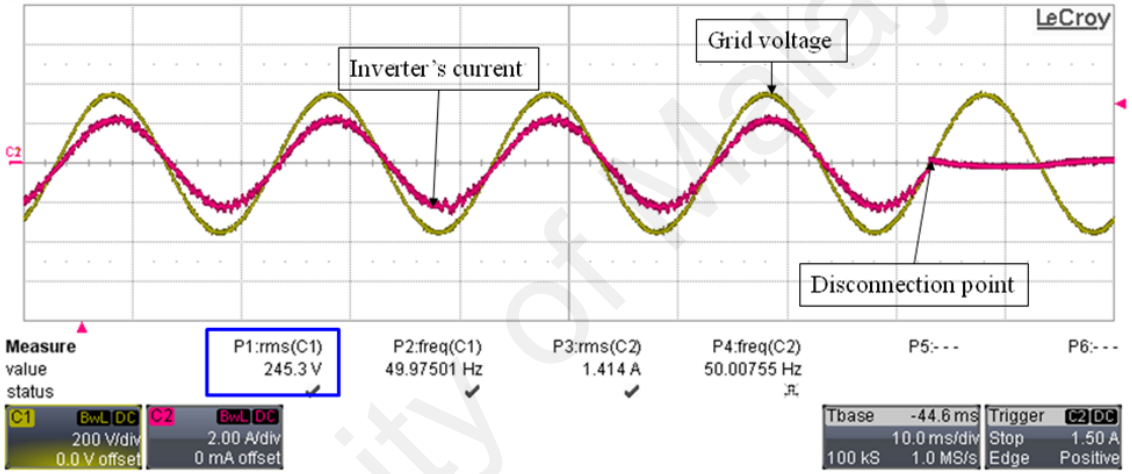


Figure 4.7: Over voltage islanding: (C1) Grid voltage and (C2) Inverter's current

4.5 The proposed under frequency and over frequency circuit

The circuit in Figure 4.8 is to ensure accurate and fast frequency detection with minimal external components. Resistor R1 forces the voltage down. Resistor pair R2 is a voltage divider, producing 2.5V as reference voltage to Op Amp LM311. The circuit output connects to RB0. Capacitor C1 connects to the Op Amp output to act as noise filter that gives the possibility to prevent noise in a simple and cost effective way. It improves triggering of the interrupt by reducing the noise in the low-voltage square-wave signals.As the square-wave signal is in phase with the grid voltage, the falling edge will indicate very accurately where the zero crossing is. This square wave signal will be the input to interrupt routine INT0, making possible the design of a zero-crossing-detection

routine in an interrupt routine and automatically making the detection fully interrupt-driven

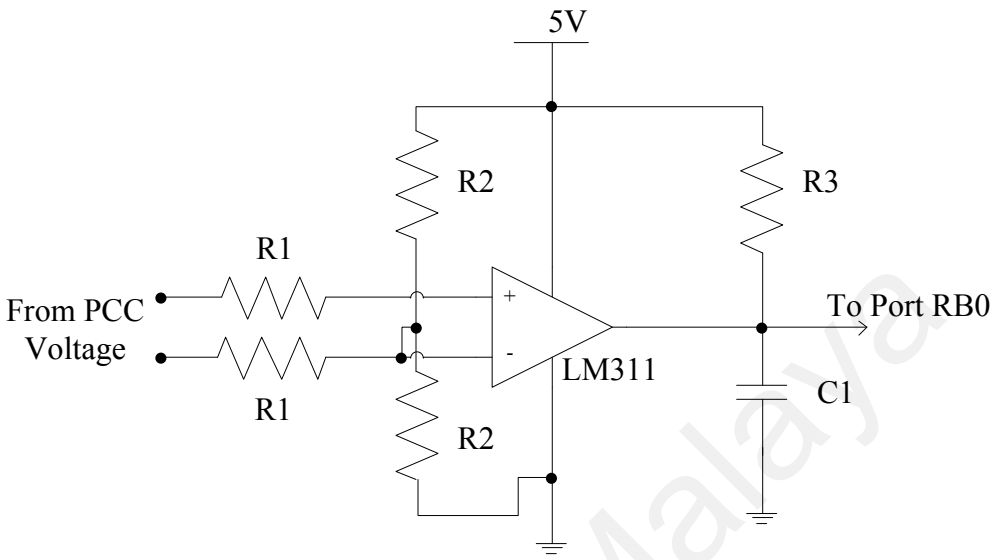


Figure 4.8: Zero crossing detector circuit for under and over frequency detection

Figure 4.9 shows a square-wave input signal and the triggered interrupt. Figure 4.10 and Figure 4.11 illustrate the over and under frequency islanding condition respectively. At this point, the voltage is maintained at 240V. For under frequency the frequency is at 48.4 Hz and over frequency is at 51.5Hz (see Figure 4.10 and Figure 4.11).

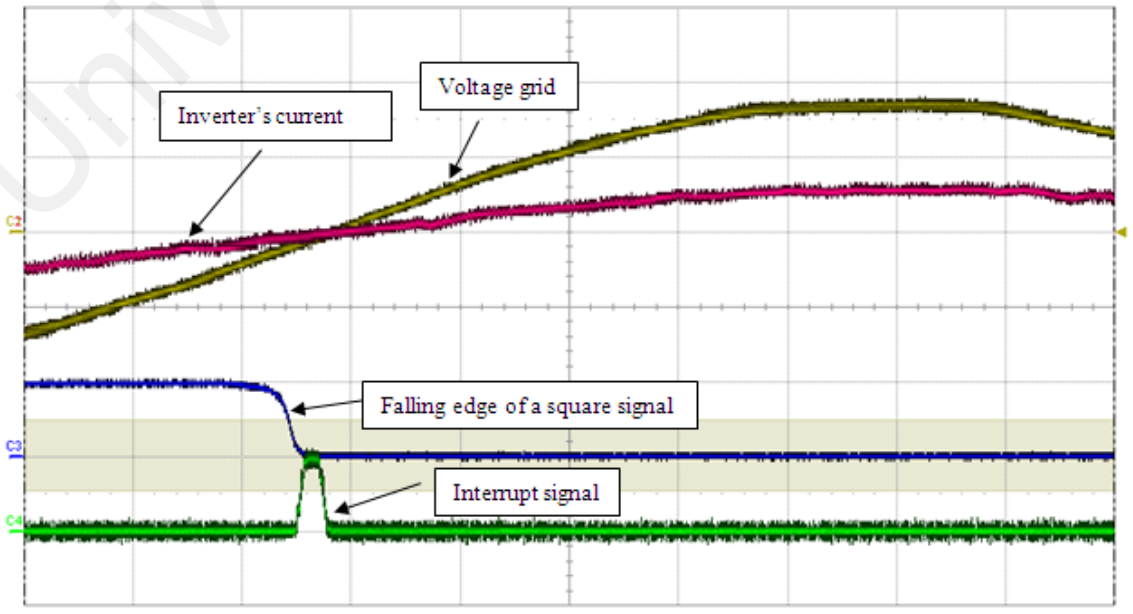


Figure 4.9: Falling edge of a square wave signal with the triggered interrupt

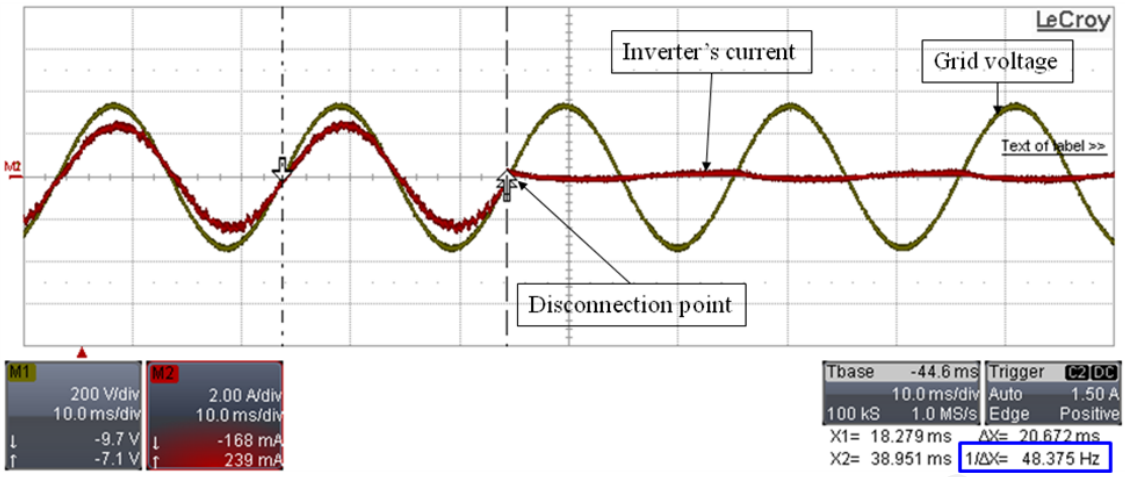


Figure 4.10: Under frequency islanding: (C1) Grid voltage and (C2) Inverter's current

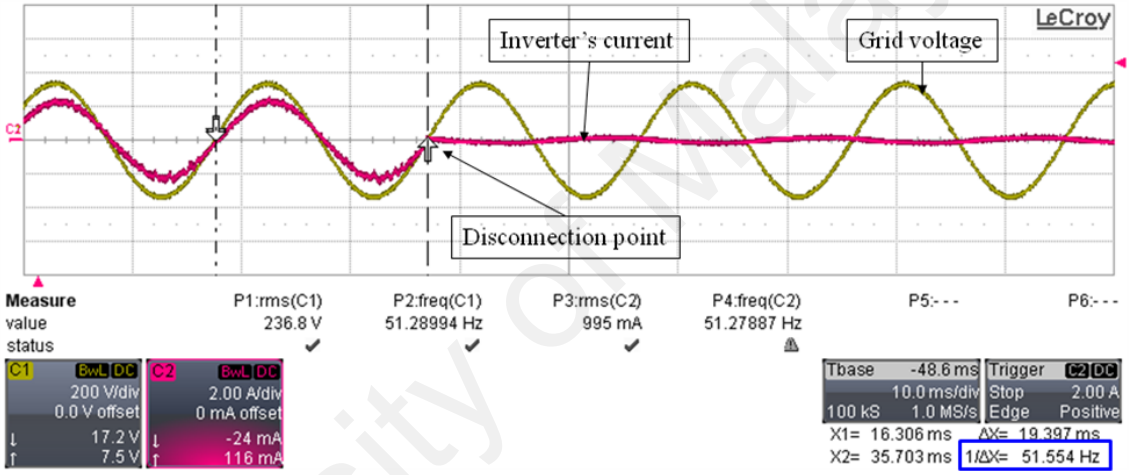


Figure 4.11: Over frequency islanding: (C1) Grid voltage and (C2) Inverter's current

4.6 Photovoltaic Array Simulator PVAS2

As provided by University of Malaya's Power Energy Dedicated Advanced Centre (UMPEDAC), a single string PV-Array Simulator PVAS2 is used for this project. Photovoltaic Array Simulator PVAS2 is part of a system to create the steady state and dynamic electrical behavior of photovoltaic arrays. It is intended to be used for test and research on PV inverter units as well as MPPT battery chargers. Through the flexibility of possible system settings, a wide range of test can be performed depending on the used measurement devices. The following are examples of the possible test:

- MPPT accuracy

- Maximum power point tracking (MPPT) behavior during changing irradiance conditions
- MPPT behavior on partially shaded arrays (local maxima)
- Power efficiency tests (Pout/Pin) at various operation conditions
- Inverter behavior on changing input voltage or current

All functions are controlled by the PVAS2 control VI, a Lab View application which gives comfortable access to all functions. Depending on the DC supply used, the PVAS2 control also allows to remotely control the functions of the DC supply, particularly to set its output voltage.

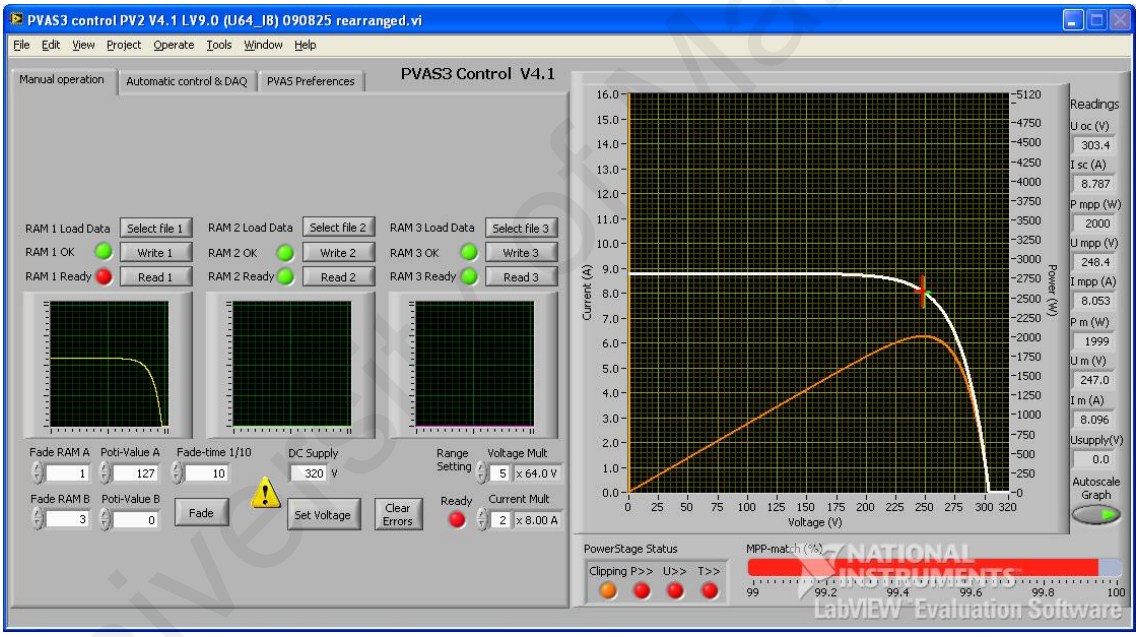


Figure 4.12: PVAS2 control GUI

The graphical user interface of the PVAS2 control software is divided into two parts (Figure 4.12 from left to right):

1. Control dialogue, containing three Tabs with manual and automatic control functions as well as a tab for setting the preferences.
2. State display, which shows the actual I-V curve and the current operating point of the device under test

With the window (tab) as shown in Figure 4.13, all direct hardware functions of the PVAS2 can be accessed. The main functions are setting the hardware scaling factors for voltage and current, writing to and reading I-V curves from the RAMs 1 to 3 and set fading levels and start fading with a specified time. Figure 4.13 shows the manual control tab in detail. The upper part of the window is the RAM control area and contains three similar areas representing the three RAMs integrated in the PVAS2 (RAM 1 to 3). The lower part is used for general controls. For this research, the output voltage of the DC supply of 320V is used. The range of the simulated PV voltage was at 5 x 64 V and simulated PV output current was at 2 x 8A. For all the experiments conducted, the poti-value A (for fading up and down the I-V curves stored in the RAMs) was set to 32 for 500W, 64 for 1000W, 96 for 1500W and 127 for 2000W inverter output power.

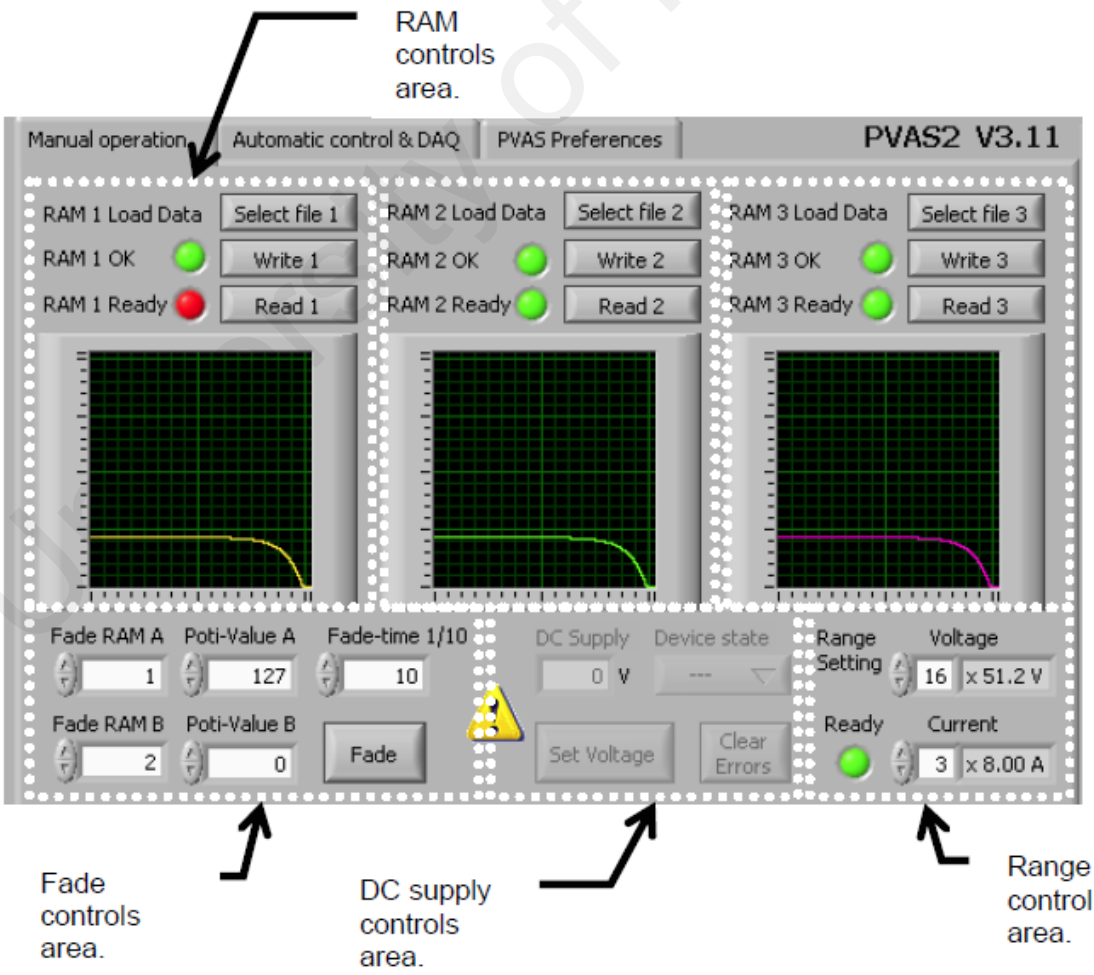


Figure 4.13: The manual operation tab in detail

4.7 Islanding Algorithm

Figure 4.15 shows the control algorithm of the proposed passive islanding detection, applied in PIC18F4550, which processes the algorithm through C programming language. PIC18F4550 collects analog inputs data from the under/over voltage circuit through RD7 and RD6. There is a filter in the programming algorithm to meet AS 4777.3-2005 standard reconnection time. The filter samples the signals 150 times for normal voltage condition which is 240V and compares the values to ensure stability. Only when the value is the same for all the samples, the event will proceed to the next procedure. This filter samples value can be changed according to the standard followed by researcher. For frequency calculation, a simple zero crossing circuit is utilized. The square wave produced by the zero crossing detector has the same frequency as the grid. By feeding the produced signal into the RB0 of the PIC18F4550, the microcontroller is programmed to be a very accurate zero crossing detector with an interrupt driven code. In this proposed algorithm, RC0 will be set high for a short period of time and then immediately start looking for the next falling edge zero crossing. Figure 4.14(a) shows RC0 going high for short periods of time at each falling edge zero crossing.

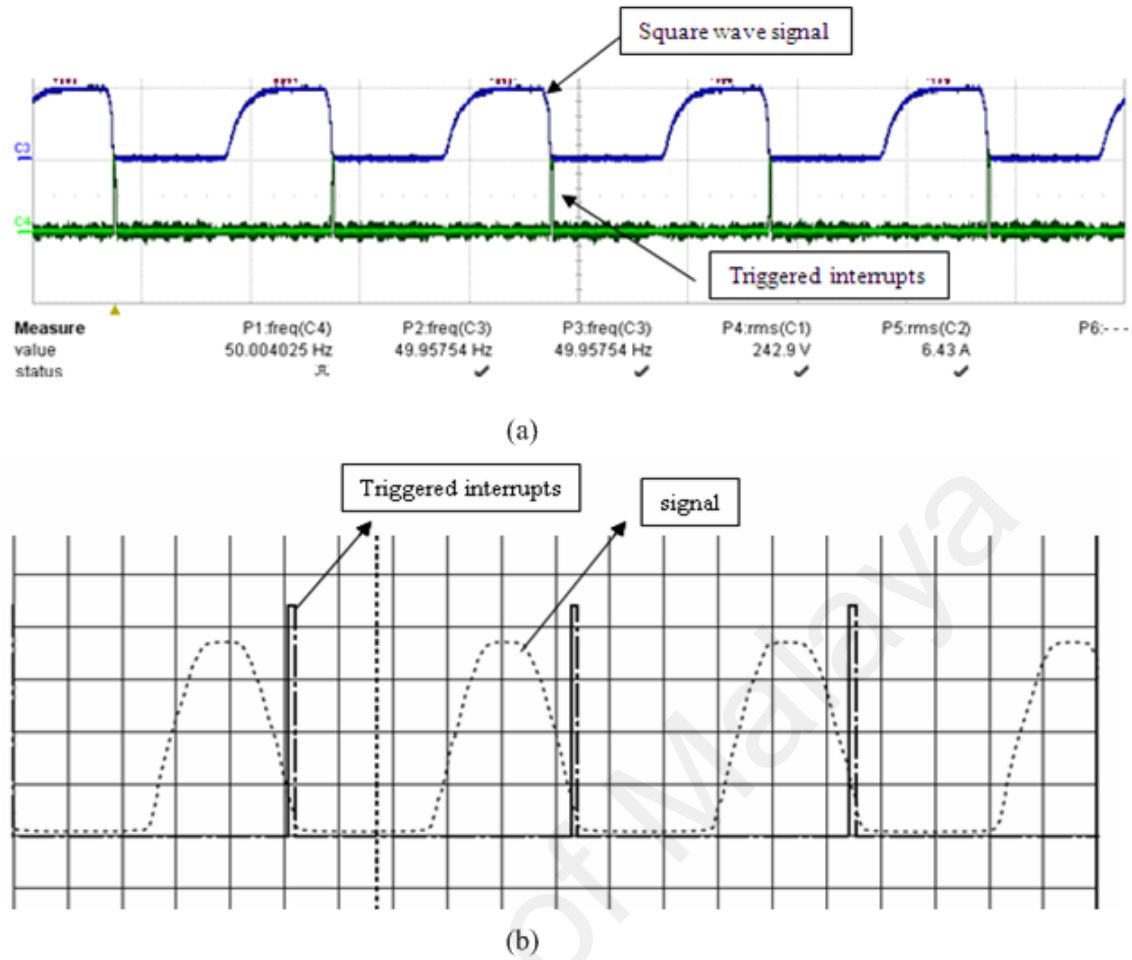


Figure 4.14: (a) RC0 going high for short periods of time at each falling edge zero crossing and (b) Screenshot from Proteus ISIS simulation of the zero crossing.

In order to make sure that the interrupts are valid and not only products of spikes on RB0, another filter (called noise filter) is implemented in the interrupt routine. The filter samples the level on the interrupt line 25 times and compares the values to ensure stability. If the value is not the same for all the samples, the event will be discarded and the routine returns to the main program waiting for new interrupt. Next procedure is toggling the light-emitting diode (LED). If LED is turned on, the timer is also on and vice versa. The value of the overflow counter is stored into the TMR0L and TMR0H memory. The obtained values from the memory are then compared with the standard constant frequency value. In order to set the standard constant frequency value, Port D is fully utilized to serve this purpose. TMR0H and TMR0L memory values are then transferred to Port D and the frequency value can be identified. If the compared values

from the memory are out of range from the constant, then microcontroller will trigger another filter. The under/over frequency filter samples the signals 3 times for under/over frequency and 150 samples for normal condition to ensure stability of the value. If the value is the same for all the samples, the routine will proceed to the next procedure. To further optimize the filter, the samples value can be changed according to the standard that one's require.

If the routine passed under/over voltage filter and under/over frequency filter, last stage is the confirmation stage before islanding signal is sent from PIC18F4550 to main inverter controller. The islanding signal will trigger main inverter controller to turn off the relay in order to disconnect the inverter from the grid. Table 4.1 described the subroutine of the proposed method.

Table 4.1: Subroutine of the proposed method

Subroutine name	Algorithm
Initialization/configuration	1. Set all pins to digital. 2. Set RB0 as input. 3. Set Port C as output. 4. Set RD7 and RD6 as input. 5. Clear all ports. 6. Clear the counter value.
Setup	1. Enable falling edge interrupt. 2. Enable external interrupt 1 on B0. 3. Turn on pull ups in Port D. 4. Active on falling edge. 5. Setting up Timer0. 6. Clear the TMR0H and TMR0L values.
Timer	1. Increment of the overflow counter. 2. Clear flag TMR01F.
Timer "OFF"	1. Set the over/under frequency values. 2. Reset the counter value. 3. Reset the TMR0H and TMR0L values. 4. Reset the INT0IF value.

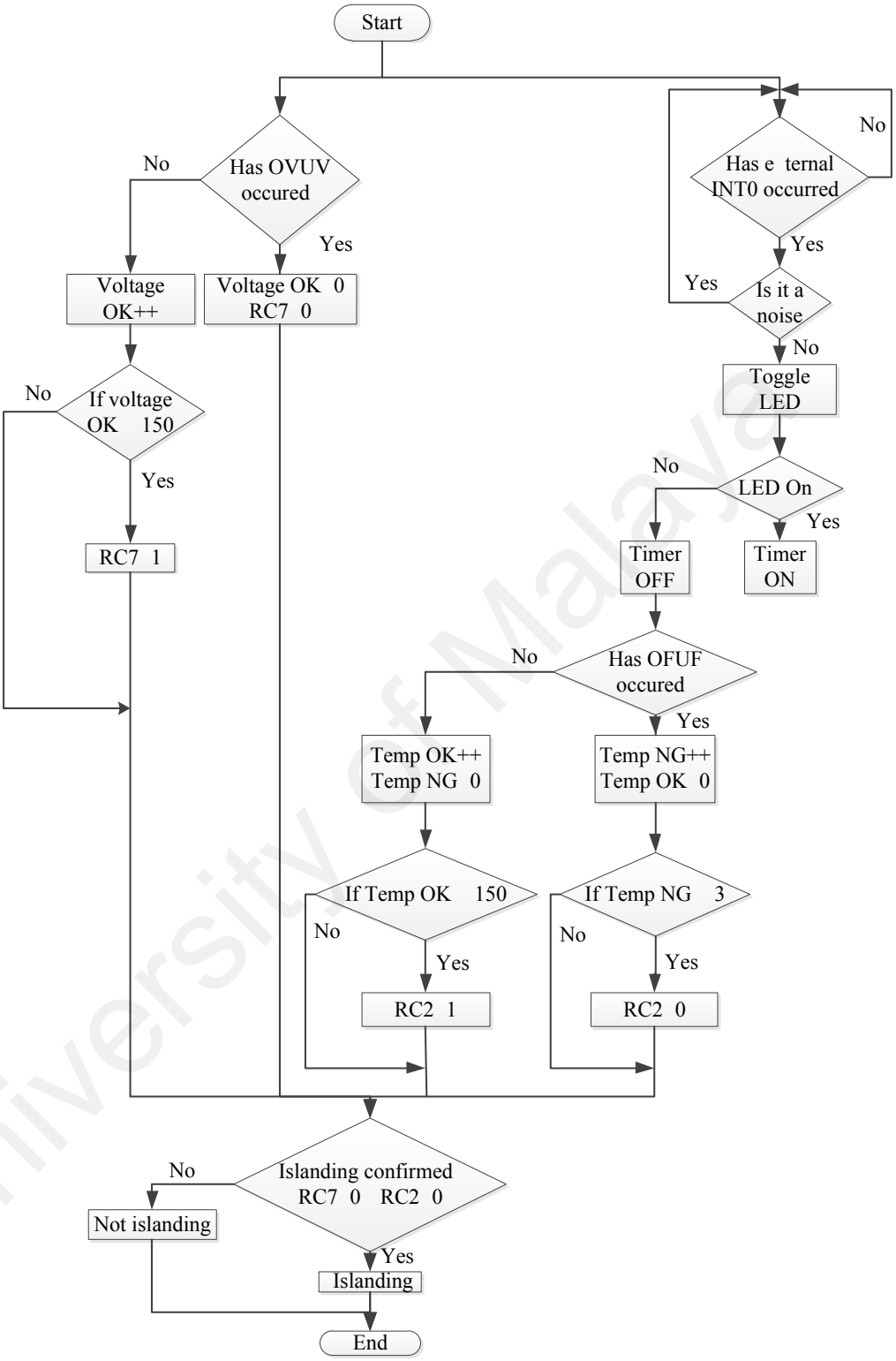


Figure 4.15: Islanding algorithm

Control algorithm of the proposed passive islanding method applied in the main inverter controller is shown in Figure 4.16. There is another waiting procedure before the inverter is connected to the grid. The value of GPI0A11 is monitored in order to turn the relay on or off. The complete programming in PIC can be viewed in Appendix A.

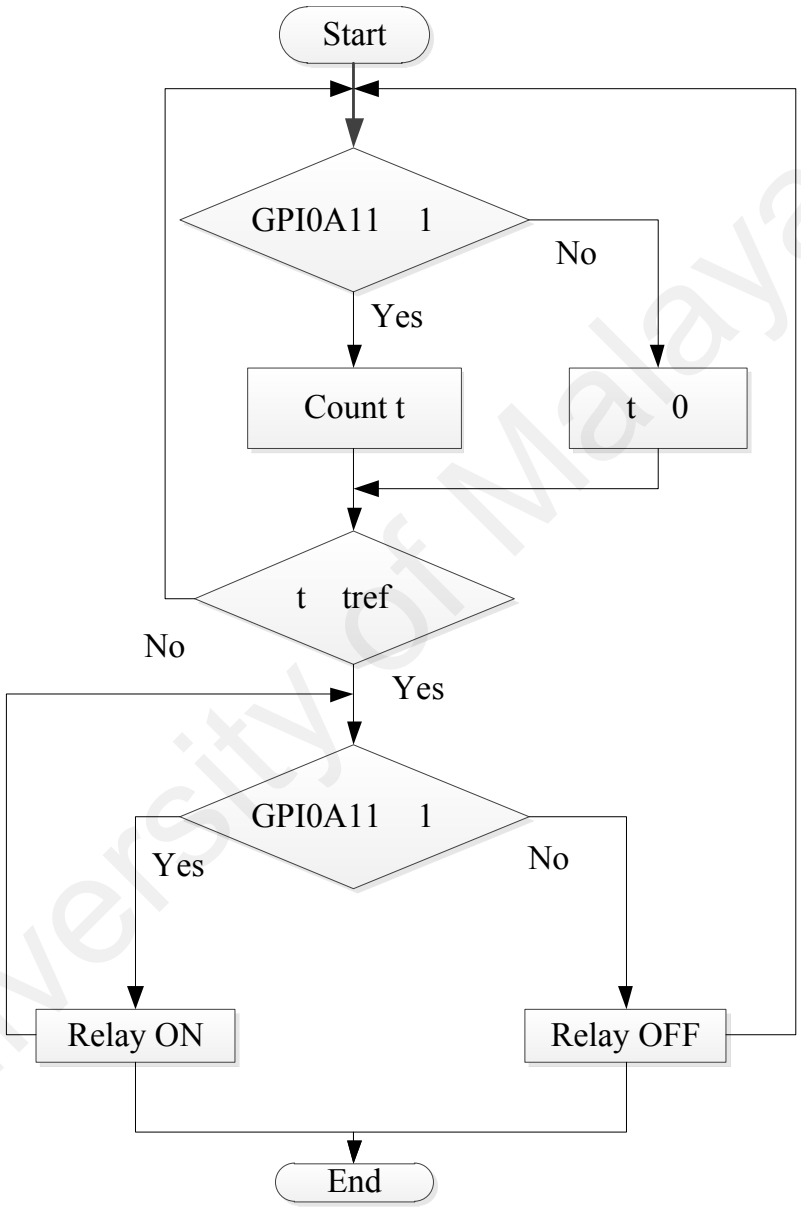


Figure 4.16: Algorithm in main inverter controller (TMS320F2812DSP)

4.8 PIC Software Development (MPLAB IDE)

The software development tool for PIC is called MPLAB IDE. The key feature of the MPLAB IDE is to serve the whole development chain. It supports programming in C language and Assembler. It is divided into three parts: the project list part, working areaand the output. The development flow of most PIC-based applications consists of four basic phases: application design, code creation, debug, and analysis/tuning. MPLAB IDE starts by clicking on the MPLAB IDE icon and control window will appear as in Figure 4.17.

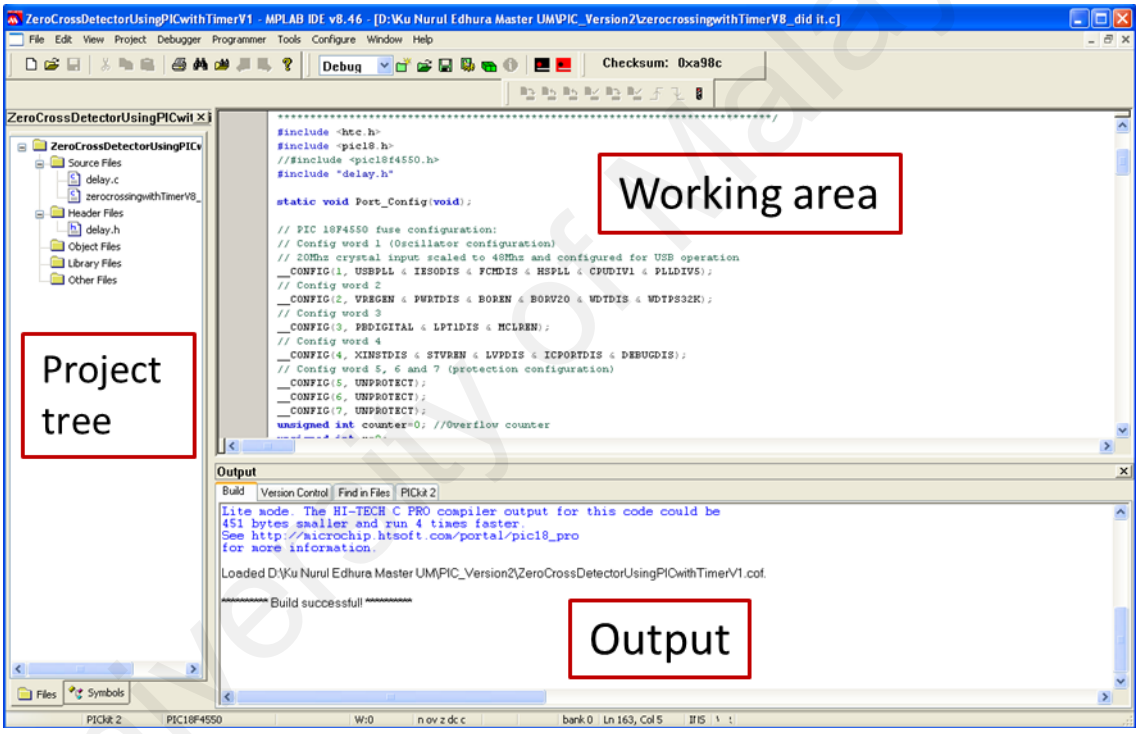


Figure 4.17: MPLAB IDE control window

On this MPLAB IDE control window, it can build, compile, load and run the project onto PIC. It has real time mode function that can monitor the value of the parameters in real-time while running the experiment. The following Figure 4.18 shows further procedure on how to develop, build and run a program code in MPLAB IDE environment.

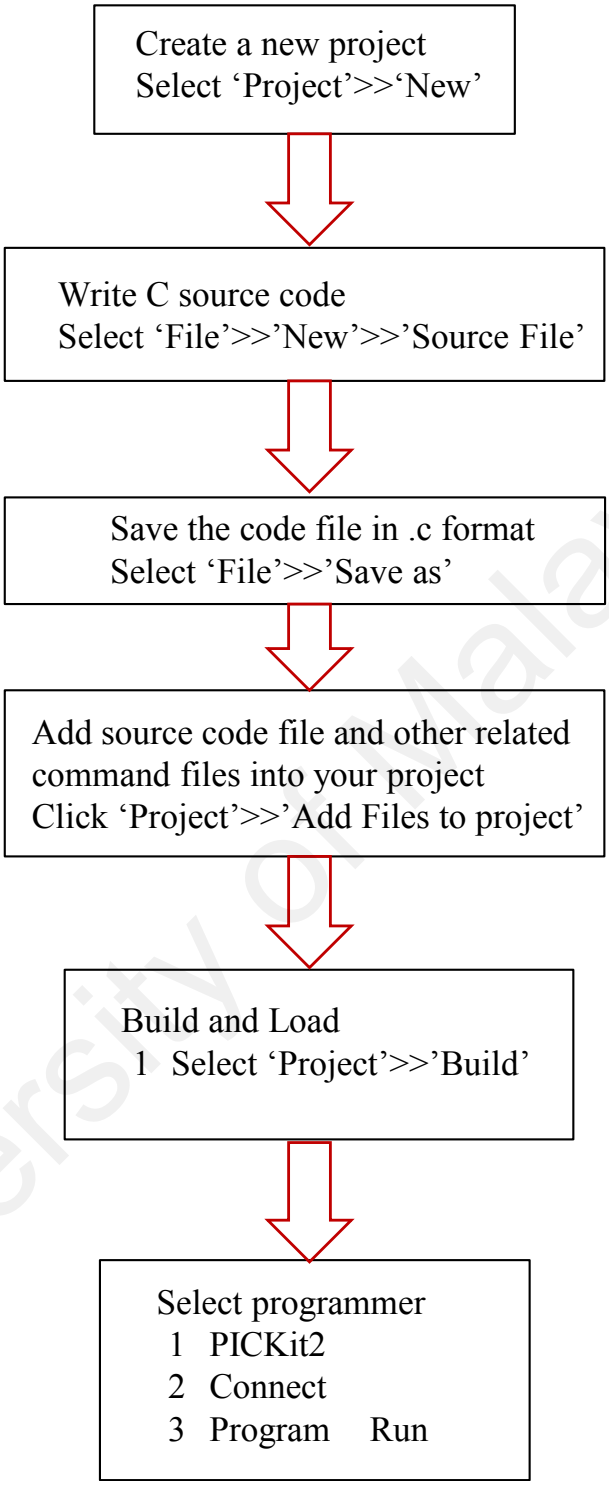


Figure 4.18: Develop, build and run a program code in MPLAB IDE

CHAPTER 5

Simulation and Experiment Results

5.1 Introduction

As mentioned in Chapter 3, the None Detection Zone (NDZ) for the proposed method can be mapped as Figure 5.1 below. The under voltage (UV) / over voltage (OV) and under frequency (UF) / over frequency (OF) of the proposed method were set according to AS 4777.3-2005 standard (Please refer to section 4.4 and 4.5 for the exact values).

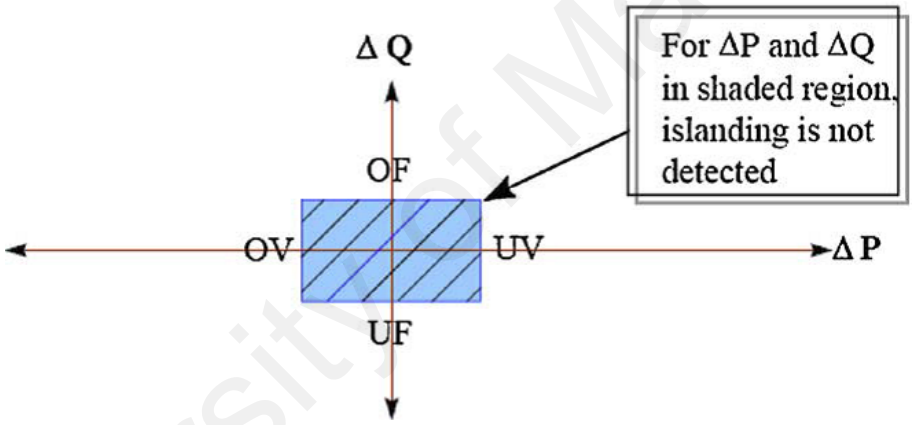


Figure 5.1: NDZ mapping in ΔP versus ΔQ space for the proposed method

5.2 Simulation Results

Figure 5.2 shows the simulation of the proposed method using PSIM system. The DC voltage source was 400V, the grid voltage 240V, the grid frequency 50Hz, and the output filter inductance 5mH. The inverter was designed for 2kW power output. The RMS current injected into the grid was 8A. The main parameters of the simulation were as those of the experiments. The inverter was loaded by a parallel R-L-C circuit with quality factors 1, 2, and 2.5. Islanding is applied after 0.3 seconds of the simulation.

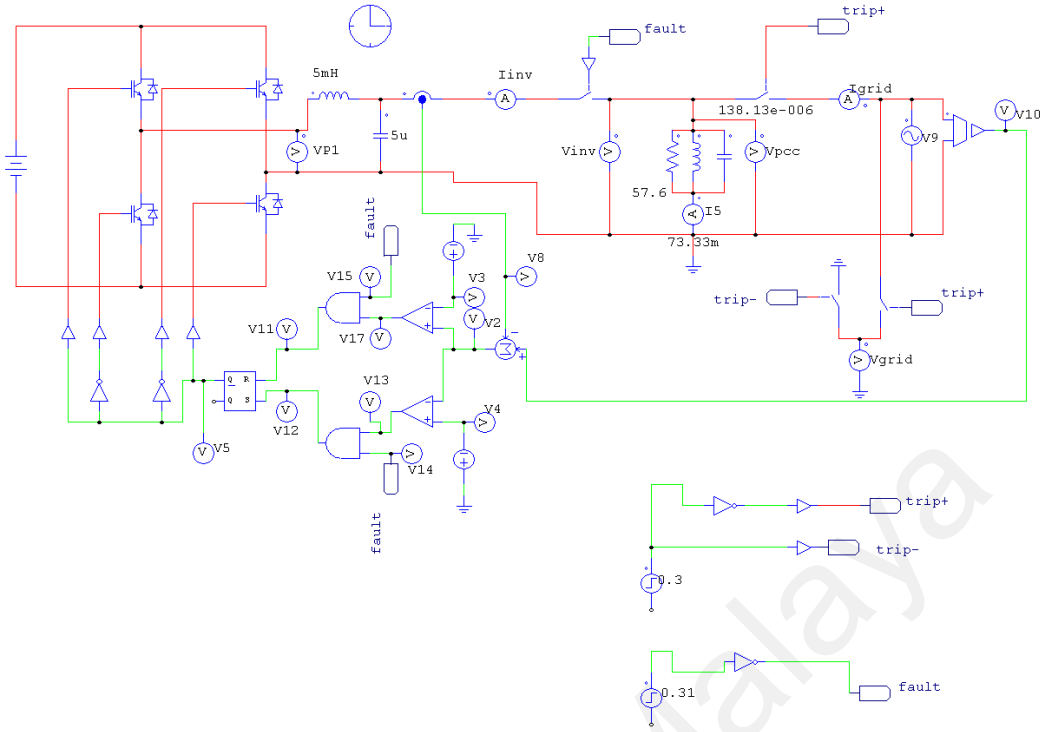


Figure 5.2: Simulation

For Figure 5.3, the inverter was simulated to produce 500W (25%) output power with 2A of RMS current injected into the grid. The inverter was loaded with a pure resistive load R of 57.6Ω. Simulation for R load with 1kW (50%) inverter output power under islanding operation produced an output Vpcc and inverter current waveforms as in Figure 5.4. Waveform of produced inverter current is at unity power factor with the grid voltage. The scale of inverter current waveform is enlarged to be 10 times. The injected RMS current to the grid is 4A. Figure 5.5 and Figure 5.6 respectively show the output V_{PCC} and inverter current waveforms for R load with 1.5kW (75%) inverter output power and R load with 2kW (100%) inverter output power under islanding operation. The injected RMS current to the grid for 1.5kW and 2kW are 6A and 8A respectively. In the following simulations, the grid connected inverter will be tripped off when islanding is detected.

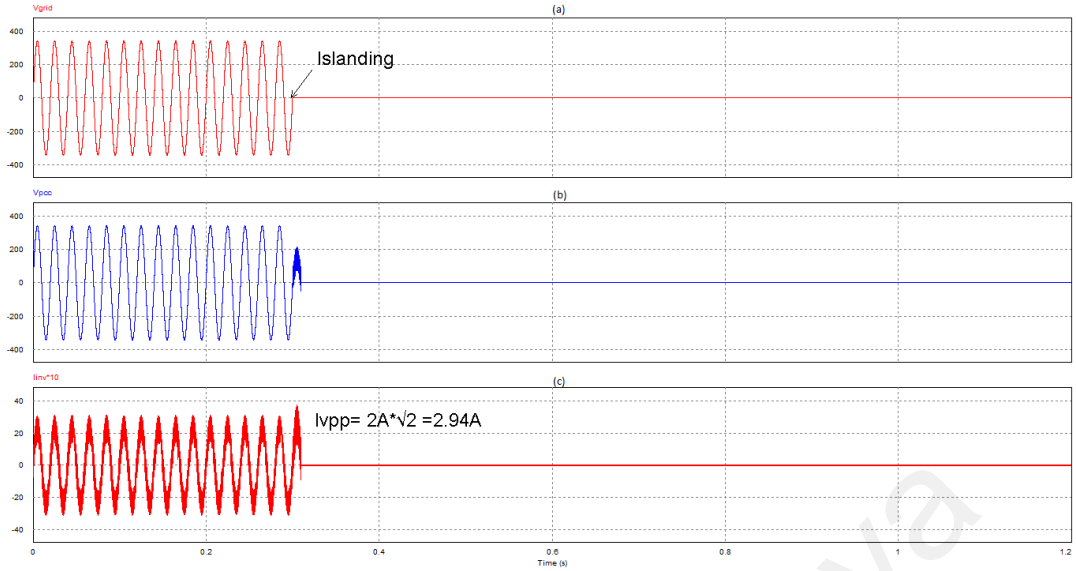


Figure 5.3: Simulation result for R load with 25% (500W) inverter output under islanding operation with (a): V_{grid}, (b): V_{PCC}, and (c): I_{inv}*10

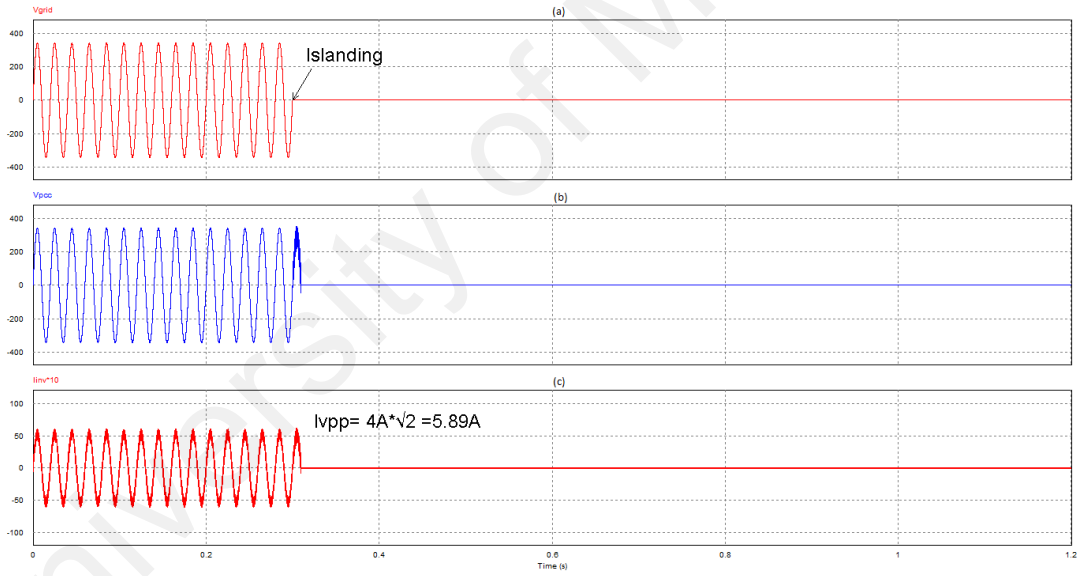


Figure 5.4: Simulation result for R load with 50% (1kW) inverter output under islanding operation with (a): V_{grid}, (b): V_{PCC}, and (c): I_{inv}*10

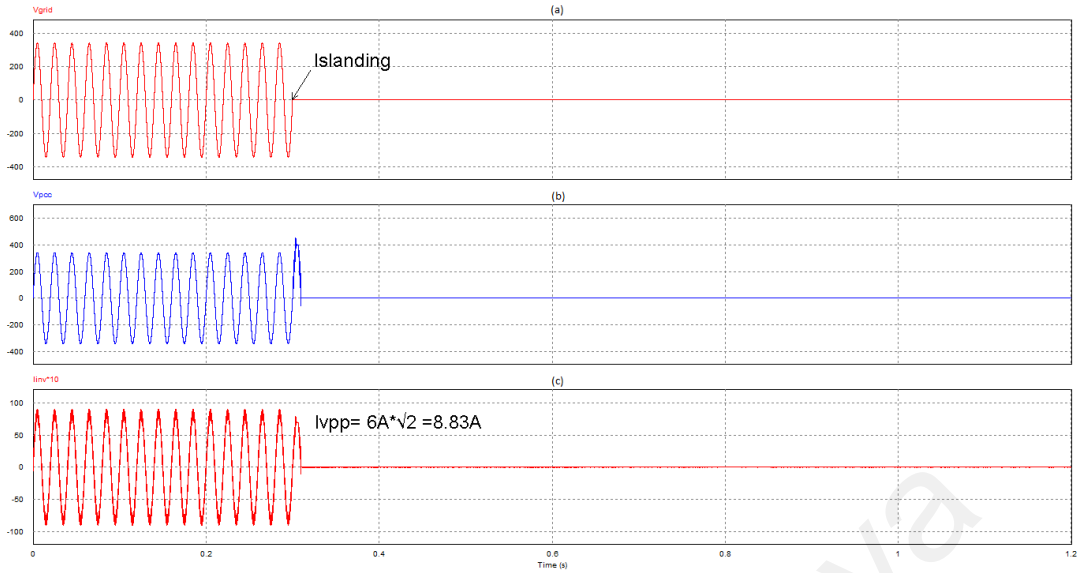


Figure 5.5: Simulation result for R load with 75% (1.5kW) inverter output under islanding operation with (a): V_{grid}, (b): V_{PCC}, and (c): I_{inv}*10

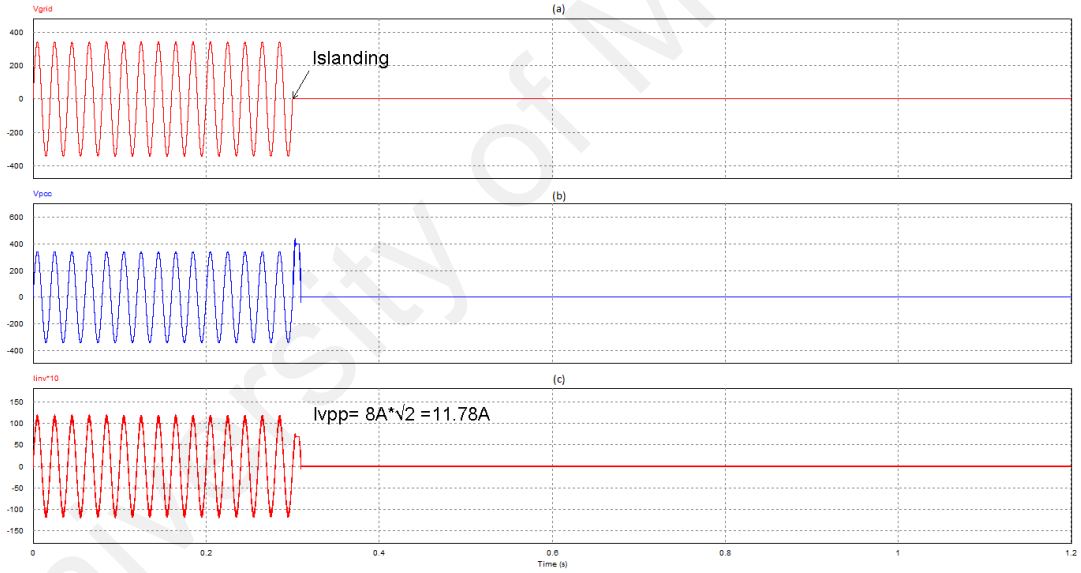


Figure 5.6: Simulation result for R load with 100% (2kW) inverter output under islanding operation with (a): V_{grid}, (b): V_{PCC}, and (c): I_{inv}*10

From the simulation results (Figure 5.3, Figure 5.4, Figure 5.5 and Figure 5.6), it can be concluded that the ratio of inverter's output and load consumption can affect the amplitude of the load voltage (V_{PCC}).

Figure 5.7 shows the simulation result for R-L under islanding operation with 1kW inverter output power. The inverter output current is almost the same for both simulation and experiment results (see Figure 5.7 and Figure 5.17). From the simulation result for

R-L load under islanding condition, the value of the maximum inverter output current before inverter is tripped off is 7.08A and 5.7A from the experiment (see Figure 5.17). Table 5.3 lists the load parameters of the simulations.

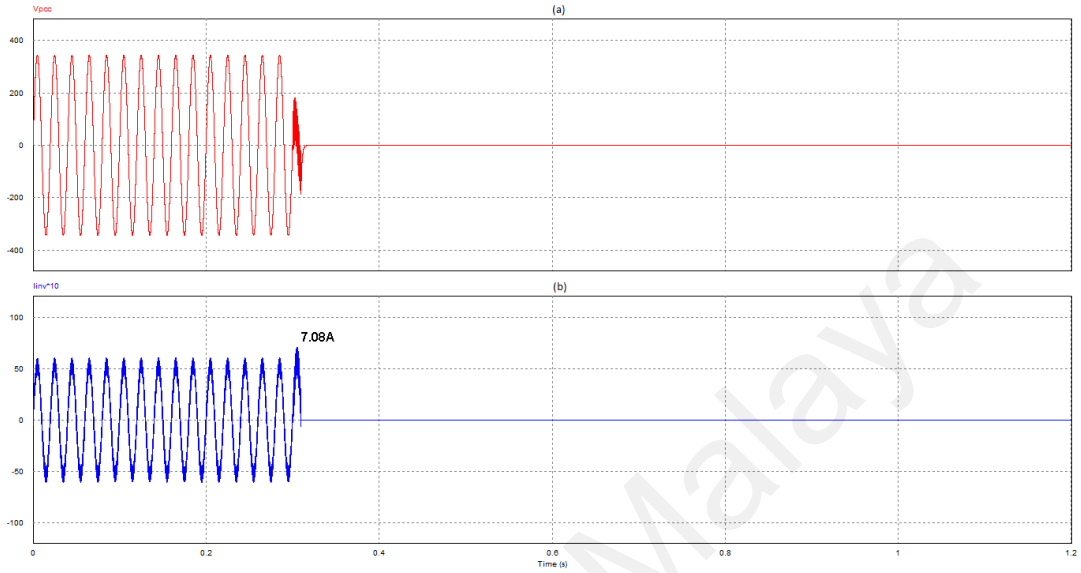


Figure 5.7: Simulation result for R-L load under islanding operation with Q=2.5 and P=1kW with (a): V_{PCC}, and (b): I_{inv}*10

Figure 5.8 shows the simulation result for R-C under islanding operation with 1kW inverter output power. The V_{PCC} voltage is almost the same for both simulation and experiment results (see Figure 5.8 and Figure 5.18). From the simulation result for R- C load under islanding condition, the value of V_{PCC} voltage before inverter is tripped off is 160V and 216V from the experiment (see Figure 5.18).

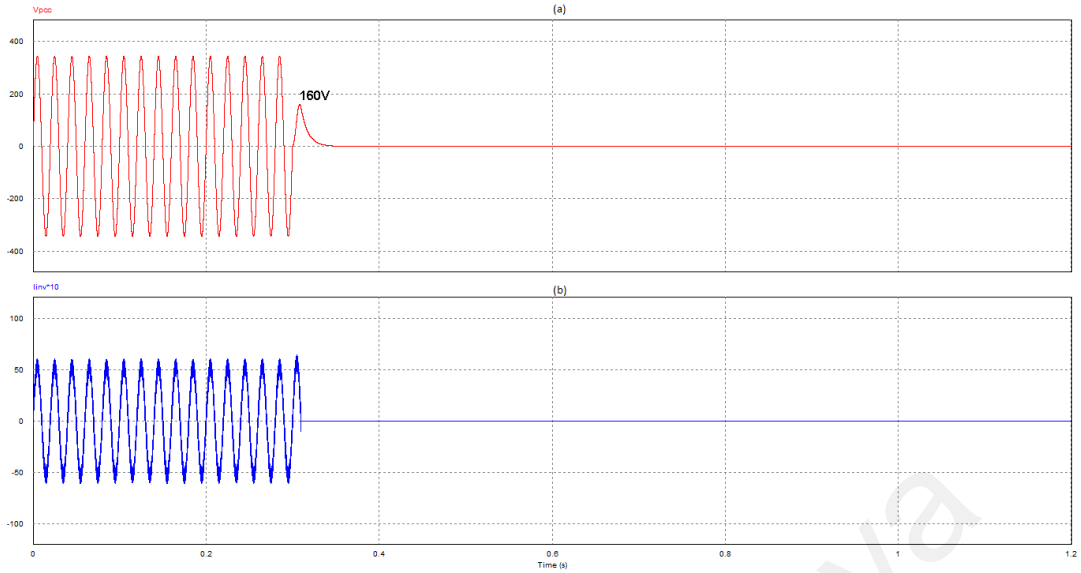


Figure 5.8: Simulation result for R-C load under islanding operation with Q=2.5 and P=1kW with (a): V_{PCC}, and (b): I_{inv}*10

Figure 5.9, Figure 5.10 and Figure 5.11 show the voltage of point of common coupling V_{PCC}, inverter's current and voltage and grid current and voltage for Q = 1, 2 and 2.5 (see Table 5.4) ideally when the inverter is tripped off. The experiment results (Figure 5.19, Figure 5.20 and Figure 5.21) have supported below simulation results where it can be concluded that different quality factors of R- L- C load can affect the amplitude of the load voltage (V_{PCC}).

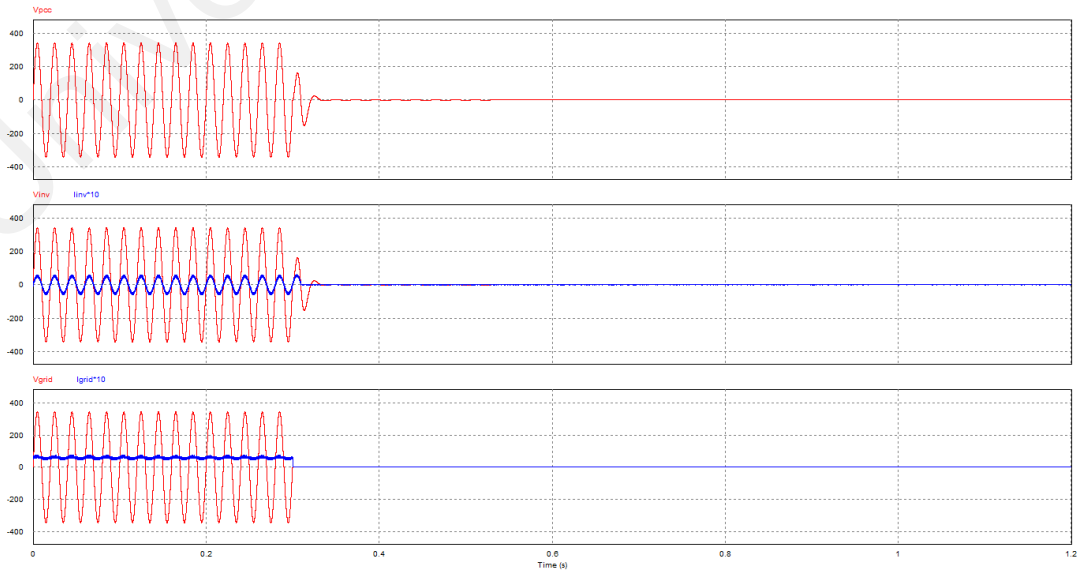


Figure 5.9: Simulation result under islanding detection at Q=1

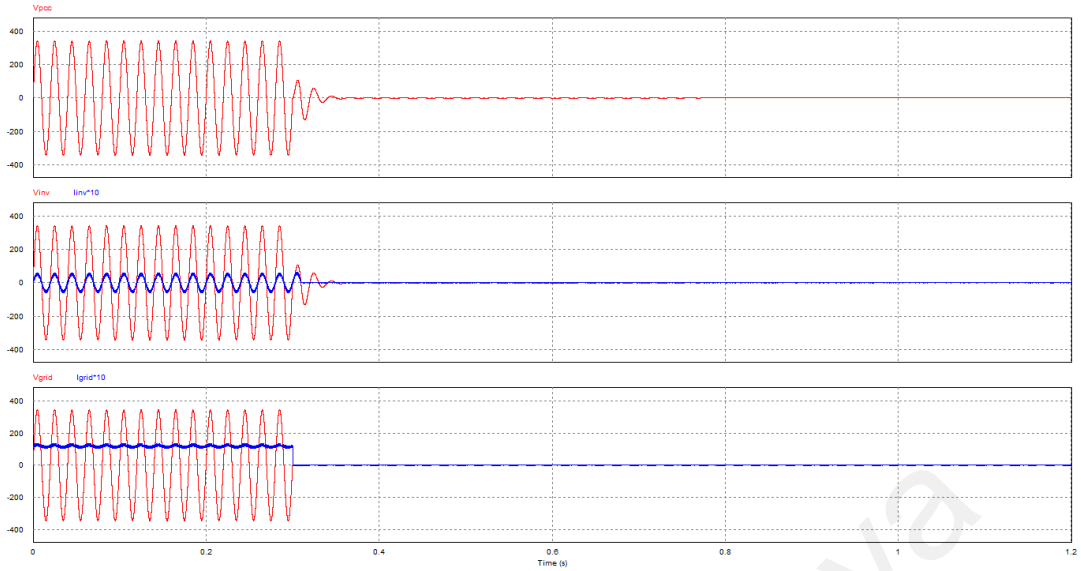


Figure 5.10: Simulation result under islanding detection at Q=2

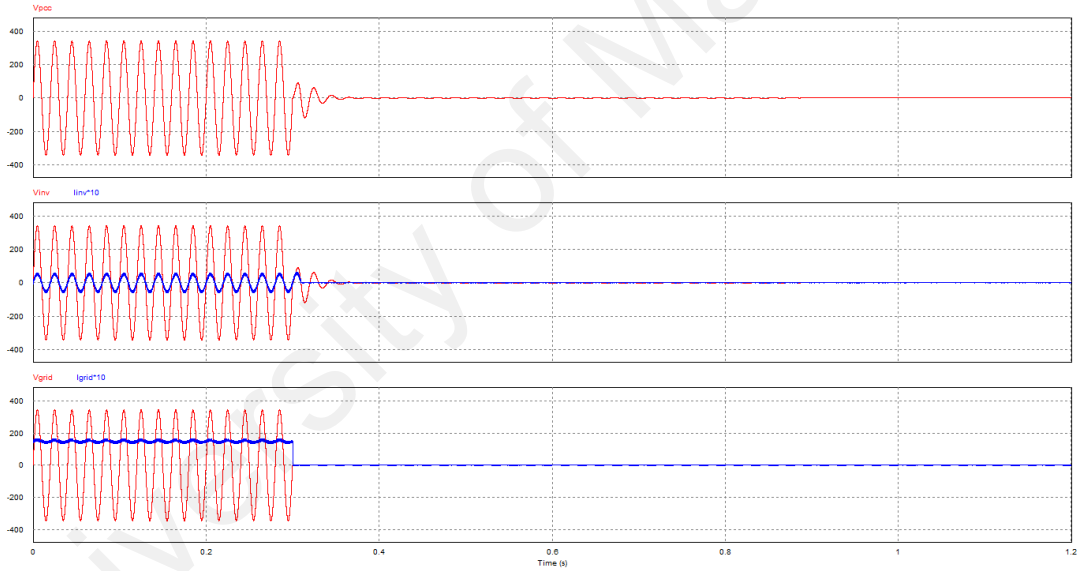
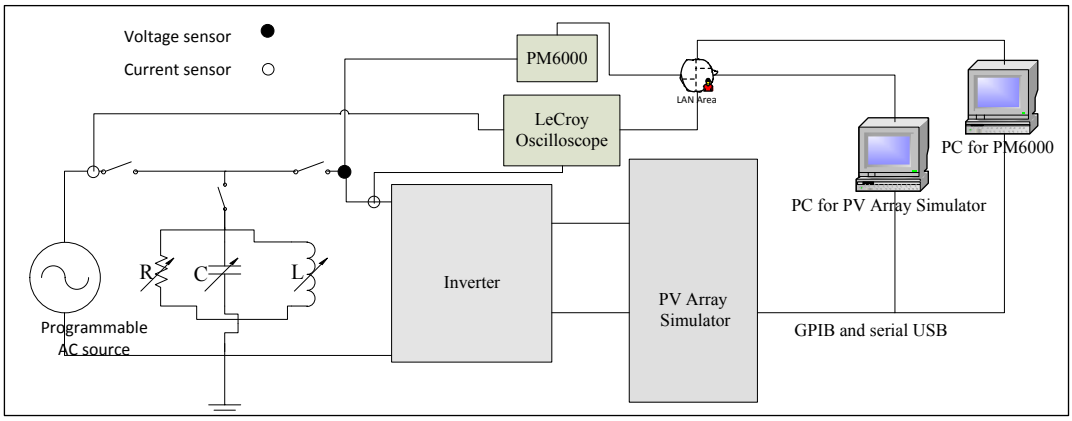


Figure 5.11: Simulation result under islanding detection at Q=2.5

5.3 Experiment results

Figure 5.12 shows the PV grid-connected inverter hardware prototype controller interface with the anti-islanding detection, implemented on PIC 18F4550 to validate the performance of the proposed passive islanding detection algorithm.



a

b

Figure 5.12: (a) Islanding test and (b) the laboratory test equipment with the proposed passive islanding detection method

Table 5.2 lists the prototype parameters of the single phase grid-connected PV inverter. The hardware was tested under various load conditions. Equipment such as PV array simulator, resistor-inductor-capacitor (R-L-C) load, programmable AC source, PM6000, and LeCroy Oscilloscope were used. The details of each parts and parameters are described further in Table 5.1. The test was conducted from 500W to 2kW power output. In the following experiments, the grid-connected inverter was controlled to generate balanced real power with the load. Various load types were used to verify the proposed islanding detection method. Table 5.4 lists the load parameters of the experiments. The parameters of the resistor-inductor-capacitor (R-L-C) load were as specified by the IEEE Std. 929-2000 (*IEEE Recommended Practice for Utility Interface of Photovoltaic (PV) Systems*, 2000) for testing islanding operation performance. IEEE Std. 929-2000 states

that a non-islanding inverter must shut down within 2 seconds of grid disconnection for loads with a quality factor (Q_f) equals to or lower than 2.5. The values for L and C are calculated through this formula:

$$P = \frac{V^2}{R} \tag{5.1}$$

$$L = \frac{R}{Q_f \times \omega} \tag{5.2}$$

$$C = \left(\frac{Q_f}{R}\right)^2 \times L \tag{5.3}$$

Table 5.1: Prototype part's name, value and manufacturer

Part	Part Name	Value	Manufacturer
R	Three Phase Variable Resistive Load	EM-26-01-12K	-
L	Variable Inductor	3kVAr 50/60Hz MV1107	Terco
DSP	eZdspTMF2812	-	Texas Instrument
C	Variable capacitor	-	UMPEDAC
AC Source	Programmable AC source Model 6560	-	Chroma
PM6000	Power Analyzer	-	Voltech
Oscilloscope	Lecroy WaveRunner 64Xi-A	600MHz Oscilloscope 10GS/s	LeCroy
PV Array simulator	Single string PV-Array Simulator PVAS2	-	Arsenal research

Table 5.2: Parameters of the single-phase grid-connected PV inverter prototype

Parameter	Value
D_1	RHRP30120 V_{RR} = 1200V, I = 30A
$S_1 - S_4$	IGBT IRG4PH50UD V_{CE} = 1200, I_c = 24A
Filter inductor (L_f)	5mH
Switching Frequency	20kHz

Table 5.3: Load parameters of the simulation and experiment at Q=2.5 and P=1kW

Types	R	L	C
Pure resistor load	57.6Ω	-	-
Resistor-inductor load	57.6Ω	73.33mH	-
Resistor-capacitor load	57.6Ω	-	138.13μF
Resistor-inductor-capacitor load	57.6Ω	73.33mH	138.13μF

Table 5.4: Load parameters of the simulation and experiment at Q=1, 2, 2.5, and P=1kW

Quality factor	R	L	C
1	57.6Ω	183.35mH	55.26μF
2	57.6Ω	91.67mH	110.52μF
2.5	57.6Ω	73.33mH	138.13μF

The grid system was first connected to the inverter and then removed to create islanding. Figure 5.13, Figure 5.14, Figure 5.15 and Figure 5.16 give the different inverter outputs: 25%, 50%, 75% and 100% with pure resistive load under islanding condition. From the experiment results, the injected RMS current (I_{inv}) for resistive R load under islanding operation for 25% (500W) inverter output power is 1.367A (see Figure 5.13). Meanwhile, the injected RMS current (I_{inv}) for resistive R load under islanding operation for 50% (1kW), 75% (1.5kW) and 100% (2kW) inverter output powers are 2.694A (See Figure 5.14), 4.06A (See Figure 5.15) and 5.17A (See Figure 5.16) respectively. The results conclude that the ratio of the inverter's output and load consumption can affect the amplitude of the load voltage (V_{PCC}).

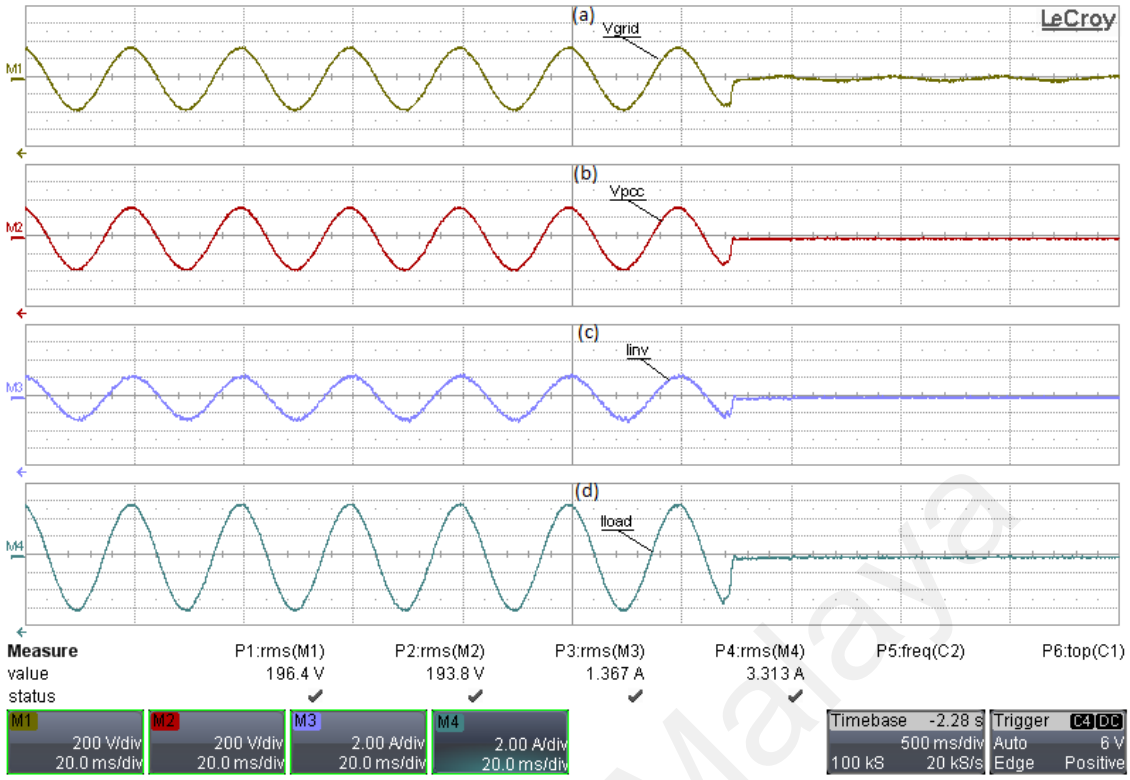


Figure 5.13: Experiment result for resistive R load under islanding operation for 25% (500W) inverter output with (a):(M1) V_{grid}, (b):(M2) V_{PCC}, (c):(M3) the inverter output current and (d):(M4) load current

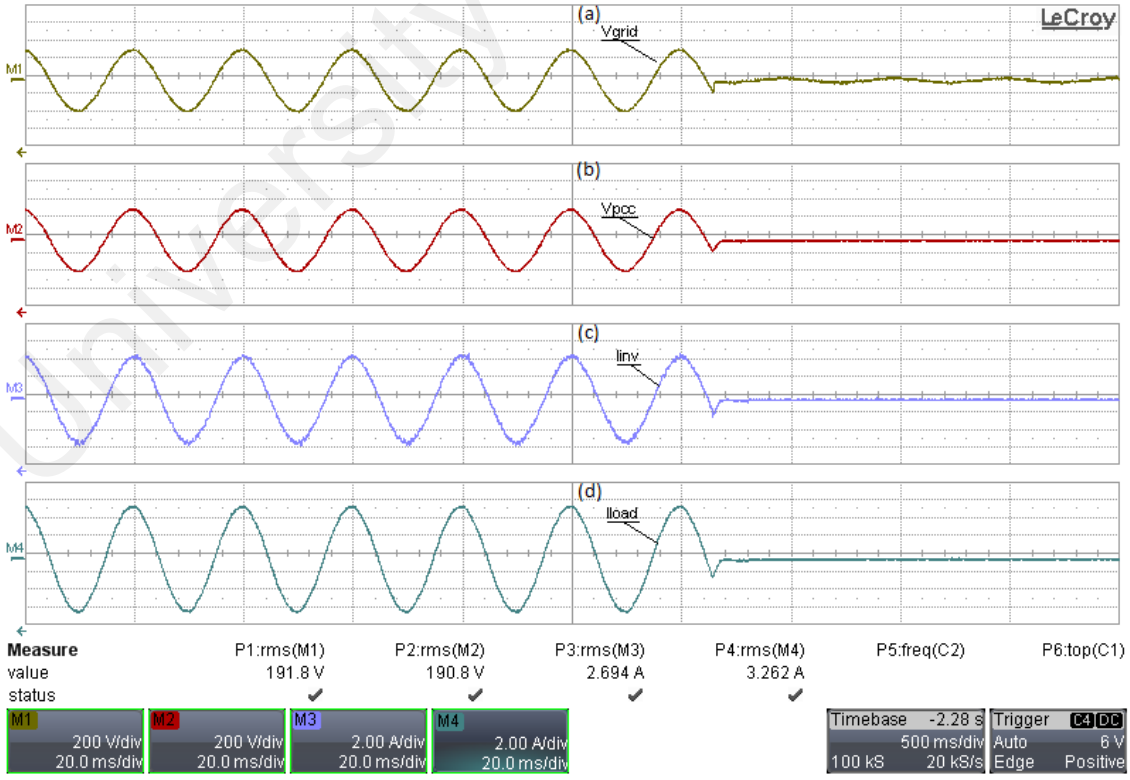


Figure 5.14: Experiment result for resistive R load under islanding operation for 50% (1kW) inverter output with (a):(M1) V_{grid}, (b):(M2) V_{PCC}, (c):(M3) the inverter output current and (d):(M4) load current

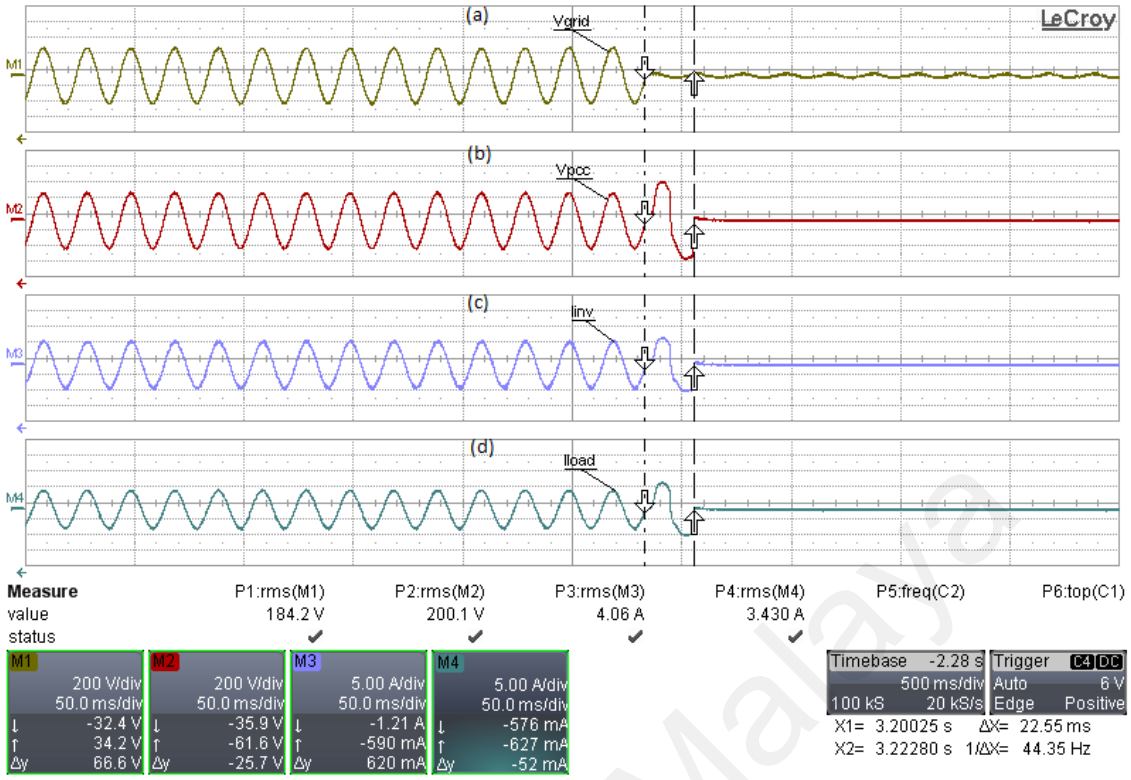


Figure 5.15: Experiment result for resistive R load under islanding operation for 75% (1.5kW) inverter output with (a):(M1) V_{grid}, (b):(M2) V_{PCC}, (c):(M3) the inverter output current and (d):(M4) load current

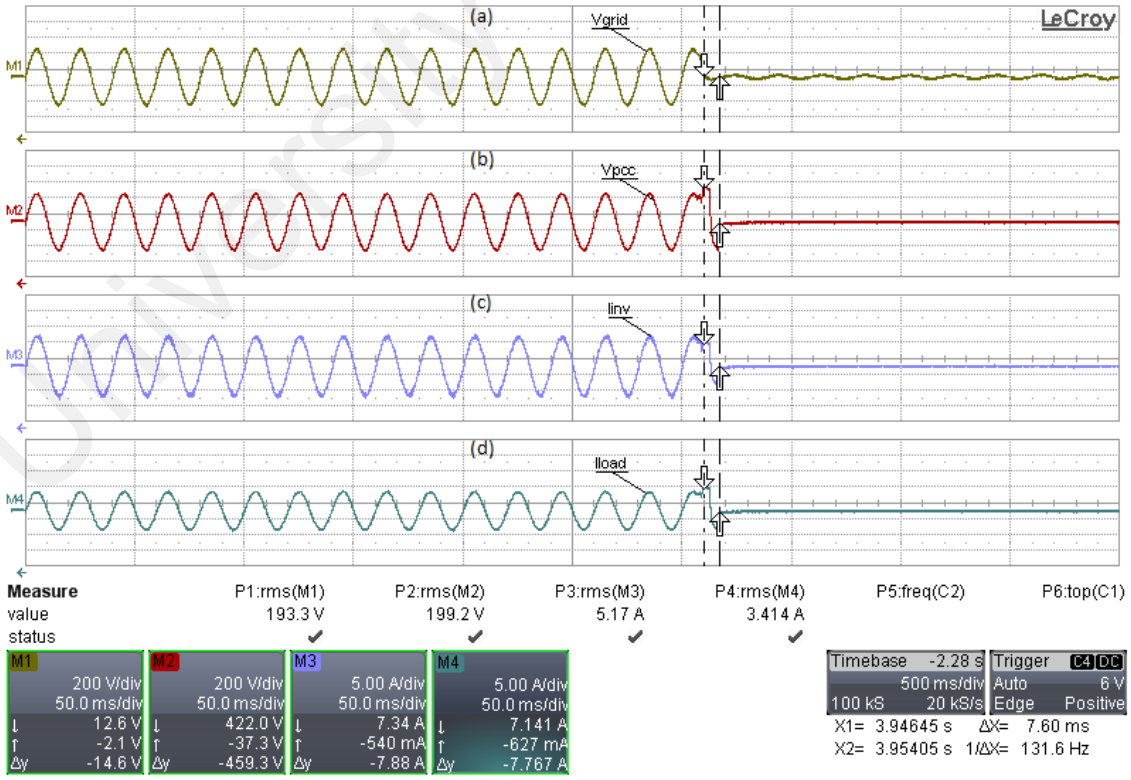


Figure 5.16: Experiment result for resistive R load under islanding operation for 100% (2kW) inverter output with (a):(M1) V_{grid}, (b):(M2) V_{PCC}, (c):(M3) the inverter output current and (d):(M4) load current

Figure 5.17 and Figure 5.18 show the experimental results for the R-L and R-C load under islanding operation. In the following experiments, the grid connected inverter will be tripped off when islanding is detected.

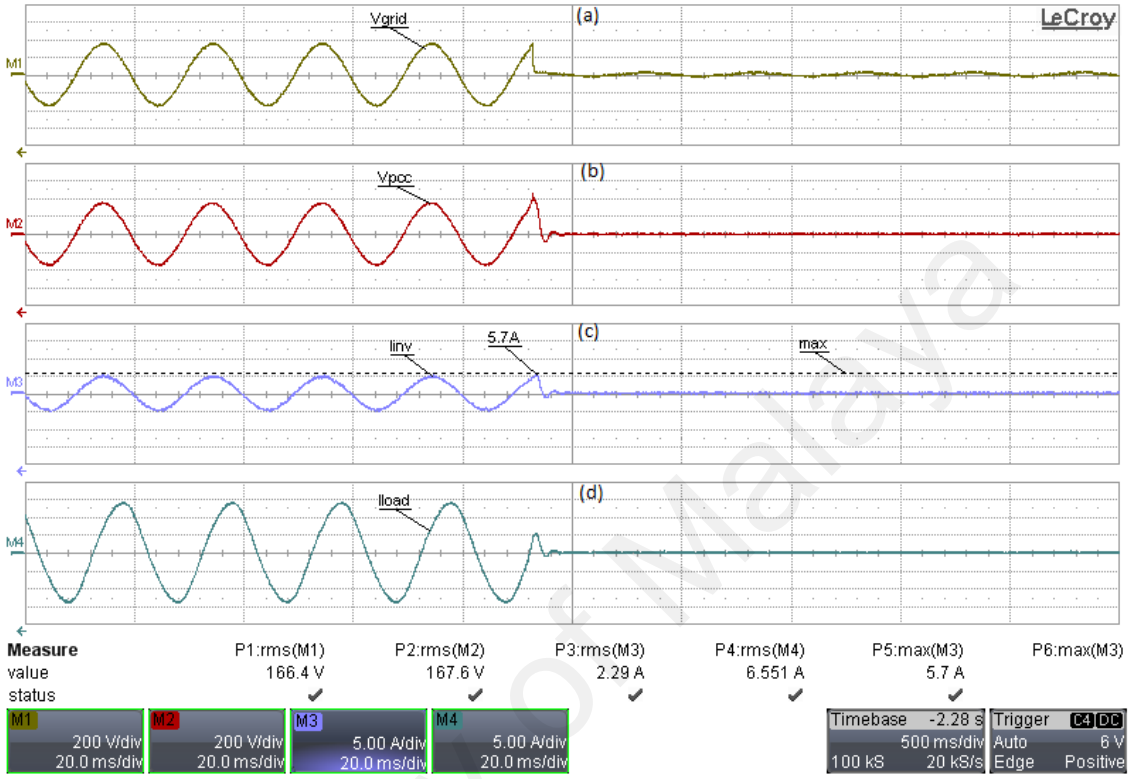


Figure 5.17: Experimental result for R-L load under islanding operation with (a):(M1) V_{grid}, (b):(M2) V_{PCC}, (c):(M3) the inverter output current and (d):(M4) load current

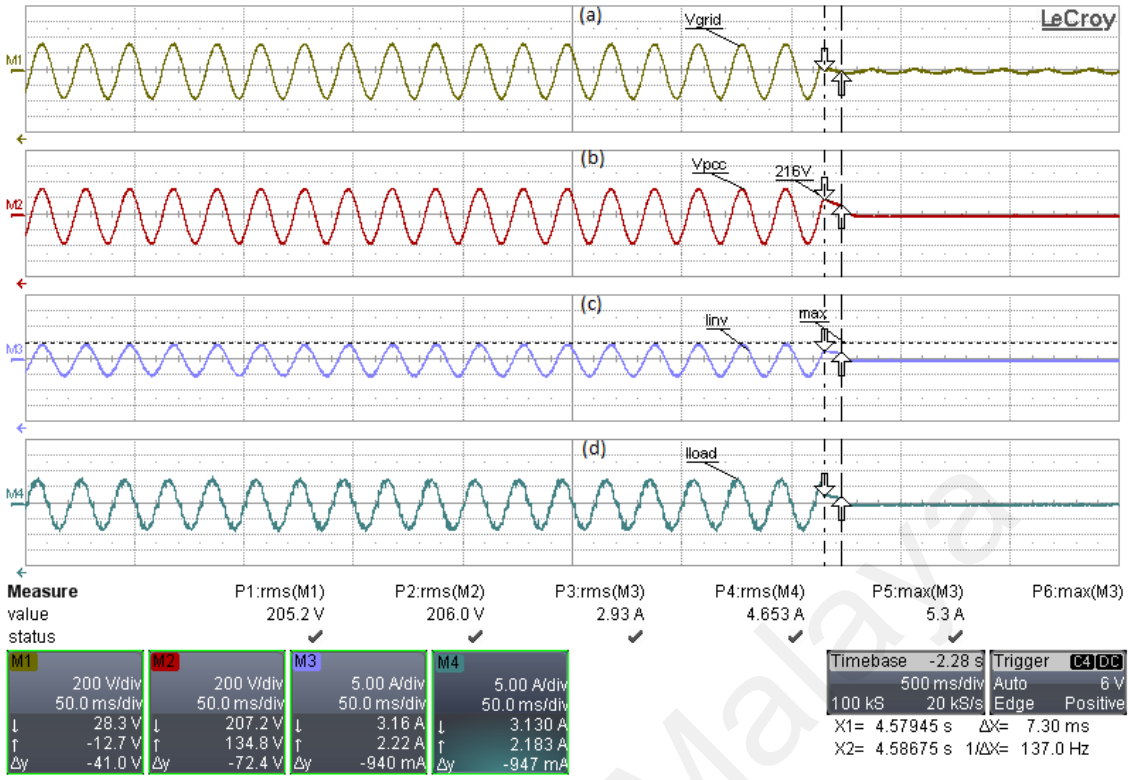


Figure 5.18: Experimental result for R-C load under islanding operation with with (a):(M1) V_{grid}, (b):(M2) V_{PCC}, (c):(M3) the inverter output current and (d):(M4) load current

Under islanding conditions, the magnitude and frequency of the voltage at PCC tend to slide from the rated grid values. It has been proven that the larger the power imbalance (ΔP and ΔQ in local generation and consumption in the islanded system prior to grid disconnection), the larger the variations are in the frequency of the voltage and voltage at the PCC. Therefore, standard under/over frequency and under/over voltage protections are successful in preventing islanding in system with large enough power imbalances. The islanding condition for the experiments conducted was made to have the smallest power imbalance possible, i.e., the worst-case scenario.

Figure 5.19, Figure 5.20 and Figure 5.21 show the experiment results for R-L-C load under islanding, at Q=1, Q=2, and Q=2.5. In the following experiments, the grid-connected inverter will be tripped off 21.25ms (Q=1), 24.8ms (Q=2) and 55.7ms (Q=2.5) (see Figure 5.19, Figure 5.20 and Figure 5.21) after the grid is disconnected. From all the following experiments (see Figure 5.19, Figure 5.20 and Figure 5.21), the inverter

(V_{PCC}) briefly swings up to slightly more than + and – 400 volt peak after the grid is disconnected, and then shuts down. The detection time of islanding operation may be different under different loads and different quality factors of RLC load. As Figure 5.22 shows, (M2) and (M3), at inverter output 1kW and R-L-C load with Q=2.5, the inverter output current was almost identical with the load current. This indicates the worst case for islanding detection, where the power-flow between the grid-connected inverter and the load is balanced.

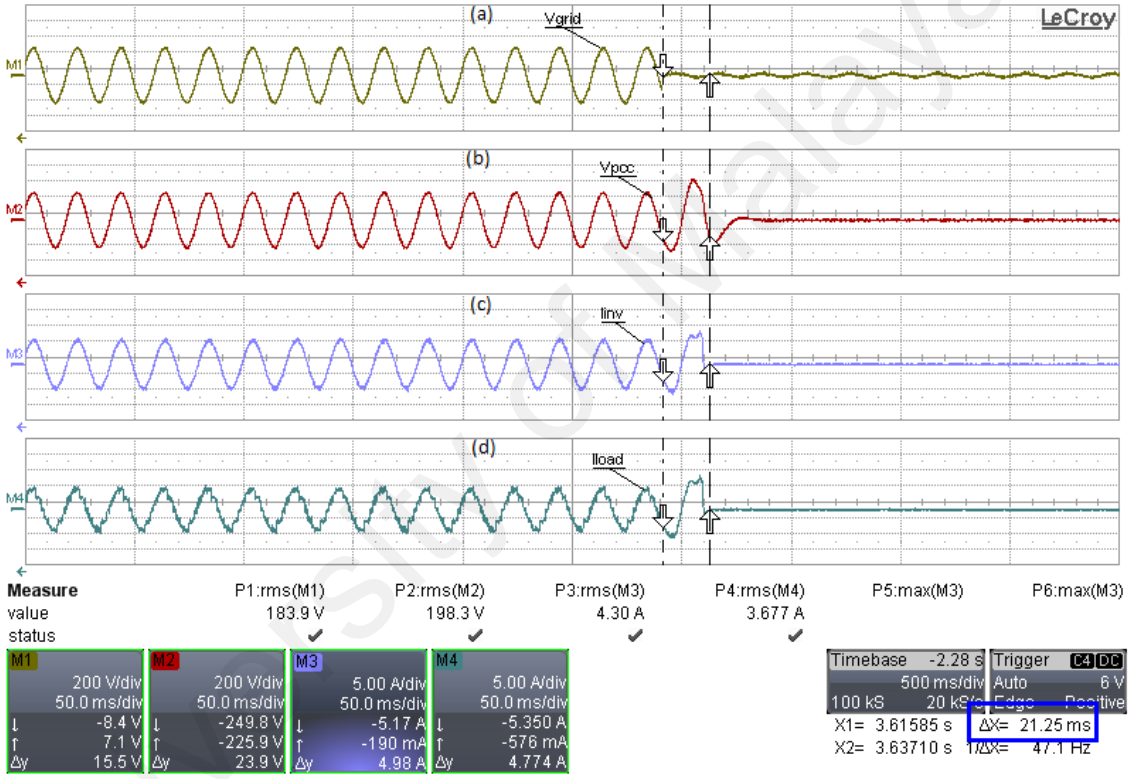


Figure 5.19: Experimental result for R-L-C load under islanding operation at Q=1 with (a):(M1) V_{grid}, (b):(M2) V_{PCC}, (c):(M3) the inverter output current and (d):(M4) load current

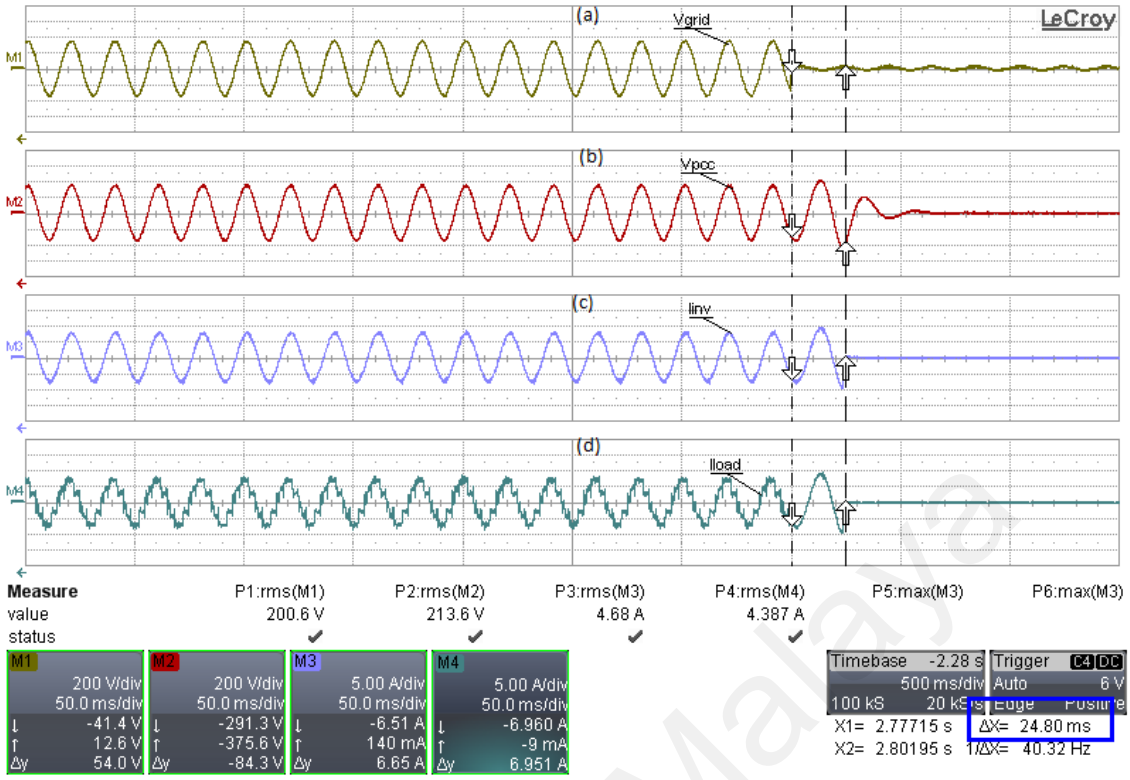


Figure 5.20: Experimental result for R-L-C load under islanding operation at Q=2 with (a):(M1) V_{grid}, (b):(M2) V_{PCC}, (c): (M3) the inverter output current and (d):(M4) load current

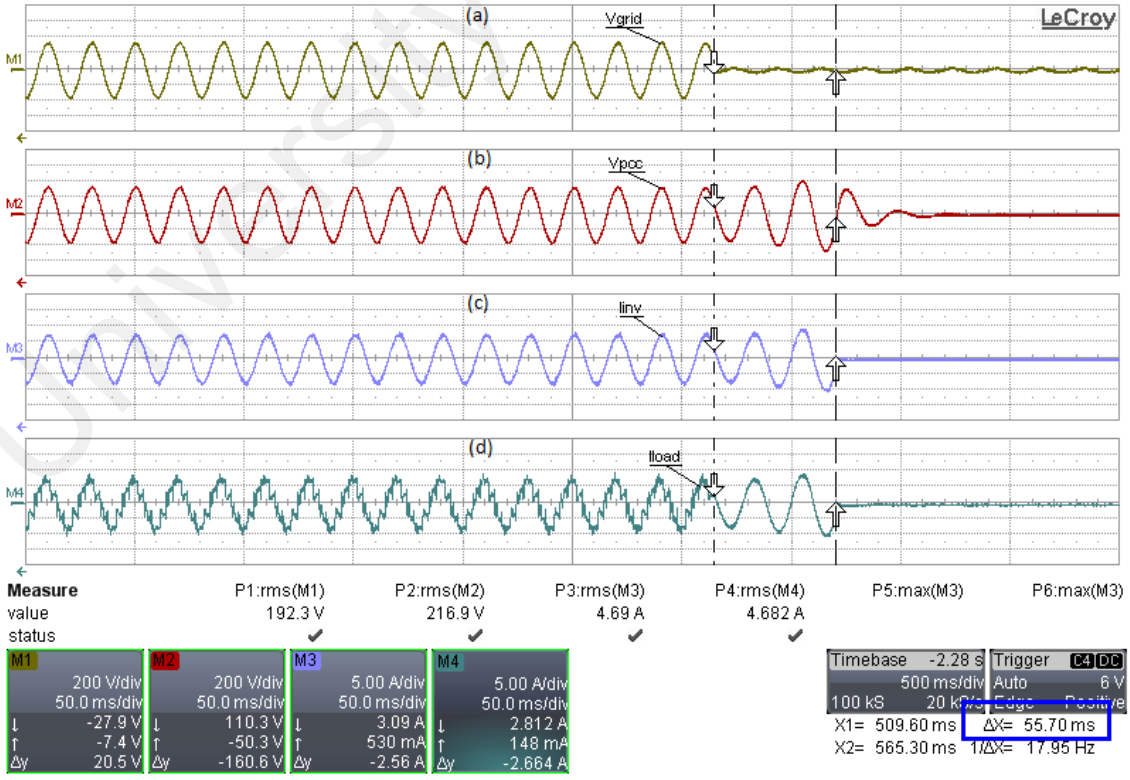


Figure 5.21: Experimental result for R-L-C load under islanding operation at Q=2.5 with (a):(M1) V_{grid}, (b):(M2) V_{PCC}, (c): (M3) the inverter output current and (d):(M4) load current

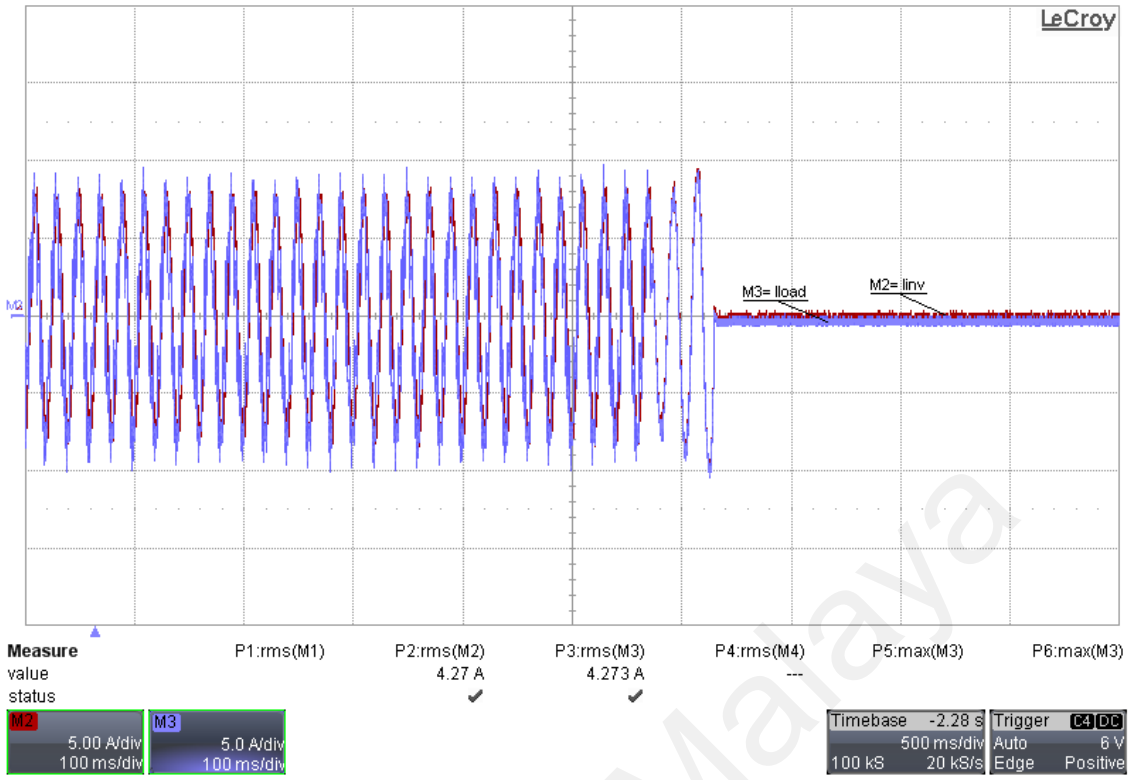


Figure 5.22: Experiment results for R-L-C load under islanding operation at Q=2.5 with (M2) the inverter output current, (M3) load current

Table 5.5 lists the disconnection times when the grid is disconnected until the inverter is tripped off. As shown in Table 5.6 the disconnection time is less than 0.3 seconds (24.8ms) for R-L-C load with Q=2. PM6000 Universal Power analyser was set to the minimum time setting available for data recording (every 0.3 seconds). The detection time satisfies the IEEE 929-2000 control standard, verifying that the proposed islanding method is able to detect islanding effectively. As shown in Table 5.5, the inverter current value immediately zeros out after the grid is disconnected.

Table 5.5: Detection times for the R-L-C load with Q=2 as taken by PM6000 Universal Power Analyzer

Timestamp		Channel	A rms	Watt
20130130155137.30	B	Load	5.00	1091.88
20130130155137.30	C	Grid	2.51	-182.38
20130130155137.30	D	Inverter	5.35	1283.13
20130130155137.60	B	Load	0.00	0.00
20130130155137.60	C	Grid	0.00	0.00
20130130155137.60	D	Inverter	0.00	0.00

Table 5.6: Detection times for the different quality factors

Capacity inverter output	Quality factor of the RLC Load	Detection time
1kW	1	21.25ms
1kW	2	24.8ms
1kW	2.5	55.7ms

According to IEEE Std. 929-2000 standard, the relationship between the amplitude of the load voltage and the maximum trip time for determining the islanding condition are shown in Table 5.7. All the experiment results show the amplitudes of the load voltage (V_{PCC}) to have passed the following requirement.

Table 5.7: Response to abnormal voltages

Voltage (at PCC)	Maximum trip time
V<120 (V<50%)	6 cycles
$120 \leq$ V < 211 (50% $\leq$ V < 88%)	120 cycles
$211 \leq$ V $\leq$ 264 (88% $\leq$ V $\leq$ 110%)	Normal operation
264 < V < 329 (110% < V <137%)	120 cycles
$329 \leq$ V (137% $\leq$ V)	2 cycles

The proposed method is shown to effectively and effortlessly detect islanding operation under different load types and quality factors. As Figure 5.23 shows, the inverter comes “on-line” and gradually increases its output power from zero to 1000 Watt. Figure 5.23 shows the transition as the inverter power increases and the grid transitions from delivering the load power to zero. Note that the load power stays constant during the transition period.

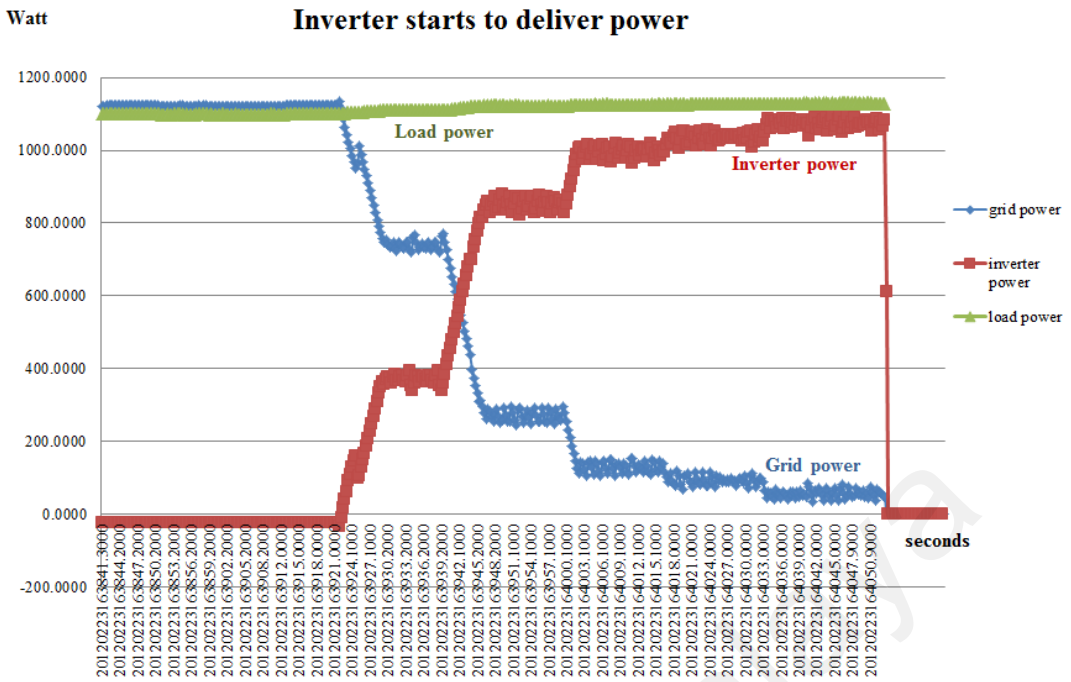


Figure 5.23: The inverter comes "on-line" and gradually increases its output to 1kW

5.4 Disconnection time for different method and algorithm

To prove that the proposed passive islanding detection has advantages over the implemented algorithm in TMS320F2812 DSP in terms of disconnection times, the corresponding comparisons were made on both passive islanding methods. Low cost PIC18F4550 compared with ATMEGA and TMS320F2812 DSP with under/over voltage and under-/over frequency islanding detection algorithms, were compared. The circuit connections and algorithms of the past methods are as in (Syamsuddin et al., 2009). The prototype of both methods monitored grid voltage and grid frequency at PCC.

The disconnection time of PIC18F4550 was much faster than that of ATMEGA and TMS320F2812. The cost of design and implementation for the proposed method were also much less. All disconnection times for ATMEGA and DSP TMS320F2812 based method were taken from “Testing of PV inverter no 2/2010 by Inverter quality control centre (IQCC) University Technology Malaysia Skudai Johor, 2010” report conducted on 15th July 2010 (Dr. Zainal & Dr. Naziha, 2010). Meanwhile, disconnection times for PIC 18F4550 were measured using PM6000 Universal Power Analyser. The disconnection

times were validated according to AS 4777.3-2005 standard. Table 5.8 compares the disconnection times.

Table 5.8: Disconnection times of the two methods

	Disconnection Time			
	Under voltage	Over voltage	Under frequency	Over frequency
ATMEGA and DSP based algorithm	Could not be determined	1.2 seconds	2.1seconds	52.5 seconds
PIC 18F4550 algorithm	0.6 seconds	0.6 seconds	0.6 seconds	0.6 seconds

As the table shows, the proposed method is much faster and more stable than the past method (very unstable). Although over-voltage disconnection time of the past method passed the less-than-2-seconds standard, the proposed method enabled much faster disconnection. From (Syamsuddin et al., 2009), this method used TMS320F2812 DSP for reading the grid voltage at the sensor signal through the ADC and calculates the RMS voltage value for under/over voltage disconnection. This may add some lagging to the systems when detecting under/over voltage. The proposed circuit and algorithm aim to correct the problem.

CHAPTER 6

Conclusion and Future Work

6.1 Conclusion

A low cost and effective passive method for islanding detection in single phase grid connected PV inverter has been applied to prototype and the islanding test was successfully tested and measured. In this work, an analog circuit for under/over voltage protection has been developed, to ensure fast detection with no added delay. An under/over frequency circuit has also been developed, for accurate and fast frequency detection and with minimal external components. A new algorithm is developed in a low cost PIC18F4550. The circuit topology, control algorithm, and operational principle of the proposed method have been presented in details. PIC18F4550 optimized the method's performance, which has drastically improved the disconnection time of a past method. The low cost, effective and minimal of external components are also the forte of this proposed method. A prototype is developed and tested to demonstrate the performance and feasibility of the proposed method. The experiment results showed that the proposed islanding detection method is able to detect islanding operation effectively under various load types, inverter output powers and quality factors. As a conclusion, all stated objectives of this work have been successfully met.

6.2 Author's Contribution

A key aspect in the construction of the proposed passive islanding system was to ensure simple implementations and efficient working operation. Major contributions of this work are as follows:

- The new hardware prototype design of the under/over voltage circuit and under/over

frequency circuit have been developed.

- Islanding control method has been implemented using PIC18F4550 to calculate the frequency values and control the voltage and frequency limitation of the single phase grid connected PV inverter.
- Islanding test has successfully been tested under different RLC load with different quality factors and inverter output powers.
- Reduction in the disconnection time of the inverter from the grid via optimization of the islanding algorithm.

6.3 Future works

Future work can be performed on the existing design to improve and increase the performance of the islanding detection method. Suggested future works are:

a) To develop a new islanding protection technique such as active islanding.

b) To combine the passive developed method with any active islanding method for further increase in performance.

c) To use wavelet transformation as passive islanding detection method.

APPENDIX A

Programming for the Proposed Islanding Method

```
/*****************************************************************

Device     :    PIC18F4550

File name : Islanding.c

Author     : Ku Nurul Edhura

Description : UMPEDAC

Compiler   : MPLAB IDE v8.46

*****************************************************************
#include <htc.h>
#include <pic18.h>
//#include <pic18f4550.h>
#include "delay.h"

static void Port_Config(void);

// PIC 18F4550 fuse configuration:
__CONFIG(1, USBPLL & IESODIS & FCMDIS & HSPLL & CPUDIV1 & PLLDIV5);
// Config word 2
__CONFIG(2, VREGEN & PWRTDIS & BOREN & BORV20 & WDTDIS & WDTPS32K);
// Config word 3
__CONFIG(3, PBDIGITAL & LPT1DIS & MCLREN);
```

```
27 // Config word 4
28 __CONFIG(4, XINSTDIS & STVREN & LVPDIS & ICPORTDIS & DEBUGDIS);
29 // Config word 5, 6 and 7 (protection configuration)
30 __CONFIG(5, UNPROTECT);
31 __CONFIG(6, UNPROTECT);
32 __CONFIG(7, UNPROTECT);
33 unsigned int counter=0; //Overflow counter
34 unsigned int x=0;
35 unsigned int y=0;
36 unsigned int k=0;
37 char tempOK;
38 char tempKO;
39 char voltageOK;
40 char voltageKO;
41 /*********************************************************************
42     Function : char setup(void)
43 *********************************************************************
44
45 void setup ()
46
47 {
48   INTCON=0b11111000;      //GIE=1,PEIE=1,TMR0IE=1,INT0IE=1,RBIE=1,TMR0IF
       =0,INTOIF=0,RBIF=0
49
50   INTCON2=0b10000000;
51   INT0IE=1;
52 .
53   //RBPU=0;
54   RDPU=0;
55   INTEDG0=0;
```

```
56
57   //Setup  Timer0
58 T0PS0=1;                                  T0PS1=1;
59 T0PS2=1;
60  PSA=0;
61 T0CS=0;
62   T08BIT=0;
63  TMR0H=0;
64  TMR0L=0;
65 }
66
67 /*************************************************************************


68     Function : void C_task main (void)
69 /*************************************************************************


70 void main ()
71  {
72       Port_Config();
73       setup();
74     while(1);
75 }
76 /*************************************************************************


77
78 #define RETURN 100
79
80   char i;
81   void interrupt highISR()
82 {
```

```
83      if(RD7==0  ||  RD6==0)
84      {RC7=0;  voltageOK=0;}
85
86      else
87      {voltageOK++;
88      if(voltageOK  >150)
89      {  RC7=1;}}
90
91      if  (RC7==1 && RC2==1)
92      {RC1=1;}
93      else
94      {RC1=0;}
95
96  if(TMR0IE)
97
98    {          //TMR0 Overflow ISR
99                                        //
100       counter++;
101
102         TMR0IF=0;
103     }
104
105 if(INT0IE && INT0IF)
106  {
107         char i,temp;
108
109        for  (temp= 0;temp<25;)
110         {
111         if(!(PORTB & (2<<RB0)))
112          temp++;
```

```
113          else
114             temp = RETURN;
115             }
116
117        if(temp != RETURN)
118         {
119         if(RC6==0)
120         RC6=1;
121         else
122         RC6=0;
123
124     if (RC6==1)
125  ((PORTC & (RC6==1)))
126     {TMR0ON=1;}
127        else
128        {TMR0ON=0;
129         k=counter;
130         x= TMR0L;
131         y= TMR0H;
132         //PORTD=y;
133
134       if(((TMR0H<<8) + TMR0L) >= 968 || ((TMR0H<<8) + TMR0L)<=912 )
135
136             {tempKO++; tempOK=0;
137         if(tempKO >3)
138             { RC2=0;}}
139         else
140         {tempOK++; tempKO=0;
141         if(tempOK >150)
142             { RC2=1;}}
```

```
143
144          counter=0;
145          TMR0H=0;
146          TMR0L=0;
147        }
148
149               RC0=1;
150               for(i=0xFF;i>0;i--);
151               RC0=0;
152              }
153
154    INT0IF=0;
155    }
156 }
157     static void Port_Config(void)
158 {
159    ADCON1 = 0x0F;
160 TRISA = 0b00000000;
161 TRISB = 0b00000001;
162 RB2 RB1 RB0
163 TRISC = 0b00000000;
164  TRISD = 0b11000000;
165  TRISE = 0b00000000;
166  PORTA = 0b00000000;
167  PORTB = 0b00000000;
168  PORTC = 0b00000000;
169  PORTD = 0b00000000;
170  PORTE = 0b00000000;
171 }
```

APPENDIX B

Photos of Hardware

Main Subsystems

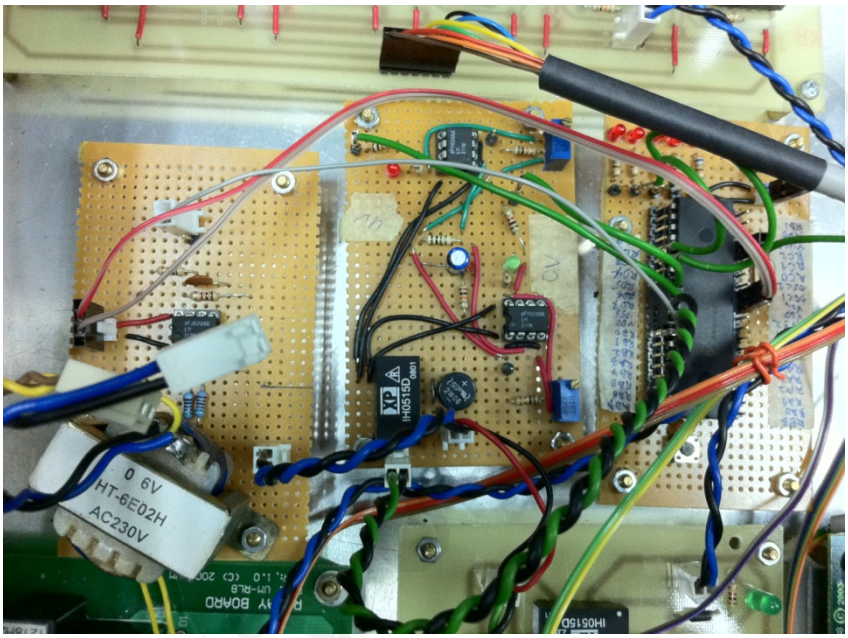


Figure B.1: The proposed under/over voltage and under/over frequency circuits

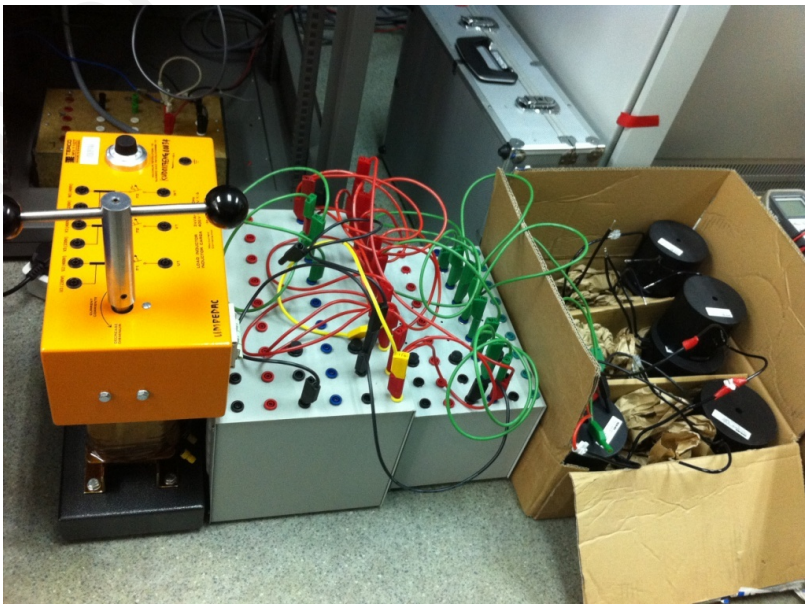


Figure B.2: Variable Inductor and Capacitor loads

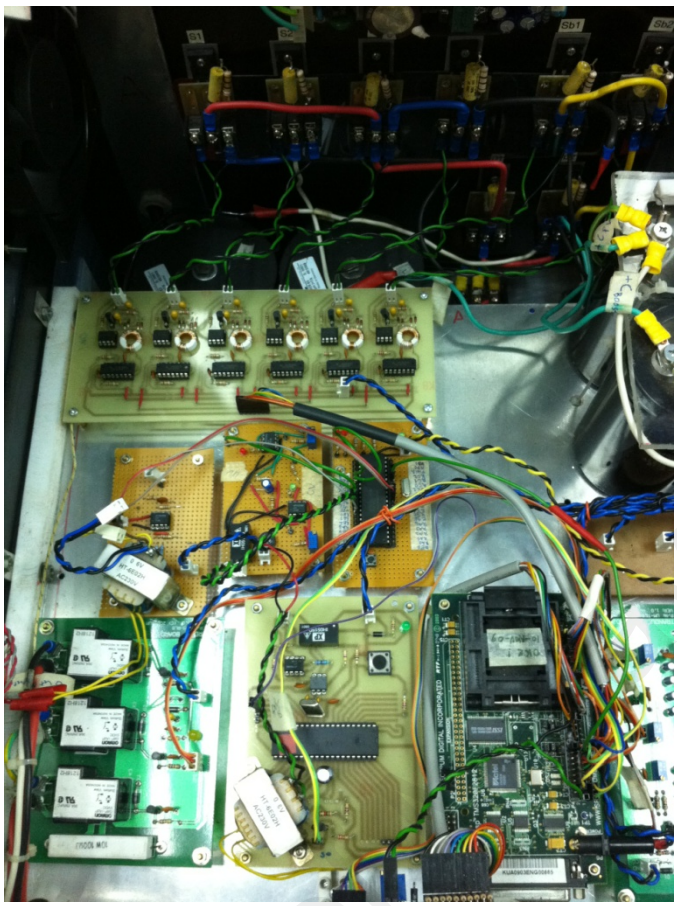


Figure B.3: Proposed circuits with PIC18F4550, gate drive circuits, sensor circuits and eZdspTM F2812 board.

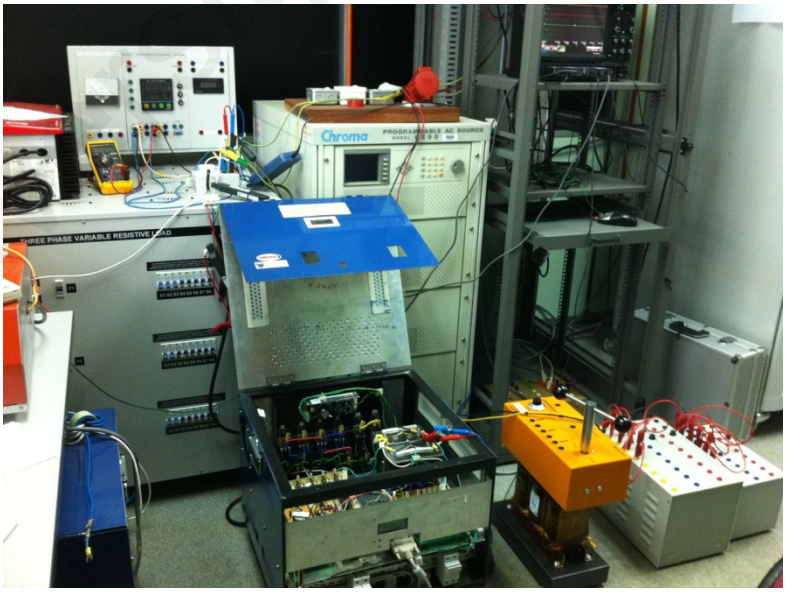


Figure B.4: Three Phase Variable Resistive Load and Single Phase Grid Connected PV Inverter.

Figure B.5: L-C Meter

Figure B.6: PM6000 Power Analyzer and Lecroy Wave Runner 64Xi-A Oscilloscope.

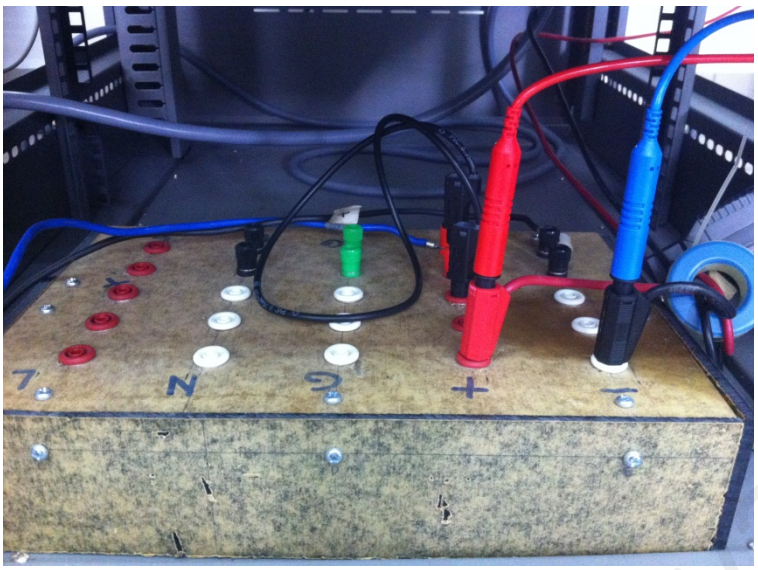


Figure B.7: DC and AC connections

Figure B.8: Single Phase grid connected PV inverter

Figure B.9: Programmable AC source Model 6560

Complete System

Figure B.10: Complete systems prototype

Figure B.11: Close-up view

Figure B.12: Islanding Test with Resistive load, inverter and Programmable AC source Model 6560

APPENDIX C

PIC18F4550

PIC18F4550 Architecture

The special PIC18F4550 features include C Compiler Optimized Architecture with optional Extended Instruction Set, 100,000 Erase/Write Cycle Enhanced Flash Program Memory typical, 1,000,000 Erase/Write Cycle Data EEPROM Memory typical, Flash/-Data EEPROM Retention: > 40 years, Self-Programmable under Software Control, Priority Levels for Interrupts, 8 x 8 Single-Cycle Hardware Multiplier, Extended Watchdog Timer (WDT) which has a programmable period from 41 ms to 131s, Programmable Code Protection, Single-Supply 5V In-Circuit Serial Programming™(ICSP™) via two pins, In-Circuit Debug (ICD) via two pins and Wide Operating Voltage Range (2.0V to 5.5V). Figure 1 below shows the 40 pin diagrams of PIC18F4550.

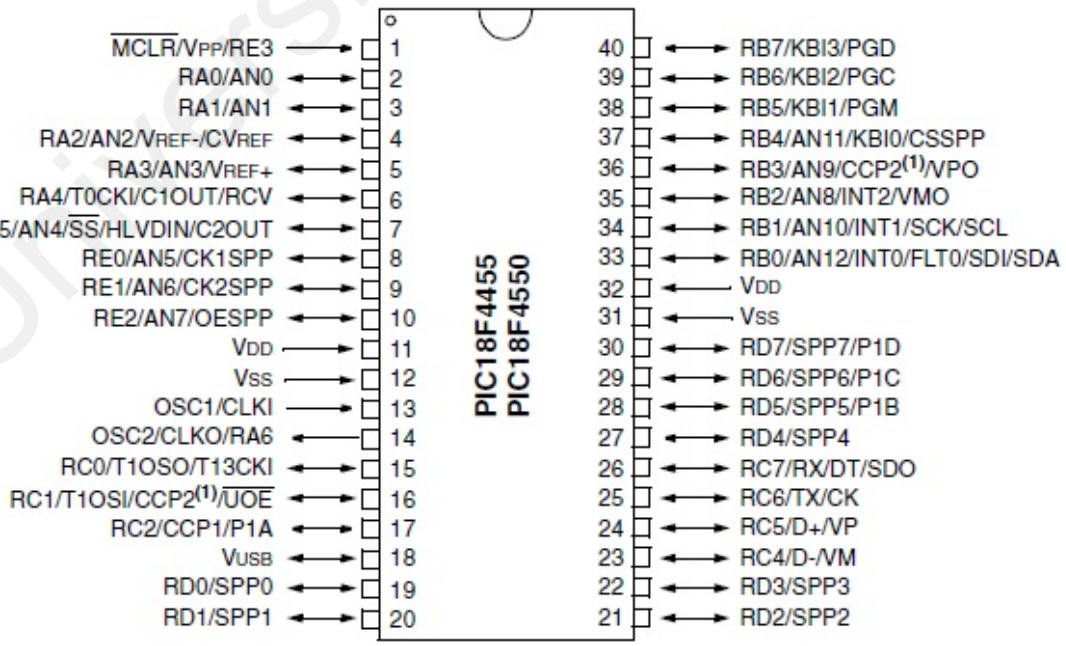


Figure C.1: 40 pin diagrams of PIC18F4550.

Connector configuration ICSP

In-circuit-serial-programming (ICSP) is a way of programming a PIC while it is still attached to the application circuit. ICSP provides a convenient way of programming PIC Microchips without removing the chip from the development or production board. This is simply done with two lines for clock and data and three other lines for power, ground and the programming voltage. Figure 2 below is ICSP pin locations for PIC18F4550.

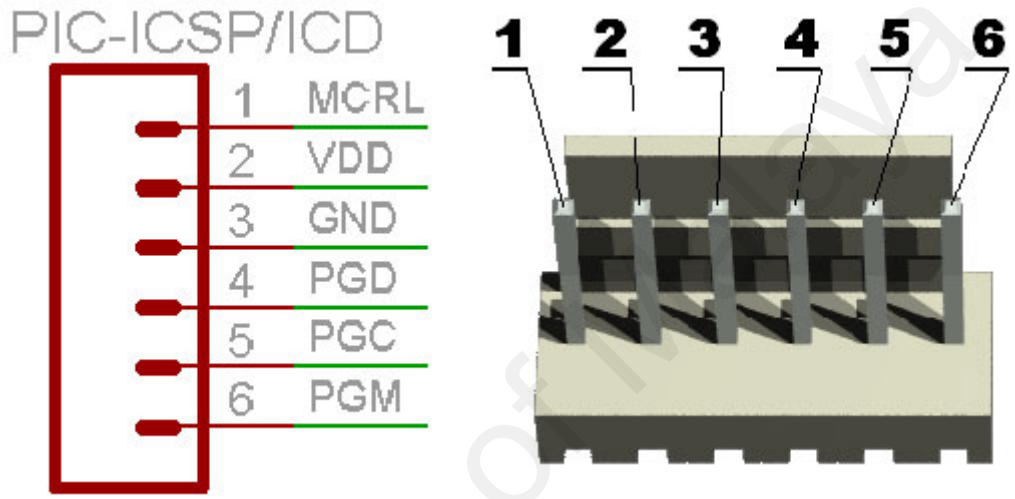


Figure C.2: Connector ICSP pin locations for PIC18F4550

The pin-out for Microchip PIC18F4550 standard 6 pin connector for in-circuit-serial-programming (ICSP) is listed in Table C.1 below:

Table C.1: ICSP

Pins	Name	Function
1	MCLR/Vpp (programming voltage)	Device Reset and Programming Enable.
2	Vdd(+5V)	Positive power input to the PIC.
3	GND	Negative power input to the PIC and the zero volts reference for the remaining signals. Voltages of the other signals are implicitly with respect to GND.
4	PGD	In-Circuit Debugger and ICSP programming data pin.
5	PGC	Serial execution (ICSP™) clock input for ICSP
6	LVP (low-voltage programming mode control)	

The Peripherals of PIC18F4550

The PIC18F4550 has a lot of functions. The peripherals highlights of PIC18F4550 include 25mA high current sink/source, three external interrupts, four timer modules (Timer0 to Timer3), up to 2 capture/compare/PWM (CCP) modules, enhanced capture/-compare/PWM (ECCP) module which include multiple output modes, selectable polarity, programmable dead time and auto-shutdown and auto-restart, enhanced USART module which consist of LIN bus support, master synchronous serial port (MSSP) module supporting 3-wire SPI (all 4 modes) and I^2C™Master and Slave modes, 10-bit up to 13-channel analog-to-digital converter module (A/D) with programmable acquisition time and dual analog comparators with input multiplexing. Due to the concentration of the objective for this dissertation, among all of the functions of PIC18F4550 only the important functions and most related to this method are described. The basic features of PIC18F4550 are shown in Table 2:

Table C.2: Device feature

Features	PIC18F4550
Operating Frequency	DC – 48 MHz
Program Memory (Bytes)	32768
Program Memory (Instructions)	16384
Data Memory (Bytes)	2048
Data EEPROM Memory (Bytes)	256
Interrupt Sources	20
I/O Ports	Ports A, B, C, D, E
Timers	4
Capture/Compare/PWM Modules	1
Enhanced Capture/Compare/PWM Modules	1
Serial Communications	MSSP,Enhanced USART
Universal Serial Bus (USB) Module	1
Streaming Parallel Port (SPP)	Yes
10-Bit Analog-to-Digital Module	13 Input Channels
Comparators	2

continued on the next page

Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional),WDT
Programmable Low-Voltage Detect	Yes
Programmable Brown-out Reset	Yes
Instruction Set	75 Instructions; 83 with Extended Instruction Set enabled
Packages	40-pin PDIP 44-pin QFN 44-pin TQFP

APPENDIX D

List of Publications from this work

Manuscript Published

Ku Nurul Edhura, J.Selvaraj, and N.A Rahim, "A review of the islanding detection methods in grid-connected PV inverters", *Renewable and Sustainable Energy Reviews, 21(0) 756-766.*

doi: http://dx.doi.org/10.1016/j.rser.2013.01.018 (Q1- ISI Journal)

Ku Nurul Edhura, N.A Rahim, J.Selvaraj, Ahmad Rivai and Krismadinata Chaniago, "An effective passive islanding detection method for PV single-phase grid-connected inverter", *Solar Energy, 97(0), 155-167.*

doi: http://dx.doi.org/10.1016/j.solener.2013.08.011 (Q2- ISI Journal)

Manuscript under review

N.A Rahim, Maaspaliza, and Ku Nurul Edhura, "Single Phase Grid Connected Inverter with Islanding Detection and Low Ground Current Leakage", *IET Power Electronics.* (ISI Journal)

Proceeding

Ku Nurul Edhura, N.A Rahim, J.Selvaraj, and Ahmad Rivai, "A Low Cost and Effective Passive Islanding Method in Single Phase Grid Connected PV inverter", *2012 Sustainable Future Energy Conference, Brune*i on 21-23 November 2012.

REFERENCES

Angelis-Dimakis, A., Biberacher, M., Dominguez, J., Fiorese, G., Gadocha, S., Gnansounou, E., ... Robba, M. (2011). Methods and tools to evaluate the availability of renewable energy sources. *Renewable and Sustainable Energy Reviews*, *15*(2), 1182-1200. doi: 10.1016/j.rser.2010.09.049

Arachchige, L. W., & Rajapakse, A. (2011). A pattern recognition approach for detecting power islands using transient signals Part I: Design and implementation. In *Power and Energy Society General Meeting, 2011 IEEE* (p. 1-1).

Bahrani, B., Karimi, H., & Iravani, R. (2011). Nondetection zone assessment of an active islanding detection method and its experimental evaluation. *Power Delivery, IEEE Transactions on*, *26*(2), 517-525.

Calais, M., Agelidis, V. G., & Meinhardt, M. (1999). Multilevel converters for single-phase grid connected photovoltaic systems: an overview. *Solar Energy*, *66*(5), 325-335.

Calais, M., Myrzik, J., Spooner, T., & Agelidis, V. G. (2002). Inverters for single-phase grid connected photovoltaic systems-an overview. In *Power Electronics Specialists Conference, 2002. pesc 02. 2002 IEEE 33rd annual* (Vol. 4, p. 1995-2000).

Cardenas, A., & Agbossou, K. (2012). Experimental evaluation of voltage positive feedback based anti-islanding algorithm: Multi-inverter case. *Energy Conversion, IEEE Transactions on*, *27*(2), 498-506.

Cardenas, A., Agbossou, K., & Doumbia, M. L. (2009). An active anti-islanding algorithm for inverter based multi-source der systems. In *Power and Energy Engineering Conference, 2009. APPEEC 2009. Asia-Pacific* (p. 1-6).

Chiang, W.-J., Jou, H.-L., & Wu, J.-C. (2012). Active islanding detection method for inverter-based distribution generation power system. *International Journal of Electrical Power & Energy Systems*, *42*(1), 158-166.

Chiang, W.-J., Jou, H.-L., Wu, J.-C., Wu, K.-D., & Feng, Y.-T. (2010). Active islanding detection method for the grid-connected photovoltaic generation system. *Electric Power Systems Research*, *80*(4), 372-379.

Chowdhury, S. P., Chowdhury, S., & Crossley, P. A. (2009). Islanding protection of active distribution networks with renewable distributed generators: A comprehensive survey. *Electric Power Systems Research*, *79*(6), 984-992.

Ciobotaru, M., Agelidis, V., & Teodorescu, R. (2008). Accurate and less-disturbing active anti-islanding method based on pll for grid-connected PV inverters. In *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE* (p. 4569-4576).

Corporation, S. (March 1, 2011). *Application note PVA-600-1: Guide to interpreting I-V curve measurements of PV arrays.*

Dash, P. K., Padhee, M., & Panigrahi, T. K. (2012). A hybrid time–frequency approach based fuzzy logic system for power island detection in grid connected distributed generation. *International Journal of Electrical Power & Energy Systems*, *42*(1), 453-464.

Deb, S. K. (2000). Chapter 584 - recent developments in high-efficiency PV cells. In A. A. M. Sayigh (Ed.), *World Renewable Energy Congress VI* (p. 2658-2663). Oxford: Pergamon.

De Mango, F., Liserre, M., & Aquila, A. D. (2006). Overview of anti-islanding algorithms for PV systems. Part II: Activemethods. In *Power Electronics and Motion Control Conference, 2006. EPE-PEMC 2006. 12th International* (p. 1884-1889).

De Mango, F., Liserre, M., Aquila, A. D., & Pigazo, A. (2006). Overview of anti-islanding algorithms for PV systems. Part I: Passive methods. In *Power Electronics and Motion Control Conference, 2006. EPE-PEMC 2006. 12th international* (p. 1878-1883).

Dr. Robert H. Wills, P. (1994). *The interconnection of photovoltaic systems with the utility grid: An overview for utility engineers sand94-1057* (Tech. Rep.). Sandia National Laboratories.

Dr. Zainal, S., & Dr. Naziha, A. A. (2010). *Testing of PV inverter report no 2/202 15th july 2010* (Tech. Rep.). University Teknology Malaysia Skudai Johor.

Eltawil, M. A., & Zhao, Z. (2010). Grid-connected photovoltaic power systems: Technical and potential problems—a review. *Renewable and Sustainable Energy Reviews*, *14*(1), 112-129.

Freitas, W., Wilsun, X., Affonso, C. M., & Zhenyu, H. (2005). Comparative analysis between rocof and vector surge relays for distributed generation applications. *Power Delivery, IEEE Transactions on*, *20*(2), 1315-1324.

Funabashi, T., Koyanagi, K., & Yokoyama, R. (2003). A review of islanding detection methods for distributed resources. In *Power Tech Conference Proceedings, 2003 IEEE Bologna* (Vol. 2, p. 6 pp. Vol.2).

Grid connection of energy systems via inverters - Part 2: Inverter requirements (No. AS 4777.2-2005). (2005).

Grid connection of energy systems via inverters - Part 3: Grid protection requirements. (No. AS 4777.3 - 2005). (2005).

Hamzeh, M., Farhangi, S., & Farhangi, B. (2008). A new control method in PV grid connected inverters for anti-islanding protection by impedance monitoring. In *Control and Modeling for Power Electronics, 2008. COMPEL 2008. 11th Workshop* (p. 1-5).

Hanif, M., Basu, M., & Gaughan, K. (2011). A discussion of anti-islanding protection schemes incorporated in a inverter based dg. In *Environment and Electrical Engineering (EEEIC), 2011 10th International Conference* (p. 1-5).

Hanif, M., Dwivedi, U. D., Basu, M., & Gaughan, K. (2010). Wavelet based islanding detection of dc-ac inverter interfaced dg systems. In *Universities Power Engineering Conference (UPEC), 2010 45th International* (p. 1-5).

Hernandez-Gonzalez, G., & Iravani, R. (2006). Current injection for active islanding detection of electronically-interfaced distributed resources. *Power Delivery, IEEE Transactions on*, *21*(3), 1698-1705.

IEEE Recommended Practice for Utility Interface of Photovoltaic (PV) Systems. (2000).

Indu Rani, B., Srikanth, M., Saravana Ilango, G., & Nagamani, C. (2013). An active islanding detection technique for current controlled inverter. *Renewable Energy*, *51*(0), 189-196.

Jae-Hyung, K., Jun-Gu, K., Young-Hyok, J., Yong-Chae, J., & Chung-Yuen, W. (2011). An islanding detection method for a grid-connected system based on the goertzel algorithm. *Power Electronics, IEEE Transactions on*, *26*(4), 1049-1055.

Jun, Z., Dehong, X., Guoqiao, S., Ye, Z., Ning, H., & Jie, M. (2013). An improved islanding detection method for a grid-connected inverter with intermittent bilateral reactive power variation. *Power Electronics, IEEE Transactions on*, *28*(1), 268-278.

Jung, Y., Choi, J., & Yu, G. (2007). A novel active anti-islanding method for grid-connected photovoltaic inverter. In *Photovoltaic Energy Conversion, Conference Record of the 2006 IEEE 4th World Conference.*

Karimi, H., Yazdani, A., & Iravani, R. (2008). Negative-sequence current injection for fast islanding detection of a distributed resource unit. *Power Electronics, IEEE Transactions on*, *23*(1), 298-307.

Kaundinya, D. P., Balachandra, P., & Ravindranath, N. H. (2009). Grid-connected versus stand-alone energy systems for decentralized power—a review of literature. *Renewable and Sustainable Energy Reviews*, *13*(8), 2041-2050.

Krismadinata. (2012). Modified h-bridge multilevel inverter for photovoltaic system (Doctoral dissertation, University of Malaya, Malaysia). *PhD Thesis*, *University of Malaya, Malaysia*.

Kunte, R. S., & Wenzhong, G. (2008). Comparison and review of islanding detection techniques for distributed energy resources. In *Power Symposium, 2008. NAPS '08. 40th North American* (p. 1-8).

Kyocera. (2008). High efficiency multicrystal photovoltaic module kd135gx-lpu in kyocera (ed.) [Computer software manual].

Lee, J. B., Chen, Z., Allen, M. G., Rohatgi, A., & Arya, R. (1995). A miniaturized high-voltage solar cell array as an electrostatic mems power supply. *Microelectromechanical Systems, Journal of*, *4*(3), 102-108.

Liserre, M., Pigazo, A., Dell'Aquila, A., & Moreno, V. M. (2006). An anti-islanding method for single-phase inverters based on a grid voltage sensorless control. *Indus-*

trial Electronics, IEEE Transactions on, *53*(5), 1418-1426.

Llaria, A., Curea, O., Jiménez, J., & Camblong, H. (2011). Survey on microgrids: Unplanned islanding and related inverter control techniques. *Renewable Energy*, *36*(8), 2052-2061.

Lopes, L. A. C., & Huili, S. (2006). Performance assessment of active frequency drifting islanding detection methods. *Energy Conversion, IEEE Transactions on*, *21*(1), 171-180.

Mahat, P., Zhe, C., & Bak-Jensen, B. (2009). A hybrid islanding detection technique using average rate of voltage change and real power shift. *Power Delivery, IEEE Transactions on*, *24*(2), 764-771.

Mohamad, H., Mokhlis, H., Bakar, A. H. A., & Ping, H. W. (2011). A review on islanding operation and control for distribution network connected with small hydro power plant. *Renewable and Sustainable Energy Reviews*, *15*(8), 3952-3962.

Morsi, W. G., Diduch, C. P., & Chang, L. (2010). A new islanding detection approach using wavelet packet transform for wind-based distributed generation. In *Power Electronics for Distributed Generation Systems (PEDG), 2010 2nd IEEE International Symposium* (p. 495-500).

Najy, W. K. A., Zeineldin, H. H., Alaboudy, A. H. K., & Wei Lee, W. (2011). A bayesian passive islanding detection method for inverter-based distributed generation using esprit. *Power Delivery, IEEE Transactions on*, *26*(4), 2687-2696.

Nema, P., Nema, R. K., & Rangnekar, S. (2009). A current and future state of art development of hybrid energy system using wind and PV-solar: A review. *Renewable and Sustainable Energy Reviews*, *13*(8), 2096-2103.

Nguyen, D. D. (2008). Modeling and reconfiguration of solar photovoltaic arrays under non-uniform shadow conditions (Doctoral dissertation, Northeastern University). *PhD thesis,Northeastern University*.

O'Kane, P., & Fox, B. (1997). Loss of mains detection for embedded generation by system impedance monitoring. In *Developments in Power System Protection, sixth International Conference on (Conf. Publ. no. 434)* (p. 95-98).

Padhee, M., Dash, P. K., Krishnanand, K. R., & Rout, P. K. (2012). A fast gauss-newton algorithm for islanding detection in distributed generation. *Smart Grid, IEEE Transactions on*, *3*(3), 1181-1191.

Parida, B., Iniyan, S., & Goic, R. (2011). A review of solar photovoltaic technologies. *Renewable and Sustainable Energy Reviews*, *15*(3), 1625-1636.

Pigazo, A., Liserre, M., Mastromauro, R. A., Moreno, V. M., & Dell'Aquila, A. (2009). Wavelet-based islanding detection in grid-connected PV systems. *Industrial Electronics, IEEE Transactions on*, *56*(11), 4445-4455.

Pigazo, A., Moreno, V. M., Liserre, M., & Dell'Aquila, A. (2007). Wavelet-based island-

ing detection algorithm for single-phase photovoltaic (PV) distributed generation systems. In *Industrial Electronics, 2007. ISIE 2007. IEEE International Symposium* (p. 2409-2413).

Rahim, N. A., Chaniago, K., & Selvaraj, J. (2011). Single-phase seven-level grid-connected inverter for photovoltaic system. *Industrial Electronics, IEEE Transactions on*, *58*(6), 2435-2443.

Ramakumar, R., & Bigger, J. E. (1993). Photovoltaic systems. *Proceedings of the IEEE*, *81*(3), 365-377.

Ranade, S. J., Prasad, N. R., Omick, S., & Kazda, L. F. (1989). A study of islanding in utility-connected residential photovoltaic systems part i-models and analytical methods. *Power Engineering Review, IEEE*, *9*(9), 45-45.

Rath, J. K. (2003). Low temperature polycrystalline silicon: a review on deposition, physical properties and solar cell applications. *Solar Energy Materials and Solar Cells*, *76*(4), 431-487.

Ray, P. K., Kishor, N., & Mohanty, S. R. (2010). S-transform based islanding detection in grid-connected distributed generation based power system. In *Energy Conference and Exhibition (EnergyCon), 2010 IEEE International* (p. 612-617).

Ray, P. K., Kishor, N., & Mohanty, S. R. (2012). Islanding and power quality disturbance detection in grid-connected hybrid power system using wavelet and s-transform. *Smart Grid, IEEE Transactions on*, *3*(3), 1082-1094.

Redfern, M. A., Usta, O., & Fielding, G. (1993). Protection against loss of utility grid supply for a dispersed storage and generation unit. *Power Delivery, IEEE Transactions on*, *8*(3), 948-954.

Reigosa, D., Briz, F., Blanco, C., Garcia, P., & Guerrero, J. M. (2011). Active islanding detection using high frequency signal injection. In *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE* (p. 2183-2190).

Reigosa, D., Briz, F., Charro, C. B., Garcia, P., & Guerrero, J. M. (2012). Active islanding detection using high-frequency signal injection. *Industry Applications, IEEE Transactions on*, *48*(5), 1588-1597.

Ropp, M. E., Begovic, M., Rohatgi, A., Kern, G. A., Bonn, S., R. H., & Gonzalez, S. (2000). Determining the relative effectiveness of islanding detection methods using phase criteria and nondetection zones. *Energy Conversion, IEEE Transactions on*, *15*(3), 290-296.

Shariatinasab, R., & Akbari, M. (2010). New islanding detection technique for dg using discrete wavelet transform. In *Power and Energy (PECon), 2010 IEEE International Conference* (p. 294-299).

Smith, G. A., Onions, P. A., & Infield, D. G. (2000). Predicting islanding operation of grid connected PV inverters. *Electric Power Applications, IEE Proceedings -*, *147*(1), 1-6.

Soo-Hyoung, L., & Jung-Wook, P. (2009). New islanding detection method for inverter-based distributed generation considering its switching frequency. In *Industry Applications Society Annual Meeting, 2009. IAS 2009. IEEE* (p. 1-8).

Strath, N. (2005). Islanding detection in power systems (Doctoral dissertation, Department of Industrial Electrical Engineering and Automation Lund University). *Department of Industrial Electrical Engineering and Automation Lund University*.

Sung-Il, J., & Kwang-Ho, K. (2004). An islanding detection method for distributed generations using voltage unbalance and total harmonic distortion of current. *Power Delivery, IEEE Transactions on*, *19*(2), 745-752.

Syamsuddin, S., Rahim, N. A., Krismadinata, & Selvaraj, J. (2009). Implementation of tms320f2812 in islanding detection for photovoltaic grid connected inverter. In *Technical Postgraduates (TECHPOS), 2009 International Conference* (p. 1-5).

T5-09, R. I. (2002). *Evaluation of islanding detection methods for photovoltaic utility interactive power systems* (Tech. Rep.). International Energy Agency Implementing agreement on Photovoltaic Power Systems, U.S.A.

Yafaoui, A., Bin, W., & Kouro, S. (2012). Improved active frequency drift anti-islanding detection method for grid connected photovoltaic systems. *Power Electronics, IEEE Transactions on*, *27*(5), 2367-2375.

Yip, H. T., Millar, G., Lloyd, G. J., Dysko, A., Burt, G. M., & Tumilty, R. (2010). Islanding detection using an accumulated phase angle drift measurement. In *Developments in Power System Protection (DPSP 2010). managing the Change, 10th IET International Conference on* (p. 1-5).

Yong-zheng Zhang, H. S., & Lopes, L. A. C. (2007). *An islanding detection enhancer for a system with multiple photovoltaic inverters.*

Yu, B., Matsui, M., So, J., & Yu, G. (2008). A high power quality anti-islanding method using effective power variation. *Solar Energy*, *82*(4), 368-378.

Yu, B., Matsui, M., & Yu, G. (2010). A review of current anti-islanding methods for photovoltaic power system. *Solar Energy*, *84*(5), 745-754.

Zeineldin, H., & Kirtley, J. (2009). A simple technique for islanding detection with negligible non-detection zone. In *Power & Energy Society General Meeting, 2009. PES '09. IEEE* (p. 1-1).

Zeineldin, H. H., & Conti, S. (2011). Sandia frequency shift parameter selection for multi-inverter systems to eliminate non-detection zone. *Renewable Power Generation, IET*, *5*(2), 175-183.

Zeineldin, H. H., & Kennedy, S. (2009). Sandia frequency-shift parameter selection to eliminate nondetection zones. *Power Delivery, IEEE Transactions on*, *24*(1), 486-487.

Zhihong, Y., Kolwalkar, A., Yu, Z., Pengwei, D., & Reigh, W. (2004). Evaluation of anti-

islanding schemes based on nondetection zone concept. *Power Electronics, IEEE Transactions on*, *19*(5), 1171-1176.

Zhou, H., Tong, C., Mao, M., & Gao, C. (2010). Development of single-phase photovoltaic grid-connected inverter based on dsp control. In *Power Electronics for Distributed Generation Systems (PEDG), 2010 2nd IEEE International Symposium* (p. 650-653).