A NEW SWITCHING ALGORITHM BASED ON SINGLE-PHASE MODULATOR FOR Z-SOURCE INVERTERS WITH REDUCED COMPUTATION TIME AND ENHANCED OUTPUT VOLTAGE

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FACULTY OF ENGINEERING
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Name of Candidate: **Nassereddine Sabeur**

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A NEW SWITCHING ALGORITHM BASED ON SINGLE-PHASE MODULATOR FOR Z-SOURCE INVERTERS WITH REDUCED COMPUTATION TIME AND ENHANCED OUTPUT VOLTAGE

ABSTRACT

The inverter is one of the most common power electronics device used in industrial application. The main objective of the inverter is to produce an ac output waveform from a dc source. The main drawback of VSI is that the maximum output voltage obtained can never exceed the dc-link voltage. To obtain an output voltage higher than the input, an additional stage of dc/dc converter is required, which increases the cost of the system and decreases the efficiency. Recently, Z-source inverter (ZSI) is introduced to overcome the aforementioned disadvantages of VSI where a unique impedance network is coupled between the dc power source and the inverter main circuit. The obtained efficiency is higher due to the main feature of ZSI, which combines the advantages of buck/boost in one stage power conversion. Moreover, the reliability is improved due to the inclusion of the shoot-through (ST) interval, which is not allowed in VSI because it destroys the switching devices. The operation of ZSI has an additional ST state to boost the dc-link voltage besides the eight switching states in conventional converters, i.e. six active and two null vectors.

This study proposes a new unified control method for the Z-source inverter family (ZSI), also called the One Dimension for Z-Source Inverters (ODZSI) based on the Single-Phase Modulator technique. The attractiveness of the modulation method lies on its extreme simplicity. A simple mathematical model is necessary to develop the ODZSI, and the calculations relative to switching sequence and the duty-cycles determination are highly simplified. The ODZSI is proposed to modulate single-phase H-bridge ZSI. Then, the same concept is extended to modulate three-phase qZSI/ZSI. In addition, the ODZSI can be used to control different impedance-source topologies.

To achieve a maximum voltage gain, the ODZSI-MBC_3 is proposed. The shoot-through period is maximized by turning ON all the switches during the zero states, while the active states are kept unchanged. The obtained results using the ODZSI-MBC_3 are compared with those obtained with the carrier-based maximum boost control (CB-MBC), showing that the output voltage quality is enhanced with reduced computation burden.

In order to reduce the switching losses, the ODZI-MBC_1 is also proposed. By using a carefully selected shoot-through states, the number of the switching transition is significantly decreased as each switch is locked to the positive or negative dc-rail during a period of $2\pi/3$. Only two switches of the same leg will turn ON during the shoot through and the three ST times are distributed per two legs per control cycle. Additionally, as compared with space vector techniques, the inverter power losses are decreased, and the total execution time is reduced by 45%.

The obtained results ensure the feasibility and validate the performance of the ODZSI. Moreover, due to the simple structure of the proposed control scheme and the reduced total execution time, it can be easily implemented on a slow and cheap controller. The presented concepts have been verified in simulations using Matlab/Simulink and validated experimentally.

Keywords: Pulse width modulation, Z-source inverter (ZSI), shoot-through (ST) control, space-vector modulation, time-domain modulator

ALGORITMA PENSUISAN BARU BERDASARKAN MODULASI SATU FASA UNTUK KONVERTER SUMBER Z DENGAN PENGURANGAN MASA PERLAKUAN DAN PENAMBAHBAIKAN VOLTAN KELUARAN

ABSTRAK

Penyongsang kuasa adalah salah satu peranti elektronik kuasa yang biasanya digunakan dalam aplikasi perindustrian. Objektif utama penyongsang adalah menghasilkan keluaran gelombang ac dari sumber dc. Kelemahan utama VSI adalah voltan keluaran maksimum yang diperoleh tidak boleh melebihi voltan dc-link. Untuk mendapatkan voltan keluaran yang lebih tinggi daripada input, satu peringkat tambahan penukar dc / dc diperlukan, yang akan meningkatkan kos sistem dan mengurangkan kecekapan. Kebelakangan ini, penyongsang Z-sumber (ZSI) diperkenalkan untuk mengatasi keburukan VSI yang dinyatakan di atas di mana rangkaian galangan unik digabungkan antara sumber kuasa dc dan litar utama penyongsang. Kecekapan yang diperoleh adalah lebih tinggi disebabkan oleh ciri utama ZSI, yang menggabungkan kelebihan buck/boost dalam penukaran kuasa satu peringkat. Selain itu, relibiliti diperbaiki kerana kemasukan pengamiran masukan terus (ST), yang tidak dibenarkan dalam VSI kerana boleh memusnahkan peranti pensuisan. Pengoperasian ZSI mempunyai keadaan ST tambahan untuk meningkatkan voltan dc-link selain lapan keadaan pensuisan dalam penukar konvensional, iaitu enam aktif dan dua vektor null.

Kajian ini mencadangkan kaedah kawalan bersepadu bagi keluarga penyongsang Z-sumber (ZSI), yang juga dikenali sebagai Penyongsang Z-sumber Satu Dimensi (ODZSI) berdasarkan Teknik Modulasi Fasa Tunggal. Daya tarikan kaedah modulasi terletak pada kemudahan penggunaan. Model matematik yang mudah diperlukan untuk membangunkan ODZSI, dan perhitungan relatif terhadap kitaran dan penentuan kitaran telah dipermudahkan. ODZSI dicadangkan untuk memodulasi ZSI fasa tunggal ZSI. Kemudian, konsep yang sama diperluaskan untuk memodulasi tiga fasa qZSI / ZSI. Di

samping itu, ODZSI boleh digunakan untuk mengawal topologi sumber-sumber galangan yang berbeza.

ODZSI-MBC_3 dicadangkan untuk, mencapai gandaan voltan maksimum. Tempoh masukan terus dimaksimumkan dengan mengaktifkan semua suis semasa keadaan sifar, sementara keadaan aktif disimpan tidak berubah. Hasil yang diperolehi menggunakan ODZSI-MBC_3 dibandingkan dengan talian kawalan ransangan boost maksimum (CB-MBC), menunjukkan bahawa kualiti keluaran voltan dipertingkatkan dengan beban pengiraan yang dipermudahkan.

Untuk mengurangkan kehilangan pensuisan, ODZI-MBC_1 juga dicadangkan. Dengan menggunakan keadaan jenis masukan terus yang terpilih, bilangan peralihan pensuisan berkurangan dengan ketara memandangkan setiap suis ditentukan ke rangkaian dc positif atau negatif semasa tempoh $2\pi/3$. Hanya dua suis dalam rangkaian yang sama akan diaktifkan semasa mauskan terus dan tiga kali ganda ST akan diagihkan setiap kitaran kawalan dua rangkaian. Di samping itu, berbanding dengan teknik vektor ruang, kehilangan kuasa penyongsang dikurangankan, dan jumlah masa pelaksanaan dikurangkan sebanyak 45%.

Keputusan yang diperolehi menjamin kebolehlaksanaan dan mengesahkan prestasi ODZSI. Tambahan pula, disebabkan oleh strukturnya yang ringkas pada skim kawalan yang dicadangkan dan pengurangan tempoh masa perlaksanaan, membolehkan ia dilaksanakan pada pengawal yang pasif dan murah. Konsep yang dikemukakan telah disahkan secara simulasi menggunakan perisian Matlab/Simulink dan dibuktikan melalui eksperimen.

Kata kunci: denyut modulasi lebar jalur, penyongsang Z-sumber (ZSI), masukan langsung (ST), ruang vektor modulasi, modulator domain masa

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Nassereddine Sabeur.

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$\overrightarrow{V_1}$ and $\overrightarrow{V_2}$	:	Stationary Vectors
ac	:	Alternating Current
B	:	Boost factor
BZSI	:	Bidirectional Z-source inverter
CB-MBC	:	Carrier Based Maximum Boost Control
CB-PWM	:	carrier-based Pulse-Width-Modulation
CCM	:	Continuous Conduction Mode
CSI	:	Current Source Inverter
D	:	The shoot-through duty ratio
dc	:	Direct Current
DCM	:	Discontinuous Conduction Mode
EMI	:	Electromagnetic Interference
G	:	Voltage Gain
I_{ac}	:	Load current
IGBT	:	Insulated Gate Bipolar Transistor
IMN	:	Impedance Network
INT	:	Integer Function
I_{ph}	:	The average current flowing throw the switch
MBC	:	Maximum Boost Control
MCBC	:	Maximum constant Boost Control
MPC	:	Model Predictive Control
MSVPWM	:	Modified Space Vector Pulse-width Modulation
ODZSI	:	One Dimension for quasi Z- source Inverter
ODZSI-MBC_1	:	ODZSI based Maximum Boost Control for One-Leg Shoot-Through

ODZSI-MBC_3	:	ODZSI based Maximum Boost Control for three-Leg Shoot-Through
PAM	:	Pulse-Amplitude Modulation
PWM	:	Pulse Width Modulation
qZSI	:	Quasi- Z- Source Inverter
SBC	:	Simple Boost Control
SCR	:	Silicon-Controlled Rectifier
SDP	:	switch device power
SiC devices	:	Silicon Carbide devices
SL-SZI	:	Switched Inductor (SL) Z-Source Inverter.
SPWM	:	Sine Pulse-Width Modulation
SV-MBC	:	Space Vector Maximum Boost Control
S_x	:	Switching state
THD	:	Total Harmonic Distortion
T_{nst}	:	Non-shout- through time
T_s	:	Sampling time
T_{st}	:	Shout-Through time
V_{dc}	:	Dc Voltage fed the impedance source
V_{in}	:	Voltage across the main bridge
V_{LL}	:	Line voltage
V_{ph}	:	Phase voltage
VSC	:	Voltage Source Converter
VSI	:	Voltage Source Inverter
$V_{xg\text{-}ref}$	:	the line-to-ground reference voltage
ZSI	:	Z- Source Inverter
ZSVM	:	Z- source Space Vector Modulation
ZSVM	:	Z- source Space Vector Modulation

CHAPTER 1: INTRODUCTION

1.1 Introduction

In recent years, many efforts are made to research and use new energy sources because the potential for an energy crisis is increasing. Voltage source inverters (VSIs) have gained much attention in the area of energy distribution and control due to their advantages. The voltage/current inverter has been widely used in several applications such as adjustable speed drives (ASDs), uninterruptible power supplies (UPS), induction heating, ac power supplies , active power filters, flexible ac transmission systems (FACTSs), and voltage compensators, etc. However, the traditional inverters (voltage or current source fed) have some conceptual barriers and use limitations, which will be reviewed in the next sections. The presented Z-source inverter (ZSI) by (Fang Zheng Peng, 2003) can overcome these limitations due to its unique features.

1.2 Traditional Inverters

An inverter (power inverter) is an electrical device that converts dc power or direct current (dc) to ac power or alternating current (ac). This conversion is ensured by a modulating technique that controls the amount of time and the sequence used to switch the power devices to obtain the desired output voltage and frequency. There are two types of traditional inverters, namely voltage source (fed) inverters (VSI) and current source (fed) inverters (CSI).

1.2.1 Voltage Source Inverter (VSI)

The basic topology of the three-phase voltage source inverter is shown in Figure 1.1. The input to the inverter is a dc voltage source usually with a capacitor in parallel to absorb the high frequency current ripple. The inverter bridge consists of six switches with a freewheeling diode in parallel with each of them (Miaosen, 2006).

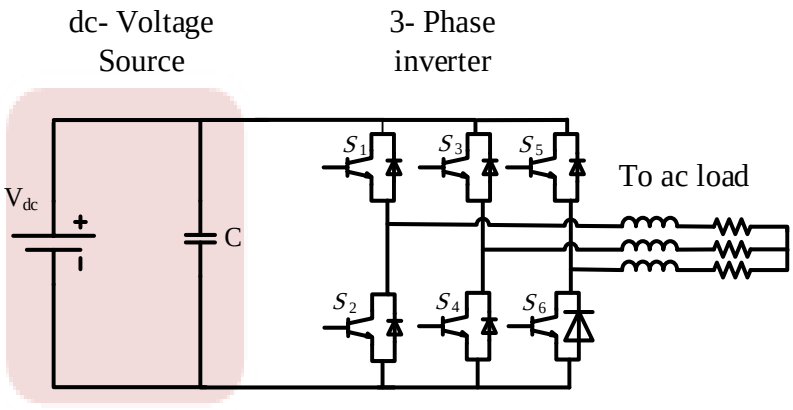


Figure 1.1: Basic Topology of Voltage Source Inverter.

1.2.1.1 Limitation of VSI

The voltage source inverter has the following conceptual and theoretical barriers and limitations.

i. The V-source inverter is a buck (step-down) inverter for dc-to-ac power conversion because the ac output voltage cannot exceed the dc-rail voltage. To obtain an output voltage higher than the input, an additional dc-dc converter is required which increases the size and the cost of the system and lowers efficiency. Moreover, the V-source converter is a boost (step-up) rectifier (or boost converter) for ac-to-dc power conversion.

ii. The upper and lower devices of each phase leg must not be gated ON simultaneously. Otherwise the devices will be destroyed. The shoot-through problem by electromagnetic interference (EMI) noise's misgating-on is a major killer to the converter's reliability. Therefore a dead time should be provided to block both upper and lower devices in the VSI, which causes waveform distortion, etc.

iii. An output LC filter is needed for providing a sinusoidal voltage compared with the current-source inverter, which causes additional power loss and control complexity.

1.2.2 Current Source Inverter

The basic topology of the traditional three-phase current-source inverter (abbreviated as CSI) is shown in Figure 1.2. A dc current source feeds the main inverter circuit. The dc current source can be a relatively large dc inductor fed by a voltage source. Six switches are used in the main circuit, each is traditionally composed of a semiconductor switching device with reverse block capability such as a gate-turn-off thyristor (GTO) and SCR or a power transistor with a series diode to provide unidirectional current flow and bidirectional voltage blocking (Fang Zheng Peng, 2003).

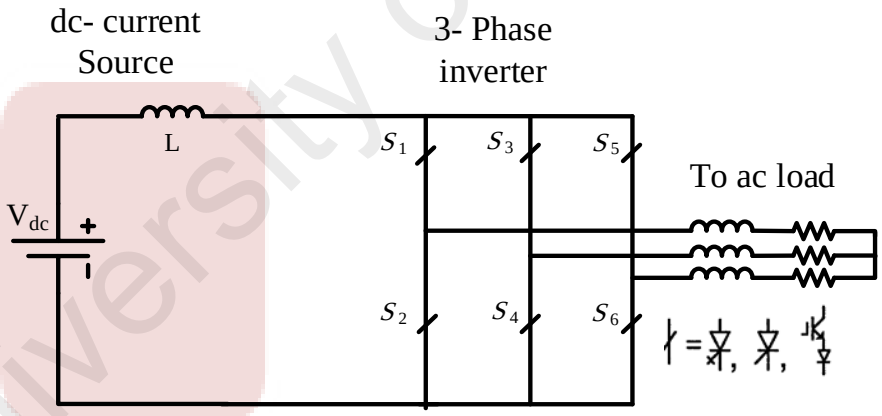


Figure 1.2: Current Source Inverter.

1.2.2.1 Limitation of CSI

The current source inverter has the following conceptual and theoretical barriers and limitations.

i. The current source inverter is a boost inverter for dc-to-ac power conversion and the I-source converter is a buck rectifier (or buck converter) for ac-to-dc power conversion.

   For applications where a wide voltage range is desirable, an additional dc–dc buck (or boost) converter is needed. The additional power conversion stage increases system cost and decreases the efficiency.

ii. At least one of the upper devices and one of the lower devices have to be gated ON and maintained ON at any time. Otherwise, an open circuit of the dc inductor would occur and destroy the devices. The open-circuit problem by EMI noise's misgating-off is a major concern of the converter's reliability. Overlap time for safe current commutation is needed in the current source converter, which also causes waveform distortion, etc.

iii. A series diode should be used in combination with the main switches of the current source converter such as insulated gate bipolar transistors (IGBTs) to block reverse voltage. This requires a high-performance IGBT modules and intelligent power modules (IPMs).

In addition, both the VSI and the CSI have the following common problems.

i. The obtainable output voltage range is limited to be either greater or smaller than the input voltage. Therefore, they are either a boost or a buck converter and cannot be a buck–boost converters.

ii. Their main circuits cannot be interchangeable. In other words, neither the VSI main circuit can be used for the CSI, nor vice versa.

iv. They are vulnerable to EMI noise in terms of reliability.

Consequently, solving the aforementioned shortcomings would benefit further industrial applications of Voltage/current source inverters.

1.3 Problem Statement

The conventional two-level voltage source inverter (VSI) is widely used in the industry for performing power conversion from dc to ac, the three-phase inverter bridge is fed from a dc source filtered by a relatively large capacitor connected in parallel. The VSI is a buck (step down) dc-ac converter. To obtain an output voltage higher than the dc input, an additional dc-dc converter is required which increases the size and the cost of the system. The recently proposed Z-source inverter presented in (Fang Zheng Peng, 2003) can overcome some of these limitations. An impedance-source network can be generalized as a two-port network with a combination of two basic passive linear elements, e.g. inductor (L) and capacitor (C). On the other hand, diverse derivations and modifications of the impedance network are possible by adding different non-linear elements in the impedance network, such as switches and diodes to ameliorate the performance of the circuit. Since the publication of the first impedance-source network in 2003, various topologies and control methods using different impedance-source networks have been presented in the literature with both buck and boost capabilities. Many control techniques, such as carrier-based PWM (CB-PWM) and modified space vector PWM (MSVPWM), have been proposed for controlling shoot-through in ZSI (U. S. Ali & Kamaraj; Barathy, Kavitha, & Viswanathan, 2014; Diab, Elserougi, Massoud, Abdel-Khalik, & Ahmed, 2016; Fang Zheng Peng, Shen, & Qian, 2005; Shen et al., 2006; K. Yu, Luo, & Zhu, 2012a) with the aim of achieving a wide range of modulation, less commutation per switching cycle, low device stress, higher efficiency, and simple implementation. A considerable work have been done on this subject, especially for the PWM control methods. However, with the point of view of the practical implementation, the modified space vector PWM method is very complex and needs longer calculation time than any other methods which cannot be implemented on slow DSP controllers. Furthermore, different topologies have been derived from the basic topology depending

on the application. The research on impedance source networks is accelerating because there is no one-size-fits-all solution in practical use when considering cost, simplicity, and performance. Each topology and control method may find a niche for certain application.

1.4 Objectives

The goal of this research is to propose a new switching algorithm for impedance-source inverters with accurate switching pattern and reduced calculation effort for easy implementation with slower controllers. The research objectives of this work can be broadly classified as:

i. To propose a new time-domain duty-cycle computation techniques for single and three-phase impedance-source topologies called the One Dimension for ZSI (ODZSI).
ii. To validate the proposed control strategies through simulation and experimental verifications under different conditions.
iii. To compare the performance of the proposed control schemes with the exciting control methods.
iv. To minimize the computational burden of the algorithm, and enhance the output voltage waveform.

1.5 Outline of the thesis

Chapter 2 provides a survey of the well-known impedance-source networks, and it is organized as follows: the first section focuses on the research advances in developing the most popular impedance-source topologies, where the basic Z-source inverter circuits are well addressed. Other recent inverter topologies, its topological advances, disadvantages, and their potential applications are distinctly presented. In section two, the most applicable

modulation techniques for impedance source single and three-phase topologies are presented and compared based on their complexity and conversion functionality.

Chapter 3 presents a new control schemes for Z-source and quasi Z-source inverters, the schemes are applied for both single and three-phase topologies. The fundamental and operation principles of the proposed control techniques, the mathematical details regarding the development of these strategies are provided. Moreover, the implantation of maximum boost control based ODZSI is discussed in details starting with determination of the V_{ref}, the calculation of the dwell times of the stationary vectors till identifying the signal gates for the switches.

Chapter four deals with the experimental implementations of the proposed control schemes. The experimental test results are provided in this chapter. All proposed control strategies have been experimentally verified. Switching signals, voltage and current measurements have been presented to demonstrate the feasibility and performance of the proposed control strategies. In this chapter also, the results have been discussed. The presented modulation schemes were compared with other counterparts. Finally, the semiconductor losses in the inverter were calculated using the PLECS libraries coupled to the Matlab/Simulink platform. The conduction and switching losses using different control strategies for qZSI were studied.

The last chapter includes concluding remarks, the contribution of thesis and the recommended suggestions for the future work.

CHAPTER 2: REVIEW OF IMPEDANCE-SOURCE INVERTER TOPOLOGIES AND RELEVENT CONTROL TECHNIQUES

2.1 Introduction

Many impedance-source network topologies and wide variety of control methods have been developed in the recent literature. This chapter critically reviews the research advances in developing the impedance-source network topologies and their modulation techniques. Basic impedance-source network circuits such as Z-source inverter, quasi Z-source inverter, semi Z-source/ quasi Z-source inverters are well addressed. Other innovative inverter topologies, its topological advances, disadvantages, and their potential applications are distinctly presented. Then, a look is taken at the most recent impedance-source network configurations. In this chapter also the widely used and well-known modulation PWM methods for impedance-source single-phase and three-phase inverters are taken into account and compared based on their complexity and conversion functionality.

2.2 Impedance source network topologies

The impedance source network concept has gained increasing attention and different converter topologies with buck, boost, buck-boost, unidirectional, bidirectional, isolated as well as non-isolated converters have been used in several applications, such as wind power generation (Ramasamy, Palaniappan, & Yakoh, 2013; Supatti & Peng, 2008), photovoltaic systems (Ahmed & Mekhilef, 2015; Erginer & Sarul, 2014; Hanif, Basu, & Gaughan, 2011; Y. Huang, Shen, Peng, & Wang, 2006; Husev, Roncero-Clemente, Romero-Cadaval, Vinnikov, & Jalakas, 2016; Liang, Liu, Ge, & Abu-Rub, 2017; Moinoddin, Abu-Rub, & Iqbal, 2013; Yushan, Baoming, Abu-Rub, & Fang Zheng, 2014), uninterruptible power supply (UPS) (Kulka & Undeland, 2008; Z. J. Zhou, Zhang, Xu, & Shen, 2008), distributed generation (Abu-Rub et al., 2013; Ge et al., 2013; Y. Li,

Anderson, Peng, & Liu, 2009; Y. Li, Jiang, Cintron-Rivera, & Peng, 2013; Siwakoti & Town, 2013), battery storage (Cintron-Rivera, Li, Jiang, & Peng, 2011; J. Liu, Jiang, Cao, & Peng, 2013; Navas, G, Puma, A, & Filho, 2016), electrical drive systems (Ellabban & Abu-Rub, 2013; Tenner, Gunther, & Hofmann, 2013; Vijay, Shruthi, Kini, Viswanatha, & Bhatt, 2014), flywheel energy storage systems (Amodeo, Chiacchiarini, & Oliva, 2012), electronic loads (Rosas-Caro, Peng, Cha, & Rogers, 2009), dc circuit breaker (K. A. Corzine & Ashton, 2012), wireless power transfer (Wang, Liu, Tang, & Ali, 2017) and others (Siwakoti, Fang Zheng, Blaabjerg, Poh Chiang, & Town, 2015).

Different power converter topologies with impedance-source networks have been derived from the basic topology depending on their applications, *e.g*. quasi Z-source (Anderson & Peng, 2008; Y. Li et al., 2013), Γ-Z-source (Loh, Li, & Blaabjerg, 2012, 2013; Mo, Loh, & Blaabjerg, 2014), T-source (Strzelecki, Adamowicz, Strzelecka, & Bury, 2009), Trans Z-source (D. Li, Loh, Zhu, Gao, & Blaabjerg, 2013a; Qian, Peng, & Cha, 2011), TZ-source (Nguyen, Lim, & Kim, 2013), LCCT Z-source (Adamowicz, Strzelecki, Peng, Guzinski, & Rub, 2011), TSTS Z-source (L. Huang, Zhang, Hang, Yao, & Lu, 2013), semi Z-source/quasi Z-source (Dong Cao, Shuai Jiang, Xianhao Yu, & Fang Zheng Peng, 2011a; Dong Cao, Shuai Jiang, Xianhao Yu, & Fang Z Peng, 2011b), capacitor diode assisted (Gajanayake, Luo, Gooi, So, & Siow, 2010), intermediate-transformer-isolated Z-source (Jiang, Cao, & Peng, 2011), distributed Z-source(Cha, Peng, & Yoo, 2010; Fang Z Peng, 2008), switched inductor/capacitor (Nguyen, Lim, & Cho, 2011; Zhu, Yu, & Luo, 2010), embedded Z-source (Gao, Loh, Li, & Blaabjerg, 2011; Loh, Gao, & Blaabjerg, 2010), enhanced/improved Z-source (Cai, Qu, & Zhang, 2013; D. Li, Loh, Zhu, Gao, & Blaabjerg, 2013b) , and finally also Y-source(Siwakoti, Loh, Blaabjerg, & Town, 2014). Each topology has a unique features for different or particular applications. The research on this area is growing rapidly and the main focus

is: to reduce the Z-source network size and rate, to achieve higher power density, to extend the voltage gain range and design an optimized and robust controllers.

Figure 2.1 shows the general configuration of an impedance source network for electric power conversion.

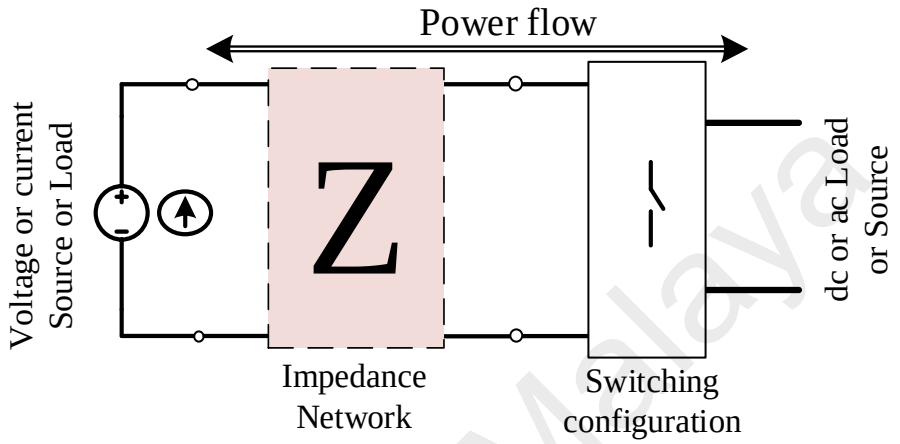


Figure 2.1: A general circuit configuration of an impedance-sourced network for power electronic conversion.

The impedance-source network is broadly classified into two categories based on magnetics: a) non-transformer based, and b) coupled or transformer based as shown in Figure 2.2. Each topology has distinct features and may find a niche for certain application.

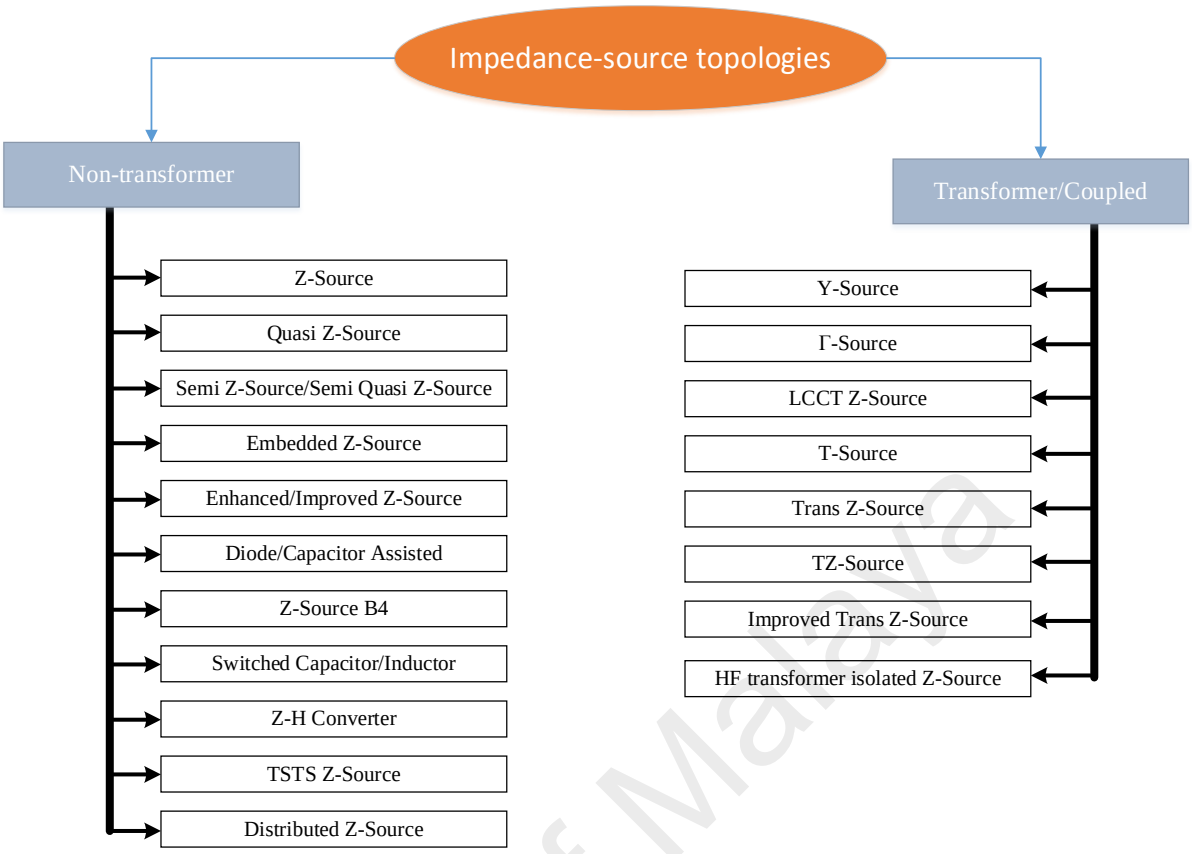


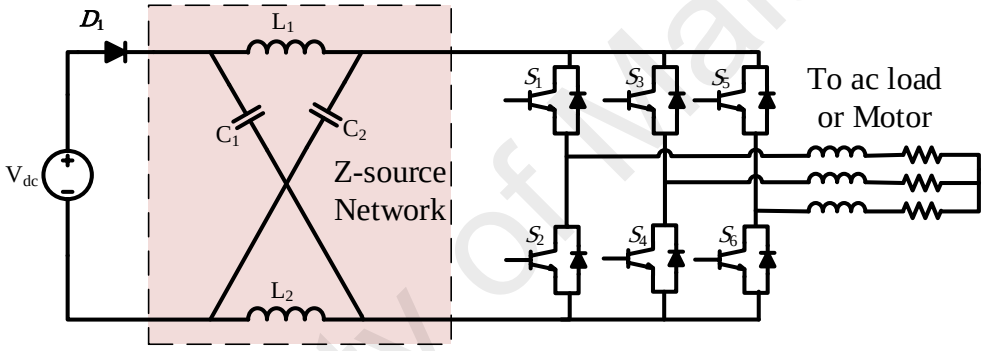
Figure 2.2: Categorization of Impedance-source topologies.

All impedance-source topologies are mainly derived from the Z-source network by modifying the original impedance network, or by rearranging the connections of inductors and capacitors. Each Z-source network topology yields unique features for different or particular application needs.

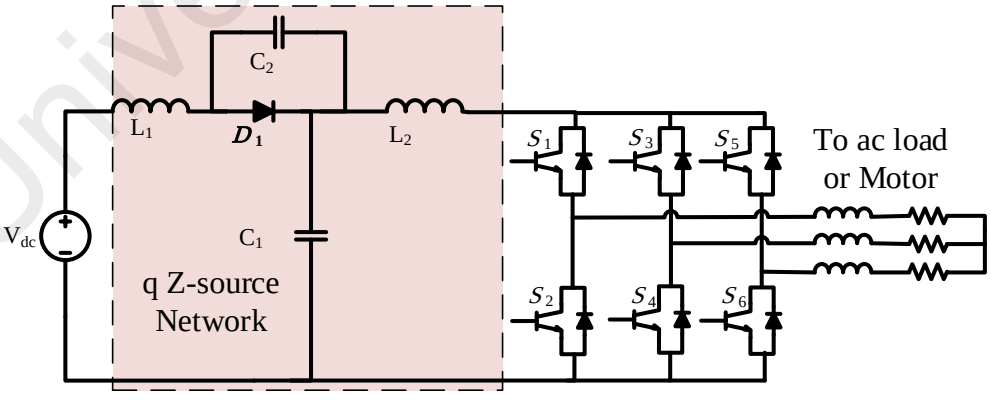
2.2.1 Z-Source/ Quasi Z-Source

Z-source converters are broadly classified into two types, voltage-fed and current-fed. However, unlike the traditional voltage-fed/current-fed inverter, the impedance source network provides a buffer between the source and the inverter bridge and facilitates a short and an open circuit at any time depending on the mode of operation. Traditional voltage-fed Z-Source impedance networks in Figure 2.3 (a) has some drawbacks that resulted in decreasing the converter efficiency, such as unidirectional power flow, high

inrush current during starting, a discontinuous input current, higher Z-network capacitor voltage, isolated source, and inverter dc rail. Various voltage -fed topologies derived from ZSI and qZSI (Figure 2.3 b, c & d) with improved performance were proposed by (Yushan Liu, Ge, Abu-Rub, & Peng, 2013; Loh, Gajanayake, Vilathgamuwa, & Blaabjerg, 2008; Yu Tang, Shaojun Xie, & Jiudong Ding, 2014; Yang, Peng, Lei, Inoshita, & Qian, 2011) to solve the problem of ZSIs. Moreover, the authors in (Guo et al., 2013) proposed a bidirectional qZSI (BqZSI) by replacing the input diode by an active switch S_7 with a parallel diode as shown in Figure 2.3 (d). Through proper control of the switch S_7, the bidirectional power flow can be achieved.



(a)



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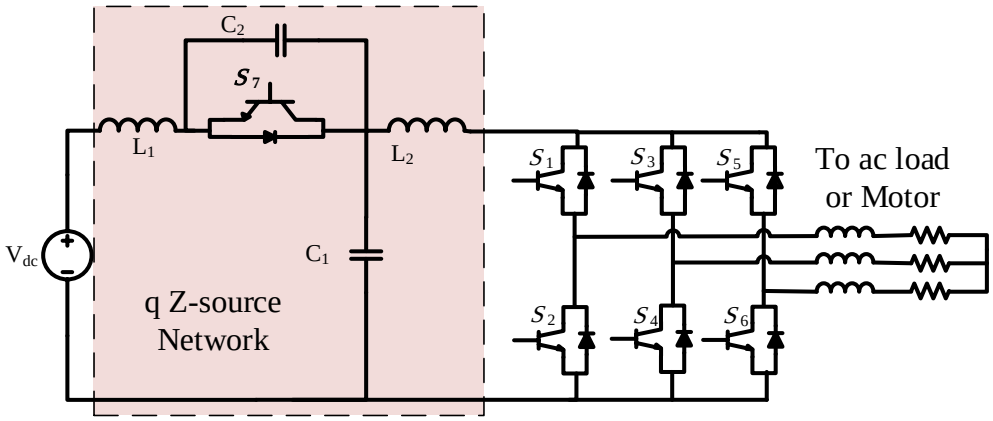
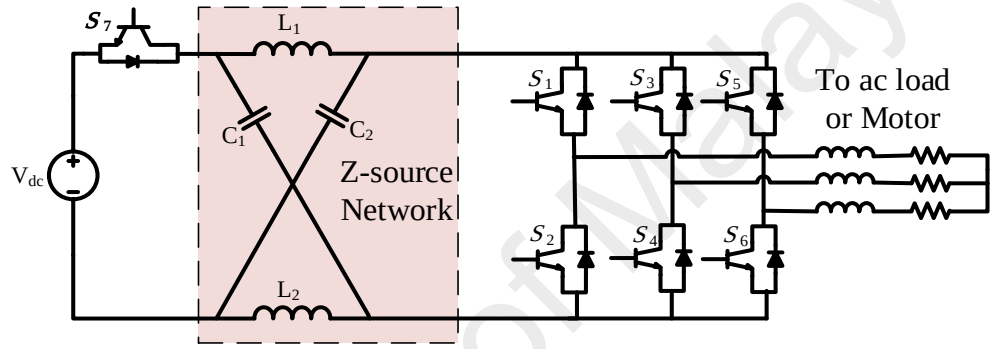


(c)



(d)

Figure 2.3: (a) ZSI with discontinuous input current; **(b)** qZSI with continuous input current; **(c)** BqZSI, and **(d)** BSZI.

In addition, the basic topology of ZSI can be changed into a bidirectional ZSI (BZSI), as shown in Figure 2.3 (d), by the replacement of input diode D_1 by a bidirectional switch S_7. This operates during the regenerative mode in the same way as the diode during the inverter mode, and its gate signal is the complement of the ST signal. The BZSI is able to exchange energy between ac and dc energy storages in both directions. There is no need for additional sensors or control circuits because the cost of the ZSI improvement is very low (Rabkowski, 2007).

2.2.2 Enhanced/Improved Z-Source

Various modifications are proposed within the Z-source and quasi Z-source networks to improve the boost capability of impedance source networks. In the same context, an enhanced-boost Z-source inverter is proposed in (Cai et al., 2013; D. Li et al., 2013b) with alternate-cascaded switched and tapped-inductor cells using some lower-rated components. Likewise, an improved Z-source is proposed in (Tang, Xie, & Zhang, 2011a) and plotted in Figure 2.4. Compared to previous Z-source inverter topology, it can reduce the Z-source capacitor voltage stress greatly, and has an inherent imitation to inrush current. Moreover, Soft-start strategy has been also proposed to avoid the inrush current and resonance between the Z-capacitors and the Z-inductors.

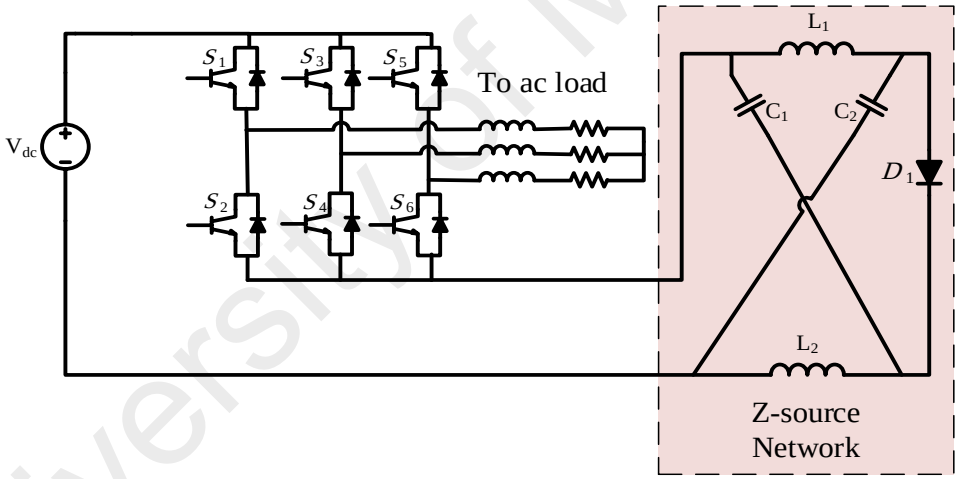
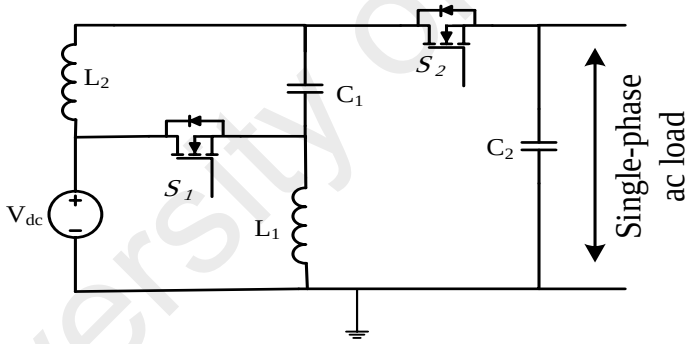


Figure 2.4: Improved Z-source inverter topology.

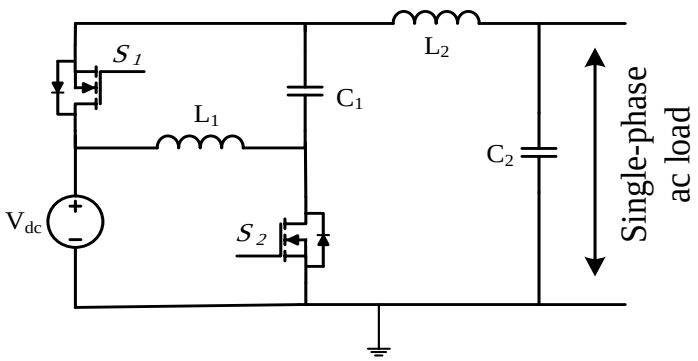
2.2.3 Semi-Z-Source/Semi-Quasi Z-Source

Several single-phase non-isolated semi-Z-source inverters for small distributed power generator in grid-connected applications with low cost and doubly grounded features have been presented in (Cao et al., 2011a; Cao et al., 2011b) and depicted in Figure 2.5. These semi-Z-source inverters employ the Z-source/quasi-Z-source network and only two active switches to achieve the same output voltage as the traditional voltage-fed full-bridge inverter. The two active switches of the semi-Z-source inverter are controlled

complementarily. Unlike the traditional ZSI/qZSI, a shoot-through state is not applicable to a semi-Z-source. By operating switch S_1 with duty cycle changing from 0 to 2/3, the inverters is able to output the same voltage range ($+V_{dc}$ to $-V_{dc}$) as the full-bridge inverter. When the duty cycle of S_1 changes from (0 to 0.5), the inverter can output the positive output voltage; when the duty cycle of S_1 changes from (0.5 to 2/3), and the inverter can output the negative output voltage. When the duty cycle is equal to 0.5, the semi-Z-source inverters are able to output zero voltage. The input dc source and the output ac voltage of the semi-Z-source inverter share the same ground, thus leading to less leakage ground current advantages over other non-doubly grounded inverters, such as voltage fed full-bridge inverter. A modified modulation technique SPWM (see 2.3.1) for semi-Z-source inverter is used to get the desired duty cycle to generate a sinusoidal output.



(a)



(b)

Figure 2.5: (a) Semi Z-source inverter, and **(b)** Semi-quasi-Z-source inverter topologies.

The advantage of the semi-Z-source and semi-quasi-Z-source inverters is that they can be implemented using fewer switches compared to a traditional ZSI and qZSI, however, the voltage stress on the switching devices is high. This topology is suitable for a grid-connected micro-PV inverter with high-voltage SiC devices.

2.2.4 Embedded Z-Source

The embedded Z-source (EZ-source) was proposed in (Loh et al., 2010) using an impedance network with the relevant dc sources embedded within. Comparing with the Z-source inverters, the embedded EZ-source inverters have the advantages of drawing a smoother current from the dc input sources without using external second-order filters and a lower required capacitive voltage. These advantages are attained with no degradation in gain, diode blocking voltage, and other characteristic properties of the X-shaped impedance network for the same specified shoot-through duration. With slight modification introduced, an alternative family of dc-link EZ-source inverters can also be implemented with an even lower network capacitive voltage attained at the expense of no inherent inductive filtering, a noisier source current waveform even under no voltage boosting condition, and the presence of a small negative capacitive voltage. Furthermore, the EZ-source inverter has been divided into an asymmetrical and a symmetrical structure, depending on whether one or two dc sources are inserted to the X-shaped impedance network (Gao et al., 2011). Figure 2.6 shows the circuit topology of a two-level embedded Z-source inverter. There are other similar embedded topologies with one or two dc sources suitable for battery storage systems.

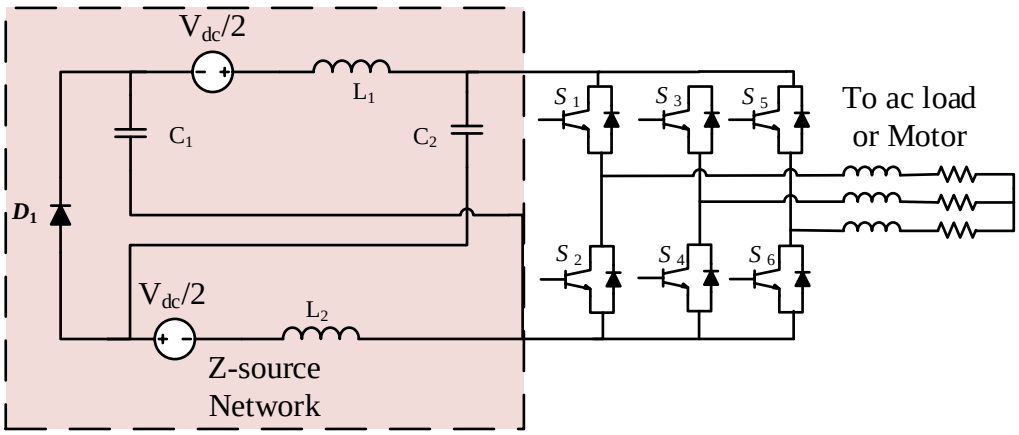


Figure 2.6: Two-level Embedded Z-source inverter.

2.2.5 Z-H Converter

A new kind of power converter, Z-H converter, is proposed in (F. Zhang, Peng, & Qian, 2008). The Z-H converter has similar operating concept to the Z-source inverter but has a different structure as shown in Figure 2.7. This topology has different features compared to Z-source inverter. There's no shoot-through switching state in the Z-H converter and the front end diode is eliminated. The gain of the converter is similar to that of the Z-source network but it has two modes of operation, i.e. boost mode in D = [0, 0.5] with positive output voltage and boost mode in D = [0.5, 1] with negative output voltage. The energy transfer can be bidirectional in Z-H converter and it can be applied to dc-dc, dc-ac, ac-dc, and ac-ac power.

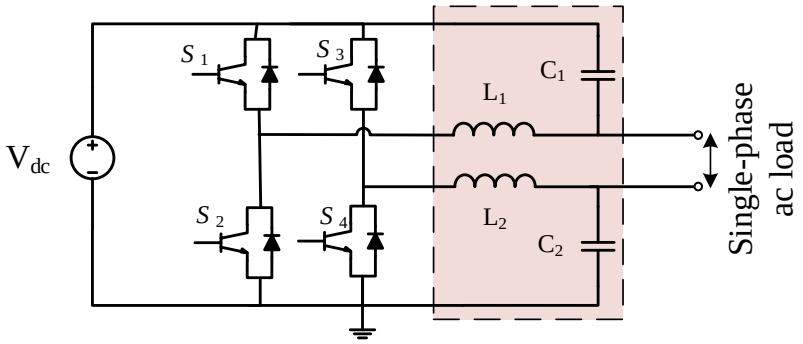


Figure 2.7: Z-H inverter.

2.2.6 Z-Source B4 Converter

Inspired by the traditional B4 VSI, a B4 Z-source and "inverted" Z-source inverters that can perform voltage buck-boost operation with the use of reduced active semiconductor switches, enhanced reliability and lower cost have been proposed in (Loh, Duan, Liang, Gao, & Blaabjerg, 2007). Using only passive clamping diodes introduces a unique shoot-through state, whose phase output voltages are all forced to zero. Tapping from knowledge that active states of a B4 inverter always oppose each other to give an interval of zero average voltages, modulation scheme for controlling the proposed B4 inverters is carefully formulated with shoot-through states replacing equal durations of the (0, 0) and (1, 1) states for voltage boosting and to give an unaltered volt-sec average per switching cycle.

Figure 2.8 shows the Z-source B4 inverter topology for a three-phase power conversion.

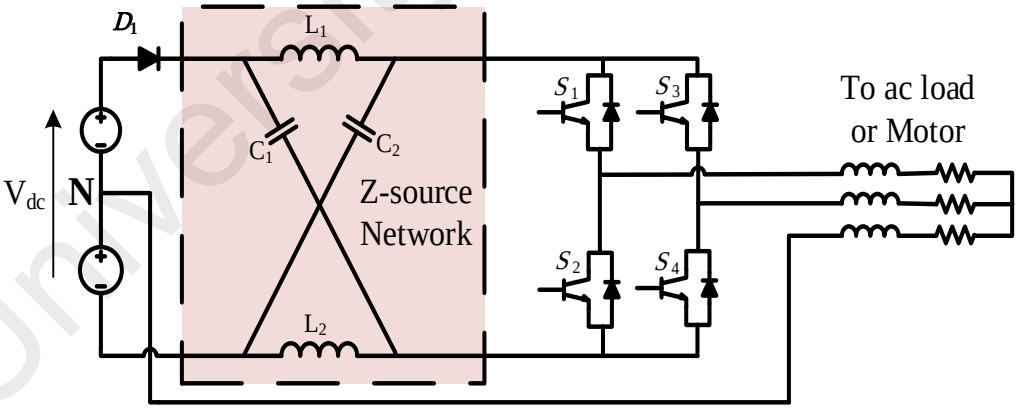


Figure 2.8: B4 Z-source inverter topology.

2.2.7 Switched Inductor

A developed impedance-type power inverter termed the switched inductor (SL) Z-source inverter is proposed in (Nguyen et al., 2011; Zhu et al., 2010), this inverter employs a unique SL impedance network to couple the main circuit and the power source to enlarge voltage adjustability as shown in Figure 2.9. Compared with the classical Z-source inverter, the proposed inverter increases the voltage boost inversion ability significantly. Only a very short shoot-through zero state is required to obtain high voltage conversion ratios, which is beneficial for improving the output power quality of the main circuit. In addition, the voltage buck inversion ability is also provided in this inverter for those applications that need low ac voltages. A switched inductor ZSI/qZSI provides continuous input current and reduced voltage stress on the capacitor. Similar to the classical Z-source inverter, the concepts of SL Z-source inverter can be applied to various applications of dc–ac, ac–ac, dc–dc, and ac–dc power conversion.

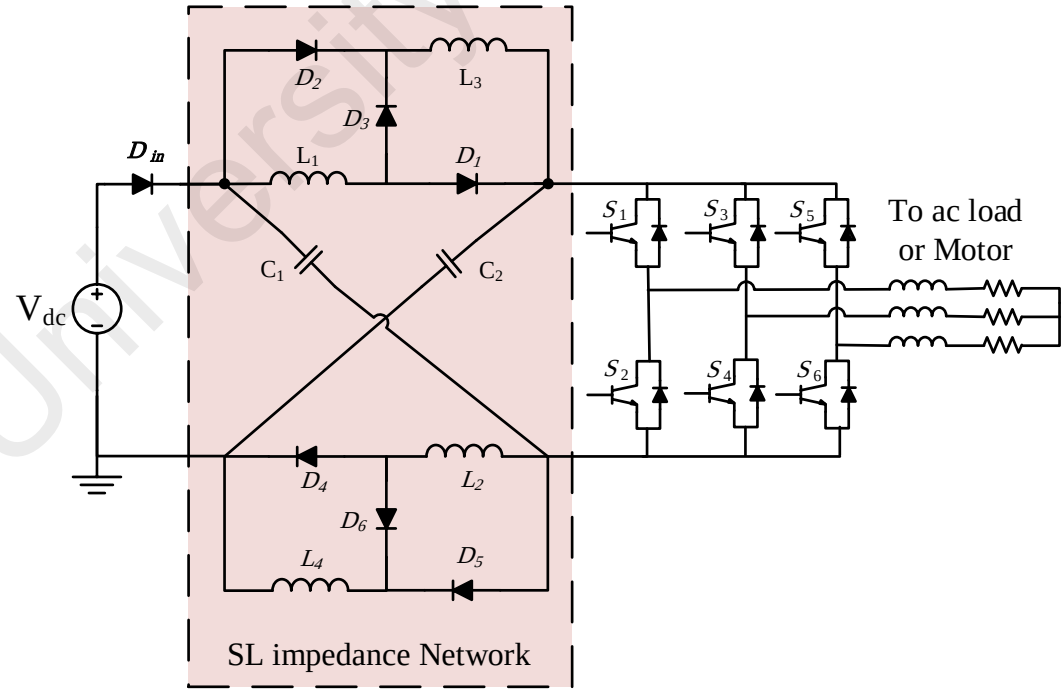


Figure 2.9: Topology of SL Z-source inverter.

Impedance source networks have added a new chapter in the field of power electronics with their unique features and properties that overcome most of the problems faced by traditional converter topologies. All the above circuit modifications aims to improve the performance of the basic ZSI and avoid its drawbacks. Furthermore, they do not have any effect on the voltage gain of the ZSI.

The different impedance source network topologies predominant in the literature are summarized in Table 2.1(Ellabban & Abu-Rub, 2016, Siwakoti, Fang Zheng, Blaabjerg, Poh Chiang, Town, et al., 2015), it appears that the BqZSI is the most improved ZSI topology, which gives the best performance with just replacing the input diode by a bidirectional switch and rearranging the Z-network elements. A close study of all the relevant topologies reveals that the modifications are motivated by one or more of the following reasons: **1)** to increase the boost; **2)** to increase the reliability of the system; **3)** to reduce the voltage stress on the active and passive devices; **4)** to better utilize the input voltage (dc-link); and **5)** to reduce the size and number of both active and passive devices etc.

Table 2.1. Summary of impedance source network topologies**.**

Impedance Network Topology	Boost Factor	Voltage Stress on the Switching Device	No. of Semicon-ductors	No. of Capa-citors	No. of Induc-tors	Features
Z-Source (Fang Zheng Peng, 2003)	$B = \frac{1}{1-2d_{st}}$	$\frac{1}{1-2d_{st}} V_{dc}$	1 diode	2	2	• Elementary circuit to overcome the conceptual and theoretical barrier of VSI and CSI • Discontinuous input current and higher voltage stress on capacitors.
Quasi Z-Source (Anderson & Peng, 2008)	$B = \frac{1}{1-2d_{st}}$	$\frac{1}{1-2d_{st}} V_{dc}$	1 diode	2	2	• First modification of Z-source network. • Continuous and discontinuous input current. • Reduced passive component ratings.
BqZSI (Guo et al., 2013)	$B = \frac{1}{1-2d_{st}}$	$\frac{1}{1-2d_{st-max}} V_{dc}$	1 switch with parallel diode	2	2	• Common grounding of the input power source and the dc link. • Reduced leakage currents • Reduced passive component ratings. • Bidirectional power flow.

Table 2.1: Continued

Improved Z-Source (Tang et al., 2011a)	$B = \frac{1}{1-2d_{st}}$	$\frac{1}{1-2d_{st}}V_{dc}$	1 diode	2	2	• Can reduce the Z-source capacitor voltage stress greatly • Has an inherent limitation to inrush current. • Same control strategies as ZSI/qZSI
Semi Z-Source (Cao et al., 2011a; Cao et al., 2011b)	$B = \frac{1-2d}{1-d}$	$\frac{1}{1-d}V_{dc}$	2 switches	2	2	• Reduced active components count. • Lower cost. • Common ground to load. • Higher voltage stress across switches compared to ZSI/qZSI. • Eliminate leakage currents and suitable for grid-connected PV system. • No shoot-through state.
Embedded Z-Source (Loh et al., 2010), (Gao et al., 2011)	$B = \frac{1}{1-2d_{st}}$	$\frac{1}{1-2d_{st}}V_{dc}$	1 diode	2	2	• Produces a smoother and smaller current/voltage maintained across the dc input source and within the impedance network without adding additional components or passive filter.
Z-H Converter (Loh et al., 2007).	$B = \frac{1}{1-2d_{st}}$	$\frac{1}{1-2d_{st}}V_{dc}$	4 switches	2	2	• The basic operating principle of Z-H converter and Z-source inverter are similar. • Employs an impedance network similar to that in the Z-source inverter but with different connection. • Front-end diode is eliminated. • No shoot-through state for voltage boosting. • The Z-H converter can be applied to dc-dc, dc-ac, ac-dc, and ac-ac power conversion.
Z-Source B4 (Loh et al., 2007)	$B = \frac{1}{1-2d_{st}}$	$\frac{1}{1-2d_{st}}V_{dc}$	1 diode	2	2	• Reduce the number of active semiconductors. • Lower cost • Simplify the control and gating circuitries. • Configured to actively supply two phases of a three-phase load with the third phase passively clamped using clamping diodes.
Switched Inductor (Nguyen et al., 2011; Zhu et al., 2010)	$B = \frac{1+D}{1-3D}$	$\frac{1+D}{1-3D}V_{dc}$	7 diodes	2	4	• Higher voltage boost and lower voltage stress across the capacitor compared to ZSI/qZSI. • Number of components increases with corresponding size and cost.

2.3 Modulation techniques and Control Methods for impedance-source topologies

Various modulation techniques, such as carrier-based PWM (CB-PWM) , modified space vector PWM (MSVPWM) and model predictive control (MPC) have been proposed for controlling the Z-source impedance network (Abdelhakim, Davari, Blaabjerg, & Mattavelli, 2017; U. S. Ali & Kamaraj; Bakeer, Ismeil, & Orabi, 2016; Barathy et al., 2014; Bayhan, Abu-Rub, & Balog, 2016; Diab et al., 2016; Y. Huang et al., 2006; Y. Liu, B. Ge, H. Abu-Rub, H. Sun, et al., 2016; Fang Zheng Peng et al., 2005; Poh Chiang, Vilathgamuwa, Yue Sen, Geok Tin, & Yunwei, 2005; Sajadian & Ahmadi, 2016; Shen et al., 2006; Yu Tang et al., 2014; K. Yu et al., 2012a; Y. Zhang et al., 2017) with the aim of achieving a wide range of modulation, less commutation per switching cycle, low device stress and simple implementation. Since the ZSI was proposed in 2003, considerable work have been done on this subject, especially for the PWM control methods.

Figure 2.10 (see next page) shows a broad categorization of modulation techniques for ZSI presented so far (Siwakoti, Fang Zheng, Blaabjerg, Poh Chiang, Town, et al., 2015).

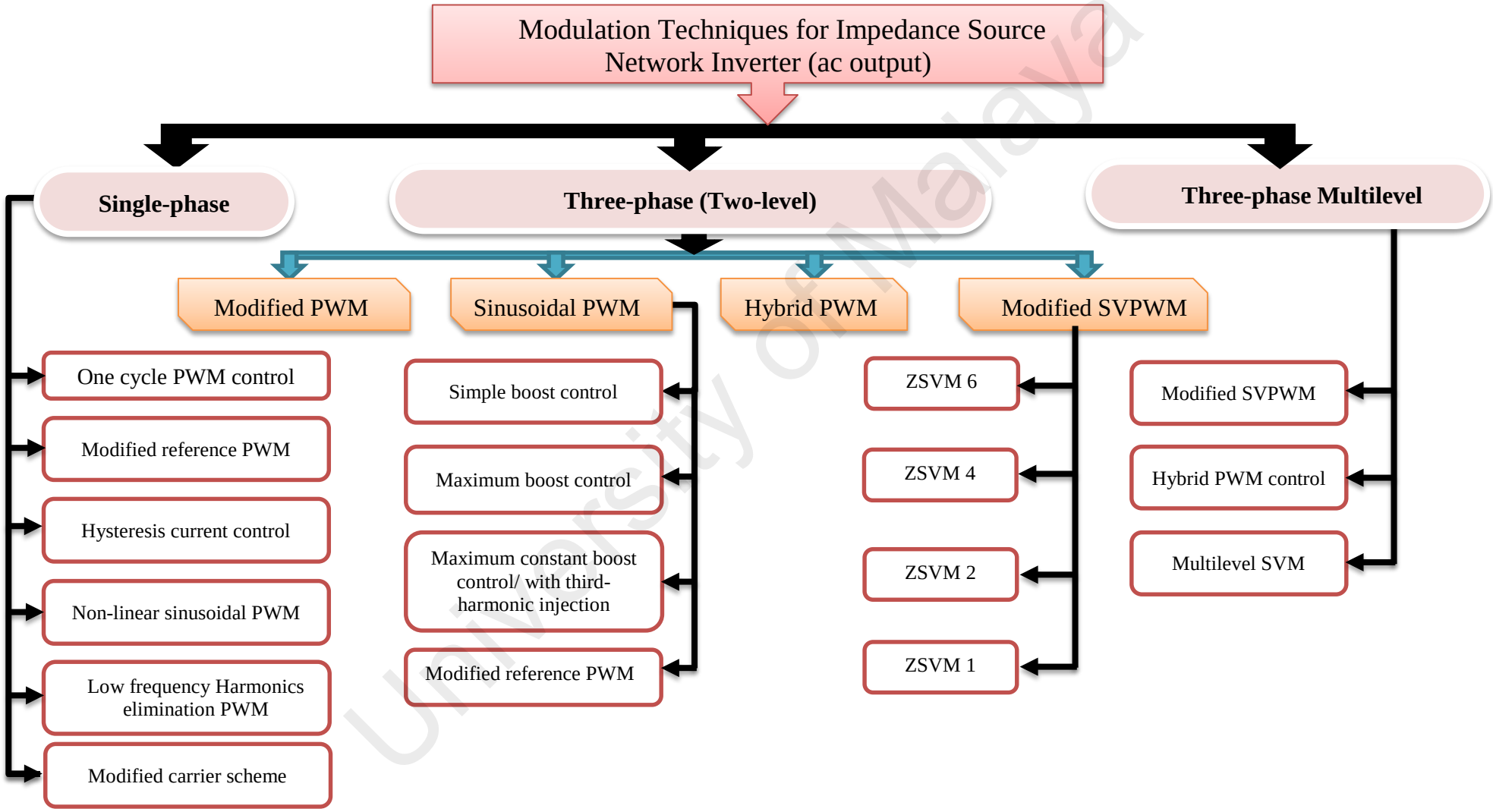


Figure 2.10: Categorization of modulation techniques for impedance source topologies.

2.3.1 Modulation Techniques for Single-Phase Topologies

Many control techniques have been proposed to control the output voltage of single-phase inverter based impedance source topologies having two switches (semi-Z-source (Cao et al., 2011a), quasi-Z-source (Tang, Xie, & Zhang, 2011b)) , four-switches (Cao et al., 2011a), (Poh Chiang et al., 2005), (Zare & Firouzjaee, 2007), or embedded Z-source (Cao et al., 2011a), (Oh et al., 2013) for different applications. The two modulation techniques called the nonlinear Sinusoidal Pulse-Width Modulation (SPWM) (Cao et al., 2011a) and one-cycle control (Tang et al., 2011b) are the most popular modulation schemes to control the two-switch topologies that offer a low-cost and simple solution for a single-phase grid-connected photovoltaic systems.

For semi-Z-source inverter proposed in (Cao et al., 2011a), the two switches are controlled complementary using a non-linear sinusoidal reference signal $v^* = 1/(2 - M\sin\omega t)$ which is compared to a carrier signal as shown in Figure 2.11. When the reference is greater than the carrier, switch S_2 is turned ON; otherwise, S2 is turned OFF. And the gate signal of S_1 is complementary with switch S_2. The same principal has been used for controlling a single-phase embedded Z-source inverter with four switches (Oh et al., 2013).

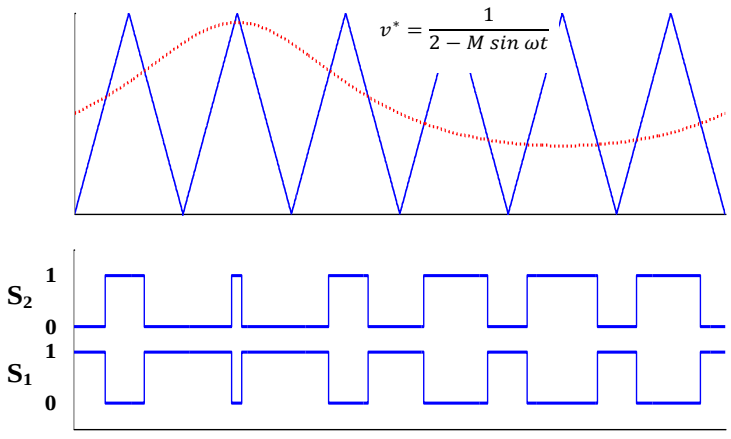


Figure 2.11: modified SPWM method for semi-Z-source inverters.

The one-cycle control strategy is presented in (Tang et al., 2011b) to control a single-phase semi-Z-source inverter. The two switches S_1 and S_2 work complementary, a clock signal (CLK) is used to switch ON any one switch. When the clock signal arrives, S_1 is turned OFF and S_2 is turned ON. Then V_{ds} (S_1) is integrated from zero and when the integration value attains ($V_i - v_{ref}$) , the integrator resets. S_1 is then turned ON and S_2 is turned OFF as shown in Figure 2.12. This control scheme is insensitive to the system model, which offers a high-efficiency constant-frequency control. However, the stress across the devises is high and this method is limited to two-switch impedance network topologies.

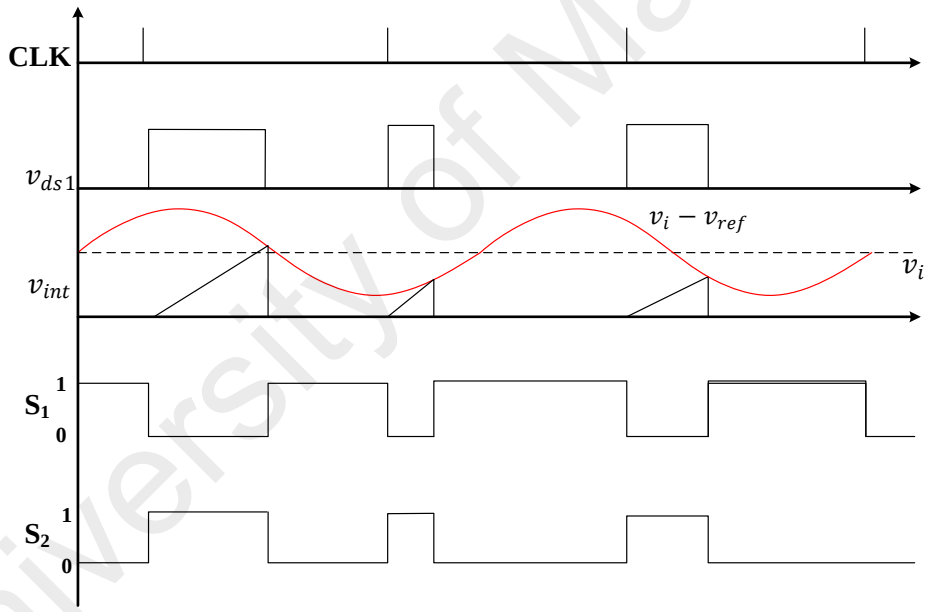
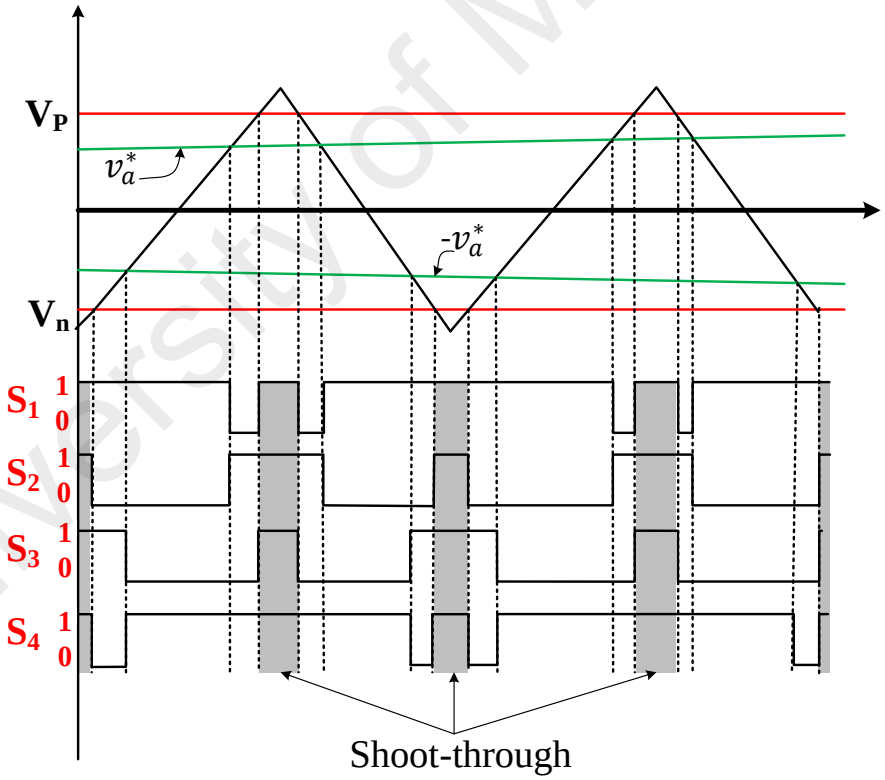


Figure 2.12: Principle waveforms of one-cycle control strategy.

In (Y. Huang et al., 2006) the authors proposed a PWM strategy for H-bridge qZSI, the two phase legs are modulated by SPWM for synthesizing the desired ac output, and the ST duty ratio is controlled by two straight line V_{sp} and V_{sn}. The ST period is distributed into two parts in each switching cycle T_s, as a result each switch will turn ON and OFF twice in every carrier cycle which leads to increase the switching losses. To enhance the

system efficiency, a modified PWM strategy for a single-phase module integrated inverter designed for a photovoltaic system is introduced in (L. Liu, Li, & Zhou, 2013) where the ST period is merged into one part by replacing the triangular carrier with a sawtooth carrier, hence each switch needs to switch ON and OFF only once per carrier cycle which results in lower switching loss and improved system efficiency during boost operation. However, merging the ST time into one part leads to double the current ripple in the inductors, therefore, the inductor size will increase compared to that of triangular carrier based method in order to keep the same inductor ripples. Consequently, the modified PWM is suitable for high-frequency applications (L. Liu et al., 2013). The principal of this control scheme is shown Figure 2.13.



(a)

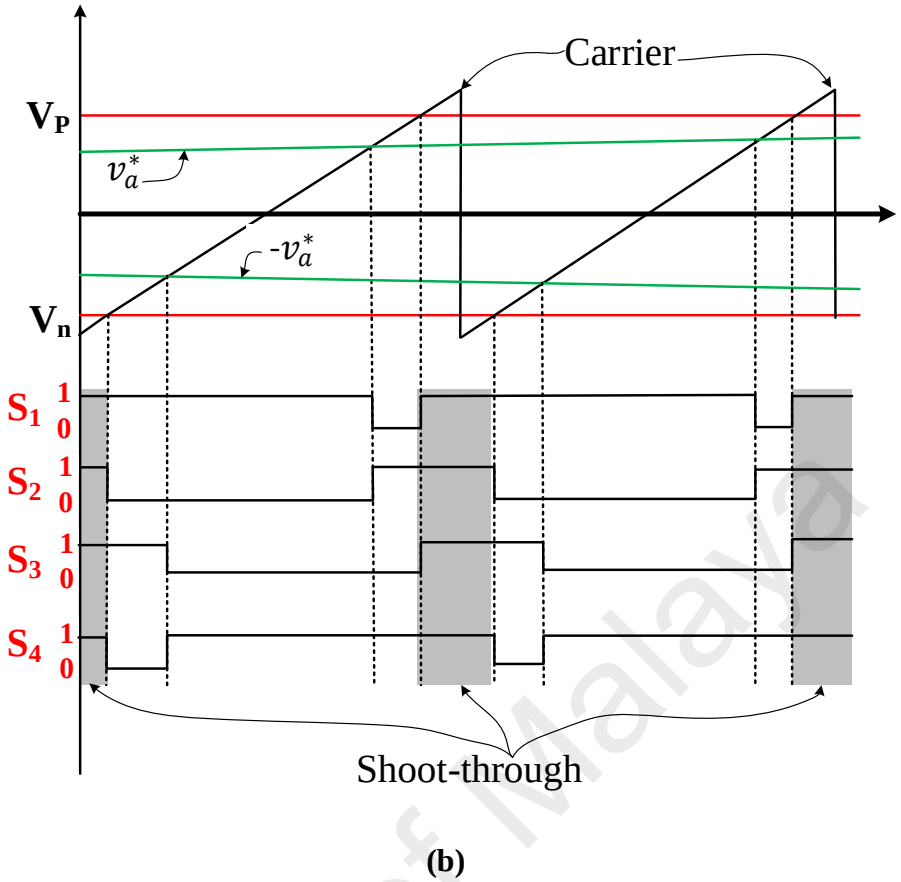


Figure 2.13: Modulation strategies for qZSI; **(a)** traditional method based on triangular carrier and **(b)** proposed method based on sawtooth carrier.

The conventional carrier-based PWM has been modified by (Poh Chiang et al., 2005) to be applicable to controlling a single-phase Z-source H-bridge topologies as Figure 2.14 shows. In this control scheme the ST interval is extracted from the null states (00 or 11) and evenly distributed within a fixed switching cycle without altering the normalized volt-sec average since both states similarly short-circuit the inverter three-phase output terminals, producing 0 V across the ac load. The same concept has been extended to modulate more complex three-phase-leg and four-phase-leg -source inverters.

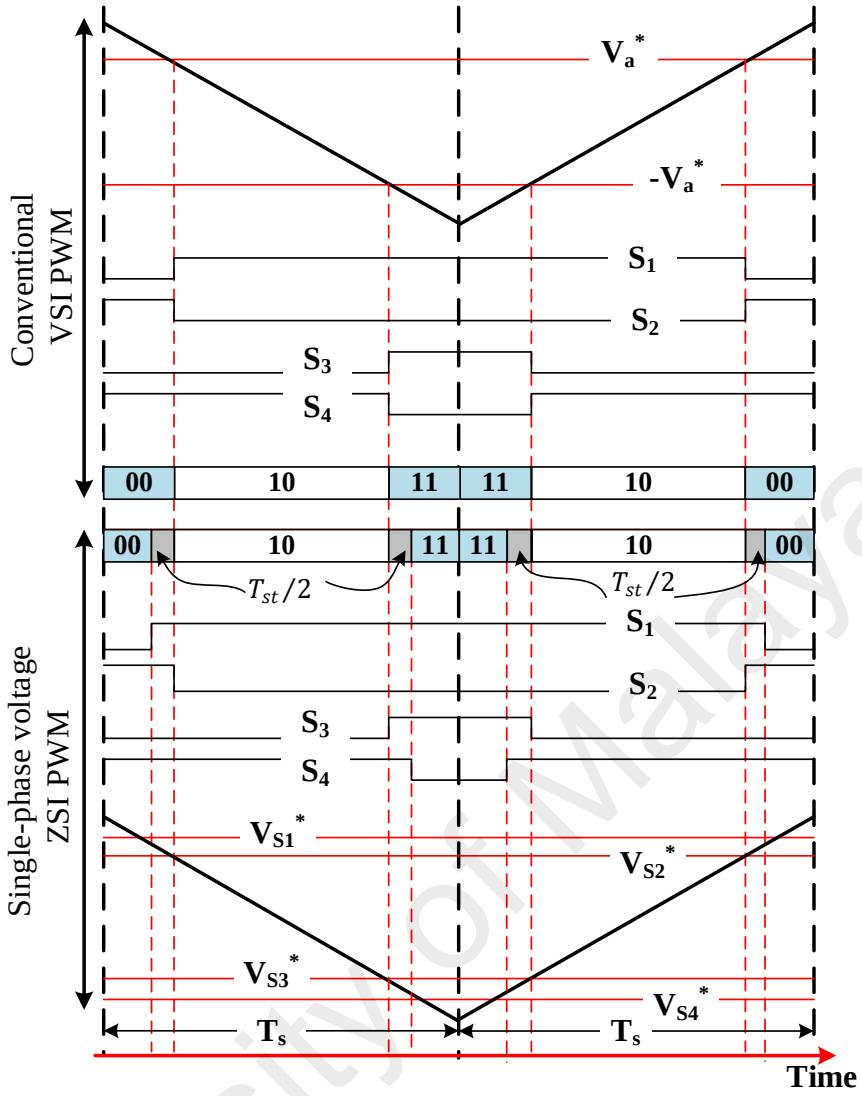


Figure 2.14: Modulation of single-phase Z-source inverter.

Besides to the above control techniques, an improved phase-shifted sinusoidal PWM is used in (Sun et al., 2014) to control the qZSI. The reference is compared with two opposite carriers to generate the desired pulses, and the shoot-through duty ratio is controlled by one straight line, thus the conduction angle of the switches is not equally dispersed for each Ts which leads to unbalanced power and thermal distributions. Furthermore, a Low-frequency Harmonics Elimination Pulse Width Modulation technique is presented in (Y. Yu, Zhang, Liang, & Cui, 2011), which could greatly reduce low-frequency capacitor voltage ripple in the impedance source network. Additionally, the authors in (Zare & Firouzjaee, 2007) have presented a unipolar hysteresis band current control method for a single-phase Z-source

inverter with symmetrical and asymmetrical Z-network configuration. This control technique with other well-known SPWM modulation techniques for single-phase Z-Source inverters are summarized in Table 2.2. Additionally, a hybrid pulse-width modulated single-phase quasi-Z-source grid-tie photovoltaic (PV) power system is proposed in (Y. Liu, Ge, Abu-Rub, & Sun, 2016). The hybrid pulse-width modulation (HPWM) combines the pulse-width modulation (PWM) and the pulse-amplitude modulation (PAM). The PWM works when the ac output voltage is lower than the dc source voltage; otherwise, the PAM operates the single-phase quasi-Z-source inverter (qZSI). The HPWM leads to the reduction of power loss, and the quasi-Z-source capacitance and inductance without any requirement to limit the dc-link 2ω ripple. For instance, in a 500 W power rating and 108 V peak output voltage single-phase qZSI system, the conventional PWM-based one requires the qZS inductance 1000 μH (or 500 μH coupled inductor) and qZS capacitance 4400 μF to buffer the 2ω dc-link voltage ripple within 5%, and inductor current ripple within 20%. Whereas, at the same power and voltage ratings, the hybrid modulation reduces the qZS inductance to 500 μH (or 250 μH coupled inductor) and qZS capacitance to 10 μF, owing to no longer restraining the dc-link 2ω ripple while maintaining ac output quality. It also benefits the efficiency improvement. Shortcomings are that a large capacitance is demanded at the PV panel terminal to prevent the 2ω ripple from propagating to the PV panel, and the high 2ω ripple on the qZS capacitance will degrade the performance of the energy storage battery when a battery is paralleled for power balance.(Yushan Liu, Abu-Rub, Ge, & Ellabban, 2016) The working principal of HPWM is plotted in Figure 2.15.

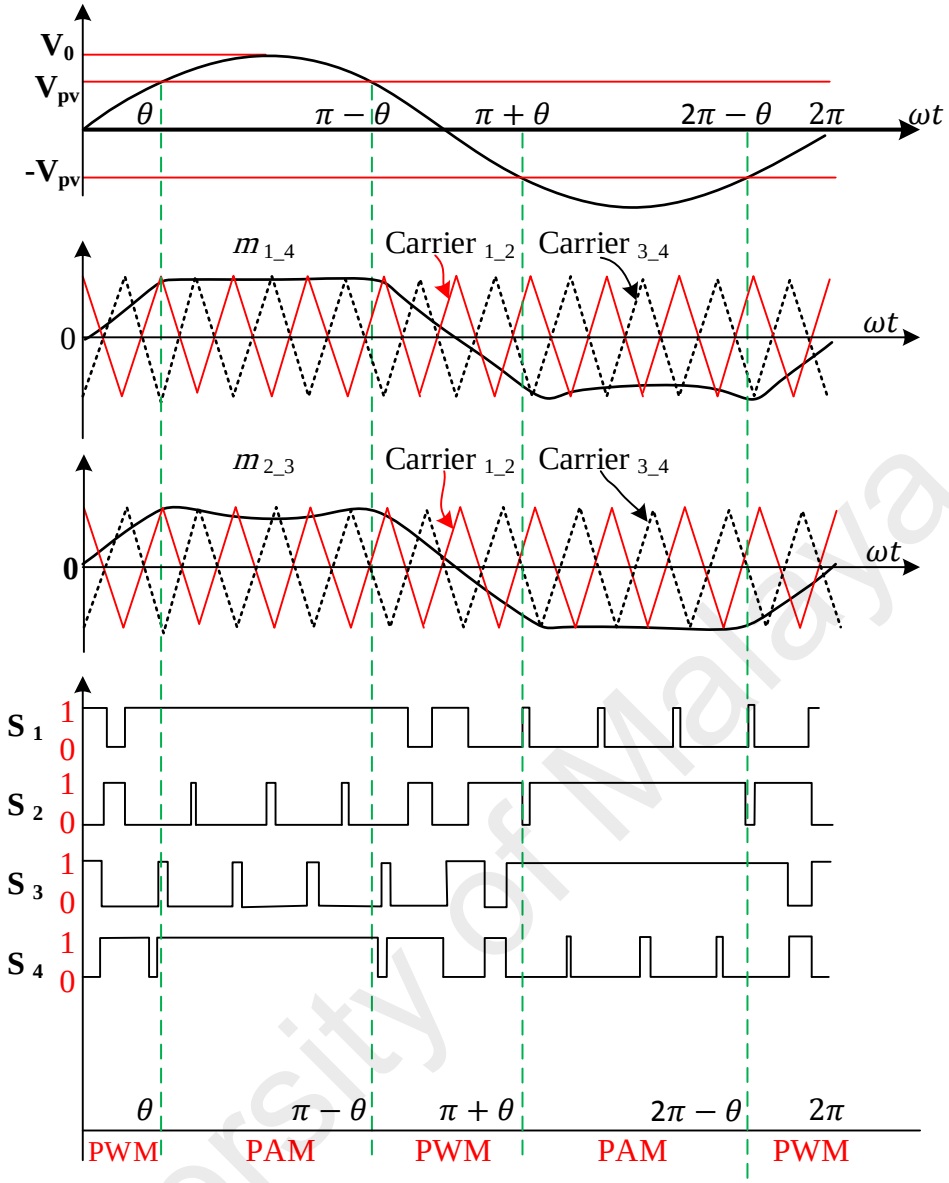


Figure 2.15: Proposed HPWM for single-phase qZSI.

Table 2.2: Comparison of the different SPWM control techniques for single-phase impedance network topologies.

Modulation Control strategy	Topology/ Number of switches (N)	Peak stress on switches	Modulating Signal	M and D range	Features
Carrier-based PWM (Poh Chiang et al., 2005)	Two-leg H-bridge N= 4	$\hat{V}_{sw} = BV_{dc}$ $\hat{I}_{sw} = Bi_o$ $B = \frac{1}{1-2D_{st}}$	Two opposite sinusoidal signals V_a and V_b V_b=-V_a $v_a^* = M \sin \omega t$	$0 \le M \le 1$ $0 \le D \le 0.5$ both are limited by M +D < 1	• The ST period is divided into two-equal interval period per control cycle. • One-leg shoot-through
One-cycle control (Tang et al., 2011b)	Single-phase Z-Source N= 2	$\hat{V}_{sw} = 3V_{dc}$ $\hat{I}_{sw} = 3I_{dc}$	One sinusoidal signal $(V_{in} - v_{ref})$ Where $v_{ref} = V_m \, sin \, \omega t$	$^1/_3 \le D \le 1$	• High-efficiency constant-frequency control • Insensitive to the system model • limited to 2-switch IMN topologies • High stress on the switching devices
Nonlinear (SPWM) (Cao et al., 2011a)	Semi-Z-source N= 2	$\hat{V}_{sw} = 3V_{dc}$ $\hat{I}_{sw} = 3I_{dc}$	$v^* = \frac{1}{2 - M \sin \omega t}$	$0 \le M \le 1$ $0 \le D \le 1$	• Low cost compared to H-bridge • High device stress • Limited to 2- switch IMN topologies • Reduces the leakage current
Unipolar hysteresis band current control (Zare & Firouzjaee, 2007)	Two-leg H-bridge N= 4	$\hat{V}_{sw} = BV_{dc}$ $\hat{I}_{sw} = Bi_o$ $B = \frac{1}{1-2D_{st}}$	A band of sinusoidal signals $v_{ref} = V_m \, sin \, \omega t$	$0 \le D \le 0.5$	• Suitable for symmetric or asymmetric IMN topologies • Robust and unaffected by load parameter changes • Higher device stress due to non-uniform switching. • High-quality output current • Switching frequency is not regular.
Modified carrier PWM (L. Liu et al., 2013)	Quasi-Z-Source inverter N= 4	$\hat{V}_{sw} = BV_{dc}$ $\hat{I}_{sw} = Bi_o$ $B = \frac{1}{1-2D_{st}}$	Two opposite sinusoidal signals V_a and V_b are compared to a sawtooth carrier V_b=-V_a $v_a^* = M \sin \omega t$	$0 \le M \le 1$ $0 \le D \le 0.5$ both are limited by M +D < 1	• One ST period per control cycle • Lower switching loss and improved system efficiency during boost operation • Two-leg shoot-through • Suitable for high frequency applications.
Hybrid pulse-width modulation (HPWM) (Y. Liu, B. Ge, H. Abu-Rub, & H. Sun, 2016)	Quasi-Z-Source inverter N= 4	Depend on the operating mode PWM or PAM	A comparison of the modulation waves (m_{1_4} and m_{2_3}) and the carriers ($Carrier_{1\_2}$ and $Carrier_{3\_4}$ are in 180◦ phase difference).	There is no limitation of M +D < 1, but they are dependent in each other.	• Has the ability to suppress low-order harmonics. • The switching events are significantly reduced, because there is no shoot-through action in the PWM and no active switching in the PAM. • Shoot-through states are apart from traditional zero states to avoid the competition of both duty cycles.

2.3.2 Modulation Techniques for Three-Phase Two-Level Inverters

The traditional modulation schemes for conventional VSI has been modified to be suitable for controlling ZSI. Many control techniques such as carrier-based PWM (CB-PWM) and modified space vector PWM (MSVPWM) have been reported in the literature to control the shoot-through in three-phase H-bridge topologies (2-level). CB-PWM schemes include Simple Boost Control (SBC), Maximum Boost Control (MBC) and Maximum Constant Boost Control (MCBC). Which will be discussed in the next sub-sections.

2.3.2.1 Simple Boost Control

The simple boost control (Miaosen, 2006), uses two straight lines equal to or greater than the peak value of the three phase references to control the shoot-through duty ratio in a traditional sinusoidal PWM, as shown in Figure 2.16. When the triangular waveform is greater than the upper line, V_p, or lower than the bottom line, V_n, the circuit turns into shoot-through state. Otherwise it operates just as traditional carrier-based PWM. In this control method, the boost factor ***B*** factor is constant because the shoot-through time interval is divided into two identical parts in one control cycle. Therefore, there is no inductor current and capacitor voltage ripples associated with the output frequency. Additionally, the increase of the modulation index ***M*** leads to the decrease of the obtainable shoot-through duty ratio, thus $\boldsymbol{D_{max}}$ is limited to (1-*M*). Moreover, when the modulation index ***M*** reaches one, $\boldsymbol{D_{max}}$ will be zero; at this point, the inverter is operating same as the traditional VSI.

This method is very straightforward; however, the resulting voltage stress across the switches is relatively high because some traditional zero states are not utilized, which will restrict the obtainable voltage gain because of the limitation of device voltage rating.

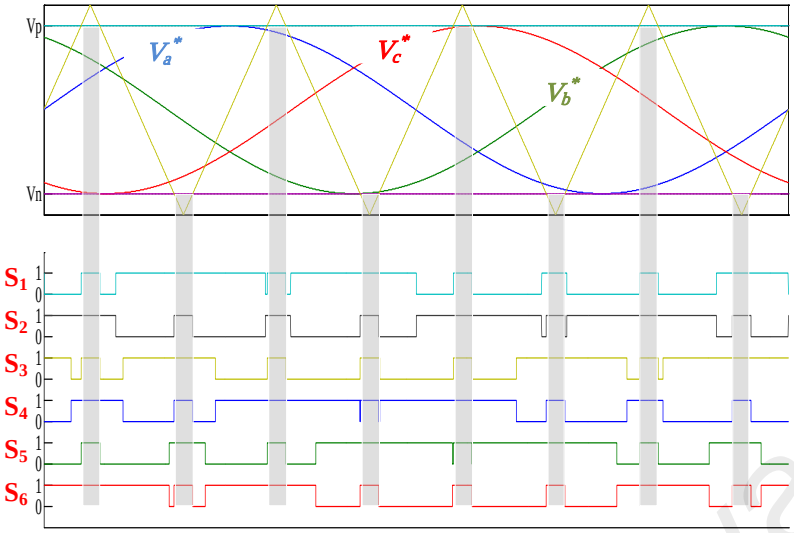


Figure 2.16: Simple Boost Control Waveforms.

2.3.2.2 Maximum Boost Control

The maximum boost control is proposed to reduce the voltage stress under a desired voltage gain. The method maximizes the shoot through period without effecting the active states by turning all zero states into the shoot through zero state as shown in Figure 2.17. The shoot-through states are inserted when the triangular carrier wave is either greater than the maximum curve of the references or smaller than the minimum of the references. The relationships of voltage gain versus modulation index, and voltage stress versus voltage gain are analyzed in detail in (Fang Zheng Peng et al., 2005). Indeed, turning all zero states into shoot through states can minimize the voltage stress across the switching devices and extend the ST duty ratio D up to $1 - \frac{3\sqrt{3}}{2\pi}M$ per control cycle. However, this method introduces a low frequency current ripple that is associated with the output frequency in the inductor current and the capacitor voltage. This will cause a higher requirement of the passive components when the output frequency becomes very low (Ellabban, Van Mier, & Lataire, 2011). Therefore, the maximum boost control is suitable for applications that have a fixed or relatively high output frequency. Third harmonic injection can also be used to extend the modulation index range from 1 to $2/\sqrt{3}$.

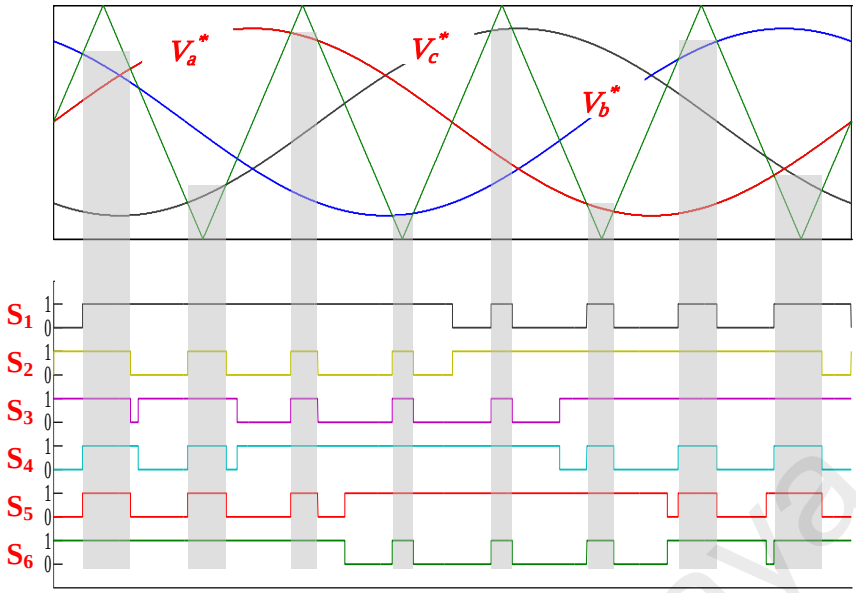


Figure 2.17: Maximum Boost Control Waveforms.

2.3.2.3 Maximum Constant Boost Control

The implementation of MCBC proposed in (Shen et al., 2006) is shown in Figure 2.18. By slightly modifying the shoot-through references of the MBC, the MCBC can keep the shoot-through duty ratio constant per switching cycle. The range of the modulation index is extended from 1 to $2/\sqrt{3}$. by injecting a third-harmonic component with 1/6 of the fundamental component magnitude to the three phase-voltage references, the inverter turns to a shoot-through state when the carrier triangle wave is greater than the upper shoot-through strait line (V_P) or smaller than the lower shoot-through line (V_N) (Siwakoti, Fang Zheng, Blaabjerg, Poh Chiang, Town, et al., 2015). Compared to MBC, the voltage stress across the switching devices is slightly higher, and the voltage gain is slightly less. However, MCBC keeps the shoot-through duty ratio always constant which eliminates the low-frequency ripple associated with the output frequency. Therefore, the inductor and capacitor requirements of the Z-network are greatly reduced (Yushan Liu et al., 2016). On the other hand, compared to SBC, this method has much lower voltage stress across the switching devices, and much higher boosting ability, i.e. $B = \frac{1}{\sqrt{3}M-1}$ (Diab et al., 2016).

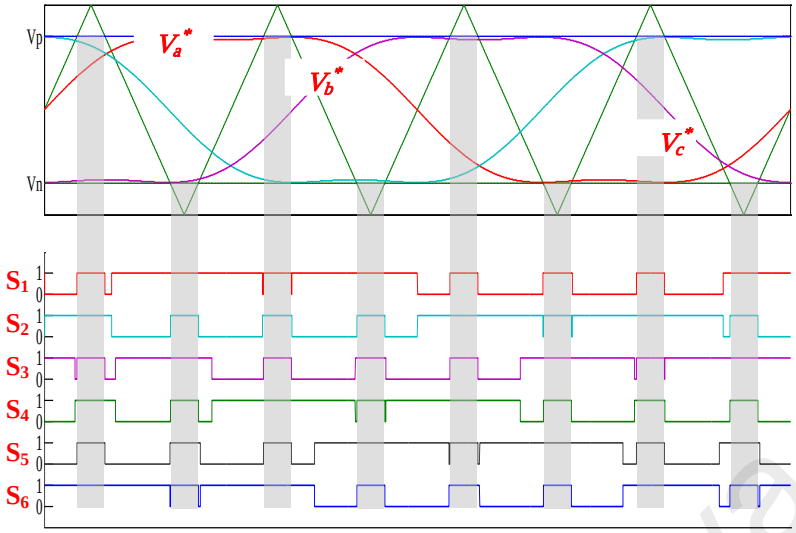


Figure 2.18: Maximum constant shoot-through boost control waveforms.

2.3.2.4 Other Modified carrier-based PWM

In (Poh Chiang et al., 2005), the well-known PWM control strategies for the conventional VSI have been modified for controlling Z-Source inverters either continuously or discontinuously. The normalized volt-sec average is kept unchanged , as well as all the unique harmonic performance features of these conventional modulation strategies due to a proper placement of the shoot-through period within the zero states without affecting the active states (Siwakoti, Fang Zheng, Blaabjerg, Poh Chiang, Town, et al., 2015). The same concept in Figure 2.14 has been extended to control more complex three-phase-leg and four-phase-leg Z-source topologies. The desired total shoot through time interval is located only on one phase-leg and divided into three realizable parts per control cycle which reduce the inductor current ripple compared to SBC, MBC and MCBC but the switches conduction losses are increased. On the other hand, in this control strategy the three phase legs bear the equal shoot-through time interval (Y. Tang, S. Xie, & J. Ding, 2014). In this manner, the allotment and arrangement of the shoot-through state is easy to realize, but the inductor current ripple is not optimized. This causes to use relatively large inductors. Therefore, to optimize the inductor current ripple, the authors in (Y. Tang et al., 2014) proposed a

modified PWM strategy where the shoot-through time intervals of three phase legs are calculated and rearranged according to the active state and zero state time intervals to achieve the minimum current ripple across the Z-source inductor, while maintaining the same total shoot-through time interval.

In addition to the aforementioned SPWM control techniques, A new modulation technique for three-phase ZSIs is proposed in (Diab et al., 2016). This modulation technique decouples the interdependence between the ST duty ratio and the modulation index inherited in all the existing PWM techniques by proposing a new parameter '***K***' by which the ST duty ratio and the boosting factor are determined, while keeping the modulation index constant at its maximum possible value. The switching waveforms of this control scheme is shown in Figure 2.19. With this technique, a reliable operation of the ZSI at high-voltage gains is ensured without significant ripples on both the capacitor voltage and the inductor current due to its advantage to reject any disturbance in the ST control parameter. Moreover, the voltage stress on the capacitors and the switching devices is lower than that of both the simple boost method and the Modified space vector PWM (MSVPWM) at the higher voltage gains, and is higher than that of both MBC and MCBC (Diab et al., 2016). This modulation technique is very suitable for PV and fuel cells applications, which necessitates high-voltage boost.

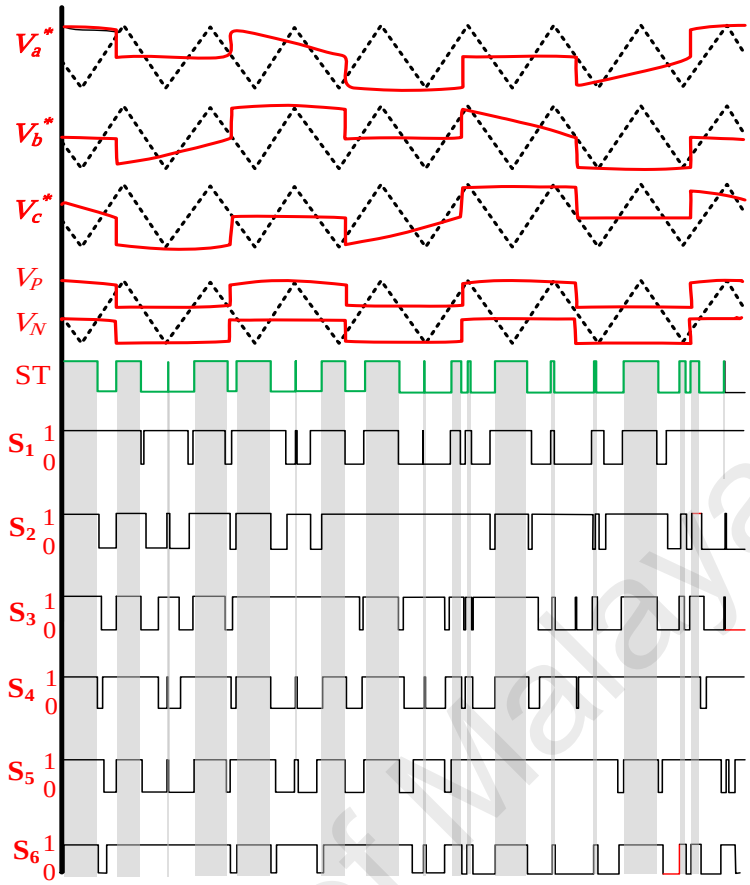


Figure 2.19: Modified PWM shoot-through boost control waveforms M = $\mathbf{1}/\sqrt{\mathbf{3}}$ and K = 0.2).

The comparison the important relations for the different SPWM modulation techniques and the proposed one in (Diab et al., 2016) is shown in Table 2.3, where the modulation index is kept constant ($M = {}^{1}/_{\sqrt{3}}$), while '***K***' is used to control the shoot-through duty ratio.

The different SPWM control techniques for three-phase two-level impedance source inverters in Table 2.3, provide different maximum *D* periods such as: $T_{sh\_max} = T_o$ for MBC; whereas for the other methods the zero states intervals are partially turned into ST states. Moreover, the voltage stress (V_S) across the switching devices incurred by SBC and Carrier-based PWM (Poh Chiang et al., 2005) is the highest, and the resulted V_S using the Modified Carrier-based PWM (Diab et al., 2016) is constant regardless the voltage gain.

Therefore, the modulation technique presented by (Diab et al., 2016) is suitable for application requiring very high-voltage boost.

Table 2.3: Comparison of the different SPWM control techniques for three-phase two-level impedance source inverters.

Parameters	Simple Boost (Miaosen, 2006)	Maximum Boost (Fang Zheng Peng et al., 2005)	Maximum Constant Boost/ With 3rd harmonic Injection (Shen et al., 2006)	Modified Carrier-based PWM (Diab et al., 2016)	Carrier-based PWM (Poh Chiang et al., 2005)
D	$1-M$	$1-\frac{3\sqrt{3}}{2\pi}M$	$1-\frac{\sqrt{3}}{2}M$	$\frac{\pi(2-K)-3}{2\pi}$	M +D < 1
Boost factor B	$\frac{1}{2M-1}$	$\frac{\pi}{3\sqrt{3}M-\pi}$	$\frac{1}{\sqrt{3}M-1}$	$\frac{\pi}{3-\pi(1-K)}$	$\frac{1}{2M-1}$
Voltage gain G	$\frac{M}{2M-1}$	$\frac{\pi M}{3\sqrt{3}M-\pi}$	$\frac{M}{\sqrt{3}M-1}$	$\frac{\pi\sqrt{3}}{3-\pi(1-K)}$	$\frac{M}{2M-1}$
Voltage stress of the switch Vs	$(2G-1)V_{dc}$	$\frac{3\sqrt{3}G-\pi}{\pi}V_{dc}$	$(\sqrt{3}G-1)V_{dc}$	$\sqrt{3}GV_{dc}$	$(2G-1)V_{dc}$
	highest	lowest	Medium	Highest at low voltage gain and low at high voltage gain	Highest
Maximum M	*1*	*M=1 and can be extended to* $\frac{2}{\sqrt{3}}$ *with 3rd harmonic Injection*	$\frac{2}{\sqrt{3}}$	$\frac{1}{\sqrt{3}}$	1
No. of Switches involved in Shoot-through state	*6*	*6*	*6*	*6*	*2*
No. of shoot-through per switching cycle	*2*	*2*	*2*	*2*	*3*

2.3.2.5 Modified Space Vector PWM (MSVPWM) Control Schemes.

The traditional SVM technique for three-phase VSI generates eight voltage space vectors, and there are six sectors, I to VI as shown in Figure 2.20 (a). The well-known algorithm can be defined as (Holmes & Lipo, 2003)

$$T_1 = T_s M sin\left[\frac{\pi}{3} - \theta + \frac{\pi}{3}(i-1)\right] \quad (2.1)$$

$$T_2 = T_s M sin\left[\theta - \frac{\pi}{3}(i-1)\right] \quad (2.2)$$

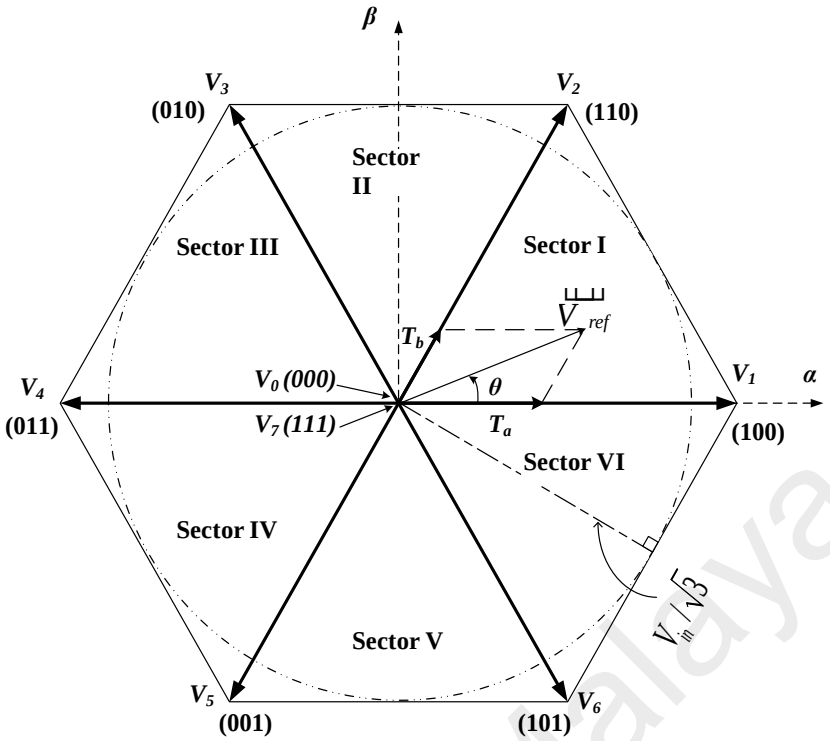
$$T_0 = T_s - T_1 - T_2 \quad (2.3)$$

$$V_{ref} = V_1 \frac{T_1}{T_s} + V_2 \frac{T_2}{T_s} \quad (2.4)$$

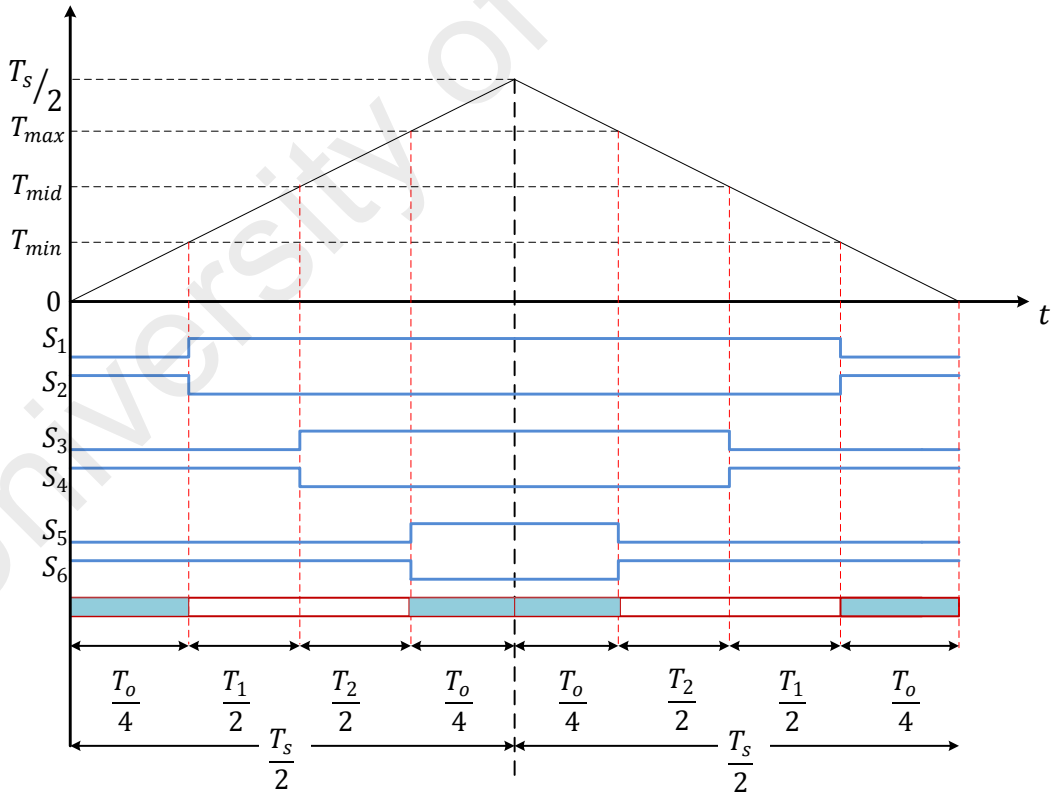
where $i \in (1, 2, \ldots, 6)$ denotes the ith sector; T_0 is the time interval of the traditional zero vector V_0; T_1 and T_2 are the time intervals of active vectors V_1 and V_2, respectively; and θ is the inclined angle of voltage reference vector V_{ref} and V_1. The modulation index M is defined as $M = \sqrt{3}V_{ref}/V_{in}$, and V_{in} is the dc-link voltage.

Figure 2.20 (b) shows the three-phase VSI switching time sequence in sector I, where T_{max}, T_{mid}, T_{min} are the maximum, middle, and minimum switching times for the three bridge legs, $T_{min} = {T_0}/{4}$, T_{mid}, $= {T_0}/{4} + {T_1}/{2}$, and $T_{max} = {T_s}/{2} - {T_0}/{4}$. Additionally, the zero state repeats periodically every $\pi/3$, so the average zero state duty ratio over one control cycle is

$$\frac{\overline{T_o}}{T_s} = \frac{1}{\pi/3}\int_0^{\pi/3}\left[1 - \frac{\sqrt{3}}{2}Msin\left(\theta + \frac{\pi}{3}\right)\right]d\theta = 1 - \frac{3\sqrt{3}M}{2\pi} \quad (2.5)$$



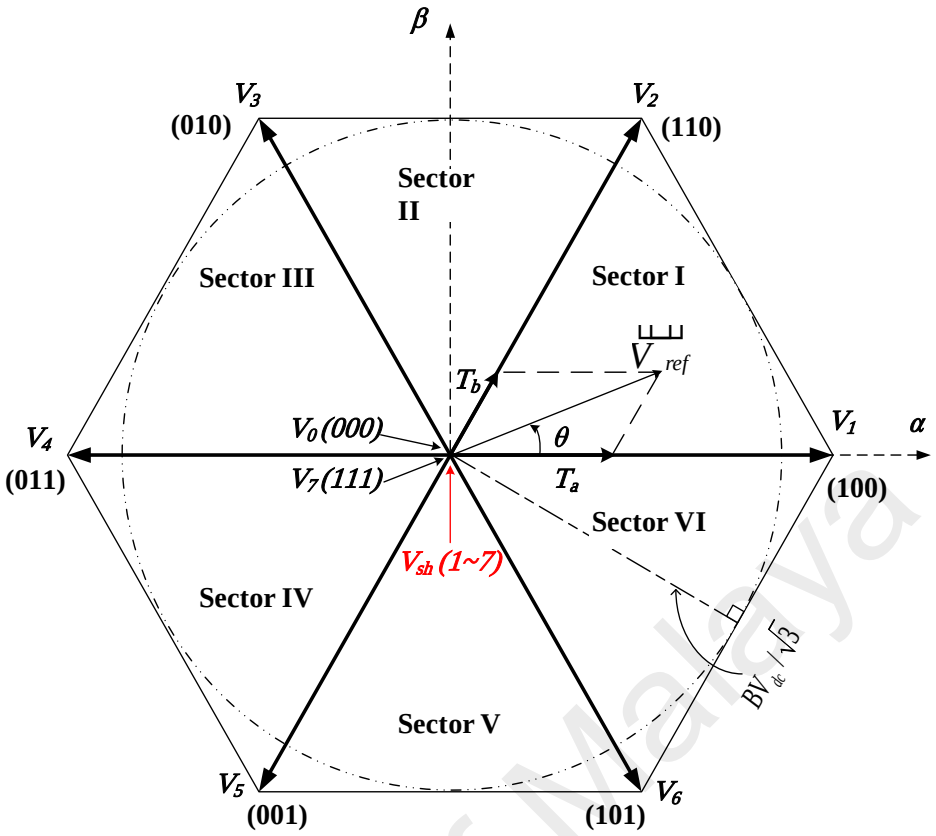
(a)



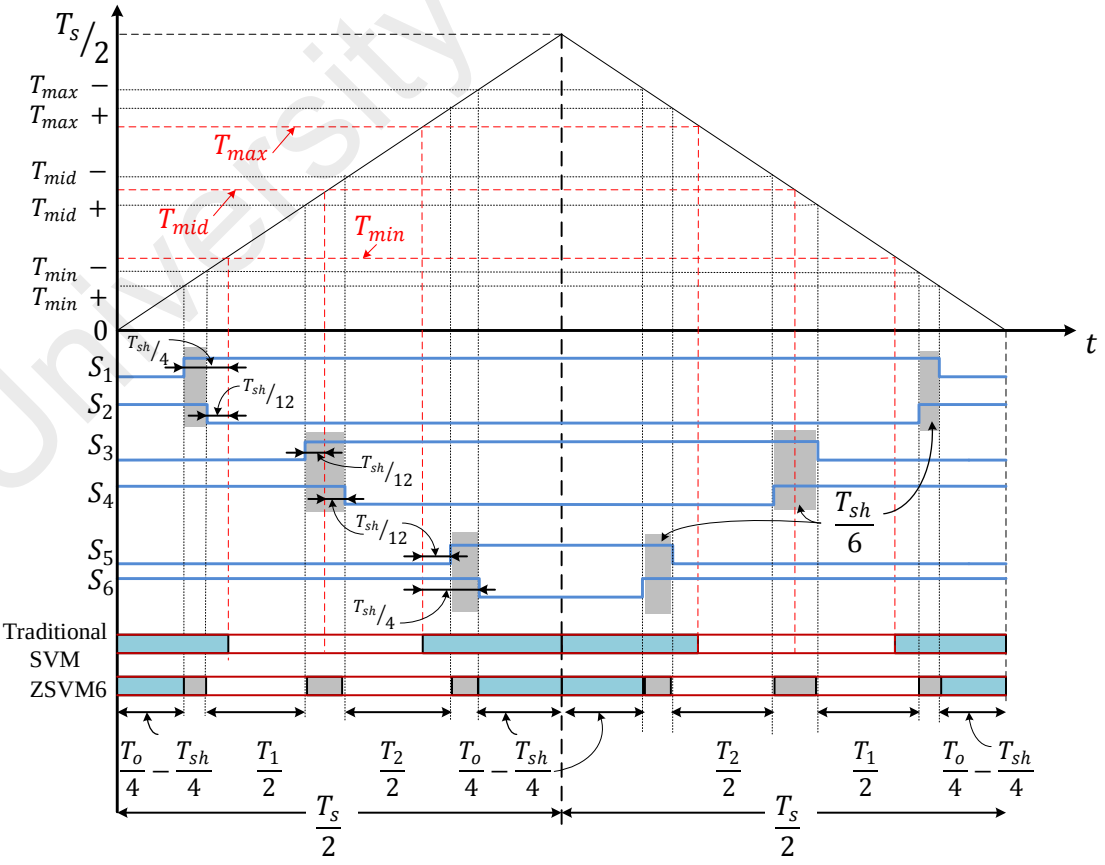
(b)

Figure 2.20: SVM for a traditional voltage source inverter; **(a)** basic voltage space vectors and **(b)** switching time sequence.

The traditional SVPWM has been modified by (U. S. Ali & Kamaraj; U Shajith Ali & Kamaraj, 2011; Jung & Keyhani, 2007; Yushan Liu, Ge, Ferreira, De Almeida, & Abu-Rub, 2011; Xu & Chen, 2017) to be applicable to ZSI due to its high voltage utilization, reduced commutation time of the switches, low current harmonics, wide linear modulation, easy digital implementation and improved output quality (K. Zhou & Wang, 2002). Figure 2.21 (a) shows the corresponding voltage space vectors of the ZSI. The shoot-through state is produced during the time intervals of the traditional zero vectors, hence the two switches' control signals of the same bridge leg are no longer complementary, even though the traditional SVM does. To avoid an additional switching actions and losses, the shoot-through states are inserted at the beginning or the end of active vector's switching moment. There are three different existing ways to distribute the shoot-through states: **1)** the total shoot-through time interval is divided into six parts evenly distributed into six switching times (Yushan Liu et al., 2011). The six switching times are modified, so called as ZSVM6. **2)** the divided six-part shoot-through time intervals are also fulfilled in each control cycle, but the four switching times are only modified in (Jung & Keyhani, 2007), so called as ZSVM4. **3)** The desired total shoot through time interval is divided into four realizable parts, but two switching times are modified in (U Shajith Ali & Kamaraj, 2011) , so called as ZSVM2. Figure 2.21 reveals their switching patterns in one switching cycle.



(a)



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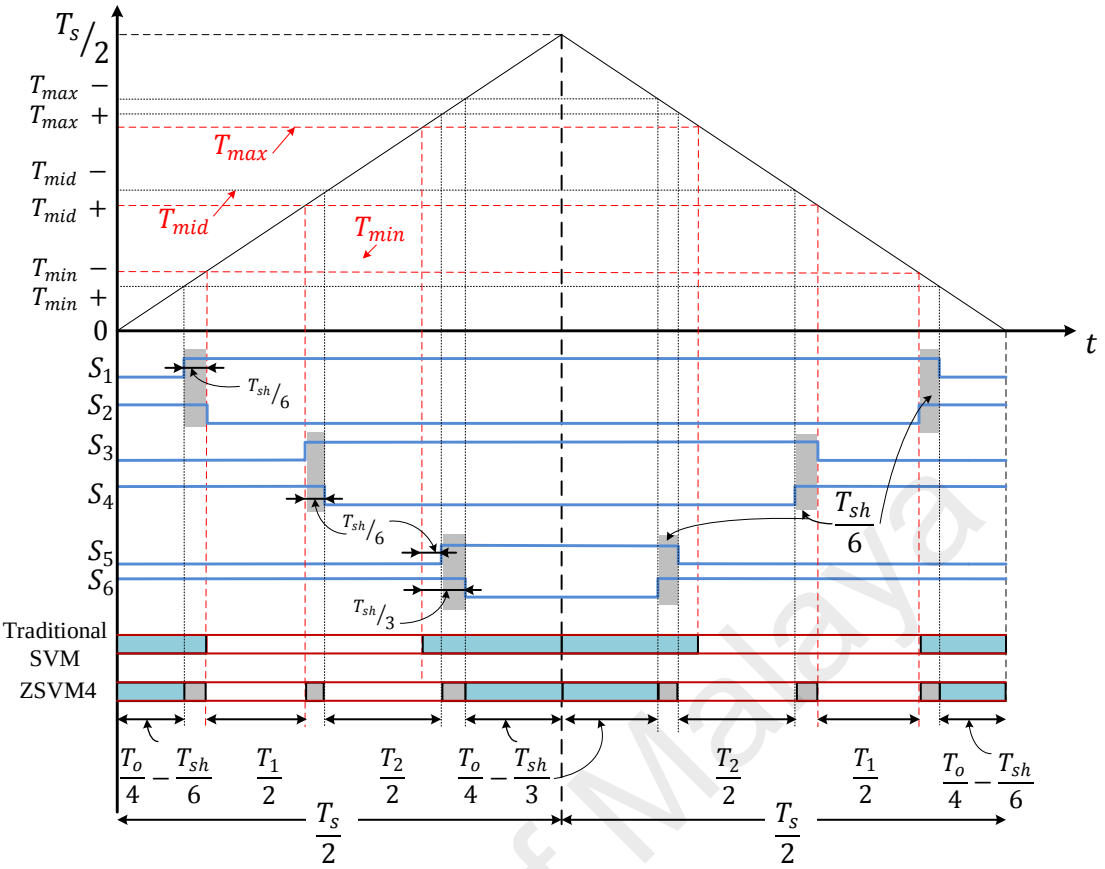

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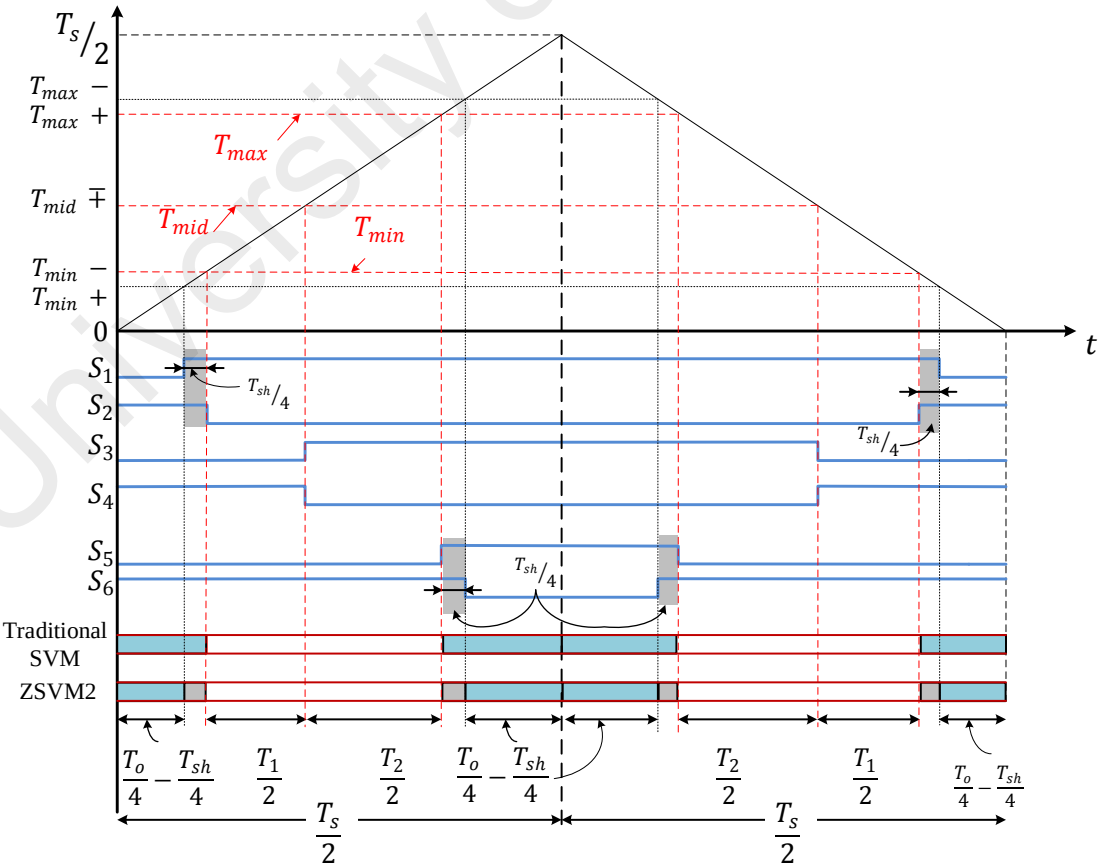
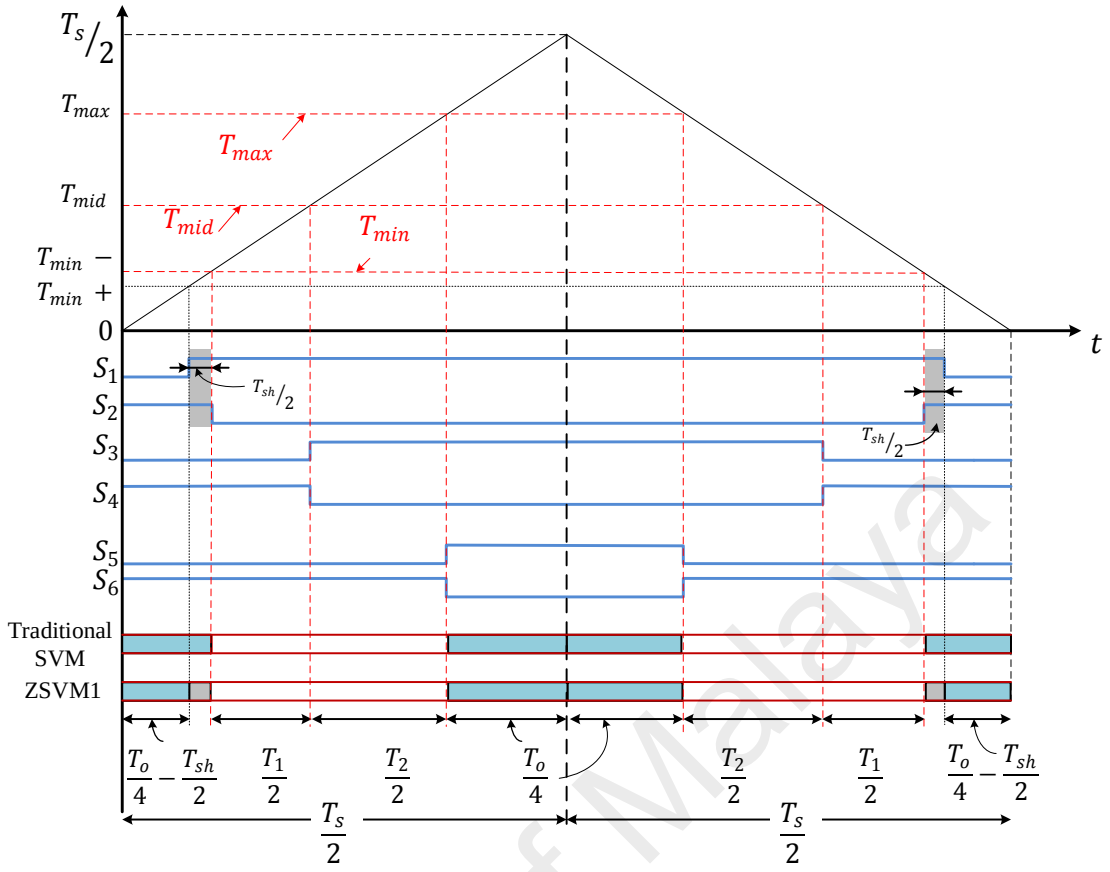


(d)



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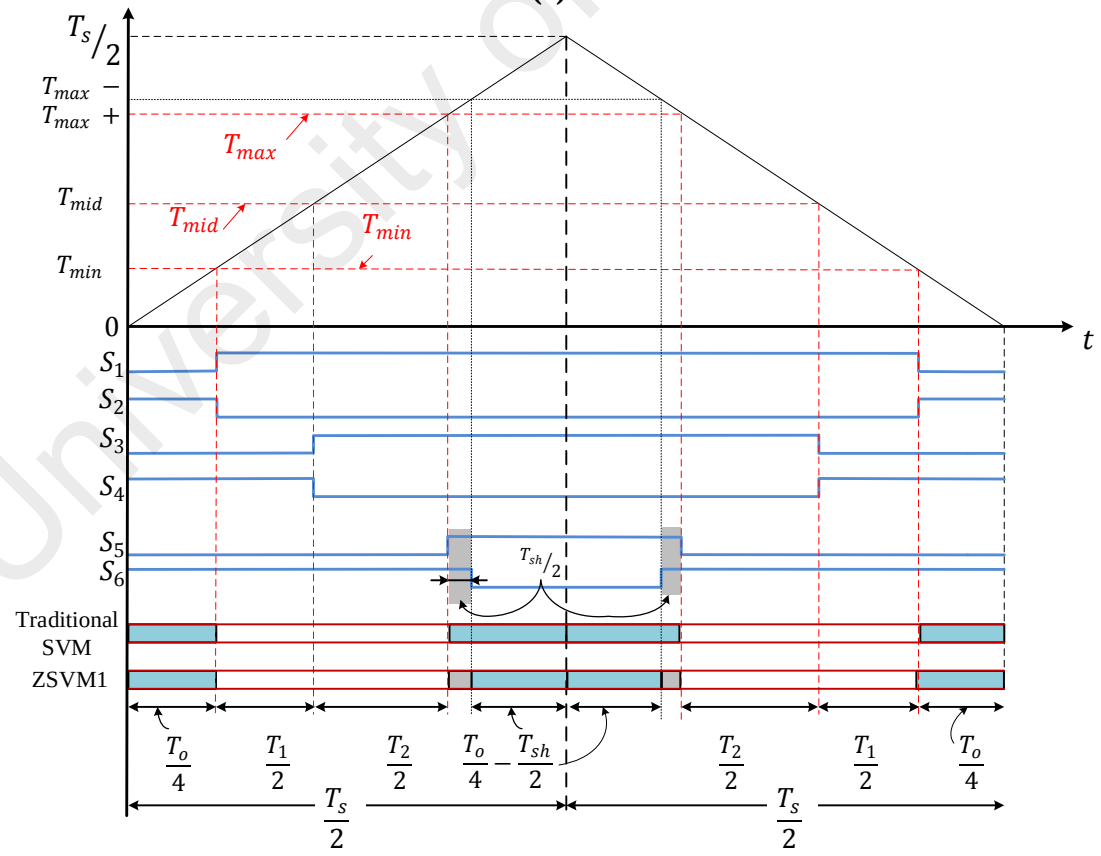


(f)

Figure 2.21: SVMs for the qZSI: **(a)** voltage space vectors; switching time sequences of **(b)** ZSVM6, **(c)** ZSVM4, **(d)** ZSVM2, **(e)** ZSVM1-I, and **(f)** ZSVM1-II

The voltage gain, voltage stress across the switch, and ac harmonic content of the three aforementioned SPWMs and the ZSVM4 are compared in (Ellabban et al., 2011) where the simulation and the experimental comparison results show that the constant maximum ST boost control method seems to be the most suitable method for the ZSI. Also, the ZSI efficiency improves by increasing the dc input voltage of and it worsens by increasing the ST duty ratio. In (Yushan Liu, Ge, Abu-Rub, & Peng, 2014), the authors present a detailed comparison of simple boost control (SBC) and four space vector modulation schemes for the three-phase Z-source/quasi-Z-source inverter (ZSVMs). The results of which show that (ZSVMs) achieve a higher dc-link voltage utilization compared to SBC and the ZSVM4 resulted in the lower current ripples when compared to ZSVM2. However a different study has been presented in (Dong, Zhang, & Cheng, 2016) showing that the maximum current ripple of ZSVM2 is lower than that of ZSVM4.

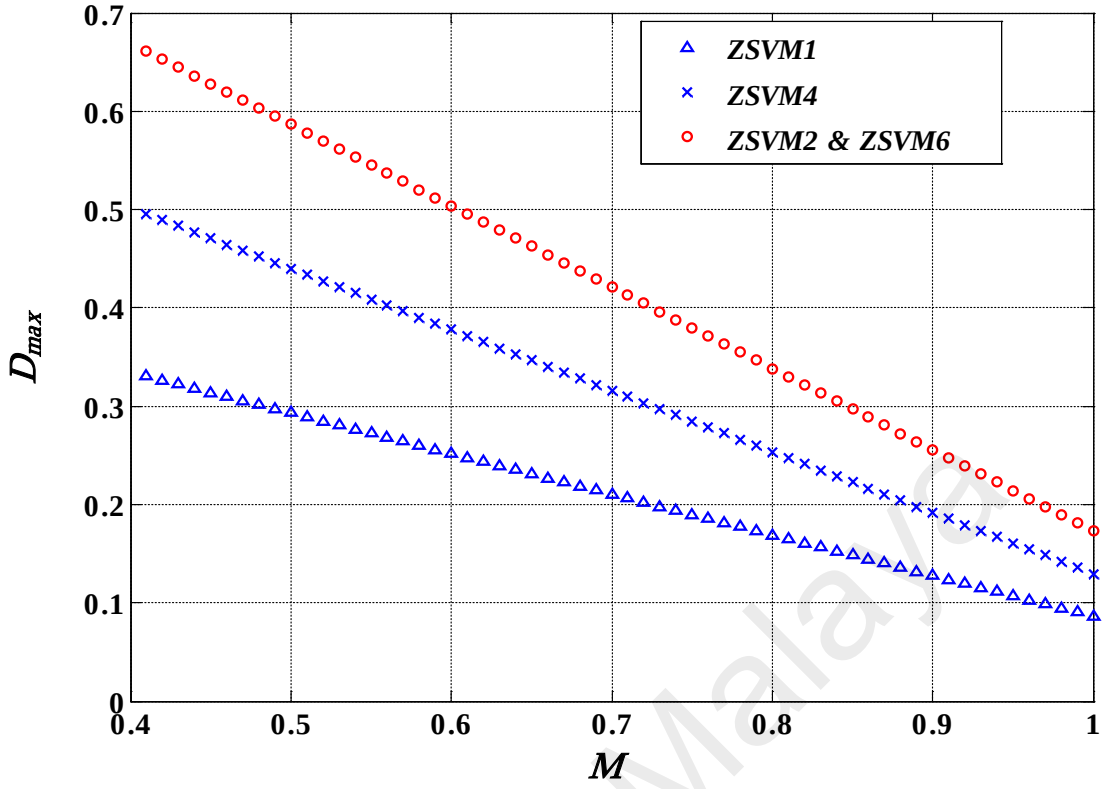
A comparison of various ZSVM techniques is shown in Table 2.4 and presented in (Yushan Liu, Ge, & Abu-Rub, 2013; Yushan Liu et al., 2014) experimentally based on various performance .

From Table 2.4, the different ZSVM techniques provide different maximum shoot-through time intervals and they can be summarized as: (1) $T_{sh,max} = T_0$ for the ZSVM6 and ZSVM2, (2) $T_{sh,max} = {3T_0}/{4}$ for the ZSVM4, (3) $T_{sh,max} = {T_0}/{2}$ for the ZSVM1. Moreover, for clear comparison of four ZSVMs, the curves of maximum shoot-through duty ratio D_{max} versus the modulation index M, and the maximum voltage stress ratio (V_s/V_{in})versus the voltage gain G are plotted in Figure 2.22 (a) and Figure 2.22 (b) respectively. It should be noted that the maximum voltage gain of ZSVM1 is not changed even if the modulation index changes, i.e. $G_{ZSVM1\,max} = MB = {2\pi}/{3\sqrt{3}} \approx 1.21$. As result, the maximum voltage stress ratio of ZSVM1 is inversely proportional to the modulation index M. In conclusion, the ZSVMs achieve the same voltage gains in a wider range of the

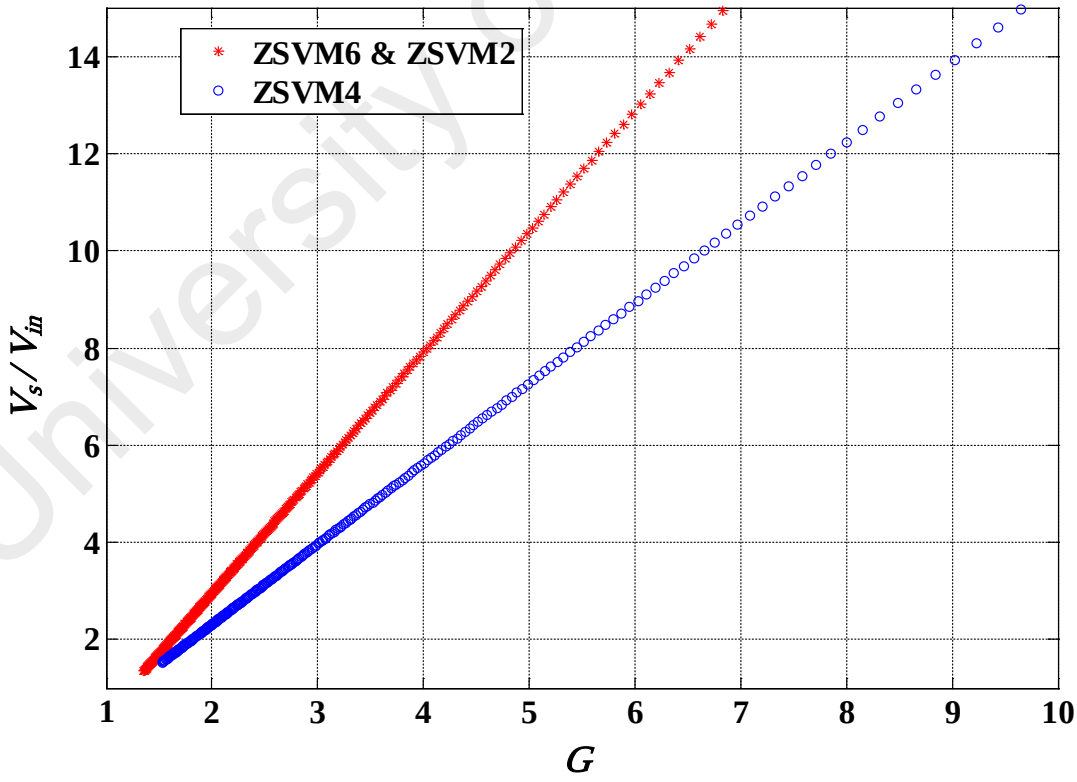
modulation index; however, the voltage stress across the switches is significantly higher than that of the simple boost control method (Yushan Liu et al., 2014).

Table 2.4: Comparisons of various SVM techniques in three-phase ZSIs

Parameters	ZSVM1	ZSVM2	ZSVM4	ZSVM6
D_{max}	$\frac{1}{2} - \frac{3\sqrt{3}M}{4\pi}$	$\frac{2\pi - 3\sqrt{3}M}{2\pi}$	$\frac{3}{4}\frac{2\pi - 3\sqrt{3}M}{2\pi}$	$\frac{2\pi - 3\sqrt{3}M}{2\pi}$
B_{max}	$\frac{2\pi}{3\sqrt{3}M}$	$\frac{\pi}{3\sqrt{3}M - \pi}$	$\frac{4\pi}{9\sqrt{3}M - 2\pi}$	$\frac{\pi}{3\sqrt{3}M - \pi}$
G_{max}	$\frac{2\pi}{3\sqrt{3}}$	$\frac{M\pi}{3\sqrt{3}M - \pi}$	$\frac{4\pi M}{9\sqrt{3}M - 2\pi}$	$\frac{M\pi}{3\sqrt{3}M - \pi}$
Voltage stress of the switch (V_s)	$\frac{2\pi}{3\sqrt{3}M}V_{dc}$	$\frac{3\sqrt{3}G - \pi}{\pi}V_{dc}$	$\frac{9\sqrt{3}G - 4\pi}{2\pi}V_{dc}$	$\frac{3\sqrt{3}G - \pi}{\pi}V_{dc}$
No. of shoot-through per switching cycle	2	4	6	6
Switches involved in Shoot-through state	2	2	2	2
Switch Device Power (SDP)	Highest	Medium	Smallest	Smallest
Current ripple in the inductor(ΔI_L)	Highest	Medium	Low	Low



(a)



(b)

Figure 2.22: (a) maximum shoot-through duty ratio versus the modulation index **(b)** switch's maximum voltage stress ratio versus the voltage gain

The flow diagram for implementing the SVPWM Based Maximum Boost Control strategy (SV-MBC) presented by (K. Yu, Luo, & Zhu, 2012b) is shown in Figure 2.23.

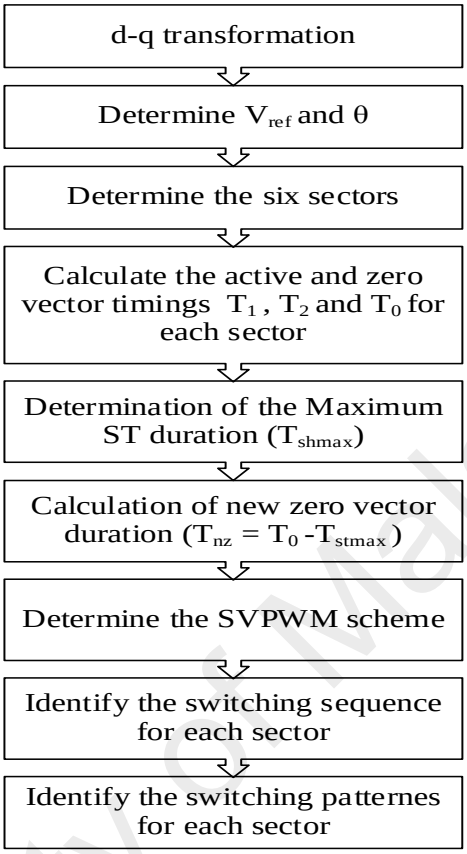


Figure 2.23: Flow diagram for SV-MBC strategy.

In addition to the aforementioned control techniques for three-phase impedance-network inverters, a hybrid pulse width modulation for Z-source converter is presented in (Santos, Filho, Oliveira, & Silva, 2010). The technique combines the theory of space-vector PWM with the ease of implementation of a triangular-comparison PWM which reduces the effort of algorithm calculation. The introduction of the distribution ratio in this technique, allows the development of a systematic approach for implementation of either conventional or any modified vector strategies.

2.4 Summary

In this chapter, an intensive overview of various voltage Z-source inverter topologies have been presented. Even though numerous configurations presented in this chapter, several more can be found in the literature. In addition, the comparison of various impedance- source networks is provided to identify the pros and cons of the predominate topologies in the literature. In the next chapter, the widely used topologies, i.e. quasi/Z-source inverter is used to be modulated by the proposed control techniques.

In the second part, many modulation schemes for single-phase impedance-source inverters such as: the one-cycle control strategy, the modified reference PWM, and others have been presented and compared. Then, the detailed modulation methods applicable for the three-phase two-level ZSI/qZSI, which are also applicable to most of the three-phase two-level impedance-source inverters are presented, compared and classified into several categories. It has been found that a gap exists in the literature where no studies have investigated the improvement of the total execution time of the modulation techniques for impedance source inverters. Based on previous literature, a new control schemes for impedance-source inverters based on space vector principles will be discussed in the next chapters

CHAPTER 3: THE PROPOSED ALGORITHMS

3.1 Introduction

In this chapter a unified control schemes for single and three-phase quasi-Z-source/ Z-source inverters are presented, also call the one dimension for Z-source inverters (ODZSI), the fundamental and operation principles of the proposed control techniques, the mathematical details regarding the development of these strategies are provided.

3.2 Modulation of single-phase H-bridge qZSI

3.2.1 Quasi ZSI

The topology of the single-phase H-bridge qZSI presented in (Anderson & Peng, 2008) is depicted in Figure 3.1, it has an additional ST state to boost the dc-link voltage besides the conventional states as compared to the traditional H-bridge inverter, i.e., traditional zero states (00) and (11), active states (10) and (01) and shoot-through states (ST 1) and (ST 2).

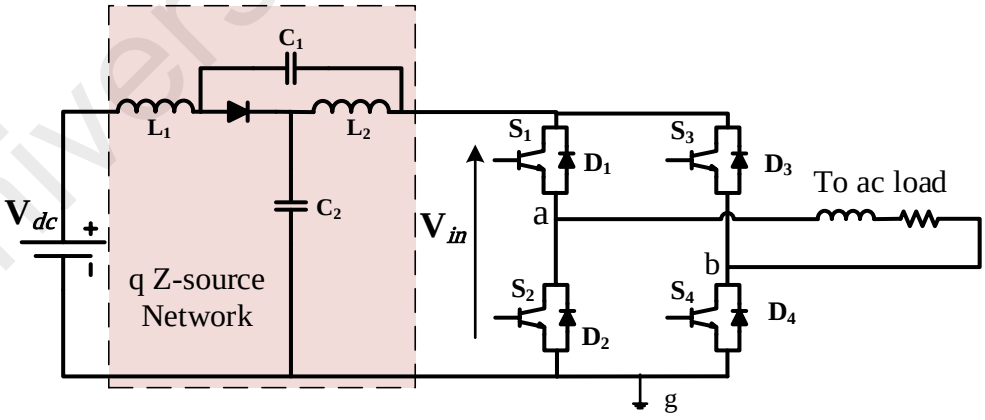


Figure 3.1: Single-phase H-bridge qZSI topology.

3.2.2 Circuit Analysis

Assuming the T_{nsh} is the non shoot-through time interval and T_{sh} is the interval of ST state during one control cycle T_s, the shoot-through duty ratio $D = \frac{T_{sh}}{T_s}$ and $T_{st} = T_S - T_{nsh}$.

At steady state, the average voltage across the capacitors C_1 and C_2 is given by the equation (3.1) and (3.2) respectively:

$$V_{c1} = \frac{T_{nsh}}{T_{nsh}-T_{sh}} V_{dc} = \frac{1-D}{1-2D} V_{dc} \tag{3.1}$$

$$V_{c2} = \frac{T_{sh}}{T_{nsh}-T_{sh}} V_{dc} = \frac{D}{1-2D} V_{dc} \tag{3.2}$$

the pick dc-link voltage across the inverter bridge is

$$\hat{V}_{in} = V_{c1} + V_{c2} = \frac{1}{1-2D} V_{dc} = B.V_{dc} \tag{3.3}$$

and the output peak phase voltage from the inverter can be expressed as

$$\hat{V}_{ph} = \frac{1}{2} M.\hat{V}_{in} \tag{3.4}$$

Using the equation (3.3), the equation (3.4) can be rewritten as

$$\hat{V}_{ph} = \frac{1}{2} M.B.V_{dc} = \frac{1}{2} G.V_{dc} \tag{3.5}$$

where M is the modulation index, G is the voltage gain and B is the boost factor.

The structure of the equivalent circuits during the shoot-through and non ST modes are depicted in Figure 3.2 and Figure 3.3 respectively.

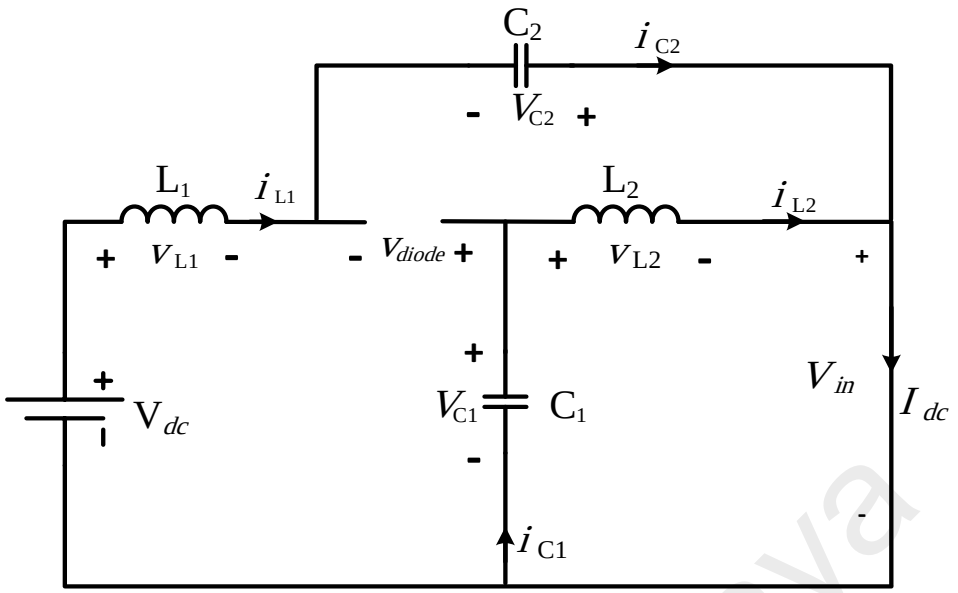


Figure 3.2: Equivalent circuit during the ST State.

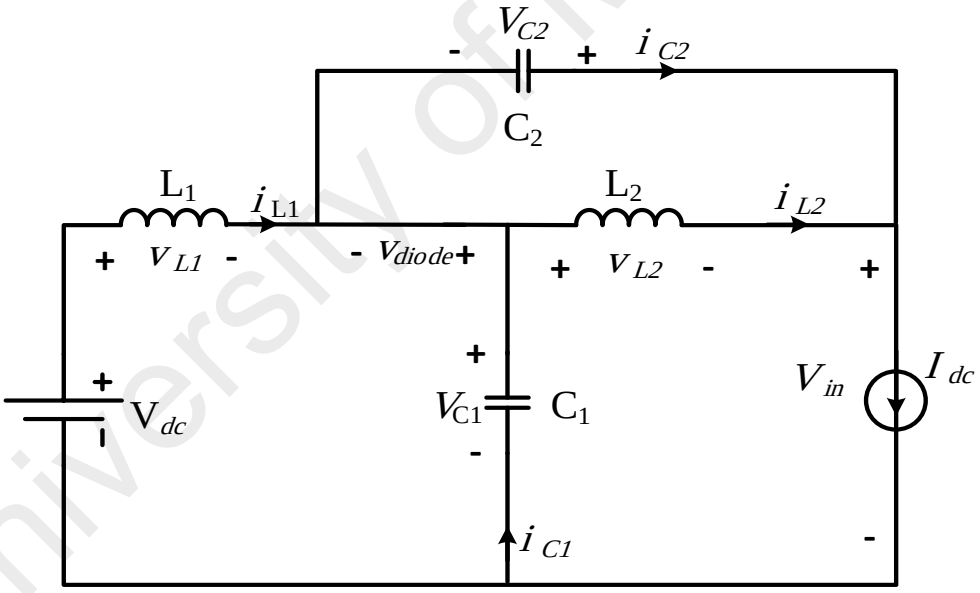


Figure 3.3: Equivalent circuit during non ST state.

3.2.3 Proposed ODZSI

The one dimension modulation technique is based on the generation of the reference line-to-ground voltage as an average of the nearest voltage levels (K. Corzine, 2003; Leon et al., 2008; Leon et al., 2010).

The voltage of the output points '*a*' or '*b*' in Figure 3.1 with respect to the ground denoted by (g) is given by:

$$V_{xg} = S_x \cdot V_{dc} \tag{3.6}$$

Where S_x represents the switching state of the phase x (x denotes phase *a* or *b*). During a sampling period, the inverter operates to produce these vectors in duty ratio proportional to each vector component.

The main task of the ODZSI is to determine the switching states and their corresponding duty cycles. As indicated in Table 3.1, The zero and active switching states can be represented by zero and active stationary vectors $\overrightarrow{V_1}$ and $\overrightarrow{V_2}$, respectively. The switching state '1' denotes that the upper switch in an inverter leg (S_1 or S_3) is ON and the inverter terminal voltage (V_{xg}) is positive ($+V_{in}$) while the switching state '0' indicates that the inverter terminal voltage is zero due to the conduction of the lower switch (S_2 or S_4).

Table 3.1: The stationary vectors, Switching states, and On-state switches.

Vector	Switching state	Switch state	V_{xg}
Zero stationary $\overrightarrow{V_1}$	0	Upper switch is OFF Lower switch is ON	0
Active stationary $\overrightarrow{V_2}$	1	Upper switch is ON Lower switch is OFF	V_{in}

In order to generate the reference voltage with a minimum distortion, the duty-cycle computation between the two nearest voltage levels of the inverter needs to be calculated accurately. Based on volt-second balancing principle and geometric expressions as shown in Figure 3.4, the dwell times for the stationary vectors can be derived as follows:

$$V_{xg\_ref}.T_s = V_1.T_1 + V_2.T_2 \tag{3.7}$$

substitution of the equation (3.6) in (3.7) yields:

$$V_{xg\_ref}.T_s = S_x.V_{dc}.T_1 + (S_x + 1).V_{dc}.T_2 \tag{3.8}$$

$$T_s = T_1 + T_2 \tag{3.9}$$

T_s is the sampling period of the modulation scheme. T_1 and T_2 are the dwell times for the stationary vectors $\overrightarrow{V_1}$ and $\overrightarrow{V_2}$ respectively.

The switching state (S_x) is determined using the integer function INT that returns the nearest integer less than or equal to its argument.

$$S_x = INT\left(\frac{V_{xg\_ref}}{V_{dc}}\right) \tag{3.10}$$

substitution of the equation (3.9) in (3.8) yields:

$$T_2 = T_s\left(\frac{V_{xg\_ref}}{V_{dc}} - S_x\right) \tag{3.11}$$

With the switching state of phase *x* ($S_{ph\text{-}x}$) and its dwell times T_1 and T_2 are calculated, the following step is to generate the qZSI switching pulses. The arrangement of the switching sequence should minimize the device switching frequency.

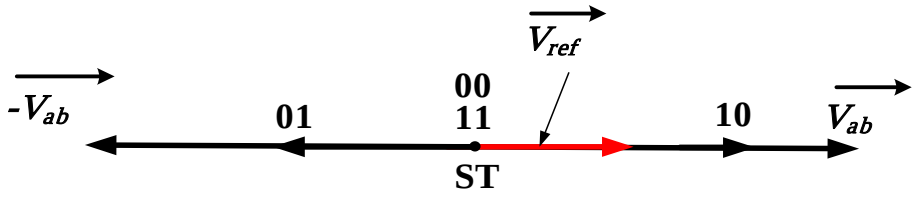
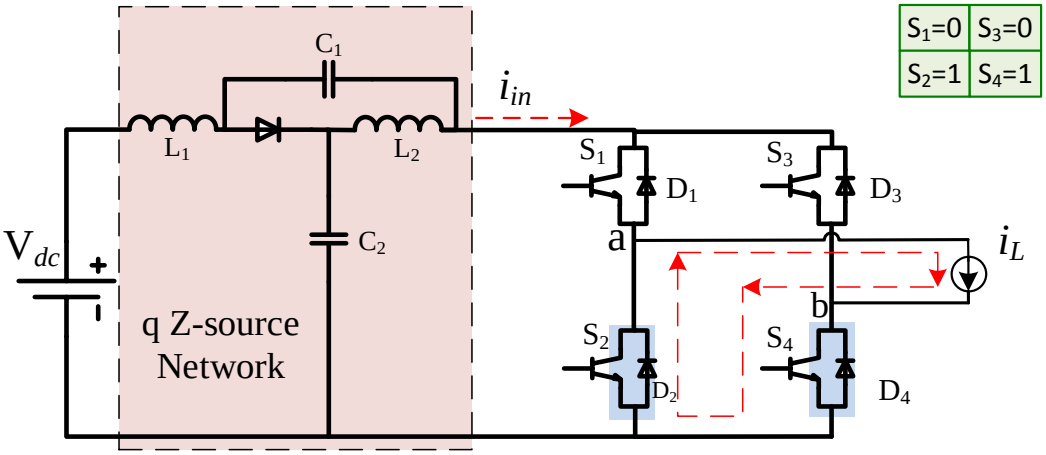


Figure 3.4: Generation of V_{ag_ref} and V_{bg_ref} .

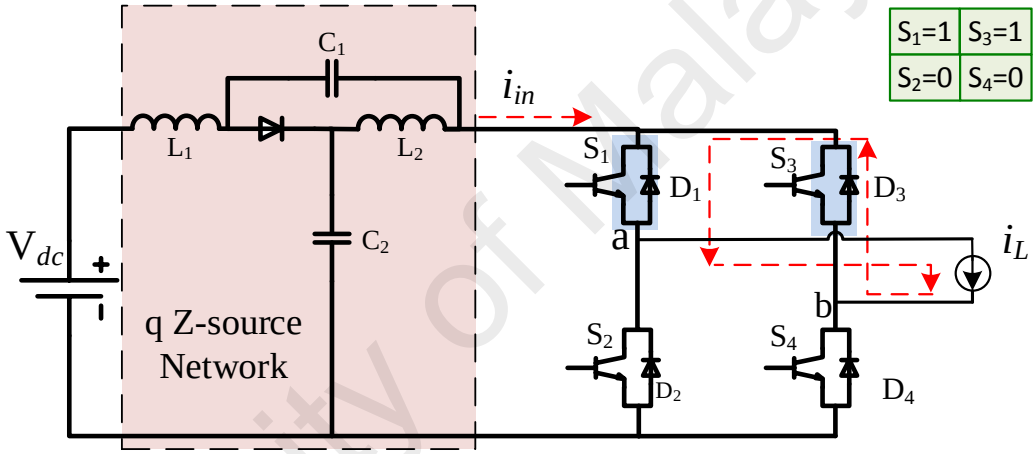
The switching states for a single-phase H- bridge qZSI controlled by ODZSI are listed in Table 3.2. The controller generates two different sequence modes within a cycle of the waveform output, the equivalent circuit of each operating state and the switching patterns are depicted in Figure 3.5 and Figure 3.6 respectively. The ST 3 will not be used since it cannot be achieved from any active or null states with only a single device switching.

Table 3.2: Switching States for a Single-phase H- bridge ZSI Controlled by ODZSI. ($\bar{S}$ is the complement of S)

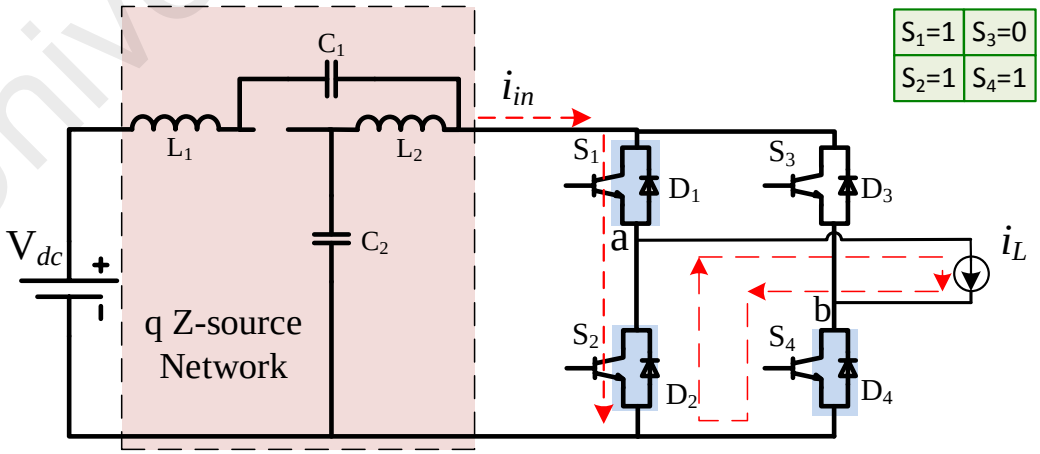
	S_1	S_2	S_3	S_4
Null (00)	0	1	0	1
Null (11)	1	0	1	0
Active (10)	1	0	0	1
Active (01)	0	1	1	0
ST 1	1	1	S_3	$\bar{S}_3$
ST 2	S_1	$\bar{S}_1$	1	1
ST 3	1	1	1	1



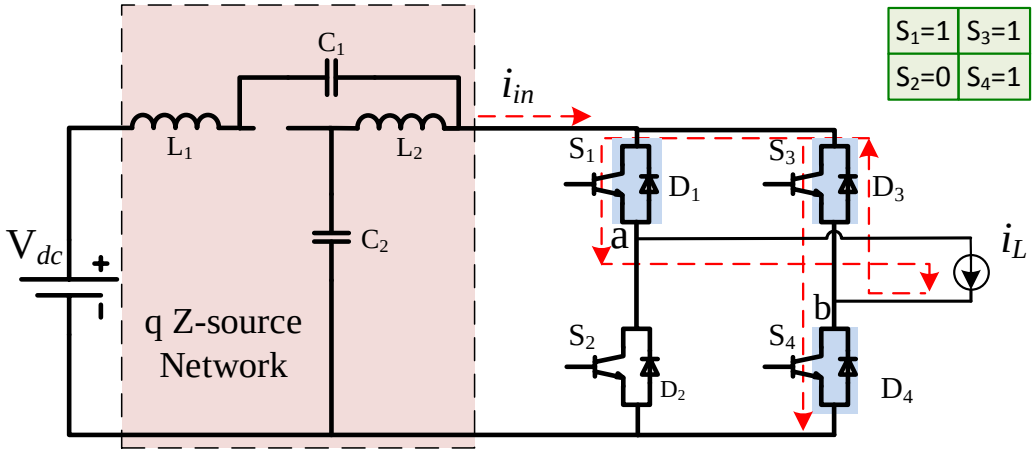
(a) Null state.



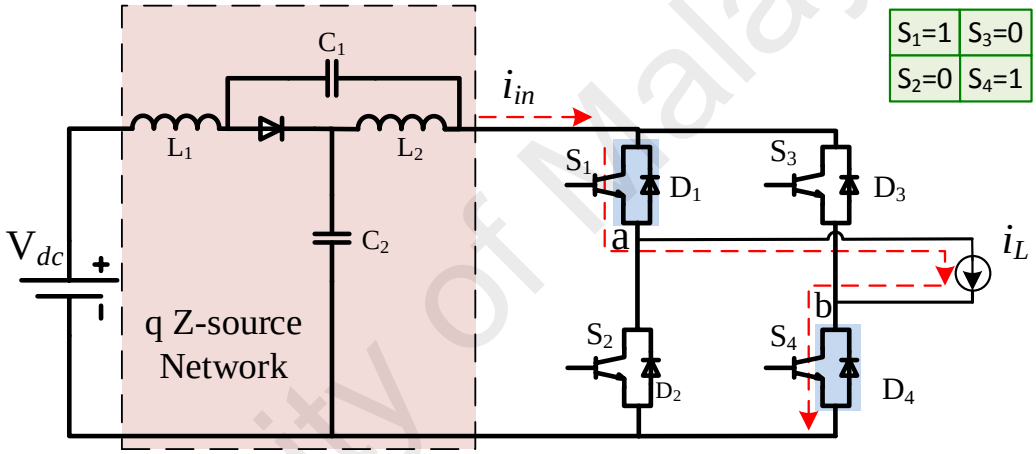
(b) Null state.



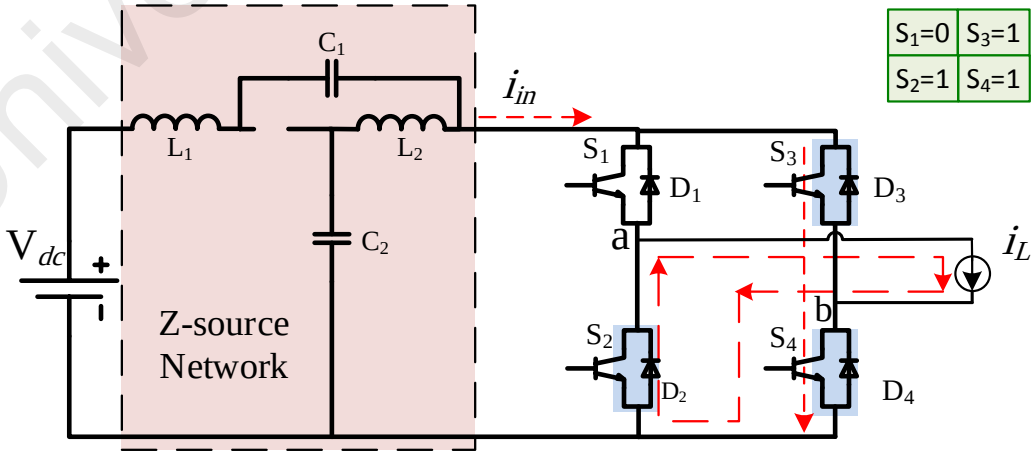
(c) Shoot-through state.



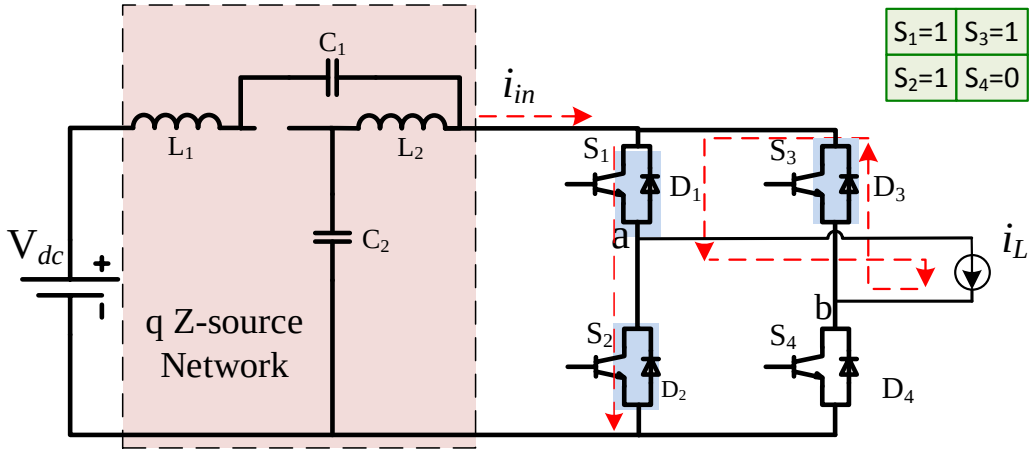
(d) Shoot-through state.



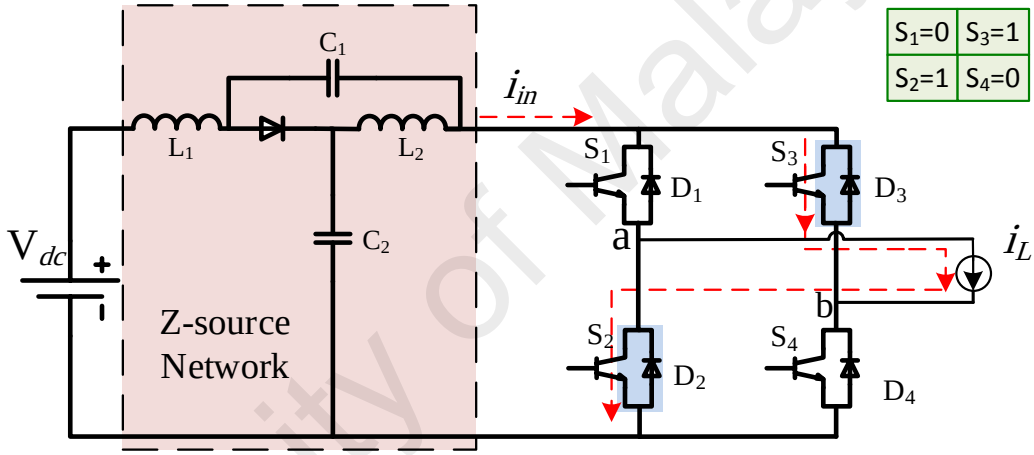
(e) Active state.



(f) Shoot-through state.



(g) Shoot-through state.



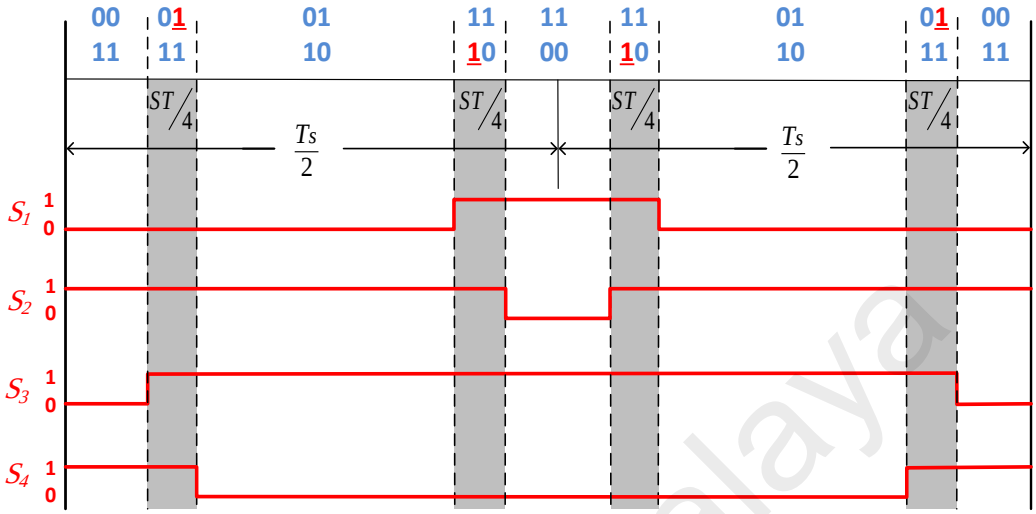
(h) Active state.

Figure 3.5: Equivalent circuits for different switching states.

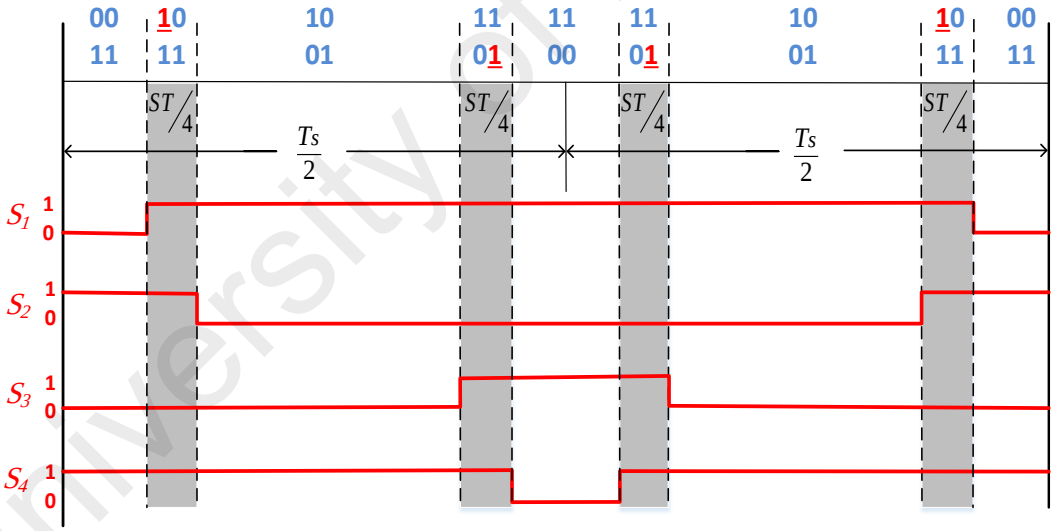
In general, the switching sequence design is not unique. The shoot-through states, however, are inserted in such way that the null intervals are maintained at the start and end of the switching cycle to achieve the optimal harmonic performance as shown in Figure 3.6.

The ST interval is extracted from the null states (00 or 11) and evenly distributed without altering the normalized volt-sec average to minimize the size of the inductors, they are inserted immediately adjacent to the active states in which the transition between the

switching states requires only one switch to change its state to ensure no additional switch commutations per control cycle are introduced.



(a) Mode I.



(b) Mode II.

Figure 3.6: The switching patterns generated by the proposed scheme.

The ST time is divided into four equal parts in every control cycle T_S which leads to reducing the inductor current ripple compared to (Poh Chiang et al., 2005), as a result the size of the inductor will be minimized significantly. Another advantage is that the inclusion of the shout-through and the transition from one mode to the next mode do not

require any additional device switching, as a result each switch (S_1~S_4) turns ON and OFF only once for every control cycle as shown in Figure 3.6.

The conduction time intervals for the four switches during one switching cycle are tabulated in Table 3.3.

Table 3.3: Conducting times for each switch during one control cycle per cycle of the fundamental frequency.

Mode	Phase A			Phase B		
	Switch	Conduction time	Switching events (ON/OFF)	Switch	Conduction time	Switching events (ON/OFF)
I	S_1	T_{2a}	2	S_3	$T_{2b}+ {}^1/_2\, T_{st}$	2
	S_2	$T_{1a}+ {}^1/_2\, T_{st}$	2	S_4	T_{1b}	2
II	S_1	$T_{2a}+ {}^1/_2 T_{st}$	2	S_3	T_{2b}	2
	S_2	T_{1a}	2	S_4	$T_{1b}+ {}^1/_2\, T_{st}$	2

3.3 Modulation of Three-phase legs.

3.3.1 Z-source inverter

The basic topology of Z-source inverter ZSI proposed by (Fang Zheng Peng, 2003) is shown in Figure 3.7.

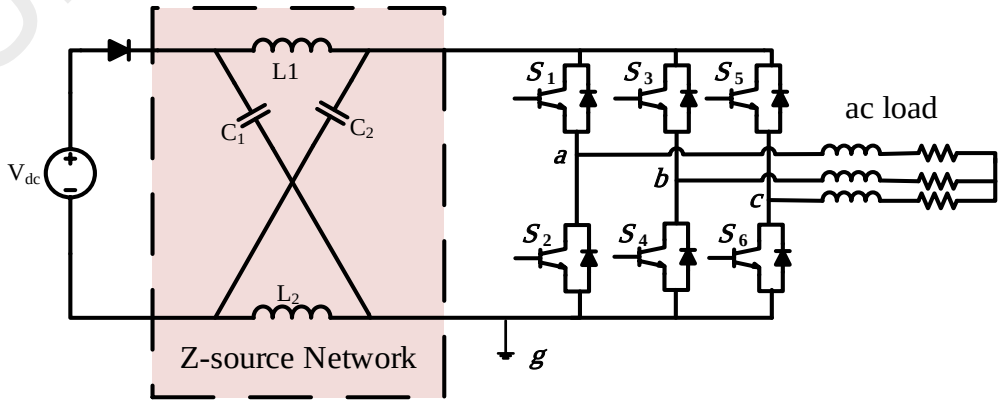


Figure 3.7: Basic topology of Z-source inverter.

3.3.2 Circuit Analysis

Assuming that the inductors L_1 and L_2 and capacitors C_1 and C_2 have the same inductance (L) and capacitance (C) respectively.

Assuming the T_{nsh} is the time interval of non ST state and T_{sh} is the interval of the ST state during one switching cycle T_s, the shoot through duty ratio $D = \frac{T_{sh}}{T_s}$.

At steady state, the average voltage across the capacitors is given by the equation (3.12):

$$V_c = \frac{T_{nsh}}{T_{nsh} - T_{sh}} V_{dc} \tag{3.12}$$

the pick dc-link voltage across the inverter bridge is

$$\hat{V}_{in} = 2V_c - V_{dc} = \frac{1}{1-2D} V_{dc} = BV_{dc} \tag{3.13}$$

$$B = \frac{1}{1-2D} \geq 1 \tag{3.14}$$

Where *B* is the boost factor resulting from the shoot-through state, and the output peak phase voltage from the inverter can be expressed as

$$\hat{V}_{ph} = M.\frac{1}{2} V_{in} \tag{3.15}$$

Using the equation (3.13), the equation (3.15) can be rewritten as

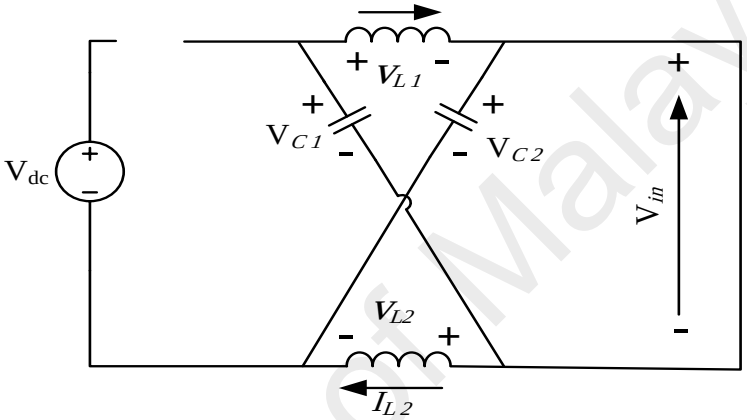
$$\hat{V}_{ph} = M.B.\frac{1}{2} V_{dc} = G\frac{1}{2}.V_{dc} \tag{3.16}$$

where *M* is the modulation index, *G* is the voltage gain and *B* is the boost factor

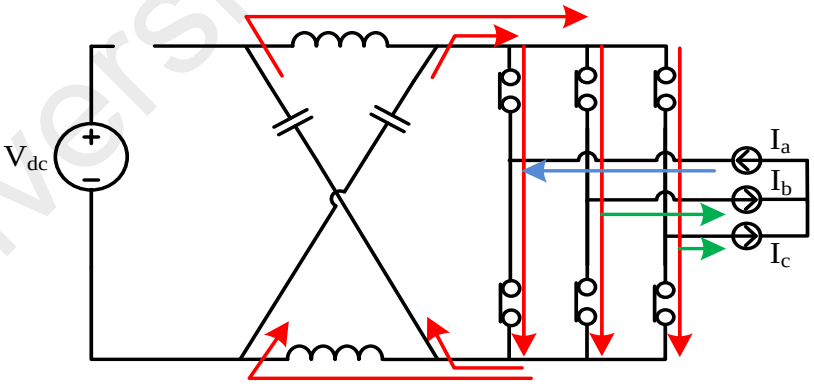
The ST state does not affect the PWM control of the inverter, because it equivalently produces the same zero voltage to the load terminal. The available ST period is limited by the zero-state period that is determined by the modulation index.

The structure of the equivalent circuits and the current paths during the ST and non ST modes are depicted in Figure 3.8 and Figure 3.9 respectively.

The inverter bridge is equivalent to a short circuit when the inverter bridge is in the shoot-through state, as shown in Figure 3.8 (a), whereas the inverter bridge becomes an equivalent current source when it is in one of the six active states, or when it is in one of the two traditional zero states as shown in Figure 3.9 (a).

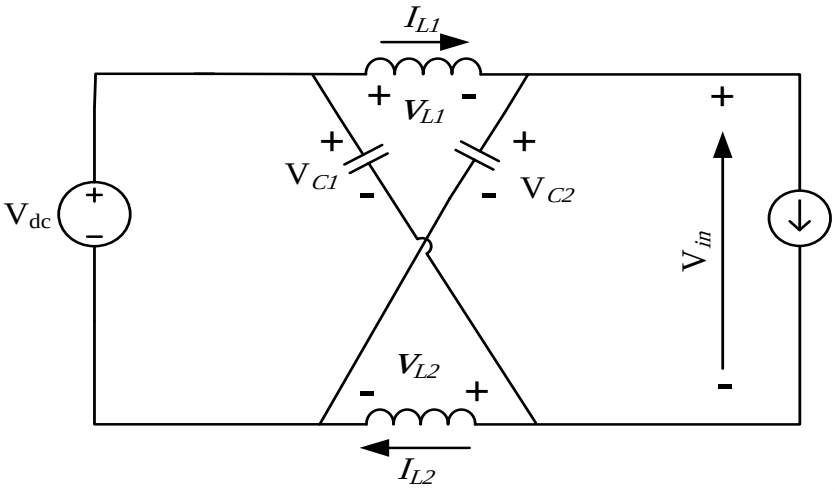


(a) Equivalent circuit during ST state.

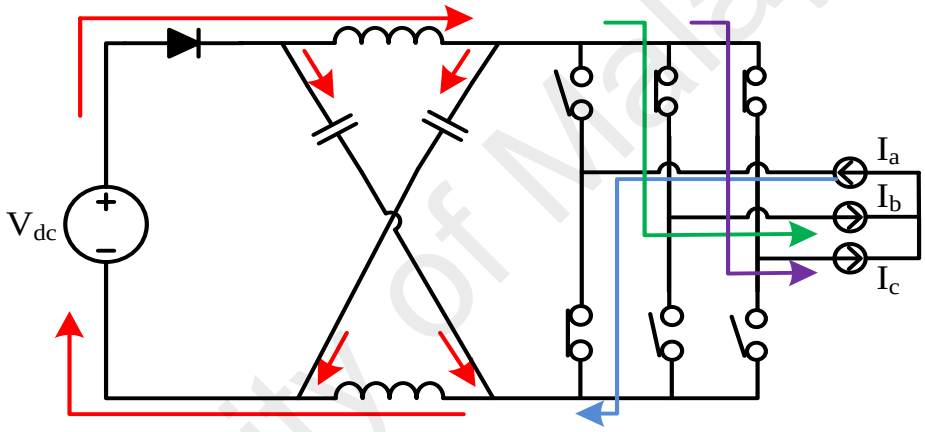


(b) Three-leg shoot-through.

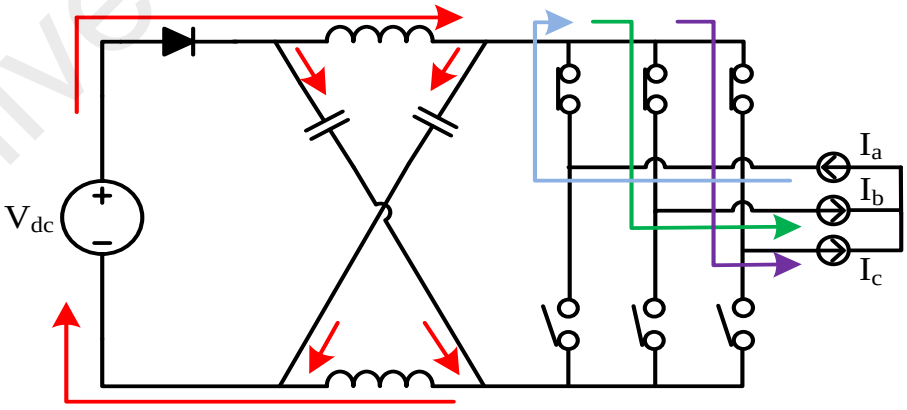
Figure 3.8: Equivalent circuit and current path during the shoot-through state.



(a) Equivalent circuit



(b) Active state.



(c) Zero state.

Figure 3.9: Equivalent circuit and current path during non ST state.

3.3.3 The Proposed ODZSI for impedance network three-phase H-bridge.

This section now extends the analysis presented in section 3.2.3. The three-phase modulation problem is reduced to very simple calculations where the main task of ODZSI is to determine the switching states and their corresponding duty cycles following the same steps.

The switching states S_a , S_b , and S_c will be defined for the *a*, *b* ,and *c* phases respectively. Assuming proper operation, the inverter output line-to-ground voltages (defined from the phase nodes *a*, *b*, and *c* to ground g in Figure 3.7) follow the switching states as

$$\begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} = BV_{dc} \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \tag{3.17}$$

The line-to-neutral voltages may be determined directly from the line-to-ground voltages by:

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} \tag{3.18}$$

Therein, the line-to ground voltage contains a third harmonic component which is added in order to maximize the inverter output voltage.

Inverter line-to-line voltages are related to the line-to-ground voltages by:

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} \tag{3.19}$$

the commanded line-to-ground voltages will be defined herein as:

$$\begin{bmatrix} v_{ag}^* \\ v_{bg}^* \\ v_{cg}^* \end{bmatrix} = \frac{MV_{dc}}{2} \begin{bmatrix} \cos(\omega t) \\ \cos\left(\omega t - \frac{2\pi}{3}\right) \\ \cos\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} + \frac{V_{dc}}{2} \left[1 - \frac{M}{6}\cos(3\omega t)\right] \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \tag{3.20}$$

where the modulation index M has a range of

$$0 \leq M \leq {}^{\sqrt{3}}/_{2} \tag{3.21}$$

and ωt is the inverter electrical angle. In the equation (3.20), the first set of terms on the right hand side define a sinusoidal set of commanded voltages with controllable amplitude and frequency through M and ωt respectively. The second set of terms on the right hand side are the common-mode terms. In this case, a dc offset is applied so that the commanded line-to-ground voltages will be within the allowable range of zero to the dc voltage. The other common-mode term is a third harmonic component which is added to fully utilize the dc source voltage.

In order to generate the reference voltage with a minimum distortion, the duty-cycle computation between the two nearest voltage levels of the power converter need to be calculated accurately. Based on volt-second balancing principle and geometric expressions as shown in Figure 3.10, the dwell times for the stationary vectors can be derived using the equations (3.7) - (3.20).

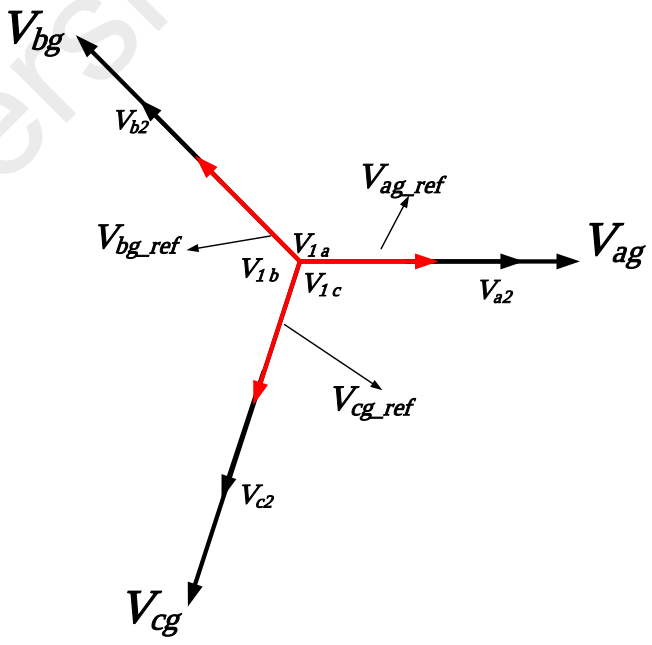


Figure 3.10: Generation of V_{ag_ref}, V_{bg_ref} and V_{cg_ref} .

With the switching state of phase x ($S_{ph\text{-}x}$) and its dwell times T_1 and T_2 are calculated, the next step is to generate the ZSI switching pulses. The arrangement of the switching sequence should minimize the device switching frequency.

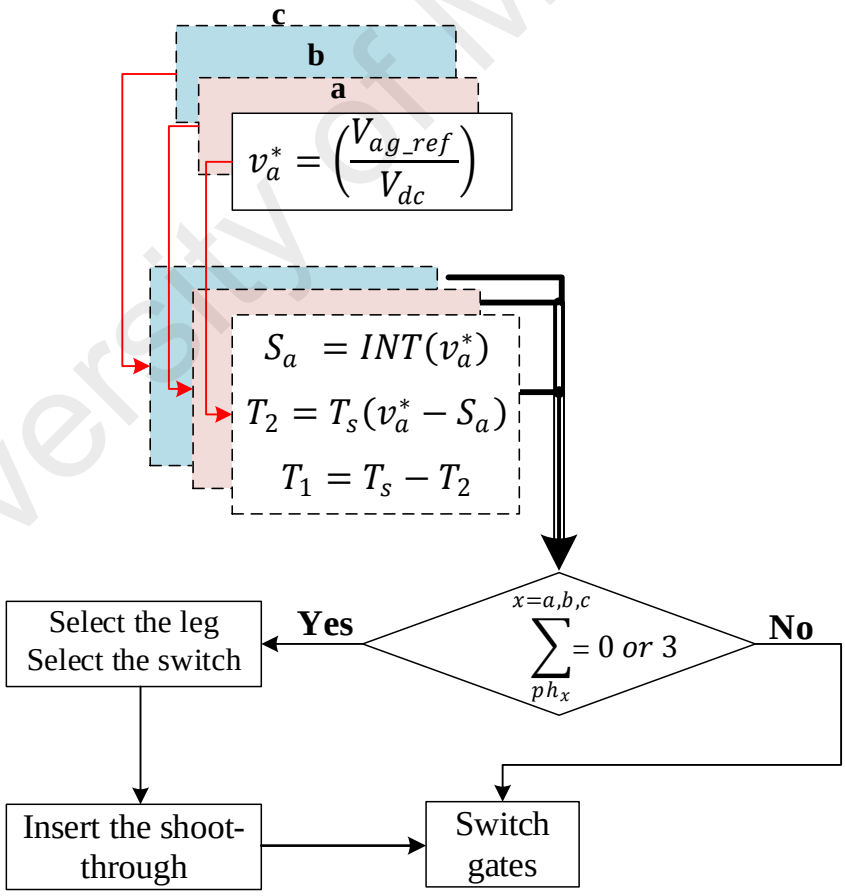
Table 3.4 lists the switching states for a three-phase legs ZSI controlled by the proposed algorithm. Besides the six active states, the three-phase ZSI has an additional ST state to boost the dc-link voltage. Again, as discussed in the above subsection, the zero states (000) and (111) can be fully or partly utilized for shoot-through states to not affect the normalized volt-sec average since the both states have the same output voltage across the load, i.e.0 V.

The ST state can be achieved by switching ON the two switches of any arm phase, two phase legs or all three legs. However, in order to ensure that no extra commutations are introduced and reduce the switching losses, the ST will be inserted only in one phase leg (ST 1, ST 2 and ST 3). The other ST states will not be used since they require the switching of at least two phase-legs at every transition. Furthermore, the switching patterns must be symmetrical to minimize the total harmonic distortion THD.

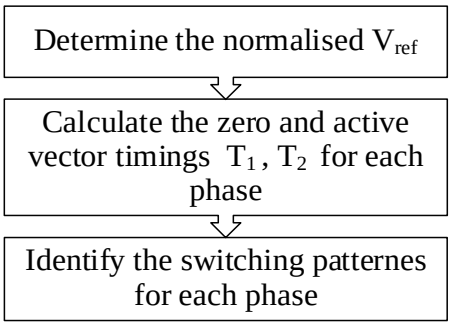
Table 3.4: The Switching States for a three-phase Legs ZSI Controlled by ODZSI. ($\bar{S}$ is the complement of S)

	S_1	**S_2**	**S_3**	**S_4**	**S_5**	**S_6**
Active (100)	1	0	0	1	0	1
Active (110)	1	0	1	0	0	1
Active (010)	0	1	1	0	0	1
Active (011)	0	1	1	0	1	0
Active (001)	0	1	0	1	1	0
Active (101)	1	0	0	1	1	0
Null (000)	0	1	0	1	0	1
Null (111)	1	0	1	0	1	0
ST 1	1	1	S_3	$\bar{S}_3$	S_5	$\bar{S}_5$
ST 2	S_1	$\bar{S}_1$	1	1	S_5	$\bar{S}_5$
ST 3	S_1	$\bar{S}_1$	S_2	$\bar{S}_4$	1	1
ST 4	1	1	1	1	S_5	$\bar{S}_5$
ST 5	1	1	S_3	$\bar{S}_3$	1	1
ST 6	S_1	$\bar{S}_1$	1	1	1	1
ST 7	1	1	1	1	1	1

The ST state is inserted when the switching state $S_{ph\text{-}a} = S_{ph\text{-}b} = S_{ph\text{-}c} = 1$ ($\sum S_{ph-x} = 3$) or $S_{ph\text{-}a} = S_{ph\text{-}b} = S_{ph\text{-}c} = 0$ ($\sum S_{ph-x} = 0$) by turning ON the upper and bottom switches of any phase leg (a, b or c) simultaneously without affecting the active vectors. In general, the switching sequence design is not unique but the selected ST are carefully inserted in which the transition from one switching state to the next involves only two switches in the same inverter leg to turn ON or OFF, and the transition from one mode to the next mode requires no switching devices for the minimization of the device switching frequency. The operation principle of the proposed modulation technique method for ZSI is depicted in Figure 3.11. This process is repeated every switching cycle for each phase to accurately determine the switching states and their dwell times.



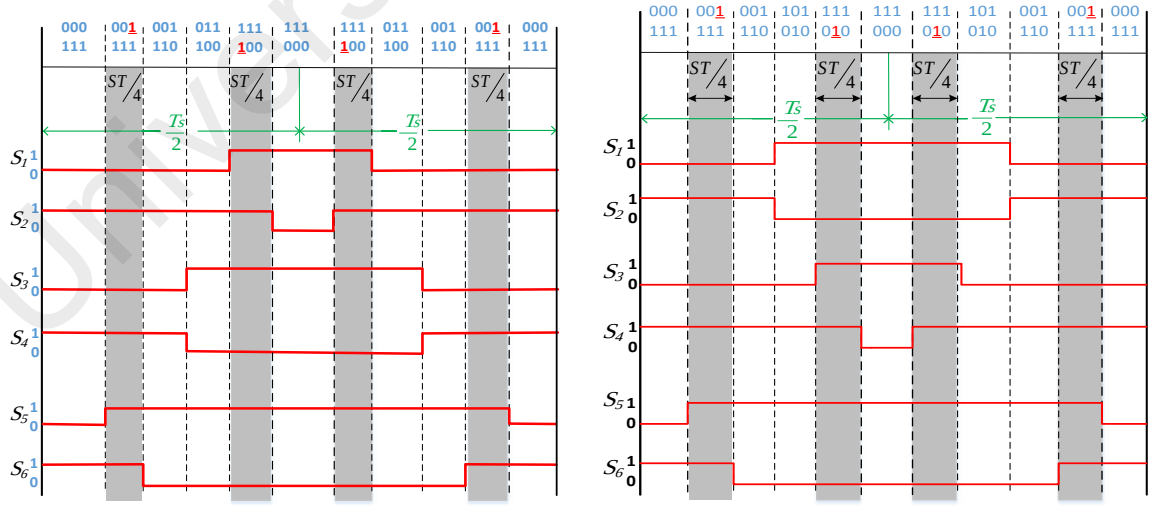
(a)



(b)

Figure 3.11: **(a)** Proposed ODZSI strategy for three-phase ZSI, and **(b)** The flow diagram.

Figure 3.12 illustrates the six different sequence modes with their corresponding switching patterns generated by the controller within a cycle of the waveform output; each mode is operating for a period of $\frac{\pi}{3}$. The ST time is divided into four equal parts in every control cycle T_S, and inserted immediately adjacent the active states during the transition from the null to the active states to avoid additional switching operations and keep each of the switches in the inverter turns ON and OFF once per sampling period.



(a) Mode I **(b)** Mode II.

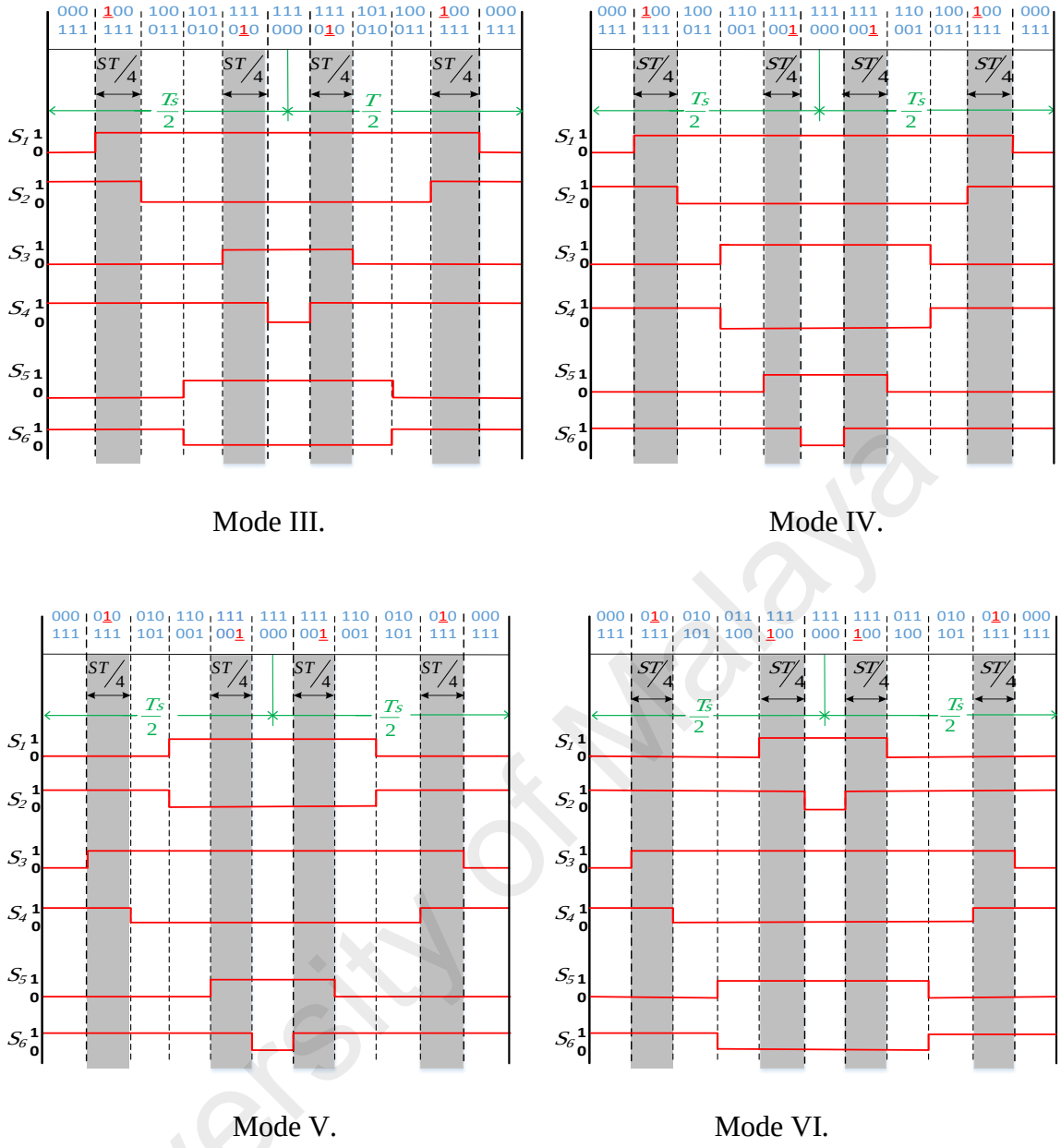


Figure 3.12: The different six modes with their corresponding switching patterns generated by the ODZSI.

Furthermore, the conduction time intervals for the six switches (S_1~S_6) during one switching cycle T_s are tabulated in Table 3.5.

Table 3.5: Conducting times for each switch during one control cycle for there-phase ZSI.

Mode	Phase A		Phase B		Phase C	
	Switch	Conduction time	Switch	Conduction time	Switch	Conduction time
I	S_1	T_{2a}	S_3	T_{2b}	S_5	$T_{2c}+\frac{1}{2}T_{st}$
	S_2	$T_{1a}+\frac{1}{2}T_{st}$	S_4	T_{1b}	S_6	T_{1c}
II	S_1	T_{2a}	S_3	T_{2b}	S_5	$T_{2c}+\frac{1}{2}T_{st}$
	S_2	T_{1a}	S_4	$T_{1b}+\frac{1}{2}T_{st}$	S_6	T_{1c}
III	S_1	$T_{2a}+\frac{1}{2}T_{st}$	S_3	T_{2b}	S_5	T_{2c}
	S_2	T_{1a}	S_4	$T_{1b}+\frac{1}{2}T_{st}$	S_6	T_{1c}
IV	S_1	$T_{2a}+\frac{1}{2}T_{st}$	S_3	T_{2b}	S_5	T_{2c}
	S_2	T_{1a}	S_4	T_{1b}	S_6	$T_{1c}+\frac{1}{2}T_{st}$
V	S_1	T_{2a}	S_3	$T_{2b}+\frac{1}{2}T_{st}$	S_5	T_{2c}
	S_2	T_{1a}	S_4	T_{1b}	S_6	$T_{1c}+\frac{1}{2}T_{st}$
VI	S_1	T_{2a}	S_3	$T_{2b}+\frac{1}{2}T_{st}$	S_5	T_{2c}
	S_2	$T_{1a}+\frac{1}{2}T_{st}$	S_4	T_{1b}	S_6	T_{1c}

3.3.4 The Implementation of ODZSI based Maximum Boost Control for One-Leg Shoot-Through (ODZSI-MBC_1)

The one-leg shoot-through mode shorts two switches on the same phase-leg of the inverter. The current path of the one-leg short-through mode is shown in Figure 3.13

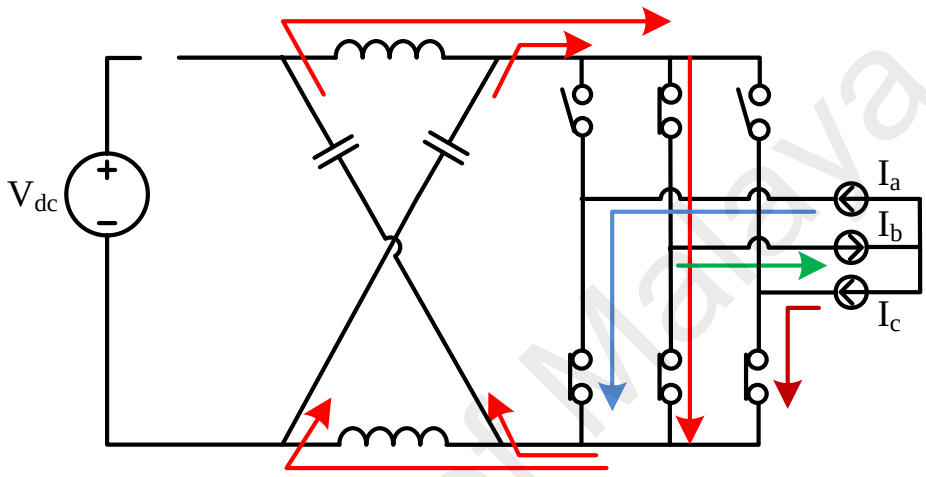


Figure 3.13: Schematic diagram of one leg shoot-through mode.

According to the principles of maximum boost control, the ST interval should be as large as possible during each carrier cycle to maximize the boost factor B.

Following the same procedure as in the previous section, the ST state is inserted when the switching state $S_{ph\text{-}a} = S_{ph\text{-}b} = S_{ph\text{-}c} = 1$ $(\sum S_{ph-x} = 3)$ or $S_{ph\text{-}a} = S_{ph\text{-}b} = S_{ph\text{-}c} = 0$ $(\sum S_{ph-x} = 0)$, where all zero states are turned to ST state by simultaneously turning ON the upper and bottom switches of any phase leg (*a*, *b*, or *c*) without affecting the active vectors. Zero states (000) and (111) are fully replaced by ST state because both states have the same output voltage across the load, i.e., 0 V, so as not affect the normalized volt-sec average. The ST state can be achieved by switching ON the two switches of any arm phase, two phase legs, or all three legs. However, ST is inserted only on one phase leg (ST 1, ST 2 and ST 3) to ensure that no extra commutations are introduced and reduce the switching

losses. The other ST states will not be used as they require that at least two phase legs switch at every transition. Furthermore, switching patterns should be symmetrical to minimize the total harmonic distortion. The operation principle of ODZSI based MBC for ZSI is depicted in Figure 3.14. This process is repeated every switching cycle for each phase to accurately determine the switching states and their dwell times.

The controller generates six different sequence modes within a cycle of the desired voltage waveform in the output, and each mode is operated for a period of $\frac{\pi}{3}$. The six modes are listed in Table 3.6, and their corresponding switching patterns are depicted in Figure 3.15. This figure shows that the number of switching transitions decreased significantly as each switch is locked to the positive or negative dc rail for a period of $2\pi/3$ per cycle of the fundamental frequency. The switching sequence design is generally not unique, but the selected ST is carefully inserted in which the transition from one mode to the next mode requires none or the minimum number of switching to decrease the device switching frequency

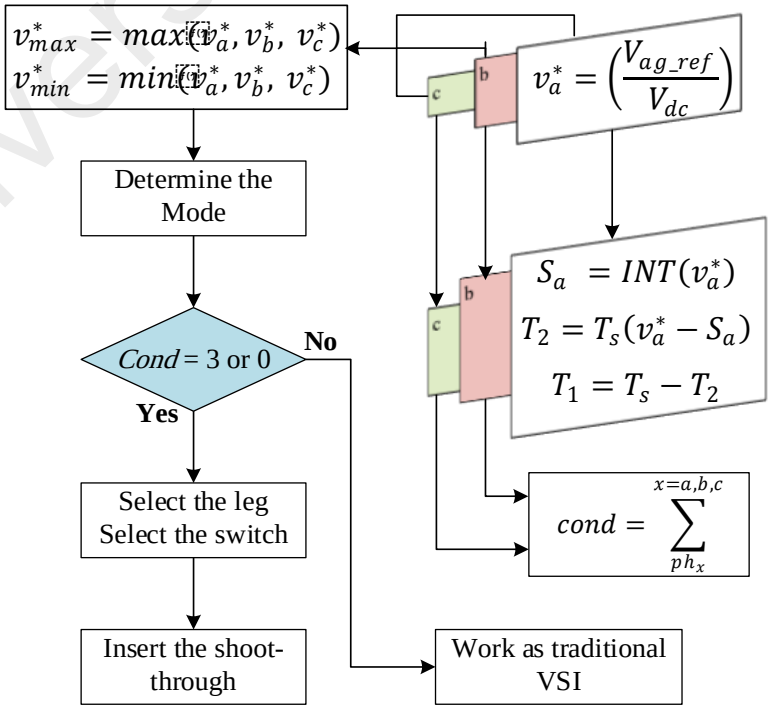


Figure 3.14: Proposed ODZSI based MBC for one-leg ST mode.

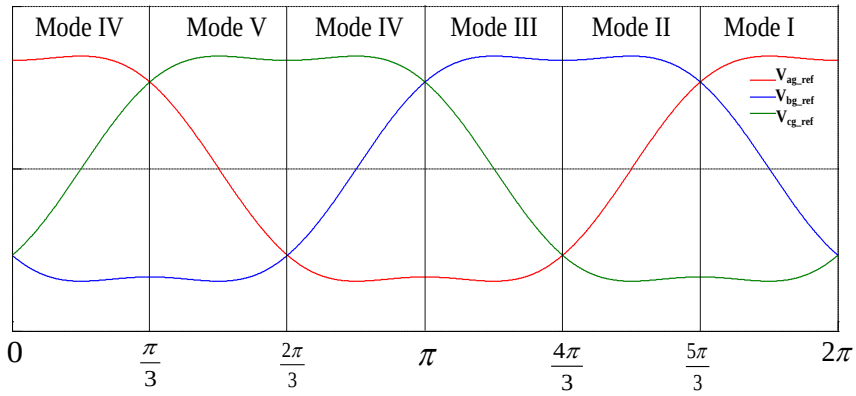
As mentioned above, the upper switch S_1 in phase *a* is ON when the minimum of three-phase normalized reference signals V^*_{min} ($V^*_{ag\_ref}$, $V^*_{bg\_ref}$, $V^*_{cg\_ref}$,) = $V^*_{ag\_ref}$ throughout Modes III and IV. Similarly, S_3 is ON when $V^*_{min} = V^*_{bg\_ref}$ during Modes V–VI, and the upper switch S_5 in phase *c* is locked to the positive dc rail when $V^*_{min} = V^*_{cg\_ref}$ in Modes I–II. Furthermore, the lower switches (even numbered) are clamped to the negative dc rail when the maximum of three-phase normalized reference signals V^*_{max} ($V^*_{ag\_ref}$, $V^*_{bg\_ref}$, $V^*_{cg\_ref}$,) = $V^*_{xg\_ref}$. Thus, when $V^*_{max} = V^*_{ag\_ref}$, S_2 is continually conducted during Modes VI and I. Similarly, when $V^*_{max} = V^*_{bg\_ref}$, the lower switch S_4 of phase *b* is ON during Modes II and III. Finally, S_6 is locked to the negative dc rail when $V^*_{max} = V^*_{cg\_ref}$ during Modes IV and V. All these cases are summarized in the equations (3.22) and (3.23).

$$\left.\begin{array}{ll} V^*_{\min} = V^*_{ag\_ref} \Rightarrow S_1 = 1 & \text{mode III-IV} \\ V^*_{\min} = V^*_{bg\_ref} \Rightarrow S_3 = 1 & \text{mode V-VI} \\ V^*_{\min} = V^*_{cg\_ref} \Rightarrow S_5 = 1 & \text{mode I-II} \end{array}\right\} \tag{3.22}$$

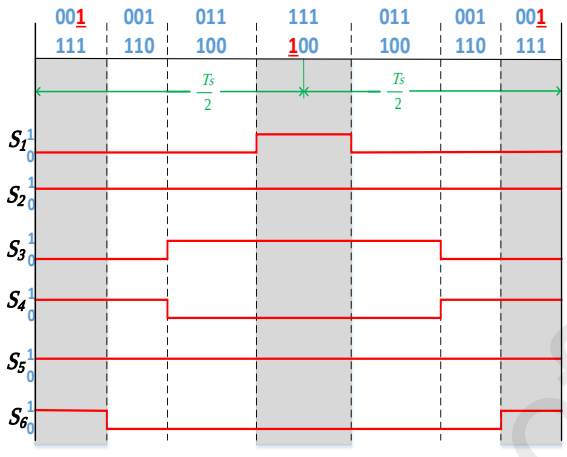
$$\left.\begin{array}{ll} V^*_{\max} = V^*_{ag\_ref} \Rightarrow S_2 = 1 & \text{mode VI-I} \\ V^*_{\max} = V^*_{bg\_ref} \Rightarrow S_4 = 1 & \text{mode II-III} \\ V^*_{\max} = V^*_{cg\_ref} \Rightarrow S_6 = 1 & \text{mode IV-V} \end{array}\right\} \tag{3.23}$$

Table 3.6: The Different Six Modes using ODZSI-MBC_1.

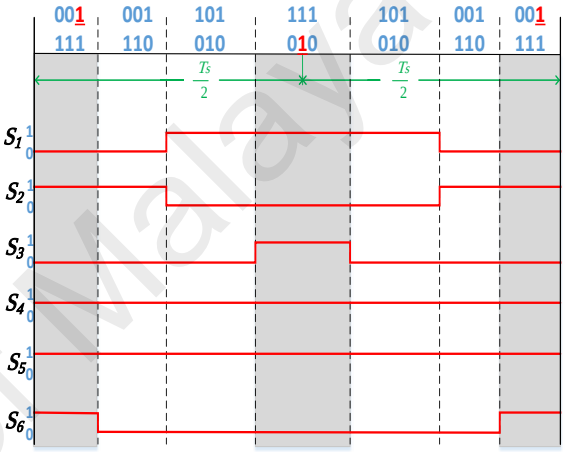
Mode	I	II	III	IV	V	VI
$V^*_{ag\_ref}$	Maximum	Middle	Minimum	Minimum	Middle	Maximum
$V^*_{bg\_ref}$	Middle	Maximum	Maximum	Middle	Minimum	Minimum
$V^*_{cg\_ref}$	Minimum	Minimum	Middle	Maximum	Maximum	Middle
ON-switches	S_5, S_2	S_5, S_4	S_1,S_4	S_1,S_6	S_6, S_3	S_3, S_2



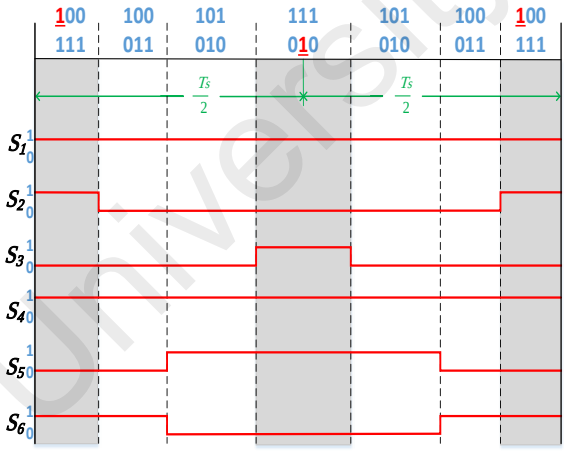
(a)



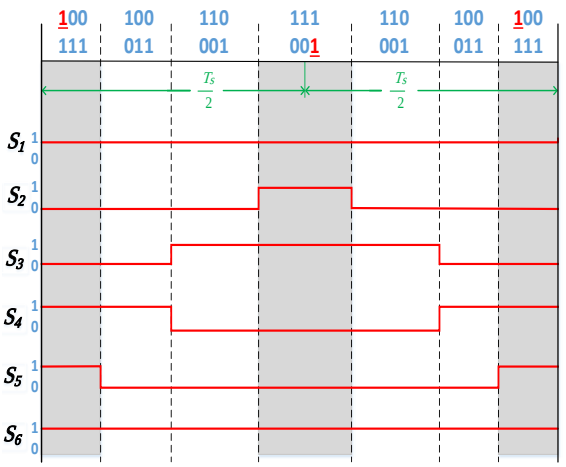
(a) Mode I.



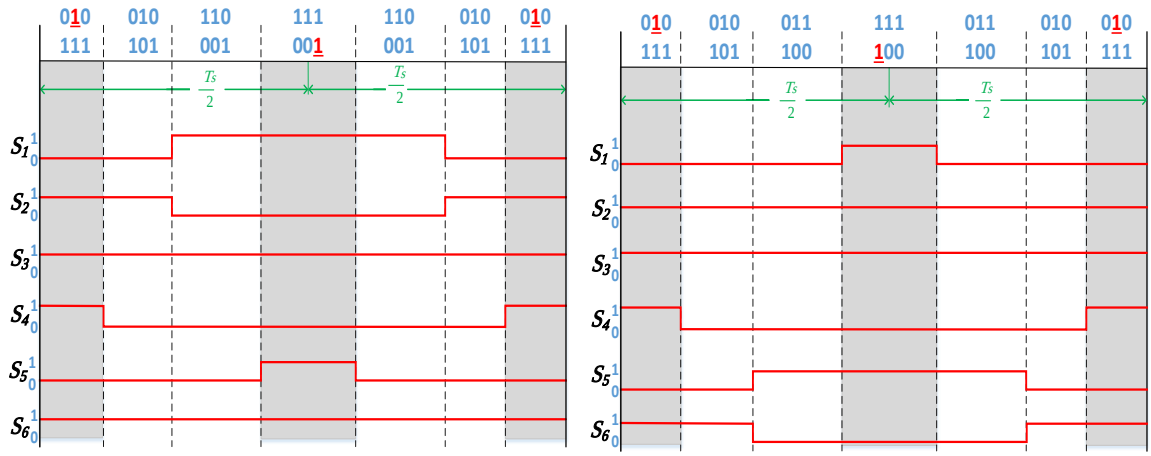
(b) Mode II



(c) Mode III



(d) Mode IV.



(e) Mode V. **(f)** Mode VI

Figure 3.15: The different six modes with their corresponding switching patterns generated by ODZSI-MBC_1.

Figure **3.16** shows the waveform of the ST throughout one cycle of the fundamental frequency for a given modulation index, as can be seen the shoot-through duty cycle 'D' varies at six times the output frequency. However, the variation of D introduces a low-frequency current ripple that is associated with the output frequency in the inductor current and the capacitor voltage.

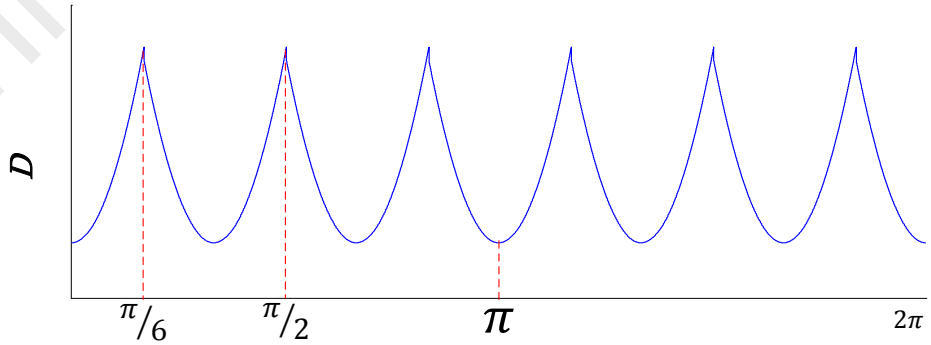


Figure 3.16: Variation of D during one cycle of the fundamental output

The ST time is repeated each period of $\pi/3$ and is given by

$$T_{st} = T_s - \frac{T_s \cdot M}{2}\left(\sin \omega t - \sin\left(\omega t - \frac{2\pi}{3}\right)\right) \tag{3.24}$$

$$D(\omega t) = 1 - \frac{\sqrt{3}}{2} M \cos\left(\omega t - \frac{\pi}{3}\right) \tag{3.25}$$

And $\frac{\pi}{6} \leq \omega t \leq \frac{\pi}{2}$

Hence the average duty ratio of the ST time can be calculated by integrating both sides of equation (3.24)

$$\overline{D} = \frac{1}{\frac{\pi}{3}} \int_{\frac{\pi}{6}}^{\frac{\pi}{2}} 1 - \frac{M}{2}\left[\sin(\omega t) - \sin(\omega t - \frac{2\pi}{3})\right] d\omega t \tag{3.26}$$

Then

$$\overline{D} = 1 - \frac{3\sqrt{3}M}{2\pi} \tag{3.27}$$

The boost factor is:

$$B = \frac{1}{1-2D} = \frac{\pi}{3\sqrt{3}M - \pi} \tag{3.28}$$

And the voltage gain:

$$G = MB = \frac{M\pi}{3\sqrt{3}M - \pi} \tag{3.29}$$

3.3.5 The Implementation of ODZSI based Maximum Boost Control for Three-leg Shoot-through (ODZSI-MBC_3)

The three-leg shoot-through mode shorts all the switches of the inverter. The current path of the three-leg short-through mode is shown in Figure 3.17.

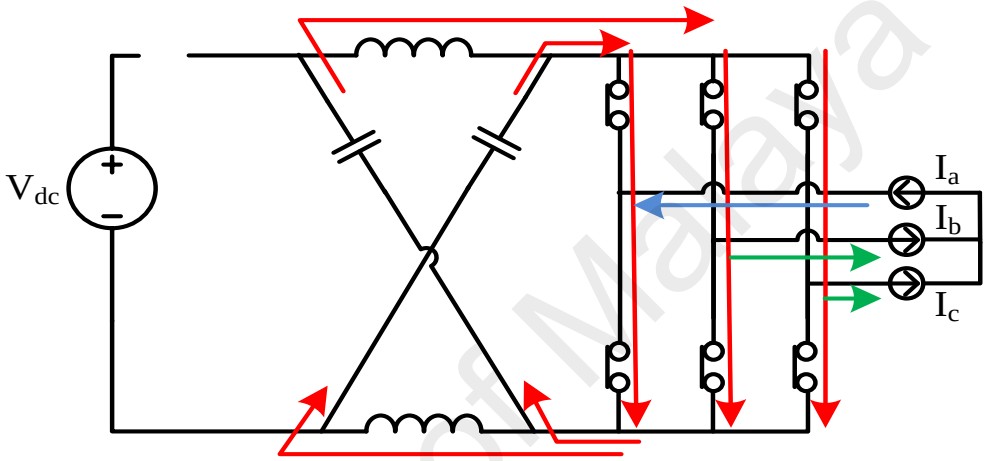


Figure 3.17: Schematic diagram of three-leg ST mode.

As mentioned earlier, the insertion of the ST state is not unique. However, For the purpose of reducing the conduction losses and improving the inverter efficiency, it is possible to involve all the three legs to produce the ST. Similarly, using the same principal of ODZSI-MBC_1 in the previous section, the ST state is introduced when the switching state $S_{ph\text{-}a} = S_{ph\text{-}b} = S_{ph\text{-}c} = 1$ ($\Sigma S_{ph\text{-}x}=3$) or $S_{ph\text{-}a} = S_{ph\text{-}b} = S_{ph\text{-}c} = 0$ ($\Sigma S_{ph\text{-}x}=0$) where all zero states are turned to ST state by turning ON all the switches (S_1~S_6) simultaneously without affecting the active vectors. Furthermore, the switching patterns must be symmetrical to minimize the total harmonic distortion. The operation principle of the proposed modulation technique method for ZSI is depicted in Figure 3.18. This process is repeated every switching cycle for each phase to determine the switching states and their dwell times accurately.

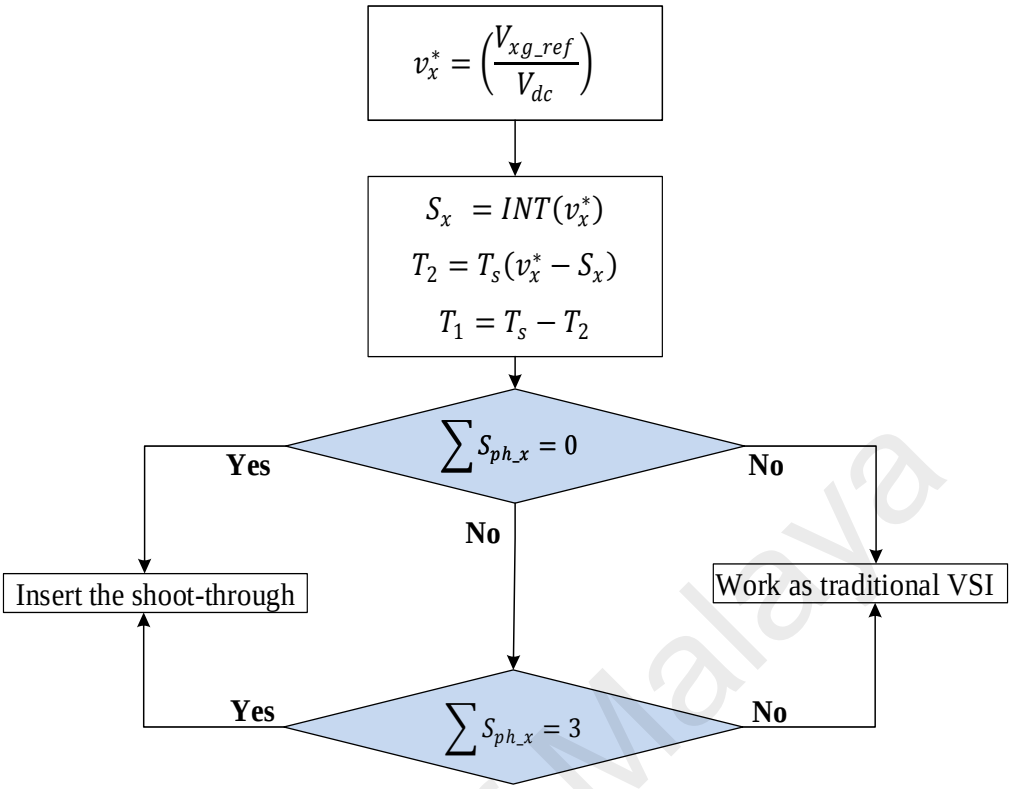
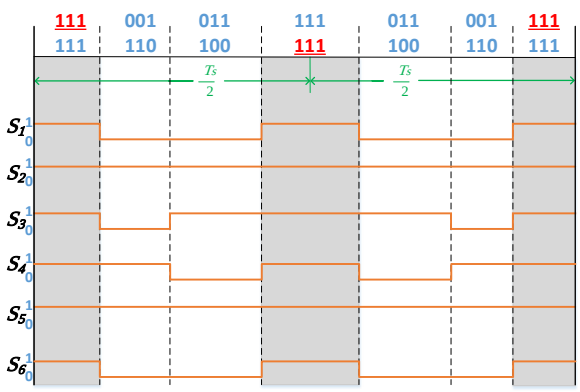
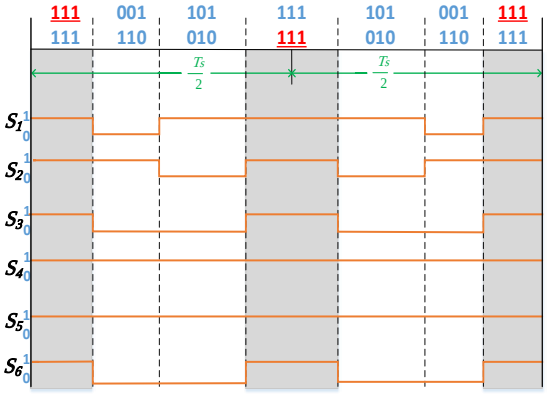


Figure 3.18: Proposed ODZSI –MBC for three-leg ST mode.

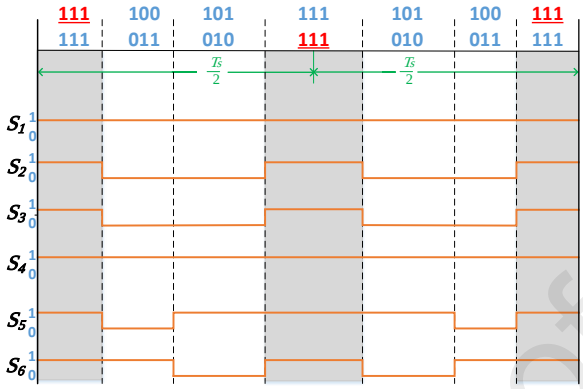
The controller generates six different sequence modes within a cycle of the desired voltage waveform at the output, each mode is operating for a period of $\frac{\pi}{3}$, these six modes and their corresponding switching patterns are depicted in Figure 3.19. It can be clearly seen that the number of the switching transition is doubled compared to ODZSI-MBC_1. In addition, the transition from one switching state to the next involves at least two switches to turn ON or OFF, and the transition from one mode to the next mode requires no switching devices.



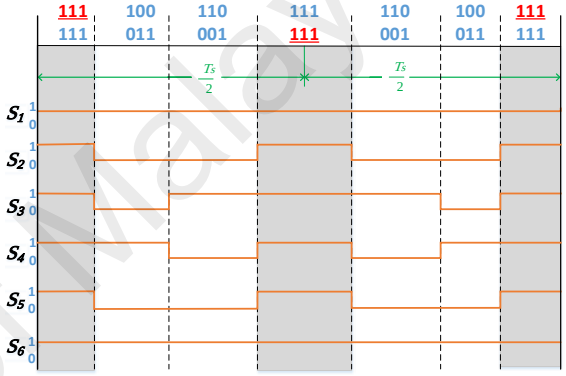
(a) Mode I.



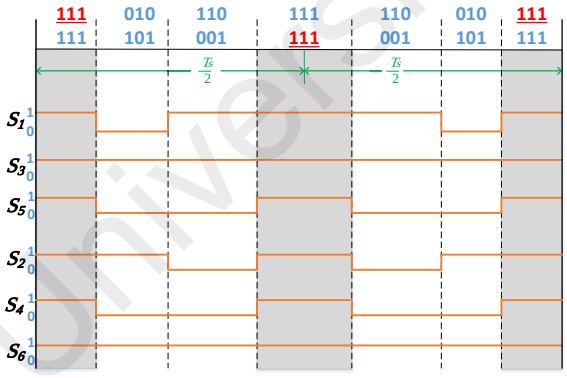
(b) Mode II



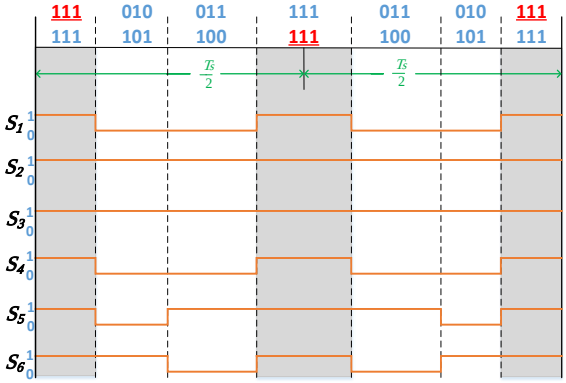
(c) Mode III



(d) Mode IV.



(d) Mode V.



(e) Mode VI

Figure 3.19: The different six modes with their corresponding switching patterns generated by ODZSI-MBC_3.

When the shoot-through is located only on one phase leg, the switching frequency losses are minimized. However, at the same time, the current stress on the switches during the shoot through time will be increased compared with shooting through all the legs simultaneously which leads to increase the conduction losses. Thus, the there-phase leg shout-through is more suitable for low switching frequency application. Moreover, Table 3.4 shows different combination of ST states ST 4 - ST 7 that can be used to reduce the current stress. By contrast, the switching losses are particularly high for high-switching-frequency applications, thereby significantly decreasing qZSI efficiency. In conclusion, a trade-off always exists between conduction (P_c) and switching (P_{sw}) losses, which determines the selection of optimized control method according to the application.

3.3.6 Power losses analysis for ODZSI-MBC

Power loss is an important index for cost estimation and cooling system in inverters design. In general, there are two (2) types of semiconductor losses in power electronics devices. Firstly, the conduction loss due to the voltage drop across the active semiconductor device when conducting current; and secondly, the switching loss occurs at each current commutation of the device and it is directly related to the switching frequency.

The loss calculation of the six switches cannot be completed based on one operation point. Thus, the energy loss in the switches during each switching cycle will be accumulated for one output voltage cycle (2π). Then, the power loss is calculated by dividing the total energy loss by 2π.

The total power loss in the switch can be represented by the equations (Graovac, Purschel, & Kiep, 2006; Klein, 2006):

$$P_{MOSFET} = P_{SW} + P_c \tag{3.29}$$

$$P_{sw} = \left(\frac{BV_{dc} * I_{ph}}{2}\right)(t_2 + t_3)(F_{sw}) \tag{3.30}$$

Where I_{ph} is the average current flowing throw the switch.

From Equation (3.30), switching losses are generated when turning ON and OFF the switch, which are proportional to switching frequency. When switching frequency reaches a certain value, switching losses become a major part of power losses, which significantly affects the inverter efficiency.

The current flowing through the ZSI switches i_{ph} consists of two components: one is the ac load current i_{ac} during the active states while the current during the shoot-through time interval is $2i_L \mp i_{ac}$ for the ODSZI_1.

We assume the output current to be sinusoidal: $i_{ac} = \sqrt{2} I_{ac} \, sin\omega t$,the conduction loss can be calculated by:

$$P_c = \frac{\omega D_{nst}}{\pi} \int_0^{2\pi/\omega} R_{ds(on)} \, i_{ac}^2 \, (t)dt + \frac{\omega D}{\pi} \int_0^{2\pi/\omega} R_{ds(on)} \, [2\overline{I_L} \mp i_{ac}(t)]^2 dt \quad (3.31)$$

where $D_{nst} = \frac{T_{nst}}{T_s}$, $R_{ds(on)}$ is the drain–source on-state resistance and $\overline{I_L}$ represents the average inductor current.

The output power of the three-phase inverter is

$$P_{out} = \frac{3}{2} \hat{V}_{ph} \hat{I}_{ac} \cos\varphi \quad (3.32)$$

Assuming that the input power and the output power are equal, $\overline{I_L}$ is derived as

$$\overline{I_L} = P_{out}/V_{dc} \quad (3.33)$$

However, for ODZSI_3 and due to the symmetrical structure of the inverter, the average current during shoot through is evenly distributed in three parallel paths. The current

through the inverter during shoot through is twice of the inductor current. Therefore, the average current value in shoot through period through each switch is $\frac{2}{3} I_L$.

A comparison between the conduction and switching losses for ODZSI-MBC and SVPWM based MSBC was carried out and it will be presented in section 4.5.1.

3.4 Summary

In this chapter the fundamental and operation principles of the unified proposed control techniques for impedance-network inverters have been presented. This concept can be applied to single-phase and three-phase impedance-network topologies. Moreover, the ODZSI-MBC_3 achieves highest voltage gain by maximizing the ST period. However this method will also result in line frequency current through the Z-source inductor, thus this will cause a higher requirement of the passive components when the output frequency becomes very low. Therefore, the maximum boost control is suitable for applications that have a fixed or relatively high output frequency. The ODSZI-MBC_1 is proposed to minimize the switching loss. The mathematical details regarding the development of these strategies are provided and will be verified by simulation and experimentally in the next chapter.

CHAPTER 4: RESULTS AND DISCUSSION.

4.1 Introduction

To verify the validity and the feasibility of the proposed control strategies presented in the previous chapter, simulations using PLECS libraries coupled to the Matlab/Simulink, and experiments have been carried out using two laboratory prototypes. Moreover, two topologies, i.e. three-phase ZSI and single-phase qZSI have been employed to study the performance of the proposed algorithms.

This chapter is organized as following: firstly, the simulation and experimental results of the proposed ODZSI for single-phase qZSI are presented. Secondly, the simulation results of the implementation of the ODZSI for three-phase quasi-ZSI / ZSI are presented. This is followed by the experimental results of each test. Then, the simulation and experimental results of the implementation of the ODZSI –MBC_1 as well as ODZSI-MBC_3 are presented and discussed. At the end, a comparison of the power losses, and the Total Execution Time using the proposed control strategies is performed with other state of the art works.

4.2 The experimental verification of the proposed ODZSI for single-phase quasi-ZSI.

The single-phase quasi-Z- source inverter depicted in Figure 3.1 is modulated by the ODZSI using the following parameters: $L_1=L_2=1.3e^{-3}$ H, $C_1=C_2=3.2e^{-3}$ F. the switching frequency F_{sw}=10 kHz, a RL load comprising a 40 Ω resistor and three-phase 23 mH inductor was used in this study. The modulation index is set to 0.8 and the duty shoot-through is 0.17. The prototype is controlled by PLECS RT Box.

The simulation waveforms of the boosted dc-link (V_{in}) and the input (V_{dc}) voltages are depicted in Figure 4.1 (a). Moreover, Figure 4.1 (b) shows the simulation waveforms of the output voltage V_{out} (top) and the load current I_{ac} (bottom).

For V_{dc}= 80 V, M=0.8 and D =0.17, and based on the equation (3.3); the boosting factor B is equal to 1.5 and the theoretical dc-link pick voltage is 120 V.

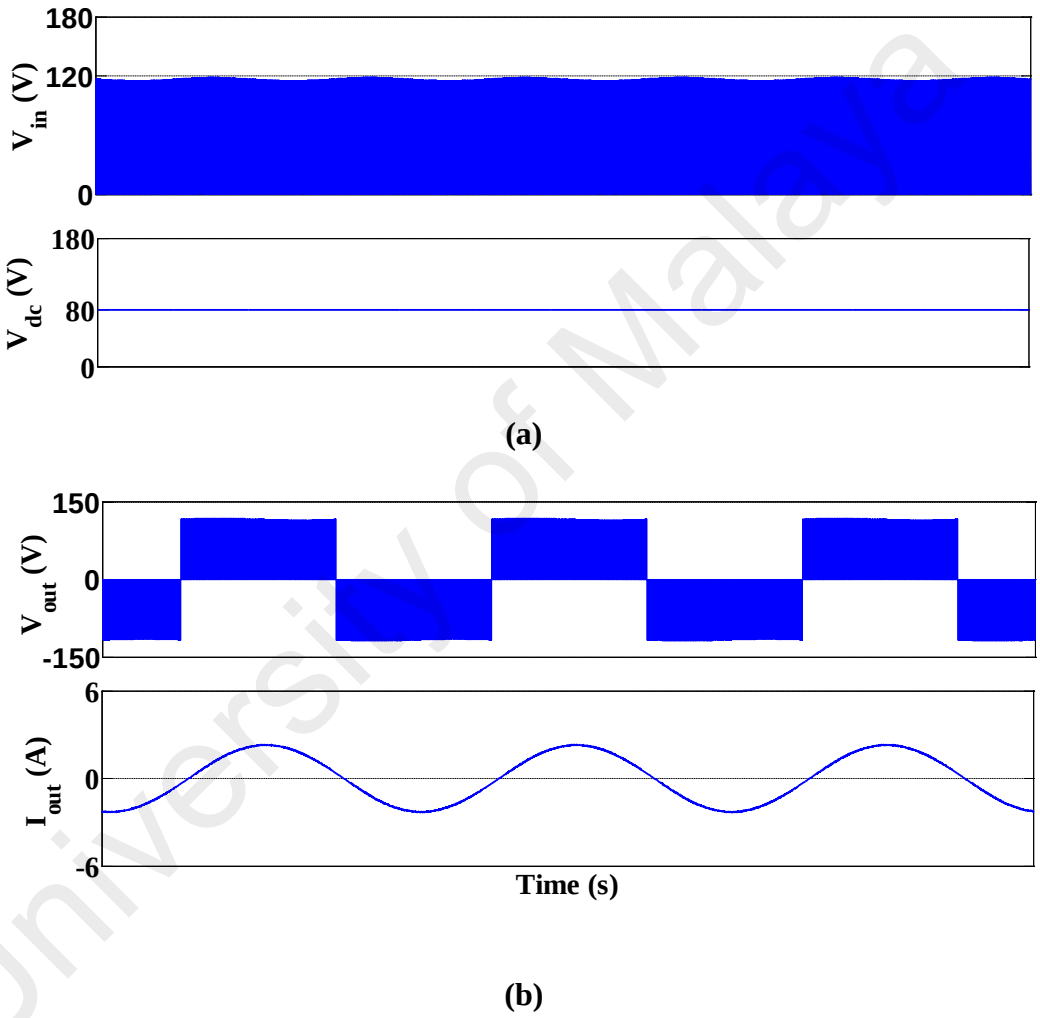


Figure 4.1: Simulation waveforms for M = 0.8 and D = 0.17 using the ODZSI. **(a)** V_{in} (top) and V_{dc} (bottom); **(b)** the output voltage (top) and the load current I_{ac} (bottom).

The simulation waveforms of V_{dc}, V_{in}, and the gate signals (S_1~ S_4) within two (2) control cycles ($2e^{-4}$ s) are plotted in Figure 4.2. It can be clearly seen that V_{in} becomes zero when the ST is inserted. As mentioned previously, the four times of ST behaviors per control cycle are achieved by the ODZSI where the two switches of the same leg are involved to produce the ST, i.e. S_3 and S_4 in the beginning and the end, and S_1 and S_2 in the middle of the control cycle, whereas the switches of the other phase-leg are working complimentary. It can be clearly seen that the controller generates the appropriate switching gate signals to achieve the desired output waveform.

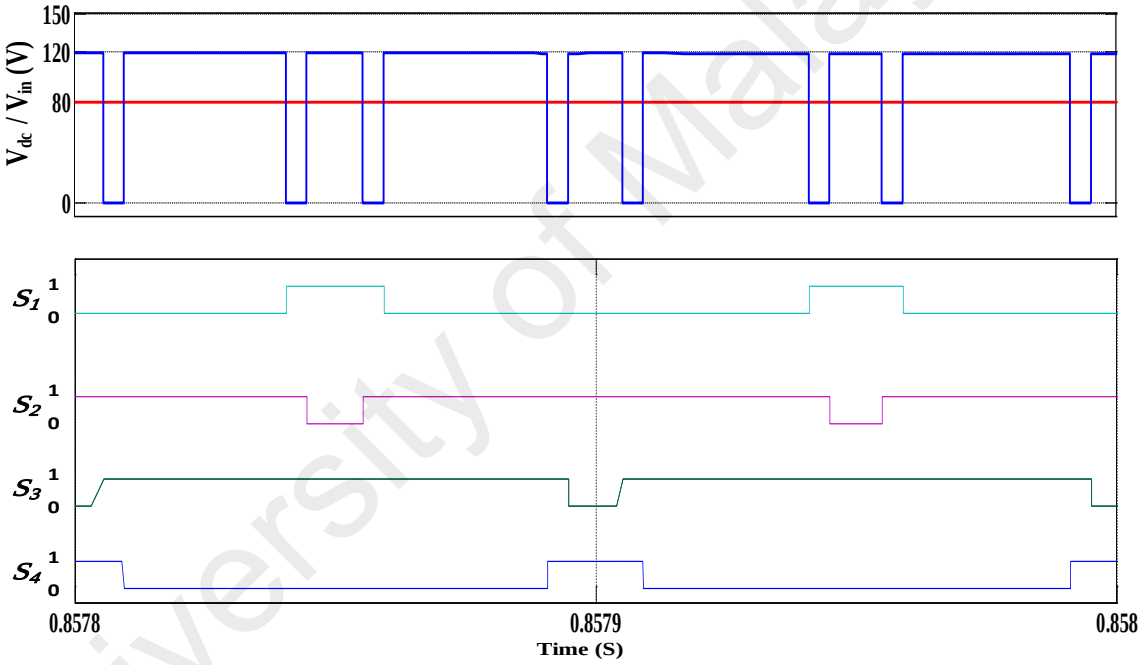
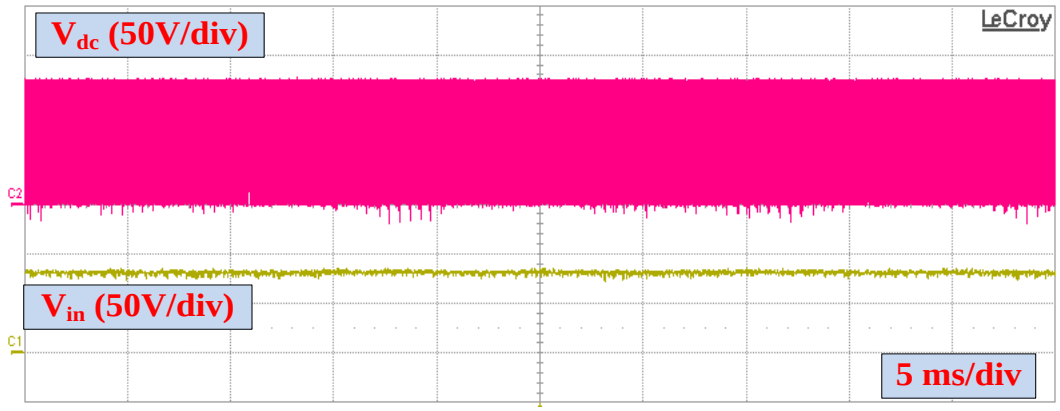
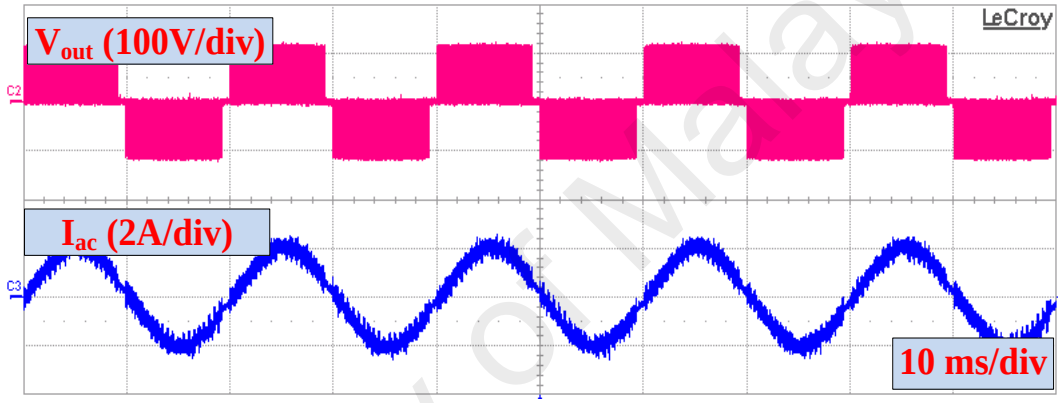


Figure 4.2: Simulation of zoomed V_{dc}, V_{in}, and the gate signals (S_1~S_4) generated by the ODZSI within two control cycles.

The obtained experimental results under the same operation parameters and the same laboratory prototype as in the simulation are illustrated in Figure 4.3. The waveform of the dc-link across the main bridge V_{in} (top) and the dc source voltage V_{dc} (bottom) are shown in Figure 4.3(a); the ac output voltage V_{out} (top) and the ac output current I_{ac} (bottom) are illustrated in Figure 4.3(b). The obtained simulation and hardware results met the desired output.



(a)



(b)

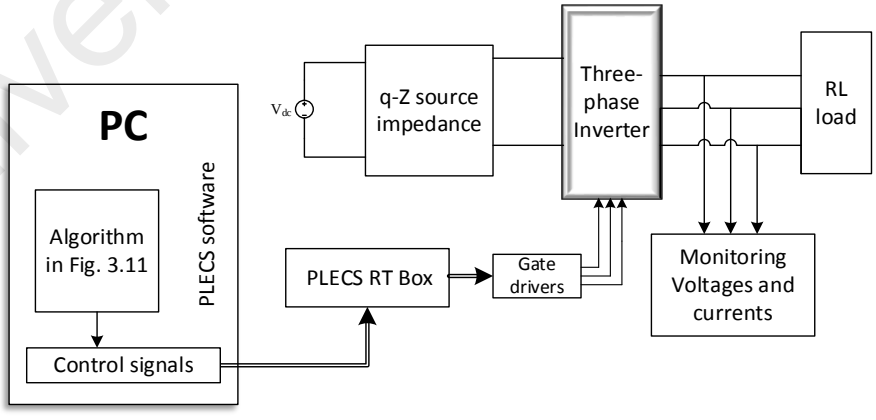
Figure 4.3: Experimental waveforms for $M = 0.8$ and $D = 0.17$ using the ODZSI. **(a)** V_{dc} (top) and V_{in} (bottom); **(b)** the voltage output (top) and the load current I_{ac} (bottom).

4.3 The experimental verification of the proposed ODZSI for three-phase quasi-ZSI.

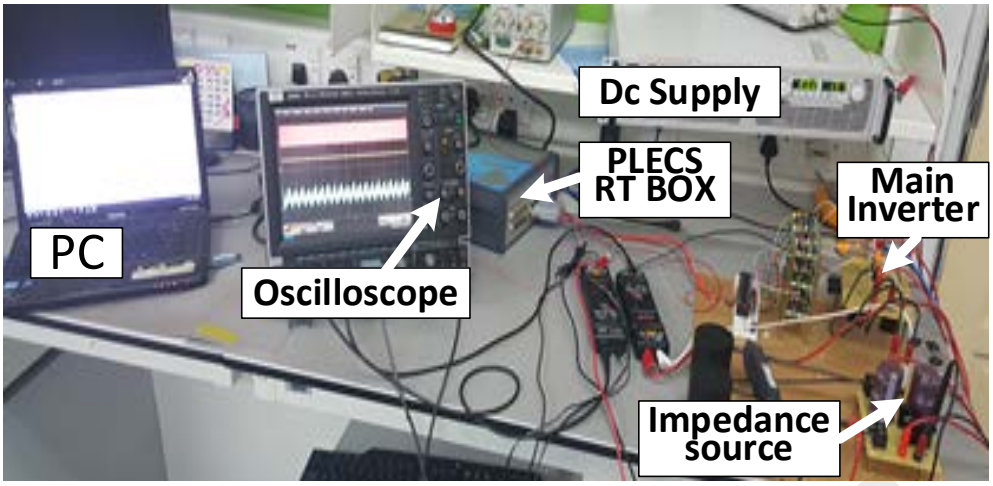
The ODZSI proposed in subsection 3.3.3 was implemented and the prototype of the three-phase quasi- ZSI depicted in Figure 2.3 (b) has been built as illustrated in Figure 4.4. The circuit specifications of the three-phase qZSI hardware are shown in Table 4.1. The prototype is controlled by PLECS RT Box.

Table 4.1: The simulation and hardware specifications.

Parameter	Value
Input voltage V_{dc}	80 V
Modulation index	0.8
ST duty ratio D	0, 0.2
Output frequency	50 Hz
Switching frequency F_{sw}	10 KHz
Impedance network capacitors	C_1=C_2=1200 µF
Impedance network inductors	L_1=L_2=1.3 mH
Three-phase RL load	25 Ω , 23 mH
Switches S_1~S_6	C2M0080120D
Input diode D_1	VS-15ETH03-N3



(a)



(b)

Figure 4.4: (a) Control block diagram; **(b)** the hardware prototype.

In the first case (no shoot-through case), a modulation index of 0.8 and shoot-through duty ratio, D=0 were used. Figure 4.5 (a) shows the simulation waveforms of the voltage across the capacitor C_1 (V_{C1}) and the input voltage (V_{dc}). The simulated line-to-line (V_{LL}) and phase (V_{ph}) output voltages are plotted in Figure 4.5 (b). A high-quality sinusoidal line current is depicted in Figure 4.5 (c). Obviously, the capacitor voltage (V_{C1}) is not boosted and maintained at 80 V by the dc source.

In the second test, the modulation index was kept at 0.8 while the ST duty ratio was set to 0.2. Figure 4.6 shows the simulated boosted waveforms, the dc-link voltage has been boosted to around 133 V according to the equations (3.13)-(3.14) and plotted in Figure 4.6(a). In addition, the line, the phase voltages are shown in Figure 4.6 (b). The line current is also observed to have been boosted as shown in Figure 4.6 (c)

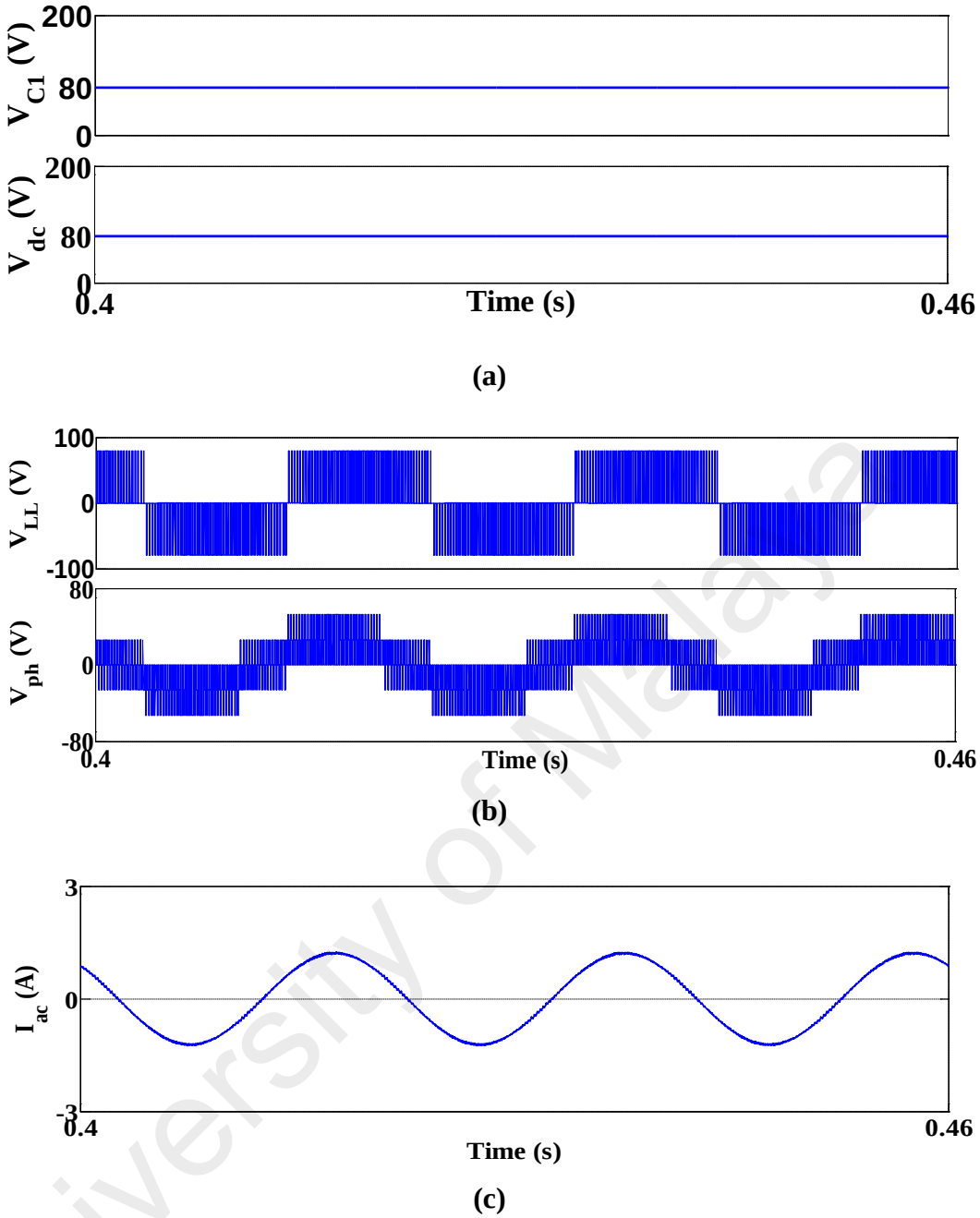
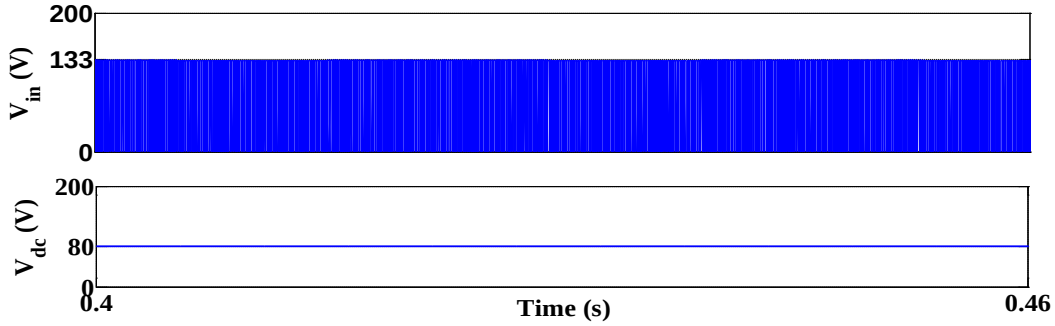
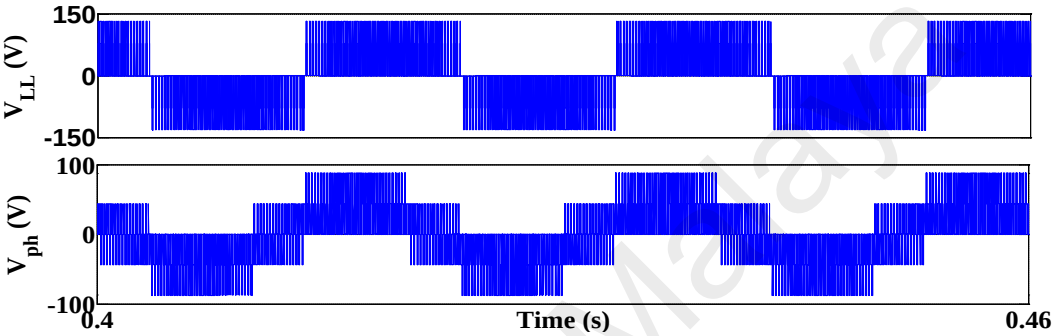


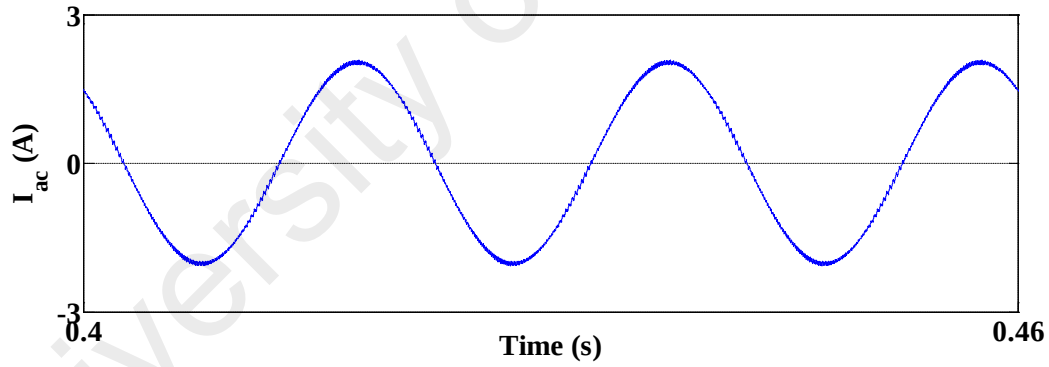
Figure 4.5: Simulation waveforms for M = 0.8 and D = 0 using the ODZSI. **(a)** V_{c1} (top) and V_{dc} (bottom); **(b)** the inverter V_{LL} (top) and V_{ph} (bottom); **(c)** the load current I_{ac}.



(a)



(b)



(c)`

Figure 4.6: Simulation waveforms for M = 0.8, D = 0.2 using the ODZSI. **(a)** V_{in} (top) and V_{dc} (bottom); **(b)** the inverter V_{LL} (top) and V_{ph} (bottom); **(c)** the load current I_{ac}.

Figure **4.7** shows the simulation waveform of inductor current I_{L1}, V_{dc}, V_{in}, and the six switches signal gates (S_1~S_6) within two (2) control cycles for M=0.8 and V_{dc}=80 V. It is obvious that V_{in} becomes zero when the ST is inserted. As mentioned previously, the four (4) times of ST behaviors per control cycle are achieved by the ODZSI where only two

switches of the same leg are involved to produce the ST, whereas the switches of the other phase-leg (S_3 , S_4) are working complimentary. It can be seen that the controller manages to generate the appropriate switching gate signals that lead the inverter to output the desired waveform.

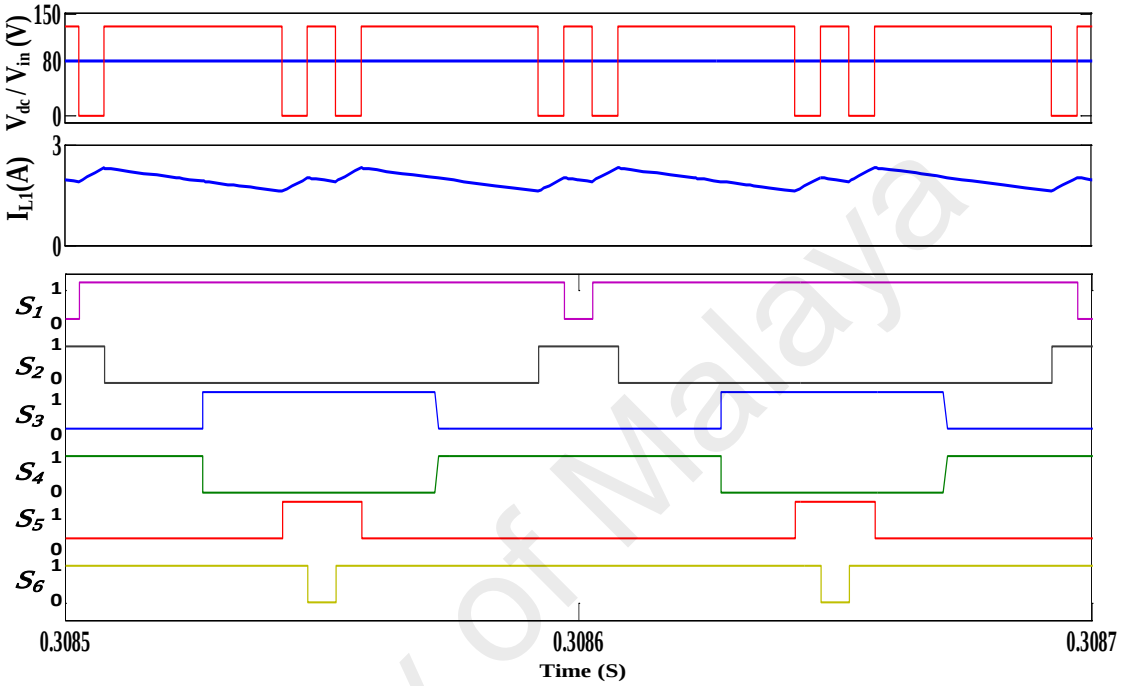
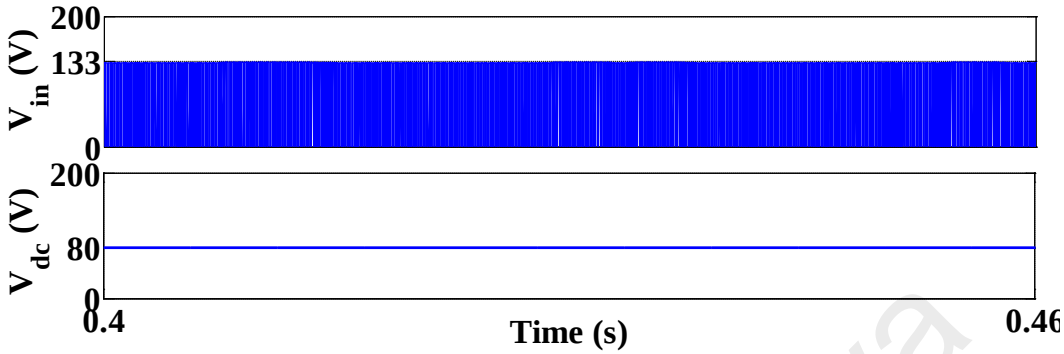


Figure 4.7: Simulation of the V_{dc} and V_{in} voltages; the inductor current I_{L1} and the gate signals (*S1~S6*) generated by ODZSI within two control cycles.

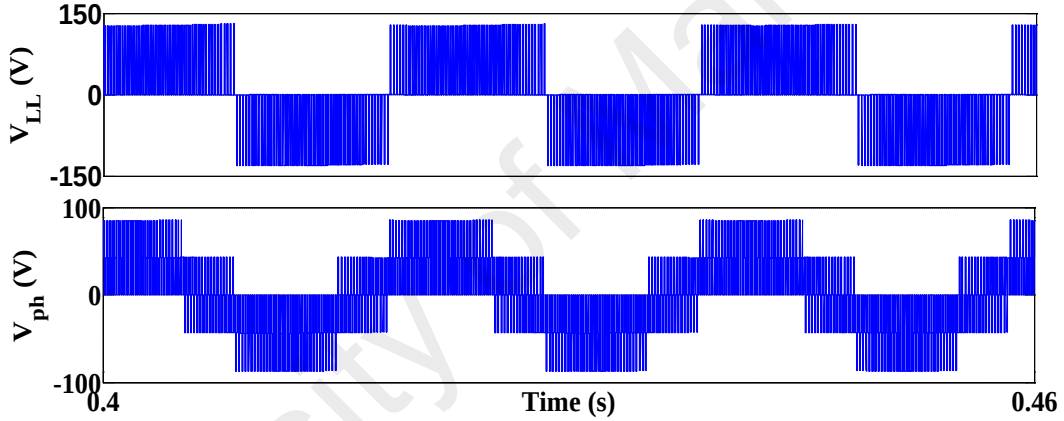
To investigate the improved performance of the proposed control algorithm for qZSI over the modified space vector strategy, simulation using MSVPWM control was carried out using the same parameters as those of ODZSI (M = 0.8 and D = 0.2). The results are shown in Figure 4.8.

The simulation waveforms of the inverter dc-link and the input voltages are depicted in Figure 4.8 (a). Moreover, Figure 4.8 (b) shows the simulation waveforms of the inverter line-to-line voltage V_{LL} (top) and V_{ph} (bottom), the load current I_{ac} is plotted in Figure 4.8 (c).

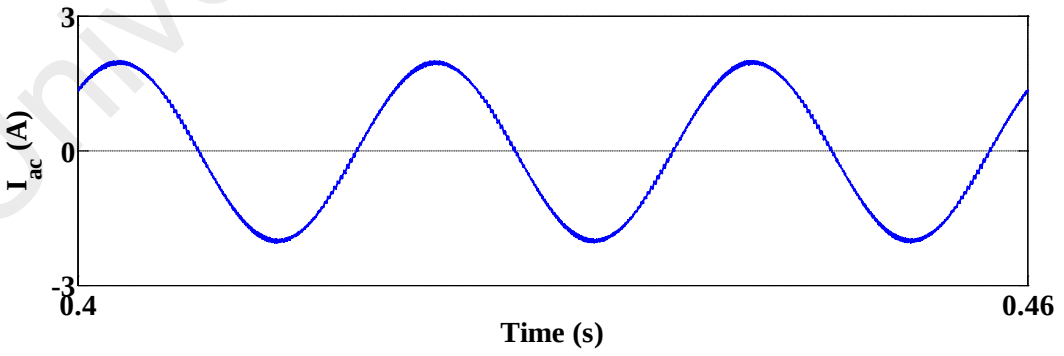
The simulation results show that the proposed control scheme is able to boost the output voltage same as the modified space vector strategy with less computation time.



(a)



(b)



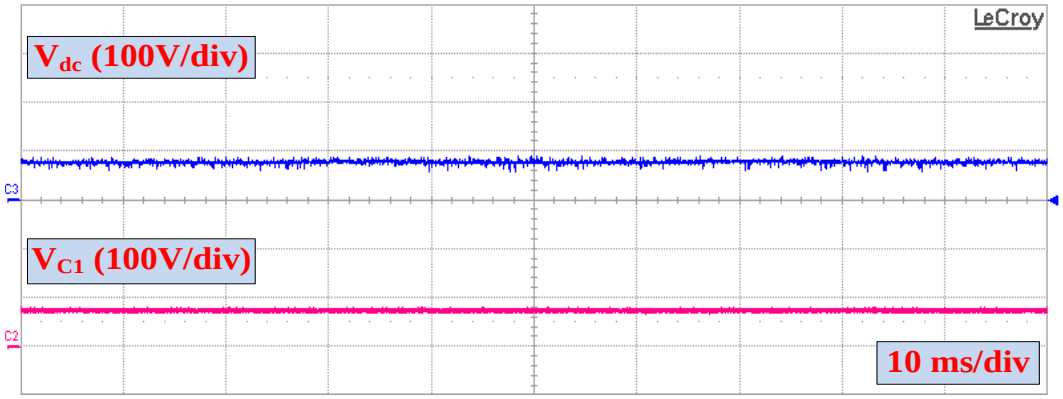
(c)

Figure 4.8: Simulation waveforms for M = 0.8 and D = 0.2 using the MSVPWM. **(a)** V_{in} (top) and V_{dc} (bottom); **(b)** the V_{LL} (top) and V_{ph} (bottom); **(c)** the load current I_{ac}.

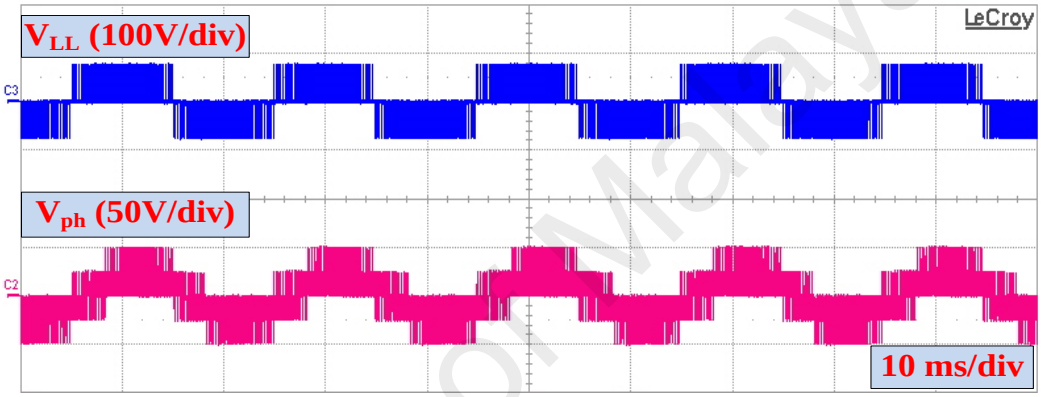
The experimental results obtained under the same operation parameters and the same laboratory prototype as in the simulation for the non-boost and boost cases are illustrated in Figure 4.9 and Figure 4.10 respectively.

For the non-boost case, the modulation is 0.8, and the shoot-through duty ratio was set to 0. From Figure 4.9 (a), the capacitor voltage (V_{C1}) is not boosted and maintained at around 80 V by the dc source as expected. The line and phase voltages are plotted in Figure 4.9 (b), and the load current is shown in Figure 4.9 (c).

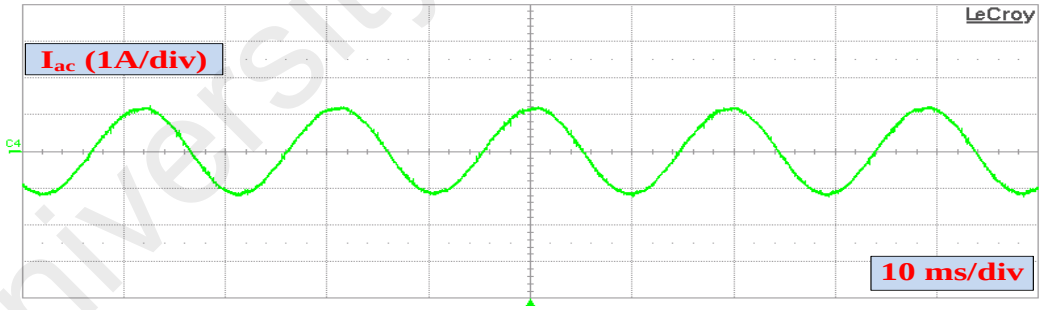
In the second test, a modulation index and shoot-through duty ratio of 0.8 and 0.2 were used respectively. The dc-link voltage is boosted to around 130 V as shown in Figure 4.10 (a), the Figure 4.10 (b) and Figure 4.10 (c) show the boosted voltages and current waveforms respectively.



(a)

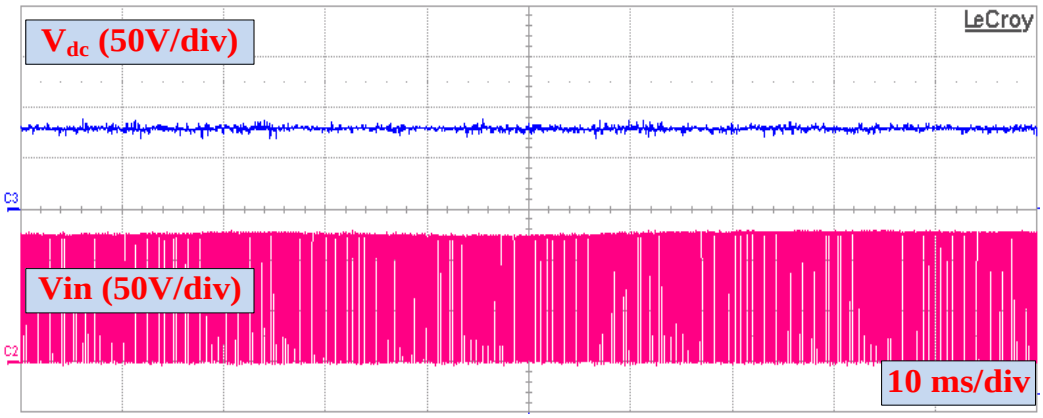


(b)

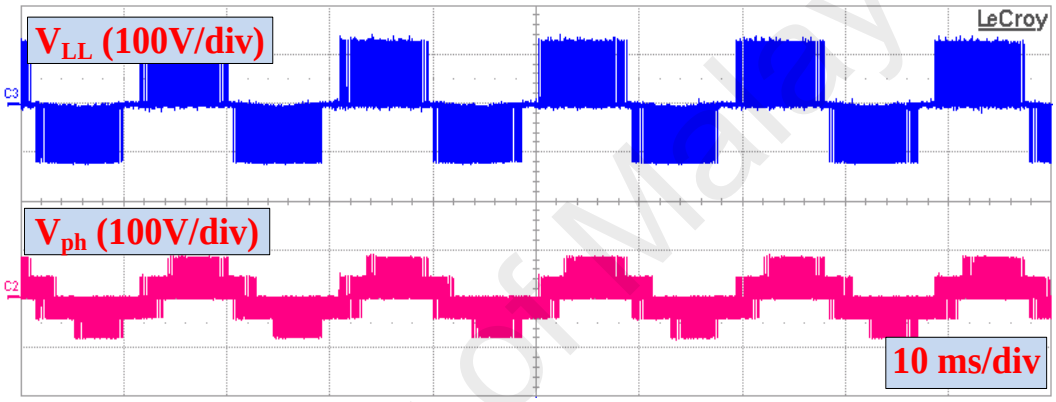


(c)

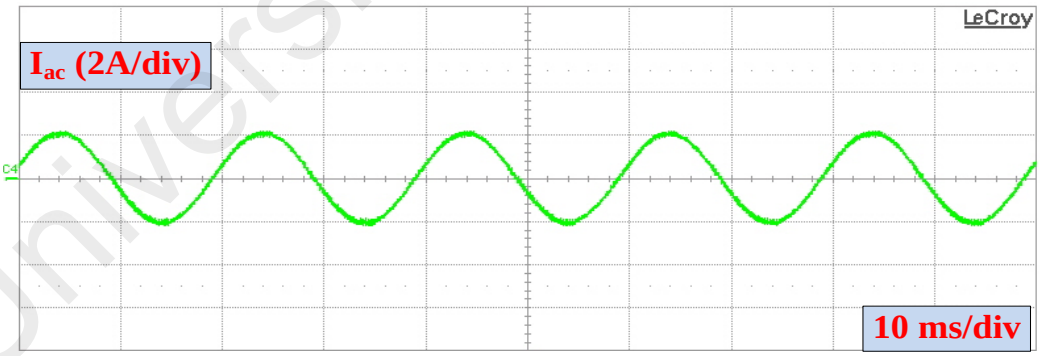
Figure 4.9: Experimental waveforms for M = 0.8 and D = 0 using the ODZSI. **(a)** V_{dc} (top) and V_{c1} (bottom); **(b)** the V_{LL} (top) and V_{ph} (bottom); **(c)** the load current I_{ac}.



(a)



(b)



(c)

Figure 4.10: Experimental waveforms for M = 0.8 and D = 0,2 using the ODZSI. **(a)** V_{dc} (top) and V_{in} (bottom); **(b)** the inverter V_{LL} (top) and V_{ph} (bottom); **(c)** the load current I_{ac}.

Figure 4.11 illustrates the inverter voltage input (V_{dc}), the voltage dc-link (V_{in}), and the inductor current (I_{L1}) during one control cycle ($1e^{-4}$ s) using the ODZSI technique.

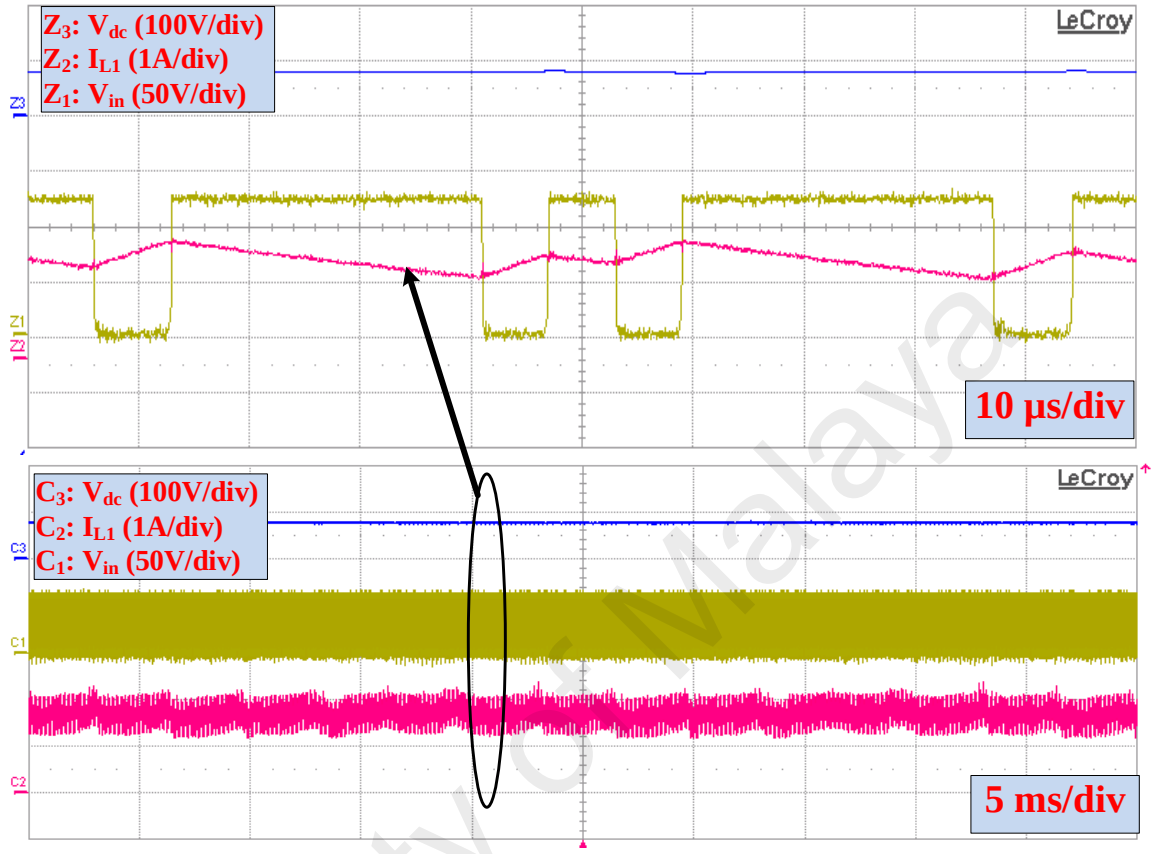


Figure 4.11: V_{dc}, V_{in} and I_{L1} during one control cycle.

The experimental results that correspond with the results attained from the simulation have clearly shown the reliability and compatibility of the ODZSI in generating the appropriate switching pules that make the inverter outputs the desired voltages.

4.4 The experimental verification of the proposed ODZSI-MBC _1

The aim of this test is to investigate the performance of the proposed control algorithm in section 0 under different input voltages to obtain the same output phase-voltage of approximately 100 V ($\hat{V}_{ph}$ =100V) using a laboratory prototype shown in Figure 4.12 . The three-phase qZSI hardware is built using the following parameters: C_1=C_2= 1.2 mF, L_1=L_2=3.2 mH, switching frequency F_{sw} = 10 kHz, a balanced RL load comprising a three-phase 25 Ω resistor and three-phase 23 mH inductor was used in this study.

Matlab/Simulink simulation results with modulation index M = 0.8, and M = 1.1 are plotted in Figure 4.13 and Figure 4.14 where their corresponding input voltages V_{dc} are 81 V and 149 V, respectively.

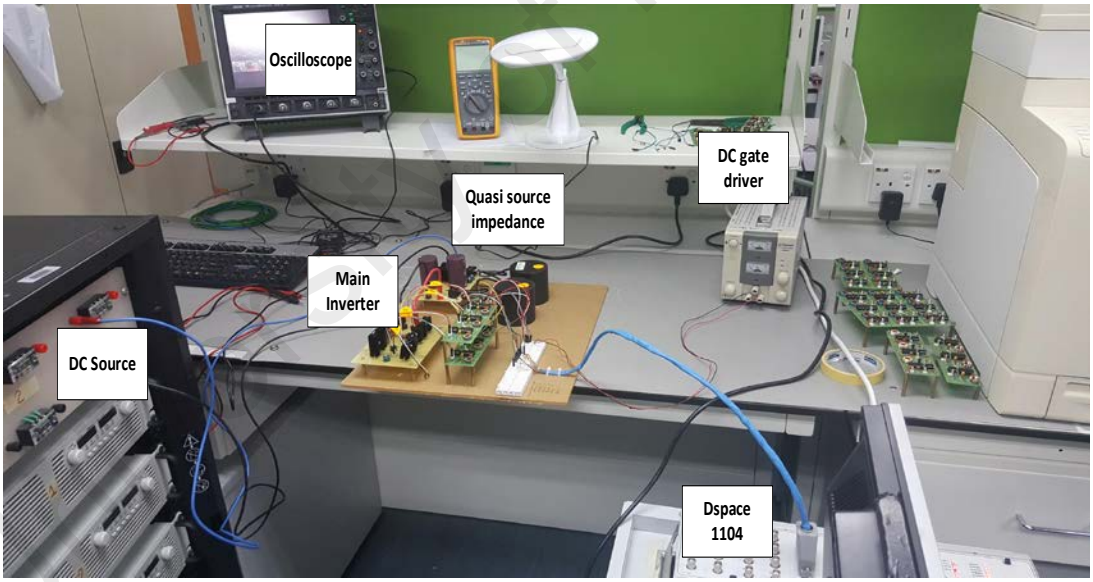
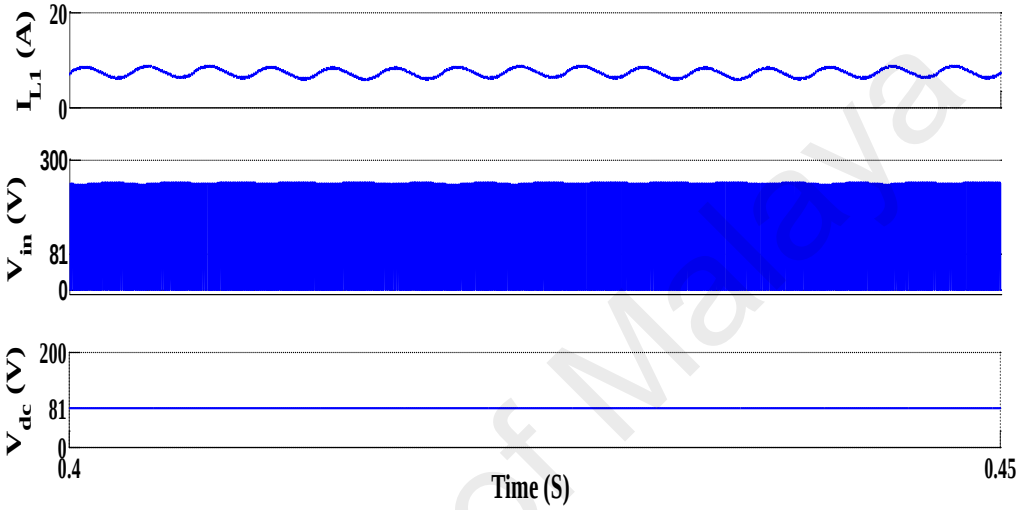
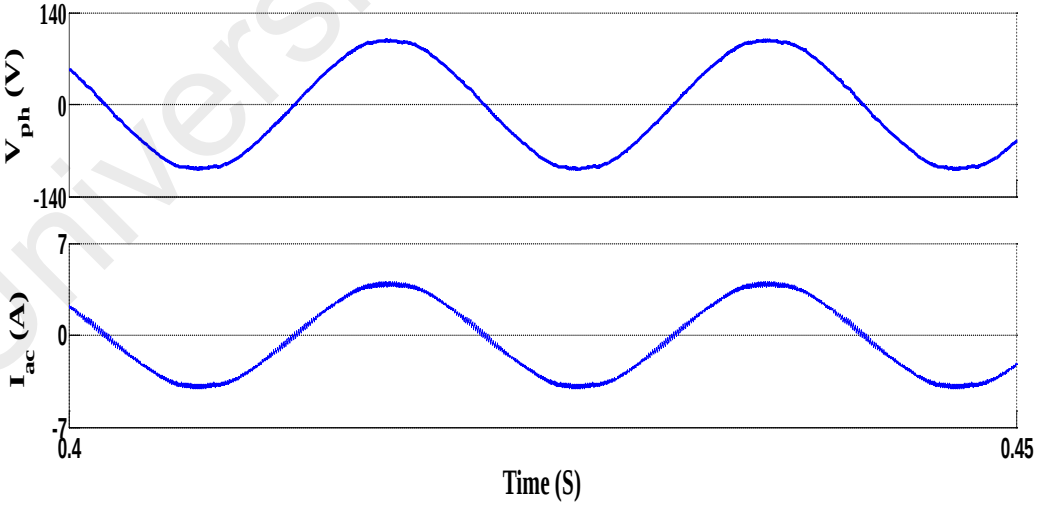


Figure 4.12: Quasi-ZSI prototype.

The simulation waveforms of the inductor current (I_{L1}), the inverter dc-link (V_{in}) and the input (V_{dc}) voltages are depicted in Figure 4.13 (a) and Figure 4.14 (a), where their corresponding modulation index values are M = 0.8 and M = 1.1, respectively. Moreover, Figure 4.13 (b) and Figure 4.14 (b) show the simulation waveforms of the inverter phase voltage V_{ph} (top) and the load current I_{ac} (bottom).

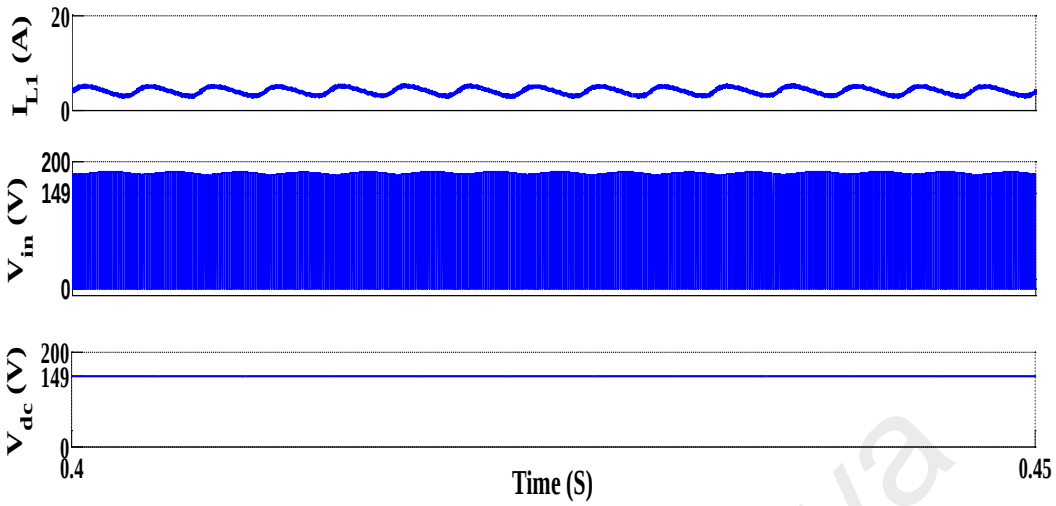


(a)

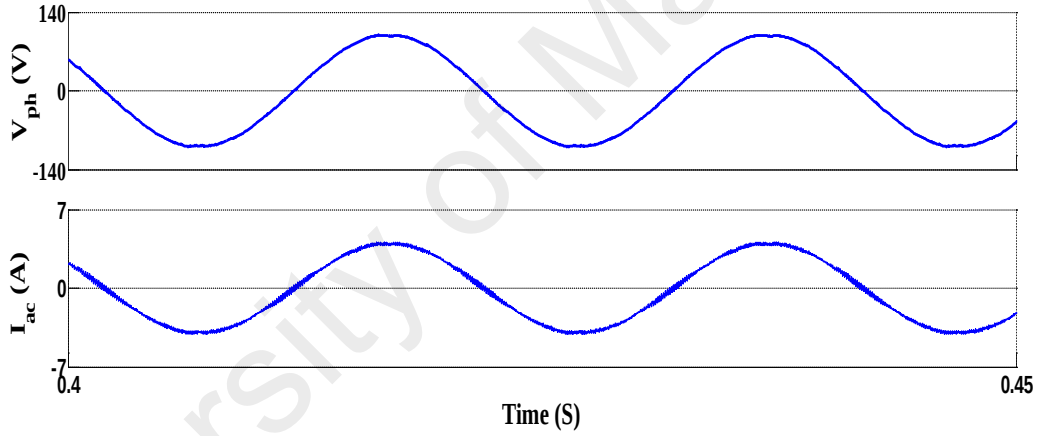


(b)

Figure 4.13: Simulation waveforms for M = 0.8**: (a)** I_{L1} (top), V_{in} (middle) and V_{dc} (bottom); **(b)** the inverter V_{ph} (top) and I_{ac} (bottom).



(a)



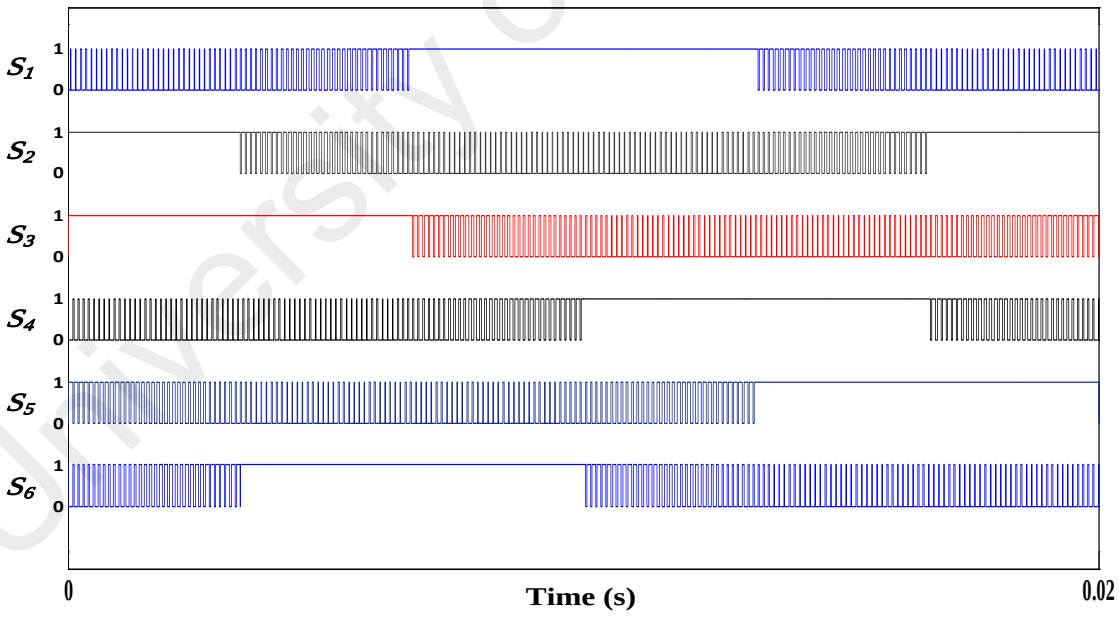
(b)

Figure 4.14: Simulation waveforms for M = 1.1**: (a)** I_{L1} (top), V_{in} (middle) and V_{dc} (bottom); **(b)** the inverter V_{ph} (top) and I_{ac} (bottom).

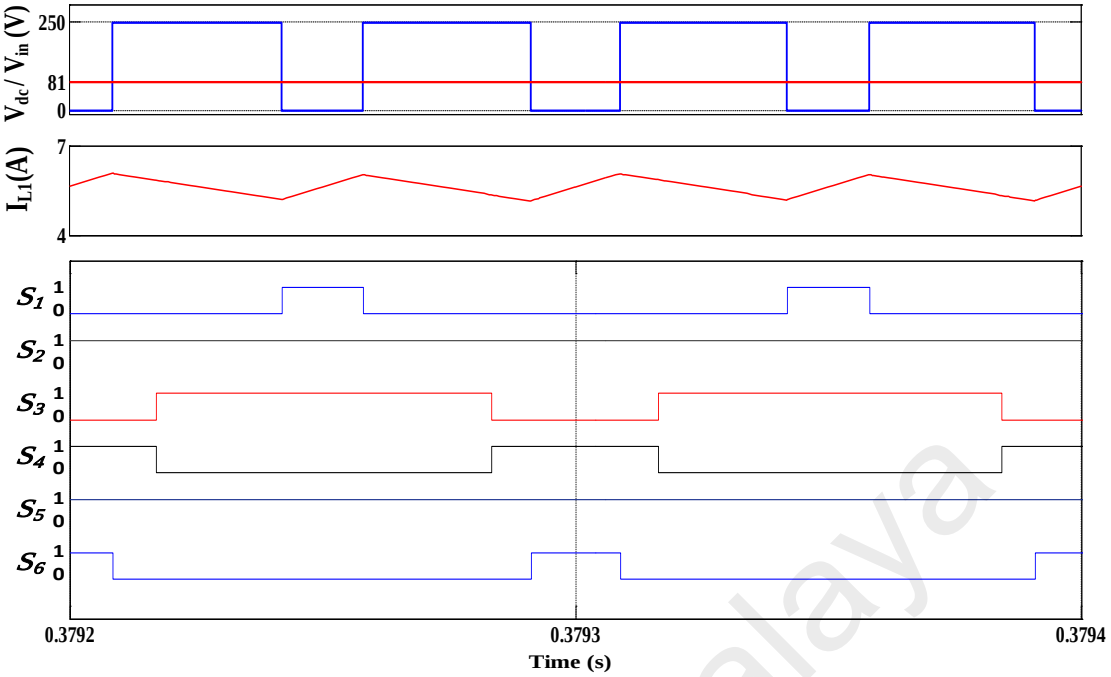
For V_{dc}= 81 V and M=0.8, based on Equations (3.13) and (3.28); the boosting factor B = 3.09 and the theoretical dc-link pick voltage is 250.6 V. Similarly, for V_{dc} = 149 V; B = 0.548 and the $\hat{V}_{in}$ would be 181.7 V as shown in Figure 4.13 and Figure 4.14. The increasing of M leads to decrease of the dc voltage across the inverter bridge because the corresponding gain G gets smaller. In the other word, the gain and M are inversely

proportional. The simulation results in Figure 4.13 and Figure 4.14 are quite consistent with the theoretical analysis, which verifies the above analysis and the control concept.

Figure 4.15 (a) shows the gate signals (S_1~S_6) within one cycle of the fundamental output frequency; the simulation waveform of V_{dc}, V_{in} , the inductor current I_{L1} and the gate signals (S_1~ S_6) within two (2) control cycles (2e^{-4} s) for M=0.8 and V_{dc}=81V are plotted in Figure 4.15 (b) . It can be clearly seen that V_{in} becomes zero when the ST is inserted. As mentioned previously, the three times of ST behaviors per control cycle are achieved by the ODZSI-MBC_1 where only two switches of the same leg are involved to produce the ST, i.e. S_5 and S_6 in the beginning and the end, and S_1 and S_2 in the middle of the control cycle, whereas S_3 and S_4 are working commentary. It can be clearly seen that the controller generates the appropriate switching gate signals to achieve the desired output waveform.



(a)

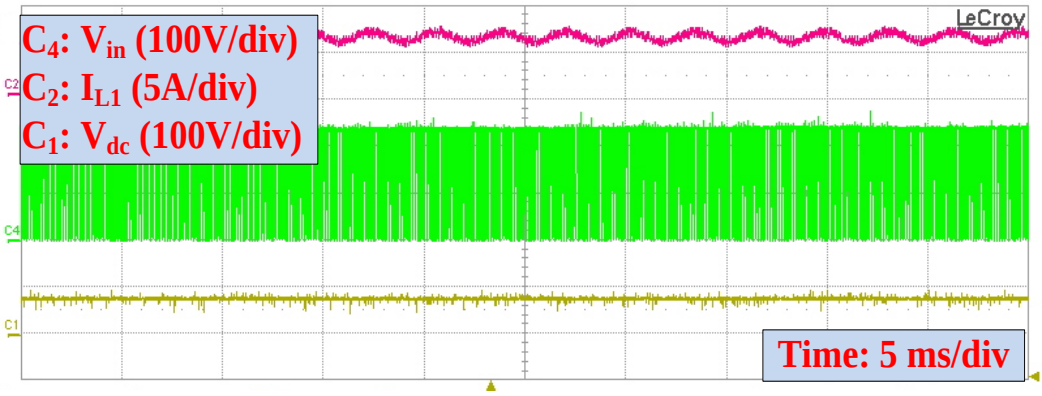


(b)

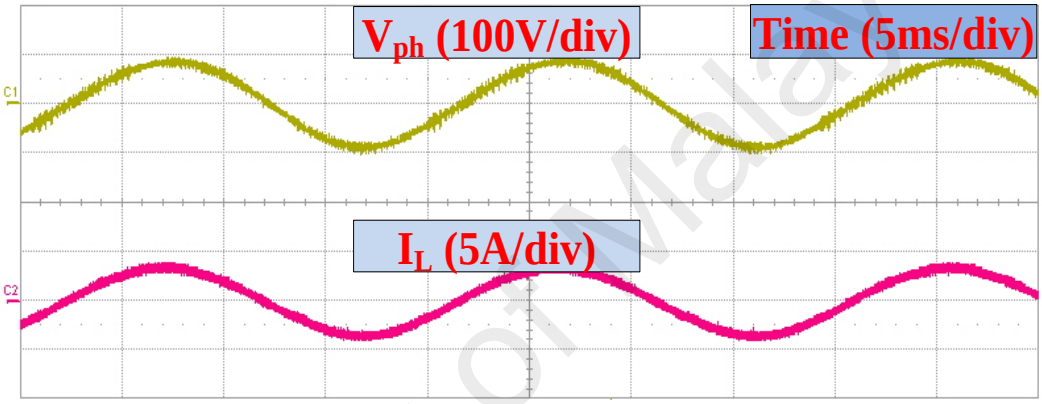
Figure 4.15: (a) gate signals (S_1~S_6)**; (b)** Simulation of zoomed V_{dc}, V_{in}, I_{L1} and the gate signals generated by the ODZSI-MBC_1 within two control cycles.

The obtained experimental results under the same operation parameters and the same laboratory prototype as in the simulation are illustrated in Figure 4.16 and Figure 4.17 at different modulation index values M = 0.8 and M=1.1 respectively. The waveform of the inductor current I_{L1} (top), the dc-link across the main bridge V_{in} (middle) and the dc source voltage V_{dc} (bottom) are plotted in part (a) of Figure 4.16 and Figure 4.17 ; the ac output voltage V_{ph} (top) and the ac output current I_{ac} (bottom) are illustrated in part (b) of Figure 4.16 and Figure 4.17; and the THD of the load current captured via YOKOGAWA WT 1800 precision power analyzer is depicted in part (c) of Figure 4.16 and Figure 4.17.

Moreover, the simulation and experimental results are identical, which validate the performance of the proposed control scheme. As mentioned earlier, the variation in the ST duty ratio will result in ripple in the inductor current (6ω) as shown in part (a) of Figures 4.16 and 4.17.



(a)



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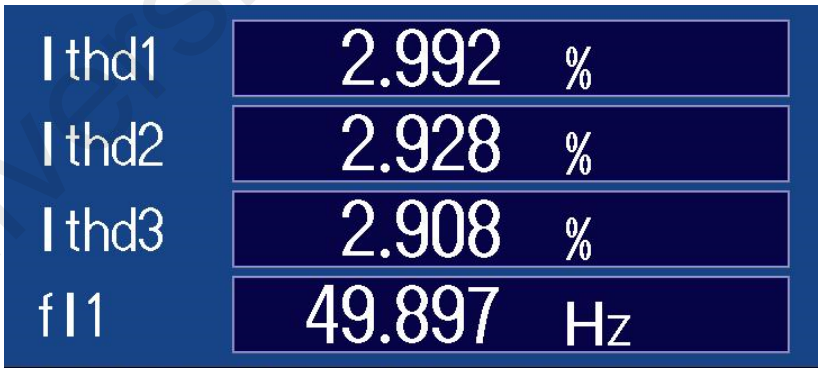
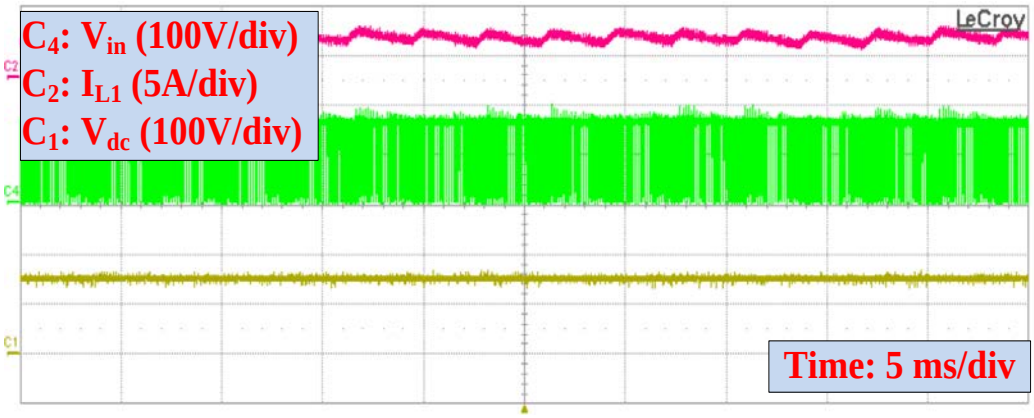
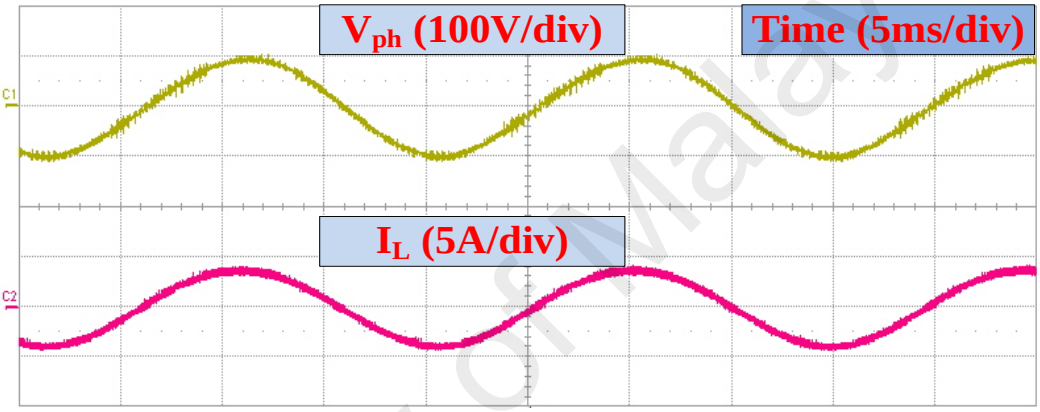


(c)

Figure 4.16: Experimental waveforms for M = 0.8: **(a)** I_{L1} (top), V_{in} (middle) and V_{dc} (bottom); **(b)** the phase voltage V_{ph} (top) and I_{ac} (bottom); and **(c)** the THD current.



(a)



(b)

(c)

Figure 4.17: Experimental waveforms for M = 1.1: **(a)** I_{L1} (top), V_{in} (middle), V_{dc} (bottom); **(b)** the phase voltage V_{ph} (top) and I_{ac} (bottom); and **(c)** the THD current.

The figures show that the output voltage is kept nearly constant regardless of the wide varying range of the input voltage and the output voltage agrees with the analysis and simulation results very well. A lower input voltage requires a greater boost factor *B*, and smaller modulation index.

Figure 4.18 illustrates the experimental results of the inverter input voltage (V_{dc}), the dc-link voltage (V_{in}), and the inductor current (I_{L1}) during two (2) control cycles ($2e^{-4}$ s) using the ODZSI-MBC_1 technique. It is observed that the inductor current is increasing during the ST while the V_{in} becomes zero.

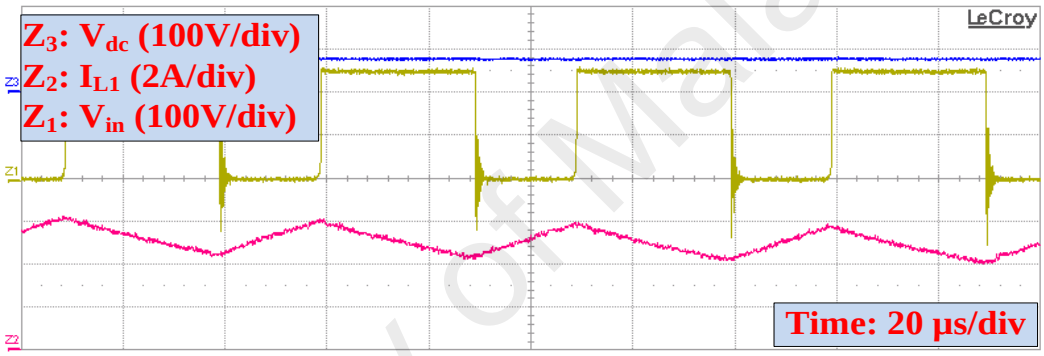


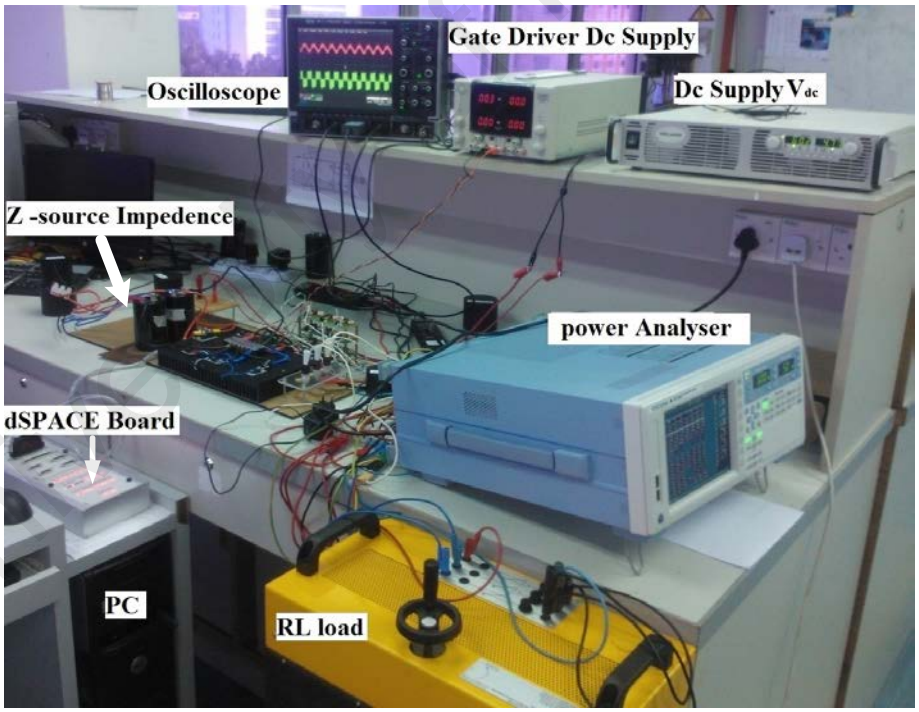
Figure 4.18: V_{dc}, V_{in} and I_{L1} during two (2) control cycles.

The experimental results that correspond with the results attained from the simulation have clearly shown the reliability and compatibility of ODZSI-MBC_1 in generating the appropriate switching pules that make the inverter outputs the desired voltages.

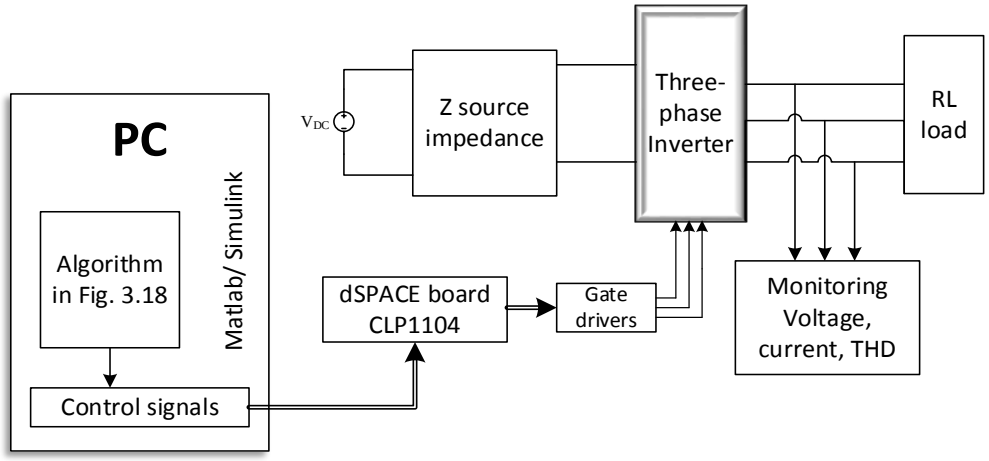
4.5 The experimental verification of the proposed ODZSI-MBC_3

As mentioned earlier, the insertion of the ST state is not unique. However, in order to reduce the rating of the switches' current, all three legs are involved to produce the ST. The aim of this test is to investigate the performance of the proposed control algorithm in section 3.3.5 under different input voltages to obtain the same output line-to -line voltage of around 60 V (RMS) using a laboratory prototype shown in Figure 4.19.

The ODZSI-MBC_3 is compared with the proposed control in (Fang Zheng Peng et al., 2005) since they have the same principal i.e. truing ON all the switches during the zero vector to produce the ST. The three-phase ZSI hardware is built using the parameters summarized in Table 4.2.



(a)



(b)

Figure 4.19: (a) Hardware prototype, **(b)** Control block diagram.

Table 4.2: Simulation model parameters of the ZSI.

Parameters	Value
Desired output line-to-line voltage V_{LL} (rms)	60 V
Z-source inductance (L_1 and L_2)	1mH
Z-source capacitance ($C_1$and C_2)	1.2mF
Switching frequency	10 kHz
ac load inductance	1.3mH
ac load resistance	9.3 Ω

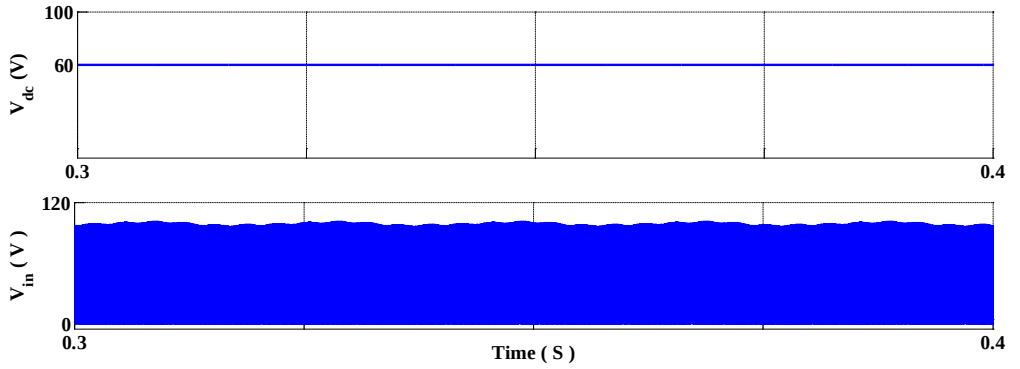
The simulation results with modulation index values M = 0.9, M = 1.1 and M = 1.15 are plotted in Figure 4.20, Figure 4.21 and Figure 4.22 where the corresponding input dc voltage source (V_{dc}) are 60, 72 and 76.5 V, respectively.

The simulation waveforms of the inverter dc-link (V_{in}) and the V_{dc} are depicted in Figure 4.20 (a), Figure 4.21(a), and Figure 4.22(a) where the corresponding modulation index values are M= 0.9, M = 1.1 and M = 1.15, respectively. Moreover, Figure 4.20 (b), Figure 4.21(b), and Figure 4.22(b) show the simulation waveforms of the inverter line-to-line V_{LL} (top) and phase V_{ph} (bottom) voltages and the Figure 4.20 (c), Figure 4.21(c), and

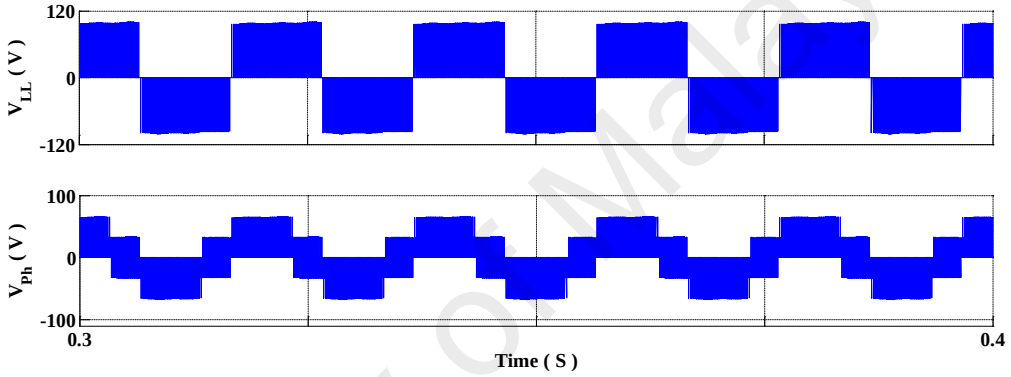
Figure 4.22(c) shows the output line current I_L. Based on the equations (3.13) (3.16) and (3.28) It can be clearly seen that the controller manages to generate the appropriate switching gate signals that lead the inverter to output the desired waveform. The obtained results are summarized in Table 4.3.

Table 4.3: Summary of obtained experimental results under different conditions

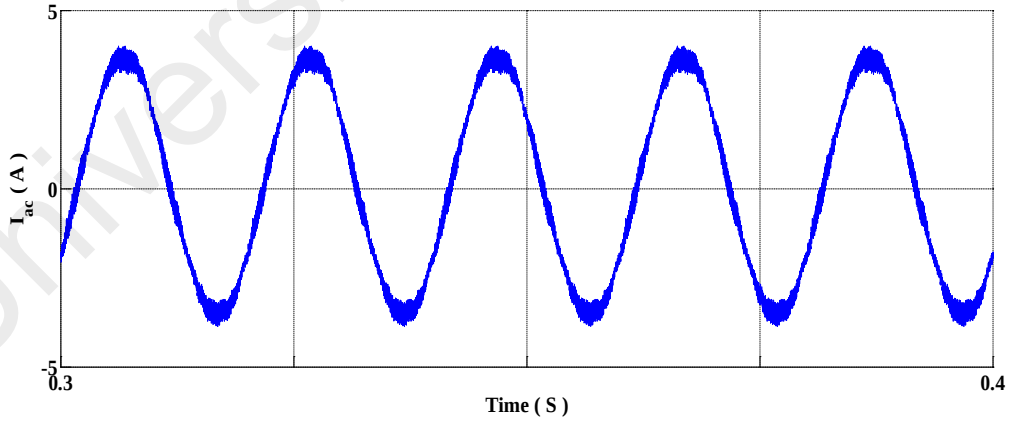
V_{dc}	M	V_{LL} (rms) (V)
60	0.9	60.78
72	1.1	59.45
76.5	1.15	59.93



(a)

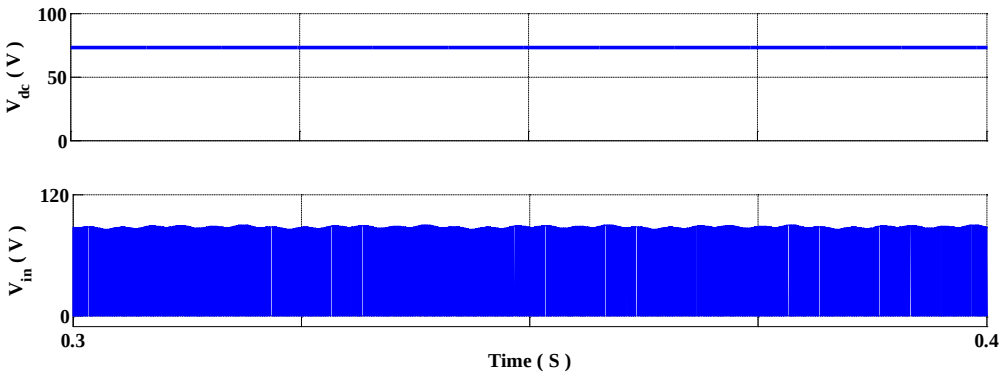


(b)

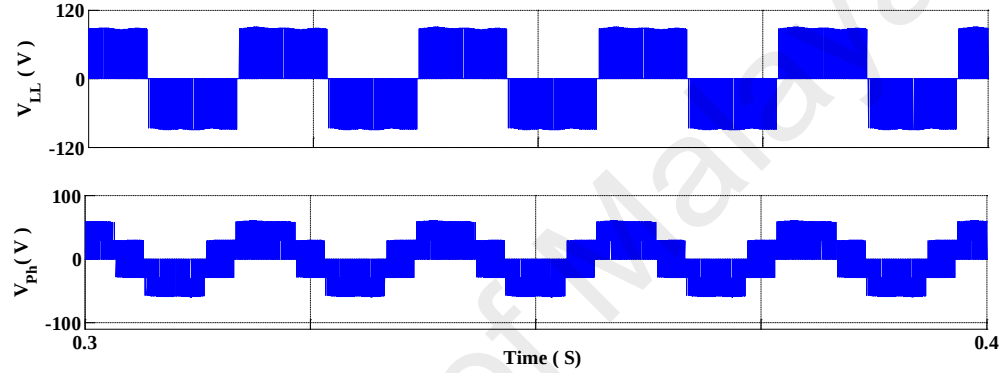


(c)

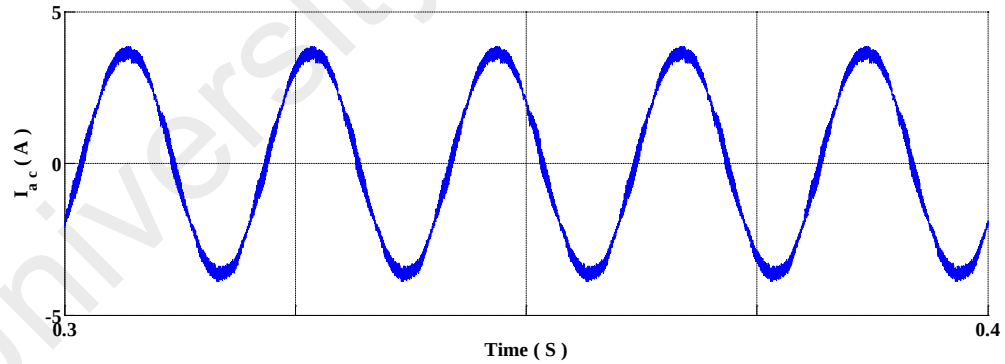
Figure 4.20: Simulation waveforms for M = 0.9 and V_{dc} = 60 V: **(a)** V_{dc} (top) and V_{in} (bottom); **(b)** the V_{LL} (top) and V_{Ph} (bottom) voltages; and **(c)** I_{ac}.



(a)

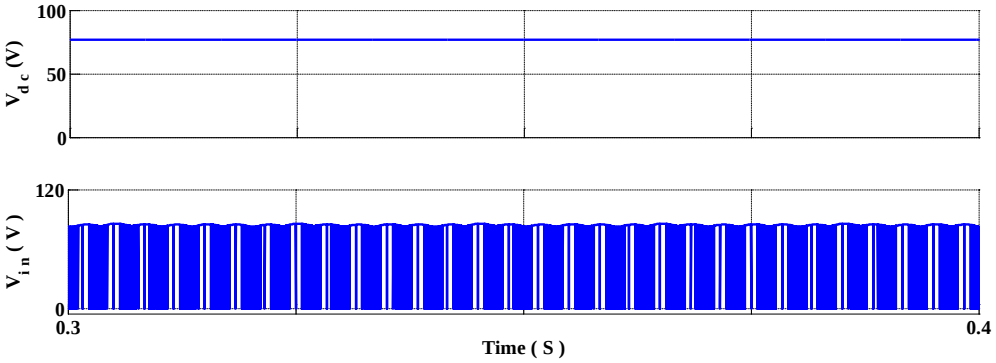


(b)

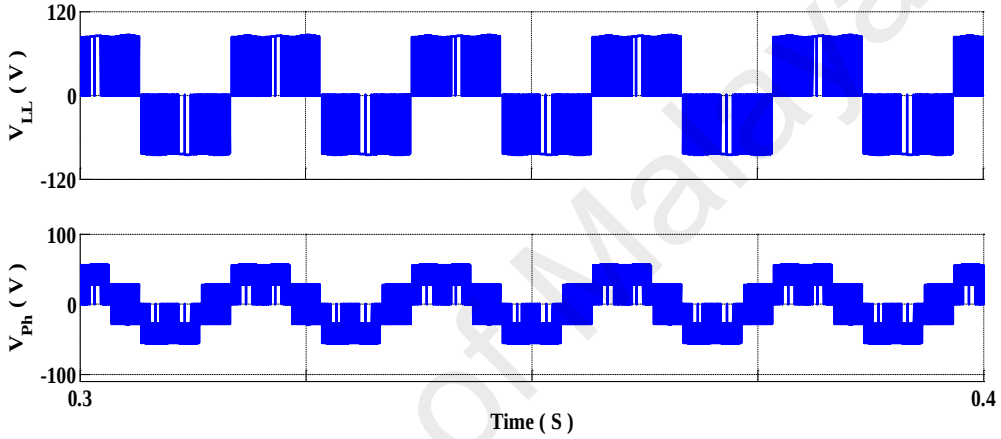


(c)

Figure 4.21: Simulation waveforms for M = 1.1 and V_{dc} = 72 V: **(a)** V_{dc} (top) and V_{in} (bottom); **(b)** the V_{LL} (top) and V_{Ph} (bottom) voltages; and **(c)** I_{ac}.



(a)



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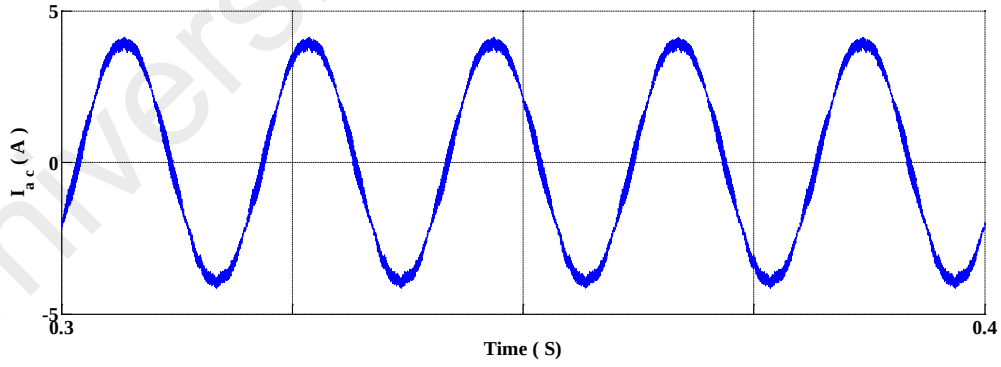
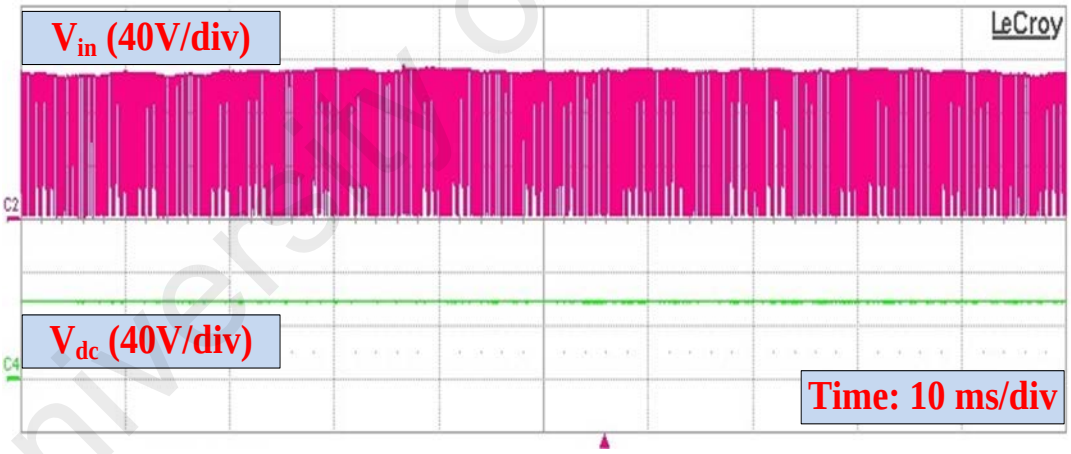


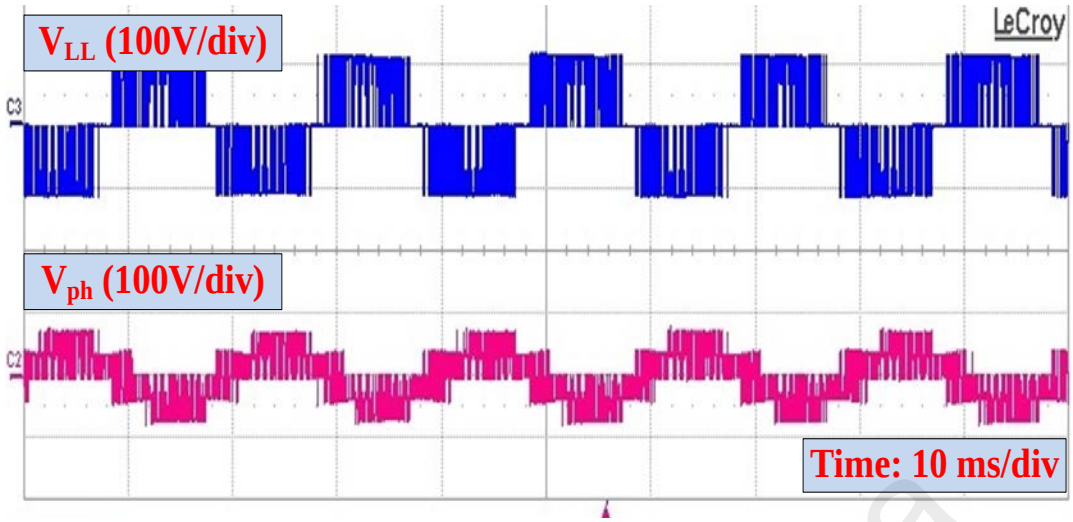
(c)

Figure 4.22: Simulation waveforms for M = 1.15 and V_{dc} = 76.5 V: **(a)** V_{dc} (top) and V_{in} (bottom); **(b)** the V_{LL} (top) and V_{Ph} (bottom) voltages; and **(c)** I_{ac}.

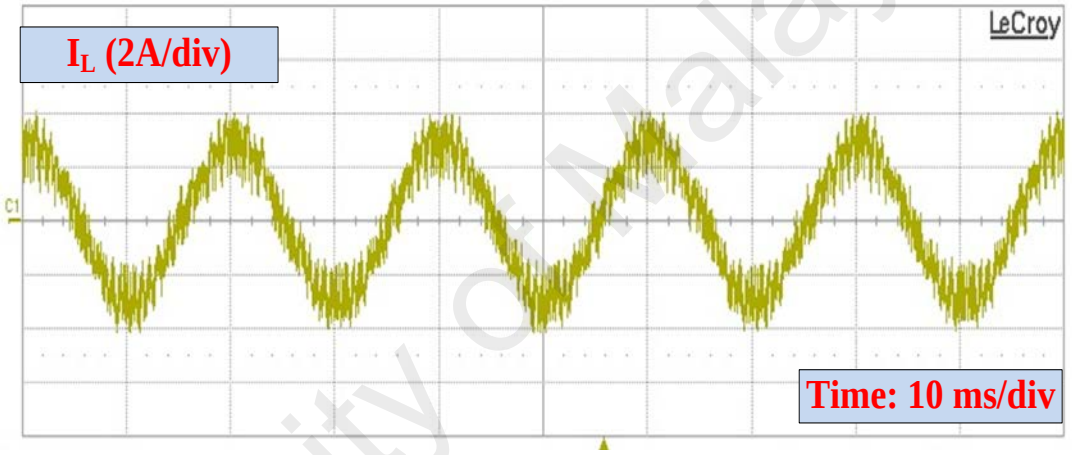
The experimental results obtained under the same operation parameters and the same laboratory prototype as in the simulation are illustrated in Figure 4.23, Figure 4.24, and Figure 4.25 at different modulation index values M = 0.9, M =1.1 and M = 1.15, respectively. The waveforms of V_{in} (top) and V_{dc} (bottom) are plotted in part (a) of Figure 4.23, Figure 4.24, and Figure 4.25; the ac output V_{LL} voltage (top) and the V_{ph} are illustrated in part (b) of Figure 4.23, Figure 4.24 and Figure 4.25, and the load current and line-to-line voltage THD spectrum, are depicted in parts (c and d) of Figure 4.23, Figure 4.24, and Figure 4.25 respectively. The THD graph contains the fundamental frequency component of approximately 60 V followed by 19 harmonics components. It is observed that there is a great matching between the proposed and conventional method. Moreover, the experimental and simulation results match very well, which verify the performance of the proposed control algorithm.



(a)



(b)



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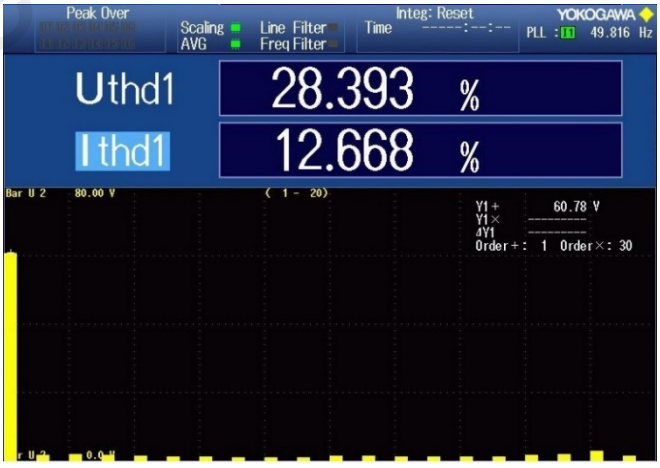
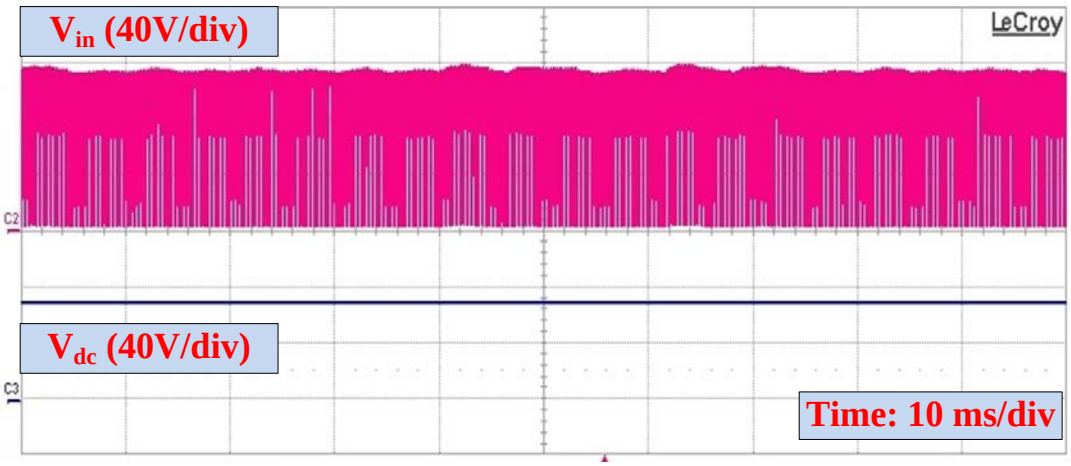


(d)

Figure 4.23 : Experimental waveforms for M= 0.9 and V_{dc} = 60 V: **(a)** V_{in} (top) and V_{dc} (bottom); **(b)** the inverter V_{LL} (top) and V_{Ph} (bottom) voltages; **(c)** I_{ac} and **(d)** the THD spectrum.



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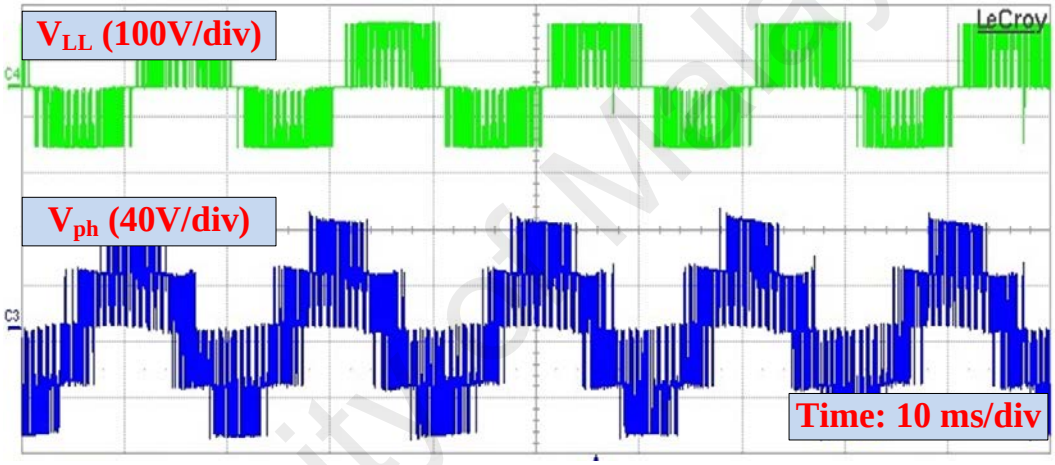

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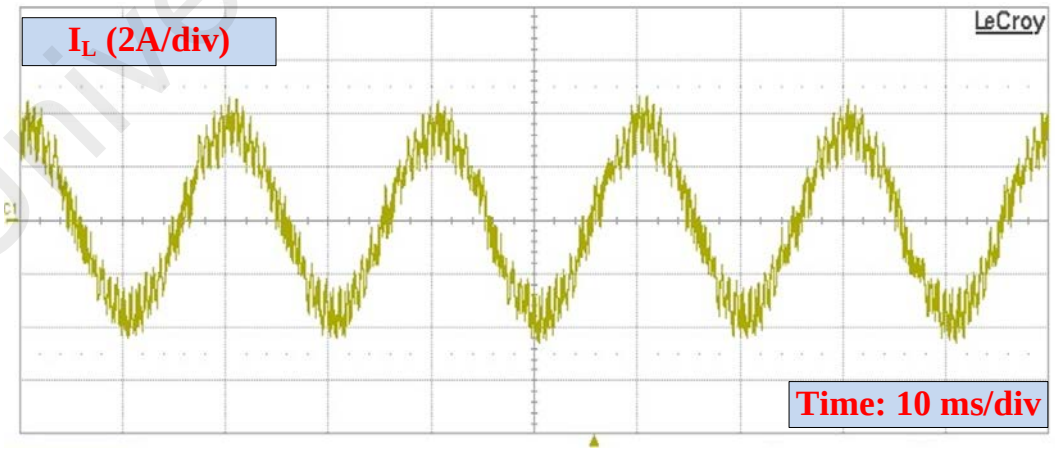
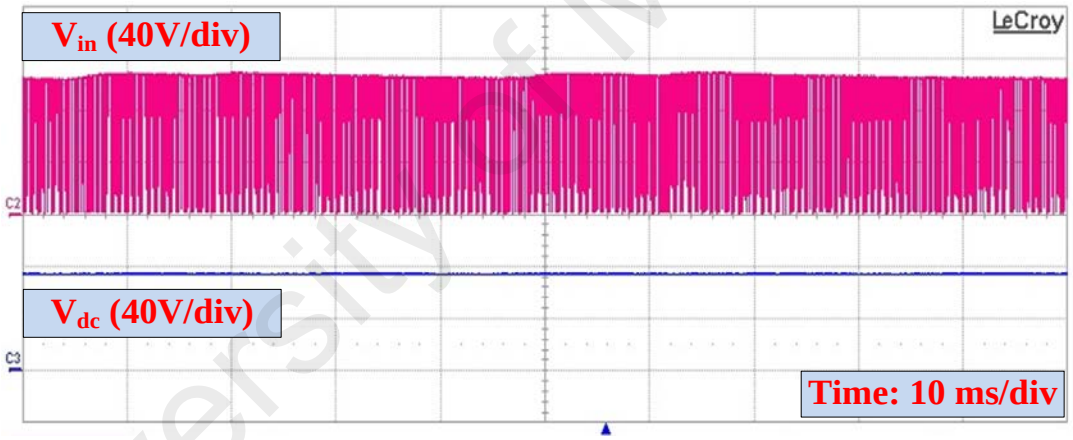


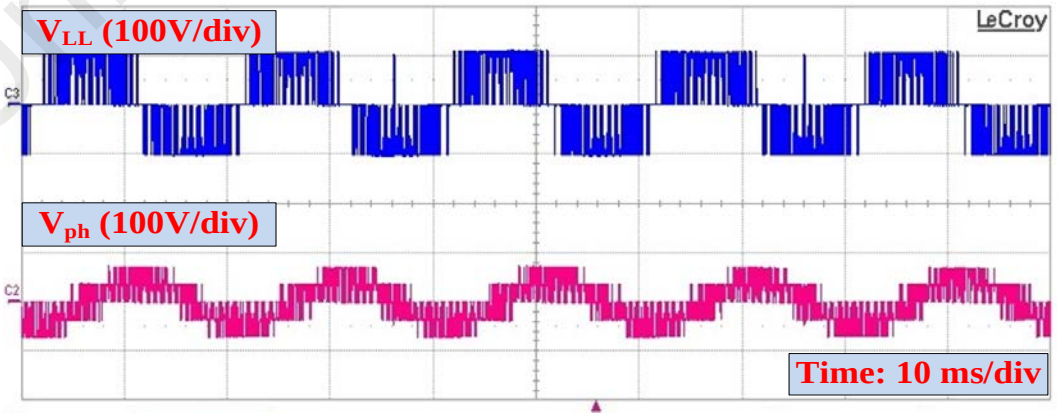
(c)

(d)

Figure 4.24: Experimental waveforms for M = 1.1 and V_{dc} = 72 V: **(a)** V_{in} (top) and V_{dc} (bottom); **(b)** the V_{LL} (top) and V_{Ph} (bottom) voltages; **(c)** I_{ac} and **(d)** the THD spectrum.



(a)



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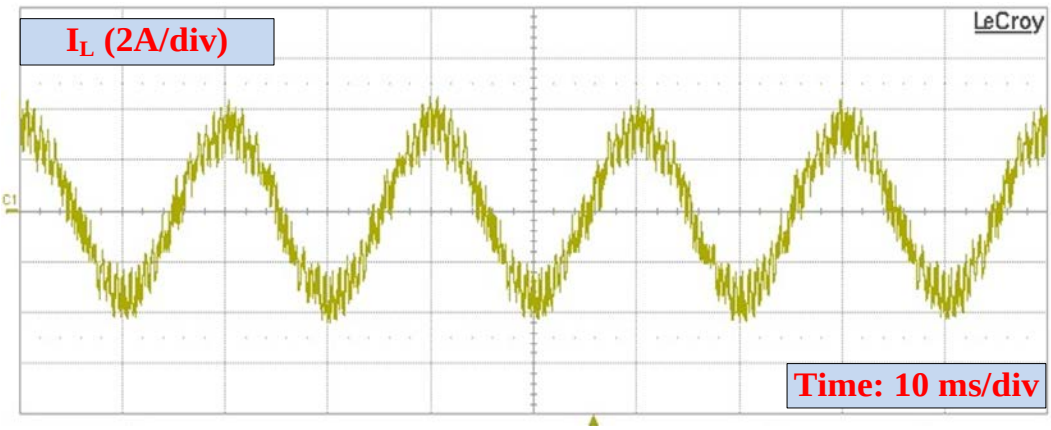

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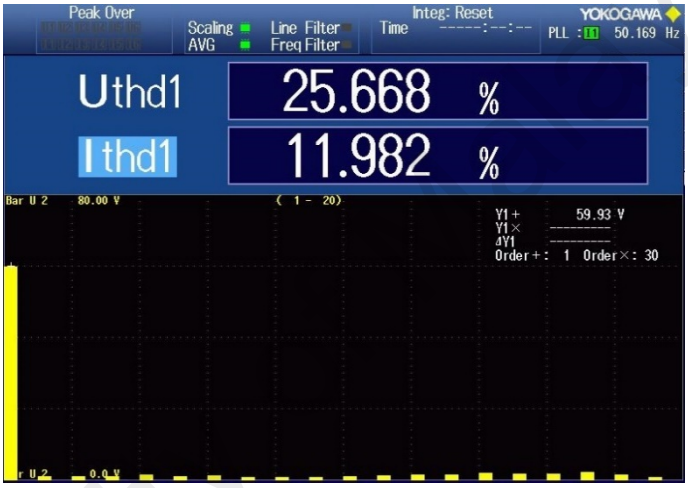


(d)

Figure 4.25 : Experimental waveforms for M = 1.15 and V_{dc} = 76.5 V: **(a)** V_{in} (top) and V_{dc} (bottom), **(b)** the V_{LL} (top) and V_{Ph} (bottom) voltages, **(c)** I_{ac} and **(d)** the THD spectrum.

The variation of THD with the modulation index for the V_{LL} voltage is depicted in Figure 4.26. This illustrates that THD is inversely proportional to the modulation index M. In other words, a lower THD in the output voltage is experienced at a higher modulation index. The graph compares the THD of the V_{LL} voltage using the ODZSI-MBC_3 and the CB-PWM proposed by (Fang Zheng Peng et al., 2005) within a range of modulation indices [0.9 –1.15]. It can be seen that the THD using ODZSI-MBC_3 is around 10% less than the conventional technique (CB-MBC) (Fang Zheng Peng et al., 2005), which enhances the output voltage quality.

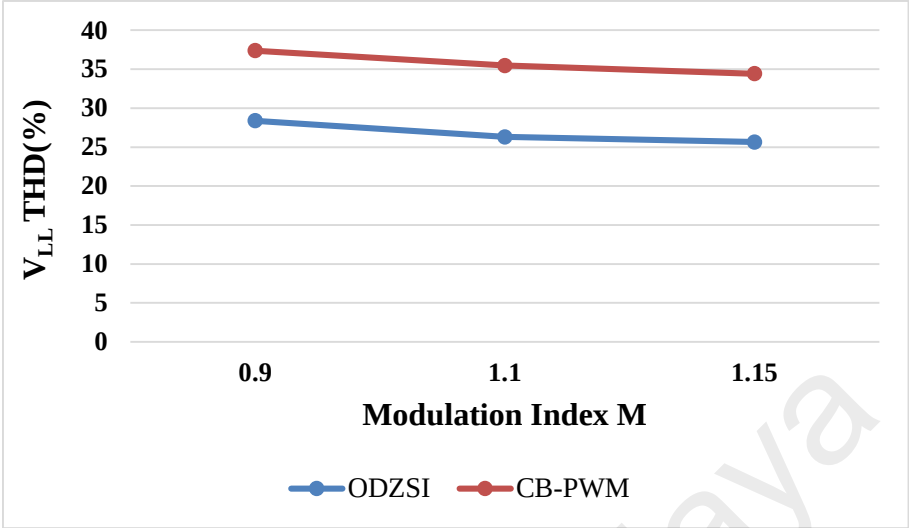
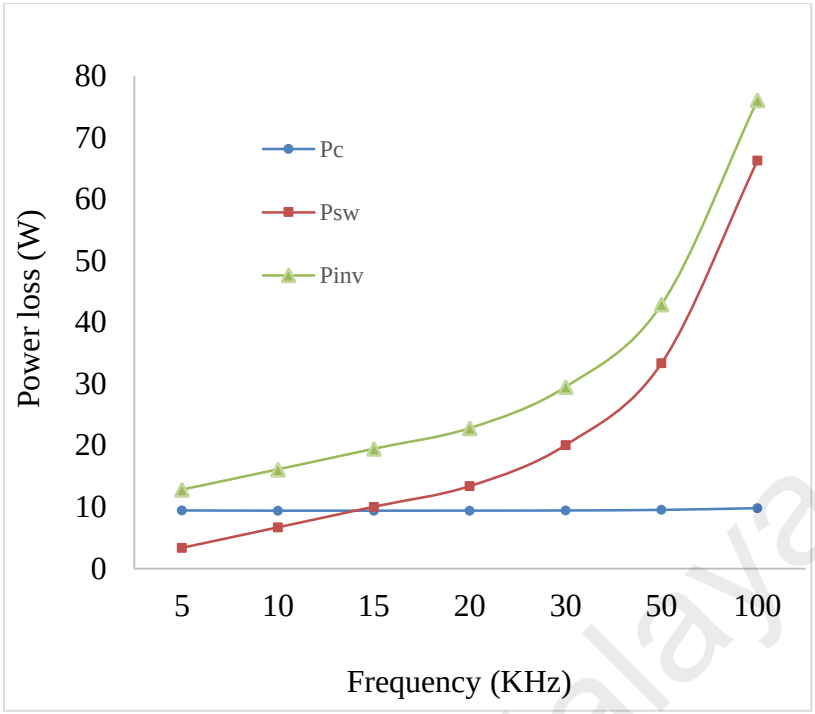


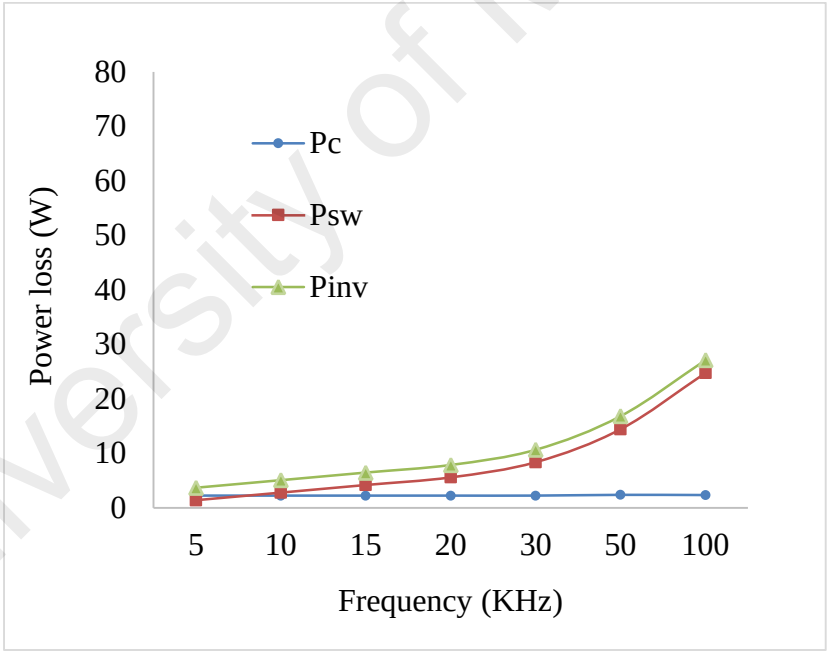
Figure 4.26: V_{LL}(THD) vs M for MBC**.**

4.5.1 Switching losses comparison

PLECS model of the inverter used in section 4.3 and controlled by ODZSI-MBC_1, is developed to measure the conduction and switching power losses at different operating conditions in section 4.4, i.e. (V_{dc} = 81, M = 0.8) and (V_{dc} = 149, M =1.1). The power loss of the inverter main bridge as a function of switching frequency for M = 0.8 and M = 1.1 is plotted in Figure 4.27. Conduction, switching, and inverter losses are defined as $P_{c,}$ P_{sw}, and P_{inv}, respectively. The gap between the two losses expands as switching frequency increases. Another important factor is the modulation index; the lower input dc voltage V_{dc} causes a higher losses on the inverter because it requires a higher voltage gain G. Consequently, a larger ST duty cycle will be used which leads to higher ST current. Moreover, changing of the switching frequency changes only the switching losses and has no influence on the conduction losses.



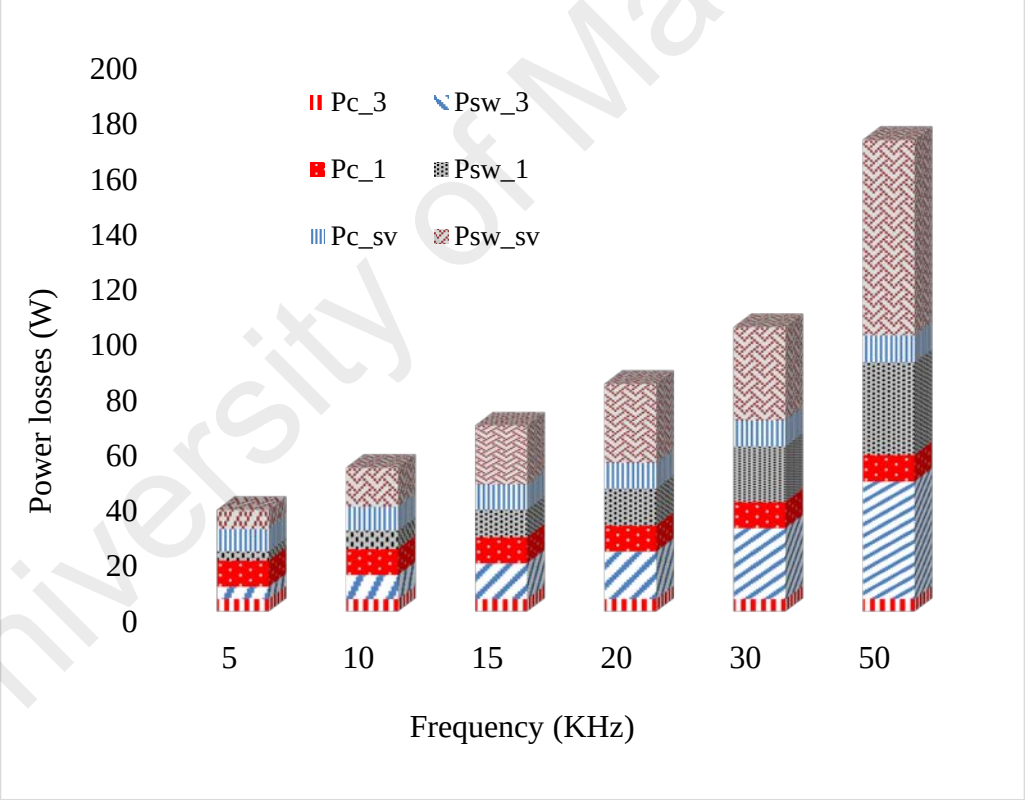
(a)



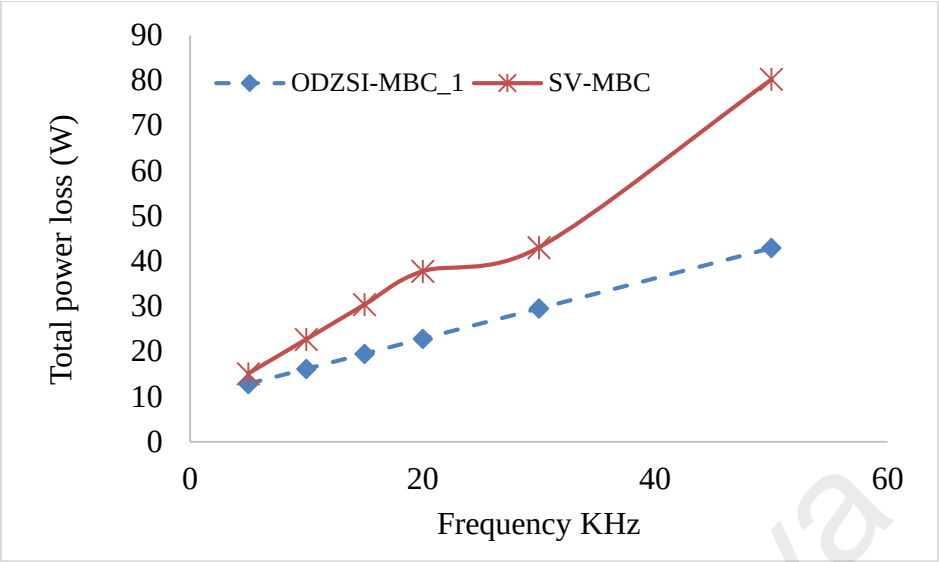
(b)

Figure 4.27: Power loss in the main bridge inverter, (a) *M*=0.8 and (b) *M*=1.1.

Figure 4.28 shows the power loss breakdown between the conduction and switching losses in the main bridge inverter with different switching frequencies. The figure compares conduction (P_{c_1}) and switching losses (P_{sw_1}) using the ODZSI-MBC_1; the conduction and switching losses using ODZSI-MBC_3 are denoted as P_{c_3} and P_{sw_3}, respectively; and the conduction (P_{c_SV}) and switching losses (P_{sw_SV}) using the SVPWM-based Maximum Boost Control (SV-MBC) strategy. The modulation index *M* is set to 0.8, and the dc input voltage is set to 81 V across all cases to obtain a $\hat{V}_{ph}$ equal to 100 V. From Figure 4.28, it can be seen that the switching loss becomes dominant with the increasing of the switching frequency F_{sw}.



(a)



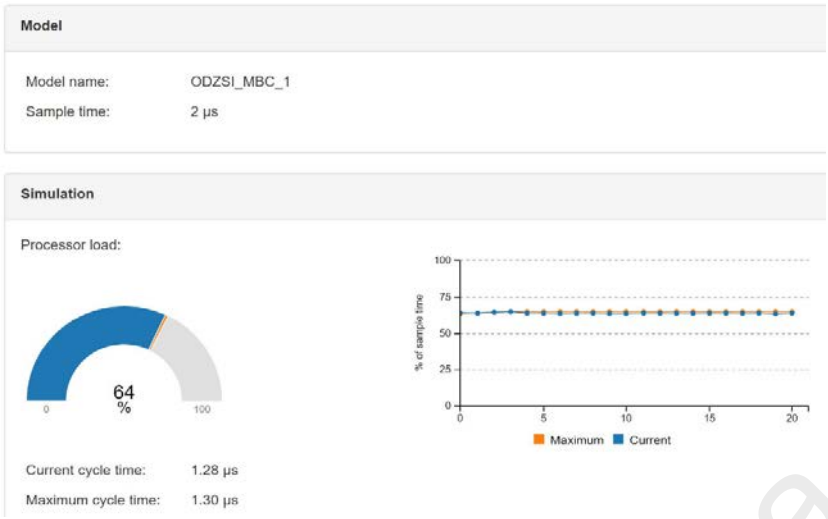
(b)

Figure 4.28: Comparison of conduction and switching losses for different control strategies.

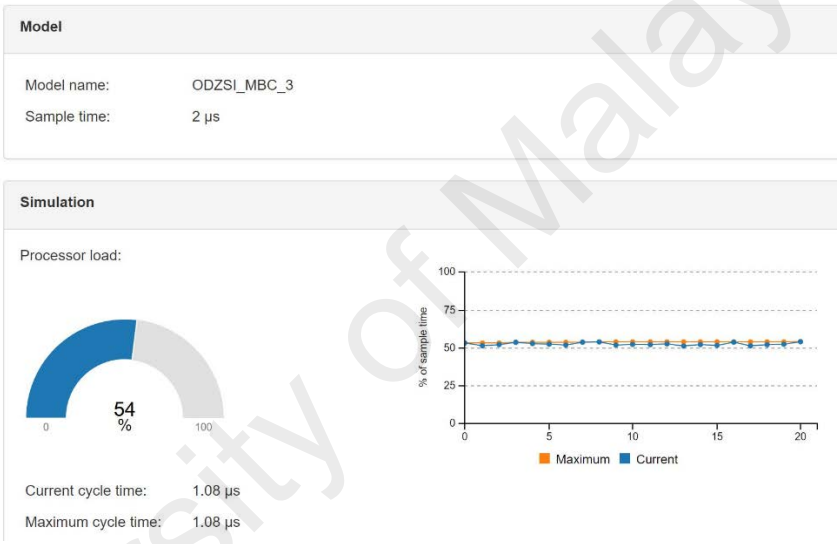
The comparison of the total inverter losses P_{inv} (conduction + switching) using the ODZSI-MBC_1 and SV-MBC (K. Yu, Luo, & Zhu, 2012b) with the corresponding six switching frequencies are shown in Figure 4.28 (b). P_{inv} varies proportionally with switching frequency. The P_{inv} incurred by ODZSI-MBC_1 is less than that incurred by SV-MBC. Consequently, the efficiency of the inverter is improved.

4.6 Comparison of the Total Execution Time (TET)

To show the good performance of the proposed control schemes, PLECS RT Box has been used to measure the total execution time of the ODZSI and other state of the art works as shown in Figure 4.29 . The total execution times recorded are 1.59 µs and 2.92 µs for the ODZSI and MSVPWM respectively. Therefore, to total execution time is reduced by 45% compared to the modified space vector. The recorded TET for the other control strategies is shown in Table 4.4.



(a)



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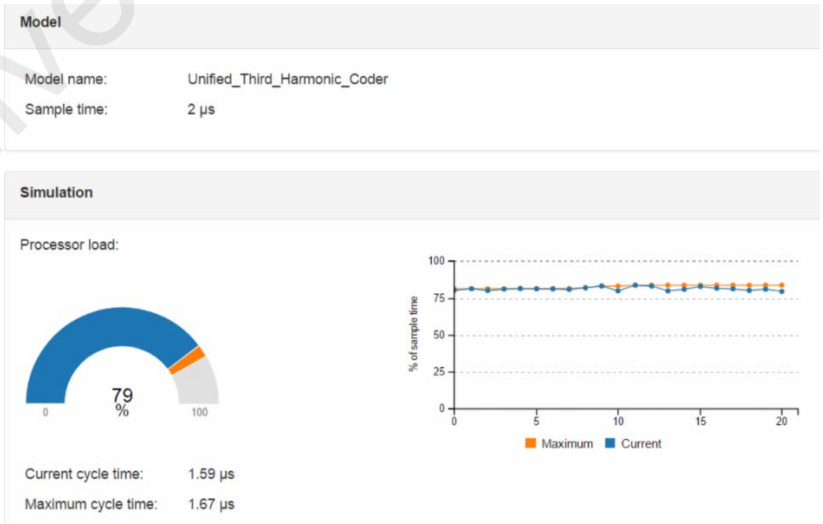

(c)

Figure 4.29: Total execution time: **(a)** ODZSI-MBC_1, **(b)** ODZSI-MBC_3, and **(c)** ODZSI for three phase

Table 4.4: The Total Execution Time

Control method	TET
ODZSI for three-phase	159 μs
ODSZI for single-phase	0.69 μs
MSVPWM	2.92 μs
ODZSI-MBC_1	1.28 μs
ODZSI-MBC_3	1.08 μs
CB-MBC	1.56 μs

4.7 Summary

In this chapter, the simulation and experimental test results of the proposed ODZSI control schemes have been presented and successfully implemented. A laboratory prototypes of qZSI/ZSI have been built. The obtained results show that the ODZSI_3 achieves the same performance as MBC CB-PWM for ZSI, and enhances the output voltage THD. Moreover, the ODZSI_1 is proposed to minimize the switching loss significantly. The switching losses comparison is provided showing that the proposed concepts offer the flexibility to choose the optimum control scheme for each application.

CHAPTER 5: CONCLUSION AND FUTURE WORK

5.1 Conclusions

The development of a new unified control scheme for impedance-network inverters with lower computation burdens, less switching losses, and with a low THD in the output is the crucial contribution of this study. The research includes a complete description of the proposed schemes, equations, comparisons with the well-known algorithms presented in the literature, and numerical analysis. The presented concepts are proven in simulations using Matlab/Simulink and validated experimentally.

In this thesis, the ODZSI modulation technique for single and three-phase H-bridge ZSI/qZSI has been implemented successfully, attaining an inverter output of good quality with extremely reduced computation burden. The low computational burden experienced with ODZSI is attributed to its simple geometrical calculations and graphical representation. Based on the two nearest output voltage levels of the inverter the reference vector is achieved. Moreover, In DSP controller, the overall execution time depends on the number of operation tasks, particularly the number of times of multiplying and dividing operations because they need a longer execution time than any other operations which is very important for the slower controllers. Due to the simple structure of the proposed control scheme and the reduced overall execution times, it can be easily implemented on a slow and cheap controller.

Firstly, the ODZSI has been implemented to modulate single-phase H-bridge quasi Z-source inverter. The ST period is inserted within the zero states (00 and 11), so as not to affect the normalized volt-sec average; while the active state remains unchanged. Using carefully inserted shoot-through pulses, only two switches of the same leg will turn ON during the shoot-through and the ST time is evenly distributed per control cycle. Hence the number of device commutations is significantly decreased.

The same principle has been extended modulate three-phase H-bridge quasi Z-source. The ST interval is extracted from the null states (000 or 111) and evenly distributed without altering the normalized volt-sec average to minimize the size of the inductors, the ST are inserted immediately adjacent to the active states in which the transition between the switching states requires only one switch to change its state to ensure no additional switch commutations per control cycle are introduced. Furthermore, to investigate the improved performance of the proposed control algorithm for qZSI over the modified space vector strategy, simulation using MSVPWM control was carried out using the same parameters as those of ODZSI. The simulation results show that the proposed control scheme is able to boost the output voltage same as the modified space vector strategy with less computation time of around 45% .

Finally, another control method has been proposed based on the single-phase modulator to obtain the maximum voltage gain of the ZSI (OD-MBC_3). The ST period is maximized by simultaneously turning all the switches ON during the zero states, whereas the active state remains unchanged to not affect the normalized volt-sec average since the both states have the same output voltage across the load, i.e. 0 V. The obtained simulation and experimental results show that the OD-MBC_3 achieves the same performance compared with CB-PWM for the ZSI with enhanced line voltage THD and lower computation time. However, this method incurs extra switching losses; therefore, an enhanced algorithm OD-MBC_1 is proposed, this algorithm has the ability to choose the appropriate phase leg to insert the ST in order to reduce the switching transitions. The ST period is located only in one phase-leg and it is maximized by turning all zero states into the ST state, while the active state times remain unchanged. Moreover, the use of a carefully selected ST significantly decreased the number of switching transitions as each switch is locked to the positive or negative dc rail during a period of $2\pi/3$. Only two switches of the same leg are turned ON during the ST state, and the ST time is distributed per two legs per control cycle.

Additionally, for a fair comparison, the total inverter losses P_{inv} (conduction + switching) using the ODZSI-MBC_1 and SV-MBC are compared since the use the same principal (the ST is located only on one leg). The P_{inv} incurred by ODZSI-MBC_1 is less than that incurred by SV-MBC. Consequently, the efficiency of the inverter is improved.

In OD-MBC_1, the ST is located on only one phase leg, thereby minimizing switching frequency. However, the current stress on the switches during the ST time will be increased compared with simultaneous ST on all legs. Thus, the OD-MBC_3 is suitable for low-switching-frequency applications. By contrast, the switching losses are particularly high for high-switching-frequency applications, thereby significantly decreasing the ZSI efficiency. In conclusion, a trade-off always exists between conduction (P_c) and switching (P_{sw}) losses, which determines the selection of optimized control method according to the application. In other word, the proposed concepts offer the flexibility of choosing the optimum control scheme based on the application.

5.2 Future work and recommendations

Although the developed control methods meet the study objectives, several issues require further investigation. The suggested future works with some recommendations are summarized in the following points.

- In this work, only the voltage fed qZSI/ZSI inverters are considered. As a counterpart, the current fed qZSI/ZSI inverter and other impedance source topologies should also be studied.
- Despite the appreciable simulation and experimental results attained using the ODZSI for single and three-phase two-level inverters, it would be a significant contribution to extend the analysis to modulate impedance source network multi-level inverter such as NPC Z-source inverter and seven-level single-phase grid-tied inverter etc.

- The qZSI/ZSI topologies are used in several applications, and the modulation techniques proposed have not targeted a specific application even though their enhanced voltage output quality and improved efficiency, it is likely to benefit renewable energy systems. In this case there is a possibility to change the dc supply with renewable energy devices such as photovoltaic or fuel-cell. Hence, an area for future investigation is to design a close loop modulator, and propose solutions that can solve unobvious concerns.

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LIST OF PUBLICATIONS AND PAPERS PRESENTED

- **N. Sabeur**, S. Mekhilef, and A. Masaoud, "**Extended maximum boost control scheme based on single-phase modulator for three-phase Z-source inverter**," *IET Power Electronics,* Volume 9, Issue 4, 30 p. 669 – 679, March 2016. (*ISI-cited publication, IF: 3.547* ***Q1***).

- **N. Sabeur**, S. Mekhilef, and A. Masaoud, "**A Simplified Time-Domain Modulation Scheme based Maximum boost Control for three-phase quasi-Z Source Inverters**," *IEEE Journal of Emerging and Selected Topics in Power Electronics.* (Accepted, DOI: 10.1109/JESTPE.2017.2763974). (*ISI-cited publication, IF: 4.269* ***Q1***).

- **N. Sabeur**, S. Mekhilef, and A. Masaoud, Mutsuo Nakaoka "**A Simple Modulation Based Maximum Boost Control Strategy for Three-Phase Quasi Z-Source Inverter,**" at the 8th IEEE International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), 2016.