

**DESIGN AND ANALYSIS OF NOVEL LOW-VOLTAGE
LOW-LOSS RF-MEMS SWITCH**

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**FACULTY OF ENGINEERING
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LOW-LOSS RF-MEMS SWITCH

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DESIGN AND ANALYSIS OF NOVEL LOW-VOLTAGE LOW-LOSS RF- MEMS SWITCH

ABSTRACT

RF-MEMS switch is a kind of electromechanical structure that is used to short or open a RF to millimeter-wave-frequency transmission line. Compared to traditional RF switches, RF-MEMS switches possess many significant advantages, such as negligible DC power consumption, small series capacitance, resistance and insertion loss, good isolation, as well as high linearity and cut-off frequency. RF-MEMS switch can be actuated by many different mechanisms, like electrostatic, electromagnetic, thermal, and piezoelectric; among them electrostatic mechanism is the most prevalent technique in use today. However, the main challenge of the electrostatic-actuated RF-MEMS switches is their comparatively high actuation voltage (20V~80V), which makes them unsatisfied for wireless communication systems; cannot be integrated with active CMOS circuitry; and lead them to have short lifetimes. The objective of this project is to design, optimize, simulate and analyze a low-voltage low-loss electrostatic-actuated RF-MEMS capacitive switch. The research methodology follows the steps of identifying the design specification, creating the novel 3D structure, optimizing the geometric dimensions, simulating and verifying the switch's properties, modeling the equivalent electric circuitry, and implementing it into the RF applications, namely MEMS phase shifters. The low-actuation voltage design is achieved by using novel combination of folded and spring beams which are used for supporting the switch's big membrane; and the low-loss property is realized by employing an inductive matching circuit, namely T-match or π -match circuit. The structure of the switch is optimized by using a new developed multi-response optimization method which is based on Taguchi method and weighted principal component analysis to accomplish the aims of low-

actuation voltage, robust structure, and relatively short switching time simultaneously. The final optimized RF-MEMS capacitive switch has actuation voltage of 3.06V with spring constant of 0.2378N/m, switching time of 34 μ s~19.5 μ s with bias voltage of 4V~7V, the insertion loss and isolation of -0.5487dB and -23.02dB, respectively, at frequency of 20GHz. By using T-match circuit, the insertion loss and isolation can be enhanced by 76.47% and 25.07%, respectively; and by using π -match circuit, the insertion loss can be improved by 76.53%. Two low-voltage low-loss MEMS phase shifters, namely MEMS switched-line phase shifter and DMTL phase shifter, by using proposed RF-MEMS switches are presented. For the 3-bit MEMS switched-line phase shifter, its average phase error and insertion loss is 0.5056° and -1.51dB, respectively, at 20GHz; both return loss and isolation are better than -11dB at a wideband frequency range of 18GHz to 22GHz; the design area is 6mm \times 4 mm. For the 3-bit DMTL phase shifter, its average phase error and insertion loss is 6.032° and -1.526dB, respectively, at 20GHz; the return loss is better than -10.05dB for all the phase shift conditions; the design area is 12.8mm \times 1.4mm.

Keywords: RF-MEMS switch, low voltage, low loss, multi-response optimization, MEMS phase shifter

REKA BENTUK DAN ANALISA NOVEL RF-MEMS SUIS YANG RENDAH VOLTAN DAN RENDAH KEHILANGAN SISIPAN

ABSTRAK

Suis RF-MEMS adalah sejenis struktur elektromekanikal dan digunakan untuk memendekkan atau membuka saluran penghantaran frekuensi gelombang mikro RF-ke-milimeter. Berbanding dengan suis RF biasa, suis RF-MEMS mempunyai kelebihan penting untuk penggunaan kuasa yang tidak dapat dielakkan, kurang kapasitansi dan rintangan siri, frekuensi potong yang tinggi, kehilangan sisipan yang rendah, pengasingan yang baik, dan garis lurus yang tinggi. Suis RF-MEMS boleh direkabentuk dalam banyak mekanisme penggerak yang berbeza, seperti elektrostatik, elektromagnetik, haba, dan piezoelektrik; antara lain suis RF-MEMS yang digunakan secara elektrostatik adalah teknik yang paling lazim digunakan pada hari ini kerana penggunaan tenaga yang hamper sifar, kelajuan beralih tinggi, saiz elektrod yang kecil, dan keserasian tinggi dengan proses litar bersepadu yang piawai. Walau bagaimanapun, cabaran terbesar bagi suis elektrostatik adalah voltan penggerak yang tinggi relatifnya (20V~80V), yang menjadikan mereka sukar untuk digunakan dalam sistem komunikasi jarak jauh atau tanpa wayar; menghadkan mereka untuk disepadukan langsung secara monolitik dengan litar CMOS aktif; dan boleh membawa mereka dengan jangka hayat yang lebih pendek. Objektif projek ini adalah untuk merekabentuk, mengoptimumkan, mensimulasikan dan menganalisis suis RF-MEMS yang menggunakan kuasa elektrostatik rendah. Metodologi penyelidikan adalah mengenal pasti spesifikasi reka bentuk, mewujudkan struktur 3D yang novel, mengoptimumkan dimensi geometri, mensimulasikan dan mengesahkan sifat suis, memodelkan litar elektrik dan melaksanakannya ke dalam aplikasi RF, iaitu pemalar fasa MEMS. Reka bentuk voltan rendah bertindak dicapai dengan menggunakan kombinasi lipatan dan gegelung yang

digunakan untuk menyokong membran besar suis; dan kehilangan sisipan yang rendah direalisasikan dengan menggunakan litar pepadanan induktif, iaitu litar padanan T atau litar padanan π . Struktur suis dioptimumkan dengan menggunakan kaedah pengoptimuman multi-respon yang dibangunkan berasaskan kaedah Taguchi dan analisis komponen utama yang dipertimbang untuk mencapai matlamat voltan rendah, struktur teguh, dan masa pensuisan yang agak singkat pada masa yang sama. Suis kapasitif RF-MEMS yang terakhir yang dioptimumkan mempunyai voltan penggunaan 3.06V dengan gegelung pemalar 0.2378N/m, masa bertukar 34 μ s~19.5 μ s dengan voltan bias 4V~7V, kehilangan sisipan dan pengasingan -0.5487dB dan -23.02dB, masing-masing, pada frekuensi 20GHz. Dengan menggunakan litar padanan T, kehilangan input dan pengasingan dapat ditingkatkan masing-masing sebanyak 76.47% dan 25.07%; dan dengan menggunakan litar padanan π , kehilangan sisipan boleh ditingkatkan sebanyak 76.53%. Dua pemindah fasa rendah MEMS voltan, iaitu MEMS fasa suis bersiri peralih dan DMTL fasa peralih, dengan menggunakan suis RF-MEMS telah dicadangkan. Untuk pemalar 3-bit MEMS fasa suis bersiri peralih, ralat fasa purata dan kehilangan sisipan min ialah 0.5056° dan -1.51dB, masing-masing pada 20GHz; kedua-dua pulangan kehilangan dan pengasingan adalah lebih baik daripada -11dB pada jarak frekuensi wideband 18 hingga 22GHz; kawasan reka bentuk adalah 6 mm \times 4 mm. Untuk 3-bit DMTL fasa peralih, kesilapan fasa purata dan kehilangan sisipan adalah 6.032° dan -1.526dB, masing-masing, pada 20GHz; kehilangan kembali adalah lebih baik daripada -10.05dB untuk semua keadaan peralihan fasa; kawasan reka bentuk adalah 12.8 mm \times 1.4 mm.

Kata kunci: suis RF-MEMS, voltan rendah, kehilangan rendah, pengoptimuman pelbagai tindak balas, MEMS fasa peralih

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LIST OF SYMBOLS AND ABBREVIATIONS

| | | |
|--------------------------------|---|---|
| IC | : | Integrated circuit |
| RF MEMS | : | Radio frequency micro-electro-mechanical systems |
| CPW | : | Coplanar waveguide |
| FET | : | Field-effect transistor |
| CMOS | : | Complementary metal-oxide-semiconductor |
| VLSI | : | Very large scale integration |
| DMTL | : | Distributed MEMS transmission line |
| FEM | : | Finite element modeling |
| T line | : | Transmission line |
| FOM | : | Figure-of-merit |
| SPST | : | Single-pole single throw |
| SPNT | : | Single-pole N throw (N=2, 3, 4...) |
| GA | : | Genetic algorithm |
| S/N | : | Signal to noise ratio |
| OA | : | Orthogonal array |
| WPCA | : | Weighted principal component analysis |
| MPI | : | Multi-response performance index |
| GaAs | : | Gallium arsenide |
| MOSFET | : | Metal-oxide-semiconductor field effect transistor |
| Al | : | Aluminum |
| SiO ₂ | : | Silicon dioxide |
| DC | : | Direct current |
| FEA | : | Finite element analysis |
| ANOVA | : | Analysis of variance |
| Si ₃ N ₄ | : | Silicon nitride |
| T/R | : | Transmit/receive |
| Q factor | : | Quality factor |
| TSBR | : | Two-step bipolar rectangular |
| S Parameters | : | Scattering parameters |
| EM | : | Electromagnetic |
| μm and mm | : | Micro meter and millimeter, respectively |
| L_t, C_t, R_t and G_t | : | Inductance, capacitance, resistance and admittance per unit length of CPW, respectively |
| Z_0 | : | Characteristic impedance of unloaded CPW (for standard RF cable, $Z_0=50\Omega$) |

| | | |
|--|---|---|
| Z_l | : | Characteristic impedance of the loaded CPW |
| ϵ_r and ϵ_{eff} | : | Dielectric constant and effective dielectric constant, respectively ($\epsilon_{eff}=(\epsilon_r+1)/2$) |
| c | : | Free-space velocity, 3×10^8 m/s |
| s | : | Periodic spacing between each two switches in DMTL phase shifter |
| C_b | : | ($=C_u$ or C_d) Equivalent capacitance of the RF-MEMS switch in DMTL phase shifter |
| C_u and C_d | : | Capacitance of the RF-MEMS switch when its bridge is at up-state and down-state position, respectively |
| C_f and C_{pp} | : | Fringing field capacitance and main part capacitance of C_u |
| C_{Ratio} | : | Down-state to up-state capacitance ratio |
| f_B | : | Bragg frequency of DMTL phase shifter |
| L_b and R_b | : | Equivalent inductance and resistance of the RF-MEMS switch in DMTL phase shifter |
| α_1 and α_2 | : | Loss per section of DMTL phase shifter's T line and MEMS bridge, respectively |
| α | : | Total loss per section of DMTL phase shifter |
| ω | : | Operation frequency |
| τ | : | Time delay per section of DMTL phase shifter |
| v_p | : | Phase velocity of the DMTL phase shifter |
| f_{cutoff} | : | Cutoff frequency of the CPW |
| L_h and Z_h | : | High-impedance T-line section's length and impedance of CPW right-angle bend |
| C_{bridge} | : | Air-bridge capacitance of CPW right-angle bend |
| $V_{pull-in}$ and $V_{pull-out}$ | : | Pull-in voltage (or actuation voltage) and pull-out voltage of the RF-MEMS switch, respectively |
| $V_{pull-in, \sigma}$ and $V_{pull-out, \sigma}$ | : | Pull-in voltage and pull-out voltage under dielectric charging effect, respectively |
| k | : | Total spring constant of the membrane and beams |
| g_0 | : | Initial gap between the membrane and the signal line |
| g_{air} | : | Air gap between the membrane and dielectric layer |
| ϵ_0 | : | Permittivity of air, 8.854×10^{-12} F/m |
| t_d | : | Thickness of the thin dielectric layer |
| A | : | Area of the membrane, namely the product of the membrane's width and length ($W\times L$) |
| $F(z, t)$ | : | External forcing function due to the electrostatic attraction across parallel plate capacitance |
| m | : | Lumped mass (total mass of membrane and beams of the RF-MEMS switch) |
| ω_r (or f_r) | : | Mechanical resonant frequency |
| ζ | : | Damping ratio |
| H_{sub} | : | Thickness of substrate |

| | | |
|---|---|--|
| G | : | Gap between the signal line and the ground plane |
| t_{CPW} | : | Thickness of the CPW (or the signal line) |
| $L1, L2, \text{ and } L3$ | : | The first, second and third length of the folded beam, respectively |
| W_{beam} | : | Beam width |
| t_{OFF} and t_{ON} | : | Switch-off and switch-on time |
| σ_v and σ_y | : | Von Mises stress and yield stress |
| V_{in} | : | Applied DC bias voltage |
| L_{h-T}, R_{h-T} and C_{h-T} | : | Equivalent lumped elements of high-impedance T-line section for T-match RF-MEMS switch |
| L_{hi-T} and W_{hi-T} | : | Length and width of high-impedance T-line section for T-match RF-MEMS switch |
| $S11_{up}$ and $S21_{up}$ | : | Up-state return loss and insertion loss |
| $S11_{down}$ and $S21_{down}$ | : | Down-state return loss and isolation |
| $\Delta S11_{up}$ and $\Delta S21_{up}$ | : | Improvement of the up-state return loss and insertion loss |
| $\Delta S11_{down}$ and $\Delta S21_{down}$ | : | Improvement of the down-state return loss and isolation |
| $L_{h-\pi}, R_{h-\pi}$ and $C_{h-\pi}$ | : | Equivalent lumped elements of high-impedance T-line section for π -match RF-MEMS switch |
| $L_{hi-\pi}$ and $W_{hi-\pi}$ | : | Length and width of high-impedance T-line section for π -match RF-MEMS switch |
| $\Delta\phi$ | : | Phase shift |
| W_s | : | Width of the CPW's signal line |
| $T0$ | : | Structure's final temperature |
| μ | : | Viscosity of the air (at standard pressure and temperature, namely 25°C and 101kPa, which is 1.845×10^{-5} kg/ms or Pa·s) |
| E | : | Young's modulus |
| E_{in}, E_{σ} and E_{total} | : | Applied electric field, parasitic electric field and total electric field, respectively |
| σ | : | Parasitic charge density in the dielectric layer |
| $P_{pull-down}$ and $P_{hold-down}$ | : | Pull-down power and hold-down power, respectively |
| Z_{up} and Z_{down} | : | Impedance of RF-MEMS switch at switch-up and switch-down state, respectively |
| Z_s | : | Impedance of shunt RF-MEMS capacitive switch |
| C_{s1}, L_{s1} and R_{s1} | : | Membrane's equivalent lumped elements for classic RF-MEMS switch |
| C_{s2}, L_{s2} and R_{s2} | : | Beams' equivalent lumped elements for classic RF-MEMS switch |

CHAPTER 1: INTRODUCTION

1.1 Background

The term of MEMS is an abbreviation of micro-electro-mechanical systems. MEMS are a process technology used to create tiny integrated devices or systems that combines mechanical and electrical components together (Allen, 2007). The size of a MEMS component ranges from one micrometer (μm) to one millimeter (mm). MEMS devices allow monolithic integration which places mechanical microstructures, micro sensors, and micro actuators with microelectronic processors or controllers together on the same chip level to reduce the parasitic capacitance, transmission loss and improve the output accuracy. Two- or three-dimensional MEMS components of small size can be fabricated in batch and precision to reduce the cost. These devices (or systems) have the ability to actuate, control, and sense micro-scale parameters, and generate the macro-scale effects. All of these advantages make MEMS technology is superior to the traditional machining or manufacturing methods in the modern Integrated Circuit (IC) and micro system design.

MEMS basically can be classified into either a sensor or an actuator; both of them can be considered as a transducer, which is a device that can transform one modality of energy or signal into another modality. MEMS sensor is a device which can measure information from a surrounding environment and provide an electrical output signal in response to the parameter it measured; while MEMS actuator is a device that can convert an electrical signal into a physical action (e.g. displacement, force, heat, and fluid flow). Therefore, MEMS devices generally can process several energy domains using one device, such as mechanical, thermal, chemical, radiant, magnetic and electrical. MEMS technologies have been developed since 1970s. Many MEMS

applications have been commercialized, such as accelerometers used to control airbag deployment in vehicles, pressure sensors for medical applications, gas chromatographs, inkjet printer heads, projection displays and micro positioners in data storage systems, telecommunications (optical and wireless), biomedical and process control areas.

RF MEMS (namely radio frequency micro-electro-mechanical systems) is a big category of MEMS devices which are designed to be operated at the radio frequency to millimeter-wave frequency (0.1GHz to 100GHz), and provide RF functions. RF MEMS are manufactured almost in the same way as semiconductors but can handle RF signals. There are various types of RF-MEMS components, such as relays, tunable capacitors, switches, integrated inductors, mechanical resonators, filters, and some representative microwave and millimeter-wave components (Yao, 2000); among them, RF-MEMS switches, switched capacitors and varactors are the most popular components so far (Sedaghat Pisheh, 2013).

RF-MEMS switch is an electromechanical structure which operates at DC to 100GHz. With the help of an input voltage control, the RF-MEMS switch can generate a series of mechanical movements to short or open a RF transmission line. Normally RF-MEMS switches can be integrated with a microstrip, planar or coplanar waveguide (CPW).

1.2 Motivation

Comparing with the traditional RF switches, such as field-effect transistors (FET) or p-i-n diodes, RF-MEMS switches have many significant advantages, such as negligible power consumption, less series capacitance and resistance, very high cut-off frequency, good isolation and high linearity; the main drawback is that RF-MEMS switches need

much higher actuation voltage (normally 20 to 80V) than the traditional RF switches (generally 3 to 5V) (Rebeiz, 2003a). For example, Blondy et al. have published one US patent on RF-MEMS switch in 2017 which has actuation voltage of 35V to 40V (Blondy et al., 2017). This high actuation voltage prevents the RF-MEMS switches to be monolithically integrated with the most active CMOS (complementary metal-oxide-semiconductor) circuitry, since most standard CMOS process fabricated ICs require compatible operating voltage supply of 5V, 3.3V or less than 3.3V (Wey, Huang, & Chow, 2002; Yusoff, Zoolfakar, Aman, & Ahmad, 2004; Analog Devices, 2016; Radant MEMS, 2013). If an external off-chip circuit or additional booster is employed, the entire system would become more complex, larger, and consume more power. For example a DC-DC converter that can be used to actuate Radant MEMS switches was produced by Radant MEMS to boost the voltage supply of 5V to 90V (Radant MEMS, 2013). On the other hand, the high voltage supply of the RF-MEMS switches are hard to be used in remote or wireless communication systems. Also Chan et al. (Chan, Lesnick, Becher, & Feng, 2003) and Goldsmith et al. (Goldsmith et al., 2001) have indicated that a high actuation voltage may lead to a shorter lifetime for capacitive RF-MEMS switches which use dielectric layers for isolation. Therefore, proposing a low-actuation voltage design for RF-MEMS capacitive switch becomes a significant engineering interesting.

In order to design electrostatic-actuated RF-MEMS capacitive switch by means of low-actuation voltage, generally it can be achieved by proposing a switch structure with large actuation area, small spring constant, and little initial air gap between the two electrodes. The ranges of air gap and actuation area are basically determined by capacitance ratio and up-state return loss, respectively (Ma, Nordin, & Soin, 2015). The most flexible and important parameter which can be designed by the researchers is the total spring constant of the membrane and beams. The spring constant cannot be

reduced too much without considering other related properties such as maximum von Mises stress and switching speed which is also affected by the specifics of the membrane and beams. Therefore, a multi-response optimization for the proposed capacitive RF-MEMS switch is definitely essential which could enhance its quality properly. There are several works focusing on the optimization of the spring constant or beams structure, such as (Gong, Zhao, Xin, Lin, & Bai, 2009; Huang et al., 2001; Kundu et al., 2010; Shalaby et al., 2009); but none of them optimize the spring constant, maximum von Mises stress, and structure's resonant frequency simultaneously in one design to obtain a low-actuation-voltage, robust-vibrating and high-switching-speed RF-MEMS capacitive switch.

Although RF-MEMS switches can provide better RF performance than the traditional RF switches, most proposed low-actuation voltage RF-MEMS capacitive switches which are actuated by electrostatic force do not present good RF performance; especially the up-state return loss (normally $< -10\text{dB}$) and insertion loss (normally $> -1\text{dB}$). It can be seen from the following works: i) Dai & Chen developed a RF-MEMS capacitive switch using CMOS and post-CMOS process with actuation voltage of 7V; however, its insertion loss is -3.1dB at 40GHz (Dai & Chen, 2006); ii) Badia et al. presented an electrostatic RF-MEMS capacitive switch using AlN (aluminum nitride) with actuation voltage of 21.8V but the up-state return loss is only -9.23dB (Badia, Buitrago, & Ionescu, 2012); iii) Deng et al. proposed a low-voltage capacitive RF-MEMS switch (actuation voltage = 16V) had insertion loss of -3dB at 50GHz (Deng, Wei, Fan, & Gan, 2015); and iv) one of my previous work on low-voltage RF-MEMS switch (actuation voltage = 3.04V) exhibits insertion loss of -5.65dB at frequency of 40GHz; v) few latest low-voltage RF-MEMS capacitive switches have been published with good isolations and insertion losses, but no return losses were reported (Shekhar et al., 2017; Shajahan & Bhat, 2018). The reason of the large insertion loss is basically

because the small gap between two electrodes or the large actuation area is used which is in order to achieve the low-actuation-voltage design (Mafinejad, Kouzani, Mafinezhad, & Mashad, 2013). Therefore improving the low-voltage RF-MEMS switches' RF performance (namely reducing the insertion loss and increase the switch-on-state return loss) is another motivation for RF-MEMS capacitive switch's design.

1.3 Research Objectives

A well designed RF-MEMS switch should demonstrate several characteristics, such as low actuation voltage, high switching speed, low insertion loss, high isolation, good reliability (Mahameed, Sinha, Pisani, & Piazza, 2008), large power handling and simple fabrication steps in order to reduce the cost. The previously developed RF-MEMS switches have demonstrated some of the specific good characteristics, such as low-actuation voltage and CMOS (complementary metal-oxide-semiconductor) compatible process in (Kuwabara et al., 2006), high isolation in (Kuwabara et al., 2006; Pacheco, Katehi, & Nguyen, 2000; Shen & Feng, 1999), low insertion loss in (Wang, McCormick, & Tien, 2004), high switching speed in (Dai & Chen, 2006), and robust design in (Shalaby et al., 2009). Different applications generally focus on different requirements; and it is not practicable to fulfill all the good characteristics in one designed RF-MEMS switch since some characteristics are conflicting, for example low spring constant and high switching speed. Here the design objectives expound the most important characteristics in this capacitive RF-MEMS switch's design.

The objectives of the research can be briefed into following three points:

1. To design, optimize, and simulate a low-voltage low-loss electrostatic RF-MEMS capacitive switch by using CMOS-compatible technology.

2. To validate the usage of the developed RF-MEMS switches by implementing them into K-band low-voltage low-loss MEMS phase shifters, namely MEMS switched-line phase shifter and DMTL (distributed MEMS transmission line) phase shifter.
3. To develop a systematic design and optimization flow in detail for RF-MEMS capacitive switch which further can be employed into other related MEMS devices' development.

1.4 Research Scope

In this project, the novel design of structure, geometric optimizations, properties' simulation, and electromagnetic modeling of the RF-MEMS switches and MEMS phase shifters are included. For the MEMS phase shifters, the final layout design is proposed in the thesis to estimate their occupation areas. The content about fabrication and measurements of the developed RF-MEMS switches and MEMS phase shifters are not included in the scope of this work, which is suggested in the future work.

1.5 Project Methodology

The research methodology for MEMS development is more or less the same which starts from defining the problem and ends with the device's finalization. In this project, the literature review about the RF-MEMS capacitive switch was done first; followed with the problem statement and design objectives. Then the design specifications for proposed low-voltage low-loss RF-MEMS capacitive switch are determined. A novel 3D structure for low-actuation voltage purpose is created and followed with the beams' optimization. In order to improve its RF performance, the T-match and π -match RF-MEMS switches are proposed and optimized. The RF-MEMS switches' electromagnetic

modelings are developed and the values of their equivalent lumped elements are extracted from the RF simulation results. In the end, the functions of the RF-MEMS switch are verified through implementing it into MEMS phase shifters where two different topologies, namely MEMS switched-line and DMTL phase shifter are designed, simulated, analyzed and compared. The main flow of the project methodology is displayed in Figure 1.1.

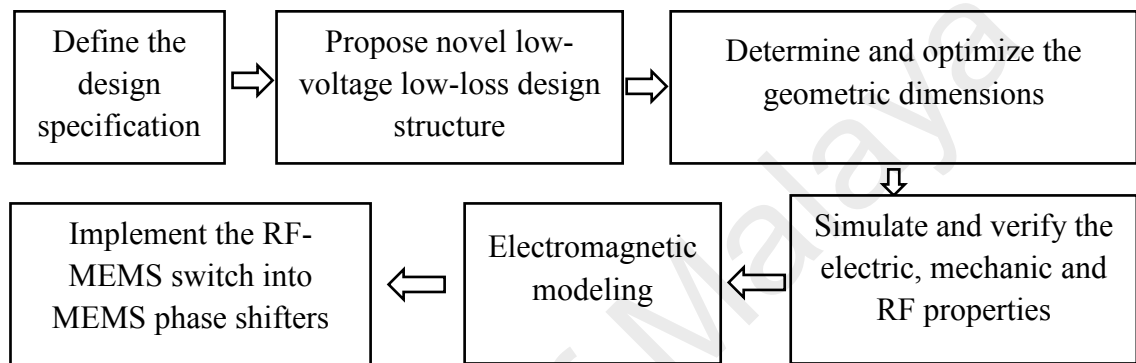


Figure 1.1: Main steps of the project methodology

1.6 Thesis Outline

The whole thesis contains totally five chapters together with appendix and references.

Chapter 2 is about the literature review for the whole research work. First, the RF-MEMS switches' overview, categories, state-of-the-art designs and interface circuits or applications are introduced. Then MEMS phase shifters, as one kind of important implementations for RF-MEMS switches, are reviewed, where MEMS switched-line phase shifter and DMTL phase shifter has been emphasized. The designed MEMS phase shifters are achieved by integrating the RF-MEMS switches and CPW line; therefore, the CPW line and its discontinuity is introduced in the last part. In order to optimize the dimensions of the RF-MEMS switch's beams, a novel multi-response optimization method which is based on Taguchi method and weighted principal component analysis is developed and employed in this work. The introduction of

Taguchi method and weighted principal component analysis is included in this chapter also.

Chapter 3 is mainly about the research methodology. A systematic design flow for the RF-MEMS capacitive switch is exploited in this chapter. The working principle and mechanical modeling of the electrostatic RF-MEMS capacitive switch is explained with the proposed novel 3D structure; and it is followed with its basic dimensions' determination (e.g. CPW, membrane and air gap) by using partial design specifications. For the switch's geometric optimization, its low-spring-constant beams are optimized by multi-response optimization method, in order to achieve the goals of low-actuation voltage, robust vibration and relatively short switching time; T-match and π -match circuits are employed in order to enhance the RF performance of the RF-MEMS switch, where the dimensions of the high-impedance transmission-line sections used in T-match and π -match circuits are optimized also. In the end of the chapter, the optimized RF-MEMS switches were implemented into the MEMS switched-line phase shifter and the DMTL phase shifter to illustrate the switches' usage.

Chapter 4 presents the research results and discussions. The optimized RF-MEMS capacitive switch is verified by finite element modeling (FEM) approach. Its static, dynamic and RF performance is simulated and analyzed. For the static simulation, the RF-MEMS switch's spring constant, resonant frequency, von Mises stress, actuation voltage, switch capacitance, and the residual stress and thermal effect on the actuation voltage is discussed. For the dynamic simulation, the RF-MEMS switch's switching time, quality factor, parasitic charge density, and the actuation voltage in time domain under dielectric charging effect is explained. Meanwhile a long lifetime control voltage, namely two-step bipolar rectangular waveform is proposed. For the RF performance, the RF-MEMS switch's S parameters, operation frequency bandwidth, switching

impedance and power handling is simulated. In order to improve the up-state return loss to meet the design specification, the T-match and π -match techniques are used; the T-match and π -match RF-MEMS switches' S parameters are simulated and compared. The optimized RF-MEMS switch, T-match RF-MEMS switch and π -match RF-MEMS switch is modeled by using RLC circuit and their lumped elements' values are extracted from their 3D structures by using Microwave office[®] software. In the end the properties of the designed 3-bit MEMS switched-line phase shifter and DMTL phase shifter are presented by using modeling simulation approach; and their results have been compared with other related designs to proof the usage and advantages of the proposed RF-MEMS switches.

The last chapter is about the conclusion of the work. The thesis contribution and the future work to be continued for the developed RF-MEMS switches are discussed.

CHAPTER 2: LITERATURE REVIEW

2.1 Introduction

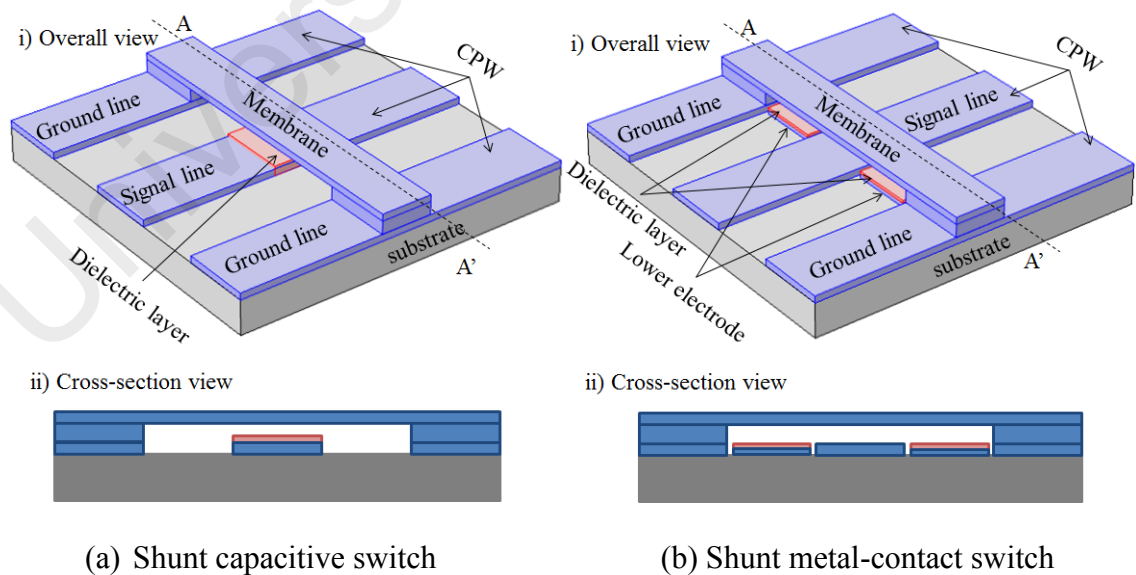
In this chapter, four topics or concepts which are used in the thesis are reviewed and studied. First is about RF-MEMS switch where its classifications, state-of-the-art designs, as well as some related applications are introduced. The second topic is about the literature review on the multi-response optimization methods, Taguchi method as well as weighted principal component analysis which will be used for the RF-MEMS switch's optimization. Then as one kind of important application, MEMS phase shifters which are implemented by RF-MEMS switches and CPW lines are studied with their classifications. Two important topologies, namely MEMS switched-line phase shifter and DMTL phase shifter, are emphasized in the third topic. Since the proposed MEMS phase shifters are constructed by optimized RF-MEMS switches and CPW, the fourth topic is about the concept and design methods of CPW transmission line (T line) and its discontinuity. In the end, it is the summary of the chapter.

2.2 RF-MEMS Switches

2.2.1 Classifications

RF-MEMS switches are devices that use mechanical movement to achieve a short or open circuit in an RF T-line circuit and operate at DC to 100GHz (Rebeiz & Muldavin, 2001; Blondy et al., 2017). Generally they are integrated together with a planar or CPW T lines. A RF-MEMS switch at least comprises of three parts, namely, a metal beam or membrane as the top electrode, a T line, and a lower pad as the bottom electrode which can be part of the T line.

RF-MEMS switches can be categorized based on many different characteristics. For example in terms of their contact mechanism, there are i) capacitive type (namely metal-dielectric-metal contact) and ii) metal-contact type (namely metal-to-metal contact) (Blondy et al., 2017). Figure 2.1 shows that (a) and (c) are RF-MEMS capacitive switches while (b) and (d) are RF-MEMS metal-contact switches. In terms of the switches' electrical connection with the T line, they can be either shunt-type or series-type switch, as shown in Figure 2.1 where (a) and (b) are shunt-type RF-MEMS switches; and (c) and (d) are series-type RF-MEMS switches. In terms of mechanical structure, the RF-MEMS switches' suspended moving part can be designed as a cantilever beam, clamp-clamp beam, or plate of diverse shapes. In Figure 2.1 (a) and (b) are designed with clamp-clamp beam while (c) and (d) are designed with cantilever beam. There are several actuation mechanisms for RF-MEMS switches, such as electrostatic, electromagnetic, thermal, piezoelectric, or several different mechanisms combined together. The RF-MEMS switches' suspended electrode also can be designed to move either vertically or laterally.



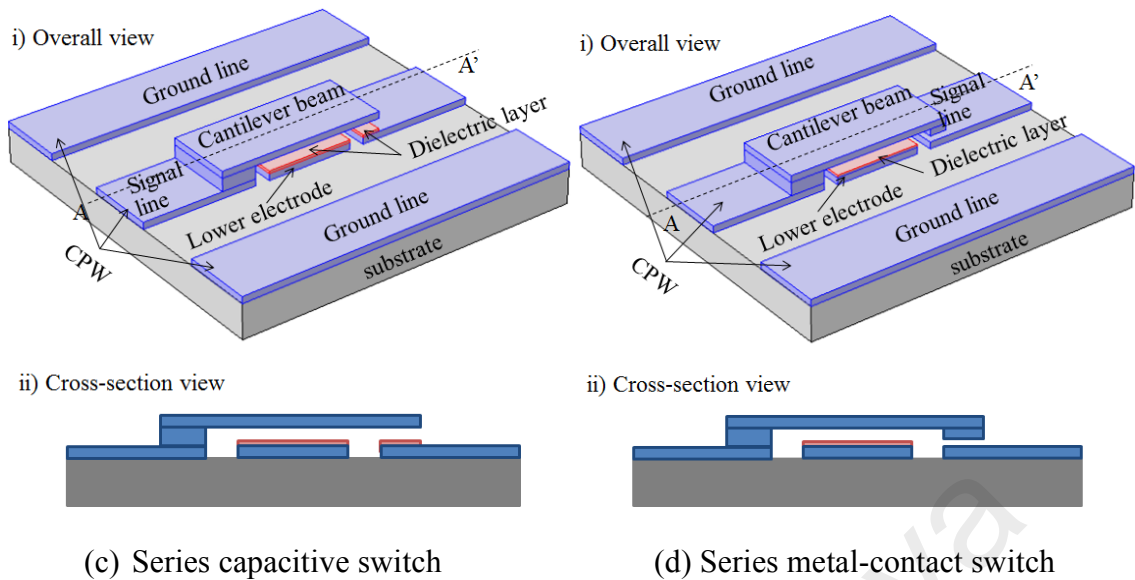


Figure 2.1: Typical RF-MEMS switch design models in different contact mechanism and electrical connection

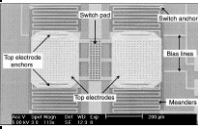
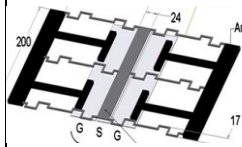
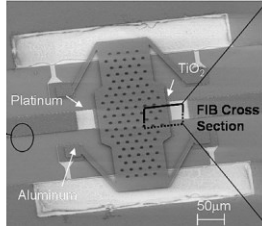
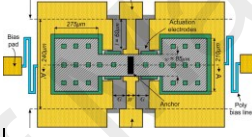
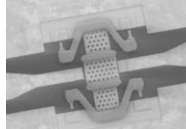
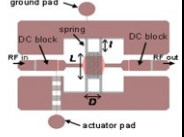
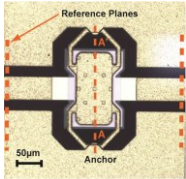
2.2.2 State-of-The-Art RF-MEMS Capacitive Switches

Among all of the different kinds of RF-MEMS switches, electrostatic-actuated capacitive RF-MEMS switch is one of the most prevalent techniques in use today (Daneshmand & Mansour, 2011; Ma, Nordin, & Soin, 2015). This is because, compared to metal-contact RF-MEMS switch, the capacitive RF-MEMS switch has less stiction problem (Brown, 1998) and can work for higher frequency range (e.g. 10GHz~120GHz). Moreover, compared to thermal, magnetic or other kinds of actuation mechanisms, the electrostatic-actuated RF-MEMS switch has nearly zero power consumption, high switching speed, small electrode size, thin structure layers used, 50-200 μN of achievable contact forces, the possibility of biasing the switch using high-resistance bias lines, and the high compatibility with a standard IC process (Angira & Rangra, 2015; Ma, Nordin, & Soin, 2015). Figure 2.1 (a) and (c) illustrate the configuration of RF-MEMS capacitive shunt and series switch, respectively; both of them are suitable for high-frequency ($>10\text{GHz}$) applications. In capacitive RF-MEMS switch, the switch's impedance is varied by the coupling capacitance's changing. In

switch-on state, the membrane is suspended in its original position; there is an air gap existing between the two electro plates; therefor the up-state capacitance is small which results in a high impedance between input and ground. In switch-off state, the membrane is pulled down to the signal line; there is only a thin dielectric layer between them; therefore the down-state capacitance is large which results in a small impedance between input and ground. So the basic principle of a capacitive RF-MEMS switch is a function of “state-off/state-on” capacitance ratio (Bansal et al., 2016) which is considered to be a crucial Figure-Of-Merit (FOM) and should be as high as possible (Chakraborty & Gupta, 2017; Shekhar, Vinoy, & Ananthasuresh, 2018; Rottenberg et al., 2003).

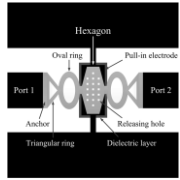
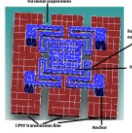
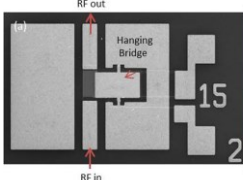
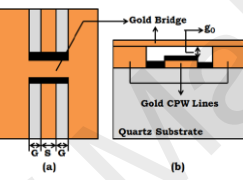
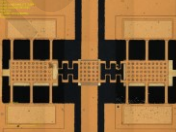
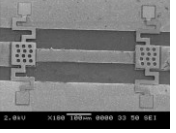
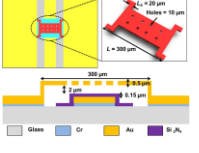
Table 2.1 has summarized some recently developed RF-MEMS capacitive switch by electrostatic-actuated mechanism. From these works, several conclusions can be obtained as following. i) Electrostatic-actuated shunt-type RF-MEMS capacitive switches are easily integrated with CPW T-line circuit to control its short or open state by using a moveable beam or membrane. ii) In order to reduce the substrate RF-signal losses, the high-resistivity silicon, quartz or GaAs is suggested as substrate. The use of normal low-resistivity silicon substrate shows degradation in terms of the insertion loss and isolation (Dai & Chen, 2006; Ma, Nordin, & Soin, 2015). A possible solution to this is to create an air trench in silicon substrate. iii) Lower spring constant can contribute to smaller actuation voltage but it limits the actuation time. iv) High relative dielectric constant can lead to a large capacitance ratio which can further reduce the switch's insertion loss and improve its isolation. v) Most electrostatic shunt capacitive RF-MEMS switches can be fabricated by using MEMS surface micromachining process which can be standard CMOS and post-CMOS process or CMOS-compatible process.

Table 2.1: Typical designs of electrostatic-actuated RF-MEMS capacitive switch

| RF-MEMS Switch | Peroulis et al., 2003, | Dai & Chen, 2006, | Fernández-Bolaños et al., 2008, | Fouladi & Mansour, 2010, | Badia et al., 2012, | Persano et al., 2012, | Zareie & Rebeiz, 2013, |
|---|---|---|--|---|---|---|---|
| Structure |  |  |  |  |  |  |  |
| Substrate | Si | Si | HR-Si (10kΩ.cm)+air trench | Si+air trench | HR-Si (3kΩ.cm) | GaAs | Quartz |
| Actuation Voltage | 6V | 7V | 8V | 82V | 21.8V | 25V | 50~55V |
| Spring Constant | 1.1N/m | 0.27N/m | --- | --- | 1.43N/m | --- | 71N/m |
| Air Gap | 3~4μm | 3.5μm | 1.62μm | 0.64~66μm | 2.3μm | 3μm | 3μm |
| Dielectric | 0.14~0.2μm Si ₃ N ₄ $\epsilon_r=6\sim7$ | 1.1μm SiO ₂ $\epsilon_r=3.9$ | 0.2μm TiO ₂ $\epsilon_r=20$ | 0.73μm SiO ₂ $\epsilon_r=3.9$ | 0.3μm AlN $\epsilon_r=9.8$ | 0.3μm Si ₃ N ₄ $\epsilon_r=6\sim7$ | 0.2μm Si ₃ N ₄ |
| Operation frequency | --- | 40GHz | 20GHz | 20GHz | 40GHz | 25GHz | 16GHz |
| On-State Return Loss | --- | -10dB | --- | -13dB | -9.23dB | --- | -17dB |
| Insertion Loss | --- | -3.1dB | <-0.5dB | -0.98dB | -0.68dB | -0.8dB | -0.2dB |
| Isolation | --- | -15dB | >-20dB | -17.9dB | -35.8dB | -57dB | -5.2dB |
| Capacitance Ratio (C _d /C _u) (F) | 44 (2.2p/50f) | 13.4 (0.15p/11.2f) | 196 (10p/60f) | 91 (2.1p/23f) | 9.87 (1.27p/0.13p) | 16.3 (2.2p/0.135p) | 6.3 (0.63p/16f) |
| Actuation Time | 52μs | 8.2μs | --- | 96μs | --- | 100μs | 20μs |
| Fabrication Process | Four-mask process | TSMC0.35μm + Maskless post-process | Six-mask process | TSMC0.35μm+ Maskless post-process | Seven-mask process | Eight-mask process | UCSD fabrication process |

Note: HR-Si means high-resistivity silicon

Table 2.1, continued: Typical designs of electrostatic-actuated RF-MEMS capacitive switch

| RF-MEMS Switch | Deng et al., 2015, | Lakshmi et al., 2015, | Bansal et al., 2016 | Chakraborty & Bhaskar, 2017 | Gopalakrishnan et al., 2017 | Shajahan & Bhat, 2018, | Shekhar et al., 2018, |
|---|---|---|--|---|---|---|---|
| Structure |  |  |  |  |  |  |  |
| Substrate | HR-Si | HR-Si | Si | Quartz | Borofloat 33 Schott glass | HR-Si (8kΩ.cm) | Pyrex glass |
| Actuation Voltage | 16V | 6.25V | 16.2V | 14.6V | 8V | 18.5V | 4.8V |
| Spring Constant | --- | --- | 0.93N/m | 32.25N/m | --- | --- | 1.34N/m |
| Air Gap | 1.25μm | 3μm | --- | 0.5μm | 2μm | 2.5μm | 2μm |
| Dielectric | 0.15μm Si ₃ N ₄ ε _r =6~7 | 0.02μm Si ₃ N ₄ ε _r =6~7 | SiO ₂ ε _r =3.9 | 0.15μm Si ₃ N ₄ ε _r =6.7 | 0.06μm Si ₃ N ₄ ε _r =7.6 | 0.2μm LTO | 0.15μm Si ₃ N ₄ ε _r =6~7 |
| Operation frequency | 50GHz | 10GHz | 10~11GHz | 22GHz | 8.223GHz | 15.1GHz | 40GHz |
| On-State Return Loss | --- | --- | --- | -21dB | --- | -27dB | -12dB |
| Insertion Loss | -3dB | -0.003dB | -0.3dB | -0.18dB | >-1dB | -0.4dB | -0.4dB |
| Isolation | -19dB | -78dB | -25dB | -25dB | -37.56dB | -52.81dB | -40dB |
| Capacitance Ratio (C _d /C _u) (F) | 6.8 (0.34p/55f) | --- | --- | 5.5 | --- | 30 (1.7p/53f) | 8.6 (0.69p/80f) |
| Actuation Time | --- | --- | 55μs | 620ns | --- | --- | 33μs |
| Fabrication Process | MEMS surface micromachining process | Four-mask process | MEMS surface micromachining process | MEMS surface micromachining process | Six-mask process | Five-mask process | Four-mask process |

Note: HR-Si means high-resistivity silicon

2.2.3 Applications

The nearly ideal electrical response of RF-MEMS switches have allowed many designers to build state-of-the-art switching circuits from 0.1GHz all the way to 120GHz (Rebeiz, 2003), such as MEMS phase shifter, reconfigurable antennas, tunable filters, MEMS-based voltage-controlled oscillators, MEMS varactors, power amplifier, switching networks, and digital capacitor banks. These switching circuits or subsystems can be further employed into lots of higher-level systems, such as cellular telephones, modern telecommunication, automotive and defense applications, base stations, satellites, wireless communication systems and other high-performance instrumentation systems (Rebeiz & Muldavin, 2001). Following are some typical examples of RF-MEMS switches' applications in each different category.

Reconfigurable antennas: Due to the good RF performances especially in high frequency range, RF-MEMS switches make the realization of reconfigurable antenna structures more efficient in terms of low insertion loss and small volumes. Some literatures have employed RF-MEMS switches and variable capacitors in reconfigurable antennas to control the resonant frequency, bandwidth, polarization, and radiation pattern (Topalli et al., 2009). For example, in 2006, two commercially available packaged RF-MEMS switches (SPST) were integrated with square spiral microstrip antennas to reconfigure the radiation pattern of the microstrip antenna between endfire and broadside over a common impedance bandwidth (Huff & Bernhard, 2006). And another similar work used four microstrip series capacitive RF-MEMS switches to monolithically integrate and package with a rectangular spiral antenna into the same substrate (both quartz and printed circuit board); finally, radiation patterns of the designed antenna for five different lengths of the spiral arm were obtained in a wideband frequency range (Jung, Lee, Li, & De Flaviis, 2006). In the work of (Topalli

et al., 2009), six RF-MEMS capacitive switches were used as loading elements on a slot antenna in order to tune its resonant frequency in a 1GHz range.

Tunable filters: For RF-MEMS capacitive switches, their properties of low loss, negligible DC power consumption, and excellent linearity make them to be a good candidate for wide-band tunable filter in microwave frequency range. A differential 4-bit 6.5-10-GHz RF-MEMS tunable filter using four capacitive RF-MEMS switches were introduced in (Entesari & Rebeiz, 2005), where the RF-MEMS switches were connected in series with high-Q metal-air-metal capacitors to make a capacitor bank and achieve a high tuning-resolution filter. Another work reported that a compact low-loss tunable X-band bandstop filter implemented on a quartz substrate using RF-MEMS capacitive switches; comparing with GaAs varactors, RF-MEMS switches can provide a much higher capacitance ratio which further can supply a wider filter tuning range (Reines, Park, & Rebeiz, 2010).

SPNT (Single-Pole-N-Throw) switches and switch matrices: The benefits of MEMS technology become more significant for SPNT switches and switch matrices; this is because both of them use lots of switching elements and any size and mass reduction of the switch would have a large impact on the entire device (Daneshmand & Mansour, 2011). Moreover comparing with conventional hybrid packaging techniques, using MEMS technology and developing monolithic packages would have less losses and better RF performance. For example, SP3T, SP4T and SP6T RF-MEMS switches were introduced in (Stehle et al., 2009) with broadband RF-behavior from 18GHz to 40GHz. In 2015, two extremely compact SPNT RF-MEMS switches based on symmetric circular topology, namely SP7T and SP11T, have been introduced; these switches can be used in compact and high performance switching networks for 3G and 4G networks (Yang, Yahiaoui, Zareie, Blondy, & Rebeiz, 2015). In 2016, a commercial product of

SP4T MEMS switch with integrated driver was promoted by Analog Devices[®] (Analog Devices, 2016), which can be operated in the frequency range of DC to 14GHz. A SPDT MEMS switch was developed by Omron[®] with actuation voltage of 34V and operated at frequency of 10GHz (Omron, 2013). A 2×2 RF-MEMS switch matrix (McErlean et al., 2005) for high power applications, a 3×3 RF-MEMS switch matrix (Daneshmand & Mansour, 2006) based on SP3T switches, and a 4×4 RF-MEMS switch matrix (Fomani & Mansour, 2009) which is suitable for construction of large switch matrices have been reported before; all of them were designed and fabricated by monolithic integration technique.

MEMS varactors: RF-MEMS capacitive switches can work as tuning elements such as MEMS varactors which are used in filters, phase shifters, or matching networks (Dussopt & Rebeiz, 2003); and the high linearity of the RF-MEMS switches can immensely reduce the related circuits' distortions or inter-channel interferences. Ylönen et al. proposed cantilever- and bridge-type varactor devices in 2006; both of them were fabricated by CMOS-compatible process; finally low loss, good matching and demonstrated reliability was obtained (Ylönen, Vähä-Heikkilä, & Kattelus, 2006). Another tunable capacitor application can be found in (Lee, Chen, Chi, Yu, & Kim, 2008), where two ZnO-actuated cantilevers supporting a big rectangular plate were created and the capacitance can be continuously tuned from 0.13pF to 1.82pF with applied voltages from -30V to +40V.

MEMS phase shifters: Microwave and millimeter-wave phase shifters are critical components in phased-array antennas for telecommunications and radar applications (Rebeiz, Tan, & Hayden, 2002). Comparing to the most conventional phase shifters based on p-i-n diodes or FET switches, MEMS switches result in lower loss phase shifters (almost 1/3 loss of the conventional phase shifters) at any frequency, especially

from 8GHz to 120 GHz (Rebeiz, Tan, & Hayden, 2002). During last fifteen years, there were many different kinds of RF-MEMS phase shifters proposed and developed. Basically they can be classified into following several topologies, namely switched-line phase shifter (Gong, Shen, & Barker, 2011; Jian, Wei, Chen, Yong, & Le, 2006; Kim, Hacker, Mihailovich, & DeNatale, 2001a; Tan, Mihailovich, Hacker, DeNatale, & Rebeiz, 2003b), distributed phase shifter (Barker & Rebeiz, 2000; Hayden & Rebeiz, 2003; Topalli, Civi, Demir, Koc, & Akin, 2008), reflection-type phase shifter (Gurbuz & Rebeiz, 2015; Lee et al., 2004; Malczewski, Eshelman, Pillans, Ehmke, & Goldsmith, 1999), high-pass low-pass phase shifter (Morton & Papapolymerou, 2008), loaded-line phase shifter (Puyal et al., 2008; Siegel, Zieglerl, Prechtel, Schonlinner, & Schumacher, 2007), as well as hybrid-topology phase shifter (Farinelli et al., 2009; Stehle et al., 2008). Each different topology has its own characteristics. For example the distributed phase shifters have very compact designs; the reflection-type phase shifters do not suffer from the high transmission-line loss; the loaded-line phase shifters result in excellent response for small phase delays; and the switched delay-line technique is the most popular and the easiest way to implement a digital phase shifter (Rebeiz, 2003b).

Other related applications: Except aforementioned applications, there are still some other RF systems using RF-MEMS switches. For example, a dual-band voltage control oscillator was introduced in (Kaynak et al., 2009), where a RF-MEMS capacitive switch was used and monolithic integrated into it. And RF-MEMS switch has also been employed in a dual-patch power amplifier (Kim, Hacker, Mihailovich, & DeNatale, 2001b) where two RF-MEMS switches were located at the input to guide the RF signal between two paths. For RF-MEMS switch with 20GHz, it can be used in the most of military communication systems, such as phase array radar or antenna (Kanzler and Benson, 2016).

All of these are the related applications which have employed RF-MEMS switches inside them in recent years. Figure 2.2 is an overview picture which has summarized most RF-MEMS switches' applications.

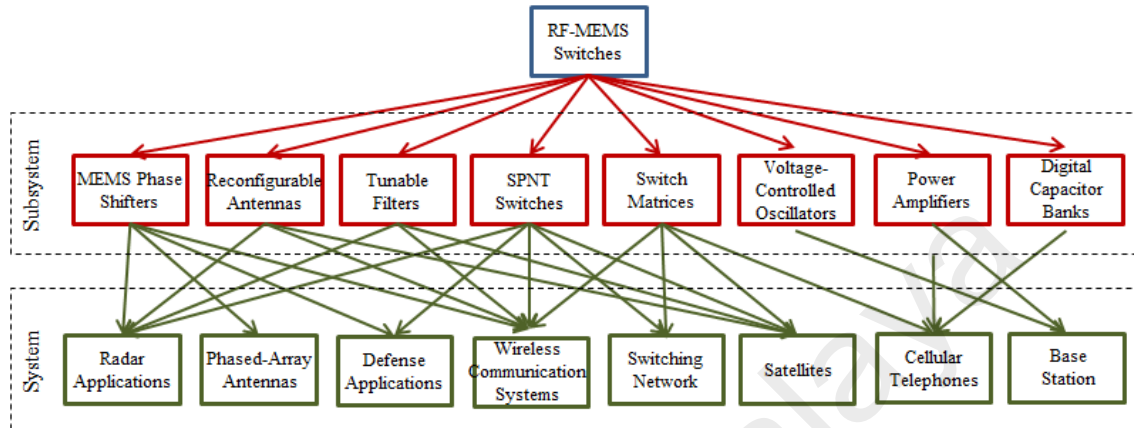


Figure 2.2: Applications of RF-MEMS switches

2.3 Multi-Response Optimization Method of RF-MEMS Switch Design

In order to determine the geometric dimensions of RF-MEMS switch's beams to achieve the switch's low-actuation voltage, short switching speed and robust vibration, a multi-response optimization is essential in this work. This is also a normal problem to be came across by the most RF-MEMS switches' design (Philippine, Sigmund, Rebeiz, & Kenny, 2013; Shalaby et al., 2009). The only difference from each work would be the optimized responses (e.g. switching speed, power handling capability or RF performance) (Badia, Buitrago, & Ionescu, 2012; Shalaby et al., 2009) or optimized parameters (e.g. geometric shapes or dimensions) (Gong, Zhao, Xin, Lin, & Bai, 2009; Peroulis, Pacheco, Sarabandi, & Katehi, 2003).

Some different methods have been used to conduct for multi-response optimization RF-MEMS switches before. For example, a general approach was used to predict the final optimum mechanical design in the work of (Huang et al., 2001), where the critical collapse voltage, residual stress, Q-factor and switching speed of a RF-MEMS

capacitive switch were considered as optimized responses; and bridge geometries were the optimized parameters. However, how to determine the compromise result between low critical collapse voltage and high switching speed was not illustrated. A metal-contact RF-MEMS switch was optimized in (Shalaby et al., 2009) for the purposes of small actuation voltage, short opening time, and large power handling capability, where the design variables were the cantilever's length, thickness, widths, and dimple size. A method of strength Pareto evolutionary algorithm was used for the multi-response optimization. A topology optimization method was used in (Philippine, Sigmund, Rebeiz, & Kenny, 2013) to systematically generate the size, shape, location of cutouts, and the overall structure for a capacitive RF-MEMS switch's membrane; the optimization responses are stress gradients and stress stiffening of the membrane. The power of topology optimization was demonstrated with a formulation which is used to find the design's compromise between stress, stiffening and curling (Philippine, Sigmund, Rebeiz, & Kenny, 2013). A 2-step optimization technique was employed in (Wang, Chow, Volakis, Saitou, & Kurabayashi, 2005) for a metal-contact RF-MEMS switch's dimple size, contact resistance, restoring force and beam geometry's optimization in order to achieve high power handling, low actuation voltage and short switch opening time. Among all of these previous papers, there is no work about RF-MEMS capacitive switch's low pull-in voltage, robust vibration and short switching time's optimization simultaneously. Moreover a time saving and easy implement multi-response optimization method is needed by most MEMS devices' optimization researchers.

In this project, a multi-response optimization method based on Taguchi method and weighted principal component analysis is first developed and introduced, which is an effective, easy understanding and implementation method for most engineering

researchers. An introduction of Taguchi method and weighted principal component analysis are detailed in the following sections.

2.3.1 Taguchi Method

Taguchi's parameter optimization is a kind of robust design method, which can be employed in a variety of problems. Taguchi defines robustness as the "insensitivity of the system performance to parameters that are uncontrollable by the designer" (Taguchi, Clausing, & Watanabe, 1987). A robust design incorporates this concept of robustness into design optimization and in order to obtain designs that optimize given performance measures while minimize sensitivities against uncontrollable parameters using different approaches, such as signal to noise ratio (Shalaby et al., 2009). Taguchi method can be used to determine the best parameters for the optimum design configuration with the least number of analytical investigations. Comparing with other optimization methods, such as genetic algorithm (GA) (Li, Su, & Chiang, 2003) or neural network (Meng & Butler, 1997), Taguchi method does not need much statistical or technical background in that specific field; and it can be easily implemented by different fields of engineering researchers (Liao, 2006; Roy, 2010).

Two main tools are used in the Taguchi method, namely; i) signal to noise ratio (S/N) which measures quality with emphasis on variation, and ii) orthogonal arrays (OAs) which accommodate many design factors (or parameters) simultaneously (Ghani, Choudhury, & Hassan, 2004). Taguchi method has been broadly used to improve the quality of manufactured goods, engineering, biotechnology, marketing and advertising; however, it has not been widely employed in the optimization of the RF-MEMS switches' dimensions.

The procedure to perform Taguchi method can be divided into following several steps. The first step is to determine the variable parameters which are going to be optimized and their possible values (or levels). The second step is to choose a proper OA according to the parameter's number and levels, and specify the levels of each parameter into the OA. Then, the simulations or experiments' performance according to the parameters' combination are carried out and recorded into the OA. Taguchi method divides the S/N characteristics into three categories, which are listed below (Fahsyar & Soin, 2012), namely (2.1) to (2.3). In the end, the optimized parameters' values are determined by their average S/N plots.

Smaller the better characteristic:

$$S/N = -10 \log_{10} \left(\frac{y_1^2 + y_2^2 + y_3^2 + \dots + y_n^2}{n} \right) \quad (2.1)$$

Nominal the best characteristic:

$$S/N = -10 \log_{10} \left[\frac{(y_1 - y_0)^2 + (y_2 - y_0)^2 + (y_3 - y_0)^2 + \dots + (y_n - y_0)^2}{n} \right] \quad (2.2)$$

Larger the better characteristic:

$$S/N = -10 \log_{10} \left[\frac{\frac{1}{y_1^2} + \frac{1}{y_2^2} + \frac{1}{y_3^2} + \dots + \frac{1}{y_n^2}}{n} \right] \quad (2.3)$$

Where, y_1, y_2 , etc. are the results of experiments, simulations or observations; y_0 is the target value of results; and n is the number of observations. For all of these characteristics, the largest S/N value is the most desirable condition (Roy, 2010).

Generally Taguchi method is good for single objective's optimization. For example, an actuation pulse was optimized in (Spasos, Tsiakmakis, Charalampidis, & Nilavalan, 2011) by Taguchi method for a purpose of achieving better switching condition. Taguchi method was utilized to optimize the milling parameters (namely cutting speed, feed rate and depth of cut); and the final optimization response is either better surface roughness or resultant force value in (Ghani, Choudhury, & Hassan, 2004).

Taguchi method can deal with the multi-response optimization which has same optimized result for every different optimized objective. However, if there are more than one objectives existing and the optimized variable parameters' setting for each objective is conflict, a compromise analysis is needed then further to determine the final optimized parameters' value with considering all the design objectives simultaneously. Therefore, Taguchi method itself will not be enough for normal multi-response optimization purpose.

2.3.2 Weighted Principal Component Analysis

In this project, a compromise analysis using weighted principal component analysis (WPCA) is proposed. WPCA basically is developed from principal component analysis. The principal component analysis is a well-known multivariate statistical method utilized for data reduction purpose. The basic idea is to represent a set of variables by a smaller number of variables known as principal components. It involves a mathematical procedure that reduces the dimensions of a set of variables by reconstructing them into uncorrelated combinations (Wu & Chyu, 2004). However, there are still some obvious limitations in the principal component analysis method. First, only the principal components with eigenvalues of larger than one are picked to be analyzed. Second, when more than one principal component is selected (or more than one principal

components' eigenvalue are larger than one), the required trade-off for a feasible solution is not defined. And third, the multi-response performance index cannot replace the multi-response solution while the chosen principal component can only be explained by total variation (Liao, 2006).

WPCA is a method based on principal component analysis while all principal components and their weights are taken into account. In order to wholly explain variation for all responses, WPCA uses the explained variation as the weight to combine all principal components into a multi-response performance index (MPI) for producing the further optimization results (Liao, 2006). Experimental results using WPCA have been reported by some literatures which can provide higher accuracy than the conventional principal component analysis (Fan, Liu, & Xu, 2011; Pinto da Costa, Alonso, & Roque, 2011).

In order to perform WPCA and obtain the MPI, a straightforward procedure needs to be carried out as explained in following. To begin with, utilizing (2.4) (Jaafar, Sidek, Miskam, & Korakkottil, 2009) normalizes the S/N value for every one of the response. The normalized value can get rid of the difference between diverse units and it should be located in the range of 0 to 1. Second, PCA is performed by using the normalized S/N values to obtain the values of explained variation for each response, the eigenvalues and eigenvectors of each principal component. Last step is to calculate MPI by (2.5), where all the principal components and their explained variations or weights are considered (Liao, 2006) in the equation.

$$x_i^*(j) = \frac{x_i(j) - x_i(j)^-}{x_i(j)^+ - x_i(j)^-} \quad (2.4)$$

Where, $x_i(j)$ means the S/N value of j th response at i th experiment number; $x_i(j)^+$ is the maximum value of $x_i(j)$ at j th response; and $x_i(j)^-$ is the minimum value of $x_i(j)$ at j th response; and $x_i^*(j)$ is the normalized response.

$$MPI = \sum_{j=1}^k W_j Z_j \quad (2.5)$$

Where, Z_j is the j th principal component which can be obtained by (2.6); W_j is the weight (or explained variation) of j th principal component; and k refers to the total response number.

$$Z_j = \sum_{i=1}^p a_{ji} x_i^*(j) \quad (2.6)$$

Where, a_{ji} is the eigenvector which satisfies the relation of $\sum_{i=1}^p a_{ji}^2 = 1$.

In the end, the optimized parameters' values can be determined by their average MPI plots, which is similar as the last step of the Taguchi method.

2.4 MEMS Phase Shifters

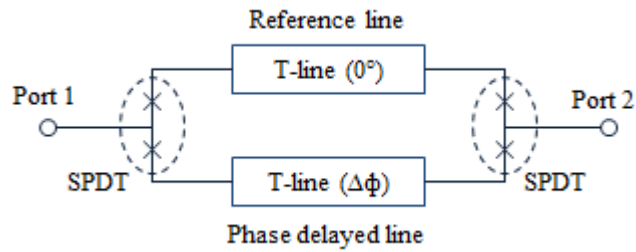
Phase shifters are devices which are employed to change transmission phase in a system; they can be constant phase changes called digital phase shifters or variable phase changes named analog phase shifters. RF phase shifters, as essential building blocks, can be used in many RF applications, such as phased array antennas in telecommunication and radar systems (Puyal et al., 2008), phase discriminators, beam forming networks, power dividers and linearization of power amplifiers (Rosu, I).

MEMS phase shifters comparing with conventional RF phase shifters which use GaAs (Gallium Arsenide) MOSFET (metal-oxide-semiconductor field effect transistor)

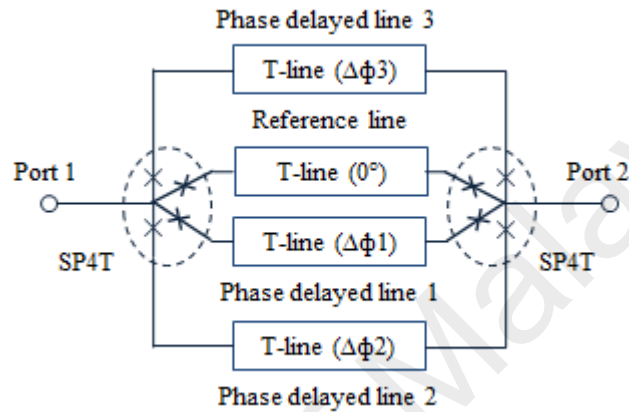
and p-i-n diodes, have lots of advantages, such as low insertion loss, negligible DC power consumption and excellent linearity which are thanks to the RF-MEMS capacitive switches' corresponding merits. According to the different categories of the MEMS phase shifters, as mentioned in section 2.2.3, the MEMS switched-line phase shifters and DMTL phase shifters are two kinds of the most prevalent topologies which employ the RF-MEMS switches inside.

2.4.1 MEMS Switched-Line Phase Shifter

MEMS switched-line phase shifter uses the RF-MEMS switches to control the signal passing through different length of T lines and generates a time delay difference among each direct path to provide desired phase shift. It is one of the most straightforward approach and the easiest way to implement a digital phase shifter. There are several works proposing the MEMS phase shifters by using the switched-line structure (Huang, Bao, Li, Wang, & Du, 2015) where RF-MEMS switches are used to direct electrical signal through either a short or long length of T line; and by different lengths of T lines, different phases are generated. Generally, there are two or more different signal pathways included; one of them is reference phase line and others are specified as different delayed phase lines. Figure 2.3 shows a two-path and a four-path switched-line phase shifter by using single-pull-double-throw (SPDT) switches and single-pull-four-throw (SP4T) switches, respectively. The T line can be designed with microstrip line or CPW line which depends on the whole circuit's requirement; and basically RF-MEMS switches can be integrated with either of them.



(a) 1-bit switched-line phase shifter by using SPDT switches



(b) 2-bit switched-line phase shifter by using SP4T switches

Figure 2.3: Topologies of switched-line phase shifter

Switched-line phase shifters are widely used since they can be easily designed, fabricated and integrated with other microwave devices; however most proposed designs need relatively high DC bias voltages, such as 30V in (Scardelletti, Ponchak, & Varaljay, 2002; Wang, Liu, & Li, 2010), 65V in (Malmqvist et al., 2010), 90V in (Huang, Bao, Li, Wang, & Du, 2015) and employ metal-contact RF-MEMS switch (Huang, Bao, Li, Wang, & Du, 2015; Malmqvist et al., 2010; Wang, Liu, & Li, 2010) which easily degrade the insertion loss with increased frequency band; additionally, in order to reduce the substrate losses, many MEMS phase shifters were developed on glass (Wang, Liu, & Li, 2010), quartz (Rizk & Rebeiz, 2003), GaAs (Malmqvist et al., 2010; Tan, Mihailovich, Hacker, DeNatale, & Rebeiz, 2003a) and RO4350 substrate (Huang, Bao, Li, Wang, & Du, 2015), which cannot be directly integrated with most standard CMOS control circuitry.

In order to integrate the designed MEMS phase shifter into remote phased array antennas or on-the-move communication systems, low-voltage supply with very little power consumption is an important consideration and big advantage comparing with using voltage-up converter or additional circuits to get high voltage supply to the phase shifter which leads to drive cost up a lot. On the other hand, proposing a MEMS phase shifter with low-enough loss can remove the power amplifier or low-noise amplifier level which is generally used in traditional RF phase shifter (Pillans et al., 2012), to reduce the chip cost and complexity. Therefore, in this project, a MEMS switched-line phase shifter with low-control voltage and low loss is proposed by using the optimized T-match RF-MEMS switch network with CPW line, which will be detailed in chapter 3.

2.4.2 DMTL Phase Shifter

DMTL (distributed MEMS transmission line) phase shifter is realized by using a high-impedance T line (normally its characteristic impedance is larger than 50Ω) with periodically loaded capacitive MEMS bridges on it. This can be done with a variety of types of T lines; however, it is most easily constructed by using CPW line, especially for shunt capacitive RF-MEMS switches (Barker & Rebeiz, 2000). The RF-MEMS switches act as shunt capacitors or varactors. By applying bias voltage to the RF-MEMS switches, the distributed capacitive loading on the T line is increased which makes the phase velocity of the T line decreasing, thus providing a different phase shift. Figure 2.4 shows a 1-bit K/Ka-band phase shifter which is constructed by a CPW line and eleven shunt capacitive RF-MEMS switches (Borgioli, Liu, Nagra, & York, 2000).

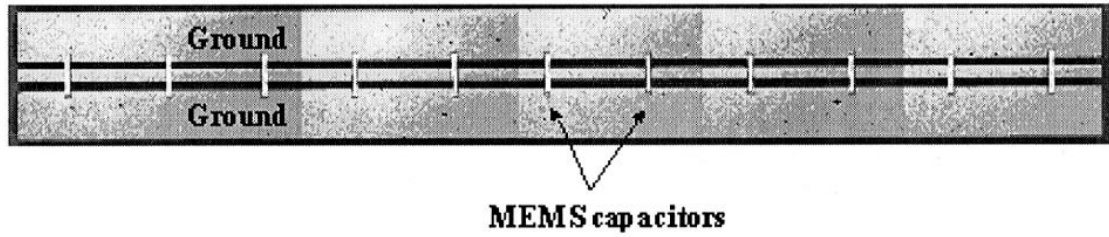


Figure 2.4: A one-bit DMTL phase shifter consists by CPW and eleven shunt capacitive RF-MEMS switches (Borgioli, Liu, Nagra, & York, 2000)

Regarding to DMTL phase shifter, there are some important basic concepts and theories need to be studied first before the designing work, as explained following.

A. Characteristic impedance of the T line

Characteristic impedance is a very important property for T lines and it can be obtained from the T line's equivalent lumped-element circuit. The T line can be classified as unloaded T line and loaded T line. For a pure lossless CPW line which is used for DMTL, if there are no any loads applied on it, its characteristic impedance can be calculated by $\sqrt{L_t/C_t}$, where L_t and C_t is the inductance and capacitance per unit length of the CPW T line and can be obtained by (2.7) and (2.8) (Barker & Rebeiz, 2000).

$$C_t = \frac{\sqrt{\epsilon_{eff}}}{cZ_0} \quad (2.7)$$

$$L_t = C_t Z_0^2 \quad (2.8)$$

Where, Z_0 and $\epsilon_{eff} (= (\epsilon_r + 1)/2)$ is the characteristic impedance and effective dielectric constant of the unloaded T line; ϵ_r is the dielectric constant of the T line's substrate; and $c (= 3 \times 10^8 \text{ m/s})$ is the free-space velocity.

When the CPW line is periodically loaded with RF-MEMS capacitive switches, the characteristic impedance of the T line is named as loaded characteristic impedance and the equivalent lumped-element circuit can be modeled as shown in Figure 2.5. If the CPW is assumed as a lossless T line (namely $R_t=0$) while L_b and R_b of the MEMS switches are neglected, the characteristic impedance of the loaded CPW line can be estimated by (2.9) (Barker & Rebeiz, 1998).

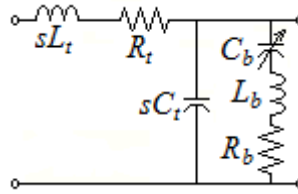


Figure 2.5: Equivalent lumped-element model for a periodically loaded CPW line

$$Z_l = \sqrt{\frac{sL_t}{sC_t + C_b}} \quad (2.9)$$

Where, Z_l is the loaded characteristic impedance; s is periodic spacing between each two switches; and C_b is the capacitance of the RF-MEMS switches (when the bridge is at up-state position, C_b equals to C_u ; when the bridge is actuated at down-state position, C_b equals to C_d).

B. Bragg frequency

Bragg frequency is a frequency at which the characteristic impedance of the T line goes to zero, indicating no power transfer, which can be calculated by (2.10) (Rebeiz, 2003c). It also can be understood as a cutoff frequency of distributed structures when the guided wavelength approaches the distributed periodic spacing (Tan, Mihailovich, Hacker, DeNatale, & Rebeiz, 2003a). In the case of the DMTL, the up-state LC resonant frequency of the MEMS bridge is very high (300GHz~600GHz), and thus the

DMTL's operation is generally limited by the Bragg frequency of the loaded line (Rebeiz, 2003c). From (2.10), it can be concluded that for the same T line the Bragg frequency of the loaded line would be low with the large MEMS-bridge capacitance. Therefore, for the design of DMTL phase shifter, the employed capacitance of the MEMS bridge cannot be too big. For example, in order to get a DMTL with minimum Bragg frequency of 50GHz, periodic spacing of longer than 300 μ m and standard unload impedance of 50 Ω (Shea et al., 1971), the MEMS bridge capacitance must be less than 268fF, 451fF and 492fF for silicon, glass and quartz substrates, respectively.

$$f_B = \frac{1}{\pi \sqrt{sL_t(sC_t + C_b)}} \quad (2.10)$$

Where, f_B is the Bragg frequency.

For the MEMS switch's modeling as shown in Figure 2.6, if its inductance value (L_b) is large enough to have a noticeable effect on the DMTL's performance, while the effect of the resistance (R_b) is almost negligible, the Bragg frequency can be estimated by (2.11) to (2.14) (Barker & Rebeiz, 2000).

$$f_B = \frac{1}{2\pi} \sqrt{\frac{b - \sqrt{b^2 - 4ac}}{2a}} \quad (2.11)$$

$$a = s^2 L_t C_t L_b C_b \quad (2.12)$$

$$b = s^2 L_t C_t + s L_t C_b + 4 L_b C_b \quad (2.13)$$

$$c = 4 \quad (2.14)$$

For example, if a DMTL with unloaded impedance of 50 Ω ; the MEMS bridge has equivalent capacitance of 120fF and inductance of 10pH to 50pH; and the whole

structure is created on quartz substrate; then the Bragg frequency of the DMTL is obtained as 93.4GH to 57.7GHz which is decreased with the MEMS bridge's inductance increasing.

C. Line loss

The loss of a DMTL mainly comes from two sources: one is the unloaded T line's own loss and the other one is from the capacitive loads or MEMS bridges. When the capacitance of the MEMS bridges is changing, the impedance of the DMTL is also varied which results in the change of the T line loss due to a change in the amount of current in the T line for the same amount of transmitted power.

If a T line is modeled by a series inductance (L_t) and resistant (R_t) per unit length, and by a shunt capacitance (C_t) and admittance (G_t) per unit length, respectively, its loss (α_1) can be calculated by (2.15) (Rebeiz, 2003d). For a CPW line, R_t represents the conductor loss and G_t represents the dielectric loss; and if the DMTL's substrate has low loss at mm-wave frequencies, the T line's main loss comes from the conductor loss (Rebeiz, 2003d). The loss of the MEMS bridge (α_2) can be calculated by (2.16) (Rebeiz, 2003d). Therefore, the total loss per section for DMTL (α) can be estimated by (2.17) (Rebeiz, 2003d); as it can be seen that the maximum total loss per section of DMTL can be obtained when the MEMS switches are actuated and C_b equals to C_d .

$$\alpha_1 = \frac{R_t}{2Z_l} + \frac{G_t Z_l}{2} \approx \frac{R_t}{2Z_l} \quad (2.15)$$

$$\alpha_2 = \frac{R_b Z_l \omega^2 C_b^2}{2} \quad (2.16)$$

$$\alpha = \alpha_1 + \alpha_2 = \frac{R_t}{2Z_l} + \frac{R_b Z_l \omega^2 C_b^2}{2} \quad (2.17)$$

Where, Z_l is the loaded impedance of the T line or DMTL's impedance; ω is the operation frequency of the DMTL.

D. Time delay and phase velocity

The time delay (τ) per section of the DMTL can be calculated by using (2.18) and model of Figure 2.5, where the loaded T line is assumed as a lossless line (namely R_t is neglected) (Rebeiz, 2003c). From this equation, it can be seen that: i) by changing the load capacitance, the time delay of the DMTL will change; and when the MEMS bridge's capacitance is increased, the time delay becomes longer. ii) The DMTL's time delay has relationship with its Bragg frequency; for a large Bragg frequency design, the time delay is small.

$$\tau = \sqrt{sL_t(sC_t + C_b)} \left(1 + \frac{\omega^2}{6\omega_B^2} + \dots \right) \approx \sqrt{sL_t(sC_t + C_b)} (\text{for } f \ll f_B) = \frac{1}{\pi f_B} \quad (2.18)$$

Then phase velocity (v_p) of the DMTL can be calculated by the periodic spacing (s) divided by the time delay as shown in (2.19). It also can be estimated using the substrate effective dielectric constant as shown in (2.20) (Rebeiz, 2003c).

$$v_p = \frac{s}{\tau} = s\pi f_B \quad (2.19)$$

$$v_p = \frac{c}{\sqrt{\epsilon_{eff}}} \quad (2.20)$$

2.5 CPW Line and Its Discontinuity

The proposed RF-MEMS capacitive switch is developed on a CPW line; moreover the RF-MEMS capacitive switches, CPW lines, CPW's right-angle bends and Tee junctions are employed in the design of MEMS phase shifters. Therefore, in this section, the CPW line and its discontinuities are studied briefly.

2.5.1 CPW Line

CPW was invented by Cheng P. Wen in 1969, which is a type of electrical transmission line and can be used to convey microwave-frequency signals. CPW is formed by a center strip of thin metallic film deposited on the surface of a dielectric slab with two ground electrodes running adjacent and parallel to the strip on the same surface (Wen, 1969), as shown in Figure 2.6. The structure is obviously symmetrical along a vertical plane running in the middle of the central strip. Comparing with conventional microstrip design, CPW has several advantages (Becks & Wolff, 1993), such as: i) no via holes are needed to connect active devices with the ground conductor; ii) low dispersion of the propagation constant and the characteristic impedance is for the coplanar mode (even mode); iii) variation of the slot and strip width offers two degrees of freedom, once the substrate height is chosen, which makes its connection of external shunt capacitive switch to become easy. It is also ideal for connecting various elements in monolithic microwave integrated circuits built on semiconducting substrates or ferromagnetic semiconductors (Wen, 1969). The only drawback of CPW line is that the parasitic coupled slot-line mode (odd mode) is excited by electrically or geometrically nonsymmetrical CPW discontinuities, such as bends and Tee-junctions (Becks & Wolff, 1993). Grounded coplanar waveguide (GCPW) is another type of CPW; its difference

from the classic CPW is a ground plane covered the entire back-face of the substrate. GCPW is usually used as an alternative to microstrip line.

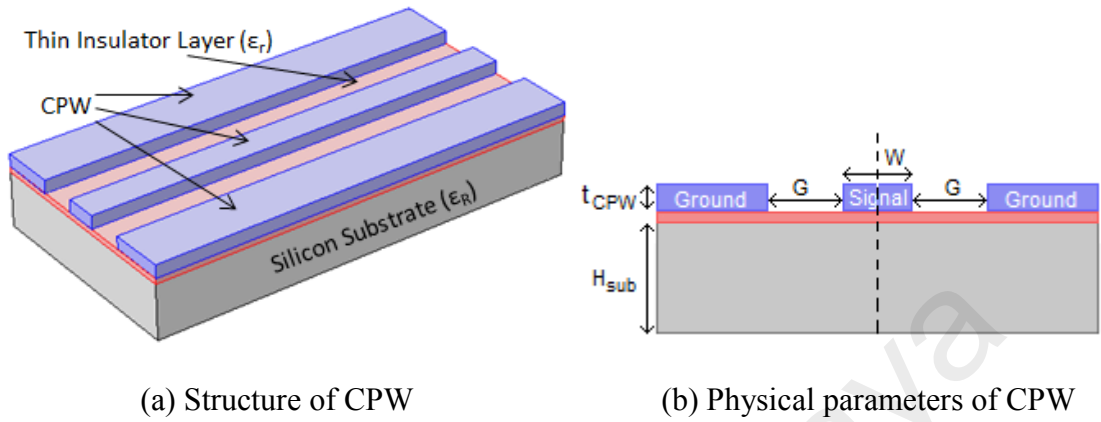


Figure 2.6: CPW with its physical parameters

The characteristic impedance, effective dielectric constant and attenuation of the CPW line are determined by the dimensions of the center strip, the gap, the thickness and permittivity of the dielectric substrate. A CPW can be quasi-statically analyzed by using the method of conformal mappings; and the equations to calculate the characteristic impedance of CPW (Z_0) are summarized in (2.21) to (2.26) (Alexandrou, Sobolewski, & Hsiang, 1992 ;Wen, 1969).

$$Z_0 = \frac{30\pi}{\sqrt{\epsilon_{eff}(f)}} \frac{K'(k)}{K(k)} \quad (2.21)$$

$$K'(k) = K(\sqrt{1-k^2}) \quad (2.22)$$

$$k = W / (W + 2G) \quad (2.23)$$

$$\sqrt{\epsilon_{eff}(f)} = \sqrt{\epsilon_q} + \frac{(\sqrt{\epsilon_r} + \sqrt{\epsilon_q})}{\left[1 + a \left(\frac{f}{f_{cutoff}}\right)^{-b}\right]} \quad (2.24)$$

$$\varepsilon_q = \frac{\varepsilon_r + 1}{2} \quad (2.25)$$

$$f_{cutoff} = \frac{c}{4H_{sub}\sqrt{\varepsilon_r - 1}} \quad (2.26)$$

Where, Z_0 is the characteristic impedance of the CPW line; $K(k)$ and $K'(k)$ is the complete elliptic integral of the first kind and its complement; W is the CPW's center conductor width; G is the CPW's gap between the center conductor and ground plane; H_{sub} is the thickness of the substrate; ε_r is the dielectric constant of the substrate; a and b are geometry dependent parameters; f_{cutoff} is the cutoff frequency; and c is the speed of the light in vacuum.

Except this formula method to calculate the characteristic impedance of the CPW, nowadays, a much easier and faster way to obtain the CPW's characteristic impedance is by the software or calculator, such as TXLINE 2003[®] or Agilent CAD tool[®]. Generally, once the substrate thickness and dielectric permittivity (or choosing the substrate material), the gap between the signal line and the ground plane, the width and thickness of the signal line, operation frequency and the CPW's material is identified, the characteristic impedance of the CPW can be obtained directly. Moreover, the effective dielectric constant and line loss can be calculated together. This method will be illustrated in Chapter 3.

2.5.2 CPW Discontinuity

CPW is a kind of transmission line with two slots coupled by the central conductor as aforementioned. When the wavelength of the signal current is larger than the slot length, any asymmetric geometry between the two slots could produce some parasitic effect,

such as right-angle bend or Tee junction, which also can be called CPW discontinuity. In this case, electric field waves propagate through two slots experience path difference at the discontinuity or bending point which causes the phase difference; and the electric fields between the two ground planes become unequal which creates finite potential difference (v_1-v_2) between two isolated ground planes, as shown in Figure 2.7 (Abuwasib, 2011). This unequal ground potential excites parasitic mode (or slot-line mode) which could be coupled with the desired CPW mode propagating throughout the circuit (Abuwasib, 2011), and degrade the performance of the CPW's right-angle bend or Tee junction.

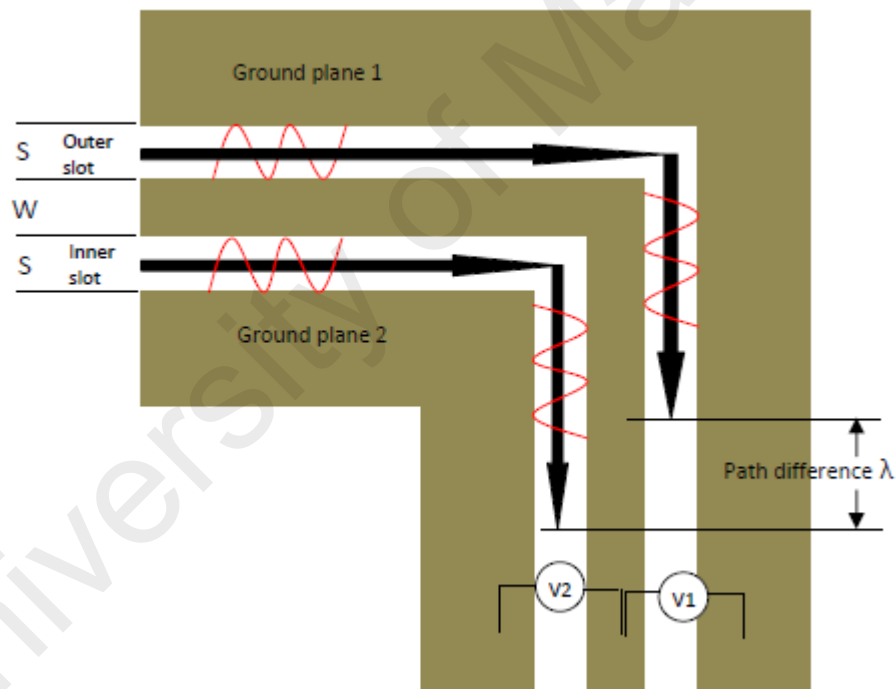


Figure 2.7: Path difference of electric field wave (red) between inner and outer slot after bending (Abuwasib, 2011)

In order to get rid of this effect for the CPW's right-angle bend, some different methods have been introduced to improve their performance, such as chamfering the outside corner of the signal conductor (Watson & Gupta, 1997), introducing dielectric overlays at the interior corner (Simons & Ponchak, 1988), and adding an air-bridge or

wire bonding between two ground planes which is the most common method to equalize the potential of the isolated ground planes (Wu, Deng, Wu, & Hsu, 1995). For the technique of signal line's outside corner chamfering, there is no a full design methodology available yet. For dielectric overlays at the interior corner, it is not suitable for monolithic-microwave integrated circuit applications. For wire bonding, it has negligible insertion loss; however, it can equalize potential only at the place where it is connected (Abuwasib, 2011). Normally for high frequency transmission line, voltage and current waves vary spatially through CPW structure, equalizing the ground potential using small bonding wire only neutralize the offset ground potential locally at that point; if unequal ground potentials come from bending and discontinuities of the CPW, then in order to equalize this it is required to put the air-bridge at the point of bending or discontinuity (Simons, 2004). Long air-bridge, as used in (Abuwasib, 2011), can equalize the potential throughout the structure well but it has large insertion loss. This is because the long air-bridge results in large bridge capacitance which causes a big undesired reflection from the point where it is connected. The short air-bridges can suppress the excitation of the coupled slot-line mode in laterally asymmetric geometries such as CPW's right-angle bend or Tee junction. However, the added air bridge introduces an additional shunt capacitance to the CPW line which causes an undesired reflection from the point where it is connected and increases the insertion loss of the CPW line. Although this drawback can be improved by reducing the width of the signal conductor or increasing the height of the air-bridge, it still may not provide enough compensation for the air-bridge's coupling capacitance. Moreover the height of air-bridge is usually limited by fabrication process.

So far, a better way to solve this problem is using air-bridges with a section of high-impedance T line to improve the performance of the CPW's discontinuity (Weller et al.,

2000). By calculating and optimizing the high-impedance T line's dimension, it can compensate the air-bridge's capacitance well.

Therefore, in this project, the technique of short air-bridge with high-impedance T-line section for equalizing the grounds' potential of CPW's discontinuity is employed. As shown in Figure 2.8, it is a CPW's right-angle bend where two air-bridges are used to equal the asymmetric ground planes' potential and the high-impedance T-line section between them is used for compensating the bridges' coupling capacitance. According to Thomas et al.'s derivation in (Weller et al., 2000), the high-impedance T-line section can minimize the reflection coefficient and its length can be calculated by (2.27).

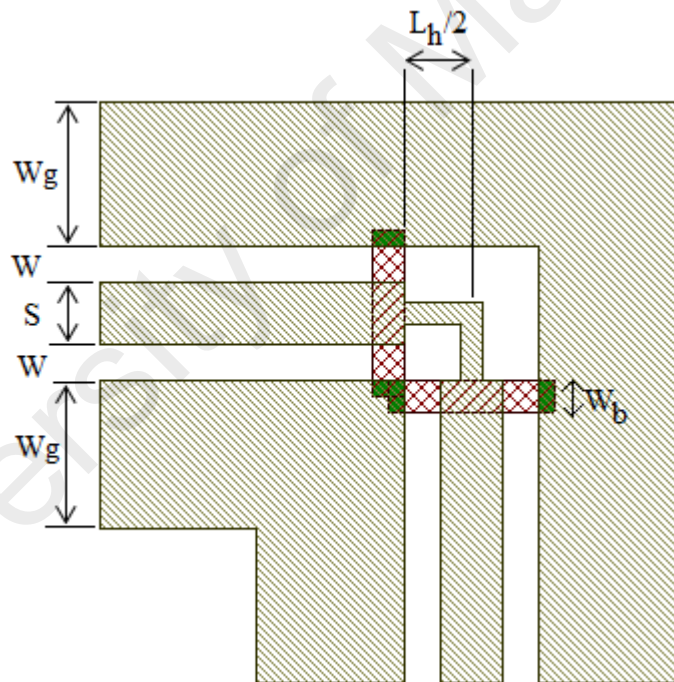


Figure 2.8: CPW's right-angle bend with air-bridges for potential equalization and high-impedance for capacitance's compensation

$$L_h = \frac{c}{\sqrt{\epsilon_{eff}}} \frac{2Z_h Z_0^2 C_{bridge}}{Z_h^2 - Z_0^2} \quad (2.27)$$

Where, L_h and Z_h is the length and impedance of the high-impedance T-line section, respectively; Z_0 is the nominal CPW impedance outside the step section; C_{bridge} is the

capacitance of the air-bridge; c is the speed of light; and ϵ_{eff} is the effective dielectric constant of the high-impedance section (for silicon substrate, $\epsilon_{eff}=6.2$). This equation also assumes that the high-impedance T-line section is uniform and extends up to the edge of each air-bridge, and it does not account for parasitics, which are inherent to the bend itself (Weller et al., 2000).

For the design of CPW Tee junction, there were two common methods mentioned in the previous papers (Becks & Wolff, 1993; Naghed, Rittweger, & Wolff, 1991; Rittweger et al., 1991) as shown in Figure 2.9. One design (type A - left Tee junction of Figure 2.9) includes three simple air bridges suspending above the signal conductor to suppress the parasitical odd mode (or slot-line mode) excitation. The other one (type B - right Tee junction of Figure 2.9) has a T shape suspending bridge which is a part of the signal conductor and closed ground metallization. It is obvious that the coupling capacitance of type B Tee junction is larger than type A since the overlapping area is larger; therefore type B's reflection coefficient increase faster than the type A's. However, both structures have no compensation techniques for the excessive coupling capacitance between the bridges and the signal conductor (or ground plane). As explained in the previous part, the coupling capacitance will cause undesired reflection for Tee junction and degrade the performance of the CPW discontinuity.

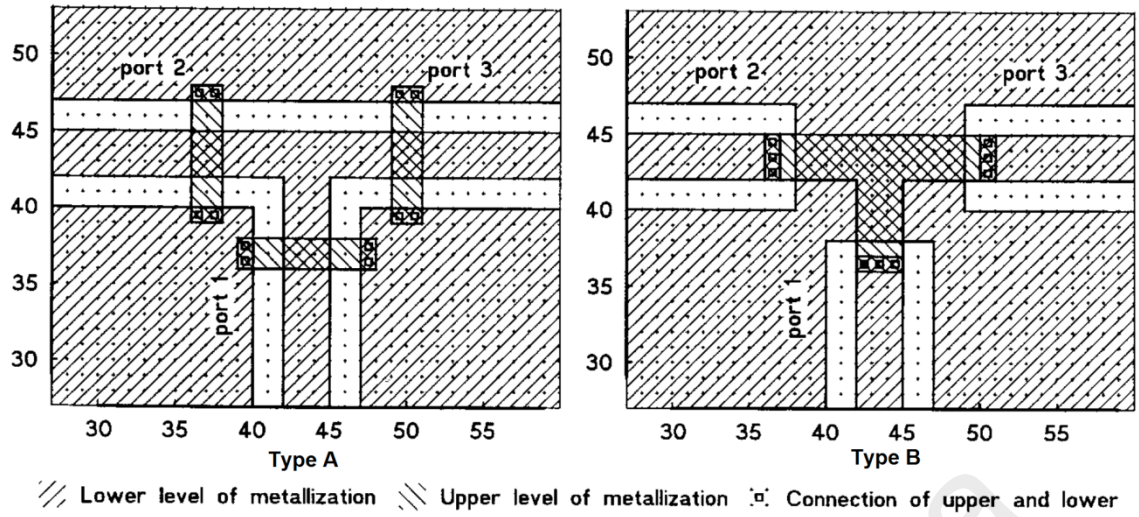
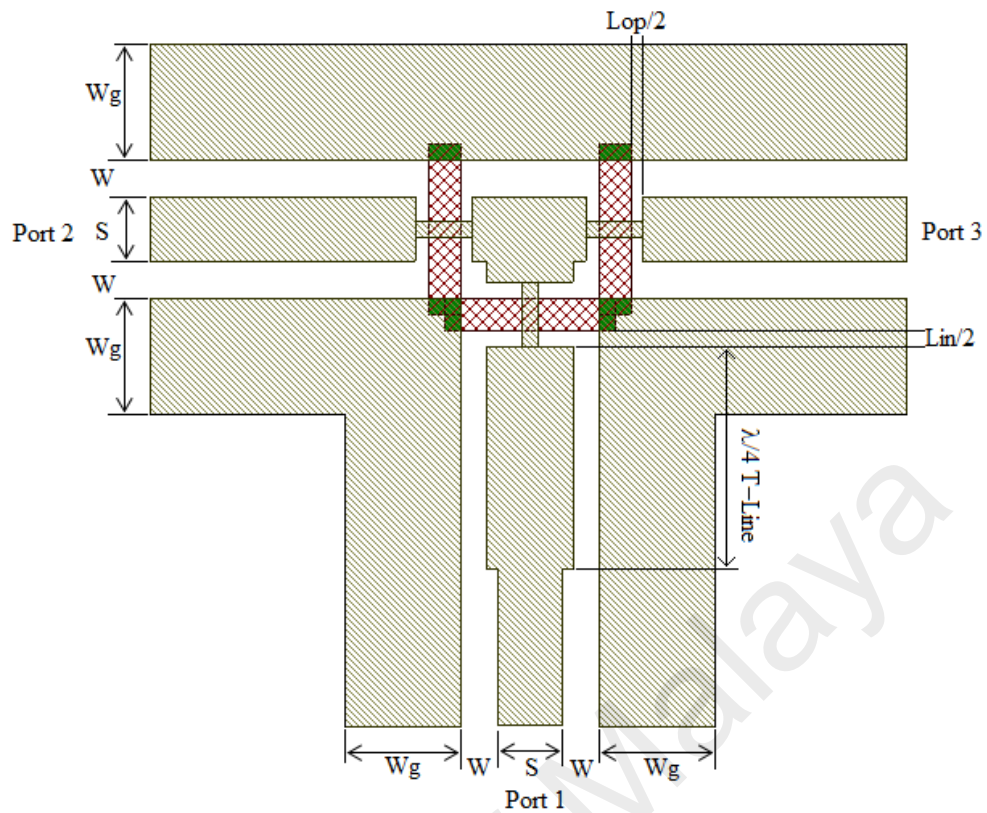


Figure 2.9: Two common structures of air-bridge CPW Tee junctions (Becks & Wolff, 1993)

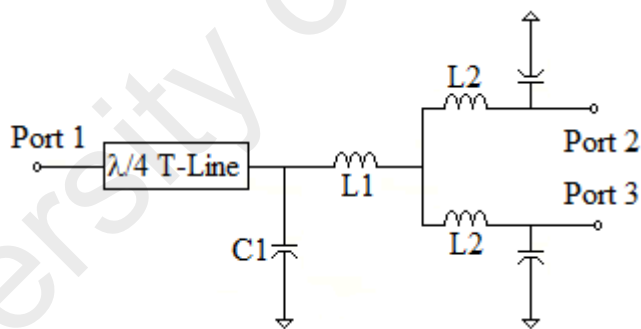
A better way to design CPW Tee junction was presented in (Weller et al., 2000), as shown in Figure 2.10. From Figure 2.10 (a), it can be seen that the CPW Tee junction consists of three air-bridges suspended above the signal conductor, three sections of high-impedance T line to compensate the coupling capacitance of the air-bridges, and a quarter-wavelength impedance transformer to obtain an impedance match with an equal impedance presented at all three ports. Figure 2.10 (b) is the equivalent circuit of the CPW Tee junction, which can be used to investigate its parasitic effects. The length of the high-impedance T-line section can be estimated by (2.28) (Weller et al., 2000).

$$L = \frac{c}{\sqrt{\epsilon_{eff}}} \cdot \frac{Z_h Z_0^2 C_{bridge}}{Z_h^2 - Z_0^2} - 0.7W_b \quad (2.28)$$

Where, L is the length of the high-impedance T-line section which can be L_{in} or L_{op} in Figure 2.10 (a); Z_h is the impedance of the high-impedance T-line section; Z_0 is the nominal CPW impedance outside the step section; C_{bridge} is the capacitance of the air-bridge; c is the speed of light; ϵ_{eff} is the effective dielectric constant in the high-impedance section (for silicon substrate, $\epsilon_{eff}=6.2$); and W_b is the width of the air-bridge.



(a) Design structure



(b) Equivalent circuit

Figure 2.10: Tee-junction CPW with air-bridges, high-impedance compensation and a quarter-wave impedance (Weller et al., 2000)

2.6 Summary

In this chapter, some important concepts and theories related to this project have been reviewed and studied. RF-MEMS switch's classifications, state-of-the-art designs and applications were presented which further were used to determine the design specifications in next chapter. The multi-response optimization method, Taguchi

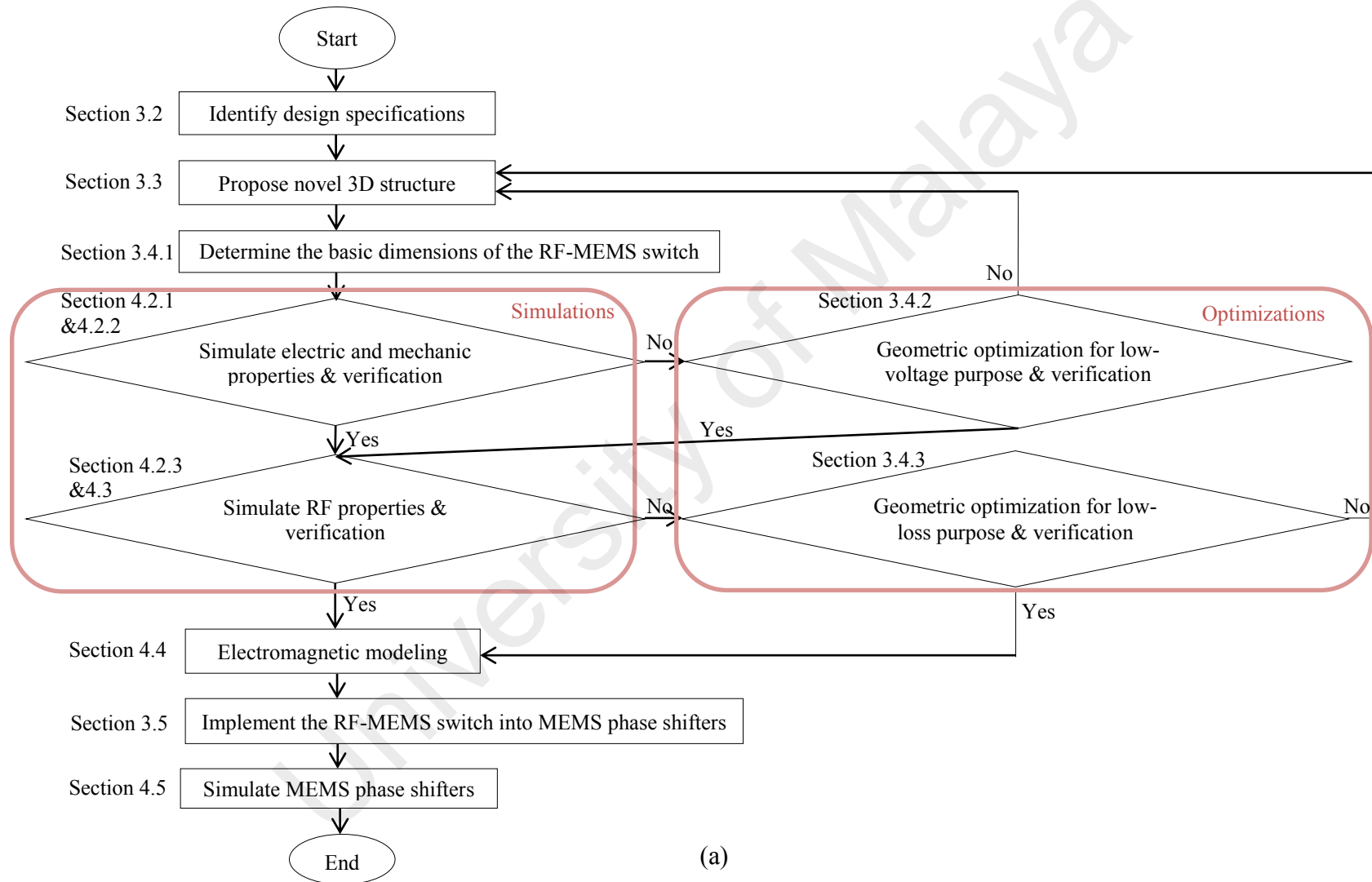
method, and weighted principal component analysis was reviewed. Comparing with other optimization methods, the multi-response optimization based on Taguchi method and weighted principal component analysis is an effective, easy understanding and implementation method for most engineering researchers which will be detailed in the Chapter 3. As one of the most important RF-MEMS switch's applications, MEMS phase shifters were studied; MEMS switched-line phase shifters and DMTL phase shifters were emphasized which will be the small applications of the developed RF-MEMS switch in this work and presented in the next chapter. In order to implement the MEMS phase shifters, CPW line and its discontinuity were used; here their theory and design methods were deliberated.

CHAPTER 3: RESEARCH METHODOLOGY

3.1 Introduction

Figure 3.1 (a) illustrates the methodology of this project, which mainly includes seven steps, namely i) identify the design specifications as explained in section 3.2, ii) propose a novel 3D structure design as described in section 3.3, iii) determine and optimize the RF-MEMS switch's dimensions as detailed in section 3.4, iv) simulate the RF-MEMS switch as presented in section 4.2 and 4.3; v) develop the RF-MEMS switch's electromagnetic modeling as described in section 4.4; vi) implement the developed RF-MEMS switches into MEMS phase shifters, as shown in section 3.5; and vii) simulate the MEMS phase shifters in section 4.5. For the determination and optimization of the RF-MEMS switch's geometric dimensions, its flow is explained in Figure 3.1 (b) which includes that: i) determining the basic dimensions, ii) optimizing the beams for low-voltage purpose, and iii) optimizing the high-impedance line for low-loss purpose. The simulation types and content of the RF-MEMS switch include static simulations (e.g., spring constant, pull-in voltage, residual stress, capacitance, and so on), dynamic simulations (e.g., switching time and pull-in voltage under dielectric charging effect) and RF performance (e.g., S parameters, operation frequency, switching impedance and power handling) as illustrate in Figure 3.1 (c). Figure 3.1 (d) presents the flow of implementation of the RF-MEMS switch into MEMS phase shifters.

In this chapter, the design specifications, device description, working principle, mechanical modeling, geometric dimensions' determination and optimization, as well as the implementation of the RF-MEMS switches into MEMS phase shifters are explained in detail.



(a)

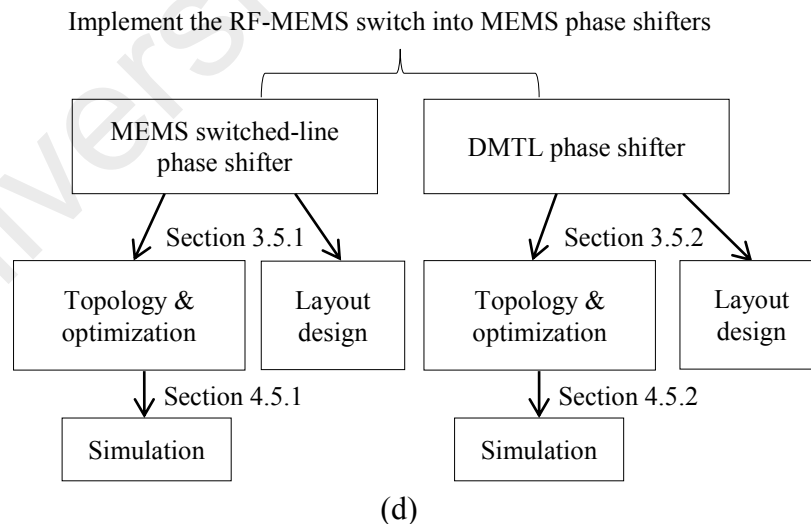
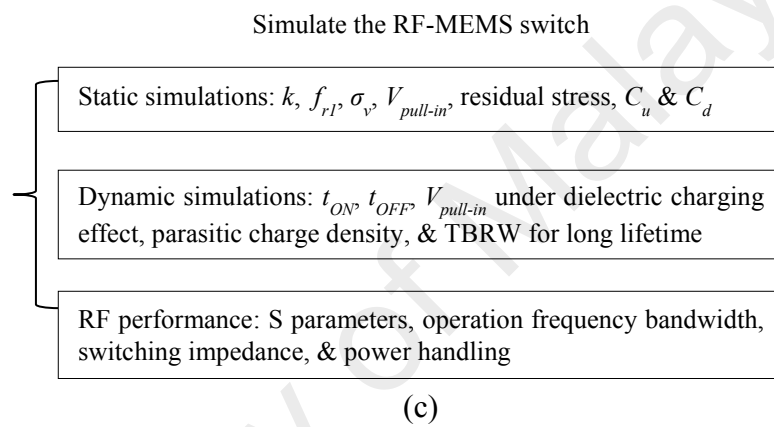
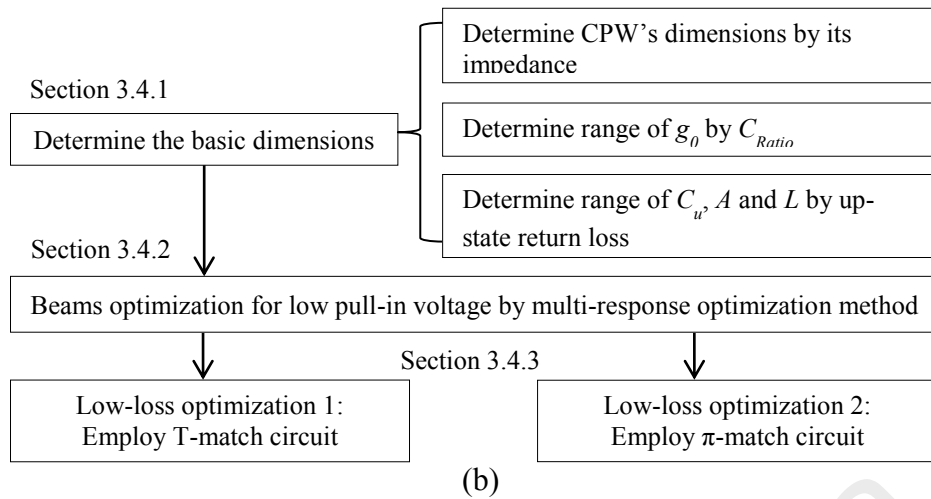


Figure 3.1: Schematic diagram of the project's methodology: (a) overall flow chart, (b) geometric dimensions' determination and optimization, (c) simulate the RF-MEMS switch, (d) implement the RF-MEMS switch into MEMS phase shifters

3.2 Identify Design Specifications

A well designed RF-MEMS switch should demonstrate several good characteristics including low actuation voltage, high switching speed, low loss, high isolation, high reliability (Mahameed, Sinha, Pisani, & Piazza, 2008), and simple fabrication steps in order to reduce the chip cost. Lots of the switches which were proposed in the literature have presented with some of these characteristics, such as high-isolation RF-MEMS capacitive switch in (Muldavin & Rebeiz, 2000), low-loss RF-MEMS switch in (Yao, Chen, Eshelman, Denniston, & Goldsmith, 1999), low-voltage RF-MEMS switch in (Guo et al., 2003), RF-MEMS switch which was fabricated by CMOS process (Dai, Peng, Liu, Wu, & Yang, 2005). However few of them focus on designing a low-voltage and low-loss RF-MEMS switch by CMOS-compatible process. Low-actuation voltage, low loss and CMOS process compatibility has become a major concern as more and more MEMS technology, especially for wireless MEMS device, is being integrated to a single chip (Lakamraju & Phillips, 2008) to reduce the cost, size, complexity and losses. Different applications usually have different requirements, specifications or characteristics, which is really difficult to satisfy all features in one device.

In this research, the goal of this work is to develop an electrostatic-actuated RF-MEMS switch with low loss and low-actuation voltage using CMOS-compatible and MEMS technology. Table 3.1 lists the design specifications in detail. Here the designed actuation voltage (or pull-in voltage) of the RF-MEMS switch is aimed to be as low as 3.3V since it is compatible with most standard CMOS IC's supply voltage (Chow, Wey, & Huang, 2004; Kuwabara et al., 2006; Yusoff, Zollfakar, Aman, & Ahmad, 2004; Analog Devices, 2016), so that the designed RF-MEMS switch can be directly integrated with the standard CMOS IC. Choosing electrostatic-actuation mechanism is because that i) it is one of the most popular technique in use today, as mentioned in section 2.2.2; ii) comparing with thermal, electromagnetic or other kinds of actuation

mechanisms, electrostatic-actuated RF-MEMS switch has negligible DC power consumption, relatively high switching speed, small design area, and the good compatibility with standard IC process (Angira & Rangra, 2015; Ma, Nordin, & Soin, 2015). Using shunt-type connection is because that the suspended electrode in shunt connection is fixed by two sides which is easier to be kept in flat than the one side fixed in series-type connection, especially for the big-membrane design. Selecting the capacitive RF-MEMS switch is because that compared to the metal-contact RF-MEMS switch, it has less stiction problem and can work for larger frequency range (Brown, 1998). An up-state return loss of less than -10dB can ensure a good input matching of the RF-MEMS switch at switch-on state (Rebeiz, 2003e). The insertion loss of higher than -1dB (Badia, Buitrago, & Ionescu, 2012; Fouladi & Mansour, 2010; Kim, 2012; Persano et al., 2012) and isolation of less than -15dB (Badia, Buitrago, & Ionescu, 2012; Fouladi & Mansour, 2010; Persano et al., 2012) are the acceptable RF performance ranges for the most capacitive RF-MEMS switches which can be further implemented into other RF circuits. Large capacitance ratio (namely, larger than 40) is conducive to produce a good RF performance (Rebeiz, 2003a). The acceptable ranges of switching time and power handling for the RF-MEMS switch is 1 to 300 μ s and less than 1W, respectively (Rebeiz, 2003a).

Table 3.1: Design specifications

| Parameter | Value (or Type) |
|-----------------------------------|---|
| Pull-in voltage ($V_{pull-in}$) | $\leq 3.3V$ (Kuwabara et al., 2006; Yusoff, Zolfakar, Aman, & Ahmad, 2004; Analog Devices, 2016) |
| Actuation mechanism | Electrostatic |
| Circuit configuration | Shunt connection |
| Contact type | Capacitive contact |
| Up-state return loss | $< -10dB$ (Rebeiz, 2003e) |
| Insertion loss | $> -1dB$ (Badia, Buitrago, & Ionescu, 2012; Fouladi & Mansour, 2010; Kim, 2012; Persano et al., 2012) |
| Isolation | $< -15dB$ (Badia, Buitrago, & Ionescu, 2012; Fouladi & Mansour, 2010; Persano et al., 2012) |
| Fabrication process | CMOS-Compatible & MEMS Surface Micromachining |
| Capacitance ratio | > 40 (Rebeiz, 2003a) |
| Switching time | $1 \sim 300\mu s$ (Rebeiz, 2003a) |
| Power handling | $< 1W$ (Rebeiz, 2003a) |

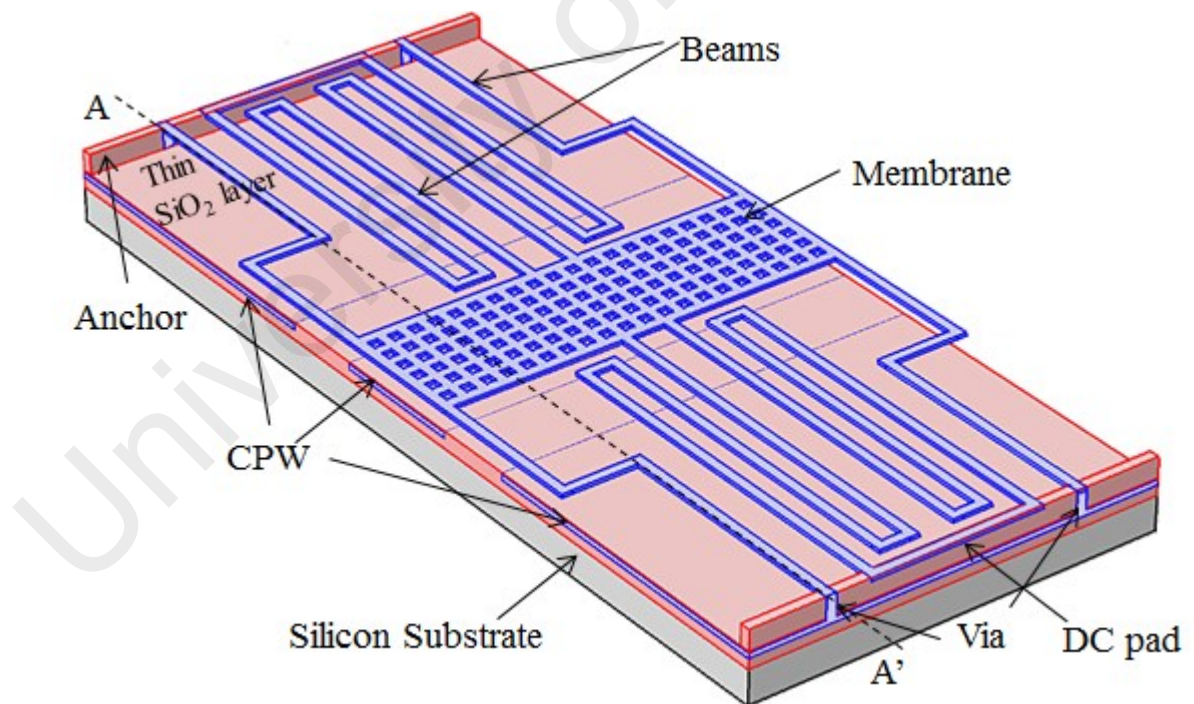
3.3 Device Description

In this section, the basic structure, working principle and mechanical modeling of the proposed capacitive RF-MEMS switch are described in detail.

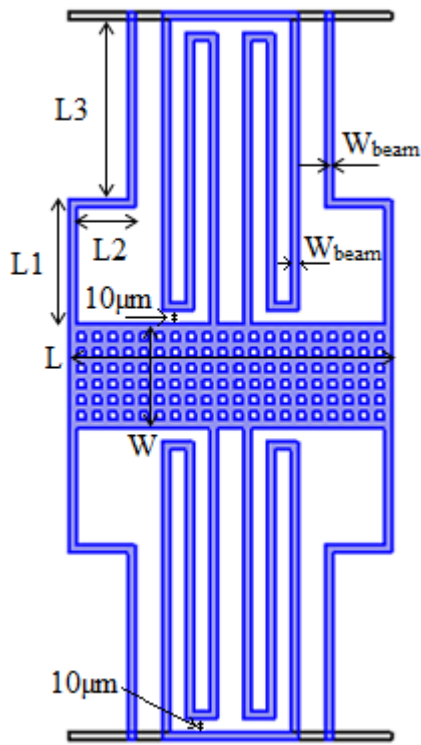
3.3.1 Structure

The structure of the RF-MEMS switch is presented in Figure 3.2 (a); it mainly includes six parts which are high-resistivity silicon substrate, CPW, a very thin dielectric layer on the surface of the CPW, a big suspended and aperture membrane, eight beams (four folded and four spring ones), as well as anchors. The reason to employ shunt-type capacitive RF-MEMS switch has been explained in section 3.2. The membrane and the signal line of the CPW are used as two electrodes of the capacitor. Spring and folded beams are utilized for reducing the whole spring constant of the switch and further to decrease the pull-in voltage of the RF-MEMS capacitive switch. The CPW, membrane and beams are all made from aluminum (Al); and silicon dioxide

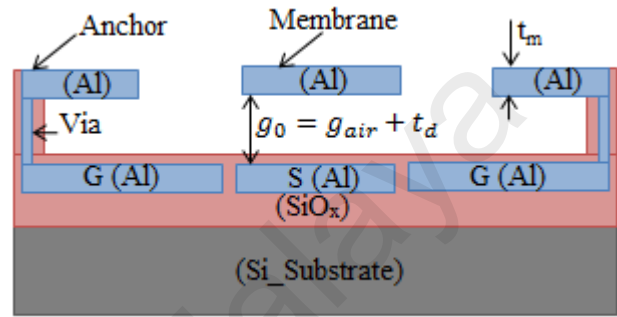
(SiO₂) is chosen as the thin dielectric layer material; both of them are the most common materials used in the CMOS-compatible process. Figure 3.2 (b) is the top view of the RF-MEMS switch which includes the geometric parameters of the membrane and beams. The small holes on the membrane are used to i) reduce the squeeze film damping, ii) increase the speed of the switch, and iii) easily release the membrane during the fabrication process. The outer four folded beams mainly provide support to the large membrane and also are connected to the ground planes by anchors (or via), as shown in Figure 3.2 (c). The inner four spring beams are used to supply the DC bias voltage to the membrane (namely the capacitor's top electrode) and keep the membrane's profile flat. The cross-section view of the RF-MEMS capacitive switch is illustrated in Figure 3.2 (c). Figure 3.2 (d) shows the DC pads' connection of the RF-MEMS switch.



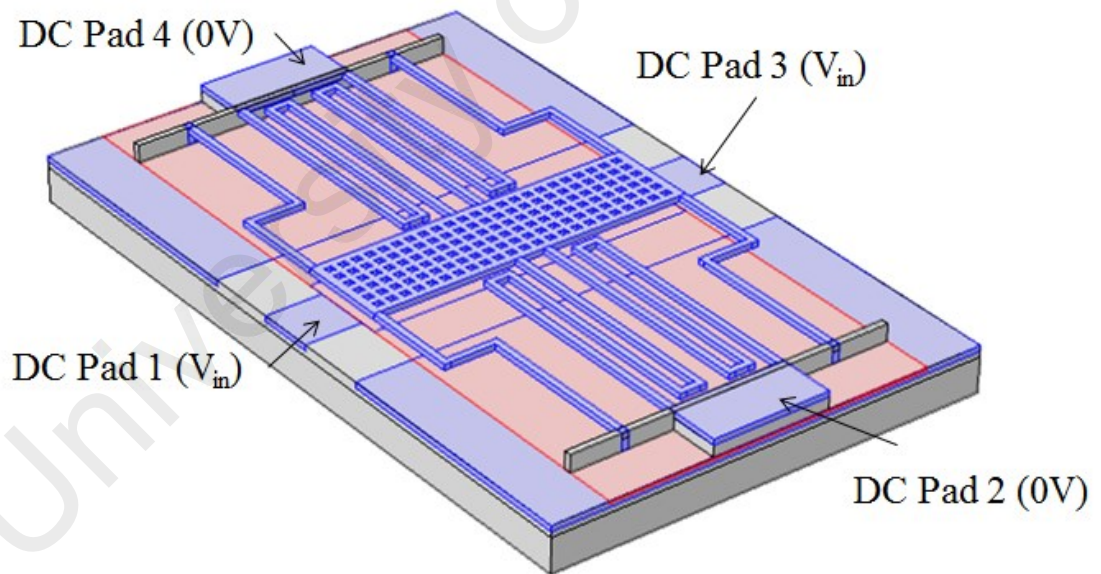
(a) Overall view



(b) Top view



(c) Cross-section view (A-A')



(d) RF-MEMS switch's DC pads design

Figure 3.2: RF-MEMS switch design

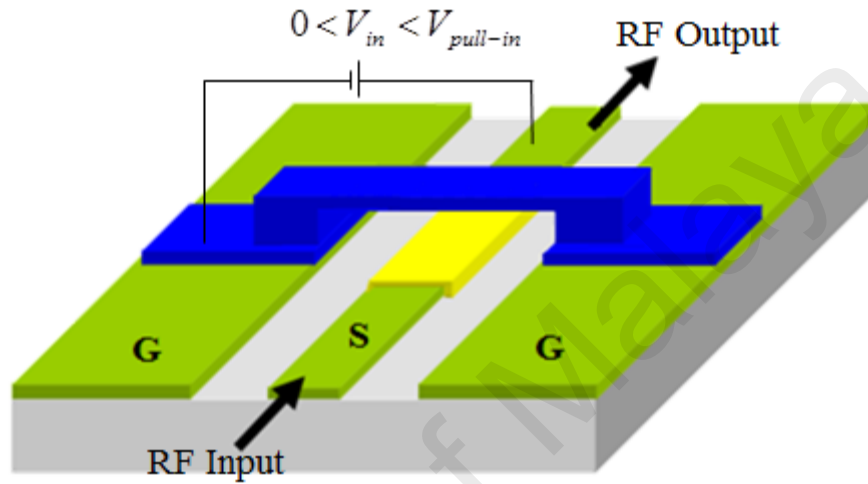
3.3.2 Working Principle

For the RF-MEMS capacitive switch, when a DC bias voltage is applied between the membrane (namely, DC Pad 2 or 4) and the signal line (namely, DC Pad 1 or 3) of the CPW, as shown in Figure 3.2 (d), an electrostatic force is induced between them to pull the movable membrane down. There is a positive feedback between the electrostatic force and the deformation of the membrane. The electrostatic force bends down the membrane and thereby reduces the air gap between the membrane and the signal line. The reduced air gap further increases the electrostatic force. At a certain voltage, the electrostatic force exceeds the beams' mechanical stress limitation which causes the membrane unstable, and the gap collapsed; this critical voltage is called pull-in voltage or actuation voltage, labeled as $V_{pull-in}$, and can be calculated by (3.1) (Gupta, 1998; Rebeiz, 2003f). Once the RF-MEMS switch is actuated, a coupling capacitor between the membrane and the signal line is induced which is due to the thin SiO₂ layer. This capacitor prevents the RF signal to be passed along the T line and bypasses it to the ground planes; at the same time the switch is turned off, as shown in Figure 3.3. When the applied DC voltage is reduced to a certain value, the membrane is rebounded back to the initial position. This voltage is called pull-out voltage, labeled as $V_{pull-out}$, and can be estimated by (3.2) (Behlert, Kunzig, Schrag, & Wachutka, 2014); the value of the pull-out voltage is almost near to zero volt. At this moment the RF-MEMS switch is turned on; and the RF signal can be propagated along the T line.

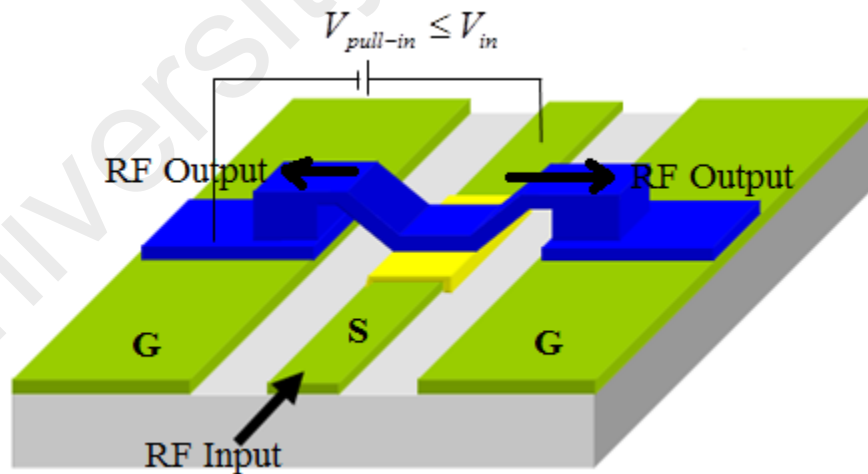
$$V_{pull-in} = \sqrt{\frac{8kg_0^3}{27\varepsilon_0 A}} \quad (3.1)$$

$$V_{pull-out} = \sqrt{\frac{2kg_0 t_d^2}{\varepsilon_0 \varepsilon_r^2 A}} \quad (3.2)$$

Where, k is the total spring constant of the membrane and beams; g_0 is the initial gap between the membrane and the signal line; ϵ_0 is the permittivity of air, $8.854 \times 10^{-12} \text{F/m}$; ϵ_r is the dielectric layer's relative permittivity; t_d is the thickness of the thin dielectric layer; and A is the actuation area, namely the product of the membrane's width and length ($W \times L$).



(a) Switch-on state



(b) Switch-off state

Figure 3.3 Working principle of shunt RF-MEMS capacitive switch

3.3.3 Mechanical Modeling

In order to model of MEMS devices, generally two aspects need to be considered which are in mechanical domain and in electric domain. Here mechanical modeling of the electrostatic-actuated RF-MEMS capacitive switch is introduced and its electromagnetic modeling will be presented in section 4.4.1 since its S parameters and impedance will be used for extracting the electromagnetic equivalent circuit.

1-D mass-spring-damper system has been widely used to model the mechanical behavior of the RF-MEMS switches since it is simple and easy to be understood, as shown in Figure. 3.4. The big membrane is assumed to move up and down while keeping its surface flat; this was achieved by using the folded and spring beams to connect the membrane and anchors.

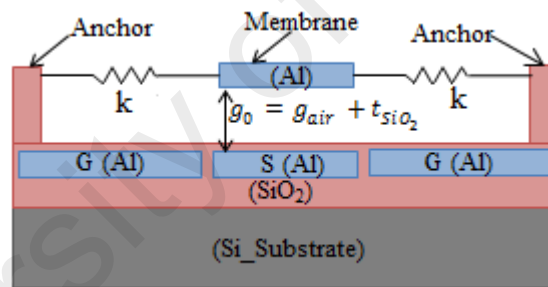


Figure 3.4: 1-D mass-spring-damper system

The governing equation of the membrane's movement motion is given by (3.3) (Muldavin, 2001),

$$m \cdot z(t)'' + c \cdot z(t)' + k \cdot z(t) = F(z, t) \quad (3.3)$$

Where, m is the lumped mass, namely membrane and beams' mass in our design; c is the viscous damping coefficient; k is the stiffness or the total spring constant of eight beams in our design; and $F(z, t)$ is the external forcing function due to the electrostatic attraction across parallel plate capacitance.

The system's mechanical resonant frequency (ω_r), damping ratio (ζ) and quality factor (Q) is obtained by (3.4-3.6).

$$\omega_r = 2\pi f_r = \sqrt{\frac{k}{m}} \quad (3.4)$$

$$\zeta = \frac{c}{2\sqrt{k \cdot m}} \quad (3.5)$$

$$Q = \frac{1}{2\zeta} = \frac{k}{\omega_0 \cdot c} \quad (3.6)$$

In this design, the lumped mass, total spring constant, damping coefficient and resonant frequency can be estimated from the 3-D finite element method simulation, such as Comsol Multiphysics[®]; and the corresponding simulation results will be detailed in chapter 4.

3.4 Geometric Dimensions' Determination

Generally the switch's physical dimensions are determined by its design specifications, such as actuation voltage, CPW's impedance, capacitance ratio, initial capacitance and RF performance or S parameter. This section shows how to derive and optimize the dimensions of the RF-MEMS switch from its design specifications. Basically the RF-MEMS switch's geometric derivation and optimization is divided into three parts or steps, as shown in Figure 3.1 (b). The first step is to determine the basic dimensions, such as the width and thickness of the CPW, air gap, actuation area, up-state capacitance and the length of the membrane. The second step is to optimize the beam dimensions for low-actuation voltage by using multi-response optimization

method. The last step is to improve the RF performance by employing T-match and π -match techniques, respectively. Following contents explain these steps in detail.

3.4.1 Determine the Basic Dimensions

This section shows how to determine the RF-MEMS switch's basic dimensions by its design specifications. The RF-MEMS switch's basic dimensions include the width, length and thickness of the CPW and membrane, as well as air gap. The design specifications of the RF-MEMS switch have been identified in section 3.2.

3.4.1.1 Dimensions of the CPW

As introduced in section 2.5.1, CPW is formed by a signal line separated from a pair of ground planes, all of them on the same plane, atop a dielectric medium, as shown in Figure 2.6. Comparing with the theoretical calculation by conformal mapping technique, there is an easier way to compute its impedance by some related software, such as TX-LINETM or Agilent CAD tool[®]. TX-LINETM software is a windows-based interactive transmission line calculator for the analysis and synthesis of transmission line structure which is embedded with AWR Design EnvironmentTM. Generally the CPW's impedance depends on the type of CPW (e.g. CPW or conductor-backed CPW) and its physic parameters, as shown in Figure 2.6 (b), namely the substrate's thickness (H_{sub}), substrate's dielectric permittivity (ϵ_R) or substrate material, the gap between the signal line and the ground plane (G), as well as the width (W) and thickness of the signal line (t_{CPW}).

Figure 3.5 shows the substrate and CPW's dimension's setting to obtain a standard RF impedance of 50Ω (Wen, 1969) by TXLINE 2003TM, where CPW model without

back ground conductor is employed which is also called the classic CPW. In order to reduce the substrate RF signal's losses, and to be compatible with CMOS process, firstly a high-resistivity ($>10\text{k}\Omega\cdot\text{cm}$) silicon-based substrate is selected; also silicon-based technology is presently the most consolidated fabrication process of RF-MEMS switches (Persano, Quaranta, Martucci, Siciliano, & Cola, 2015), as shown the setting 1 in Figure 3.5. The second setting is to choose the conductor for the CPW; here aluminum, as the most common metal material in standard CMOS process with good mechanical properties and low cost, is selected for the material of the CPW. The third setting is to fill the geometric parameters of the CPW, where the physical length of the CPW does not affect its impedance; and the other parameters were fixed as $W=80\mu\text{m}$, $G=47\mu\text{m}$, $H_{\text{sub}}=500\mu\text{m}$ and $t_{\text{CPW}}=1\mu\text{m}$. Together with the frequency of the setting 4, by clicking the leftwards arrow, the impedance of the CPW is obtained almost as 50Ω . At the same time, the effective dielectric constant, loss of the CPW line, as well as its phase constant can be calculated as shown in the results.

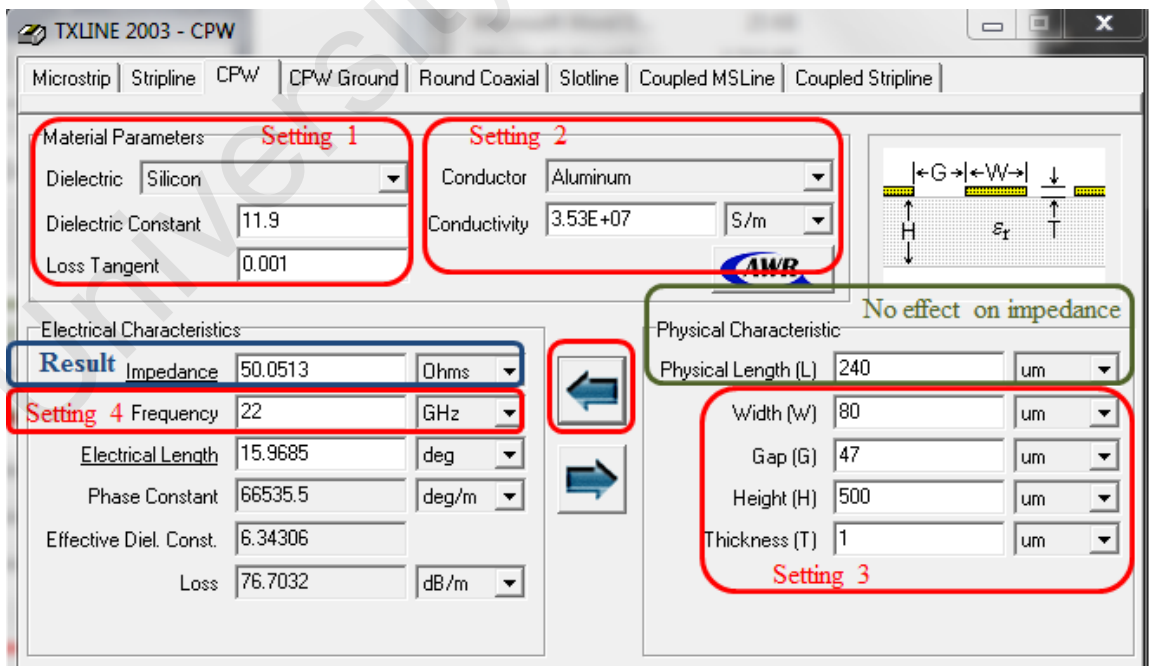


Figure 3.5: CPW line designed by TXLINE 2003™

3.4.1.2 Range of Air Gap

The capacitance of the RF-MEMS switch in turn-off state (the membrane is collapsed on the signal line) and turn-on state (the membrane is suspended at the original place) can be calculated by (3.7) and (3.8) (Rebeiz, 2003g), respectively. For off-state (or down-state) capacitance (C_d), the fringing field capacitance can be ignored since the gap between the two electrodes is too small (around $0.1\mu\text{m}$ to $0.2\mu\text{m}$); while for on-state (or up-state) capacitance (C_u), the fringing field capacitance (C_f) is around 0.3 to 0.4 times of the main part capacitance (C_{pp}) (Rebeiz, 2003g) as shown in (3.8). Then the capacitance ratio can be calculated by (3.9); and it can be seen that only the air gap, dielectric permittivity and thickness of the thin dielectric layer can affect the value of the capacitance ratio which has no relationship with the actuation area or the membrane area.

$$C_d = \frac{\epsilon_0 \epsilon_r A}{t_d} \quad (3.7)$$

$$C_u = C_{pp} + C_f = \frac{\epsilon_0 A}{g_0 + \frac{t_d}{\epsilon_r}} + C_f \quad \text{With } C_f = x \cdot C_{pp} \quad (x = 0.3 \sim 0.4) \quad (3.8)$$

$$C_{Ratio} = \frac{C_d}{C_u} = \frac{\frac{\epsilon_0 \epsilon_r A}{t_d}}{\frac{\epsilon_0 A}{g_0 + \frac{t_d}{\epsilon_r}} + C_f} = \frac{\frac{\epsilon_0 \epsilon_r A}{t_d}}{\frac{\epsilon_0 A}{g_0 + \frac{t_d}{\epsilon_r}} + x \frac{\epsilon_0 A}{g_0 + \frac{t_d}{\epsilon_r}}} = \frac{g_0 \epsilon_r + t_d}{(1+x)t_d} \quad (3.9)$$

Where, C_d is down-state capacitance; and C_u is the up-state capacitance; C_f is the fringing field capacitance of C_u ; C_{pp} is the parallel-plate capacitance of the MEMS shunt switch when it is at up state; x is a coefficient of fringing field capacitance; and C_{Ratio} is the down-state to up-state capacitance ratio.

The large capacitance ratio (≥ 40) can guarantee a high isolation ($>10\text{dB}$) and small insertion loss ($<1\text{dB}$), namely a good RF characteristic. Comparing with traditional RF switches such as FETs and p-i-n diodes, the RF-MEMS switches have higher capacitance ratio which is generally larger than 40 (Rebeiz, 2003a). From (3.9) it can be seen that, in order to obtain a large capacitance ratio, the air gap (g_0) and the relative dielectric permittivity (ϵ_r) should be increased while the thickness of dielectric layer between two electrodes (t_d) should be decreased. In this design, the dielectric constant is about 3.9 since SiO_2 is chosen. The dielectric thickness could not to be less than 1000\AA due to pinhole problem and must be able to withstand the pull-in voltage without dielectric breakdown (Rebeiz, 2003g); the typical value is around $1000\sim 2000\text{\AA}$ in all MEMS switching built today (Rebeiz, 2003g; Muldavin & Rebeiz, 2000). Then the air gap range can be estimated as shown in Figure 3.6, where the green area is the capacitance ratio of larger than 40 which has been defined in design specifications. For example, if the coefficient of fringing field capacitance is 0.3 and the dielectric thickness is $0.15\mu\text{m}$, then the air gap should be at least larger than $1.96\mu\text{m}$ to ensure a capacitance ratio of greater than 40. Similarly, if the coefficient of fringing field capacitance is 0.4 and keeping the same dielectric thickness, then the air gap should be at least more than $2.12\mu\text{m}$ to maintain a good RF performance. The air gap is also limited by the actuation voltage as shown in (3.1). If the value of g_0 is set very large, then the actuation voltage will be increased a lot which is hard to achieve the low-actuation voltage's design objective. For the most low-voltage capacitive RF-MEMS designs (Afrang & Abbaspour-Sani, 2006; Deng, Wei, Fan, & Gan, 2015; Fernández-Bolaños, Perruisseau-Carrier, Dainesi, & Ionescu, 2008; Persano et al., 2012; Zareie & Rebeiz, 2013), the value of g_0 is not larger than $3\mu\text{m}$.

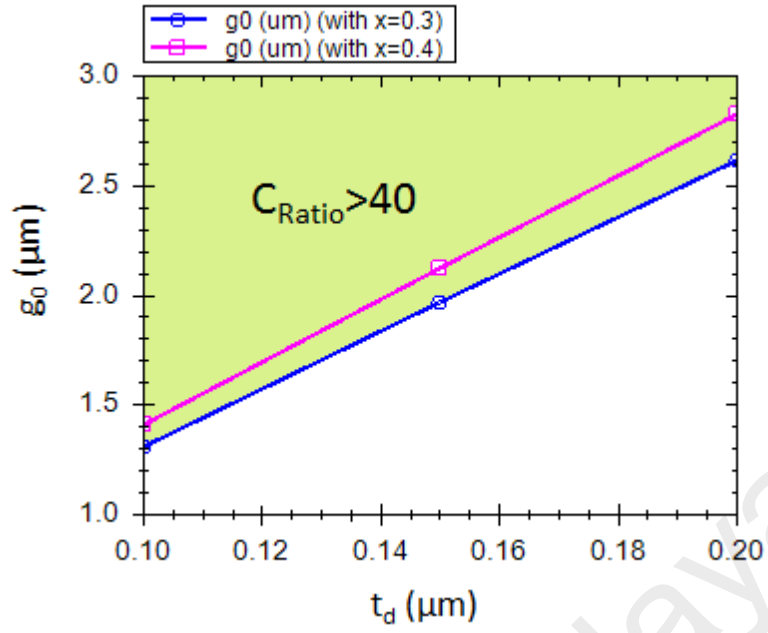


Figure 3.6: Air gap's estimation for capacitance ratio of more than 40

3.4.1.3 Range of Up-State Capacitance and Dimensions of Membrane

In order to have a good matching of the input at switch-on state (or actuated state, or up state), namely 50Ω matching, the turn-on state return loss should be at least less than -10dB (or $S11_{up} \leq -10\text{dB}$) as mentioned in part 3.2 and it can be calculated by (3.10) and (3.11) (Rebeiz, 2003a; Mafinejad, Kouzani, Mafinezhad, & Kaynak, 2012; Muldavin & Rebeiz, 2000). Then a relationship of the up-state capacitance with the operating frequency can be obtained, as shown in (3.12).

$$S11_{up} = \frac{-j\omega C_u Z_0}{2 + j\omega C_u Z_0} \quad (3.10)$$

$$\omega = 2\pi f_0 \quad (3.11)$$

$$\omega C_u Z_0 \leq \frac{2}{3} \text{ for } S11_{up} \leq -10\text{dB} \quad (3.12)$$

Where, f_0 is the RF-MEMS switch's operating frequency, for a K-band RF-MEMS switch; and Z_0 is the standard RF cable impedance which is 50Ω employed in this design.

Therefore, the range of C_u can be estimated as shown in Figure 3.7; the detail derivation is explained in Appendix A. Suppose the larger C_u , the bigger membrane is obtained with the fixed air gap, which can lead to a better isolation. For example, at the frequency of 22GHz, the C_u should be less than 96.46fF from Figure 3.7. Considering with 10% margin value for the estimation, C_u is designed at 87fF. By employing equation of (3.8) and the value of the signal line's width (W), the membrane area (A) and its length (L) can be decided, as shown in Table 3.2.

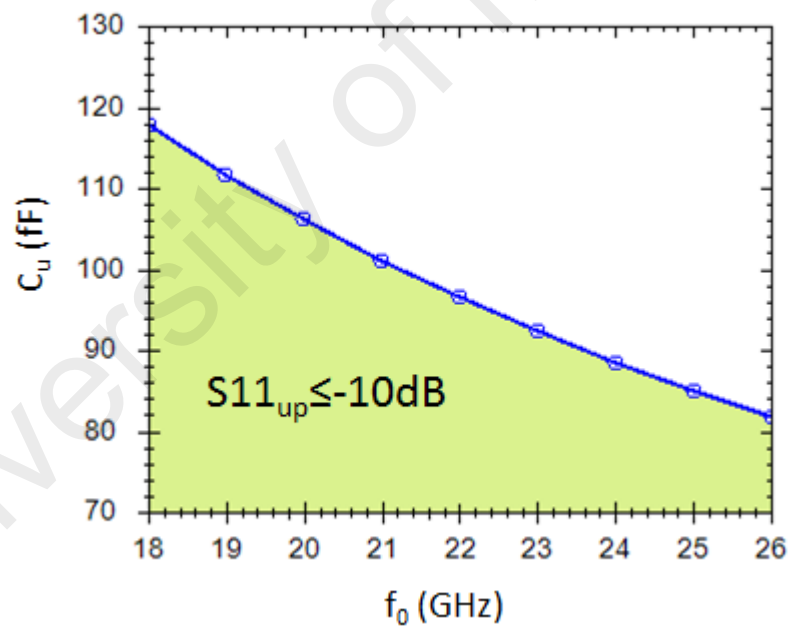


Figure 3.7: Up-state capacitance's estimation for K-band capacitive switch with $S_{11_{up}} \leq -10\text{dB}$

Table 3.2: Membrane's dimensions with C_u of 87fF

| Parameter | g_0 (μm) | t_d (μm) | A (μm^2) | W (μm) | L (μm) | |
|-----------|-------------------------|-------------------------|-------------------------|-----------------------|-----------------------|-----|
| Value | Design 1 | 2.5 | 0.15 | 19200 | 80 | 240 |
| | Design 2 | 3 | 0.15 | 22960 | 80 | 287 |
| | Design 3 | 3 | 0.1 | 22880 | 80 | 286 |
| | Design 4 | 3 | 0.2 | 23040 | 80 | 288 |

3.4.1.4 Down-State Capacitance and Capacitance Ratio

By using the estimated values of Table 3.2, equation of (3.7) and (3.9), the down-state capacitance and capacitance ratio can be obtained for each design, as summarized in Table 3.3, where four groups of design dimensions are listed and compared. It can be seen clearly that among the different air gap and dielectric thickness' conditions, Design 3 with t_d of $0.1\mu\text{m}$ and g_0 of $3\mu\text{m}$ has the largest capacitance ratio, namely 90, which can be expected to produce the best RF performance among them; therefore, parameters of Design 3 were chosen as the final dimensions for the further design and analysis.

Table 3.3: Four groups of RF-MEMS switch's dimensions with different air gap and thin dielectric thickness

| Parameter | | Value | | | |
|-------------|-------------|-------------------------------------|-------------------------------------|------------------------------------|------------------------------------|
| | | Design 1 | Design 2 | Design 3 | Design 4 |
| Thickness | t_m | $1\mu\text{m}$ | $1\mu\text{m}$ | $1\mu\text{m}$ | $1\mu\text{m}$ |
| | t_d | $0.15\mu\text{m}$ | $0.15\mu\text{m}$ | $0.1\mu\text{m}$ | $0.2\mu\text{m}$ |
| | t_{CPW} | $1\mu\text{m}$ | $1\mu\text{m}$ | $1\mu\text{m}$ | $1\mu\text{m}$ |
| | t_{SiO2} | $1\mu\text{m}$ | $1\mu\text{m}$ | $1\mu\text{m}$ | $1\mu\text{m}$ |
| g_0 | | $2.5\mu\text{m}$ | $3\mu\text{m}$ | $3\mu\text{m}$ | $3\mu\text{m}$ |
| Membrane | A | $19200\mu\text{m}^2$ | $22960\mu\text{m}^2$ | $22880\mu\text{m}^2$ | $23040\mu\text{m}^2$ |
| | W | $80\mu\text{m}$ | $80\mu\text{m}$ | $80\mu\text{m}$ | $80\mu\text{m}$ |
| | L | $240\mu\text{m}$ | $287\mu\text{m}$ | $286\mu\text{m}$ | $288\mu\text{m}$ |
| G | | $47\mu\text{m}$ | $47\mu\text{m}$ | $47\mu\text{m}$ | $47\mu\text{m}$ |
| Capacitance | C_u | 87fF | 87fF | 87fF | 87fF |
| | C_d | 4.42pF | 5.29pF | 7.9pF | 3.98pF |
| | C_{Ratio} | 50 | 60 | 90 | 45 |

3.4.2 Beams Optimization for Low Pull-In Voltage

From (3.1) it can be seen that in order to develop a RF-MEMS capacitive switch with low-actuation voltage, the total spring constant (k) and initial air gap between the two electrodes (g_0) of the switch should be small, the actuation area (A) of the switch should be large. In the previous sections, the ranges of air gap and actuation (or membrane) area have been determined by capacitance ratio and up-state return loss, respectively. Therefore, the last flexible and important parameter which can be designed and controlled by the researchers is the total spring constant of the membrane and beams. For the Design 3 of Table 3.3, the relationship of $V_{pull-in}$ and k was plotted in Figure 3.8, where it shows that i) the smaller spring constant, the smaller actuation voltage is obtained; and ii) if an actuation voltage of 3V is preferred, the total spring constant should be 0.2279N/m. Basically if considering the beam itself, a low-spring-constant beam should have small width and thickness; however this will make the beam structure to become fragile and prone to failure (Ma, Nordin, & Soin, 2015). Moreover beam's design will also affect the switch's actuation time since the actuation time is determined by the first resonant frequency of the membrane and beams. Optimizing the beam lengths ($L1$, $L2$ and $L3$) and width (W_{beam}) to obtain a low spring constant and short switching time meantime to maintain a robust operation becomes an essential problem for the design of low-actuation-voltage RF-MEMS switch. A multi-response optimization method based on Taguchi method and WPCA is first developed and employed in this work. The optimization parameters and objectives, as well as the optimization methodology and its results are presented in detailed as following.

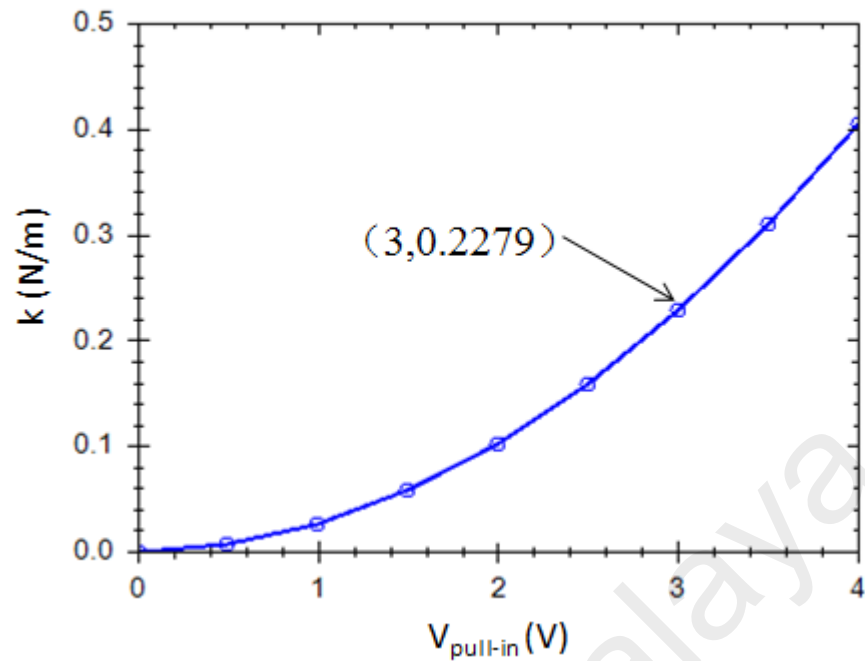


Figure 3.8: Relationships of $V_{pull-in}$ and k

3.4.2.1 Optimization Parameters and Objectives

There are four geometric parameters of the beams to be optimized as shown in Figure 3.2 (b), namely the folded beam's first length ($L1$), second length ($L2$), third length ($L3$) and width (W_{beam}) which is for both the folded and the spring beams. Their possible values are listed in Table 3.4.

Table 3.4: Variable parameters and their levels

| Variable | W_{beam} | $L1$ | $L2$ | $L3$ |
|----------|-----------------|------------------|------------------|-------------------|
| Level1 | 5 μm | 80 μm | 45 μm | 140 μm |
| Level2 | 6 μm | 85 μm | 50 μm | 145 μm |
| Level3 | 7 μm | 90 μm | 55 μm | 150 μm |

In total there are three optimized objectives to be considered in this work: i) the most important one is to obtain a small-spring-constant design which could further to ensure the switch's low actuation voltage; ii) the second is to get a relative short switching time;

and iii) the third is to achieve an acceptable maximum von Mises stress of the beams to ensure the membrane and beams' robust movement. From Figure 3.8, it can be seen that in order to get $V_{pull-in}$ of 3V with model parameters of Design 3, the total spring constant should be around 0.2279N/m which is one of the optimized objectives and is a specific value; the nominal the best characteristic was used for spring constant's S/N calculations. The RF-MEMS switch's switching time is mainly determined by the first mechanical resonant frequency (f_r) of the membrane and beams, as displayed in (3.13) and (3.14) (Dutta, Imran, Pal, Jain, & Chatterjee, 2011), which are switch-off time during pull-down condition (t_{OFF}) and switch-on time during releasing condition (t_{ON}). For switch-on time, in order to reduce its oscillation magnitude and time, the damping ratio is preferred to be 1; in another word, the behavior of the system is critically damped. Both of the switching times are inversely proportional to the first resonant frequency. Therefore, in order to get the least switching time, the first resonant frequency should be as large as possible; and the larger the better characteristic was used to calculate the S/N of f_r in the next section. Von Mises stress (σ_v) is commonly utilized by engineers to check whether their design can withstand a given load condition or not; and it is thought to be a safe haven for design engineers. By using three dimension principal stresses ($\sigma_1, \sigma_2, \sigma_3$), von Mises stress can be calculated by (3.15) (Imajey, 2012); for a complicated structure, this value can be obtained by using finite element analysis (FEA). According to distortion energy failure theory, the condition of structure's failure can be found in (3.16) (Imajey, 2012); in other word, failure happens when the maximum von Mises stress induced in the material goes beyond yield strength (for ductile material) of the material under certain voltage or force load. In this work, aluminum is used for the beams and membrane structure; its yield stress is around 15MPa to 20MPa (Howatson, 2012). Therefore, the final optimized structure should

have the maximum von Mises stress less than 15MPa under the actuated state to make sure the switch's operation well.

$$t_{OFF} = \frac{\pi}{2V_{in}} \sqrt{\frac{mg_0^3}{A\varepsilon_0}} = \left(\frac{1}{4f_r} \sqrt{\frac{27}{8}} \right) \Big|_{V_{in} \geq V_{Pull-in}} \quad (3.13)$$

$$t_{ON} = \frac{1}{4f_r} \quad (3.14)$$

Where, t_{OFF} and t_{ON} is the switching-off and switching-on time, respectively; f_r is the beams' first resonant frequency; $V_{pull-in}$ is the actuation voltage; V_{in} is the applied DC bias voltage; and m is the total weight of the membrane and beams.

$$\left[\frac{(\sigma_1 - \sigma_2)^2 + (\sigma_2 - \sigma_3)^2 + (\sigma_3 - \sigma_1)^2}{2} \right]^{\frac{1}{2}} = \sigma_v \quad (3.15)$$

$$\sigma_{v_max} \geq \sigma_y \quad (3.16)$$

Where, σ_1 , σ_2 and σ_3 is the principal stress; σ_v is von Mises stress; σ_{v_max} is the maximum von Mises stress; and σ_y is yield stress.

3.4.2.2 Optimization Methodology and Results

The methodology for this multiple objectives' optimization consists of Taguchi method and WPCA together as presented in Figure 3.9. The basic idea is that firstly using the aforementioned objectives of i) (namely, to obtain a design with spring constant of 0.2279N/m) and ii) (namely, to get a relative short switching time) as the optimization responses in the whole optimization process. Once the structure's optimized parameters are obtained, the third objective (namely, to achieve an acceptable

maximum von Mises stress) is tested. If the optimized condition is fulfilled the objective of iii), the design parameters are finalized; otherwise, tune the variable parameters' setting values (in Table 3.4), until the design structure meets all the objectives. The criterion of choosing the best combination of the variable parameters' values is that the larger of total S/N the better result preferred.

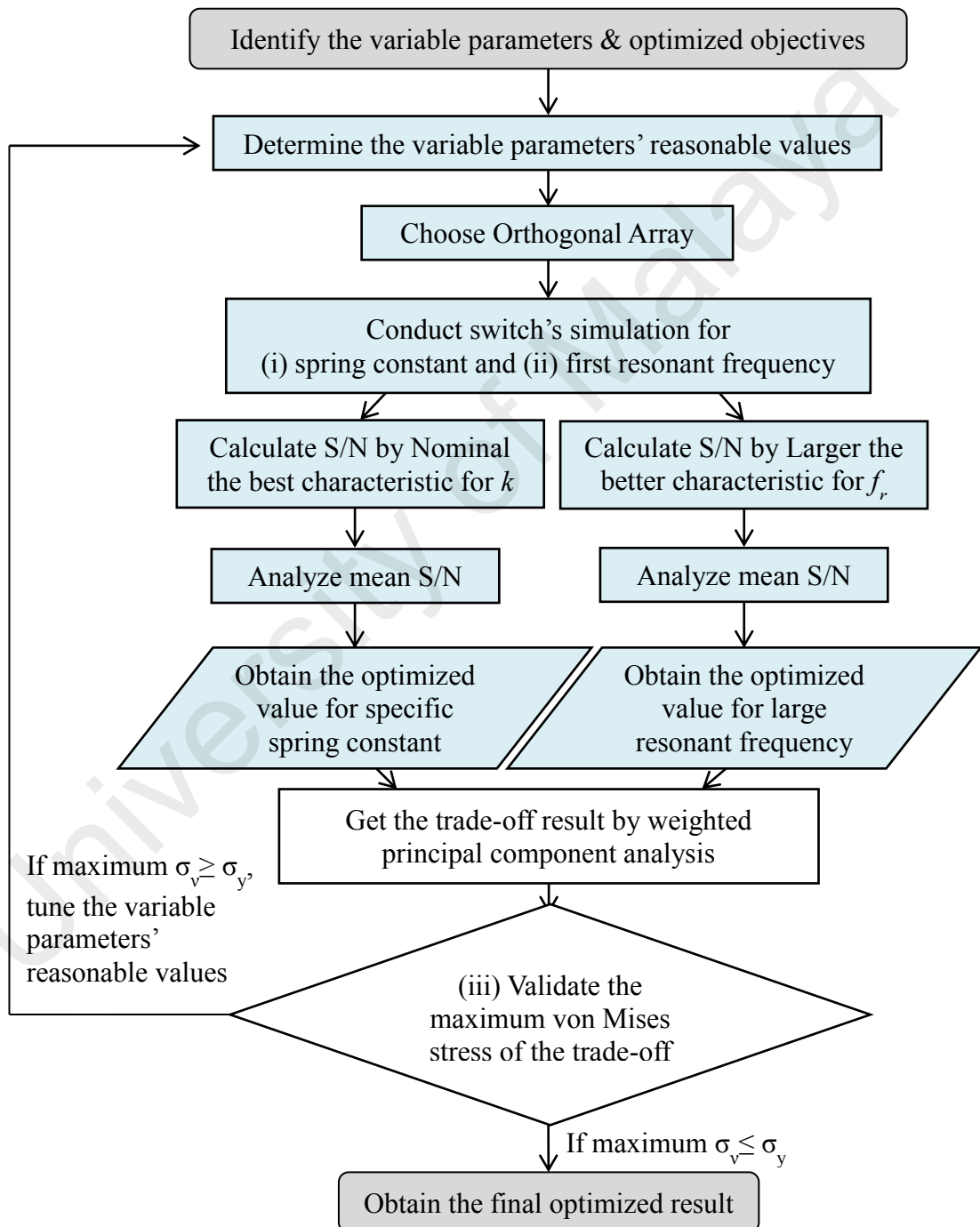


Figure 3.9: Multi-response optimization methodology

Orthogonal array (OA) of $L_9 (3^4)$ (Taguchi, Chowdhury, & Wu, 2005) is selected according to the variables' number and levels, as shown in Table 3.5 part I. As aforementioned, the spring constant with $k=0.2279N/m$ is the main optimized objective to ensure the switch's pull-in voltage of 3V; therefore the S/N of the nominal the best is chosen for the spring constant calculation, as shown in (2.2). In order to obtain less switching time, the first resonant frequency of the moving structure should be large; therefore the S/N of the larger the better is employed for the beams resonant frequency's calculation, as shown in (2.3). Then the simulated results of spring constant and the first resonant frequency as well as their corresponding S/N ratios for the OA table's variable settings are summarized in part II of the Table 3.5. The simulated results for the responses of the spring constant and the resonant frequency were obtained by FEM software, namely Comsol Multiphysics 4.3[®], where the physical model of Electromechanics was used. The boundary conditions were set as: i) fixing the ends of all the beams; ii) for the simulation of the spring constant, a linear surface force load is applied; and for the simulation of the first resonant frequency, there is no any load applied on the structure.

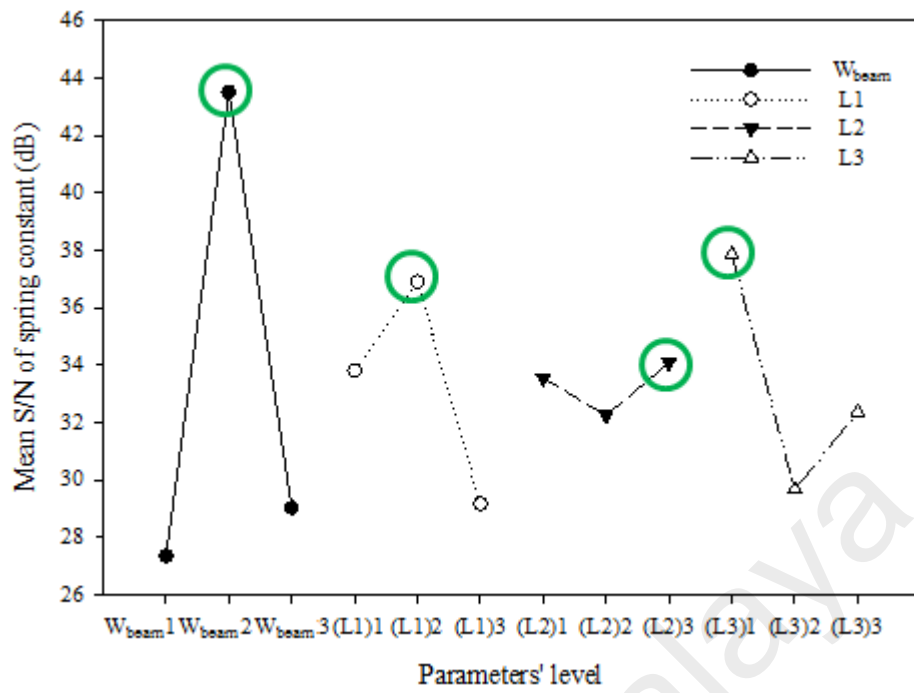
Table 3.5: Beams' optimization by Taguchi method

| Part I | | | | | Part II | | | |
|----------|------------|------|------|------|-------------------|-------------|----------------|------------|
| Exp. No. | Factors | | | | Simulated results | | Calculated S/N | |
| | W_{beam} | $L1$ | $L2$ | $L3$ | k (N/m) | f_r (kHz) | k (dB) | f_r (dB) |
| 1 | 1 | 1 | 1 | 1 | 0.2046 | 7.053 | 32.6653 | 16.9675 |
| 2 | 1 | 2 | 2 | 2 | 0.1794 | 6.547 | 26.2780 | 16.3208 |
| 3 | 1 | 3 | 3 | 3 | 0.1579 | 6.084 | 23.1036 | 15.6838 |
| 4 | 2 | 1 | 2 | 3 | 0.2200 | 6.930 | 42.0390 | 16.8147 |
| 5 | 2 | 2 | 3 | 1 | 0.2303 | 7.138 | 52.4516 | 17.0715 |
| 6 | 2 | 3 | 1 | 2 | 0.2121 | 6.769 | 36.0223 | 16.6105 |
| 7 | 3 | 1 | 3 | 2 | 0.2741 | 7.468 | 26.7166 | 17.4641 |
| 8 | 3 | 2 | 1 | 3 | 0.2531 | 7.070 | 31.9674 | 16.9884 |
| 9 | 3 | 3 | 2 | 1 | 0.2658 | 7.297 | 28.4215 | 17.2629 |

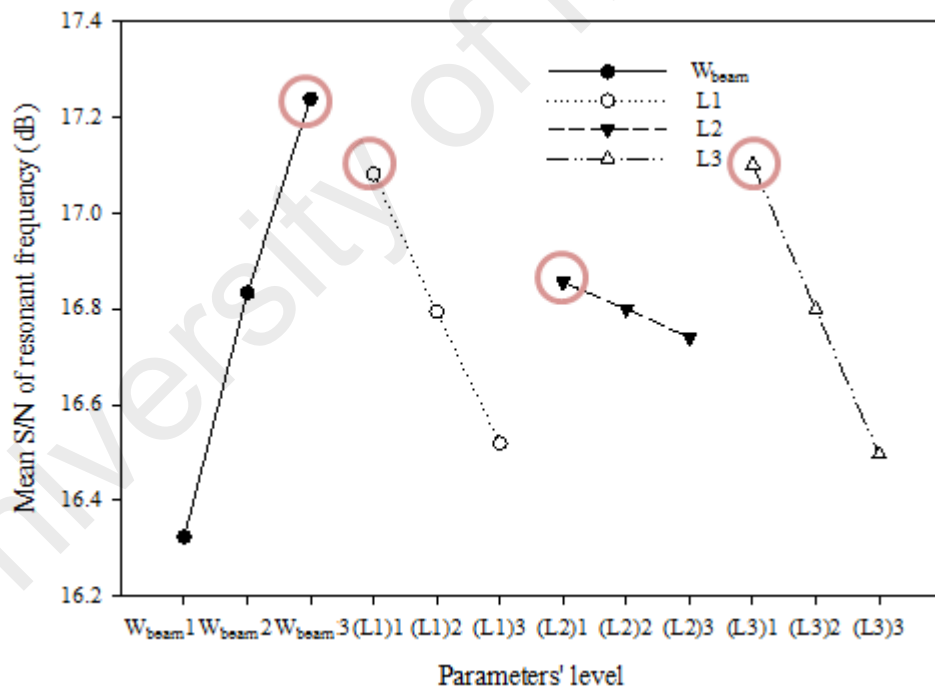
The average S/N of both the spring constant and the resonant frequency at each level are calculated in Table 3.6; and their corresponding plots are displayed in Figure 3.10. The larger value of Max-Min represents the corresponding parameter has more effect on the response, vice versa. Figure 3.10 (a) illustrates that in order to get the design with a spring constant of 0.2279N/m which is named as Model A, the four geometric parameters should be set as: $W_{beam}=W_{beam2}=6\mu m$, $L1=L1_2=85\mu m$, $L2=L2_3=55\mu m$, and $L3=L3_1=140\mu m$ (the subscript number means the corresponding level number). Figure 3.10 (b) illustrates that in order to obtain a design with the shortest switching time which is named as Model B, within the variable values' setting of Table 3.4, the parameters should be set as: $W_{beam}=W_{beam3}=7\mu m$, $L1=L1_1=80\mu m$, $L2=L2_1=45\mu m$, and $L3=L3_1=140\mu m$. The contribution of each parameter to the two optimized responses, namely the spring constant and the resonant frequency, was also investigated and calculated by Pareto analysis of variance (ANOVA) technique (Park & Antony, 2008), as shown the calculations in Table 3.7 and the pie chart results in Figure 3.11.

Table 3.6: Mean S/N for both spring constant and resonant frequency

| Factor | Mean S/N ratio for k | | | | Mean S/N ratio for f_r | | | |
|------------|------------------------|---------------|---------------|---------|--------------------------|---------|---------------|---------|
| | Level 1 | Level 2 | Level 3 | Max-Min | Level 1 | Level 2 | Level 3 | Max-Min |
| W_{beam} | 27.349 | 43.504 | 29.035 | 16.155 | 16.324 | 16.832 | 17.239 | 0.914 |
| $L1$ | 33.807 | 36.899 | 29.182 | 7.717 | 17.082 | 16.794 | 16.519 | 0.563 |
| $L2$ | 33.552 | 32.246 | 34.091 | 1.844 | 16.856 | 16.800 | 16.740 | 0.116 |
| $L3$ | 37.846 | 29.672 | 32.370 | 8.174 | 17.101 | 16.799 | 16.496 | 0.605 |



(a) Mean S/N of the spring constant



(b) Mean of S/N of the resonant frequency

Figure 3.10: Mean S/N plot

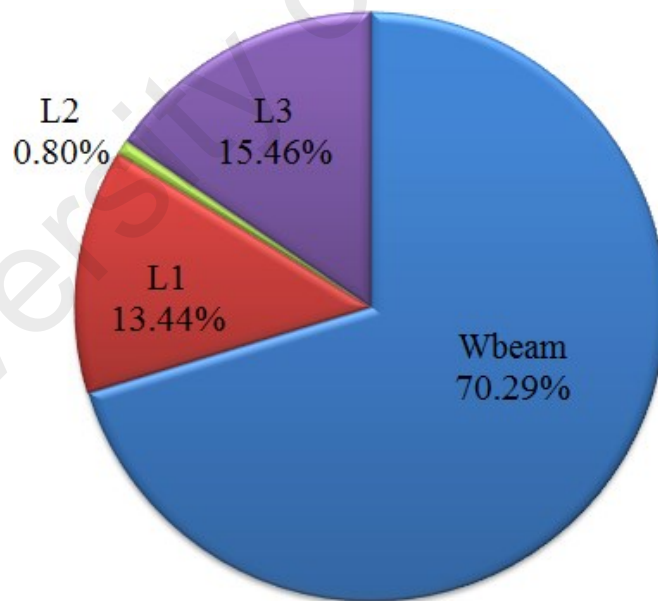
Table 3.7: Pareto ANOVA analysis

(a) For spring constant

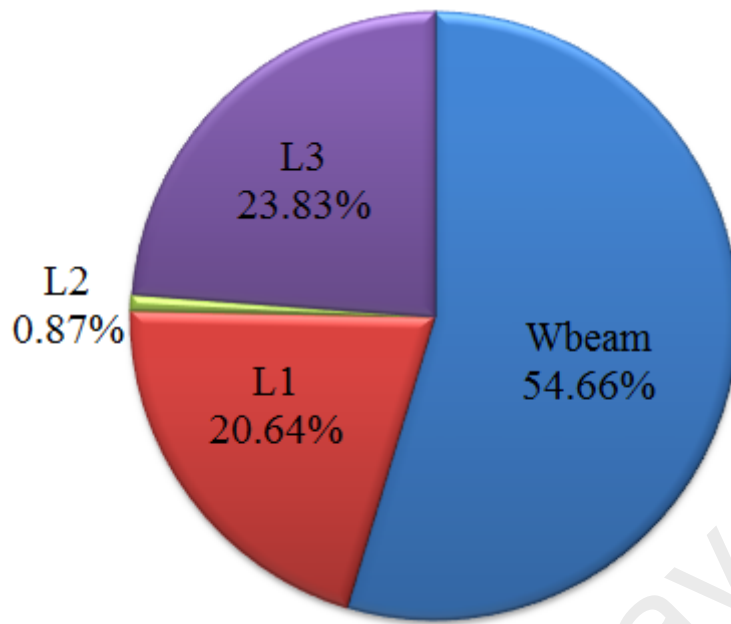
| Sum at factor level | Factor | | | | Total |
|------------------------------|------------|---------|--------|---------|----------|
| | W_{beam} | $L1$ | $L2$ | $L3$ | |
| Level 1 | 82.05 | 101.42 | 100.65 | 113.54 | 299.67 |
| Level 2 | 130.51 | 110.70 | 96.74 | 89.02 | |
| Level 3 | 87.11 | 87.55 | 102.27 | 97.11 | |
| Sum of squares of difference | 4258.754 | 814.432 | 48.570 | 936.702 | 6058.458 |
| Contribution ratio (%) | 70.294 | 13.443 | 0.802 | 15.461 | 100.000 |

(b) For resonant frequency

| Sum at factor level | Factor | | | | Total |
|------------------------------|------------|--------|-------|--------|---------|
| | W_{beam} | $L1$ | $L2$ | $L3$ | |
| Level 1 | 48.97 | 51.25 | 50.57 | 51.30 | 151.18 |
| Level 2 | 50.50 | 50.38 | 50.40 | 50.40 | |
| Level 3 | 51.72 | 49.56 | 50.22 | 49.49 | |
| Sum of squares of difference | 11.335 | 4.280 | 0.181 | 4.942 | 20.738 |
| Contribution ratio (%) | 54.659 | 20.640 | 0.871 | 23.830 | 100.000 |



(a) Spring constant



(b) Resonant frequency

Figure 3.11: Percentage contribution of each factor to the both responses

Since the four parameters' setting for the fixed spring constant of 0.2279N/m ($W_{beam}=W_{beam2}=6\mu m$, $L1=L1_2=85\mu m$, $L2=L2_3=55\mu m$, and $L3=L3_1=140\mu m$) and the largest resonant frequency ($W_{beam}=W_{beam3}=7\mu m$, $L1=L1_1=80\mu m$, $L2=L2_1=45\mu m$, and $L3=L3_1=140\mu m$) is conflict as highlighted in Figure 3.10 and their contributions for the both responses are different as displayed in Figure 3.11, a final multi-response optimized method which can obtain the trade-off results of the four parameters are needed as explained in Figure 3.9; and WPCA method is employed for the further optimization.

Following the procedures of performing the WPCA which were introduced in section 2.3.2; the normalized S/N values for both the spring constant (k) and the resonant frequency (f_r) were computed by (2.4), as displayed in Table 3.8. The PCA has been computed by using Add-Ins tool of XLSTAT in Microsoft Excel[®], where the normalized S/N values of k and f_r were set as the observations or variables; and the simulation run numbers were set as the observation labels. After the computation, a

complete PCA datasheet can be found in Microsoft Excel[®]. Table 3.9 summarized some important PCA data which were used in WPCA.

Table 3.8: Normalized S/N values and calculated MPI

| Exp. No. | Factors | | | | Normalized S/N | | MPI |
|----------|------------|------|------|------|----------------|-----------------|--------|
| | W_{beam} | $L1$ | $L2$ | $L3$ | $k(x_i^*(1))$ | $f_r(x_i^*(2))$ | |
| 1 | 1 | 1 | 1 | 1 | 0.3519 | 0.7179 | 0.3931 |
| 2 | 1 | 2 | 2 | 2 | 0.1145 | 0.3509 | 0.1573 |
| 3 | 1 | 3 | 3 | 3 | 0.0000 | 0.0000 | 0.0000 |
| 4 | 2 | 1 | 2 | 3 | 0.7127 | 0.6347 | 0.5996 |
| 5 | 2 | 2 | 3 | 1 | 1.0000 | 0.7805 | 0.8831 |
| 6 | 2 | 3 | 1 | 2 | 0.4879 | 0.5205 | 0.4288 |
| 7 | 3 | 1 | 3 | 2 | 0.1258 | 1.0000 | 0.3128 |
| 8 | 3 | 2 | 1 | 3 | 0.3104 | 0.7338 | 0.3790 |
| 9 | 3 | 3 | 2 | 1 | 0.1921 | 0.8815 | 0.3283 |

Table 3.9: Explained variation and eigenvector by PCA

| Principal component | Eigen value | Explained variation | Cumulative variation | Eigen vector $[k, f_r]$ |
|---------------------|-------------|---------------------|----------------------|-------------------------|
| Z1 | 1.319 | 65.96% | 65.96% | [0.7071, 0.7071] |
| Z2 | 0.681 | 34.04% | 100% | [0.7071, -0.7071] |

By using (2.5), MPI can be calculated as shown in (3.17) and the values were displayed in the form of the standard OA of L_9 , as presented in Table 3.8. The average values of MPI at each level for each parameter can be used to obtain the final optimized combinations for the multiple responses which is named as Model C. Specific to this case, the finalized values are $W_{beam2}(L1)_2(L2)_1(L3)_1$, as presented in Table 3.10 and Figure 3.12, where $W_{beam} = W_{beam2} = 6\mu m$, $L1 = (L1)_2 = 85\mu m$, $L2 = (L2)_1 = 45\mu m$, $L3 = (L3)_1 = 140\mu m$.

$$\begin{aligned}
 MPI &= W_1 Z_1 + W_2 Z_2 \\
 &= 0.6596 \times [Z1_{(k)} \times x_i^*(1) + Z1_{(f_r)} \times x_i^*(2)] + 0.3404 \times [Z2_{(k)} \times x_i^*(1) + Z2_{(f_r)} \times x_i^*(2)]
 \end{aligned}
 \tag{3.17}$$

Table 3.10: Mean MPI for each parameter at each level

| Factor | Mean S/N ratio | | | |
|------------|----------------|---------------|---------|---------|
| | Level 1 | Level 2 | Level 3 | Max-Min |
| W_{beam} | 0.1835 | 0.6372 | 0.3400 | 0.4537 |
| $L1$ | 0.4352 | 0.4731 | 0.2524 | 0.2207 |
| $L2$ | 0.4003 | 0.3617 | 0.3986 | 0.0386 |
| $L3$ | 0.5349 | 0.2996 | 0.3262 | 0.2353 |

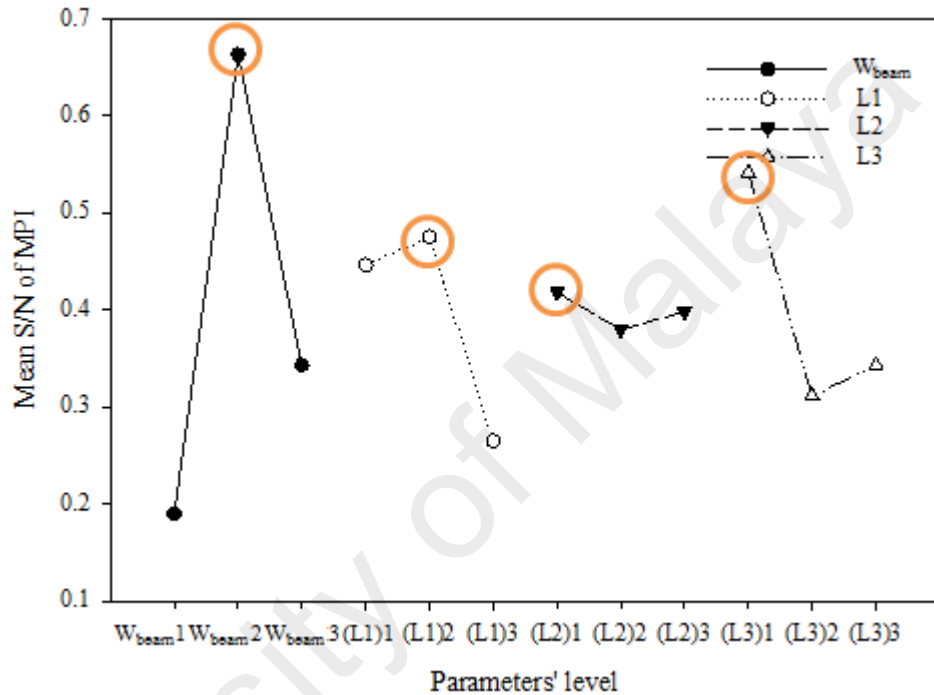


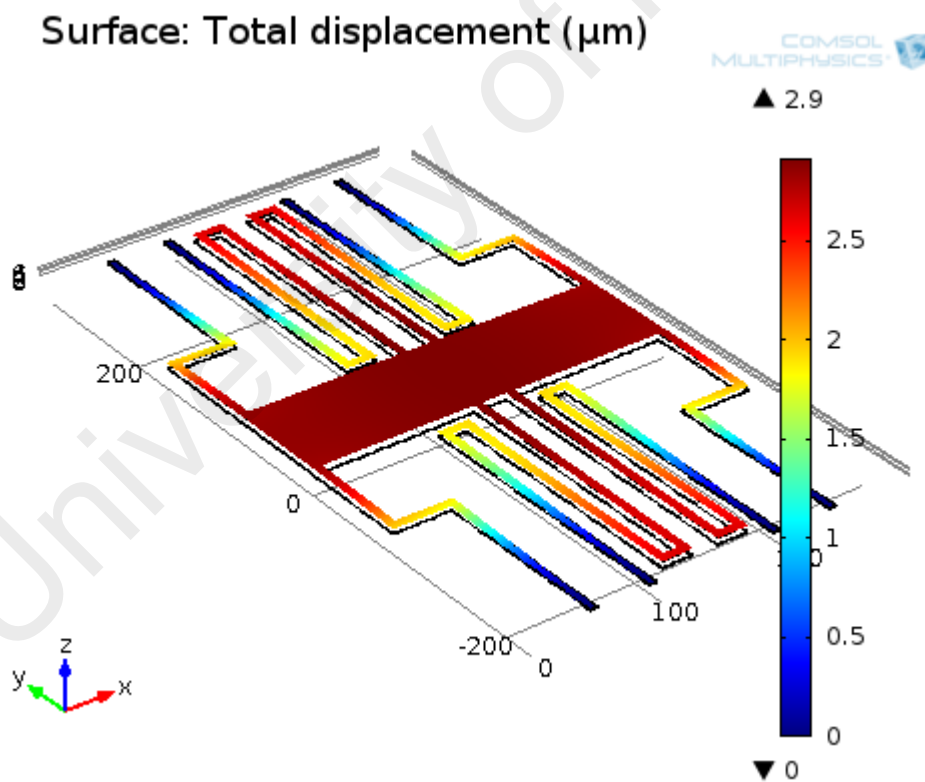
Figure 3.12: Mean S/N plot of MPI

The optimized geometric dimensions by the first two objectives were summarized in Table 3.11, where the pull-in voltage and switch-on time were calculated also for each model. It can be seen that by using WPCA technique, a trade-off model, namely Model C, is obtained, which has the spring constant of 0.2378 N/m and the first resonant frequency of 7.240 kHz.

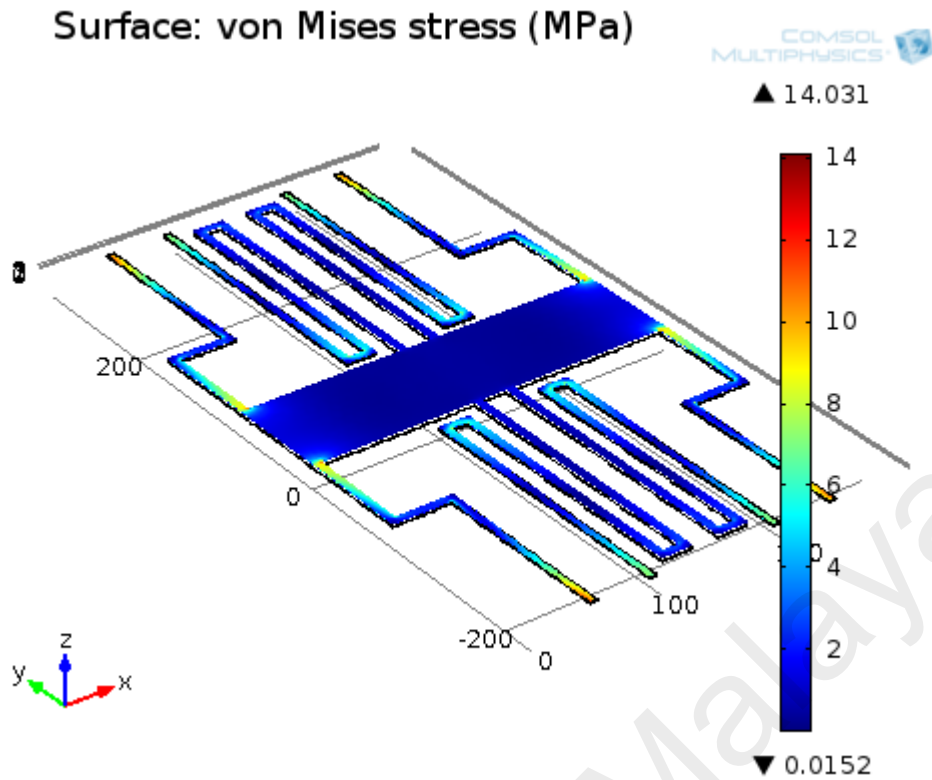
Table 3.11: Optimized results with different objectives

| Model | W_{beam} (μm) | $L1$ (μm) | $L2$ (μm) | $L3$ (μm) | k (N/m) | f_r (kHz) | Calculation | |
|---------|------------------------------|------------------------|------------------------|------------------------|-----------|-------------|-------------------|----------------------------|
| | | | | | | | $V_{pull-in}$ (V) | t_{ON} (μs) |
| Model A | $W_{beam2}=6$ | $(L1)_2=85$ | $(L2)_3=55$ | $(L3)_1=140$ | 0.2303 | 7.138 | 3.02 | 35.0 |
| Model B | $W_{beam3}=7$ | $(L1)_1=80$ | $(L2)_1=45$ | $(L3)_1=140$ | 0.3011 | 7.853 | 3.45 | 31.8 |
| Model C | $W_{beam2}=6$ | $(L1)_2=85$ | $(L2)_1=45$ | $(L3)_1=140$ | 0.2378 | 7.240 | 3.06 | 34.5 |

Following the optimization methodology flow, the last step is to test the optimized result (Model C: $W_{beam2}(L1)_2(L2)_1(L3)_1$) by first two objectives whether it fulfills the third objective or not. Physic model of Electromechanics in Comsol Multiphysics[®] was used again to estimate the maximum von Mises stress of the optimized result (Model C), with eight ends of beams fixed. The simulated maximum von Mises stress of 14.031MPa was presented in Figure 3.13 (b); when the switch is actuated, the membrane's displacement is at $2.9\mu\text{m}$ as shown in Figure 3.13 (a). This maximum von Mises stress does not reach to aluminum's yield stress of 15MPa to 20MPa (Howatson, 2012). Thus the deformation of the optimized structure can be operated in its elastic range. $W_{beam}=W_{beam2}=6\mu\text{m}$, $L1=(L1)_2=85\mu\text{m}$, $L2=(L2)_1=45\mu\text{m}$, $L3=(L3)_1=140\mu\text{m}$ is the final optimized results for the beams.



(a) Membrane's displacement of $2.9\mu\text{m}$



(b) Von Mises stress distribution

Figure 3.13: Membrane's maximum von Mises stress when switch is actuated

3.4.3 Structure Optimization for Low-Loss Design

Generally a large down-state capacitance is needed for high isolation while large capacitance ratio is desirable for good RF performance. A large down-state capacitance basically requires a large actuation area, thin dielectric layer and high relative-dielectric-constant material. Due to pinhole problems, the thickness of the dielectric layer cannot be less than $0.1\mu\text{m}$. For most standard CMOS process or CMOS-compatible processes, SiO_2 or silicon nitride (Si_3N_4) are the normal choices for the dielectric layer material (Dai & Chen, 2006; Guo et al., 2003); therefore it is not possible to use very high dielectric constant materials in the CMOS-compatible switch design. The easiest way to get large down-state capacitance is to make the actuation area big, as discussed in previous work (Badia, Buitrago, & Ionescu, 2012; Fouladi & Mansour, 2010; Kaynak et

al., 2010; Yang, Zareie, & Rebeiz, 2015). However, the big actuation area generally results in non-negligible up-state capacitance which generates high up-state return loss.

In our design, this phenomenon can be seen from the simulated S parameters of the capacitive RF-MEMS switch which will be discussed in Chapter 4, where the RF-MEMS switch's up-state return loss and insertion loss is obtained as -7.879dB and -0.5487dB at 20GHz, respectively; and the down-state return loss and isolation is -0.4557dB and -23.02dB at 20GHz, respectively. The switch's capacitance ratio is 90 with up-state capacitance of 87fF and down-state capacitance of 7.9pF, as shown in Table 3.3 Design 3. Obviously here the switch's capacitance ratio, insertion loss and isolation has met with the design specifications which was defined in Table 3.1; however the high up-state return loss (namely, >-10dB) does not satisfy with the design specification of less than -10dB since the up-state capacitance of 87fF exists.

The T-match and π -match techniques provide excellent solutions to compensate the large up-state bridge capacitance (Rebeiz, 2003h). A T-match RF-MEMS switch and π -match RF-MEMS switch which is based on the previous optimized RF-MEMS capacitive switch (named as classic RF-MEMS switch) and high-impedance T-line section is introduced separately. An optimization method based on obtaining the desirable S parameters with different lengths and widths of the high-impedance T-line sections for each topology is introduced and presented. The electrical modeling of the T-match and π -match RF-MEMS switches by extracting the lumped elements' values from FEM simulations has been developed. To the best of our knowledge, this is the first demonstration and optimization of the low-loss RF-MEMS capacitive switches at K-band frequencies.

3.4.3.1 T-Match RF-MEMS Switch

A. Design of T-match RF-MEMS switch

T-match approach is to associate high characteristic impedances on either side of the switch to compensate its equivalent low characteristic impedance (Rius, Coupez, Toutain, Person, & Legaud, 2000). Figure 3.14 shows the design of T-match RF-MEMS capacitive switch. Two short narrow T-line sections are added on both sides of the classic RF-MEMS switch which work as series inductors and provide high-impedance match at the design frequency. W_{hi-T} and L_{hi-T} represent the width and length of the high-impedance T-line section in the T-match RF-MEMS capacitive switch; here both high-impedance T-line sections have same dimensions. This technique also can be understood in the point of view of the CPW's characteristic impedance. For a lossless CPW, its characteristic impedance can be estimated by the square root of its equivalent inductance to capacitance. For the classic RF-MEMS capacitive switch at up-state condition, the non-negligible up-state capacitance increases the CPW's equivalent capacitance; in order to maintain the impedance of CPW (namely standard impedance of 50Ω) to be constant, the CPW's equivalent inductance should be increased as well. This will provide good RF performance of the RF-MEMS switch at up-state condition. Therefore, two short high-impedance T-line sections worked as inductance are added at the both sides of the classic RF-MEMS capacitive switch.

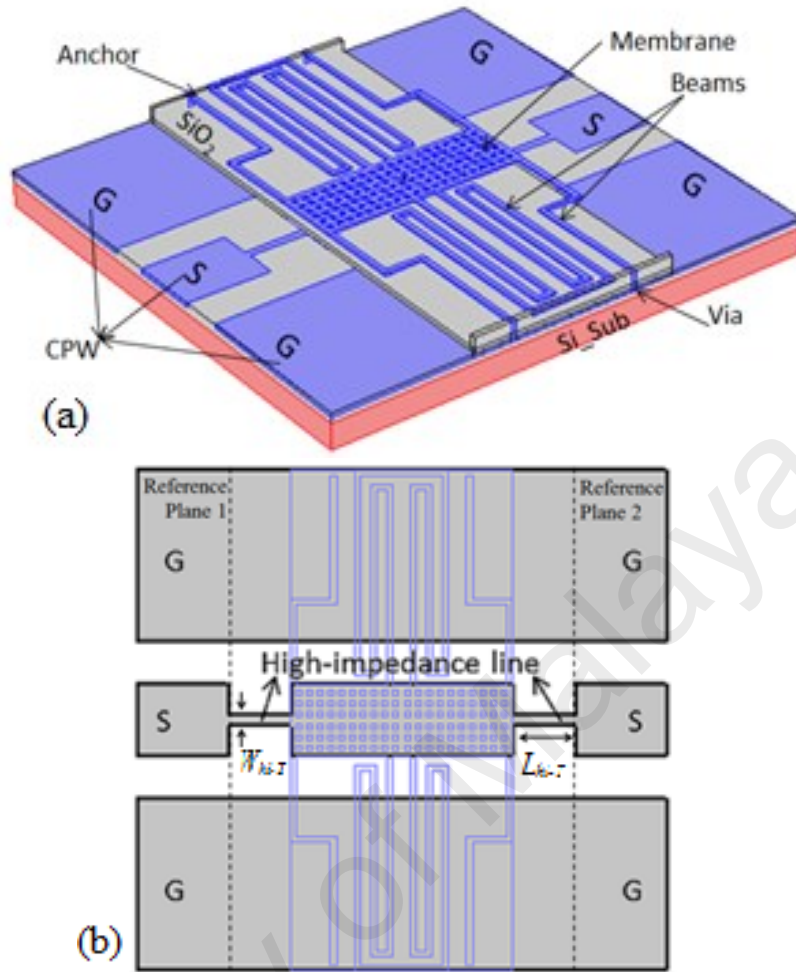


Figure 3.14: Design of T-match RF-MEMS capacitive switch (a) overall view, (b) top view

B. Optimization of high-impedance T-line sections

In order to get good RF performance and low-loss characteristics for the T-match RF-MEMS capacitive switch, the L_{hi-T} and W_{hi-T} of the high-impedance T-line sections need to be optimized. An optimization method based on the switch's RF performance (namely S parameters) simulation results has been conducted by using FEM simulator of AWR Design EnvironmentTM. The S parameters' expected ranges have been defined in Table 3.1 (namely $S11_{up} < -10dB$, $S21_{up} \& S11_{down} > -1dB$, and $S21_{down} < -15dB$) which are the optimized responses; meantime the smaller of $S11_{up}$ and $S21_{down}$ is better; the

larger of $S_{21_{up}}$ and $S_{11_{down}}$ is better. The optimized parameters are the length and width of the high-impedance T-line section (namely, L_{hi-T} and W_{hi-T}).

Table 3.12 shows the simulated S parameters of the T-match RF-MEMS capacitive switch with different values of L_{hi-T} and W_{hi-T} , where W_{hi-T} was varied from 10 μm to 70 μm and L_{hi-T} was varied from 10 μm to 310 μm . The simulated S parameters were obtained between Reference Plane 1 and 2, as shown in Figure 3.14 (b). The T-match RF-MEMS capacitive switch is optimized at 20GHz which follows the LC resonant frequency of the optimized classic RF-MEMS switch, as shown in Figure 4.19; in another word, all the simulated S parameters were obtained at frequency of 20GHz.

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Table 3.12: S parameters of the T-match RF-MEMS capacitive switch with different lengths and widths of high-impedance T-line section ($W_{hi-T}=10\mu\text{m}\sim 70\mu\text{m}$; $L_{hi-T}=10\mu\text{m}\sim 310\mu\text{m}$)

| W_{hi-T} (um) | L_{hi-T} (um) | 10 | 30 | 50 | 70 | 90 | 110 | 130 | 150 | 170 | 190 | 210 | 230 | 250 | 270 | 290 | 310 |
|-----------------|-------------------|---------|---------|---------|---------|---------|---------|----------------|----------------|----------------|----------------|---------|---------|---------|---------|---------|---------|
| 10 | $S11_{up}$ (dB) | -8.491 | -9.486 | -10.62 | -11.84 | -12.98 | -14.03 | -14.79 | -15.25 | -15.3 | -14.91 | -14.18 | -13.18 | -11.43 | -9.979 | -8.56 | -7.156 |
| | $S21_{up}$ (dB) | -0.4778 | -0.3688 | -0.2743 | -0.2042 | -0.1609 | -0.1291 | -0.1534 | -0.1184 | -0.1291 | -0.1859 | -0.233 | -0.3988 | -0.6312 | -0.8191 | -1.104 | -1.465 |
| | $S11_{down}$ (dB) | -0.5059 | -0.5437 | -0.5794 | -0.6065 | -0.6253 | -0.6245 | -0.679 | -0.6184 | -0.597 | -0.619 | -0.5977 | -0.6641 | -0.6355 | -0.6138 | -0.5936 | -0.5716 |
| | $S21_{down}$ (dB) | -23.01 | -21.98 | -21.47 | -21.88 | -22.63 | -23.53 | -25.14 | -27.19 | -28.79 | -28.86 | -28.73 | -26.74 | -25.29 | -24.4 | -23.76 | -23.18 |
| 20 | $S11_{up}$ (dB) | -8.289 | -9.098 | -10 | -10.86 | -11.71 | -12.42 | -12.92 | -13.13 | -13.05 | -12.7 | -12.11 | -11.33 | -9.941 | -8.741 | -7.559 | -6.352 |
| | $S21_{up}$ (dB) | -0.4988 | -0.3958 | -0.3024 | -0.2386 | -0.1889 | -0.1528 | -0.174 | -0.1372 | -0.1483 | -0.1738 | -0.2195 | -0.4289 | -0.6713 | -0.8734 | -1.174 | -1.553 |
| | $S11_{down}$ (dB) | -0.4848 | -0.5087 | -0.5282 | -0.5399 | -0.5472 | -0.537 | -0.5948 | -0.5246 | -0.5082 | -0.496 | -0.5166 | -0.6 | -0.5825 | -0.5654 | -0.5448 | -0.5246 |
| | $S21_{down}$ (dB) | -23.04 | -22.12 | -21.6 | -21.95 | -22.71 | -23.68 | -25.21 | -27.05 | -28.42 | -28.52 | -27.06 | -24.96 | -23.33 | -22.41 | -21.72 | -21.14 |
| 30 | $S11_{up}$ (dB) | -8.179 | -8.871 | -9.607 | -10.37 | -11.01 | -11.54 | -11.92 | -12 | -11.84 | -11.48 | -10.92 | -10.24 | -8.999 | -7.908 | -6.854 | -5.781 |
| | $S21_{up}$ (dB) | -0.51 | -0.4164 | -0.3322 | -0.2654 | -0.2224 | -0.1875 | -0.2083 | -0.1744 | -0.1864 | -0.2217 | -0.3095 | -0.5016 | -0.755 | -0.9798 | -1.297 | -1.698 |
| | $S11_{down}$ (dB) | -0.4736 | -0.4906 | -0.5074 | -0.5101 | -0.5176 | -0.5046 | -0.5574 | -0.4907 | -0.4718 | -0.4982 | -0.4823 | -0.5832 | -0.5604 | -0.5491 | -0.5341 | -0.5213 |
| | $S21_{down}$ (dB) | -22.99 | -22.06 | -21.51 | -21.92 | -22.55 | -23.68 | -25.12 | -27.12 | -28.04 | -27.17 | -26.3 | -24.01 | -22.44 | -21.37 | -20.62 | -20.01 |
| 40 | $S11_{up}$ (dB) | -8.101 | -8.705 | -9.375 | -9.977 | -10.53 | -10.95 | -11.21 | -11.22 | -11.03 | -10.65 | -10.08 | -9.455 | -8.31 | -7.31 | -6.321 | -5.343 |
| | $S21_{up}$ (dB) | -0.5203 | -0.4347 | -0.3528 | -0.295 | -0.2508 | -0.2191 | -0.2465 | -0.2159 | -0.2315 | -0.2704 | -0.3713 | -0.5717 | -0.8487 | -1.089 | -1.427 | -1.864 |
| | $S11_{down}$ (dB) | -0.465 | -0.4794 | -0.4885 | -0.4895 | -0.499 | -0.4796 | -0.54 | -0.4654 | -0.4523 | -0.4766 | -0.4685 | -0.5693 | -0.5584 | -0.5486 | -0.5318 | -0.5279 |
| | $S21_{down}$ (dB) | -22.97 | -22.1 | -21.59 | -21.94 | -22.64 | -23.7 | -25.13 | -27.07 | -27.94 | -26.89 | -25.77 | -23.39 | -21.8 | -20.66 | -19.9 | -19.21 |
| 50 | $S11_{up}$ (dB) | -8.034 | -8.577 | -9.148 | -9.714 | -10.17 | -10.49 | -10.67 | -10.63 | -10.38 | -9.948 | -9.412 | -8.809 | -7.738 | -6.77 | -5.864 | -4.908 |
| | $S21_{up}$ (dB) | -0.5279 | -0.4484 | -0.3747 | -0.3162 | -0.2812 | -0.2512 | -0.2821 | -0.2517 | -0.2741 | -0.3585 | -0.4361 | -0.6552 | -0.9446 | -1.211 | -1.571 | -2.031 |
| | $S11_{down}$ (dB) | -0.4557 | -0.4668 | -0.4737 | -0.4763 | -0.4832 | -0.4651 | -0.5245 | -0.4564 | -0.4759 | -0.4645 | -0.4554 | -0.5658 | -0.5571 | -0.5455 | -0.5363 | -0.5331 |
| | $S21_{down}$ (dB) | -23.04 | -22.2 | -21.74 | -22.15 | -22.83 | -23.93 | -25.25 | -27.09 | -27.14 | -26.55 | -25.25 | -22.86 | -21.22 | -20.19 | -19.34 | -18.66 |
| 60 | $S11_{up}$ (dB) | -7.986 | -8.473 | -9.006 | -9.458 | -9.851 | -10.11 | -10.21 | -10.12 | -9.829 | -9.405 | -8.86 | -8.272 | -7.23 | -6.358 | -5.462 | -4.584 |
| | $S21_{up}$ (dB) | -0.5349 | -0.4619 | -0.3915 | -0.342 | -0.3053 | -0.2819 | -0.3177 | -0.2959 | -0.3257 | -0.413 | -0.5002 | -0.7308 | -1.051 | -1.324 | -1.717 | -2.212 |
| | $S11_{down}$ (dB) | -0.4499 | -0.466 | -0.4675 | -0.468 | -0.4724 | -0.4573 | -0.5131 | -0.4457 | -0.4641 | -0.4528 | -0.4515 | -0.5583 | -0.5585 | -0.5501 | -0.5391 | -0.5392 |
| | $S21_{down}$ (dB) | -22.88 | -21.91 | -21.55 | -21.9 | -22.62 | -23.63 | -25.11 | -27 | -27.13 | -26.61 | -25.06 | -22.71 | -20.99 | -19.82 | -19.02 | -18.26 |
| 70 | $S11_{up}$ (dB) | -7.944 | -8.383 | -8.838 | -9.283 | -9.593 | -9.779 | -9.832 | -9.681 | -9.36 | -8.895 | -8.363 | -7.786 | -6.78 | -5.911 | -5.095 | -4.234 |
| | $S21_{up}$ (dB) | -0.5398 | -0.4732 | -0.4098 | -0.3602 | -0.3333 | -0.3133 | -0.3542 | -0.3352 | -0.3702 | -0.4744 | -0.5673 | -0.8236 | -1.161 | -1.464 | -1.87 | -2.401 |
| | $S11_{down}$ (dB) | -0.4464 | -0.4536 | -0.4596 | -0.4581 | -0.4621 | -0.4443 | -0.4998 | -0.4703 | -0.4555 | -0.445 | -0.4404 | -0.5656 | -0.5588 | -0.547 | -0.5451 | -0.5439 |
| | $S21_{down}$ (dB) | -22.77 | -21.88 | -21.39 | -21.78 | -22.57 | -23.65 | -25.19 | -26.53 | -27.14 | -26.39 | -24.85 | -22.46 | -20.78 | -19.63 | -18.76 | -17.96 |

In Table 3.12, the blue results mean that at least one of the S parameters dose not fulfill the S parameters' design specifications with the corresponding setting of L_{hi-T} and W_{hi-T} , while the black results are located in the range of design specifications. L_{hi-T} and W_{hi-T} were chosen from 10 μm to 310 μm and 10 μm to 70 μm , respectively. The minimum value of 10 μm is set by the fabrication resolution of 10 μm . The L_{hi-T} 's maximum value of 310 μm was determined by the simulated trend of SII_{up} . From Table 3.12 it can be seen that when L_{hi-T} is larger than 170 μm , the SII_{up} starts to increase with L_{hi-T} 's increase. At the same time, the whole device's length should not be larger than 1mm for most MEMS devices. The W_{hi-T} 's maximum value of 70 μm was determined by the high-impedance compensation requirement. Figure 3.15 presents the simulated impedance of CPW with different width of the signal line by TXLINE 2003TM; the simulated result shows that the narrower signal line, the larger impedance of CPW is obtained. Therefore, in order to get larger impedance than the CPW's standard characteristic impedance of 50 Ω (Shea et al., 1971), the width of the T line should be at least less than 80 μm .

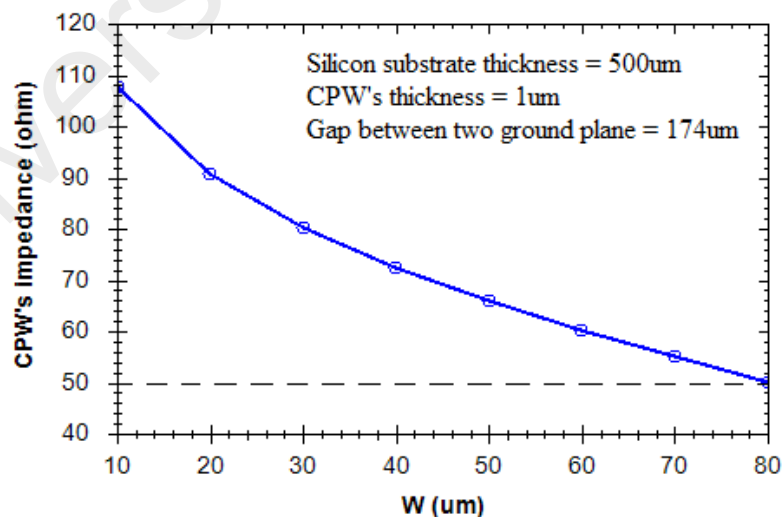


Figure 3.15: Impedance of CPW with different signal line width

In order to see and analyze the optimization results more clearly, the T-match RF-MEMS capacitive switch's up-state return loss, insertion loss, down-state return loss

and isolation have been plotted separately regarding to the different lengths and widths of the high-impedance T-line sections, as presented in Figure 3.16 to Figure 3.19, where the better results are highlighted in the gray dashed box for each S parameter.

Figure 3.16 shows that the up-state return loss when W_{hi-T} and L_{hi-T} are varied. It can be seen that narrower width of T-line section produce better up-state return loss and the better results of S_{11up} is obtained with $W_{hi-T}=10\mu\text{m}$ and $L_{hi-T}=130\mu\text{m}$ to $190\mu\text{m}$.

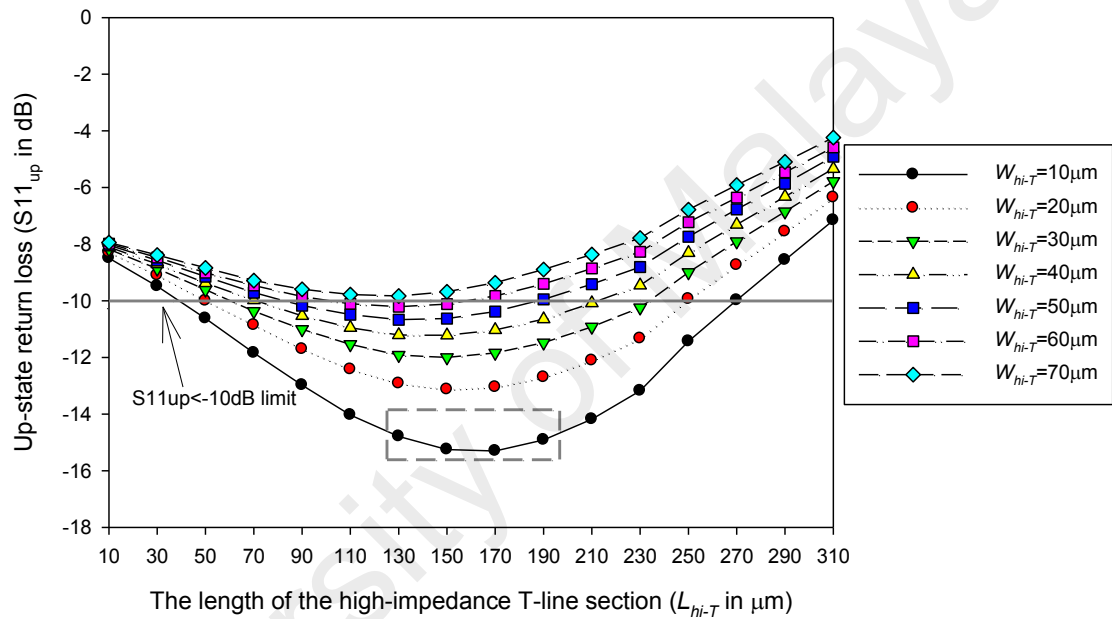


Figure 3.16: T-match RF-MEMS switch's up-state return loss with different lengths and widths of high-impedance T-line sections

Figure 3.17 shows that W_{hi-T} does not play an important role reducing the insertion loss. What is more crucial is to maintain L_{hi-T} less than $250\mu\text{m}$ to achieve $S_{21up} > -1\text{dB}$. The better insertion loss can be obtained when the high-impedance T-line sections' W_{hi-T} equals to $10\mu\text{m}$ and L_{hi-T} is from $110\mu\text{m}$ to $170\mu\text{m}$ (except $130\mu\text{m}$).

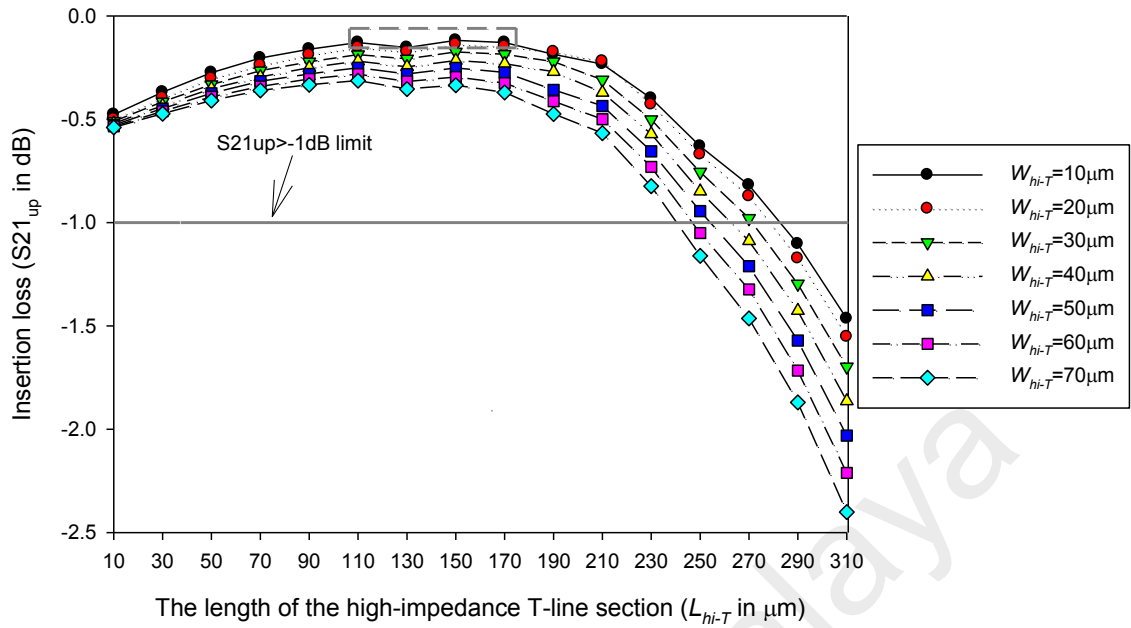


Figure 3.17: T-match RF-MEMS switch’s insertion loss with different lengths and widths of high-impedance T-line sections

Figure 3.18 shows that variation of W_{hi-T} and L_{hi-T} does not affect SII_{down} very much; the better SII_{down} values can be obtained with $W_{hi-T}=70\mu\text{m}$, $L_{hi-T}=110\mu\text{m}$ and $190\mu\text{m}$ to $210\mu\text{m}$. However, if look at the zoom in view of Figure 3.18, it shows that SII_{down} values only vary $\pm 0.3\text{dB}$; meantime all values of L_{hi-T} and W_{hi-T} comply with the requirements of $SII_{down} > -1\text{dB}$. Therefore, SII_{down} will not be the main considered response for the W_{hi-T} and L_{hi-T} ’s optimization.

Figure 3.19 shows the isolation loss when L_{hi-T} and W_{hi-T} are varied. It can be seen that smaller W_{hi-T} values produce better isolation; and the better isolation can be attained with $W_{hi-T}=10\mu\text{m}$ and $L_{hi-T}=170\mu\text{m}\sim 210\mu\text{m}$.

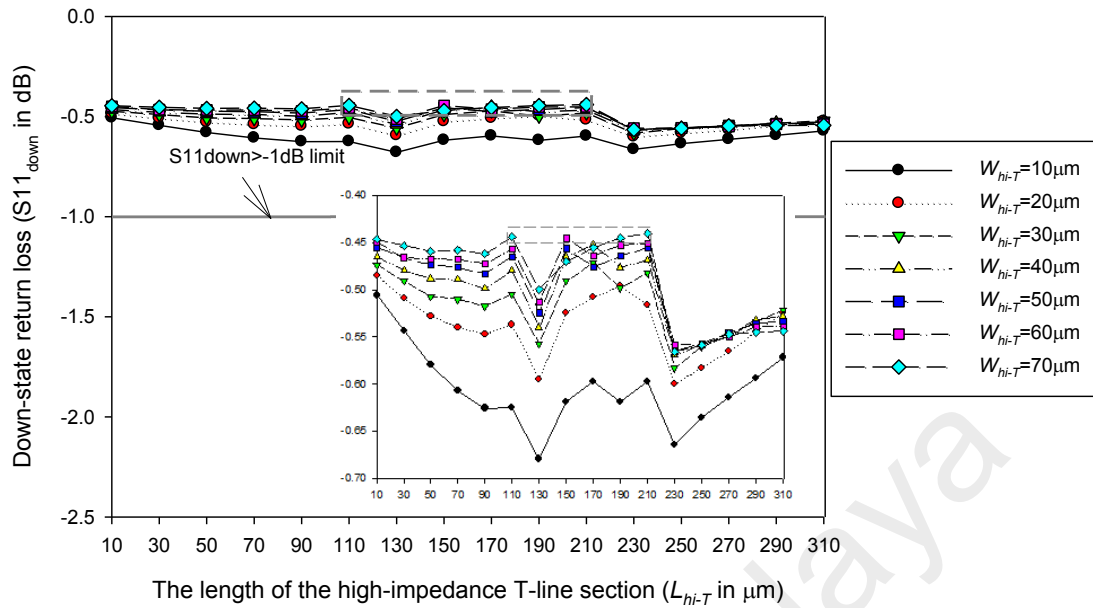


Figure 3.18: T-match RF-MEMS switch's down-state return loss with different lengths and widths of high-impedance T-line sections

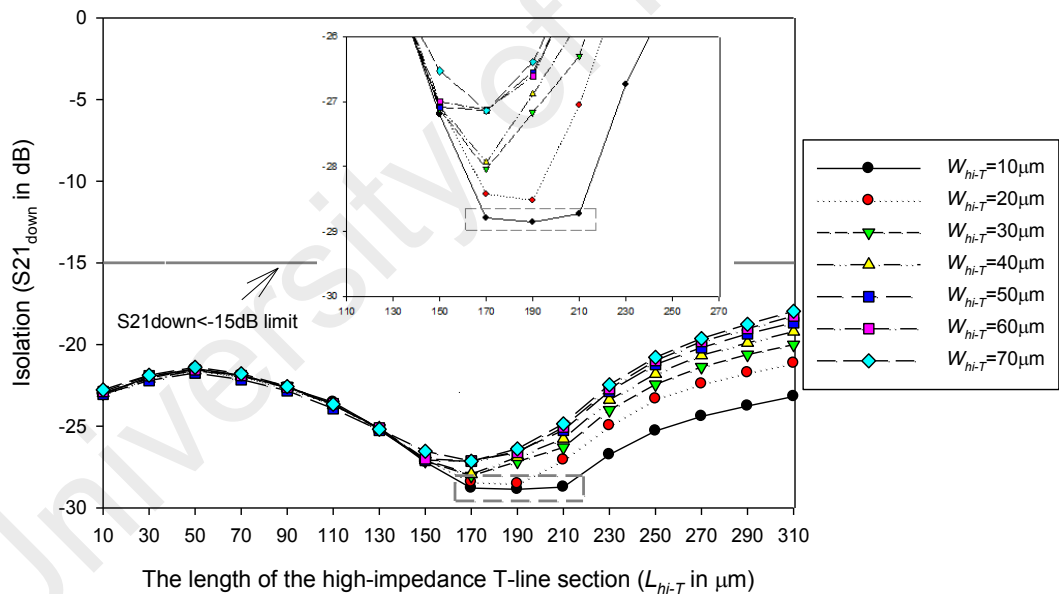


Figure 3.19: T-match RF-MEMS switch's isolation with different lengths and widths of high-impedance T-line sections

From Figure 3.16, Figure 3.17 and Figure 3.19, it can be seen that when W_{hi-T} is $10\mu\text{m}$, the up-state return loss, insertion loss and isolation of the T-match RF-MEMS switch shows the better results. Therefore, a further simulation of $W_{hi-T}=10\mu\text{m}$, $L_{hi-T}=110\mu\text{m}$ to $210\mu\text{m}$ with a smaller increment of $5\mu\text{m}$ was done, as shown in Table 3.13. Comparing with the S parameters of the classic RF-MEMS capacitive switch (namely

$S11_{up}=-7.879\text{dB}$, $S21_{up}=-0.5487\text{dB}$, $S11_{down}=-0.4557\text{dB}$ and $S21_{down}=-23.02\text{dB}$), the improvement of the T-match RF-MEMS capacitive switch at each different dimension of high-impedance T-line section was calculated and summarized in Table 3.13 by using (3.18) to (3.21). The negative values of $\Delta S11_{down}\%$ means the down-state return loss of the T-match RF-MEMS switch is degraded comparing with the classic RF-MEMS capacitive switch.

$$\Delta S11_{up}(\%) = \frac{|S11_{up-T-match}| - |S11_{up-classic}|}{|S11_{up-classic}|} \times 100\% \quad (3.18)$$

$$\Delta S21_{up}(\%) = \frac{|S21_{up-classic}| - |S21_{up-T-match}|}{|S21_{up-classic}|} \times 100\% \quad (3.19)$$

$$\Delta S11_{down}(\%) = \frac{|S11_{down-classic}| - |S11_{down-T-match}|}{|S11_{down-classic}|} \times 100\% \quad (3.20)$$

$$\Delta S21_{down}(\%) = \frac{|S21_{down-T-match}| - |S21_{down-classic}|}{|S21_{down-classic}|} \times 100\% \quad (3.21)$$

Where, $S11_{up-T-match}$, $S21_{up-T-match}$, $S11_{down-T-match}$ and $S21_{down-T-match}$ are the up-state return loss, insertion loss, down-state return loss and isolation of the T-match RF-MEMS capacitive switch, respectively, as shown in Table 3.13. $S11_{up-classic}$, $S21_{up-classic}$, $S11_{down-classic}$ and $S21_{down-classic}$ are the up-state return loss, insertion loss, down-state return loss and isolation of the classic RF-MEMS capacitive switch, respectively; their simulated values are $S11_{up-classic}=-7.879\text{dB}$, $S21_{up-classic}=-0.5487\text{dB}$, $S11_{down-classic}=-0.4557\text{dB}$ and $S21_{down-classic}=-23.02\text{dB}$, respectively (which were simulated and presented detailedly in Chapter 4). $\Delta S11_{up}$, $\Delta S21_{up}$, $\Delta S11_{down}$, and $\Delta S21_{down}$ are the S parameters' improvement of the T-match RF-MEMS capacitive switch comparing with the classic RF-MEMS capacitive switch.

Table 3.13: S parameters of the T-match RF-MEMS capacitive switch with different lengths of high-impedance T-line sections ($W_{hi-T}=10\mu\text{m}$; $L_{hi-T}=110\mu\text{m}\sim 310\mu\text{m}$)

| L_{hi-T} (um) | 110 | 115 | 120 | 125 | 130 | 135 | 140 | 145 | 150 | 155 |
|-------------------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| $S11_{up}$ (dB) | -14.03 | -14.25 | -14.47 | -14.63 | -14.79 | -14.93 | -15.00 | -15.14 | -15.25 | -15.28 |
| $S21_{up}$ (dB) | -0.13 | -0.12 | -0.12 | -0.16 | -0.15 | -0.12 | -0.12 | -0.12 | -0.12 | -0.12 |
| $S11_{down}$ (dB) | -0.62 | -0.62 | -0.62 | -0.69 | -0.68 | -0.63 | -0.62 | -0.62 | -0.62 | -0.61 |
| $S21_{down}$ (dB) | -23.60 | -24.06 | -24.32 | -24.65 | -25.14 | -25.71 | -26.42 | -26.65 | -27.19 | -27.61 |
| $\Delta S11_{up}$ (%) | 78.07 | 80.86 | 83.65 | 85.68 | 87.71 | 89.49 | 90.38 | 92.16 | 93.55 | 93.93 |
| $\Delta S21_{up}$ (%) | 76.47 | 77.51 | 77.95 | 71.26 | 72.04 | 78.35 | 77.67 | 77.86 | 78.42 | 77.84 |
| $\Delta S11_{down}$ (%) | -35.86 | -37.13 | -36.82 | -50.69 | -49.00 | -37.63 | -36.76 | -36.43 | -35.70 | -34.23 |
| $\Delta S21_{down}$ (%) | 2.52 | 4.52 | 5.65 | 7.08 | 9.21 | 11.69 | 14.77 | 15.77 | 18.11 | 19.94 |
| Total (%) | 121.20 | 125.76 | 130.43 | 113.33 | 119.97 | 141.89 | 146.07 | 149.35 | 154.39 | 157.48 |

| L_{hi-T} (um) | 160 | 165 | 170 | 175 | 180 | 185 | 190 | 195 | 200 | 205 | 210 |
|-------------------------|--------|--------|---------------|--------|--------|--------|--------|--------|--------|--------|--------|
| $S11_{up}$ (dB) | -15.30 | -15.30 | -15.30 | -15.25 | -15.14 | -14.99 | -14.91 | -14.76 | -14.60 | -14.39 | -14.18 |
| $S21_{up}$ (dB) | -0.12 | -0.12 | -0.13 | -0.16 | -0.17 | -0.18 | -0.19 | -0.19 | -0.21 | -0.22 | -0.23 |
| $S11_{down}$ (dB) | -0.61 | -0.60 | -0.60 | -0.59 | -0.63 | -0.62 | -0.62 | -0.61 | -0.61 | -0.60 | -0.60 |
| $S21_{down}$ (dB) | -28.06 | -28.43 | -28.79 | -29.05 | -28.67 | -28.85 | -28.86 | -28.99 | -28.86 | -28.87 | -28.73 |
| $\Delta S11_{up}$ (%) | 94.19 | 94.19 | 94.19 | 93.55 | 92.16 | 90.25 | 89.24 | 87.33 | 85.30 | 82.64 | 79.97 |
| $\Delta S21_{up}$ (%) | 77.40 | 77.24 | 76.47 | 70.68 | 69.42 | 67.98 | 66.12 | 64.70 | 62.42 | 60.34 | 57.54 |
| $\Delta S11_{down}$ (%) | -33.33 | -31.71 | -31.01 | -30.11 | -37.90 | -36.84 | -35.83 | -34.10 | -33.62 | -32.21 | -31.16 |
| $\Delta S21_{down}$ (%) | 21.89 | 23.50 | 25.07 | 26.19 | 24.54 | 25.33 | 25.37 | 25.93 | 25.37 | 25.41 | 24.80 |
| Total (%) | 160.15 | 163.22 | 164.72 | 160.32 | 148.22 | 146.71 | 144.89 | 143.86 | 139.47 | 136.18 | 131.15 |

In Table 3.13, it can be seen when L_{hi-T} is $170\mu\text{m}$, the total improvement percentage of the T-match RF-MEMS switch's S parameters is the largest which is about 164.72%. Therefore, the width of $10\mu\text{m}$ and length of $170\mu\text{m}$ of the optimized high-impedance T-line sections for the T-match RF-MEMS switch is determined.

3.4.3.2 Π -Match RF-MEMS Switch

A. Design of π -match RF-MEMS switch

The π -match circuit is another approach to achieve low loss for RF-MEMS capacitive switch. In this case, a short section of high-impedance T line is inserted between two classic RF-MEMS capacitive switches to result in an impedance match (Rebeiz, 2003i). Figure 3.20 presents the design of π -match RF-MEMS capacitive switch. There is a narrow T-line section added between the two classic RF-MEMS capacitive switches to provide a good high-impedance match at the design frequency of 20GHz. $W_{hi-\pi}$ and $L_{hi-\pi}$ represent the width and length of the high-impedance T-line section, respectively. Here the narrow T-line section is also served as a large series inductance to compensate the additional capacitance from the two shunt capacitive switches when the switches are at up-state condition and further to obtain the good RF performance for the CPW.

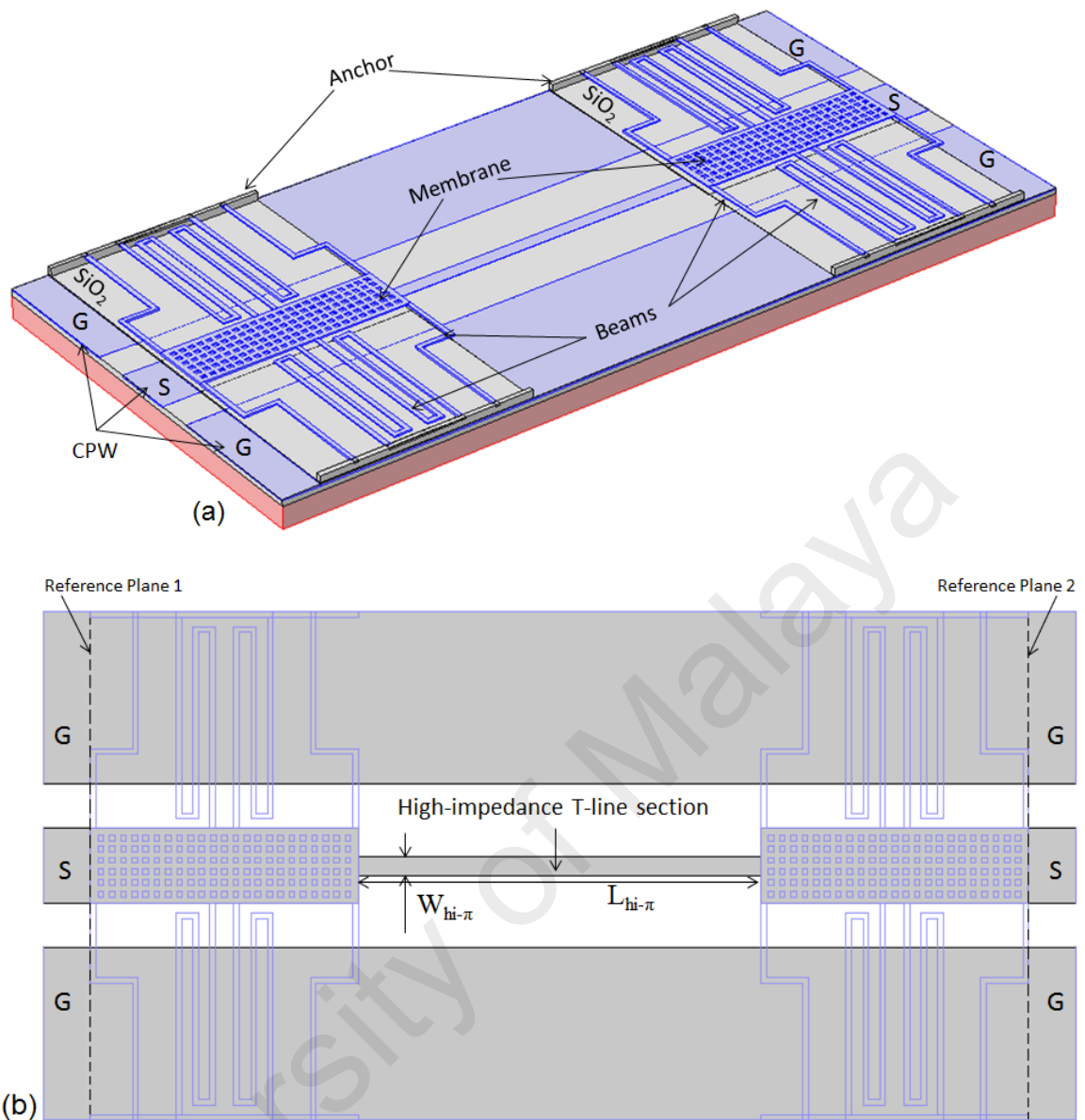


Figure 3.20: Design of π -match RF-MEMS capacitive switch (a) overall view, (b) top view

B. Optimization of middle high-impedance T-line section

In order to get good RF performance and low-loss characteristics for π -match RF-MEMS capacitive switch, the $L_{hi-\pi}$ and $W_{hi-\pi}$ of the high-impedance T-line section need to be optimized. The same optimization method based on the switch's RF performance (namely S parameters) simulation results were conducted by FEM simulator of AWR Design Environment TM, as which has been done for the T-match RF-MEMS switch's

optimization. Four optimized responses (namely $S11_{up}$, $S21_{up}$, $S11_{down}$, and $S21_{down}$) and two optimized parameters of $L_{hi-\pi}$ and $W_{hi-\pi}$ were investigated at operation frequency of 20GHz which is the design frequency of the optimized classic RF-MEMS capacitive switch.

Table 3.14 shows the simulated S parameters of the π -match RF-MEMS capacitive switch with different values of $L_{hi-\pi}$ and $W_{hi-\pi}$, where $W_{hi-\pi}$ was varied from 10 μ m to 70 μ m and $L_{hi-\pi}$ was varied from 10 μ m to 430 μ m. The simulated S parameters were obtained between Reference Plane 1 and 2, as shown in Figure 3.20 (b).

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Table 3.14: S parameters of the π -match RF-MEMS capacitive switch with different lengths and widths of high-impedance T-line sections ($W_{hi-\pi}=10\mu\text{m}\sim 70\mu\text{m}$; $L_{hi-\pi}=10\mu\text{m}\sim 430\mu\text{m}$)

| $W_{hi-\pi}$ (μm) | $L_{hi-\pi}$ (μm) | 10 | 30 | 50 | 70 | 90 | 110 | 130 | 150 | 170 | 190 | 230 | 250 | 270 | 290 | 310 | 350 | 370 | 390 | 410 | 430 |
|-----------------------------------|--------------------------------|--------|--------|--------|--------|-------|-------|-------|-------|--------|--------|--------|--------|--------|--------|---------------|---------------|---------------|---------------|---------------|---------------|
| 10 | $S11_{up}$ (dB) | -6.17 | -6.63 | -7.09 | -7.66 | -8.21 | -8.84 | -9.57 | -10.3 | -11.25 | -12.24 | -14.68 | -16.14 | -17.95 | -20.14 | -22.51 | -24.83 | -25.35 | -20.86 | -18.66 | -16.66 |
| | $S21_{up}$ (dB) | -1.07 | -0.96 | -0.86 | -0.77 | -0.68 | -0.60 | -0.52 | -0.45 | -0.38 | -0.33 | -0.25 | -0.22 | -0.20 | -0.18 | -0.18 | -0.19 | -0.20 | -0.24 | -0.27 | -0.31 |
| | $S11_{down}$ (dB) | -0.91 | -1.79 | -3.27 | -4.43 | -3.96 | -3.02 | -2.34 | -1.90 | -1.60 | -1.39 | -1.13 | -1.05 | -0.98 | -0.93 | -0.88 | -0.84 | -0.81 | -0.76 | -0.74 | -0.73 |
| | $S21_{down}$ (dB) | -14.32 | -11.43 | -9.64 | -9.17 | -9.93 | -11.2 | -12.4 | -13.6 | -14.37 | -15.62 | -17.17 | -17.80 | -18.39 | -19.00 | -19.45 | -19.93 | -20.27 | -21.02 | -21.36 | -21.58 |
| 20 | $S11_{up}$ (dB) | -6.10 | -6.45 | -6.80 | -7.22 | -7.62 | -8.06 | -8.58 | -9.08 | -9.67 | -10.28 | -11.73 | -12.46 | -13.41 | -14.43 | -15.53 | -16.93 | -18.43 | -22.39 | -24.75 | -26.51 |
| | $S21_{up}$ (dB) | -1.09 | -0.99 | -0.91 | -0.83 | -0.76 | -0.69 | -0.61 | -0.54 | -0.48 | -0.43 | -0.32 | -0.29 | -0.25 | -0.21 | -0.19 | -0.17 | -0.15 | -0.13 | -0.12 | -0.13 |
| | $S11_{down}$ (dB) | -0.82 | -1.44 | -2.50 | -3.83 | -4.45 | -3.93 | -3.14 | -2.52 | -2.08 | -1.76 | -1.37 | -1.25 | -1.14 | -1.07 | -1.00 | -0.95 | -0.91 | -0.84 | -0.82 | -0.79 |
| | $S21_{down}$ (dB) | -14.78 | -12.11 | -10.25 | -9.22 | -9.17 | -9.87 | -10.9 | -12.0 | -13.07 | -14.03 | -15.70 | -16.36 | -17.08 | -17.66 | -18.23 | -18.67 | -19.08 | -19.95 | -20.24 | -20.54 |
| 30 | $S11_{up}$ (dB) | -6.05 | -6.34 | -6.63 | -6.97 | -7.29 | -7.63 | -8.03 | -8.43 | -8.88 | -9.33 | -10.35 | -10.86 | -11.50 | -12.17 | -12.86 | -13.67 | -14.56 | -16.68 | -17.98 | -19.81 |
| | $S21_{up}$ (dB) | -1.10 | -1.02 | -0.95 | -0.88 | -0.82 | -0.75 | -0.69 | -0.62 | -0.56 | -0.51 | -0.41 | -0.37 | -0.33 | -0.29 | -0.26 | -0.23 | -0.20 | -0.16 | -0.13 | -0.12 |
| | $S11_{down}$ (dB) | -0.78 | -1.26 | -2.03 | -3.15 | -4.26 | -4.48 | -3.90 | -3.23 | -2.64 | -2.20 | -1.65 | -1.47 | -1.34 | -1.23 | -1.14 | -1.07 | -1.01 | -0.93 | -0.89 | -0.86 |
| | $S21_{down}$ (dB) | -14.97 | -12.61 | -10.86 | -9.57 | -8.98 | -9.17 | -9.85 | -10.7 | -11.77 | -12.70 | -14.42 | -15.17 | -15.85 | -16.51 | -17.08 | -17.60 | -18.02 | -18.89 | -19.27 | -19.51 |
| 40 | $S11_{up}$ (dB) | -6.01 | -6.26 | -6.50 | -6.78 | -7.04 | -7.34 | -7.66 | -7.97 | -8.32 | -8.69 | -9.48 | -9.85 | -10.34 | -10.83 | -11.35 | -11.91 | -12.51 | -13.94 | -14.74 | -15.79 |
| | $S21_{up}$ (dB) | -1.11 | -1.04 | -0.98 | -0.92 | -0.86 | -0.81 | -0.75 | -0.69 | -0.64 | -0.59 | -0.49 | -0.46 | -0.41 | -0.37 | -0.33 | -0.30 | -0.27 | -0.22 | -0.19 | -0.17 |
| | $S11_{down}$ (dB) | -0.74 | -1.14 | -1.75 | -2.67 | -3.78 | -4.46 | -4.34 | -3.79 | -3.15 | -2.61 | -1.91 | -1.69 | -1.52 | -1.38 | -1.27 | -1.18 | -1.11 | -1.00 | -0.96 | -0.93 |
| | $S21_{down}$ (dB) | -15.23 | -13.00 | -11.36 | -9.99 | -9.16 | -9.00 | -9.34 | -10.0 | -10.92 | -11.81 | -13.57 | -14.32 | -14.98 | -15.68 | -16.28 | -16.81 | -17.28 | -18.22 | -18.60 | -18.92 |
| 50 | $S11_{up}$ (dB) | -5.98 | -6.19 | -6.39 | -6.64 | -6.86 | -7.11 | -7.37 | -7.64 | -7.93 | -8.22 | -8.86 | -9.16 | -9.53 | -9.91 | -10.30 | -10.75 | -11.17 | -12.21 | -12.79 | -13.53 |
| | $S21_{up}$ (dB) | -1.12 | -1.06 | -1.01 | -0.95 | -0.90 | -0.85 | -0.80 | -0.74 | -0.70 | -0.65 | -0.56 | -0.53 | -0.49 | -0.45 | -0.41 | -0.38 | -0.35 | -0.29 | -0.26 | -0.23 |
| | $S11_{down}$ (dB) | -0.71 | -1.04 | -1.54 | -2.30 | -3.28 | -4.17 | -4.50 | -4.22 | -3.64 | -3.06 | -2.21 | -1.93 | -1.72 | -1.55 | -1.41 | -1.30 | -1.22 | -1.09 | -1.03 | -0.99 |
| | $S21_{down}$ (dB) | -15.48 | -13.37 | -11.76 | -10.43 | -9.48 | -9.03 | -9.10 | -9.51 | -10.25 | -11.07 | -12.78 | -13.54 | -14.25 | -14.91 | -15.60 | -16.16 | -16.66 | -17.56 | -17.96 | -18.44 |
| 60 | $S11_{up}$ (dB) | -5.95 | -6.13 | -6.29 | -6.51 | -6.69 | -6.90 | -7.13 | -7.35 | -7.59 | -7.83 | -8.33 | -8.58 | -8.90 | -9.19 | -9.51 | -9.86 | -10.17 | -10.99 | -11.40 | -11.96 |
| | $S21_{up}$ (dB) | -1.13 | -1.08 | -1.03 | -0.98 | -0.94 | -0.90 | -0.85 | -0.80 | -0.76 | -0.72 | -0.64 | -0.60 | -0.56 | -0.53 | -0.49 | -0.46 | -0.43 | -0.37 | -0.34 | -0.31 |
| | $S11_{down}$ (dB) | -0.69 | -0.96 | -1.36 | -1.96 | -2.78 | -3.68 | -4.40 | -4.59 | -4.21 | -3.63 | -2.63 | -2.28 | -2.00 | -1.78 | -1.60 | -1.47 | -1.36 | -1.20 | -1.13 | -1.08 |
| | $S21_{down}$ (dB) | -15.64 | -13.66 | -12.14 | -10.83 | -9.80 | -9.12 | -8.83 | -9.00 | -9.49 | -10.18 | -11.75 | -12.52 | -13.28 | -13.96 | -14.61 | -15.24 | -15.73 | -16.69 | -17.12 | -17.45 |
| 70 | $S11_{up}$ (dB) | -5.92 | -6.08 | -6.21 | -6.40 | -6.56 | -6.74 | -6.92 | -7.11 | -7.32 | -7.51 | -7.94 | -8.14 | -8.37 | -8.61 | -8.87 | -9.15 | -9.40 | -10.04 | -10.37 | -10.78 |
| | $S21_{up}$ (dB) | -1.13 | -1.09 | -1.05 | -1.01 | -0.97 | -0.94 | -0.89 | -0.85 | -0.81 | -0.77 | -0.70 | -0.67 | -0.64 | -0.60 | -0.57 | -0.54 | -0.51 | -0.45 | -0.42 | -0.39 |
| | $S11_{down}$ (dB) | -0.67 | -0.91 | -1.24 | -1.73 | -2.40 | -3.22 | -4.04 | -4.55 | -4.50 | -4.06 | -3.01 | -2.60 | -2.26 | -2.00 | -1.79 | -1.63 | -1.50 | -1.30 | -1.22 | -1.15 |
| | $S21_{down}$ (dB) | -15.84 | -13.94 | -12.50 | -11.24 | -10.2 | -9.42 | -8.95 | -8.85 | -9.12 | -9.64 | -11.12 | -11.84 | -12.58 | -13.28 | -13.91 | -14.53 | -15.09 | -16.09 | -16.49 | -16.90 |

In Table 3.14, the blue values are the results which at least one of the S parameters has not satisfied the design specifications (namely $S1I_{up} < -10\text{dB}$, $S2I_{up}$ & $S1I_{down} > -1\text{dB}$ and $S2I_{down} < -15\text{dB}$) with the corresponding setting of $L_{hi-\pi}$ and $W_{hi-\pi}$; while the black values are the results which have met the design specifications. $L_{hi-\pi}$ and $W_{hi-\pi}$ were chosen from $10\mu\text{m}$ to $430\mu\text{m}$ and $10\mu\text{m}$ to $70\mu\text{m}$, respectively. The minimum value of $10\mu\text{m}$ is basically determined by fabrication limitations. The $L_{hi-\pi}$'s maximum value of $430\mu\text{m}$ was determined by the maximum dimension of the MEMS device which should be less than 1mm (Hsu, 2008). Here total length of the π -match RF-MEMS switch includes the length of two classic RF-MEMS switches together with the length of the high-impedance T-line section. The $W_{hi-\pi}$'s maximum value of $70\mu\text{m}$ was determined by the high-impedance compensation requirement, as mentioned and explained in section 3.4.3.1; for CPW, the narrower width of the T line, the higher impedance is obtained.

In order to observe and analyze the optimization results more clearly, the π -match RF-MEMS capacitive switch's up-state return loss, insertion loss, down-state return loss and isolation have been plotted separately regarding to the different lengths and widths of the high-impedance T-line sections, as displayed in Figure 3.21 to Figure 3.24, where the better results are highlighted in the gray dashed box for each S parameter.

Figure 3.21 shows up-state return loss of the π -match RF-MEMS switch with variations of $W_{hi-\pi}$ and $L_{hi-\pi}$. It can be seen that with the smaller value of $W_{hi-\pi}$, the better $S1I_{up}$ is obtained and the relatively good $S1I_{up}$ is obtained with $W_{hi-\pi}=10\mu\text{m}$ to $20\mu\text{m}$ and $L_{hi-\pi}=310\mu\text{m}$ to $430\mu\text{m}$.

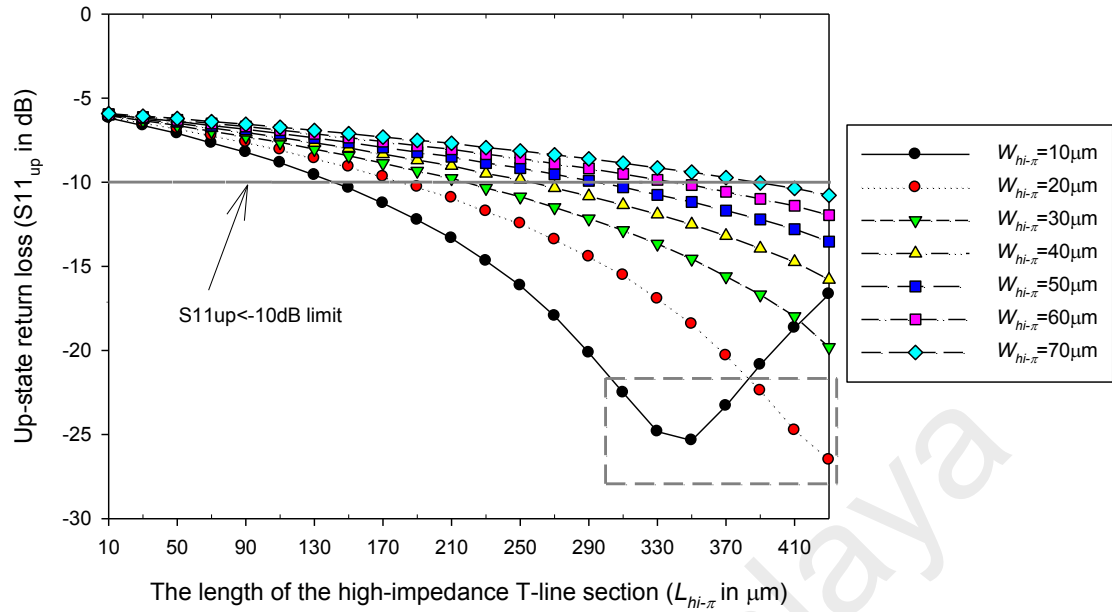


Figure 3.21: π -match RF-MEMS switch's up-state return loss with different lengths and widths of high-impedance T-line sections

Figure 3.22 shows insertion loss of the π -match RF-MEMS switch with different values of $W_{hi-\pi}$ and $L_{hi-\pi}$. It can be seen from the figure that when the $W_{hi-\pi}$ equals to $20\mu\text{m}$ and $L_{hi-\pi}$ is from $370\mu\text{m}$ to $430\mu\text{m}$, the insertion loss of the π -match RF-MEMS switch produce better results than the other conditions (namely $W_{hi-\pi}$ and $L_{hi-\pi}$ with other values).

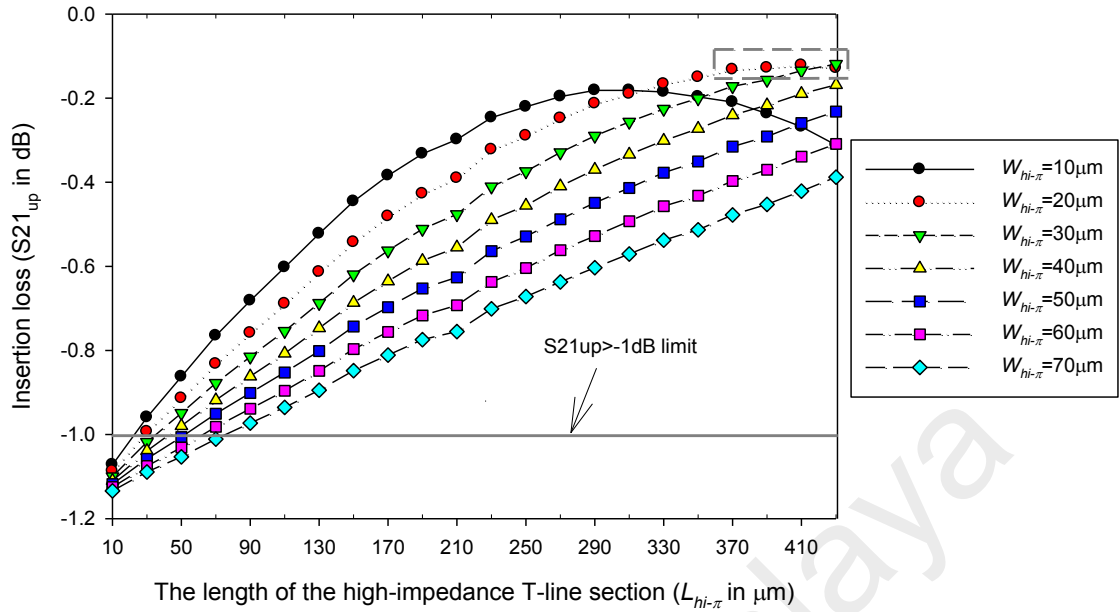


Figure 3.22: π -match RF-MEMS switch's insertion loss with different lengths and widths of high-impedance T-line sections

Figure 3.23 shows down-state return loss of the π -match RF-MEMS switch when $W_{hi-\pi}$ and $L_{hi-\pi}$ are varied. It can be seen that the better $S11_{down}$ values can be obtained with $W_{hi-\pi}=10\mu\text{m}$ and $L_{hi-\pi}=370\mu\text{m}$ to $430\mu\text{m}$.

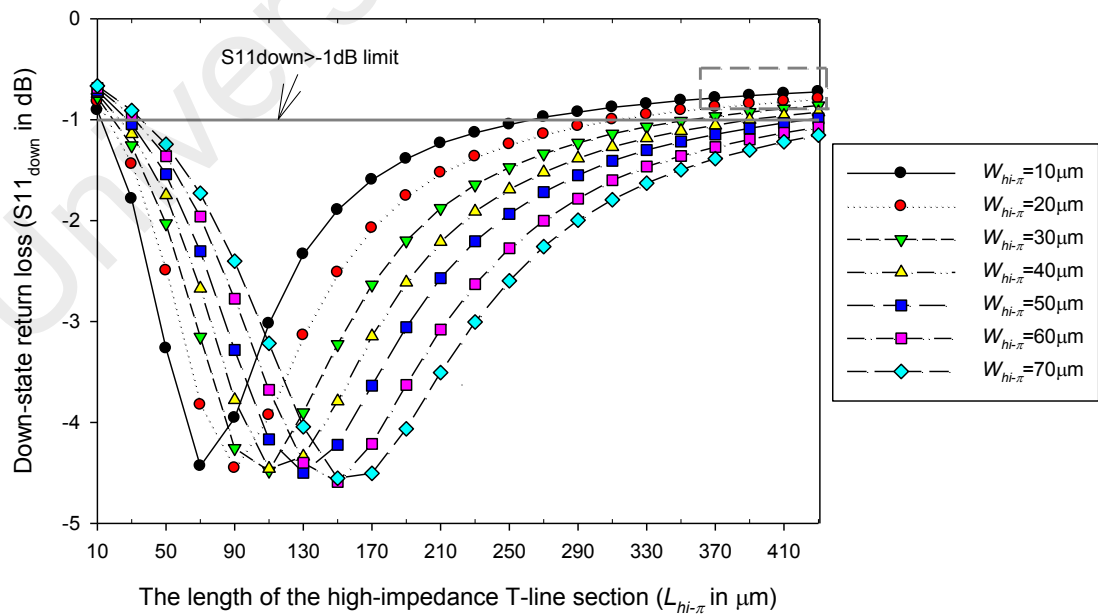


Figure 3.23: π -match RF-MEMS switch's down-state return loss with different lengths and widths of high-impedance T-line sections

Figure 3.24 presents isolation of the π -match RF-MEMS switch with varying of $W_{hi-\pi}$ and $L_{hi-\pi}$, it can be seen that the better isolation can be attained with $W_{hi-\pi}=10\mu\text{m}$ and $L_{hi-\pi}=370\mu\text{m}$ to $430\mu\text{m}$.

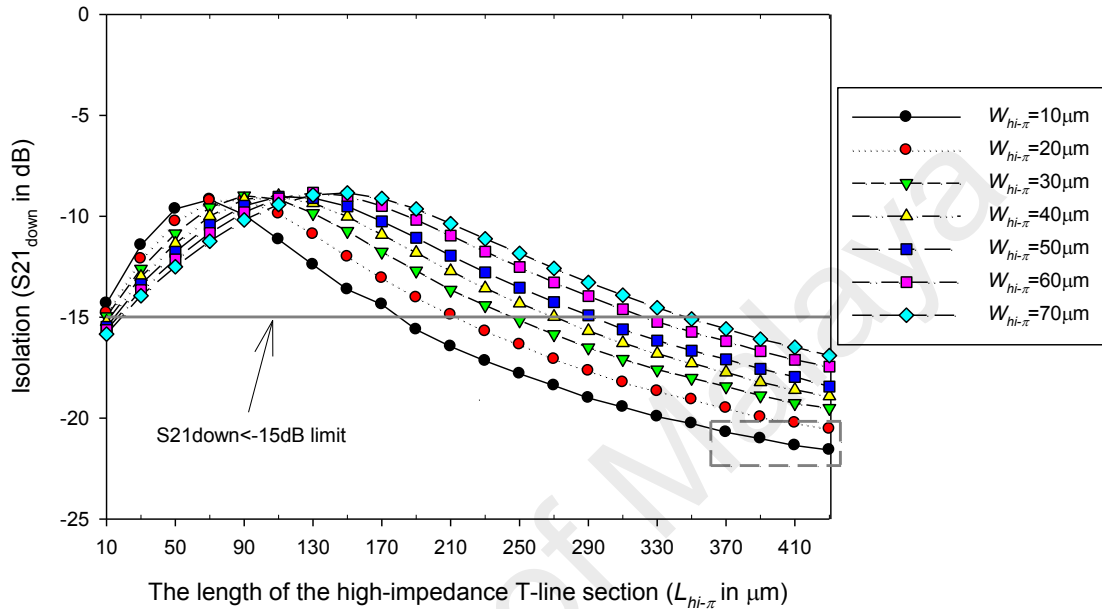


Figure 3.24: π -match RF-MEMS switch's isolation with different lengths and widths of high-impedance T-line sections

Considering all above four responses as well as $W_{hi-\pi}$ and $L_{hi-\pi}$'s setting with the better responses' result, a more detailed simulation with $W_{hi-\pi}=10\mu\text{m}$ to $20\mu\text{m}$, $L_{hi-\pi}=310\mu\text{m}$ to $430\mu\text{m}$ and increment of $5\mu\text{m}$ was done, as shown in Table 3.15. Comparing with the S parameters of the classic RF-MEMS capacitive switch (namely $S11_{up}=-7.879\text{dB}$, $S21_{up}=-0.5487\text{dB}$, $S11_{down}=-0.4557\text{dB}$ and $S21_{down}=-23.02\text{dB}$), the improvement of the π -match RF-MEMS capacitive switch at each different dimension of high-impedance T-line section was also calculated and included in Table 3.15 by using (3.18) to (3.21). The negative values of $\Delta S11_{down}$ and $\Delta S21_{down}$ mean that the down-state return loss and isolation of the π -match RF-MEMS switch is degraded comparing with the classic RF-MEMS capacitive switch.

Table 3.15: S parameters of the π -match RF-MEMS capacitive switch with different lengths and widths of high-impedance T-line sections ($W_{hi-\pi}=10\mu\text{m}\sim 20\mu\text{m}$; $L_{hi-\pi}=310\mu\text{m}\sim 430\mu\text{m}$)

| $W_{hi-\pi}$ (um) | $L_{hi-\pi}$ (um) | 310 | 315 | 320 | 325 | 330 | 335 | 340 | 345 | 350 | 355 | 360 | 365 | 370 |
|-------------------|-----------------------|--------|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|
| 10 | $S11_{up}$ (dB) | -22.5 | -23.3 | -23.8 | -24.3 | -24.8 | -25.2 | -25.5 | -25.5 | -25.4 | -25.0 | -24.6 | -23.8 | -23.3 |
| | $S21_{up}$ (dB) | -0.2 | -0.2 | -0.2 | -0.2 | -0.2 | -0.2 | -0.2 | -0.2 | -0.2 | -0.2 | -0.2 | -0.2 | -0.2 |
| | $S11_{down}$ (dB) | -0.9 | -0.9 | -0.9 | -0.8 | -0.8 | -0.8 | -0.8 | -0.8 | -0.8 | -0.8 | -0.8 | -0.8 | -0.8 |
| | $S21_{down}$ (dB) | -19.5 | -19.6 | -19.7 | -19.8 | -19.9 | -20.0 | -20.1 | -20.2 | -20.3 | -20.4 | -20.5 | -20.5 | -20.7 |
| 20 | $S11_{up}$ (dB) | -15.5 | -15.9 | -16.2 | -16.5 | -16.9 | -17.3 | -17.7 | -18.0 | -18.4 | -18.9 | -19.4 | -19.8 | -20.3 |
| | $S21_{up}$ (dB) | -0.2 | -0.2 | -0.2 | -0.2 | -0.2 | -0.2 | -0.2 | -0.2 | -0.2 | -0.1 | -0.1 | -0.1 | -0.1 |
| | $S11_{down}$ (dB) | -1.0 | -1.0 | -1.0 | -1.0 | -1.0 | -0.9 | -0.9 | -0.9 | -0.9 | -0.9 | -0.9 | -0.9 | -0.9 |
| | $S21_{down}$ (dB) | -18.2 | -18.3 | -18.4 | -18.5 | -18.7 | -18.8 | -18.9 | -19.0 | -19.1 | -19.3 | -19.4 | -19.4 | -19.5 |
| 10 | $\Delta S11_{up}\%$ | 185.7 | 195.8 | 201.9 | 208.7 | 215.1 | 219.6 | 223.0 | 224.2 | 221.7 | 217.7 | 211.7 | 202.4 | 195.7 |
| | $\Delta S21_{up}\%$ | 66.9 | 67.1 | 66.6 | 66.8 | 66.2 | 66.3 | 65.6 | 65.1 | 64.1 | 64.4 | 63.7 | 62.6 | 61.9 |
| | $\Delta S11_{down}\%$ | -92.6 | -90.5 | -88.4 | -86.5 | -85.4 | -83.2 | -81.3 | -79.4 | -77.8 | -76.6 | -75.4 | -74.5 | -72.1 |
| | $\Delta S21_{down}\%$ | -15.5 | -14.9 | -14.5 | -13.9 | -13.4 | -13.0 | -12.7 | -12.2 | -11.9 | -11.3 | -10.9 | -10.8 | -10.1 |
| | Total % | 144.5 | 157.6 | 165.6 | 175.0 | 182.6 | 189.6 | 194.5 | 197.7 | 196.1 | 194.2 | 189.1 | 179.7 | 175.4 |
| 20 | $\Delta S11_{up}\%$ | 97.1 | 101.7 | 105.7 | 109.5 | 114.9 | 119.2 | 124.4 | 128.6 | 133.9 | 139.8 | 145.6 | 151.3 | 157.8 |
| | $\Delta S21_{up}\%$ | 65.4 | 66.7 | 67.5 | 68.4 | 69.7 | 70.4 | 71.5 | 72.2 | 72.6 | 73.9 | 74.7 | 75.4 | 75.9 |
| | $\Delta S11_{down}\%$ | -119.3 | -116.7 | -114.2 | -111.0 | -108.6 | -106.2 | -104.3 | -101.8 | -99.2 | -97.5 | -95.5 | -93.8 | -91.9 |
| | $\Delta S21_{down}\%$ | -20.8 | -20.5 | -20.0 | -19.5 | -18.9 | -18.5 | -18.0 | -17.5 | -17.1 | -16.4 | -15.9 | -15.8 | -15.3 |
| | Total % | 22.3 | 31.2 | 39.0 | 47.5 | 57.0 | 64.9 | 73.6 | 81.4 | 90.2 | 99.8 | 108.9 | 117.1 | 126.5 |

Table 3.15, continued: S parameters of the π -match RF-MEMS capacitive switch with different lengths and widths of high-impedance T-line sections ($W_{hi-\pi}=10\mu\text{m}\sim 20\mu\text{m}$; $L_{hi-\pi}=310\mu\text{m}\sim 430\mu\text{m}$)

| $W_{hi-\pi}$ (um) | $L_{hi-\pi}$ (um) | 375 | 380 | 385 | 390 | 395 | 400 | 405 | 410 | 415 | 420 | 425 | 430 |
|-------------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|--------------|
| 10 | $S11_{up}$ (dB) | -22.6 | -22.1 | -21.5 | -20.9 | -20.3 | -20.2 | -19.1 | -18.7 | -18.1 | -17.6 | -17.1 | -16.7 |
| | $S21_{up}$ (dB) | -0.2 | -0.2 | -0.2 | -0.2 | -0.2 | -0.3 | -0.3 | -0.3 | -0.3 | -0.3 | -0.3 | -0.3 |
| | $S11_{down}$ (dB) | -0.8 | -0.8 | -0.8 | -0.8 | -0.8 | -0.7 | -0.7 | -0.7 | -0.7 | -0.7 | -0.7 | -0.7 |
| | $S21_{down}$ (dB) | -20.8 | -20.9 | -21.0 | -21.0 | -21.1 | -21.1 | -21.3 | -21.4 | -21.4 | -21.5 | -21.5 | -21.6 |
| 20 | $S11_{up}$ (dB) | -20.8 | -21.4 | -21.9 | -22.4 | -22.9 | -23.6 | -24.2 | -24.8 | -25.5 | -26.0 | -26.3 | -26.5 |
| | $S21_{up}$ (dB) | -0.1 | -0.1 | -0.1 | -0.1 | -0.1 | -0.1 | -0.1 | -0.1 | -0.1 | -0.1 | -0.1 | -0.1 |
| | $S11_{down}$ (dB) | -0.9 | -0.9 | -0.8 | -0.8 | -0.8 | -0.8 | -0.8 | -0.8 | -0.8 | -0.8 | -0.8 | -0.8 |
| | $S21_{down}$ (dB) | -19.6 | -19.7 | -19.8 | -20.0 | -20.0 | -20.1 | -20.1 | -20.2 | -20.2 | -20.3 | -20.4 | -20.5 |
| 10 | $\Delta S11_{up}$ % | 187.3 | 180.1 | 173.1 | 164.8 | 157.0 | 156.5 | 142.9 | 136.8 | 129.9 | 123.4 | 117.0 | 111.4 |
| | $\Delta S21_{up}$ % | 60.6 | 59.7 | 58.4 | 56.9 | 55.5 | 43.1 | 52.9 | 51.2 | 49.3 | 47.2 | 45.4 | 43.2 |
| | $\Delta S11_{down}$ % | -71.0 | -69.5 | -68.4 | -67.2 | -66.3 | -64.4 | -63.7 | -62.9 | -62.0 | -60.5 | -59.7 | -59.2 |
| | $\Delta S21_{down}$ % | -9.8 | -9.3 | -8.9 | -8.7 | -8.6 | -8.3 | -7.7 | -7.2 | -6.7 | -6.6 | -6.4 | -6.3 |
| | Total % | 167.2 | 161.0 | 154.2 | 145.7 | 137.7 | 127.0 | 124.5 | 117.9 | 110.4 | 103.5 | 96.3 | 89.2 |
| 20 | $\Delta S11_{up}$ % | 164.4 | 171.2 | 177.3 | 184.2 | 191.2 | 199.5 | 207.7 | 214.1 | 223.3 | 229.4 | 233.9 | 236.5 |
| | $\Delta S21_{up}$ % | 76.4 | 76.7 | 76.7 | 76.7 | 77.0 | 77.4 | 77.6 | 77.8 | 77.9 | 77.7 | 77.3 | 76.5 |
| | $\Delta S11_{down}$ % | -89.5 | -88.7 | -86.3 | -85.1 | -83.8 | -81.3 | -81.0 | -79.4 | -78.5 | -76.9 | -76.0 | -74.0 |
| | $\Delta S21_{down}$ % | -14.8 | -14.3 | -13.9 | -13.3 | -13.2 | -12.9 | -12.6 | -12.1 | -11.7 | -11.5 | -11.2 | -10.8 |
| | Total % | 136.5 | 145.0 | 153.7 | 162.4 | 171.2 | 182.8 | 191.7 | 200.4 | 210.9 | 218.7 | 224.1 | 228.2 |

In Table 3.15, it can be seen that among all the conditions, the largest total improvement percentage is 228.2% which can be obtained with $W_{hi-\pi}$ of 20 μm and $L_{hi-\pi}$ of 430 μm . Therefore, the optimized high-impedance T-line section of the π -match RF-MEMS switch has the width of 20 μm and length of 430 μm .

3.5 Implementation of RF-MEMS Switches into MEMS Phase Shifters

The nearly ideal electrical response of RF-MEMS switches have enabled many researchers to construct state-of-the-art switching circuits from 0.1 GHz all the way to 120 GHz (Rebeiz, 2003), such as MEMS phase shifter, reconfigurable antennas, tunable filters, MEMS-based voltage-controlled oscillators, MEMS varactors, power amplifier, switching networks, and digital capacitor banks, which can be further employed into lots of higher-level systems. RF phase shifters, as essential building blocks, can be utilized in lots of RF applications, such as phase array antennas (Puyal et al., 2008), phase discriminators, beam forming networks, power dividers and linearization of power amplifiers (Rosu).

Conventional RF phase shifters use GaAs MOSFET or p-i-n diode as switch due to their low costs; however most of them have high insertion loss (e.g. 5 - 7 dB) (Rebeiz, 2003a; Wang, Liu, & Li, 2010)) and appreciable DC power consumption (Scardelletti, Ponchak, & Varaljay, 2002) which limit the RF phase shifters' performance and usage. With the development of MEMS technology, RF phase shifters based on RF-MEMS switch network (namely MEMS phase shifters) are widely investigated and substitute for the traditional phase shifters on account of their simple structure, easy to be implemented, accurate phase shift ability (Huang, Bao, Li, Wang, & Du, 2015), low loss, low-power consumption and excellent linearity (Farinelli et al., 2010).

Basically, the MEMS phase shifters can be designed with several different kinds of topologies, such as switched-line, loaded-line, high-pass/low-pass and reflection phase shifters. The high-pass/low-pass phase shifter topology is ideal for the broad bandwidth and small size required for monolithic transmit/receive (T/R) modules (Morton & Papapolymerou, 2008); however, most designs are focused in X-band frequency which are hard to work in high frequency domain. Due to the necessity of many inductors in the circuit, the cost of the MEMS high-pass/low-pass phase shifter is quite high and fabrication procedures are relatively complicated. For the reflection-type phase shifters (Pillans et al., 2012; Polcawich, Judy, Pulskamp, Trolier-McKinstry, & Dubey, 2007), the transmission line could be very short, since this kind of phase shifters results in double phase delay per unit length as compared to other topologies; therefore a compact design can be achieved. However a 3-dB coupler is necessary with each switch which complicates the whole structure and increases the design area. Many papers present MEMS phase shifters by employing switched-line and loaded-line structures. The loaded-line phase shifter is mostly designed using DMTL structure (Bakri-Kassem, Mansour, & Safavi-Naeini, 2011; Bakri-Kassem, Mansour, & Safavi-Naeini, 2014; Dey & Koul, 2014; Reinke, Wang, Fedder, & Mukherjee, 2011); it can provide good return loss and insertion loss; meanwhile can be implemented easily using CPW or microstrip lines. For the MEMS switched-line phase shifter (Huang, Bao, Li, Wang, & Du, 2015), it is almost the most popular topology employed since it can be straightforward to design, fabricate and integrate with other microwave devices. However, most proposed DMTL and MEMS switched-line phase shifters need relatively high DC bias voltages, e.g. 15 to 90 V (Bartolucci et al., 2007; Rebeiz, 2003a; Pandey, Bansal, Jhanwar, Verma, & Rangra, 2015; Scardelletti, Ponchak, & Varaljay, 2002), and employ metal-contact RF-MEMS switches (Rebeiz, 2003a; Huang, Bao, Li, Wang, & Du, 2015; Pillans et al., 2012) which easily degrade the insertion loss with increased frequency band; also, in

order to reduce the substrate losses, glass (Borgioli, Liu, Nagra, & York, 2000), quartz (Barker & Rebeiz, 1998; Hayden & Rebeiz, 2003; Polcawich, Judy, Pulskamp, Trolier-McKinstry, & Dubey, 2007), GaAs (Pillans et al., 2012) and RO4350 substrate (Huang, Bao, Li, Wang, & Du, 2015) has been used, which are not the common materials to be used in the most standard CMOS control circuitry.

In order to integrate the RF-MEMS phase shifter into remote phased array antennas or on-the-move communication systems, low-voltage design is an important consideration; compared to use voltage-up converter. On the other hand, proposing a low-loss RF-MEMS phase shifter can eliminate the usage of power amplifier or low-noise amplifier level which generally is used in traditional RF phase shifter (Pillans et al., 2012). Therefore, in this project, we propose two kinds of low-voltage and low-loss RF-MEMS phase shifter designs using RF-MEMS switch network and CPW, which are MEMS switched-line phase shifter and DMTL phase shifter. By building the MEMS phase shifters on silicon wafer; they can be then directly integrated with other standard CMOS control circuitry on a same chip to further reduce the loss, complexity and cost.

For the rest of this section, the topologies, optimizations and layout designs of the MEMS switched-line phase shifter and DMTL phase shifter are detailed separately. Their simulation and analysis will be explained in the next chapter.

3.5.1 MEMS Switched-Line Phase Shifter's Design

Many MEMS switched-line phase shifters were constructed by using micro-stripe T line (Jian, Wei, Chen, Yong, & Le, 2006; Kingsley & Papapolymerou, 2006; Scardelletti, Ponchak, & Varaljay, 2002; Tan, Mihailovich, Hacker, DeNatale, & Rebeiz, 2003b) for easy integration with series switch. Here the CPW line was employed since

the shunt capacitive switches can be easily mounted on it. This structure could eliminate the need of big radial stubs and via holes, as well as have low radiation loss. Based on 1-bit switched-delay line and a resistive biasing network; a K-band low-voltage, low-loss, 3-bit MEMS phase shifter was constructed and optimized.

3.5.1.1 Topology and Optimization

The 3-bit switched-line phase shifter is made up of three sections of the 1-bit switched-delay line and a resistive biasing network. Figure 3.25 shows a 1-bit switched-line phase shifter, where the reference line has the phase shift of 0° ; and the delayed line has the phase shift of $\Delta\phi^\circ$. The 3-bit phase shifter, as shown in Figure 3.26 (a), realizes $2^3 = 8$ discrete phase states at interval of $360^\circ / 8 = 45^\circ$. The total length of each T line for different bit was simulated and summarized in Table 3.16. Figure 3.26 (b) and (c) model the RF-MEMS switch's two opposite states. The switch states in the reference line and the phase-delayed line are kept in opposite; while the switches connected in the same T line (reference line or phase delayed line), namely two series switches, are always keeping at the same state.

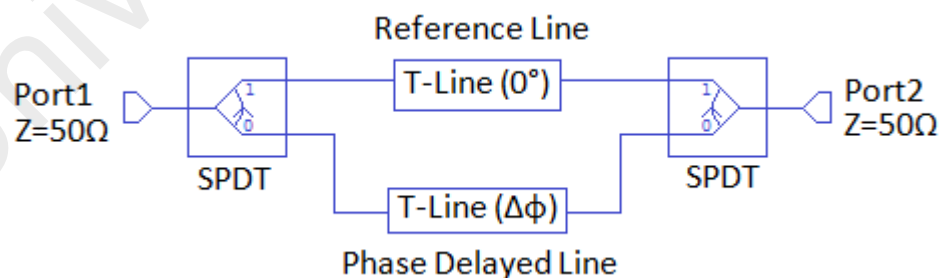
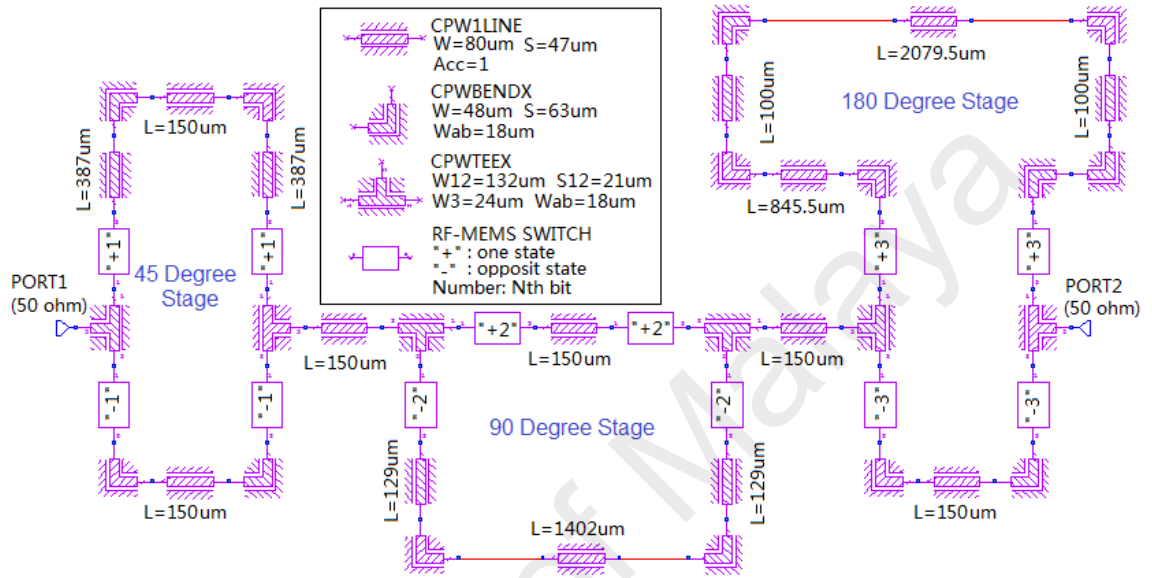


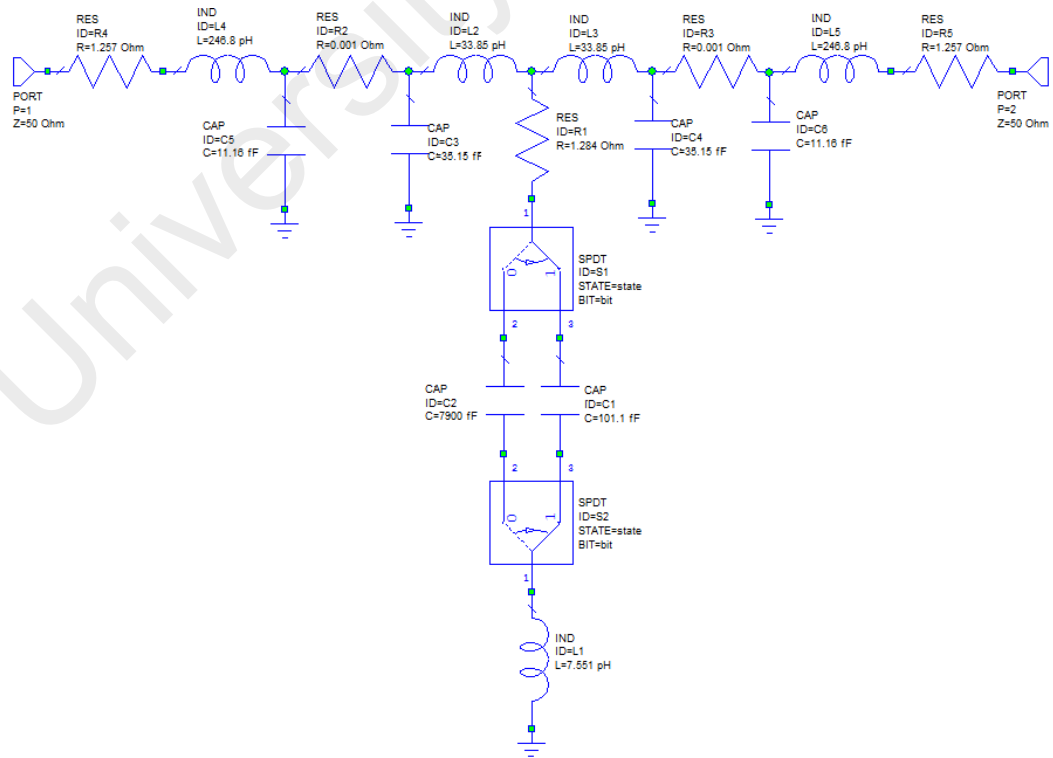
Figure 3.25: Structure of 1-bit switched-line phase shifter

Table 3.16: Total T-line length of each bit

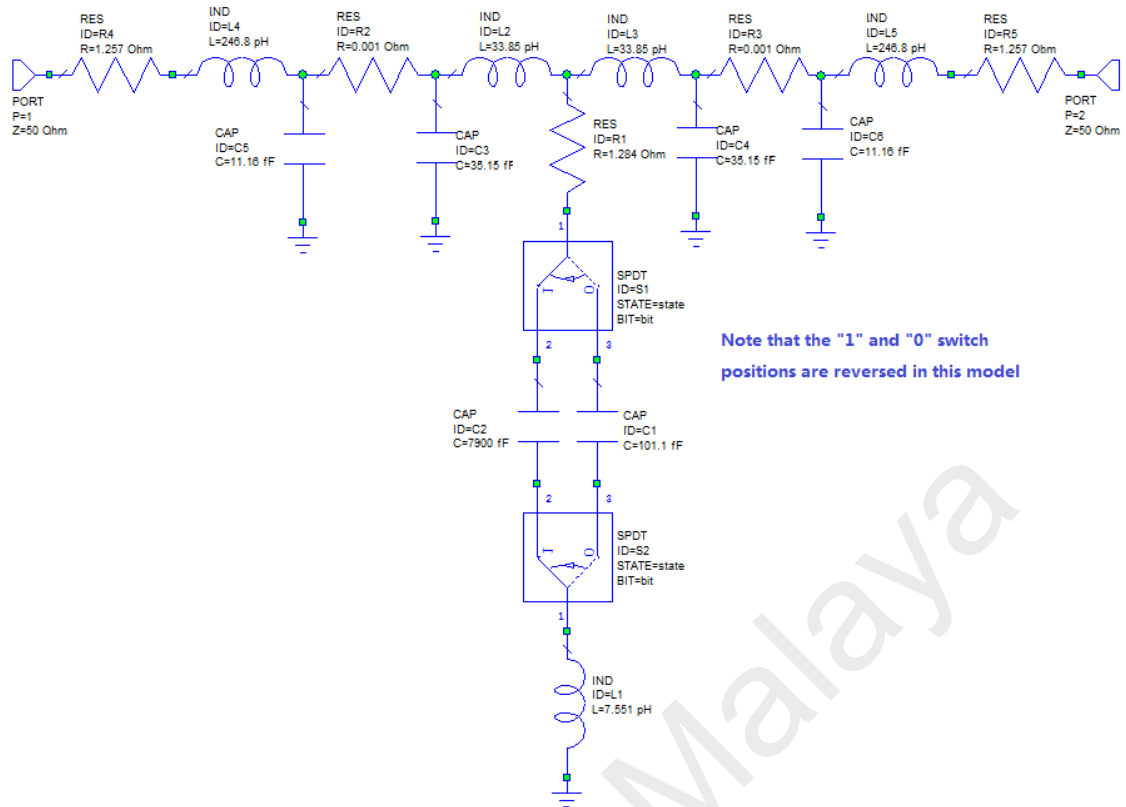
| Bit | Reference line | Phase delayed line |
|------------|-------------------|--------------------|
| 45 Degree | 150 μm | 924 μm |
| 90 Degree | 150 μm | 1660 μm |
| 180 Degree | 150 μm | 3125 μm |



(a) Whole circuit design



(b) Switch on at state "1"



(c) Switch off at state “1”

Figure 3.26: Circuit topology of 3-bit switched-line phase shifter

From Figure 3.26 (a), it can be seen that CPW’s 90° bend and Tee junctions are used in the MEMS switched-line phase shifter. In order to design the 90°-bend CPW with impedance of 50 Ω, the tune tool from Microwave office® has been used as shown in Figure 3.27, where the variables are the width of T line (W) and height of the air bridge (W_{ab}); the distance between two ground plane is kept as constant (174μm). The simulation results show that when the width of T line equals to 47.5μm, and the height of the bridge is 18μm, the impedance of the 90°-bend CPW is almost located at the point of 50Ω with frequency of 20GHz. S parameters of the 90°-bend CPW were displayed in Figure 3.28, where its return loss is -0.01318dB and isolation is -43.61dB.

CPWBENDX
 ID=TL1
 W=W1 um
 S=(174-W1)/2 um
 Wab=Wab um

W1=47.5
 Wab=18

CPW_SUB
 Er=11.9
 H=500 um
 T=1 um
 Rho=1.086
 Tand=0
 Hcover=100 um
 Hab=3 um
 Cover=0
 Gnd=0

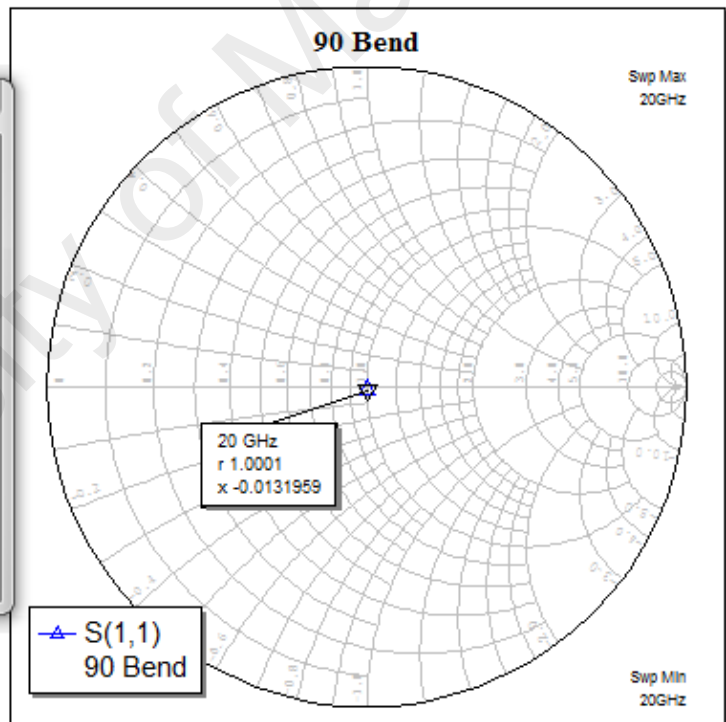
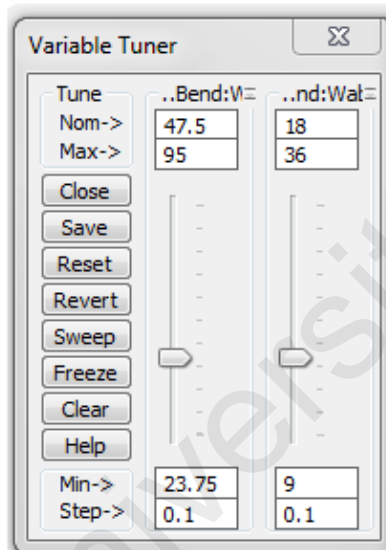
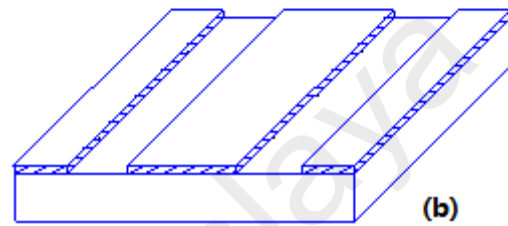
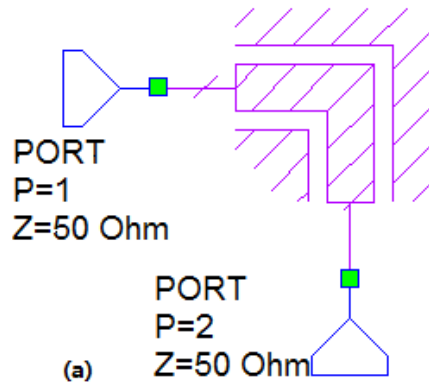


Figure 3.27: 90°-bend CPW's optimization (a) circuit modeling (b) substrate definition of CPW (c) impedance of 90°-bend of CPW

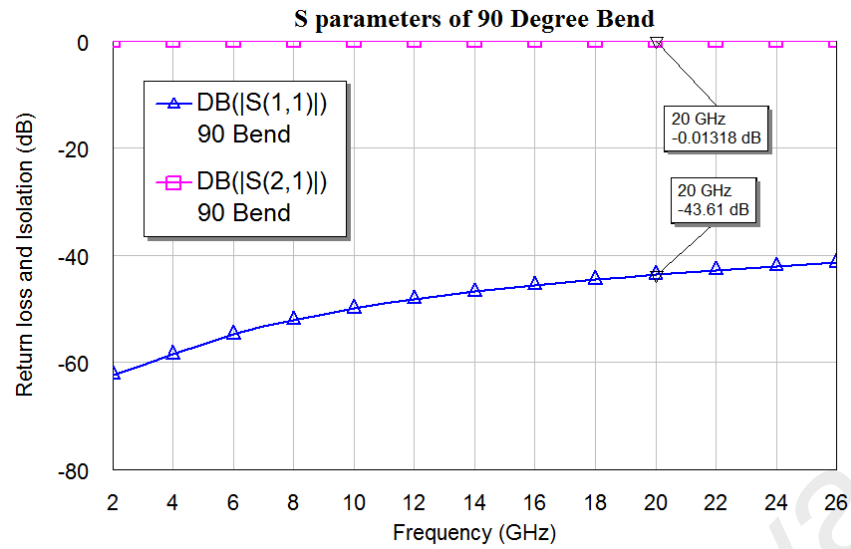


Figure 3.28: S parameters of the optimized 90°-bend CPW

The optimization of the CPW's Tee junction also has been done by tune tool of Microwave office[®], as shown in Figure 3.29. In the software, the variable parameters, namely $W12$, $S12$, $W3$ and W_{ab} have strict limitations as listed in (3.22) to (3.25).

$$0.25 \leq (W12 + 2 \times S12) / H_{sub} \leq 4.0 \quad (3.22)$$

$$0.1 \leq W12 / (W12 + 2 \times S12) \leq 0.9 \quad (3.23)$$

$$0.1 \leq W3 / (W12 + 2 \times S12) \leq 0.9 \quad (3.24)$$

$$0.1 \leq W_{ab} / (W12 + 2 \times S12) \leq 0.5 \quad (3.25)$$

Where, $W12$ is the width of signal line at port 1 and port 2; $S12$ is the gap width at port 1 and port 2; $W3$ is the width of signal line at port 3; W_{ab} is the width of air-bridge conductor at all ports; H_{sub} is the thickness of the substrate. Similar as the T-match RF-MEMS switch design, the thickness of the substrate is 500 μ m; the gap between two ground planes is 174 μ m, namely $W12 + 2 \times S12 = 174 \mu\text{m}$. The final optimized results for

both CPW's 90° bend and Tee junction with air bridges' dimensions are summarized in Table 3.17.

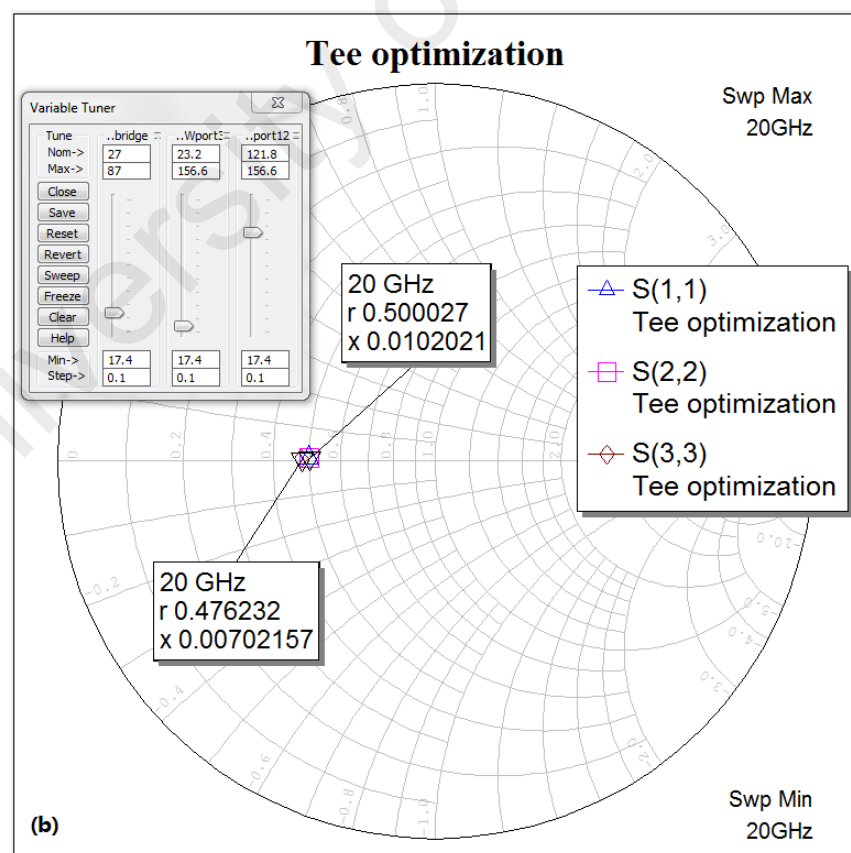
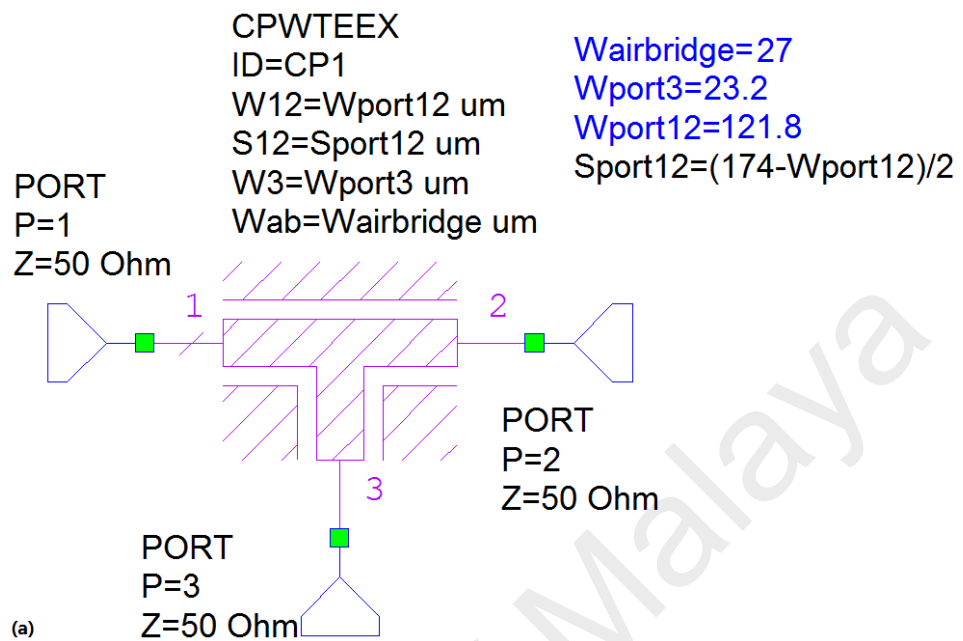


Figure 3.29: Tee junction's optimization (a) circuit modeling (b) impedance of tee junction

Table 3.17: Optimized dimensions of CPW discontinuities

| Parameter | 90° bend | | | | Tee junction | | | | |
|-------------------------|----------|-------|----------|----------|--------------|----------|-------|----------|----------|
| | W | S | W_{ab} | h_{ab} | W_{12} | S_{12} | W_3 | W_{ab} | h_{ab} |
| Value (μm) | 47.5 | 63.25 | 18 | 20 | 121.8 | 26.1 | 23.2 | 27 | 20 |

3.5.1.2 Layout Design

Figure 3.30 shows the complete layout of the MEMS 3-bit switched-line phase shifter. The G / S / G pads are RF signal’s input and output at both left and right sides. Totally three pairs of DC bias pads (i.e. A and A’, B and B’, C and C’) are included; each pair of them has one with V_{in} ($V_{in} > V_{pull-in}$) and the other one with 0V. The whole design area is about 6 mm \times 4 mm. Table 3.18 lists all the switches’ state for each proposed phase delay.

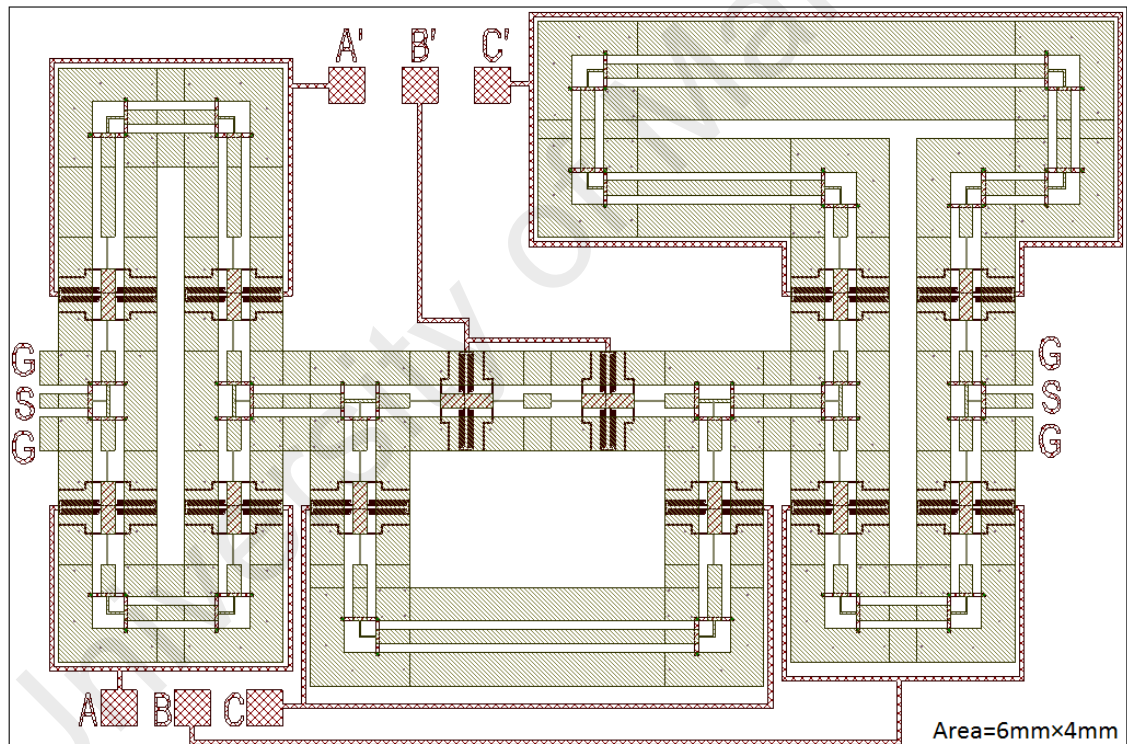


Figure 3.30: Layout of the RF-MEMS 3-bit switched-line phase shifter

Table 3.18 Phase delays with the RF-MEMS switches’ operation

| Applied voltage potential | | | | | | Phase shift |
|---------------------------|----|----|----|----|----|-------------|
| A | A' | B | B' | C | C' | |
| 0 | 4V | 4V | 0 | 0 | 4V | 0° |
| 4V | 0 | 4V | 0 | 0 | 4V | 45° |
| 0 | 4V | 0 | 4V | 0 | 4V | 90° |
| 4V | 0 | 0 | 4V | 0 | 4V | 135° |
| 0 | 4V | 4V | 0 | 4V | 0 | 180° |

| | | | | | | |
|----|----|----|----|----|---|------|
| 4V | 0 | 4V | 0 | 4V | 0 | 225° |
| 0 | 4V | 0 | 4V | 4V | 0 | 270° |
| 4V | 0 | 0 | 4V | 4V | 0 | 315° |

Note: assume $V_{in}=4V (\geq V_{pull-in}=3.04V)$

3.5.2 DMTL Phase Shifter's Design

DMTL phase shifter is constructed by using a high-impedance T line with characteristic impedance larger than 50Ω capacitively loaded by the periodic placement of MEMS bridges. This can be designed with many different types of T lines; however, using CPW to implement is one of the easiest approaches, especially for shunt RF-MEMS capacitive switches (Barker & Rebeiz, 2000). The RF-MEMS switches act as shunt capacitors or varactors. By applying DC bias voltage to the RF-MEMS switches, the distributed capacitive loading on the T line is increased which makes the phase velocity of the T line decreasing, thus providing a different phase shift.

In this part, a K-band 3-bit low-loss DMTL phase shifter based on the RF-MEMS capacitive switch and CPW is proposed and optimized which is followed by its layout considerations and design.

3.5.2.1 Topology and Optimization

The objective of this part is to design a 3-bit DMTL phase shifter operating at 20GHz on silicon substrate by using CPW and the RF-MEMS capacitive switches. Similar as the MEMS switched-line phase shifter's design, the 3-bit phase shifter should include three sections and each of them has phase shifter of 45° , 90° , and 180° , respectively. However, the difference from the MEMS switched-line phase shifter is for the DMTL phase shifter, the periodic spacing between each nearest two MEMS switches is constant. If the 45° -bit section is determined, the 90° -bit and 180° -bit section can be realized by cascading two and three of 45° -bit sections, respectively. Therefore, it can

be seen that the design of 45°-bit phase shift is the base of the whole work, which needs to finalize the CPW unloaded impedance, periodic spacing, up- and down-state capacitance, as well as the switch number of the 45°-bit section.

Here a design procedure from (Rebeiz, 2003j) has been referred, improved and specified in this work, which basically includes three steps.

First, using the design specifications of i) CPW unloaded impedance (Z_0) and ii) maximum return loss (S_{11}) determines the loaded impedances of the DMTL with the capacitive MEMS switches in the up- and down-state positions by (3.26) and (3.27) (Rebeiz, 2003j).

$$Z_{lu} = Z_0 \sqrt{\frac{1+\rho}{1-\rho}} \quad (3.26)$$

$$Z_{ld} = \frac{50^2}{Z_{lu}} \quad (3.27)$$

Where, the DMTL phase shifter is assumed to be fed by 50-Ω ports; Z_0 is CPW unloaded-line impedance; ρ is the maximum allowable reflection coefficient ($-1 < \rho < 1$).

Second, using the design specifications of i) substrate material (ϵ_{eff}) and ii) Bragg frequency (f_B) together with obtained Z_{lu} and Z_{ld} in the first step determines the values of the up-state capacitance (C_u), the capacitance ratio (C_{Ratio}), periodic spacing (s) and down-state capacitance (C_d) by equations of (3.28) to (3.30) (Rebeiz, 2003j).

$$C_u = \frac{Z_{ld}(Z_0^2 - Z_{lu}^2)}{Z_{lu}^2 \pi f_B Z_0^2} \quad (3.28)$$

$$S = \frac{Z_{ld}c}{\pi f_B Z_0 \sqrt{\epsilon_{eff}}} \quad (3.29)$$

$$C_{Ratio} = \left(\frac{Z_{lu}}{Z_{ld}} \right)^2 \frac{Z_0^2 - Z_{ld}^2}{Z_0^2 - Z_{lu}^2} \quad (3.30)$$

Third, the phase shift per unit length ($\Delta\phi$) can be calculated by using (3.31) (Rebeiz, 2003k; Jha, 2008). The phase shift between each nearest two MEMS switches can be obtained by multiplying $\Delta\phi$ and periodic spacing together. In the end, using 45° to divide the phase shift between each two switches can get the numbers of the periodic CPW and switch for 45° -bit section.

$$\Delta\phi = \frac{\omega Z_0 \sqrt{\epsilon_{eff}}}{c} \left(\frac{1}{Z_{ld}} - \frac{1}{Z_{lu}} \right) (Rad / m) = \frac{57.3\omega Z_0 \sqrt{\epsilon_{eff}}}{c} \left(\frac{1}{Z_{ld}} - \frac{1}{Z_{lu}} \right) (Degree / m) \quad (3.31)$$

It has been mentioned in (Rebeiz, 2003l) that optimum CPW unloaded-line impedance for frequency of 30GHz and silicon substrate occurs at $Z_0=50\sim 55\Omega$; and if taking into account the loss of the loading capacitor, an impedance of $65\sim 75\Omega$ is recommended. For our DMTL phase shifter's design, there is no any additional loading capacitor except MEMS switches, the silicon is chosen as the substrate ($\epsilon_{eff}=6.2$) too and the operation frequency (f_0) is at 20GHz. Then a bit wider range of the CPW unloaded-line impedance is considered for the optimization purpose, namely $50\sim 75\Omega$. For 3-bit DMTL phase shifters, typically, a maximum return loss of -15dB is required for each bit section. This is because that the DMTL is to be cascaded in 45° , 90° and 180° sections (Tan, Mihailovich, Hacker, DeNatale, & Rebeiz, 2003a); this ensures that input return loss will remain lower than -10dB (Barker & Rebeiz, 1998; Borgioli, Liu, Nagra, & York, 2000; Hayden & Rebeiz, 2003) for any state of the phase shifter. The return loss of -15dB for 1-bit section is assumed, which means the reflection coefficient

(ρ) should be 0.18 (Return Loss= $-20 \times \text{Log}(\rho)$). By employing the values of Z_0 and the 1-bit section's reflection coefficient together with (3.26) and (3.27), the range of up- and down-state loaded impedance (Z_{lu} and Z_{ld}) was determined, as shown in Table 3.19.

In the second step, the most important parameter to be decided is the Bragg frequency. The 3-bit DMTL phase shifter is designed to be operated at frequency of 20GHz. The Bragg frequency of 60GHz ($f_B=3 \times f$) is assumed to guarantee a wideband and robust performance of the DMTL phase shifter (Rebeiz, 2003m). Then the up-state capacitance (C_u), the capacitance ratio (C_{Ratio}), periodic spacing (s), and down-state capacitance (C_d) was obtained by (3.28) to (3.30), as shown in Table 3.19. The phase shift per unit length ($\Delta\phi$) is found from the change in the phase constant, as shown in (3.31). $\Delta\phi$ together with the phase shift between each two MEMS switches for different values of Z_0 was also calculated in Table 3.19. Then the numbers of the periodic CPW line (n) and MEMS switches ($n+1$) for 45°-bit was obtained. Table 3.19 has listed all the calculated results for Z_{lu} , Z_{ld} , C_u , s , C_{Ratio} , C_d , $\Delta\phi$ and n with the design specifications of $S_{11}=-15dB$, $Z_0 = 50 \sim 75\Omega$, $f_0 = 20GHz$, $f_B = 60GHz$ and silicon substrate. From this table it can be seen that when CPW unloaded impedance is 65 Ω , the periodic spacing is 309 μm , and the phase shift between each two MEMS switch is 22.5°, the number of switch for 45°-bit section is an integer number of two. Therefore, in Table 3.19 the fourth condition (No. 4) was chosen as the design parameter for 3-bit DMTL phase shifter operating at 20GHz.

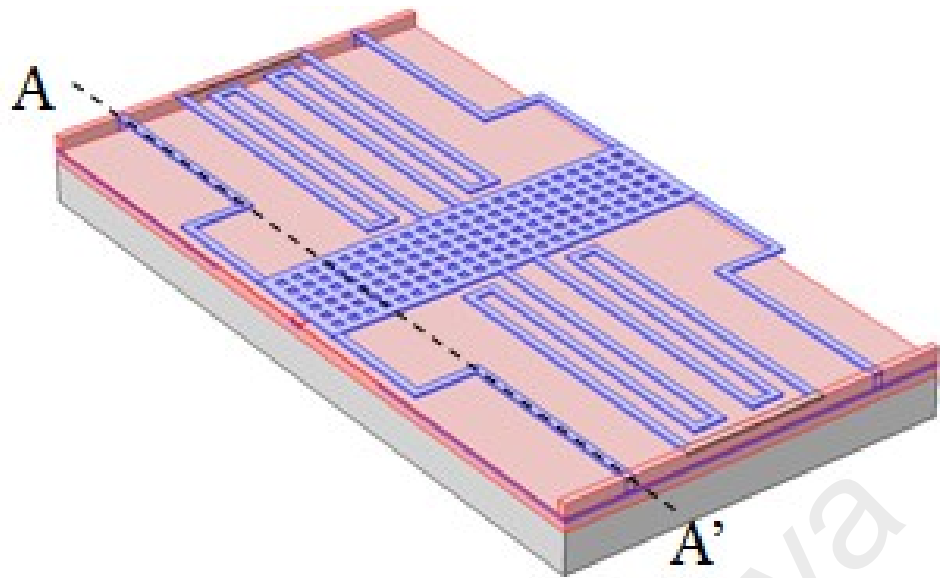
Table 3.19: Calculated C_u , s , C_{Ratio} , C_d , $\Delta\phi$ and n with different CPW unloaded impedance of 50~75 Ω

| No. | $S11$ (dB) | ρ | Z_0 (Ω) | Z_{lu} (Ω) | Z_{ld} (Ω) | f (GHz) | f_B (GHz) | C_u (fF) | s (μ m) | C_{Ratio} | C_d (fF) | $\Delta\phi$ ($^\circ$ /cm) | $s \times \Delta\phi$ ($^\circ$) | n |
|----------|------------|-------------|--------------------|-----------------------|-----------------------|-----------|-------------|-------------|----------------|-------------|--------------|------------------------------|------------------------------------|------------|
| 1 | 15 | 0.18 | 50 | 60 | 42 | 20 | 60 | 27.0 | 522 | 1.4 | 38.8 | 223.1 | 11.7 | 3.9 |
| 2 | 15 | 0.18 | 55 | 66 | 38 | 20 | 60 | 20.3 | 432 | 3.6 | 73.6 | 376.6 | 16.3 | 2.8 |
| 3 | 15 | 0.18 | 60 | 72 | 35 | 20 | 60 | 15.6 | 363 | 6.5 | 101.6 | 544.8 | 19.8 | 2.3 |
| 4 | 15 | 0.18 | 65 | 78 | 32 | 20 | 60 | 12.3 | 309 | 10.2 | 125.2 | 727.6 | 22.5 | 2.0 |
| 5 | 15 | 0.18 | 70 | 84 | 30 | 20 | 60 | 9.8 | 267 | 14.8 | 146.0 | 925.1 | 24.7 | 1.8 |
| 6 | 15 | 0.18 | 75 | 90 | 28 | 20 | 60 | 8.0 | 232 | 20.6 | 164.7 | 1137.1 | 26.4 | 1.7 |

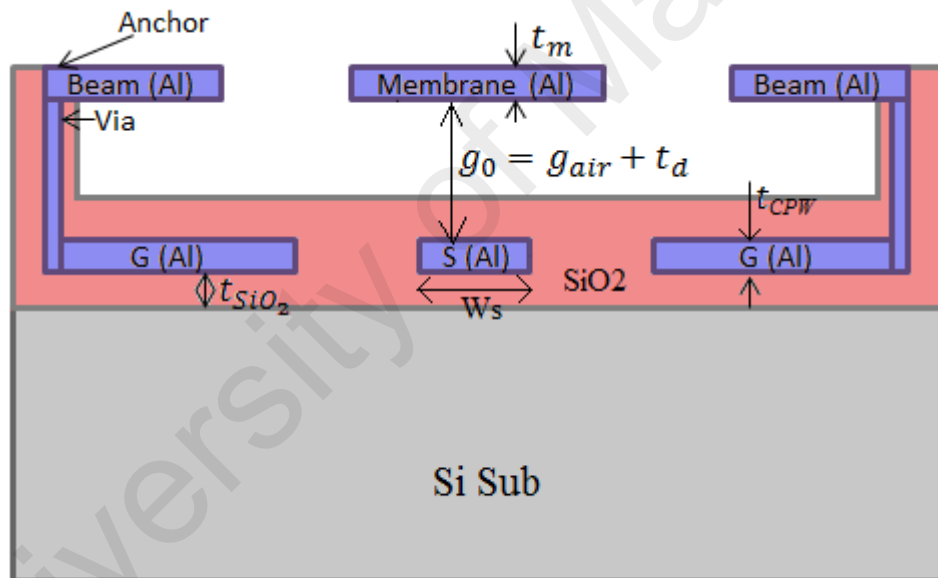
3.5.2.2 Layout Design

A. Capacitive RF-MEMS switch

From Table 3.19 it can be seen that, for the DMTL phase shifter, the up- and down-state capacitance values of the RF-MEMS capacitive switch should be 12.3fF and 125.2fF, respectively, which is much less than the previously proposed classic RF-MEMS switch's capacitance values (namely, Table 3.3 Design 3 $C_u=87fF$ and $C_d=7.9pF$). There are several methods for modifying the switch's capacitance (Borgioli, Liu, Nagra, & York, 2000), such as i) increasing the thickness of dielectric layer coating on the central conductor, ii) shrinking the size of the upper membrane, and iii) placing a discrete small capacitor (C_s) in series with MEMS switch and keeping $C_u \ll C_s \ll C_d$. Some previous works have employed the additional discrete series capacitor in their DMTL phase shifters; however the series capacitor increases the overall insertion loss of the phase shifter and the performance of the DMTL is dominated by the Q factor of the series capacitor (Rebeiz, 2003) which easily degrades the DMTL's accuracy. If shrinking the membrane area, it needs change the overall design of the proposed RF-MEMS switch, especially for beams and spring constant. In this work, the thicker dielectric layer on the signal line and a narrower signal line has been used together to reduce the capacitance of the RF-MEMS switch. Figure 3.31 presents the detail design of the modified RF-MEMS capacitive switch which is used in the DMTL phase shifter. The dimensions of the modified RF-MEMS capacitive switch is basically followed the optimized dimensions of the Design 3 in Table 2.3. The only changes are the width of the signal line (W_s), air gap (g_{air}) and thickness of the thin dielectric layer (t_d), as summarized in Table 3.20.



(a) Overall view



(b) Cross-section view from A-A'

Figure 3.31: Modified RF-MEMS capacitive switch for the 3-bit DMTL phase shifter

Table 3.20: Modified dimensions of the classic RF-MEMS switch for DMTL phase shifter

| Parameter | W_s (μm) | g_{air} (μm) | t_d (μm) |
|-----------|-------------------------|-----------------------------|-------------------------|
| Value | 10 | 1.85 | 0.79 |

B. DMTL phase shifter

Figure 3.32 presents the complete layout of the 3-bit DMTL phase shifter which consists of 21 modified RF-MEMS capacitive switches, a 65- Ω CPW, two DC blocks between each bit, two 50- Ω feeds, three DC bias pads, and several high-resistance DC bias lines. The switch numbers for 45°-bit, 90°-bit, and 180°-bit are three, six and twelve, respectively. The signal line of the CPW is set to be zero DC potential; and the actuation voltages applied on the DC bias pads. In order to separate the applied voltage of each bit section, two DC blocks have been added to the ground line of the CPW. The switches within each bit section have been connected together by high-resistance bias line to be operated with same voltage potential. Totally three DC bias pads (i.e. A, B, and C) are included. Table 3.21 lists all the switches' state for each proposed phase delay. The whole design area can be estimated from the layout design which is 12.8 mm \times 1.4 mm.

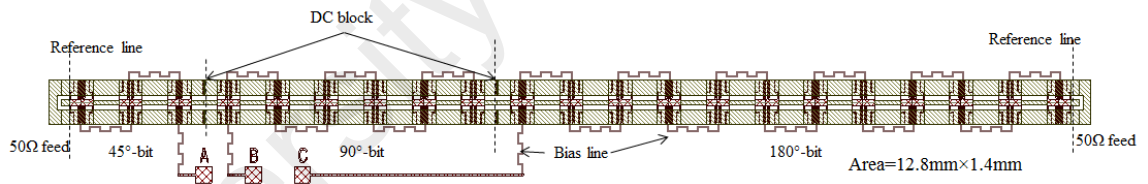


Figure 3.32: Layout of the 3-bit DMTL phase shifter

Table 3.21: Phase delays with RF-MEMS switches' operation

| Applied voltage potential | | | Phase shift |
|---------------------------|----|----|-------------|
| A | B | C | |
| 0 | 0 | 0 | 0° |
| 6V | 0 | 0 | 45° |
| 0 | 6V | 0 | 90° |
| 6V | 6V | 0 | 135° |
| 0 | 0 | 6V | 180° |
| 6V | 0 | 6V | 225° |
| 0 | 6V | 6V | 270° |
| 6V | 6V | 6V | 315° |

Note: assume $V_{DC}=6V (\geq V_{pull-in}=5V)$

3.6 Summary

In this chapter, the overall methodology of the project was introduced which is the core and the most important content of this project, as displayed in Figure 3.1. In the methodology flow, the design parts were presented, which includes the RF-MEMS capacitive switch's design specifications, structure and working principle descriptions, mechanical modeling, geometric optimization for low-actuation voltage and low-loss purposes, as well as the implementation of the RF-MEMS capacitive switches into MEMS switched-line phase shifter and DMTL phase shifter to verify their usages.

This research methodology is not only developed for the RF-MEMS capacitive switch design, but also can be used for other MEMS device design especially with multiple design objectives. Two novelties are included in this projects: i) the unique 3D structure design of the RF-MEMS capacitive switch with low-actuation voltage and low-loss purposes; and ii) the new multi-response optimization method which is developed basing on Taguchi method and weighted principal component analysis.

CHAPTER 4: RESULTS AND DISCUSSION

4.1 Introduction

The previous chapter introduced the research methodology of this project as well as the design and optimization of the low-actuation-voltage low-loss RF-MEMS capacitive switches for MEMS switched-line phase shifter and DMTL phase shifter. In this chapter, the simulations and analysis of the developed RF-MEMS switches and MEMS phase shifters are presented and discussed. Discussions focus on four aspects, namely static simulations, dynamic simulations, RF performance and equivalent circuits modeling.

4.2 FEM Simulations and Analysis of the RF-MEMS Capacitive Switch

FEM simulation is a means of predicting and optimizing the behavior of diverse complex objects, systems or structures which are often associated - without relying on physically existing models, prototypes or measurements. It involves numerically separating the system being investigated into very large number of small (finite) volumes, computing the physical states (e.g. stress, displacement, potential, temperature, frequency, etc.) of each individual volume and utilizing an iterative process to estimate the neighboring volumes until a physically practical solution is obtained for the whole system. The main advantages of utilizing FEM simulations is the capability to visualize the distribution of different properties and based on it obtaining a detailed understanding of the behavior and connections among different factors affecting a system. This can assist the researchers to identify the system's most important design factors, design results, and potential error sources, and then make the necessary improvements – without time-consuming and costly fabrication and measurements, especially for MEMS devices. For most FEM applications, the procedures to compute the FEM

simulation are more or less the same, which generally includes choosing the physical model, creating the geometry, adding the materials, setting the boundary conditions and loads, meshing the structure, running the simulation, checking and analyzing the results. In this section, the optimized low-actuation-voltage RF-MEMS capacitive switch (or the classic RF-MEMS capacitive switch) is simulated and analyzed which includes its mechanical properties, electrical properties, as well as the RF performance by the Multiphysics software of Comsol Multiphysics[®] and AWR[®] Design Environment.

4.2.1 Static Simulations

Static simulation computes a model's function or property at a particular time or a single state. For example, in this section, the RF-MEMS switch' spring constant, resonant frequency, stress distribution, pull-in voltage, switch-on and switch-off capacitance has been simulated and investigated.

4.2.1.1 Spring Constant, Resonant Frequency, Von Mises Stress

The RF-MEMS switch's optimization for low pull-in voltage has been done in chapter 3, where in order to finalize the beams dimensions; multi-response optimization has been proposed. Spring constant, resonant frequency and maximum von Mises stress are three responses that directly affect the switch's other properties, such as pull-in voltage, switching time and robust conditions.

In accordance with the dimensions listed in Table 3.3 Design 3, as well as the optimized models in Table 3.11, the three responses, namely spring constant, resonant frequency and von Mises stress, have been simulated by Comsol Multiphysics[®].

For the settings of the static simulations, the optimized membrane and beam structures (Model A, Model B and Model C listed in Table 3.11) were created in physics model of Solid Mechanics first. Aluminum was chosen as the metal material for the CPW, membrane and beams; and its material properties follow the default setting of the materials' library. All beams' ends, CPW and structure's substrate were fixed in the boundary conditions' setting. To simulate the spring constant and von Mises stress, a linear surface force load is applied on the membrane to model as the electrostatic force while the membrane's vertical displacement and maximum stress is observed. To simulate the resonant frequency of the suspended membrane and beam structure, there is no any load applied on the device.

Figure 4.1 shows the simulated total spring constant of each optimized model which is the reciprocal of the vertical displacement's slope, where Model A has the spring constant of 0.2303N/m; Model B's spring constant is 0.3011N/m; and the spring constant of the multi-response optimized Model C is 0.2378N/m. When the pull-in voltage is applied on the switch which is actuated, the membrane's vertical displacement is 2.9 μ m; the maximum von Mises stress of Model A, B and C is 13.586MPa, 14.172MPa, and 14.031MPa, respectively, as shown in Figure 4.2. All of these maximum von Mises stresses are less than the aluminum's yield stress (15MPa~20MPa) (Howatson, 2012); therefore the structure is stable and robust. The simulated 1st resonant frequency of Model A, B and C is located at 7.138 kHz, 7.853 kHz and 7.24 kHz, respectively. The values of spring constant and resonant frequency for the Model C are the trade-off results; this multi-response-optimized model's other mechanical and electrical properties were further investigated in the following parts.

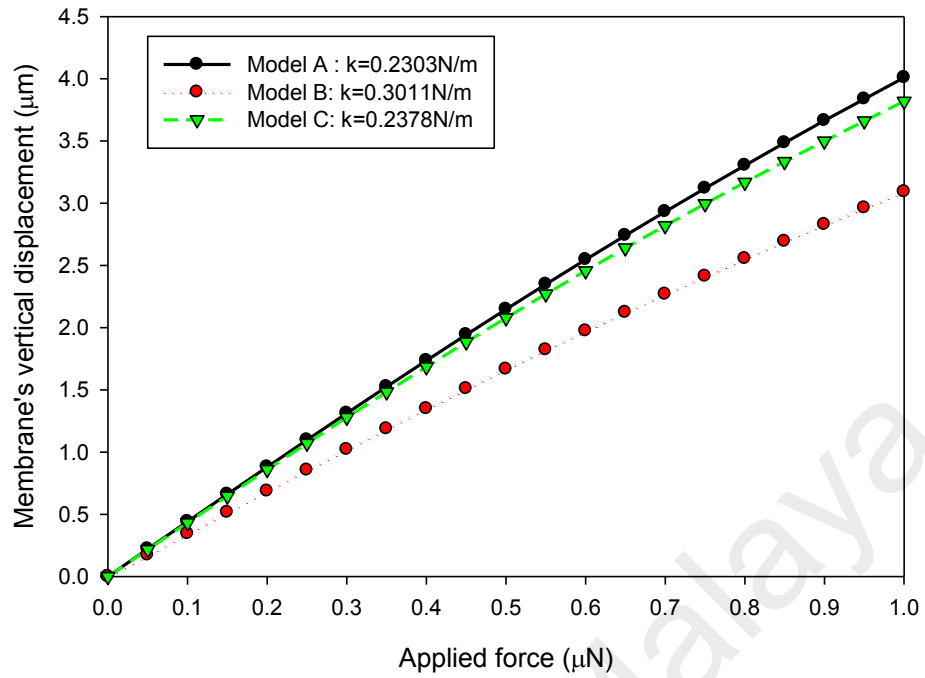
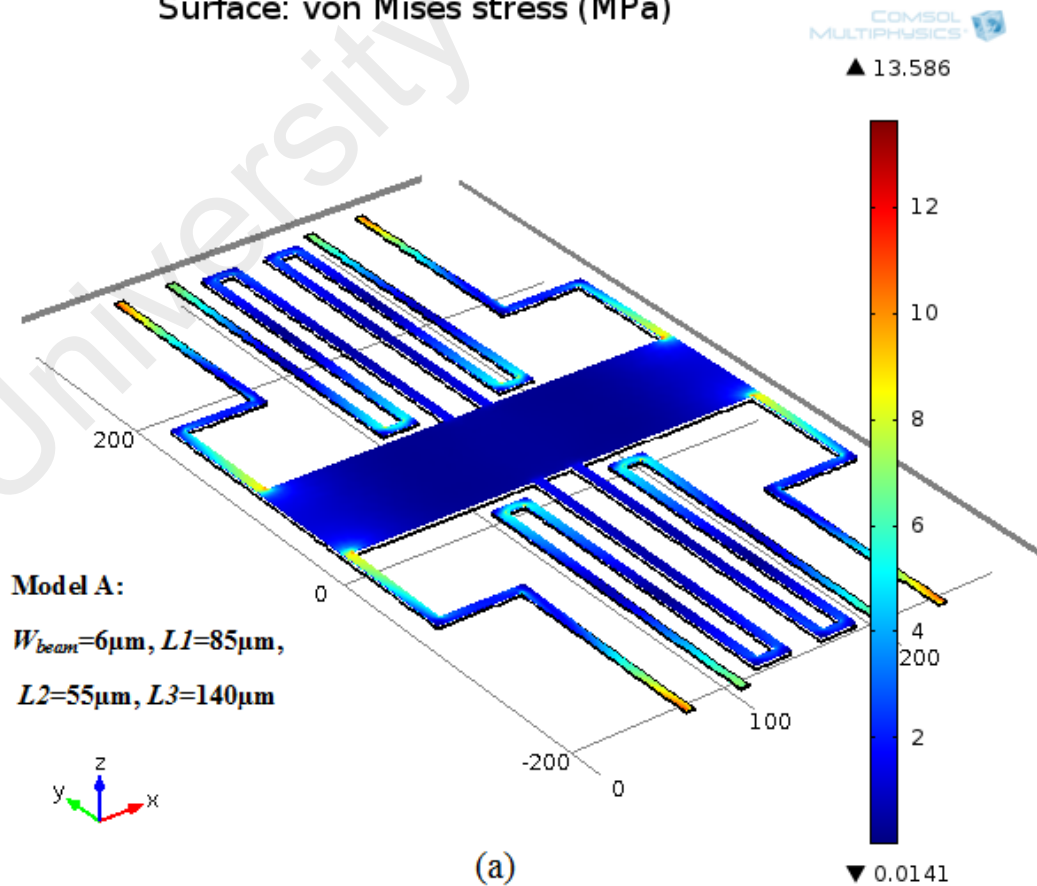


Figure 4.1: Spring constant of each optimized model

Surface: von Mises stress (MPa)



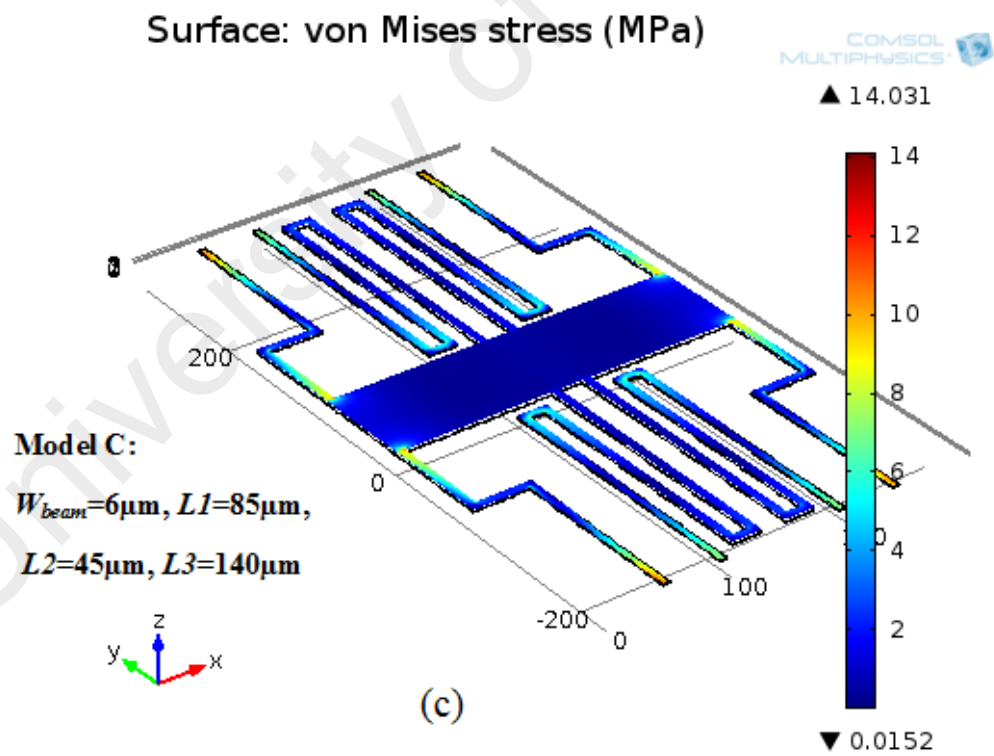
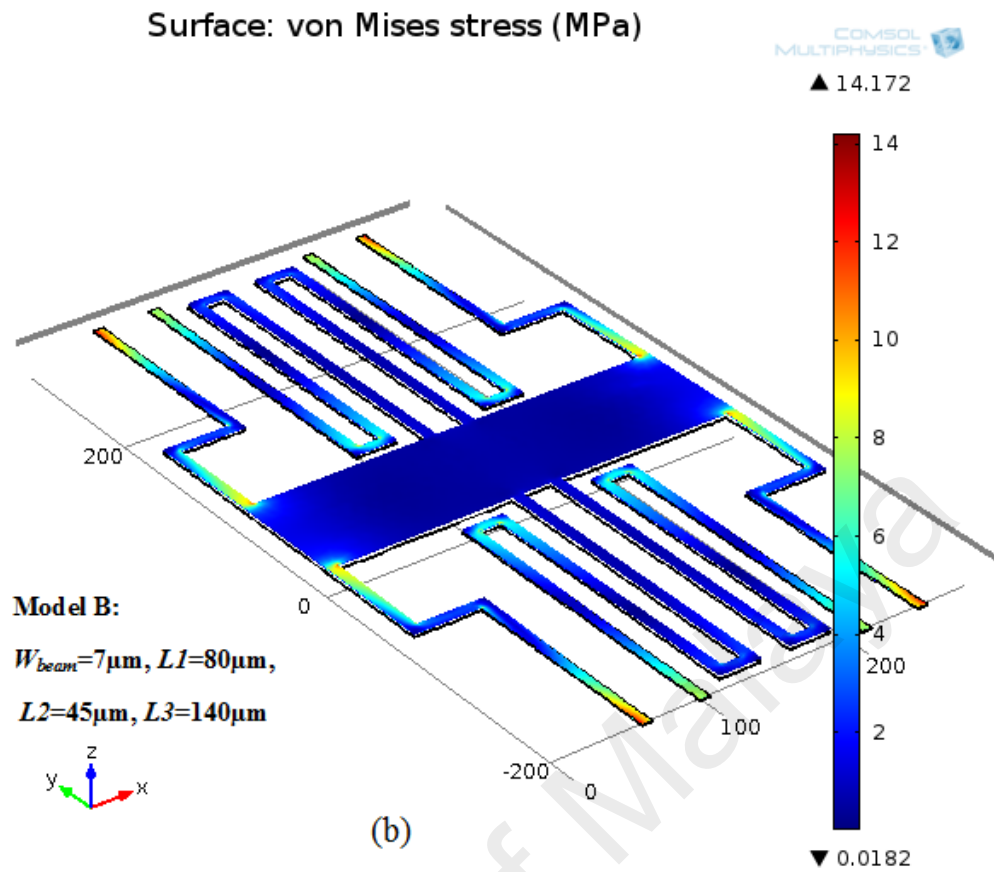


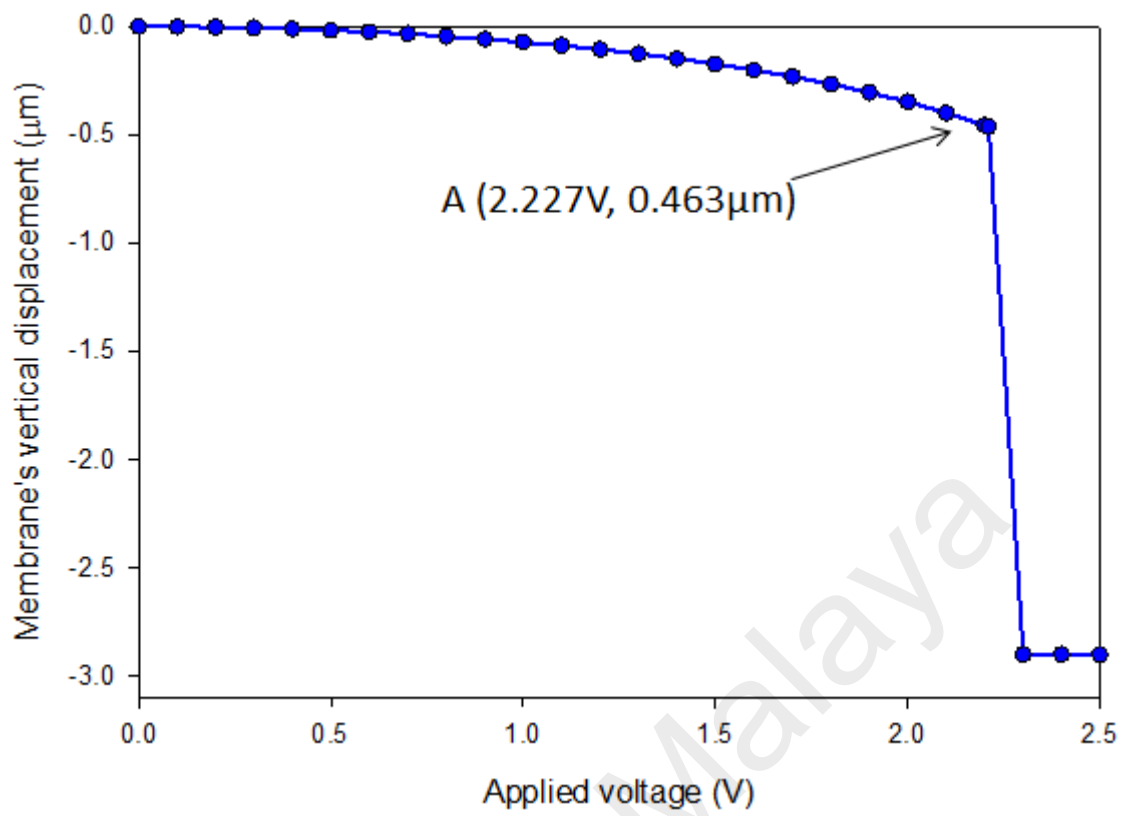
Figure 4.2: Von Mises stress distribution of each optimized model at actuated state

4.2.1.2 Pull-In Voltage and Residual Stress

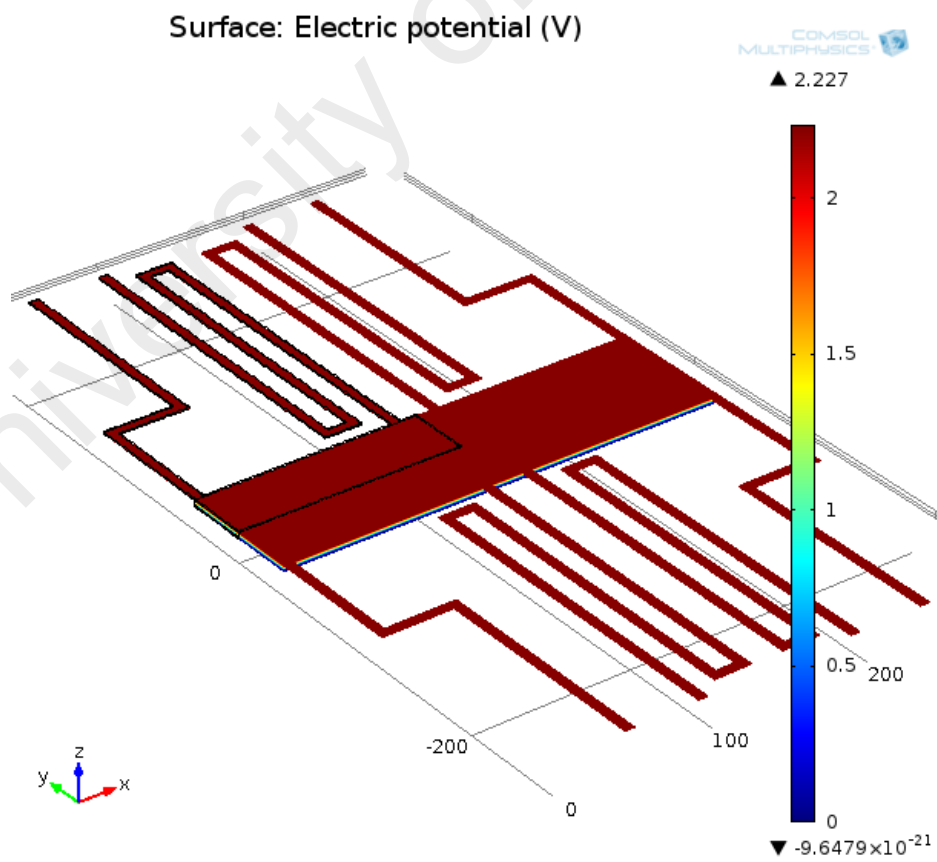
As section 3.3.2 mentioned, pull-in voltage ($V_{pull-in}$) is a critical voltage at which point, the electrostatic force exceeds the mechanical stress limit of the beams which causes the membrane collapsing on the bottom electrode; in other words, the switch is actuated. $V_{pull-in}$ is one of the most important design specifications (or design objectives) which can be observed by FEM simulations. In Comsol Multiphysics[®], the physics model of Electromechanics was employed; and a 3-D structure as shown in Figure 3.2 (a) was created in according to the dimensions mentioned in Table 3.3 Design 3 and the optimized Model C in Table 3.11. Each material's mechanical property which is employed in the structure is summarized in Table 4.1. The boundary conditions for the simulation of $V_{pull-in}$ were set as following: i) the CPW, silicon substrate and dielectric layer was set as fixed domain; ii) all of the beams' ends were set as fixed face; iii) the signal line's potential was set to be zero volt to simplify the simulation; and iv) the membrane domain was assigned with a linearly rising voltage load, in order to find the $V_{pull-in}$. The model was then meshed by free tetrahedral with minimum element size of $5\mu\text{m}$ (Here the minimum mesh size is usually determined by the computer's memory as well as the simulation results). And then the simulated $V_{pull-in}$ in stationary study mode is displayed in Figure 4.3; where it shows that the simulated $V_{pull-in}$ is 2.227V which is less than the calculated value ($V_{pull-in}=3.06\text{V}$ @ $k=0.2378\text{N/m}$) since its finite mesh element size is used.

Table 4.1: Materials' mechanic properties

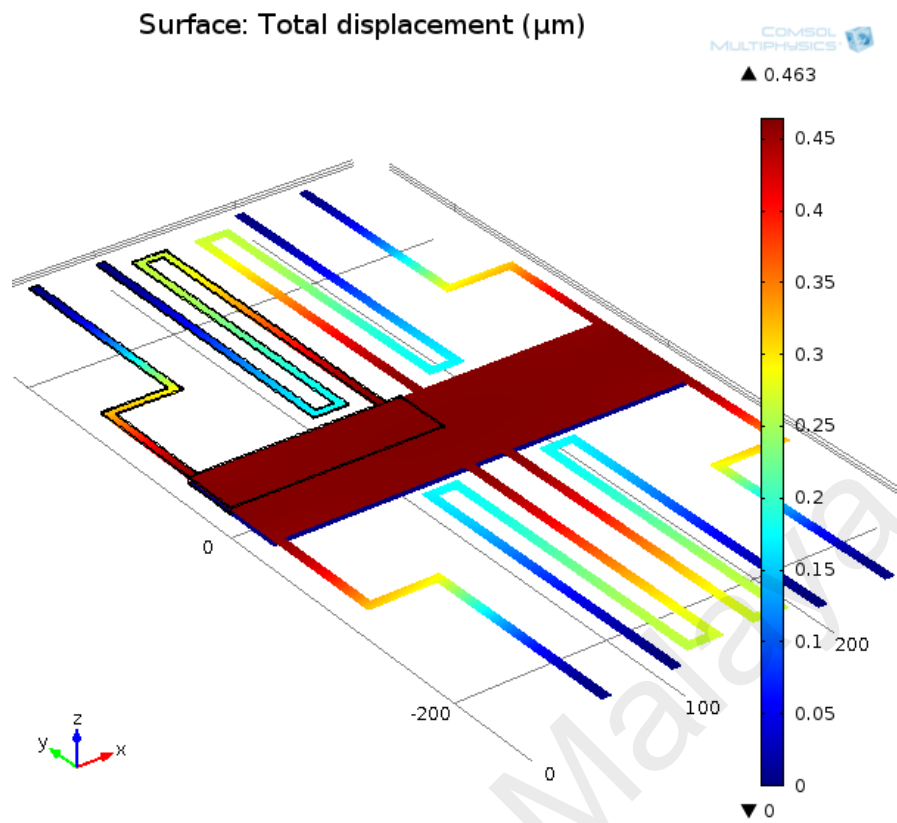
| Material | Density | Young's modulus | Poisson ratio | Dielectric constant |
|------------------------------------|--------------------|-----------------|---------------|---------------------|
| Silicon (Si) | 2.3g/cm^3 | 170GPa | 0.26 | 11.9 |
| Silicon Dioxide (SiO_2) | 2.2g/cm^3 | 70GPa | 0.17 | 3.9 |
| Aluminum (Al) | 2.7g/cm^3 | 70GPa | 0.35 | - |



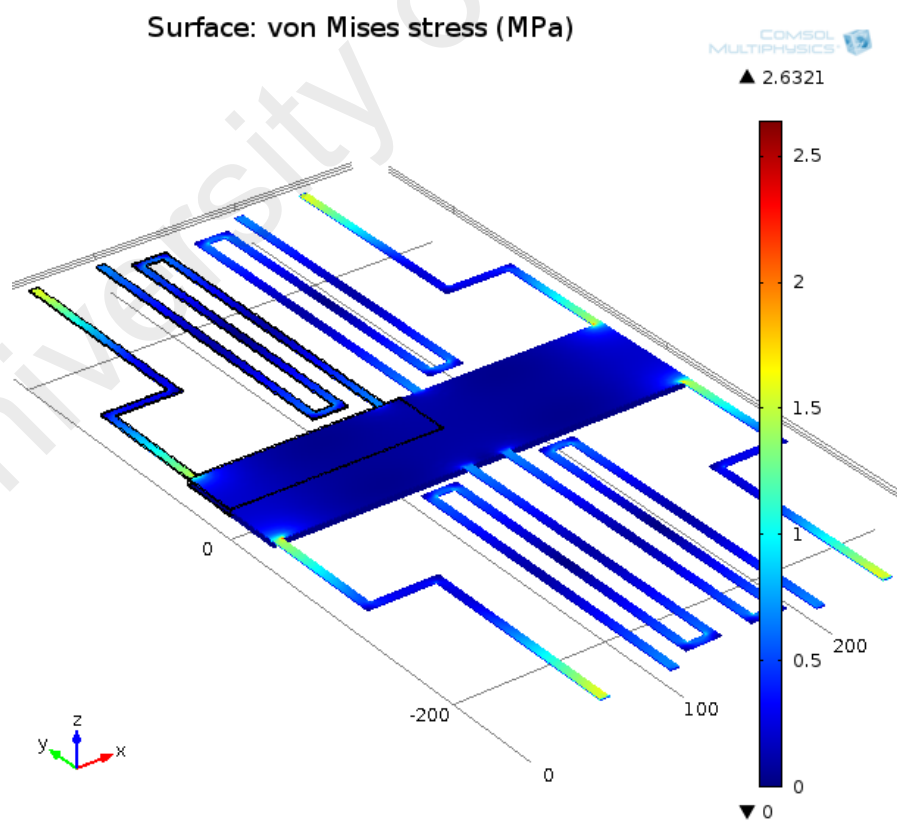
(a) Relationship of membrane's displacement and V_{in}



(b) Applied voltage is 2.227V (namely $V_{in}=2.227V$)



(c) 3-D view of displacement at $V_{in}=2.227V$



(d) 3-D view of von Mises stress at $V_{in}=2.227V$

Figure 4.3: Membrane's displacement with swept bias voltage (V_{in})

There were wide variations of measured $V_{pull-in}$ compared to theoretically estimated values. One of the important reasons for this variation in $V_{pull-in}$ is due to the presence of residual stress of the beam materials (Dutta, Imran, Pal, Jain, & Chatterjee, 2011). Basically, there are two types of residual stress which are both caused by the manufacturing processes: i) extrinsic stress and ii) intrinsic stress (Chen, Baughn, Yao, & Goldsmith, 2002). Extrinsic stress is produced by the mismatch in thermal expansion coefficients of the deposited thin film and substrate; while intrinsic stress is generated due to strain misfit encountered during phase transformation in the formation of a solid layer of a thin film. Generally there is no direct computation method to estimate the contribution of the intrinsic stress to the total residual stress (Chen, Baughn, Yao, & Goldsmith, 2002). However from previous literature, the residual stress gradients of the thin aluminum layer which is deposited by cost effectiveness and low processing temperature method namely electroplating were found to be varied mostly between 20MPa/ μm to -20MPa/ μm (Dutta, Imran, Pal, Jain, & Chatterjee, 2011). In this work, we have investigated the effect of a wider residual stress gradient's range on the $V_{pull-in}$ and maximum von Mises stress using simulation approach, which is from 50MPa/ μm to -50MPa/ μm , as shown in Figure 4.4. From this result, it can be concluded that: i) $V_{pull-in}$ is reduced with larger tensile stress (positive stress gradient) and increased with higher compressive stress (negative stress gradient); ii) if both tensile stress and compressive stress increased at the initial state, the maximum von Mises stress grows fast which is not the desired condition for the RF-MEMS switch; iii) the residual stress gradient within -16MPa/ μm to 16MPa/ μm is acceptable (green color part) since the maximum von Mises stress of the beam is in its elastic deformation condition; this residual stress gradient can be reduced by optimizing the fabrication process and creating holes in the membrane (Rebeiz, 2003). Figure 4.5 shows the von Mises stress distribution of the structure under high residual stress gradient (e.g., 45MPa/ μm); where it can be seen that

the maximum von Mises stress occurs at the anchor part of the beam. This stress can be reduced by making the anchor wider and thicker.

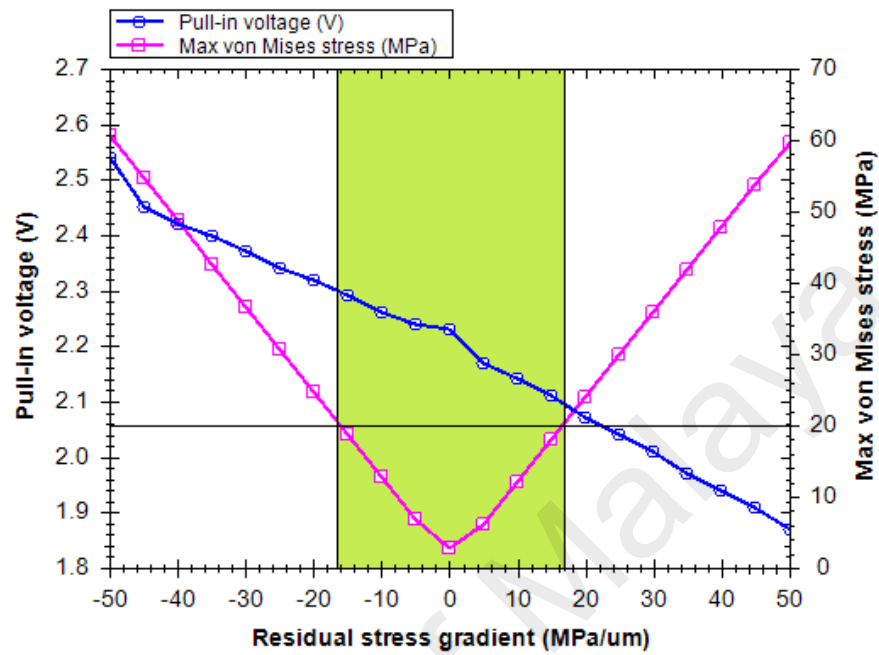


Figure 4.4: Effect of residual stress on $V_{pull-in}$

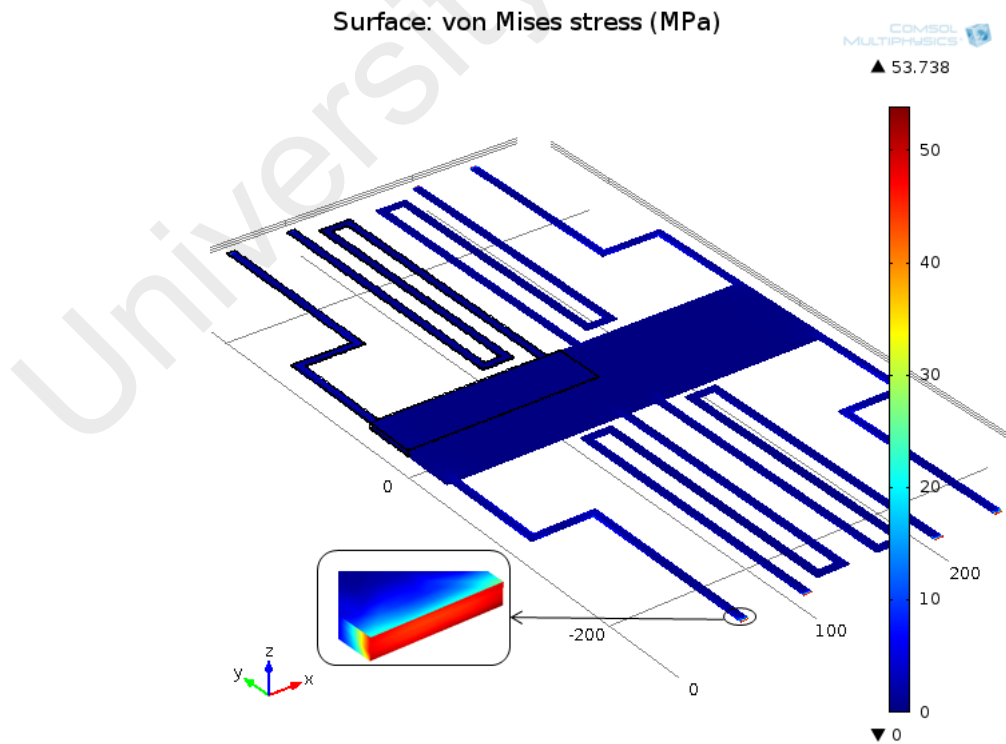


Figure 4.5: Maximum von Mises stress of the beams under residual stress gradient of $45\text{MPa}/\mu\text{m}$

Temperature's changes of the environment surrounding the beams also affect the $V_{pull-in}$; due to thermal effect on the beams' structure. As shown in Figure 4.6, if the switch undergoes a temperature change from a reference temperature of 20°C to a final temperature of 50°C without applying any bias voltage, the beams and membrane will be stretched and deformed causing the switch's $V_{pull-in}$ to change. Figure 4.7 simulates the thermal effect on the $V_{pull-in}$ within a wide temperature changing range of -20°C to 50°C, where the reference temperature is room temperature, 20°C; and T0 is the structure's final temperature. From this simulation result, it can be concluded that: i) the $V_{pull-in}$ decreases when the temperature increases; ii) under structure's thermal effect, the maximum von Mises stress of the structure is linearly increased by 3MPa/°C; iii) the maximum temperature change for the switch's robust operation should be kept less than 16°C.

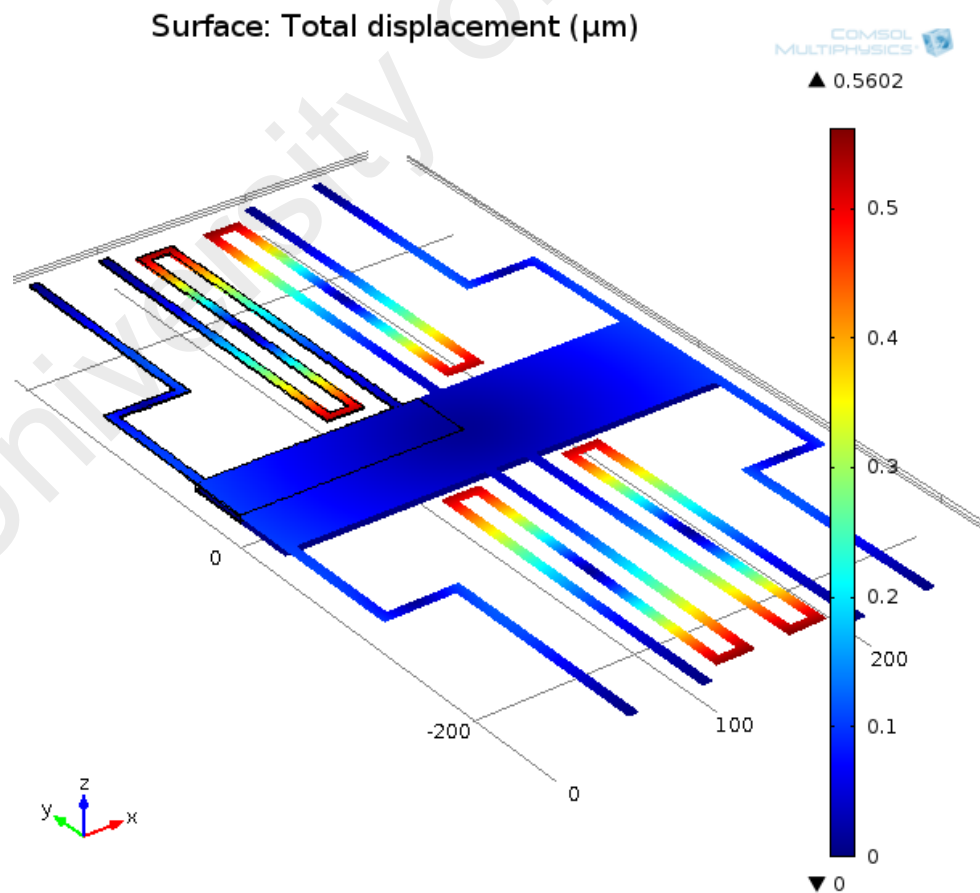


Figure 4.6: Beams and membrane's thermal effect with temperature of 20°C to 50°C and voltage load of 0V

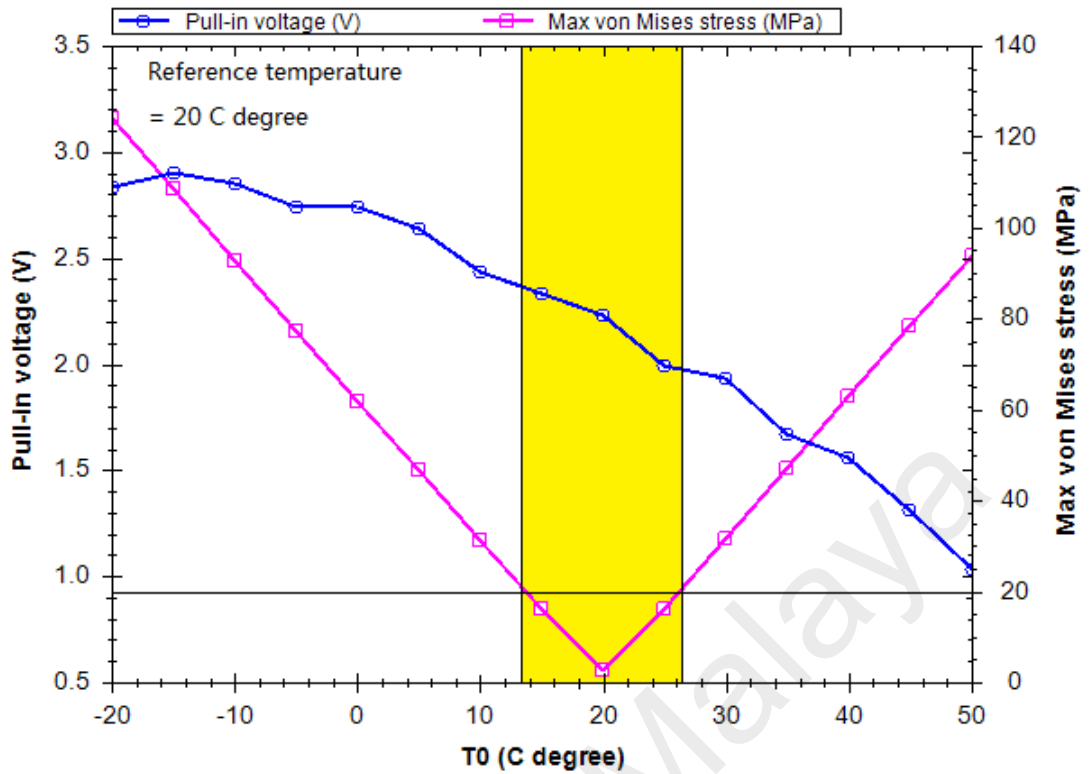


Figure 4.7: Structure's thermal effect on $V_{pull-in}$

4.2.1.3 Switch Capacitance

To verify the switch's capacitance at both switch-on and switch-off states by FEM simulation, the model of Electromechanics in Comsol Multiphysics® is employed and the boundary conditions are set as follows: i) both electrode plates are fixed; ii) the potentials of the bottom electrode are set to be 0V and the top electrode to 1V; and iii) for switch-on state, there is thin SiO₂ and air gap between two electrodes while for switch-off state, only a thin SiO₂ layer exists. Table 4.2 compares the simulated and calculated results of the RF-MEMS capacitive switch. It can be seen that all the simulated results match well with the design values in Table 3.3; the only difference is that simulated up-state capacitance (C_u) is a bit less than the calculated C_u since the fringing capacitance cannot be modeled in the simulation.

Table 4.2: Comparison of simulated and calculated switch capacitance

| Design 3 | Calculated C_u | Simulated C_u | Calculated C_d | Simulated C_d |
|----------|------------------|-----------------|------------------|-----------------|
| Values | 87fF | 69.244fF | 7.9pF | 7.9008pF |

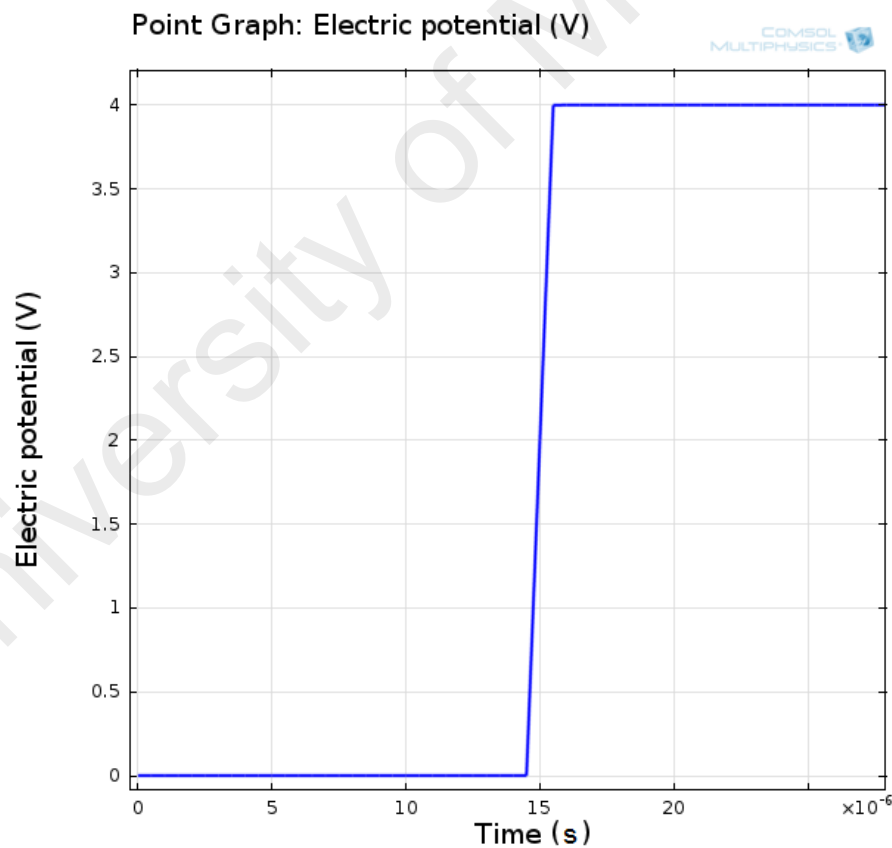
4.2.2 Dynamic Simulations

In dynamic domain, the optimized RF-MEMS switch's switching time, quality factor, dielectric charging effect on the pull voltages (namely pull-in voltage and pull-out voltage), parasitic charge density, as well as a two-step bipolar rectangular waveform for long lifetime has been discussed and verified by Comsol Multiphysics[®], where Electromechanics model was employed as the physics environment. The simulated structure was established in according to the dimensions mentioned in Table 3.3 Design 3, as well as the optimized beams with $W_{beam}=W_{beam2}=6\mu m$, $L1=(L1)_2=85\mu m$, $L2=(L2)_1=45\mu m$, $L3=(L3)_1=140\mu m$. The materials' properties of each layer were listed in Table 4.1, which are the default settings from the software's material library.

4.2.2.1 Switching Time and Quality Factor

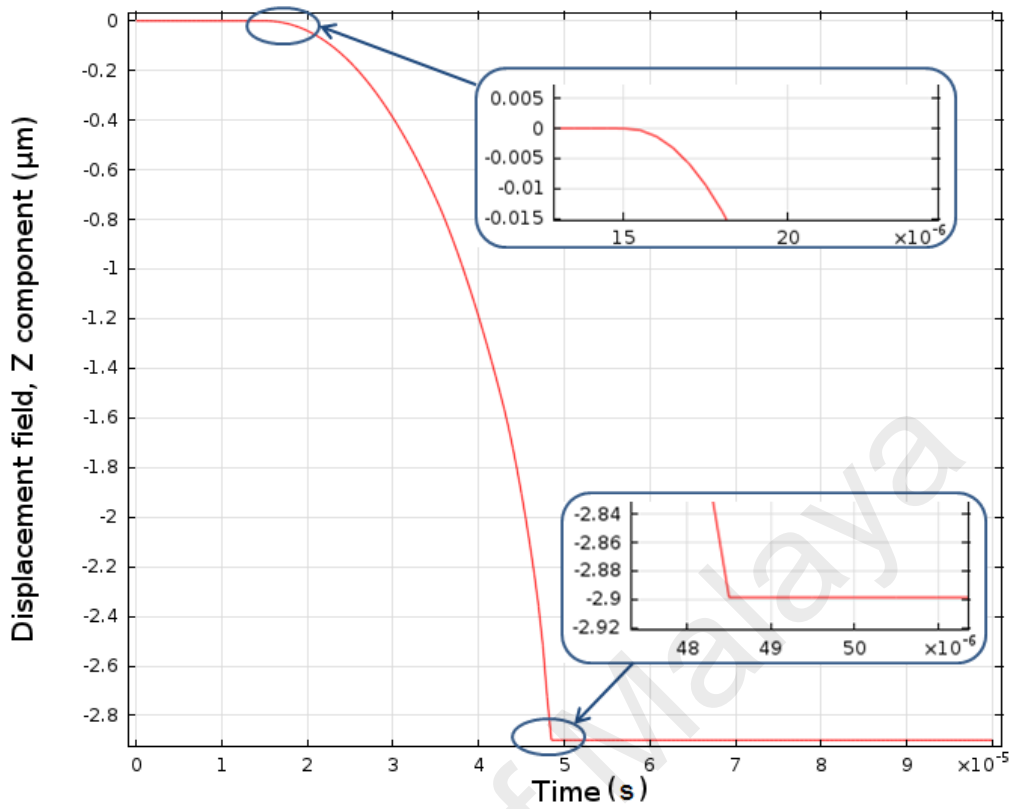
In electro-mechanical domain, the switching time of the RF-MEMS switch is also an important parameter to estimate the switch's working property. Switching time is defined as the time used to move the membrane from one state to the other one under a DC bias voltage control. Therefore, basically there are two different switching times: i) actuation time which is the time to pull the membrane from up state to down state, namely switching-off time (t_{OFF}); and ii) release time which is the time cost for the membrane rebounding from the down state to the up state with the bias voltage removed, namely switching-on time (t_{ON}).

The actuation time of the optimized RF-MEMS switch has been computed by a time dependent simulation from Comsol Multiphysics 4.3[®]. The boundary conditions were set as similar as the static simulation, with an additional step-up voltage load applied on the membrane, as shown in Figure 4.8 (a). The high level voltage of the step function (namely, 4V) is a bit larger than the $V_{pull-in}$; and its rise time is adjusted within 1 μ s which is much less than the actuation time, in order to minimize the effect of the applied voltage's rising time on the result. The simulated results of membrane's vertical movement are presented in Figure 4.8 (b). Figure 4.9 shows the actuation times of the optimized RF-MEMS switch with different amplitudes of the step-up voltage which is ranging from 4V to 7V.



(a) Applied voltage

Point Graph: Displacement field, Z component (μm)



(b) Membrane's displacement

Figure 4.8: Simulation of actuation time

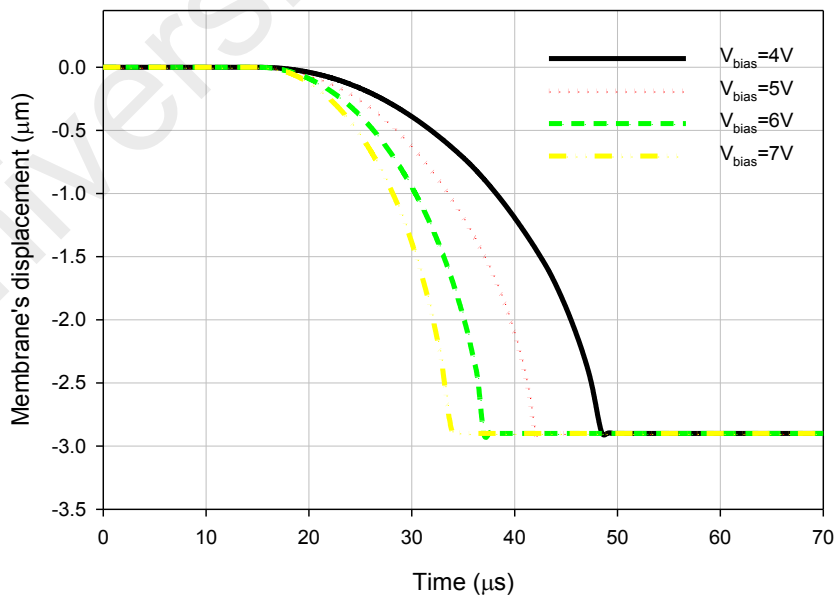


Figure 4.9: Simulated actuation time with different bias voltages

Table 4.3 summarizes the both calculated and simulated actuation times, where the calculated results were obtained by using (3.13). From these results, it can be seen that: i) the results of calculated and simulated actuation times agree with each other; here the calculated actuation time is larger than simulated value since in the calculation the total mass of the membrane and beams are used in (3.13); while in the simulation the effective mass was used. The effective mass is a bit less than the total mass since only the membrane and some part of the beam is moving; ii) the actuation time is inversely proportional to the bias voltage; with larger bias voltage, the less actuation time can be obtained; therefore, both low $V_{pull-in}$ and very short actuation time are not able to be achieved simultaneously; iii) the actuation time of the RF-MEMS capacitive switch is affected by its mechanical structure and generally the actuation time is inversely proportional to total resonant frequency of the membrane and beams which can be observed by (3.13).

Table 4.3: Comparison of calculated and simulated actuation time

| Bias voltage (V) | Actuation time ($t_{off}/\mu s$) | | Difference (%) |
|---------------------|------------------------------------|------------|-------------------|
| | Calculation | Simulation | |
| 4 | 39.7 | 34 | 14.4 |
| 5 | 31.8 | 27.5 | 13.5 |
| 6 | 26.5 | 22.5 | 15.1 |
| 7 | 22.7 | 19.5 | 14.1 |

The release time of the RF-MEMS capacitive switch is strongly dependent on the natural frequency and damping ratio of the membrane and beams which can be obtained by (3.4) and (3.5). Generally the release time can be estimated by employing a 1-D mass-spring-damper model, as shown in the governing equation of motion (3.3) (Muldavin, 2001). Specific to the optimized RF-MEMS capacitive switch, $m=7.683 \times 10^{-11} kg$; $k=0.2378 N/m$; $F(z,t)=0$ at $V_{in}=0V$; the initial condition of turning on the switch are $\dot{z}=0$ (namely, the velocity of the membrane is 0) and $z=-3\mu m$ (namely the initial position or displacement of the membrane is $-3\mu m$) at $t=0$.

According to the value range of the damping ratio, the behavior of the membrane's vibration until it returns to the zero displacement can be categorized into three conditions, which are under damping ($0 < \zeta < 1$), critical damping ($\zeta = 1$) and over damping ($\zeta > 1$) conditions. Then the equation of (3.3) has following three different possible solutions.

For underdamped condition, where $0 < \zeta < 1$, the membrane's behavior can be estimated by using (4.1 - 4.4).

$$Z(t) = e^{-\zeta\omega_0 t} [A \cos(\omega_d t) + B \sin(\omega_d t)] \quad (4.1)$$

$$\omega_d = \omega_0 \sqrt{1 - \zeta^2} \quad (4.2)$$

$$A = Z(0) \quad (4.3)$$

$$B = \frac{1}{\omega_d} \left[\zeta \omega_0 Z(0) + \dot{Z}(0) \right] \quad (4.4)$$

Where, $Z(t)$ is the membrane's vertical displacement at corresponding time; A and B are the coefficients and determined by the initial conditions of the system; ω_d is the damped angular frequency or ringing frequency of the system.

For critical damped condition, where $\zeta = 1$, the membrane's displacement can be obtained by using (4.5 - 4.7).

$$Z(t) = (A + Bt) e^{-\omega_0 t} \quad (4.5)$$

$$A = Z(0) \quad (4.6)$$

$$B = \dot{Z}(0) + \omega_0 Z(0) \quad (4.7)$$

For overdamped condition, where $\zeta > 1$, the membrane's displacement can be calculated by using (4.8 – 4.12).

$$Z(t) = Ae^{\gamma_+ t} + Be^{\gamma_- t} \quad (4.8)$$

$$\gamma_+ = -\zeta\omega_0 + \omega_0\sqrt{\zeta^2 - 1} \quad (4.9)$$

$$\gamma_- = -\zeta\omega_0 - \omega_0\sqrt{\zeta^2 - 1} \quad (4.10)$$

$$A = Z(0) + \frac{\gamma_+ Z(0) - \dot{Z}(0)}{\gamma_- - \gamma_+} \quad (4.11)$$

$$B = -\frac{\gamma_- Z(0) - \dot{Z}(0)}{\gamma_- - \gamma_+} \quad (4.12)$$

Where, γ_+ and γ_- are two roots of the (4.1)'s characteristic equation.

The RF-MEMS switch release times under different damping conditions have been plotted in Figure 4.10, where the damping ratio has been assumed as different values of 0.25, 0.5, 1, 1.5 and 2. From the plot, it can be seen that when the membrane is vibrated at the critical damping condition ($\zeta=1$), it can reach the stable position (namely zero displacement) by the shortest time (around 143 μ s) for the design.

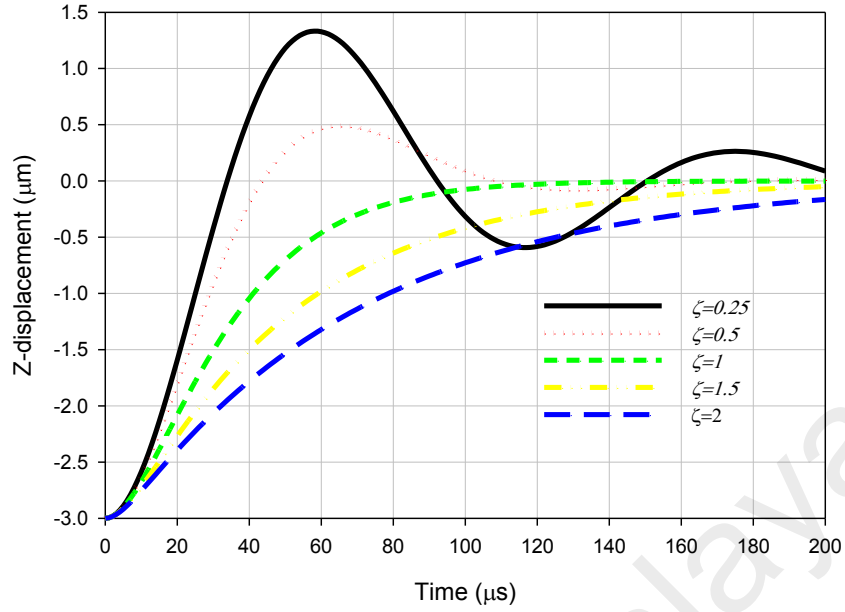


Figure 4.10: RF-MEMS switch release times with different damping ratios

From (3.5), it can be seen that the damping ratio is determined by the value of membrane and beam's mass, spring constant and damping coefficient. The mass and spring constant of the optimized membrane and beam is $7.683 \times 10^{-11} \text{kg}$ and 0.2378N/m , respectively. Therefore, in order to get $\zeta=1$, the only parameter can be optimized is damping coefficient, which can be calculated by (4.13) (Rebeiz, 2003n).

$$b = \frac{12}{N\pi} \frac{\mu A^2}{g_0^3} \left(\frac{p}{2} - \frac{p^2}{8} - \frac{\ln(p)}{4} - \frac{3}{8} \right) \quad (4.13)$$

Where, μ is the viscosity of the air, at standard pressure and temperature (25°C and 101kPa), which is $1.845 \times 10^{-5} \text{kg/ms}$ (or $\text{Pa}\cdot\text{s}$); A is the area of the membrane; N is the total number of the holes on the membrane; p is the fraction of the open area on the membrane; and g_0 is the air gap between two parallel plate.

Using (4.13), the desired value of damping coefficient can be obtained by controlling the number of holes and the fraction of the open area on the membrane. Figure 4.11 shows part of the membrane with square holes in it. When the edge of the square hole (h)

is set to be $7\mu\text{m}$ and the distance between each two holes (d) is $12\mu\text{m}$, the total number of the holes on the membrane can be calculated to be 42 and the damping coefficient is 8.81957×10^{-6} with the damping ratio of 1.03. Moreover, since $h \ll 4 \times g_0$, the effect of the holes on the up-state capacitance is negligible and the electrostatic force is not affected by the defined hole density (Rebeiz, 2003o).

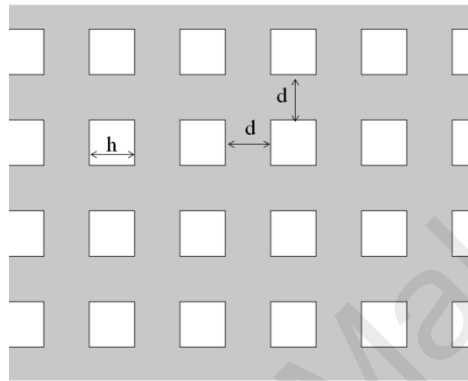


Figure 4.11: Partial membrane with square holes on it

The concept of quality factor is applicable in many different fields of physics and engineering and it can be referred as Q factor. The Q factor is a dimensionless parameter; and it demonstrates the energy loss within a resonant element which could be anything from a mechanical pendulum, an element in mechanical structure, or inside electronic circuit, for example, a resonant circuit. Here, the Q factor of the RF-MEMS switch is mainly discussed in its mechanical domain, which can be estimated by using (4.14) (Rebeiz, 2003n); this equation is a first-order approximation of the Q factor for a fixed-fixed beam. The calculated Q factor of the optimized RF-MEMS switch is 0.158 which is less than 0.5 and leads to a slow switching time (Rebeiz, 2003n), as shown in Figure 4.8 (b), which is around $34\mu\text{s}$ with the applied DC bias voltage of 4V. If increasing the membrane's thickness to $1.4\mu\text{m}$ and air gap to $3.5\mu\text{m}$, a larger Q factor of 0.574 could be attained; however, the increased membrane's thickness and air gap would make the pull-in voltage to rise about 2.2 times.

$$Q = \frac{\sqrt{E\rho}t^2}{\mu\left(\frac{WL}{2}\right)^2} g_0^3 \quad (4.14)$$

Where, $E=70GPa$ and $\rho=2700kg/m^3$ is the Al's Young's modulus and density, respectively; $L=280\mu m$, $W=80\mu m$, and $t=1\mu m$ is the membrane's length, width and thickness, respectively; $g_0=2.9\mu m$ is the air gap between the two electrodes; and $\mu=0.87 \times 1.845 \times 10^{-5} Pa \cdot s$ is the effective viscosity of air (Rebeiz, 2003n).

4.2.2.2 Pull Voltages under Dielectric Charging Effect

Dielectric charging effect on capacitive RF-MEMS switches plays an important role to cause the relevant failure mechanism, such as stiction failure. This phenomenon can be observed and analyzed by simulating the pull voltages (namely, pull-in and pull-out voltages) in time domain which is a new method based on FEM simulations.

When a RF-MEMS capacitive switch is actuated for the 1st time and the membrane collapses on the bottom layer, the applied electric field (E_{in}) across the dielectric layer can be obtained by (4.15), which is at least larger than $1.1934MV/cm$ for the optimized RF-MEMS capacitive switch. The applied high electric field easily tunnels the charges into the dielectric (Goldsmith et al., 2001) and traps them on the surface and bulk of the dielectric layer and then induces a parasitic electric field (E_{σ}) which changes the total applied electric field (E_{total}) as shown in (4.16) (Behlert, Kunzig, Schrag, & Wachutka, 2014), and further acts on the switch's $V_{pull-in}$ and $V_{pull-out}$ characteristics. For capacitive RF-MEMS switch, if the $V_{pull-out}$ is reduced to 0V, the membrane cannot be rebounded and the switch sticks on the dielectric. This effect is known as stiction effect.

$$E_{in} = \frac{\epsilon_r V_{in}}{t_d} \geq \frac{\epsilon_r V_{pull-in}}{t_d} = 1.1934 MV/cm \quad (V_{in} \geq V_{pull-in} = 3.06V) \quad (4.15)$$

$$E_{total} = E_{in} + E_{\sigma} = \frac{V_{in}}{t_{eff} - z} + \frac{\sigma t_d / \epsilon_0 \epsilon_r}{t_{eff} - z} \quad (t_{eff} = g_0 + t_d / \epsilon_r) \quad (4.16)$$

Where, ϵ_r is the SiO₂ layer's relative permittivity; V_{in} is the applied voltage; t_{eff} is the effective thickness; σ is parasitic charge density in the dielectric layer; and z is the membrane's vertical displacement.

According to R. Behlert's electromechanical model, under quasi-static motion, before the membrane totally collapses on the bottom layer, the electrostatic force induced by applied voltage equals to the spring's mechanical force. The relationship of V_{in} and z is shown in (4.17). $V_{pull-in}$ and $V_{pull-out}$ with the effect of dielectric charges can be estimated by replacing $z=(1/3)t_{eff}$ and $z=g_0$, respectively, as shown in (4.18) and (4.19).

$$V_{in}(z) = -\frac{\sigma t_d}{\epsilon_0 \epsilon_r} \pm (t_{eff} - z) \sqrt{\frac{2k}{\epsilon_0 A}} z \quad (4.17)$$

$$V_{pull-in_σ} = -\frac{\sigma t_d}{\epsilon_0 \epsilon_r} \pm t_{eff} \sqrt{\frac{8k}{27 \epsilon_0 A}} t_{eff} \quad (4.18)$$

$$V_{pull-out_σ} = -\frac{\sigma t_d}{\epsilon_0 \epsilon_r} \pm (t_{eff} - g_0) \sqrt{\frac{2k}{\epsilon_0 A}} g_0 \quad (4.19)$$

Where, $V_{pull-in_σ}$ and $V_{pull-out_σ}$ are the pull-in and pull-out voltages under dielectric charging effect, respectively.

Figure 4.12 shows the simulated $V_{pull-in}$ and $V_{pull-out}$ in time domain. Here FEM simulation was conducted by Comsol Multiphysics 4.3[®]. In Electromechanics module, a

quarter of switch was built with two symmetric boundaries in order to simplify the simulation; the beam end was fixed; and other boundary conditions were set similar as last section. A modified bipolar triangular waveform with frequency of 0.5 kHz and amplitude of 4V is applied. From this graph it can be seen that, in the first cycle, when the membrane was first pushed at point A where $z=(1/3)g_0$, the $V_{pull-in}$ is 3.04V (at point A') which matches with both static simulation and calculation results. Once the applied voltage is reduced to 0.7V ($V_{pull-out-\sigma}$) at point B', the membrane is released from the down state (point B) to the up state. After two cycles, the $V_{pull-in}$ was reduced to 3.0V as $V_{pull-in-\sigma}$ (at point C'); and after three cycles, the $V_{pull-out-\sigma}$ in was reduced to -0.69V at point D'. The graph illustrates that $V_{pull-out-\sigma}$ is smaller than $V_{pull-in-\sigma}$; the trend of $V_{pull-in}$ and $V_{pull-out}$ becomes smaller caused by the dielectric charging effect which can be used to estimate the lifetime of the switch under dielectric charging effect.

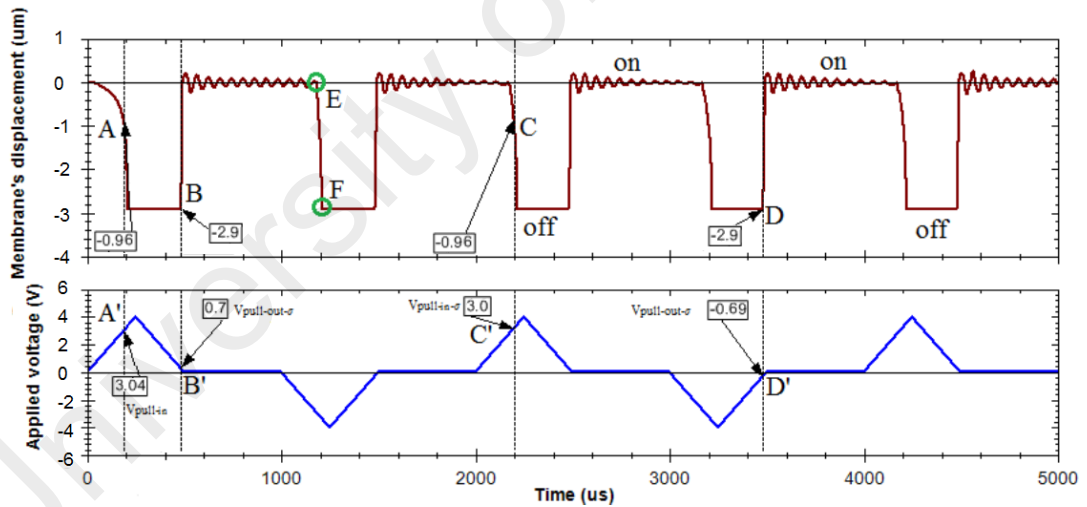


Figure 4.12: Applied voltage and membrane's displacement in time domain

4.2.2.3 Parasitic Charge Density

From (4.17) it can be seen that, the parasitic charge density in the SiO_2 layer should be estimated after the switch was actuated for the 1st time. In Figure 4.12, extracting the simulated data of $V_{in}(z)$ and z from point E to point F; replacing these values to (4.17),

the parasitic charge density is obtained as shown in Figure 4.13. Also the electric field generated from V_{in} and parasitic charges are displayed in the graph.

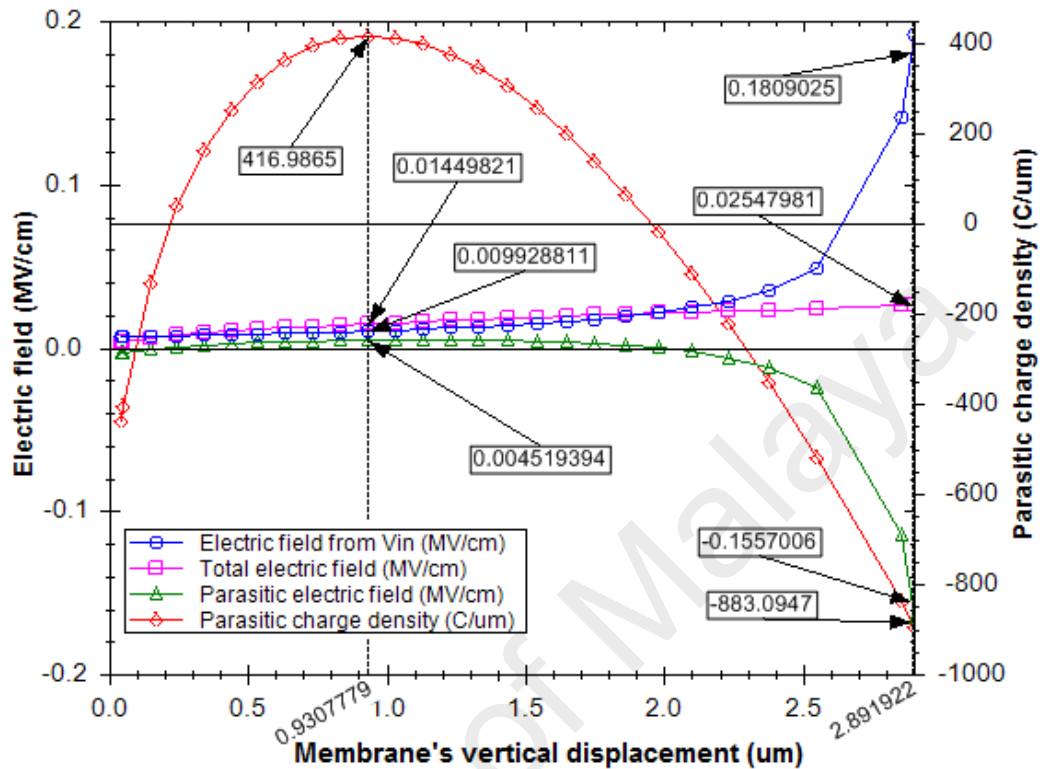


Figure 4.13: Parasitic charge density and electric field

From Figure 4.13 it can be seen that: i) when small voltage is applied, very small ($<0.04\text{MV/cm}$) electric field is induced, resulting in less than $2.5\mu\text{m}$ vertical displacement; both electric field from V_{in} and parasitic charges are in the range of few kV/m . ii) When the displacement is increased larger than $2\mu\text{m}$ ($\approx(2/3)g_0$), namely the switch is turned off with a large applied voltage, a larger parasitic electric field is produced. iii) The positive largest parasitic charge density appears at the displacement equaling to $0.9\mu\text{m}$ ($\approx(1/3)g_0$) which is around $417\text{C}/\mu\text{m}$; and the negative largest parasitic charge density occurs at when the membrane total collapse on the bottom electrode which is around $-883\text{C}/\mu\text{m}$. iv) A larger parasitic electric field is produced with high parasitic charge density which counteracts with a very big E_{Vin} . v) The total electric field at switch-off state is ten times larger than the one generated at switch-on state.

4.2.2.4 Two-Step Bipolar Rectangular Waveform for Long Lifetime

Referring to Figure 4.12 it can be seen when a triangular waveform is used for V_{in} to control the RF-MEMS switch, the duty cycle of the membrane's displacement is difficult to be controlled at 50% with specific amplitude and frequency. In addition, in order to get a long time turn-off state, a high amplitude waveform is needed which easily induces more parasitic charges with high electric field. In the real condition, the average applied voltage to turn off the switch is at least 4V to 6 V (Goldsmith et al., 2001), which will make the amplitude of the triangular bias voltage much higher. To overcome this problem, a two-step bipolar rectangular (TSBR) waveform is suggested as shown in Figure 4.14. The TSBR waveform not only supplies 50% duty cycle's displacement, but also has less dielectric charging effect and longer lifetime switch. The TSBR waveform basically is dependent on the actuation time, $V_{pull-in}$, $V_{pull-out}$, and switch speed. The switching speed is generally determined by the specific application, such as 1 kHz was used in (Goldsmith et al., 2001). ΔV means that the two voltage levels of TSBR waveform should be a bit higher than the switch's pull voltages. The novel TSBR waveform used has several advantages: i) a quick narrow pulse voltage, with amplitude higher than $V_{pull-in}$ and duration larger than actuation time, can fast turn on the switch. Afterwards, a less magnitude quiescent voltage which is a bit larger than $V_{pull-out}$ can hold the switch in on state. Both settings can minimize the dielectric charging effect when high voltage is applied across the switch dielectric (Goldsmith et al., 2001). ii) A setting of $t_{switchoff}=t_{switchon}$ can make sure that the duty cycle of membrane's displacement is 50%. iii) A bipolar waveform can dramatically release the accumulated charges in the dielectric layer and further increase the switch's lifetime. The frequency of switch on and off is twice of the TSBR waveform's frequency.

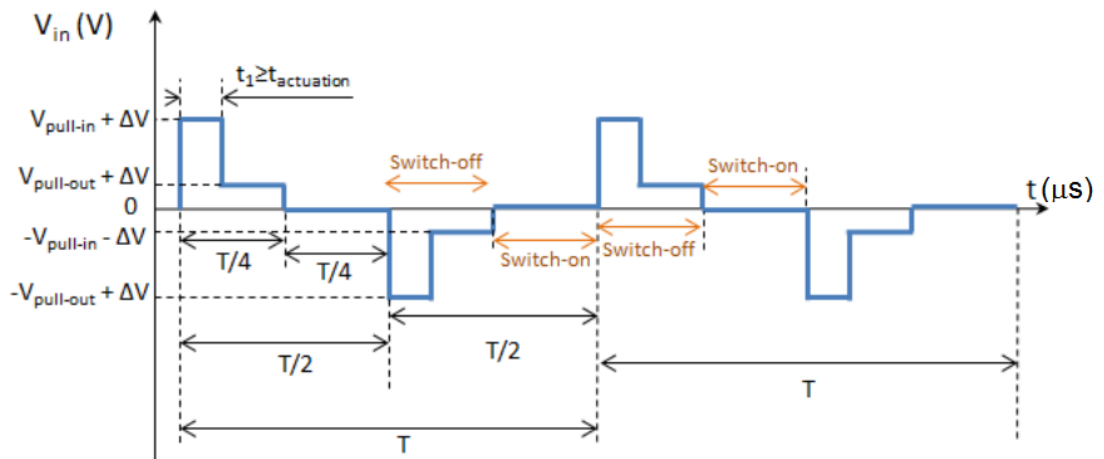


Figure 4.14: Two-step bipolar rectangular waveform

4.2.3 RF Performance

The RF performance of the RF-MEMS capacitive switch can be obtained by estimating its Scattering parameters (or S parameters) (Shea et al., 1971). S parameters are used to illustrate the electrical behavior of linear electrical networks when the networks experience various steady state stimuli by electrical signals. S parameters are commonly utilized for networks operating at RF and microwave frequencies where signal power and energy considerations are more easily quantified than currents and voltages. The S-parameter matrix for the 2-port network, as shown in Figure 4.15, is probably the most commonly employed and serves as the basic building block for generating the higher order matrices of larger networks (Choma & Chen, 2007). For two-port network, the relationship among the reflected, incident power waves and the S-parameter matrix is given by (4.20) (Choma & Chen, 2007).

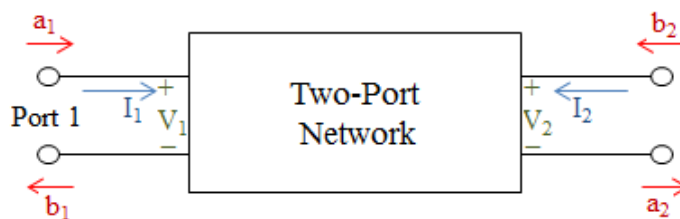


Figure 4.15: Two-port network

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \quad (4.20)$$

Where, a_1 b_1 and a_2 b_2 are two ports of RF-MEMS switch's equivalent circuit. In a RF switch, the insertion loss (4.21) and input return loss (4.22) is the most important parameters to be considered both at switch-on and switch-off states.

$$IL = -20 \log_{10} |S_{21}| dB \quad (4.21)$$

$$RL = -20 \log_{10} |S_{11}| dB \quad (4.22)$$

In this project, the RF-MEMS capacitive switch is connected in shunt with the signal line; depending on the values of applied DC voltage, the switch either leaves the signal line undisturbed or connects it to the ground line. For an ideal shunt switch, its input return loss should be close to infinite and insertion loss should be zero when no DC voltage is applied (namely, the membrane is at up-state position); otherwise its isolation should be close to infinite when the a DC bias voltage is applied (namely, the membrane is at down-state position).

The RF performance of the classic RF-MEMS capacitive switch was simulated by Electromagnetic (EM) simulator of AWR Design Environment 10[®] in this work. For EM simulations, the RF-MEMS switch is considered from a digital point of view; only the membrane's initial and final positions are investigated without considering its dynamical behavior (such as actuation speed and gas damping contributions); this is because the switch-on and switch-off states are the only situations necessary for assessing the whole device's RF performances (Bartolucci, Angelis, Lucibello, Marcelli, & proietti, 2012).

4.2.3.1 S Parameters and Operational Frequency Bandwidth

Figure 4.16 and Figure 4.17 present the simulated S-parameters of the classic RF-MEMS capacitive switch. When the switch is not actuated, namely at switch-on state, its return loss and insertion loss is -7.879dB and -0.5487dB at 20GHz, respectively. When the switch is actuated, namely at switch-off state, its return loss and isolation is -0.4557dB and -23.02dB at 20GHz, respectively. Both insertion loss and isolation of the classic RF-MEMS switch at 20GHz meet with the most RF devices' requirements; however the switch-on state (or up-state) return loss is out of the design specification range.

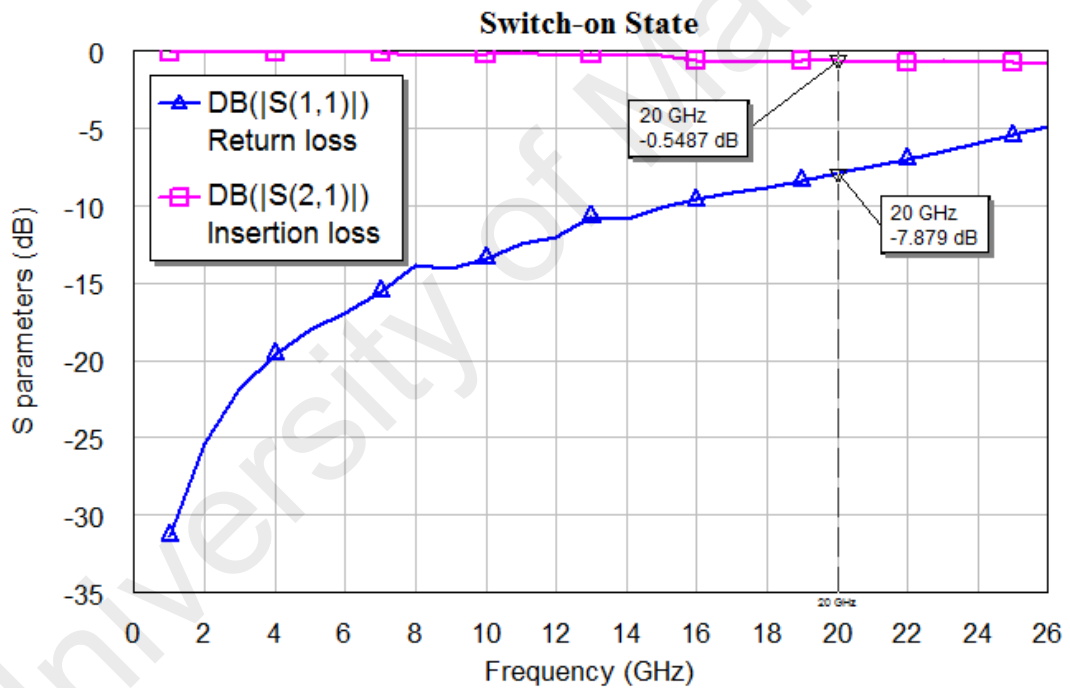


Figure 4.16: Return loss and insertion loss at switch-on (or up) state

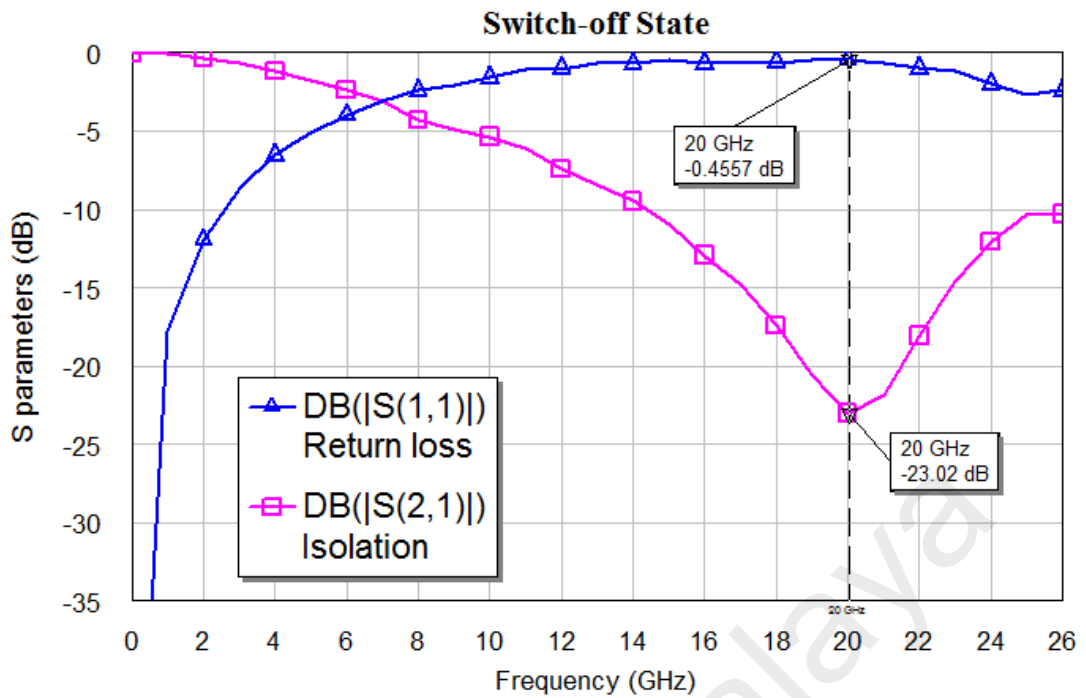


Figure 4.17: Return loss and isolation at switch-off (or down) state

The operation frequency bandwidth of the switch can be estimated from the switch's insertion loss and isolation. In other word, the switch should be operated in the frequency range where its isolation and insertion loss simultaneously fulfills the design specifications. In this design, the isolation is specified less than -15dB and the insertion loss is required to be higher than -1dB, as stated in chapter 3. Figure 4.18 plots the classic RF-MEMS capacitive switch's insertion loss and isolation together in one graph. It can be seen that in the frequency range of 1GHz to 26GHz, insertion loss is entirely located in the range of higher than -1dB; therefore, the switch's operation bandwidth is basically determined by the isolation of this switch. In Figure 4.18, f_L means lower frequency which is limited by the minimum frequency value to satisfy the requirement of isolation less than -15dB; f_U means upper frequency which is limited by the maximum frequency value to realize the requirement of isolation less than -15dB. Then the classic RF-MEMS switch's operation bandwidth can be calculated by the difference of the f_U and f_L . As the simulation results show that f_L is 17GHz and f_U equals to 22.8GHz; therefore, the bandwidth of the RF-MEMS switch is 5.8GHz.

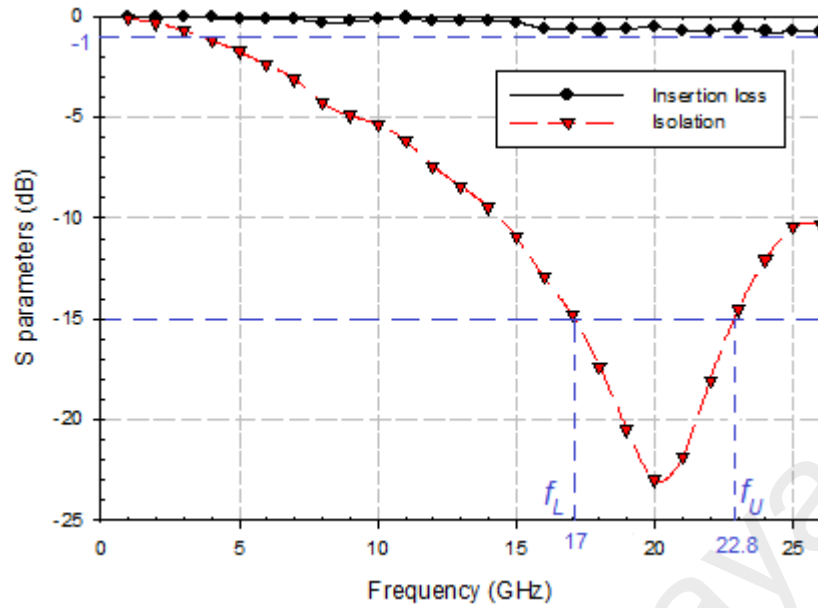


Figure 4.18: Frequency bandwidth of the RF-MEMS capacitive switch

4.2.3.2 Switching Impedance

The RF-MEMS switch's switch-on and switch-off impedance were simulated and presented in Figure 4.19. The results show that when the switch is not actuated (namely, at switch-on state), its impedance is close to 50Ω point (center point of the Smith chart), therefore it works as a transmission line. Since the switch capacitance at switch-on state is relatively small (around 85fF), its corresponding reactance ($-j\frac{1}{\omega_0 C_u}$) is large; and then the total impedance is located in lower part of the Smith chart. On the contrary, when the switch is actuated (namely, at switch-off state), the impedance point is near to the short connection point (leftmost point of the Smith chart) which bypasses the RF signal to the ground plane; the total impedance is inclined to inductive area since C_d is much larger than C_u and the capacitive reactance ($-j\frac{1}{\omega_0 C_d}$) is much smaller than the beams' inductive reactance.

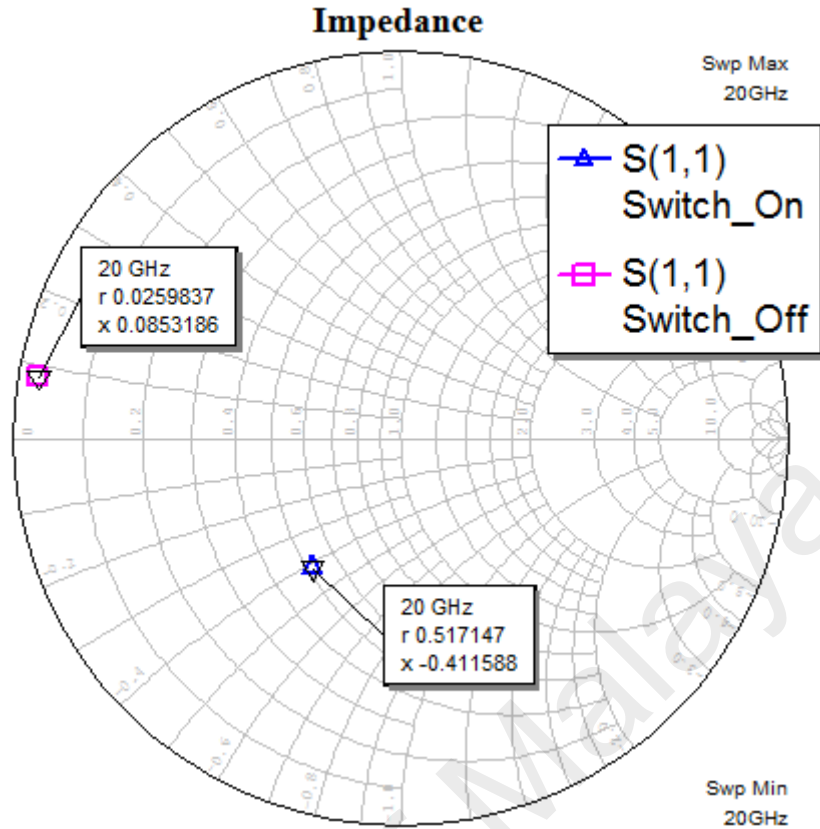


Figure 4.19: Impedance of the RF-MEMS capacitive switch at both switch-on and switch-off states

4.2.3.3 Power Handling

For power handling capability of the RF-MEMS capacitive switch, there are basically two parameters to be considered; one is the power needed to actuate the switch which is called pull-down power ($P_{pull-down}$); and the other one is the required power to hold the membrane in the down state which is named hold-down power ($P_{hold-down}$). The $P_{pull-down}$ can be estimated from $V_{pull-in}$ and impedance of the switch, as shown in (4.23); and the $P_{hold-down}$ can be obtained by (4.24) (Muldavain, 2001; Pacheco, 2004).

$$P_{pull-down} = \frac{V_{pull-in}^2}{Z_{up}} = \frac{8kg_0^3}{27\epsilon_0AZ_{up}} \quad (4.23)$$

$$P_{hold-down} = \frac{2kg_0(t_d/\epsilon_r)^2}{\epsilon_0 AZ_{down}} \left(1 + \frac{\omega^2 Z_{down}^2 \epsilon_0^2 A^2}{4(t_d/\epsilon_r)^2} \right) \quad (4.24)$$

Where, Z_{up} and Z_{down} is the impedance of the RF-MEMS switch at switch-up (or switch-on) and switch-down (or switch-off) state, respectively; $\omega=2\pi f$ is the operation frequency of the switch.

By using the RF-MEMS switch's optimized design parameters which was mentioned in Chapter 3, namely $k=0.2378N/m$, $g_0=3\mu m$, $\epsilon_0=8.854 \times 10^{-12}F/m$, $A=80\mu m \times 286\mu m$, $t_d=0.1\mu m$, $\epsilon_r=3.9$, as well as the impedance simulation results of $Z_{down}=Z_0 \times (0.0259837+j0.0853186)$ and $Z_{up}=Z_0 \times (0.517147-j0.411588)$ at the frequency of 20GHz, the $P_{pull-down}$ and $P_{hold-down}$ can be obtained as 284.17mW and 6.13mW, respectively.

In the whole operation frequency band, namely from 17GHz to 23GHz, the switch's impedance at both switch-on state and switch-off state is shown in Figure 4.20. From this result it can be seen that when the switch is working at 17GHz, its impedance at switch-on and switch-off state is closer to the ideal condition. The RF-MEMS capacitive switch's ideal switch-on state impedance is 50Ω and the switch works as a standard transmission line. The RF-MEMS capacitive switch's ideal switch-off state impedance is close to 0Ω and the switch works as a short circuit to pass the RF signal to the ground line.

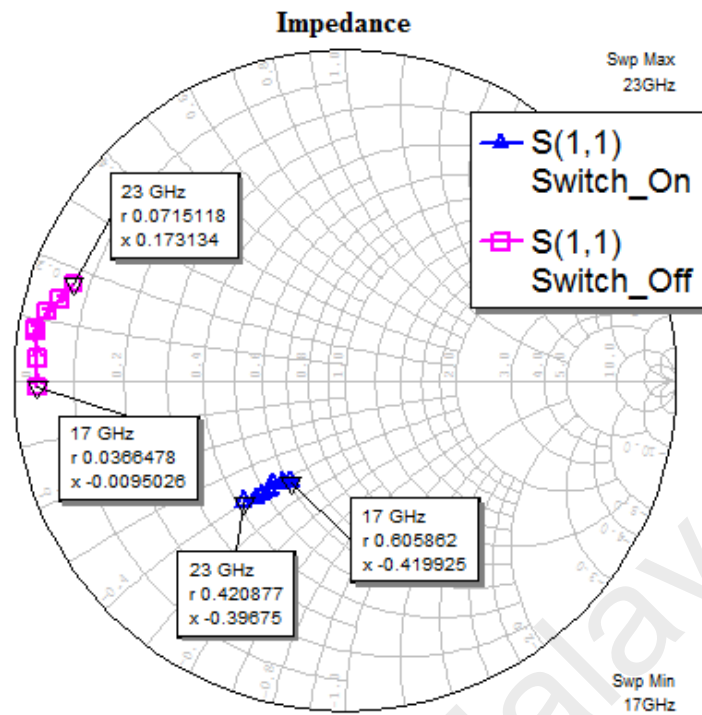


Figure 4.20: Relationship of impedance of the RF-MEMS capacitive switch with operation frequency

By employing (4.23) and (4.24), the relationships of the pull-down power and hold-down power with operation frequency and switch's impedance were plotted in Figure 4.21 and Figure 4.22, respectively.

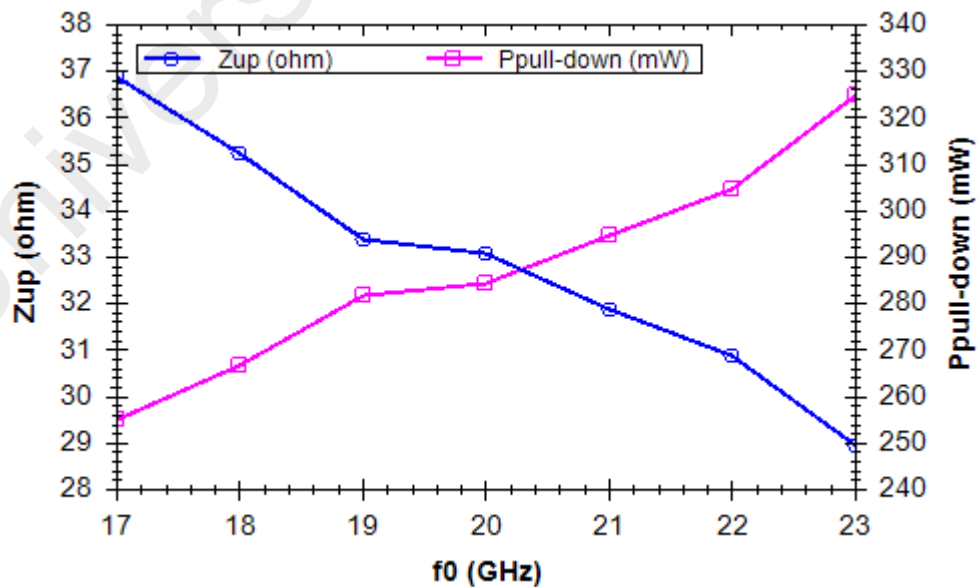


Figure 4.21: Relationship of RF-MEMS capacitive switch's operation frequency, up-state impedance and pull-down power

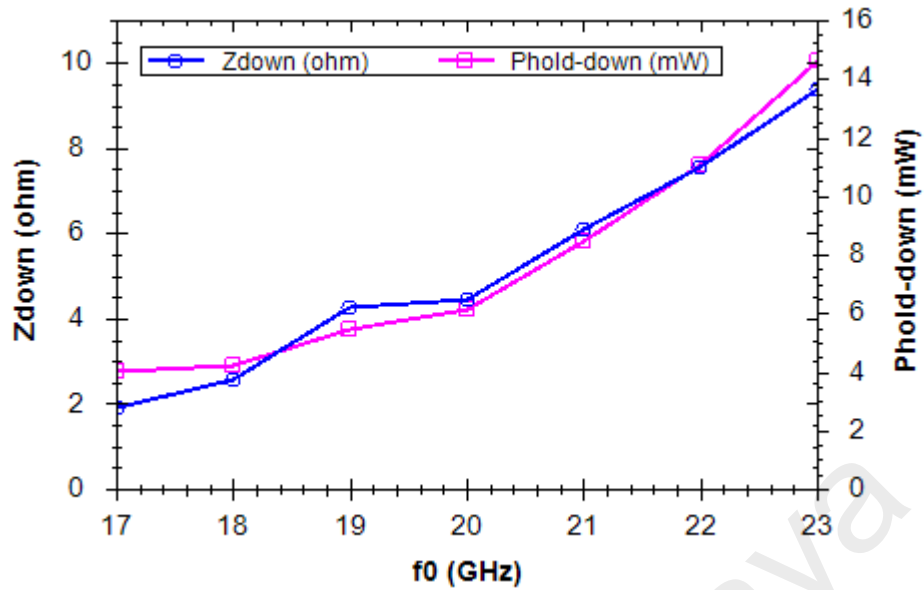


Figure 4.22: Relationship of RF-MEMS capacitive switch's operation frequency, down-state impedance and hold-down power

From Figure 4.21, it can be seen that when the operation frequency is increased from 17GHz to 23GHz, the RF-MEMS switch's up-state impedance decreases in the range of 37Ω to 29Ω while the pull-down power is increased from 255mW to 325mW. From Figure 4.22, it can be seen that when the operation frequency is creasing from 17GHz to 23GHz, the RF-MEMS switch's down-state impedance ranges from 1.9Ω to 9.4Ω and hold-down power is increased from 4mW to 14.6mW. Both pull-down power and hold-down power are less than 1W which match with design specification defined in section 3.2. Figure 4.23 compares a power handling of the proposed RF-MEMS capacitive switch with other works which shows the normal range of power handling for the RF-MEMS capacitive switches located in 20dBm (100mW) to 30dBm (1W).

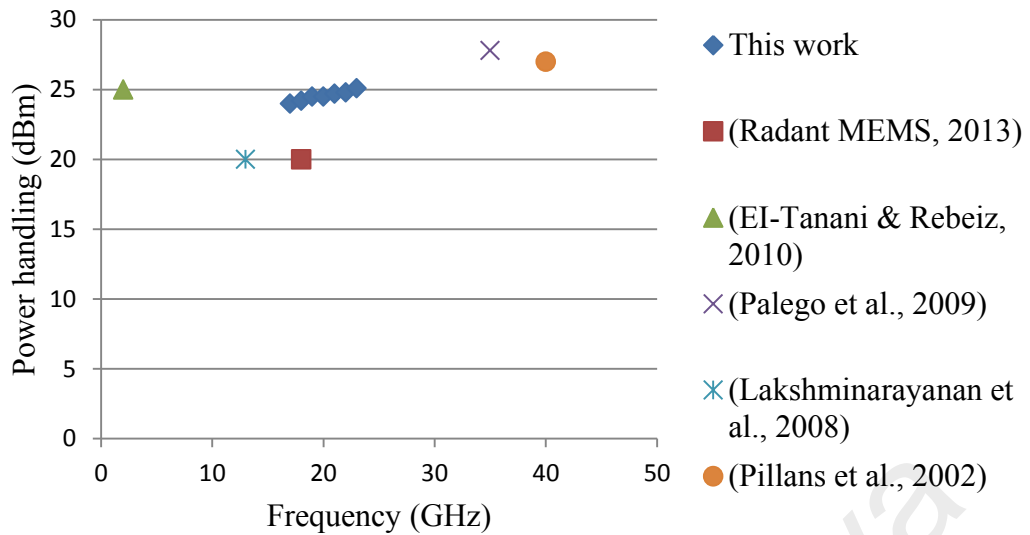


Figure 4.23: Power handling comparison

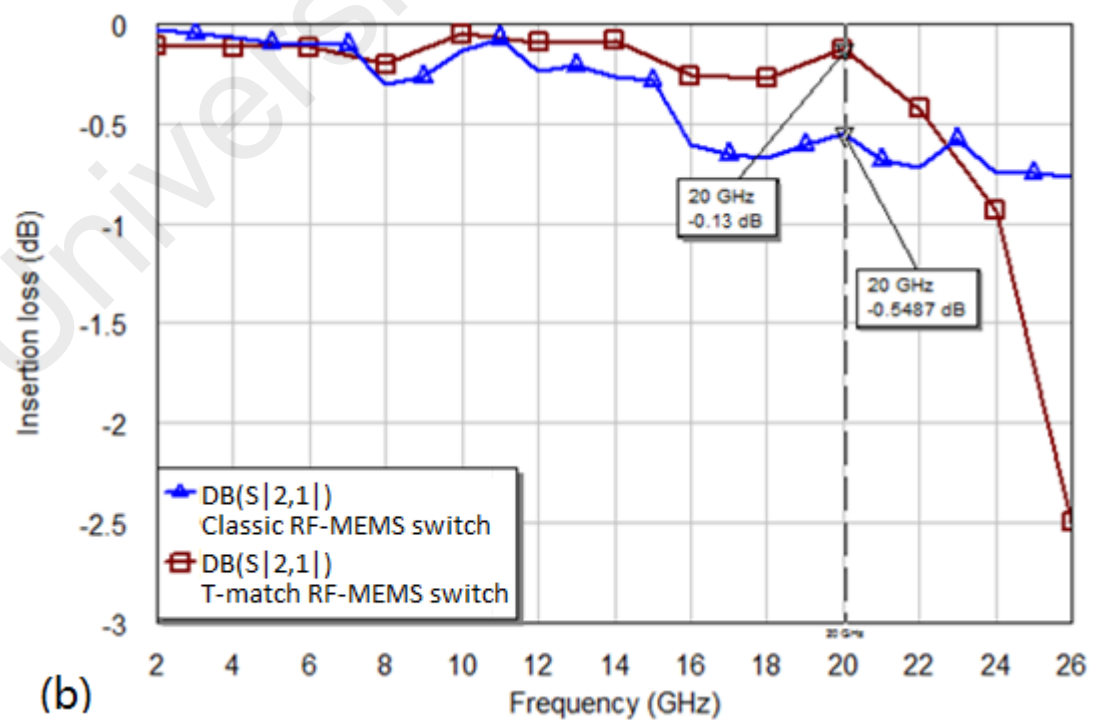
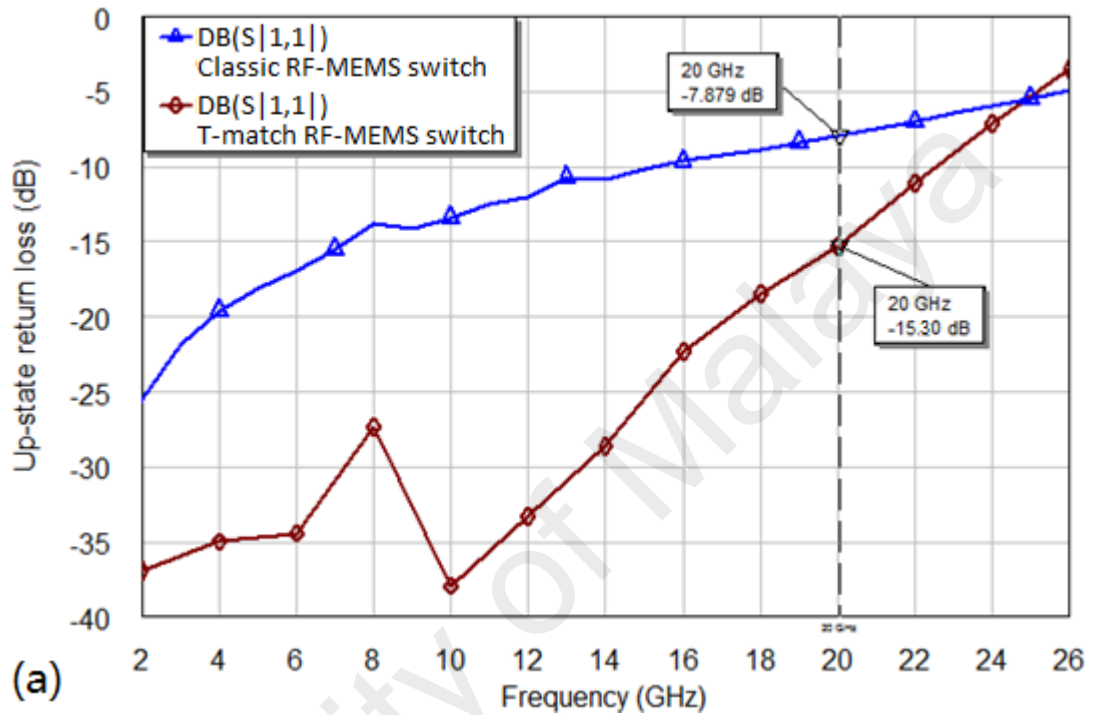
4.3 RF Performance of the Improved Low-Loss RF-MEMS Capacitive Switches

In this section, the RF performance of the improved low-loss RF-MEMS capacitive switches, namely the T-match and π -match RF-MEMS capacitive switches, have been computed by AWR Design Environment 10TM, which also were compared with the S parameters of the classic.

4.3.1 RF Performance of the T-Match RF-MEMS Switch

Figure 4.24 presents the simulated S parameters of the T-match RF-MEMS switch; meantime they are compared with the classic RF-MEMS capacitive switch's RF performance. The simulation results show that: i) the up-state return loss, insertion loss, isolation and down-state return loss of the T-match RF-MEMS switch is -15.30dB, -0.13dB, -0.60dB and -28.79dB, respectively, at frequency of 20GHz; ii) compared to the classic RF-MEMS switch, the up-state return loss, insertion loss and isolation of the T-match RF-MEMS switch are improved by 94.19%, 76.47% and 25.07%, respectively,

at 20GHz, while the down-state return loss is degraded by 31.01%; iii) S parameters of the T-match RF-MEMS switch at 20GHz all satisfy the predefined design specifications; iv) the overall RF performance of the T-match RF-MEMS switch is better than the classic RF-MEMS switch's.



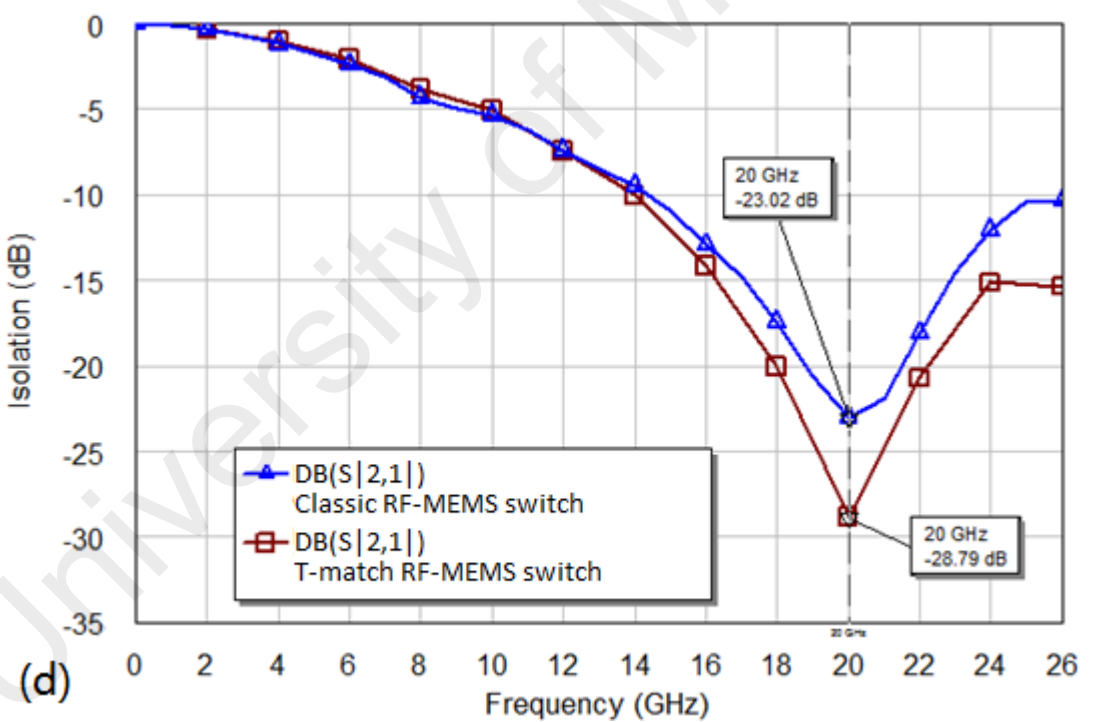
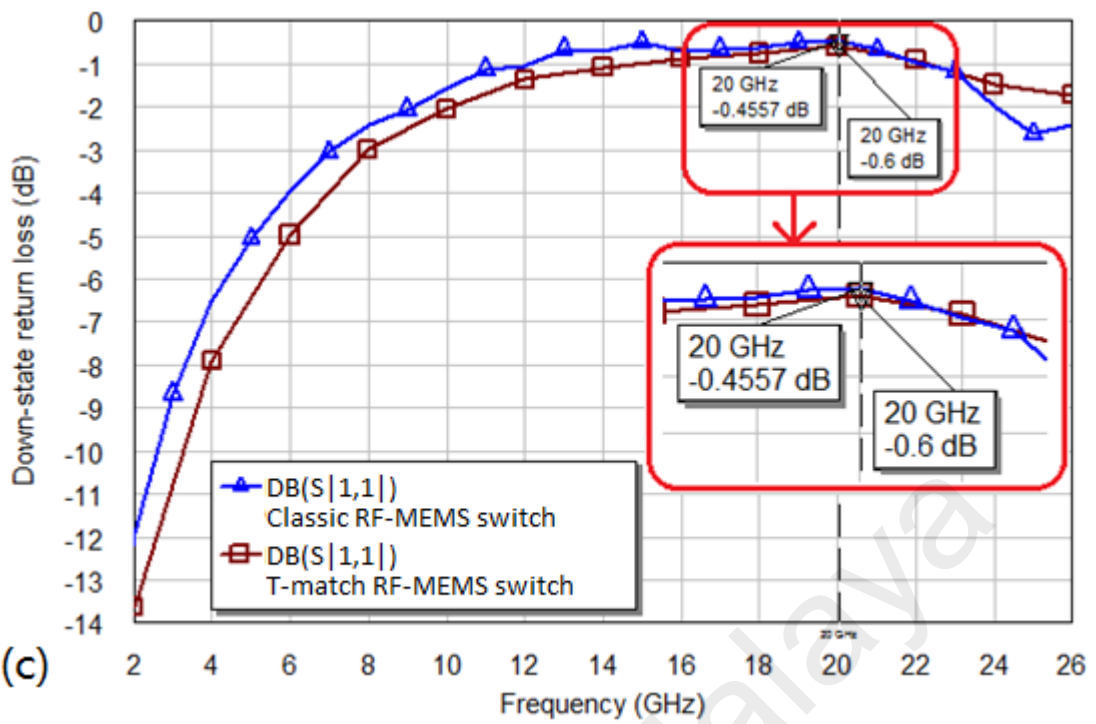
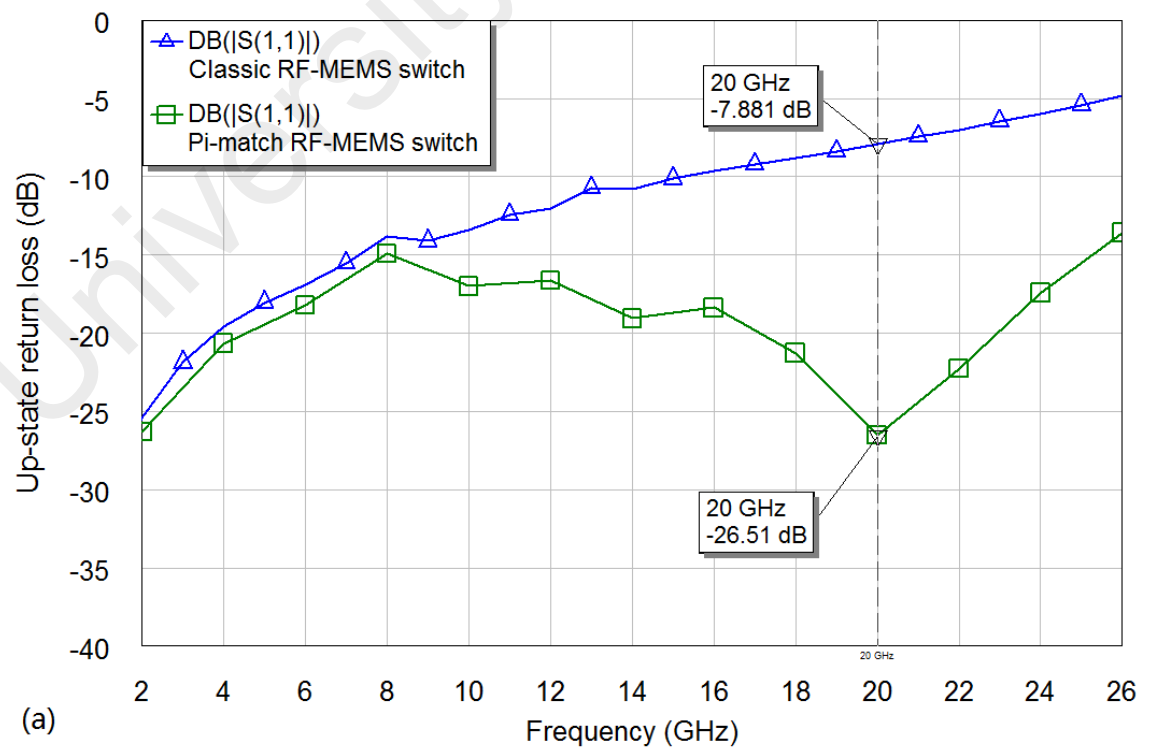


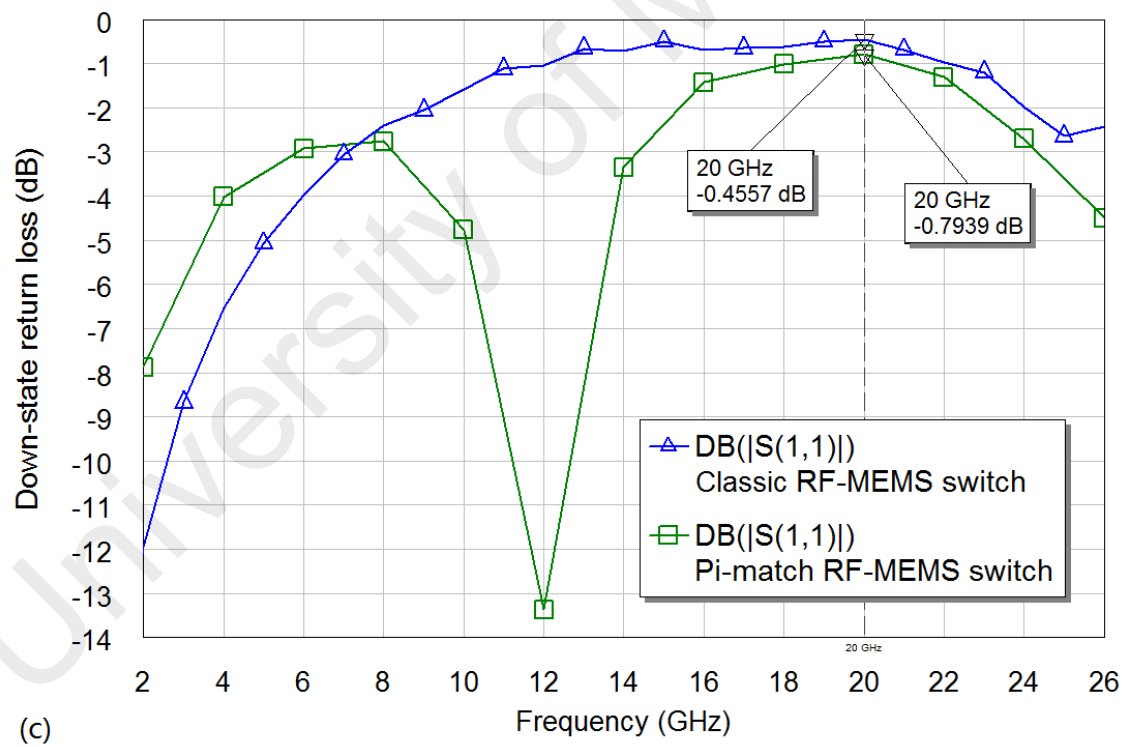
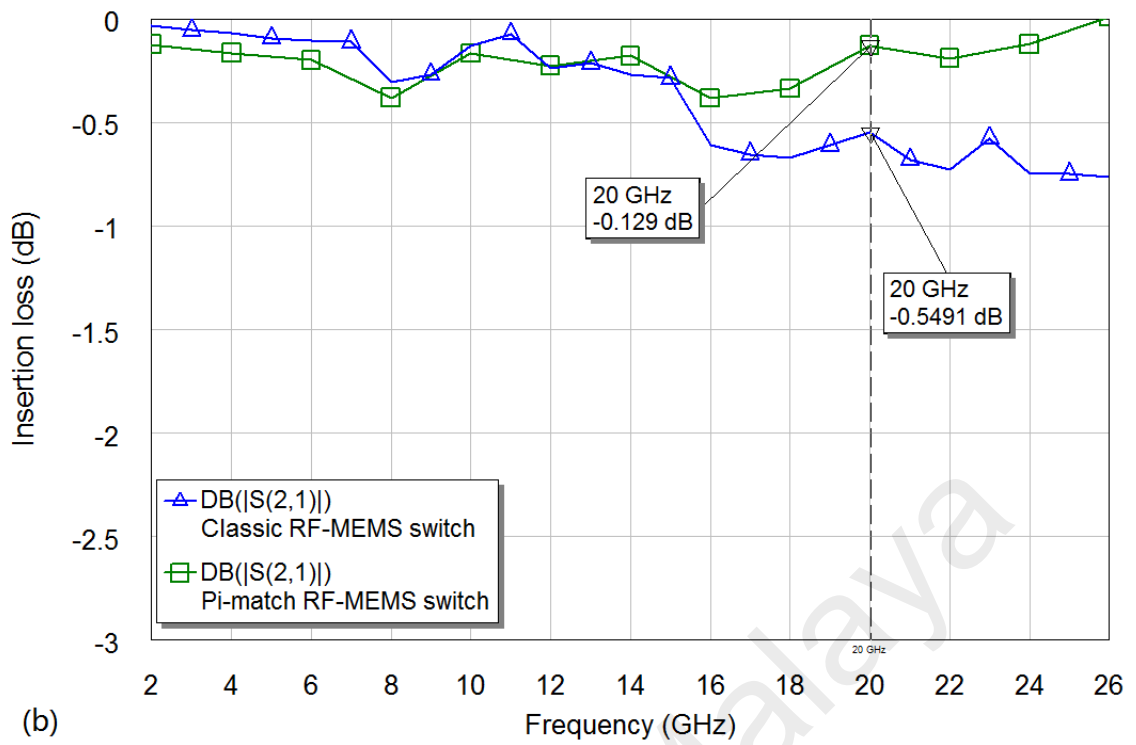
Figure 4.24: S parameters' comparison of the optimized T-match RF-MEMS switch with the classic RF-MEMS switch: (a) up-state return loss ($S_{11_{up}}$), (b) insertion loss ($S_{21_{up}}$), (c) down-state return loss ($S_{11_{down}}$), (d) isolation ($S_{21_{down}}$)

4.3.2 RF Performance of the π -Match RF-MEMS Switch

Figure 4.25 presents the simulated S parameters of the π -match RF-MEMS switch while they were compared with the classic RF-MEMS capacitive switch's RF performance. These results show that: i) the up-state return loss, insertion loss, isolation and down-state return loss of the π -match RF-MEMS switch is -26.51dB, -0.129dB, -0.7939dB and -20.54dB, respectively, at frequency of 20GHz; ii) compared to the classic RF-MEMS switch, the π -match RF-MEMS switch's up-state return loss and insertion loss are improved by 236.5% and 76.5%, at 20GHz, while the down-state return loss and isolation is degraded by 74% and 10.8%, respectively, at 20GHz; iii) S parameters of the π -match RF-MEMS switch at 20GHz all satisfy the predefined design specifications; iv) the overall RF performance of the π -match RF-MEMS switch is better than the classic RF-MEMS switch's; v) the advantage of the π -match RF-MEMS is that it has very high up-state return loss while the drawback is relatively large design area needed.



(a)



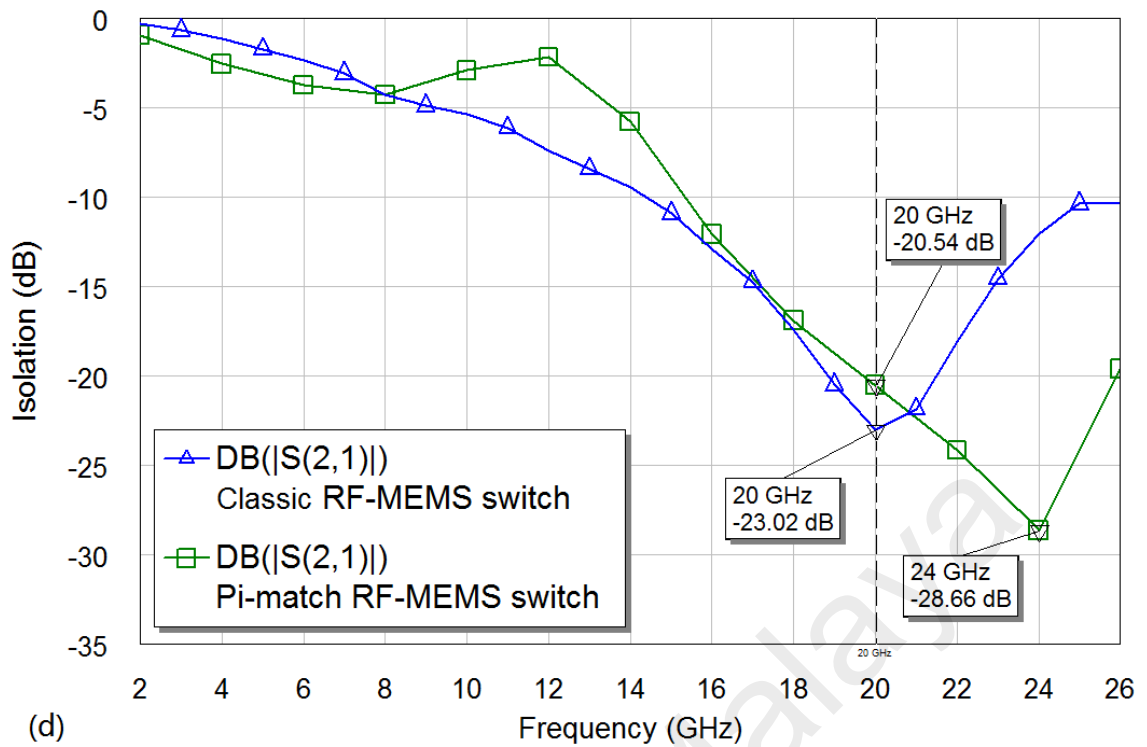


Figure 4.25: S parameters' comparison of the optimized π -match RF-MEMS switch with classic RF-MEMS switch: (a) up-state return loss ($S_{11_{up}}$), (b) insertion loss ($S_{21_{up}}$), (c) down-state return loss ($S_{11_{down}}$), (d) isolation ($S_{21_{down}}$)

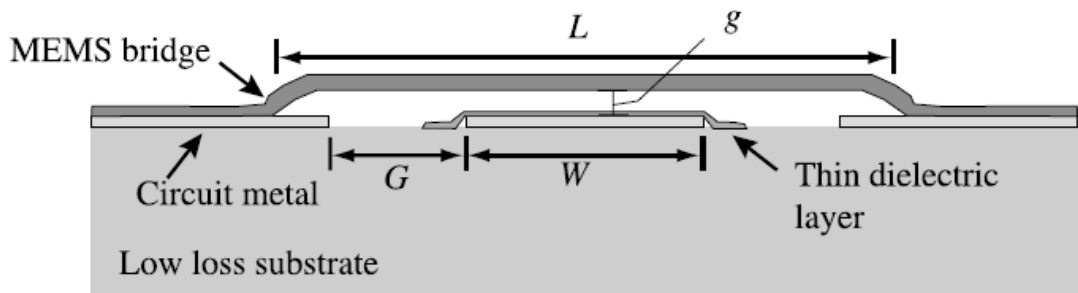
4.4 RF-MEMS Switches' Electromagnetic Modeling Simulations

EM modeling is a way toward displaying the association of electromagnetic fields with physical objects and the environment. In this section, the EM modeling of the classic, T-match and π -match RF-MEMS switches is presented. From the simulated S parameters of these switches, their equivalent lumped elements were extracted.

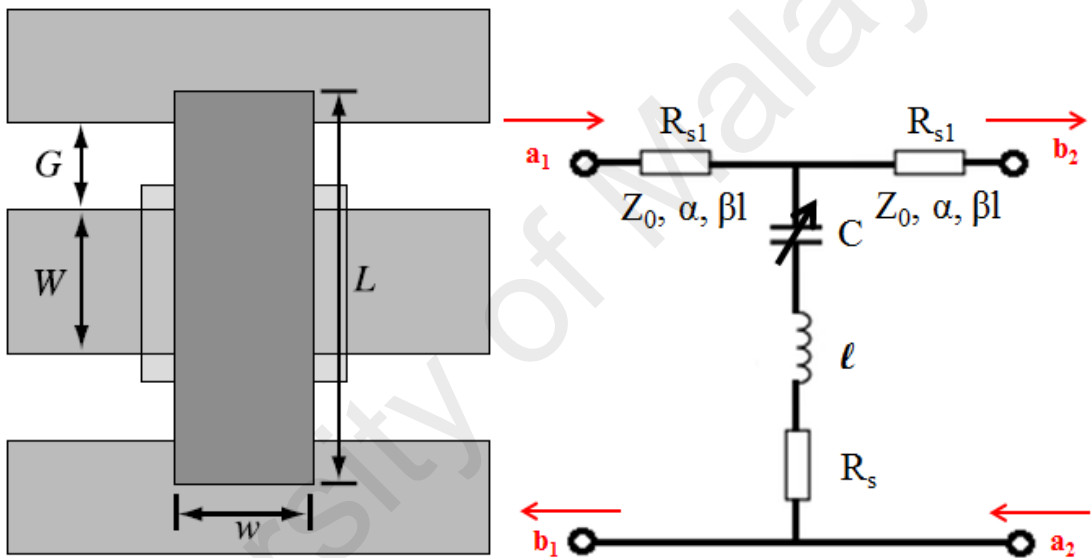
4.4.1 Classic RF-MEMS Capacitive Switch

Generally the RF-MEMS shunt capacitive switch can be modeled by two short sections of transmission line and a lumped RLC model of the membrane (Muldivin & Rebeiz, 2000). Figure 4.26 show a typical RF-MEMS shunt capacitive switch together with its equivalent circuit modeling. The impedance of the RF-MEMS shunt capacitive

switch can be approximated by (4.25); and (4.26) can be used to calculate its cutoff frequency.



(a) Cross-section view of the switch



(b) Plan view of the switch (c) Equivalent circuit of the switch

Figure 4.26: Typical RF-MEMS shunt capacitive switch and its equivalent circuit (Rebeiz, 2003p)

$$Z_s = R_s + j\omega l + \frac{1}{j\omega C} = \begin{cases} \frac{1}{j\omega C} & \leftarrow f \ll f_0 \\ R_s & \leftarrow f = f_0 \\ j\omega l & \leftarrow f \gg f_0 \end{cases} \quad (4.25)$$

$$f_c = \frac{1}{2\pi C_u R_s} \quad (4.26)$$

Where, Z_s is the impedance of the shunt capacitive switch; R_s is the series resistance; l is the inductance; C can be C_d during actuating state and C_u during releasing state; f_0 is the LC series-resonant frequency ($f_0 = (1/2\pi) \times 1/\sqrt{LC}$).

For the classic RF-MEMS capacitive switch, as shown in Figure 3.2 where four folded beams and four spring beams are used to support a big membrane, its equivalent circuit is presented in Figure 4.27 which is a bit different from Figure 4.26 (c). A series resistance and inductance, as well as a shunt capacitance were used to model the spring beams.

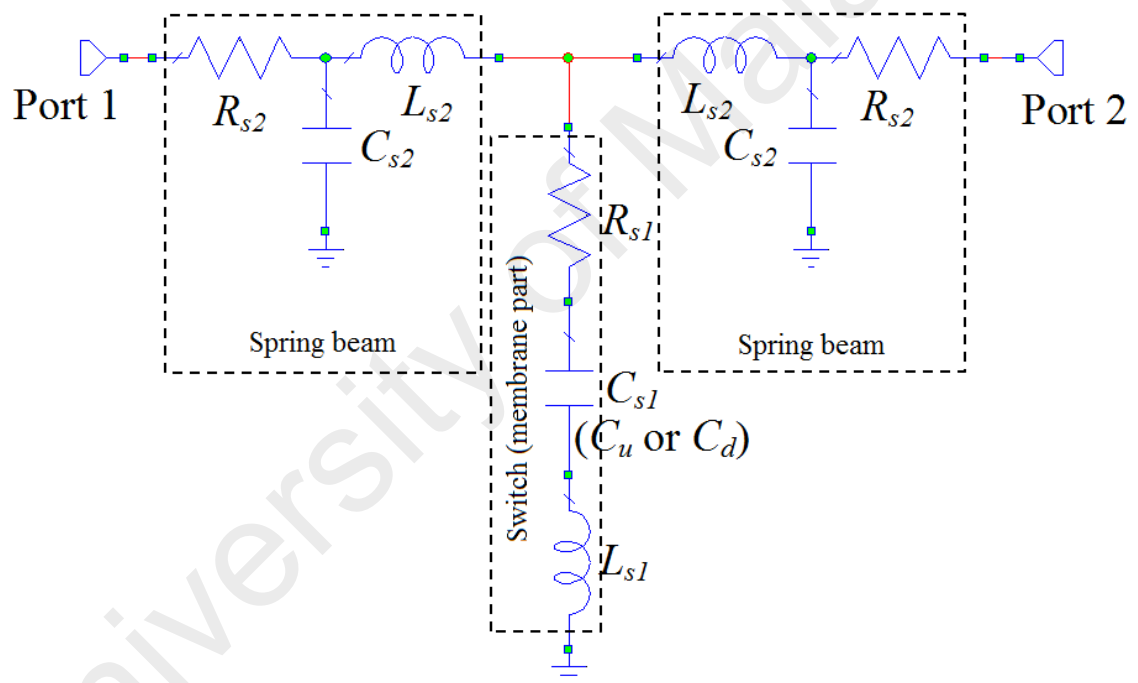


Figure 4.27: Classic RF-MEMS capacitive switch's equivalent circuit

The simulated S parameters of the classic RF-MEMS switch can be used to derive its equivalent electric components, namely RLC values. In the equivalent RLC circuit of the classic RF-MEMS switch (as shown in Figure 4.27), C_{s1} can be replaced by C_u or C_d , when the membrane is at up or down state, respectively. By replacing the simulated switch's LC resonant frequency which is located at the minimum point of isolation and the value of the down-state capacitance into the equation of (4.27), the equivalent

inductance (L_{s1}) of the switch can be obtained. The series resistance (R_{s1}) can be derived from the minimum isolation where the down-state membrane and beams is best fitted around LC resonant frequency (Rebeiz, 2003q), as shown in equation (4.28).

For the optimized classic RF-MEMS shunt capacitive switch model (namely, $t_d=0.1\mu\text{m}$, $g_0=3\mu\text{m}$, $A=W\times L=80\mu\text{m}\times 286\mu\text{m}$, $L1=85\mu\text{m}$, $L2=45\mu\text{m}$, $L3=140\mu\text{m}$, and $w=6\mu\text{m}$), its equivalent lumped elements were derived from the simulated S parameters first. Then the tune tool of the EM simulator was used to tune the values of the lumped elements a bit, in order to match the impedance of the equivalent circuit with the impedance of the classic switch's 3D structure. The final results were summarized in Table 4.4. Figure 4.28 presents the simulated impedance comparison of the classic switch's 3D structure and equivalent circuit, which are agreeing well with each other.

$$f_0 = \frac{1}{2\pi\sqrt{L_{s1}C_d}} \quad (4.27)$$

$$S_{21}|_{\omega_0} = \frac{2R_{s1}\|Z_0}{R_{s1}\|Z_0 + Z_0} \cong \frac{2R_{s1}}{Z_0} \quad (4.28)$$

Where, f_0 is switch's LC resonant frequency when the switch is actuated with $C_{s1}=C_d$; L_{s1} is the switch's equivalent inductance; $S_{21}|_{\omega_0}$ is the switch's minimum isolation, namely the isolation at the LC resonant frequency point; R_{s1} is the switch's equivalent resistance; and Z_0 is the standard RF impedance (50Ω).

Table 4.4: Equivalent lumped elements of the classic RF-MEMS capacitive switch

| Parameter | f_0 (GHz) | Equivalent lumped elements | | | | | | |
|-----------|----------------|----------------------------|-----------|-----------|--------------|-----------------------|--------------|--------------|
| | | R_{s1} (Ω) | C_d (F) | C_u (F) | L_{s1} (H) | R_{s2} (Ω) | C_{s2} (F) | L_{s2} (H) |
| Value | 20 | 1.284 | 7.9p | 101.1f | 7.551p | 0.001 | 35.15f | 33.85p |

Classic RF-MEMS Switch

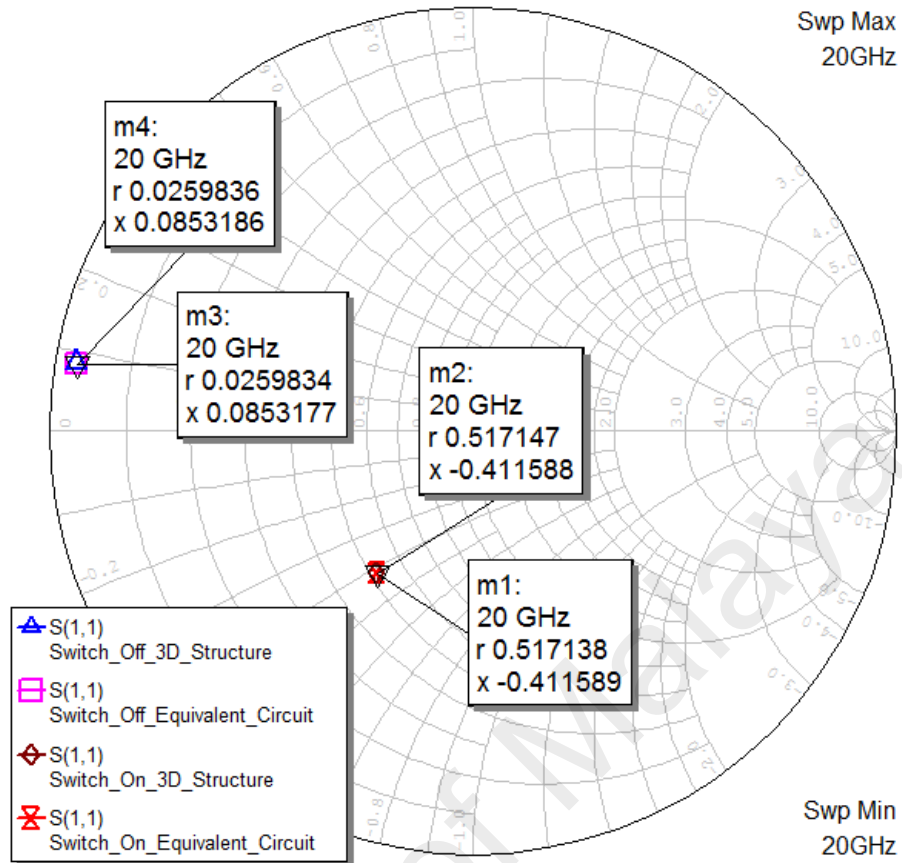


Figure 4.28: Impedance comparison of the classic RF-MEMS capacitive switch's 3D structure and equivalent circuit

4.4.2 T-Match RF-MEMS Capacitive Switch

The optimized T-match RF-MEMS capacitive switch can be modeled by a RLC equivalent circuit, as presented in Figure 4.29; where L_{h-T} , R_{h-T} , and C_{h-T} are the inductance, resistance and capacitance of the high-impedance T-line section, respectively; R_{s1} , C_{s1} , L_{s1} , R_{s2} , C_{s2} and L_{s2} are equivalent lumped elements of the classic RF-MEMS capacitive switch, (C_{s1} can be equaled to C_d or C_u according to the operation state of the switch).

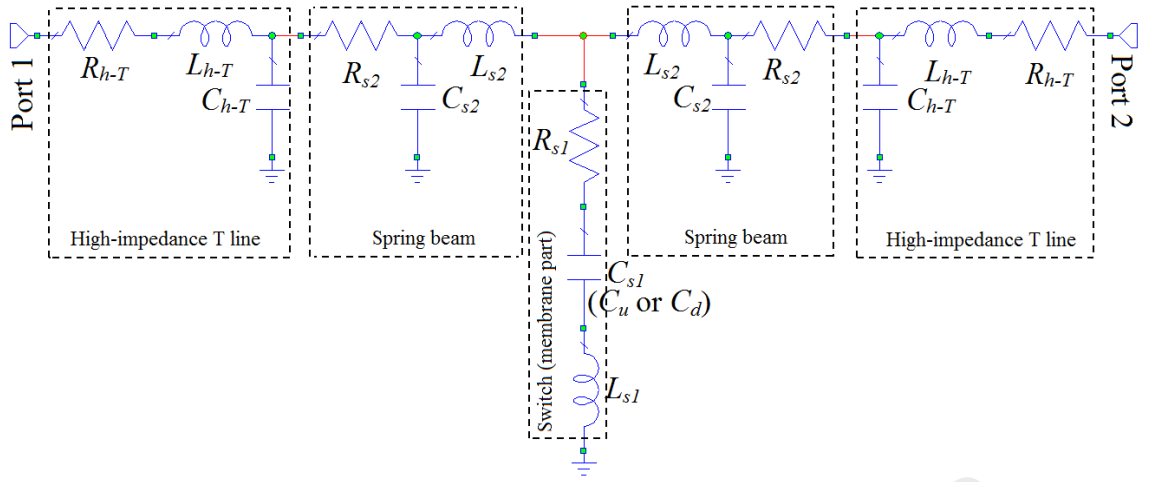


Figure 4.29: T-match RF-MEMS capacitive switch's equivalent circuit

The equivalent lumped element values of the classic RF-MEMS switch have been obtained in the last part. The values of L_{h-T} , R_{h-T} , and C_{h-T} can be extracted by simulating the T-match RF-MEMS switch's impedance or S parameters. If considering the high-impedance T-line section as an ideal inductor, its inductance and the impedance can be directly calculated by using (4.29) and (4.30) (Ma, Nordin, & Soin, 2016). By tuning the values of L_{h-T} , R_{h-T} , and C_{h-T} , at same time comparing the input impedance of the equivalent circuits with the 3D structures of the T-match RF-MEMS switch at different states, the equivalent lumped element values of the high-impedance T-line section can be estimated and obtained as shown in Table 4.5. Figure 4.30 displays the simulated impedance of the T-match RF-MEMS switch's 3D structure and equivalent circuit, which are matching well with each other.

$$L_{h-T} = \frac{1 \pm \sqrt{1 - (\omega C_u Z_0)^2}}{\omega^2 C_u} \quad (4.29)$$

$$Z_{h-T} = \frac{L_{h-T} c}{L_4 \sqrt{\epsilon_{eff}}} \quad (4.30)$$

Where, Z_0 is the standard impedance (50Ω) of RF transmission line; Z_{h-T} is the impedance of the added T line; ϵ_{eff} is the relative effective dielectric constant of the T

line which is about 6.2 for silicon substrate design; and c is the speed of the light in free space (3×10^8 m/s).

Table 4.5: Equivalent lumped elements of the high-impedance T-line section for the T-match RF-MEMS capacitive switch

| Parameter | f_0 (GHz) | Equivalent lumped elements | | |
|-----------|-------------|----------------------------|---------------|---------------|
| | | R_{h-T} (Ω) | C_{h-T} (F) | L_{h-T} (H) |
| Value | 20 | 1.257 | 11.16f | 246.8p |

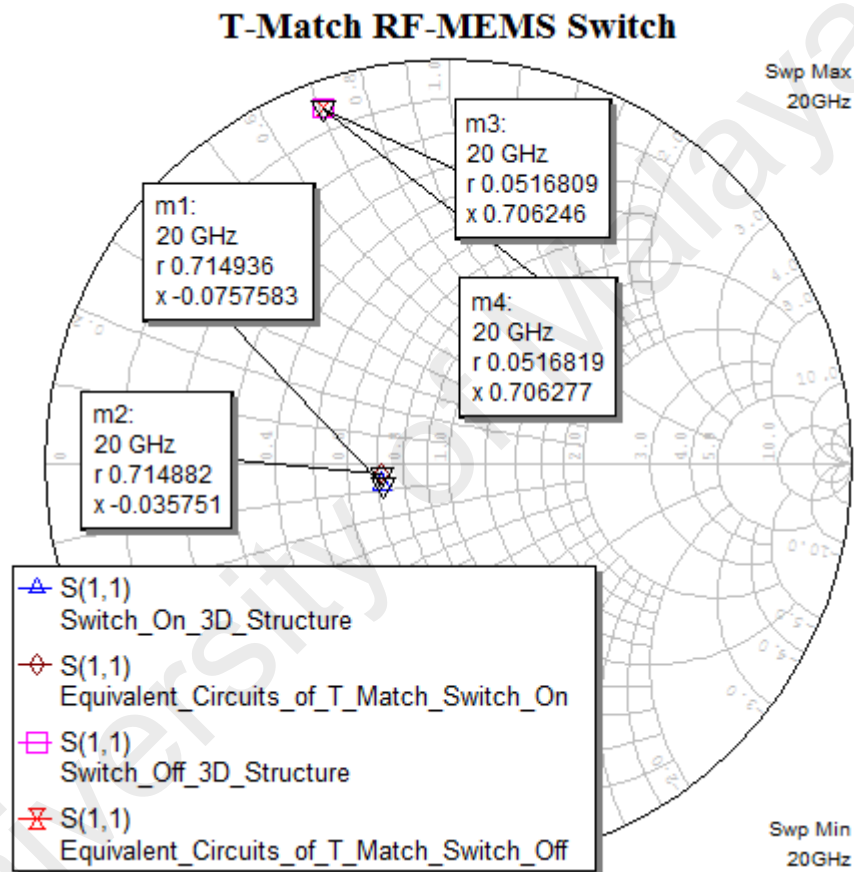


Figure 4.30: Simulated impedance of the T-match RF-MEMS capacitive switch's 3D structure and its equivalent circuit

4.4.3 Π -Match RF-MEMS Capacitive Switch

The optimized π -match RF-MEMS capacitive switch can be roughly modeled by a RLC equivalent circuit, as presented in Figure 4.31. $L_{h-\pi}$, $R_{h-\pi}$, and $C_{h-\pi}$ are the equivalent inductance, resistance and capacitance of the high-impedance T-line section

in the π -match RF-MEMS switch, respectively. Two classic RF-MEMS switches' equivalent circuits were added on the both sides of the high-impedance T-line section.

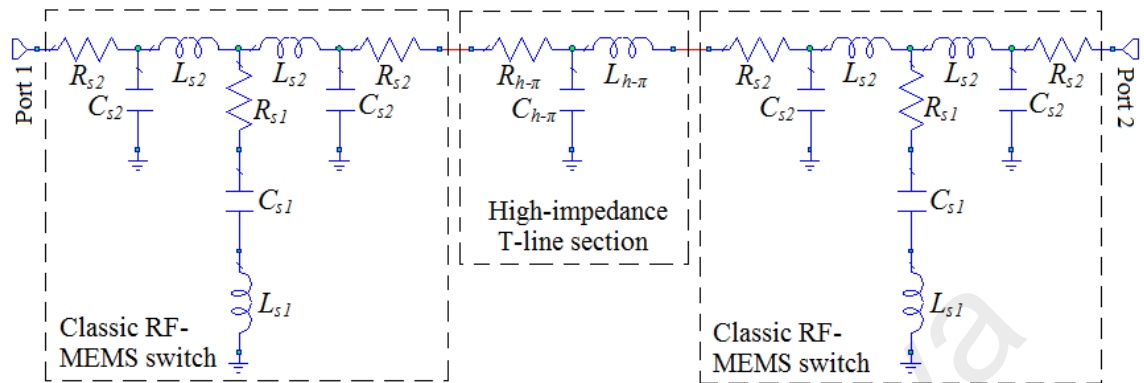


Figure 4.31: Equivalent circuit of the π -match capacitive RF-MEMS switch

If we consider the classic RF-MEMS switch and high-impedance T-line section as ideal components, then only two parallel capacitors (C_{s1}) from the classic RF-MEMS switches and a series inductor ($L_{h-\pi}$) from high-impedance T-line section will be considered in the π -match equivalent circuit. By setting the input impedance of the circuit to be 50Ω , the value of $L_{h-\pi}$ can be derived as shown in (4.31), while its corresponding impedance can be estimated by (4.32) (Rebeiz, 2003i).

$$L_{h-\pi} = \frac{2Z_0^2 C_u}{1 + (\omega C_u Z_0)^2} \quad (4.31)$$

$$Z_{h-\pi} = \frac{L_{h-\pi} c}{L_{hi-\pi} \sqrt{\epsilon_{eff}}} \quad (4.32)$$

Where, Z_0 is the standard impedance (50Ω) of the RF transmission line; $Z_{h-\pi}$ is the impedance of the high-impedance T-line section; ϵ_{eff} is the relative effective dielectric constant of the T-line section which is about 6.2 for silicon substrate design; and c is the speed of the light in free space (3×10^8 m/s).

By using above mentioned calculation method, the rough values of the equivalent circuit's components can be estimated first. Then in order to get a close or better result, a tune tool of linear simulator in AWR™ has been used to adjust the values of $L_{h-\pi}$, $R_{h-\pi}$ and $C_{h-\pi}$, while comparing the both impedance of the 3D structure and its equivalent circuit. The final results are summarized in Table 4.6. Figure 4.32 presents the simulated impedance of the π -match RF-MEMS switch's 3D structure and its equivalent circuit, which are almost matching with each other.

Table 4.6: Equivalent lumped elements of the optimized π -match RF-MEMS capacitive switch

| Parameter | f_0 (GHz) | Equivalent lumped elements | | |
|-----------|----------------|----------------------------|-----------------|-----------------|
| | | $R_{\pi-T}$ (Ω) | $C_{\pi-T}$ (F) | $L_{\pi-T}$ (H) |
| Value | 20 | 0.2926 | 15.83f | 333p |

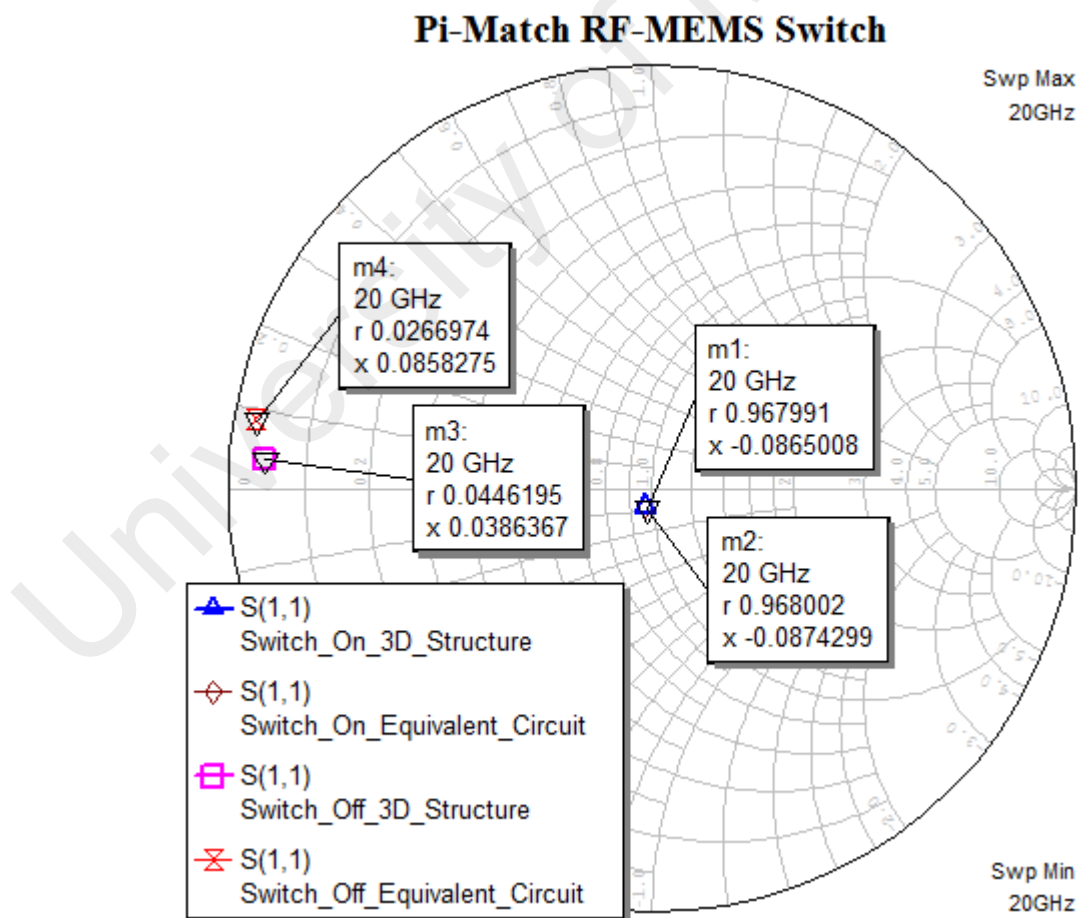


Figure 4.32: Simulated impedance of the π -match RF-MEMS switch's 3D structure and its equivalent circuit

4.5 Simulations of the MEMS Phase Shifters

In this section, the properties of the proposed MEMS phase shifters, namely MEMS switched-line phase shifter and DMTL phase shifter have been simulated and verified by using the EM simulator of AWR Design Environment 10TM.

4.5.1 Simulations of the MEMS Switched-Line Phase Shifter

The RF-MEMS switched-line phase shifter's properties and functions have been simulated and verified by FEM simulations, as shown in Figure 4.33 to Figure 4.36. For 3-bit phase shifter, there are a total of eight phase states, as displayed in Figure 4.33, which are 0°, 45.03°, 88.09°, 136°, 180°, 225°, 268°, and 316° at the frequency of 20 GHz. The phase error for each phase shift is presented in Figure 4.34, where the average phase error is 0.2445° at the frequency of 20 GHz.

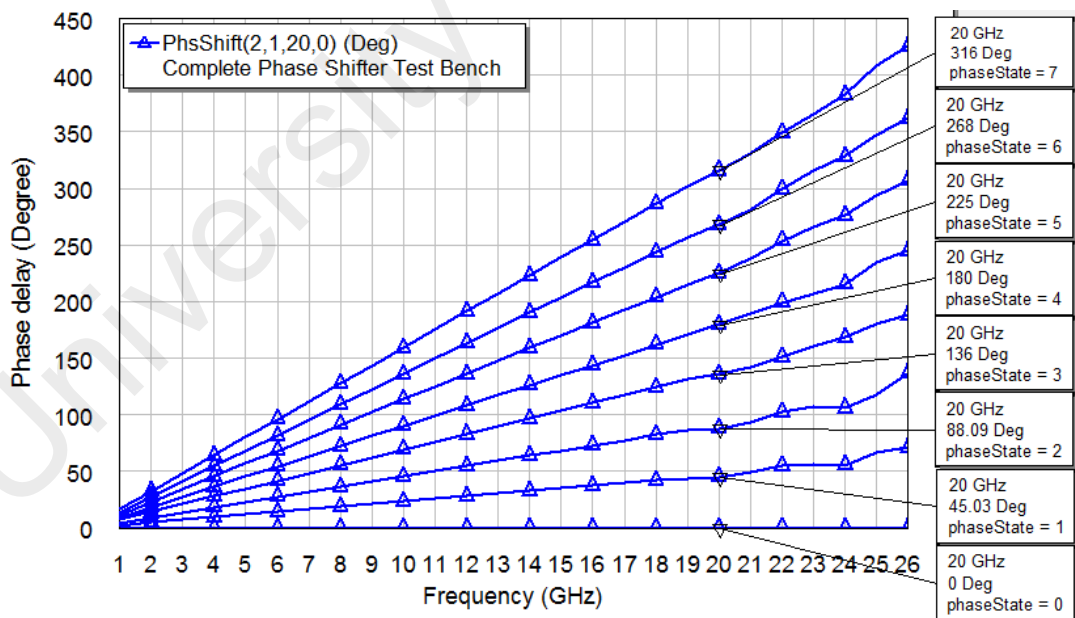


Figure 4.33: Phase shifts of the 3-bit MEMS switched-line phase shifter

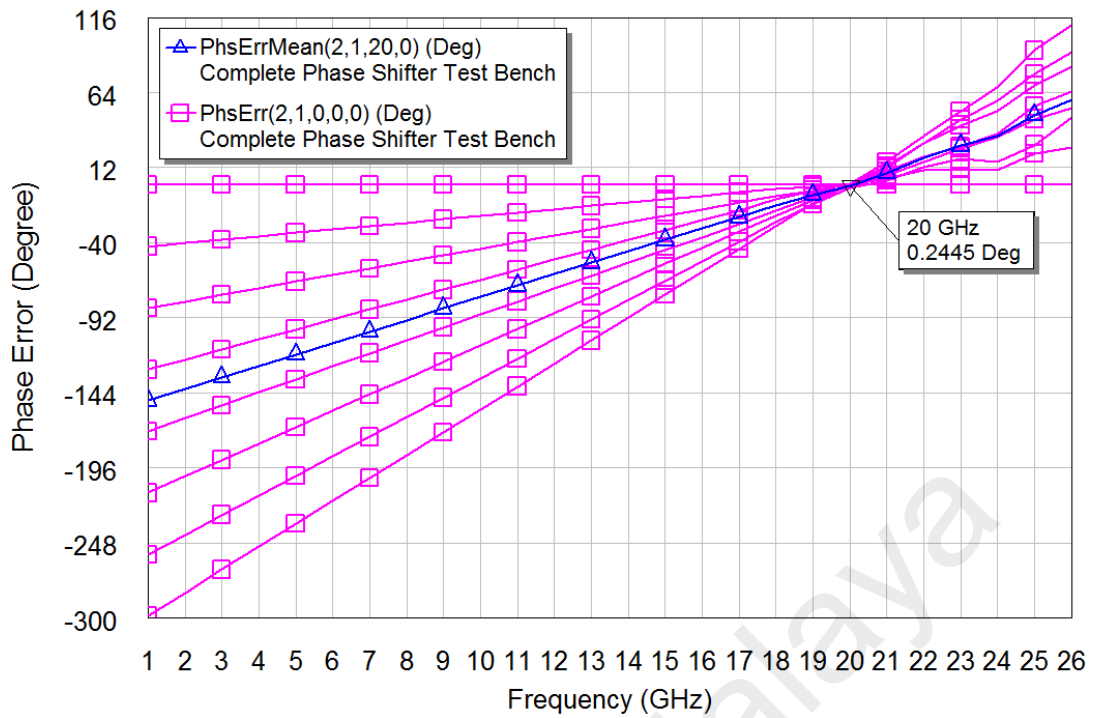


Figure 4.34: Phase errors of the 3-bit MEMS switched-line phase shifter

The insertion loss of the MEMS switched-line phase shifter is presented in Figure 4.35. It can be seen that the average insertion loss is -2.447dB; for all the phase shifts, the minimum insertion loss is -2.0414dB and the maximum insertion loss is -2.722dB at the frequency of 20GHz. The return loss for the phase shift of 45°, 90° and 180° are presented in Figure 4.36. It shows that all the return losses are higher than 10dB in a wideband range of less than 20GHz; meanwhile, the curve of S11 is identical to S22 which means the proposed MEMS switched-line phase shifter is a reciprocal network (Shea et al., 1971); it works effectively on signals passing through it in either direction.

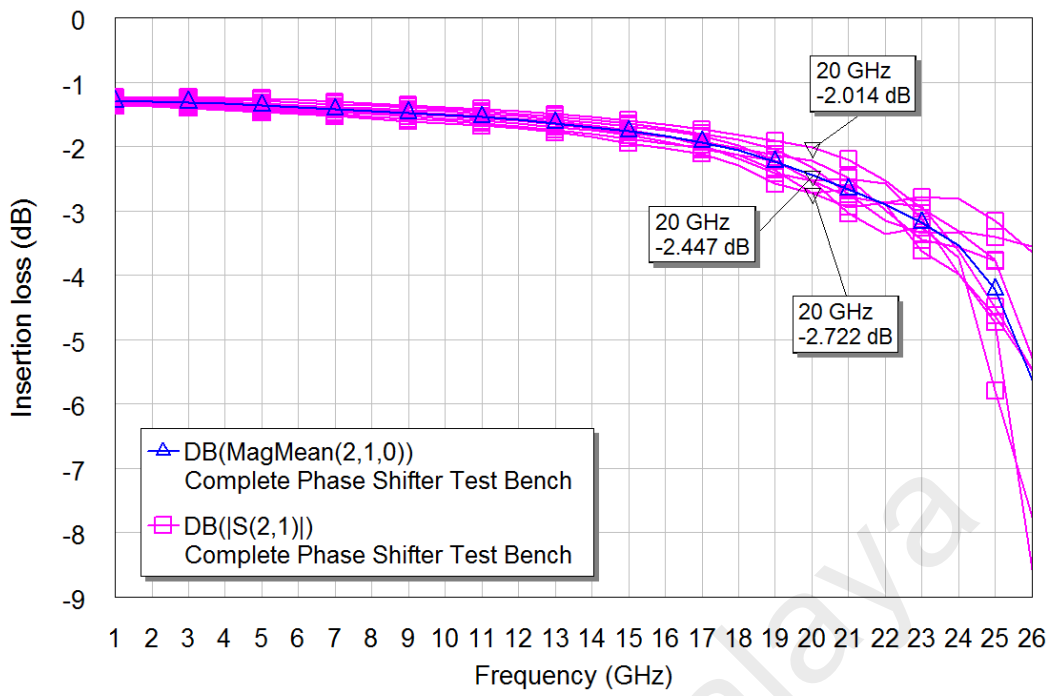
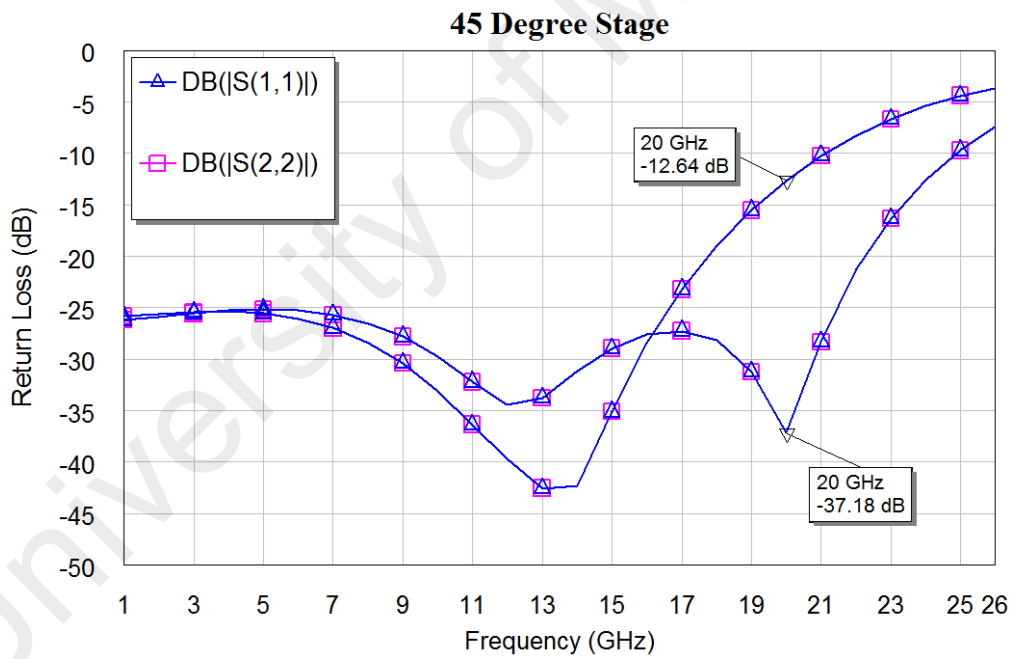
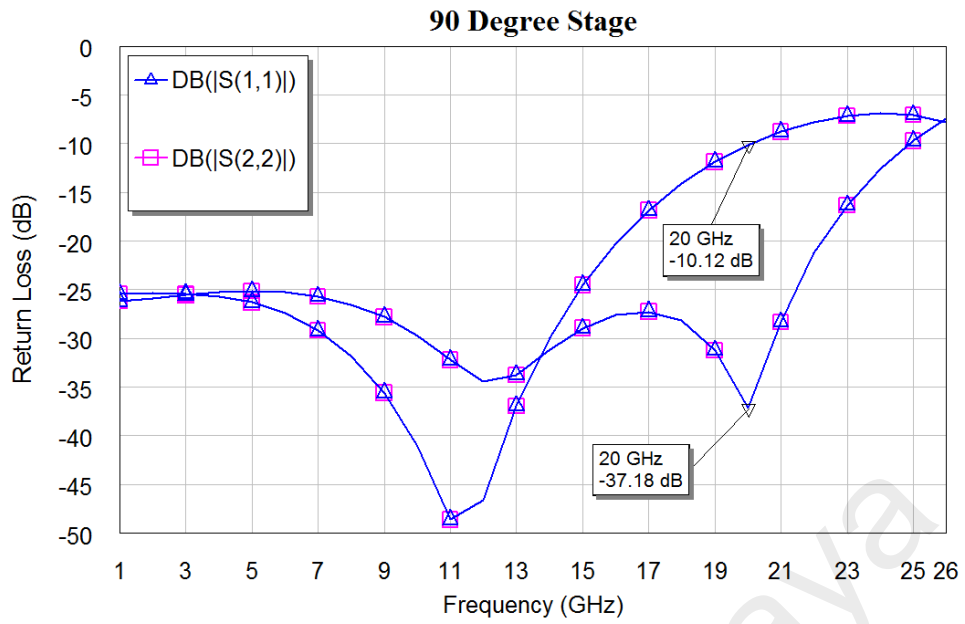


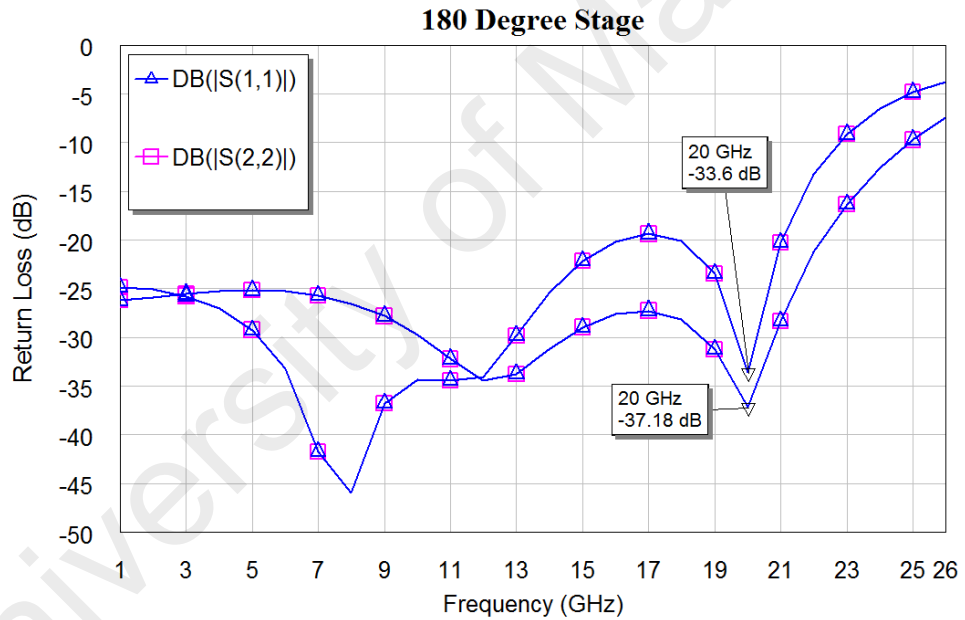
Figure 4.35: Insertion loss of the 3-bit switched-line phase shifter



(a) 45°-bit stage



(b) 90°-bit stage



(c) 180°-bit stage

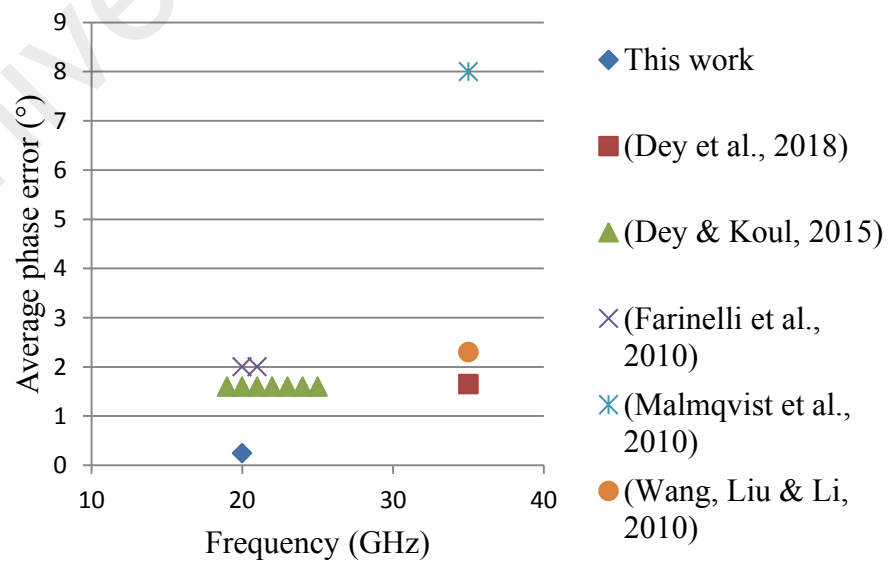
Figure 4.36: The switched-line phase shifter’s return loss at each stage

A comparison of the proposed MEMS switched-line phase shifter with other state-of-the-art work is summarized in Table 4.7. Figure 4.37 plot the average phase error and actuation voltage’s comparison of this work with other state-of-the-art MEMS phase shifters. From these results, it can be seen that the proposed MEMS switched-line phase shifter has very low voltage of 3V and very small average phase

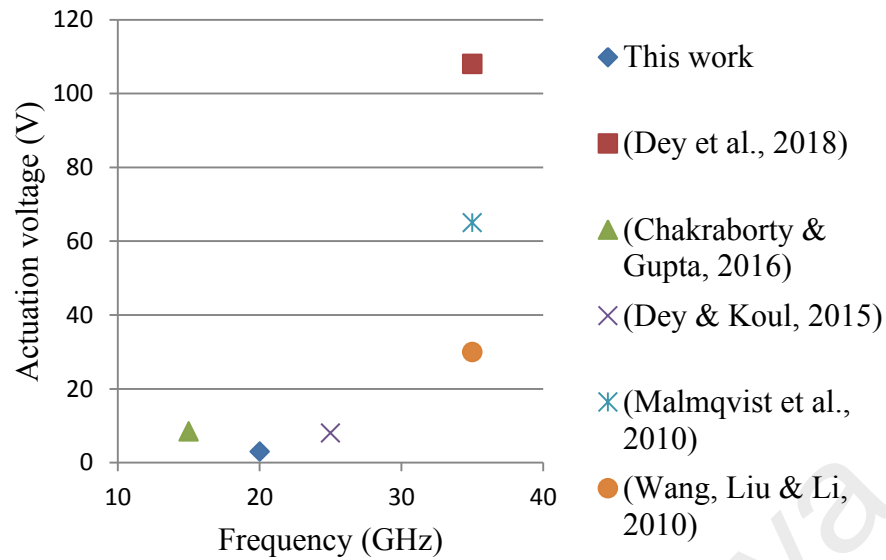
error of 0.2445° which thanks to the usage of low-voltage low-loss T-match RF-MEMS capacitive switch.

Table 4.7: Comparison of MEMS switched-line phase shifter designs

| Reference | (Farinelli et al., 2010) | (Malmqvist et al., 2010) | (Wang, Liu, & Li, 2010) | This work |
|------------------------|---|--|--|---|
| Frequency | 20.2-21.2GHz | 35GHz | 35GHz | 20GHz |
| Switch type | Hybrid | Metal-contact | Metal-contact | Capacitive |
| $V_{pull-in}$ | - | 65V | 30V | 3V |
| T-line type | Micro strip | CPW | CPW | CPW |
| Substrate | 200 μm , high resistivity, Si | 600 μm , GaAs | Borofloat TM glass | 500 μm , high resistivity, Si |
| Bit No. | 5 | 3 | 3 | 3 |
| RMS phase error | $<2^\circ$ | 8° | 2.3° | 0.2445° |
| Average insertion loss | 2.1dB | 4.8dB | 2.35dB | 2.447dB |
| Return loss | $>15\text{dB}$ | - | $>12\text{dB}$ | $>10\text{dB}$ |
| Design area | 6.5 \times 4.5mm ² (total) | 2 \times 4mm ² (total) | 3 \times 2mm ² (for 1-bit) | 6 \times 4mm ² (total) |
| Remark | The most significant 4 bits are realized by switched lines and the less significant bit uses loaded line topology | The two largest bits are realized by switched delay lines and the smallest bit uses loaded line techniques | Air-bridge with step compensation technique is used to improve the performance of CPW bend | Novel T-match low-voltage-control low-loss RF-MEMS switch is used |



(a) Average phase error



(b) Actuation voltage

Figure 4.37: Important properties' comparison of the state-of-the-art MEMS phase shifters

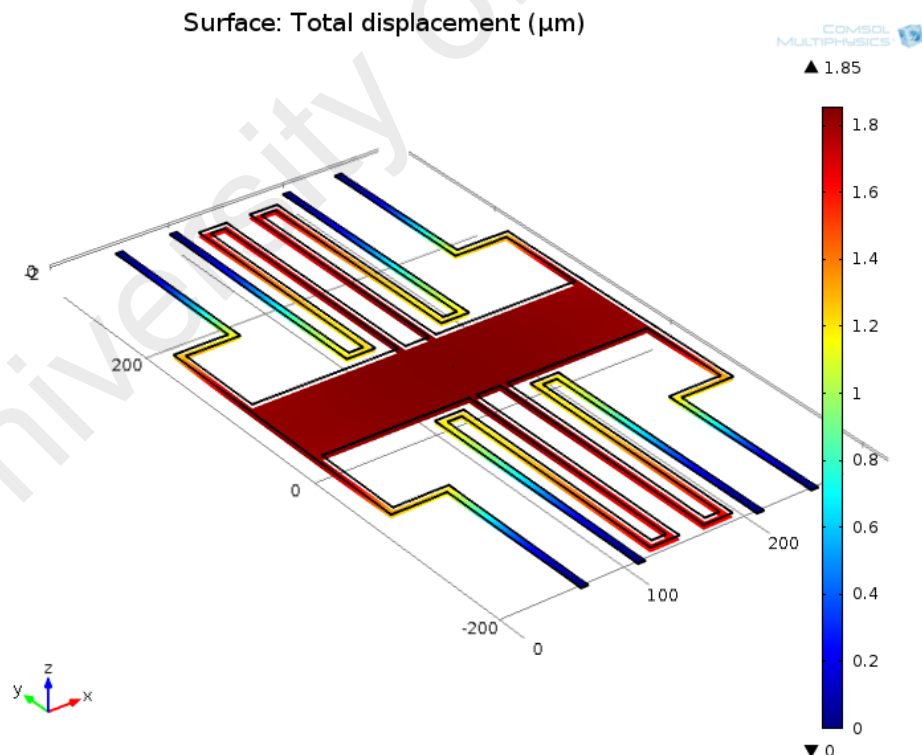
4.5.2 Simulations of the DMTL Phase Shifter

As mentioned in section 3.5.2.2, in order to fulfill the capacitance requirement of the proposed DMTL phase shifter, the classic RF-MEMS switch has been modified with a narrower signal line and thicker dielectric layer. This section presents the simulation and verifications of the modified RF-MEMS capacitive switch and the designed 3-bit DMTL phase shifter.

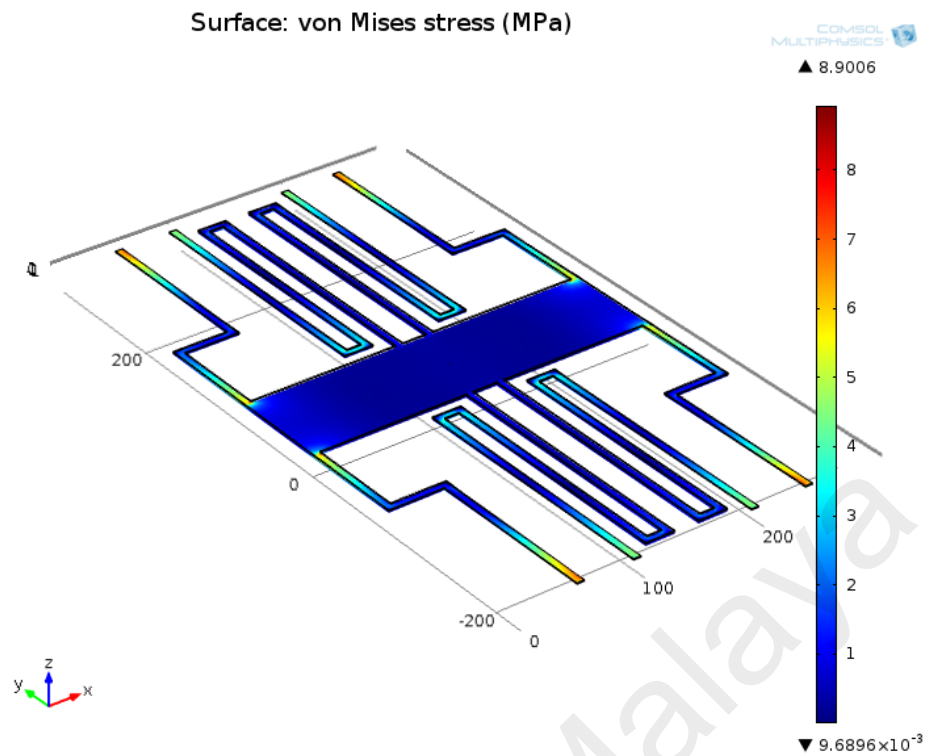
4.5.2.1 Modified Classic RF-MEMS Switch

Some important characteristics of the modified RF-MEMS capacitive switch have been verified by Comsol Multiphysics® in this section, such as capacitance, pull-in voltage, vertical displacement, and von Mises stress.

The simulation model was created according to the structure shown in Figure 3.31, the dimensions of Design 3 in Table 3.3 and Table 3.20. The materials' and boundary conditions' settings are same as the settings in section 4.2.1. The simulated capacitance for switch-on state is 12.337fF and switch-off state is 125.01fF. Comparing with the design values of 12.3fF and 125.2fF, the error is within 0.3%. Figure 4.38 shows the maximum vertical displacement of the membrane and its maximum von Mises stress when the switch is actuated. The maximum displacement is 1.85 μm ; and at the same time, the maximum von Mises stress is 8.9MPa which is much less than the aluminum's yield stress (15~20MPa) (Howatson, 2012); therefore the structure is stable and robust. The pull-in voltage of the modified RF-MEMS capacitive switch was simulated also as displayed in Figure 4.39, which is around 5V. This increased pull-in voltage is mainly due to the narrower signal line used which makes the actuation area to become smaller.



(a) Membrane's vertical displacement



(b) Membrane's maximum von Mises stress

Figure 4.38: The maximum vertical displacement and von Mises stress distribution of the modified RF-MEMS capacitive switch

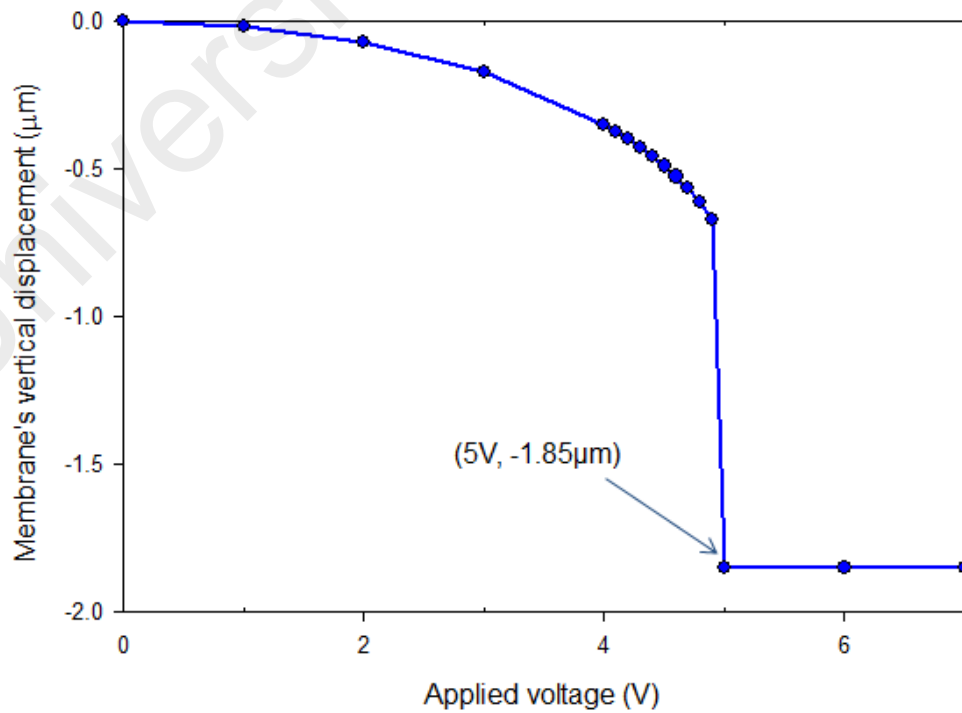


Figure 4.39: Simulated pull-in voltage of the modified RF-MEMS capacitive switch

4.5.2.2 DMTL Phase Shifter

The designed 3-bit DMTL phase shifter has been simulated and verified by FEM approach by using Microwave Office[®]. In this simulation, the periodic spacing has been optimized first in order to obtain the best insertion loss and return loss of the DMTL phase shifter by using simulation tune function in the software. And periodic spacing of 312 μm (instead of 309 μm) was determined and employed finally. Figure 4.40 shows the unloaded CPW's impedance simulation, where in order to obtain a 65- Ω CPW at 20 GHz with 500- μm silicon substrate, the width of the signal line and the gap between signal line and ground line should be 44 μm and 65 μm , respectively. The DMTL phase shifter's properties and functions were displayed in Figure 4.41 to Figure 4.45.

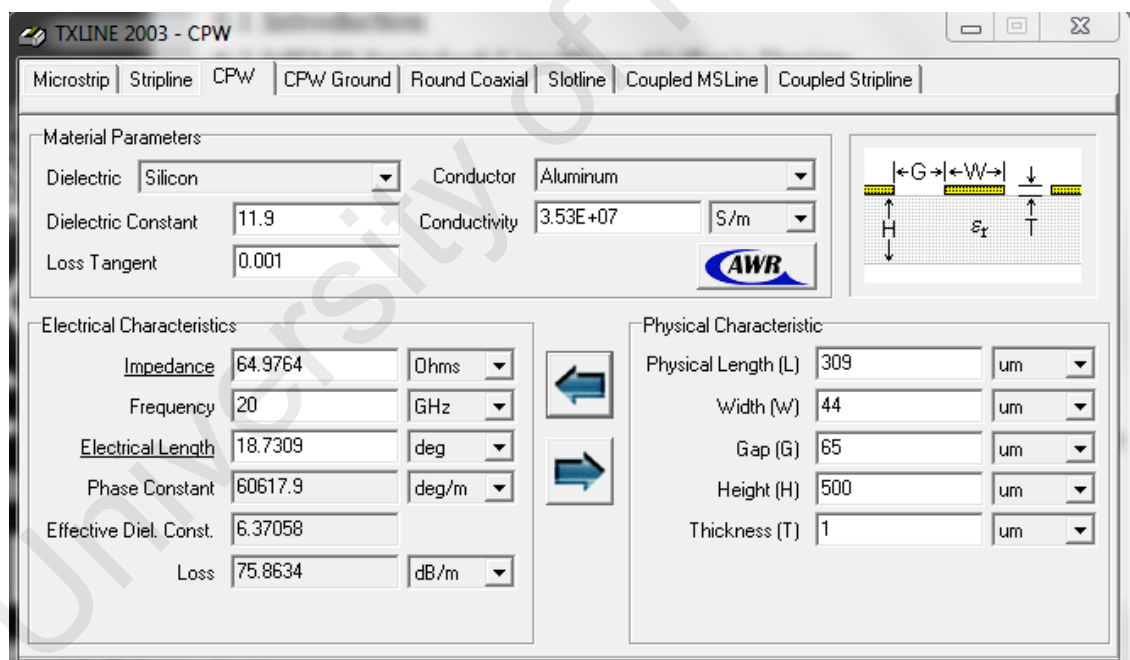


Figure 4.40: 65- Ω CPW line's characteristic

For 3-bit phase shifter, there are a total of eight existing phase states, as displayed in Figure 4.41, which are 0° , 46.68° , 93.54° , 140.1° , 186.5° , 2232.6° , 280.9° , and 328° at the frequency of 20 GHz. The phase error for each phase shift and their mean value are

presented in Figure 4.42, where the average phase error is 6.032° at the frequency of 20 GHz and average 0° phase error is happened at frequency of 19.47GHz.

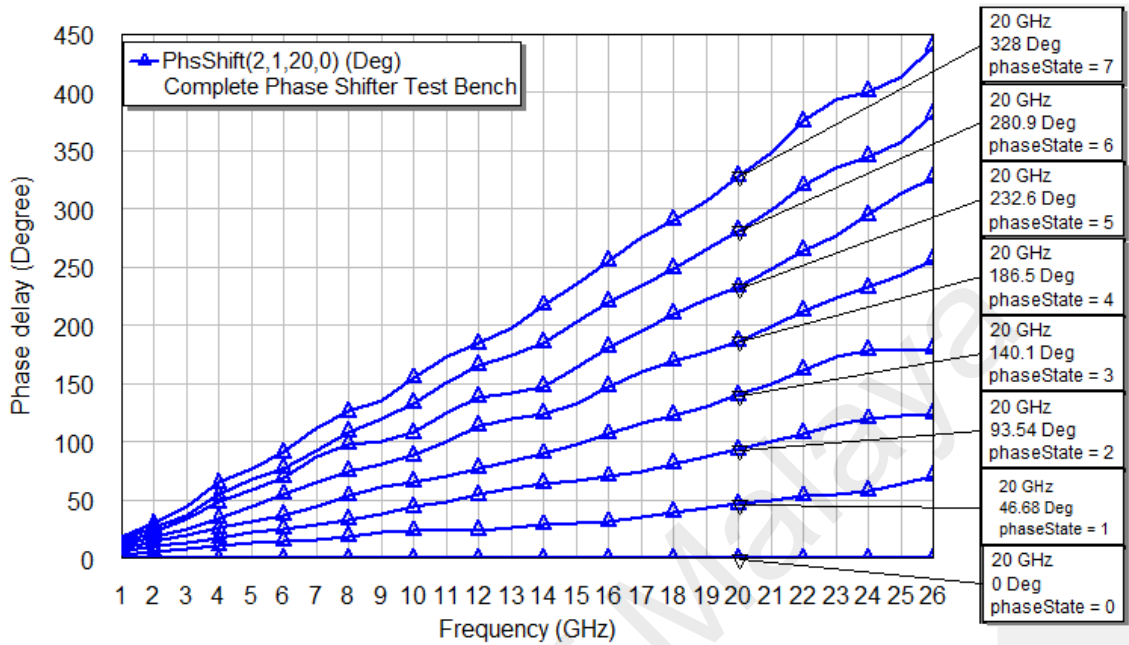


Figure 4.41: Phase delay of the 3-bit DMTL phase shifter

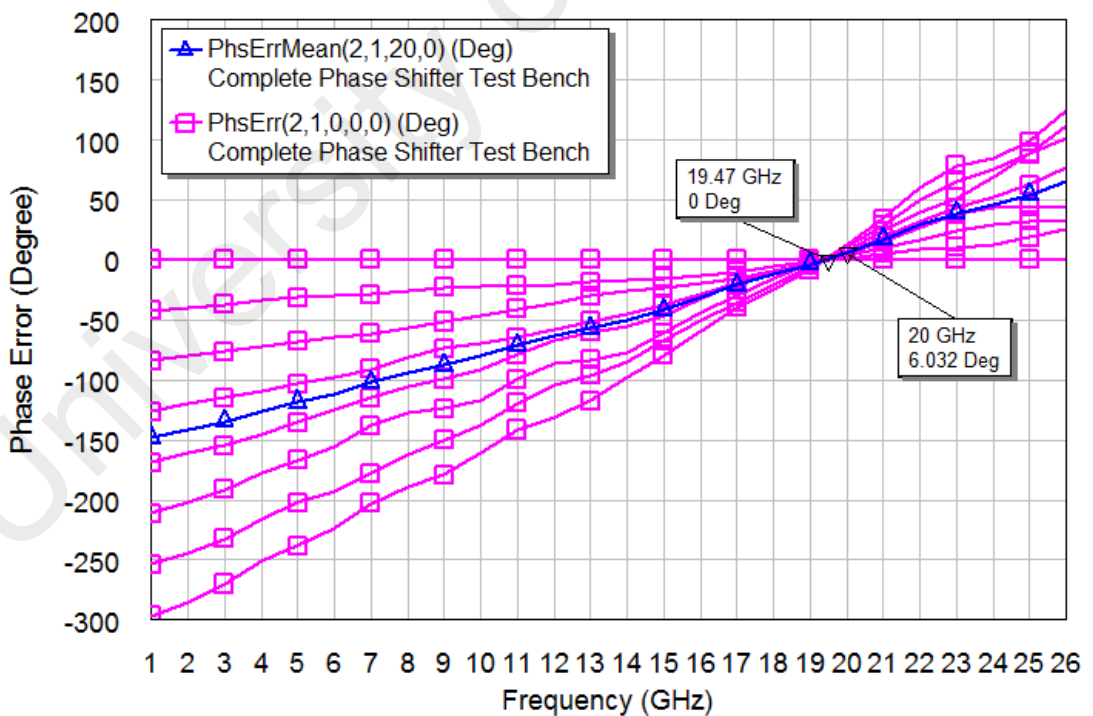
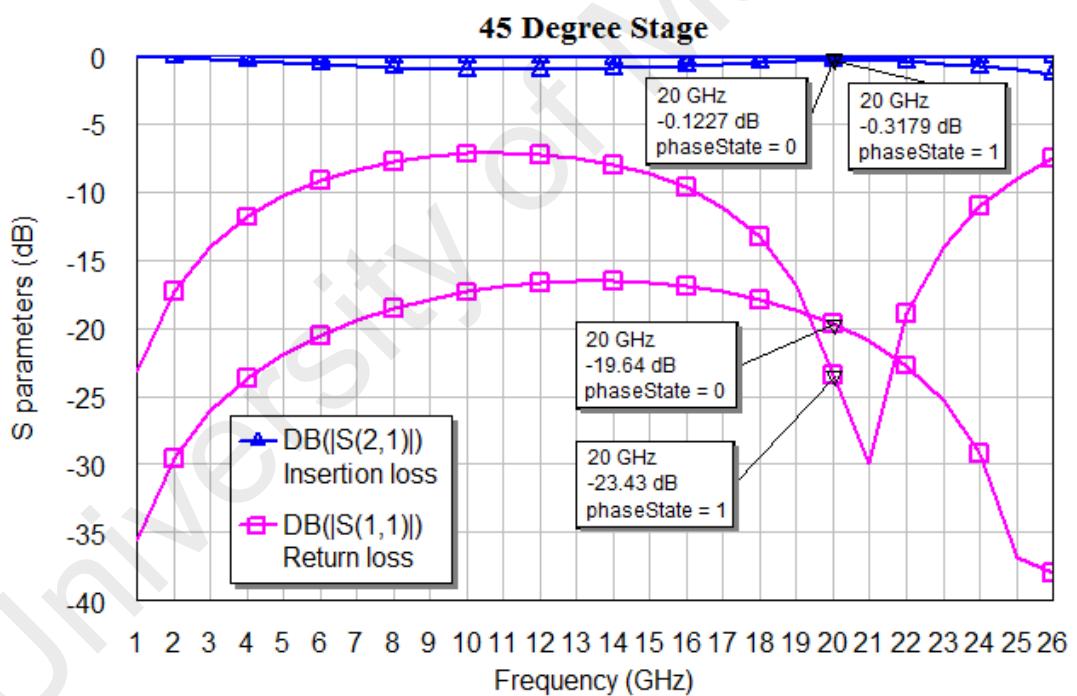


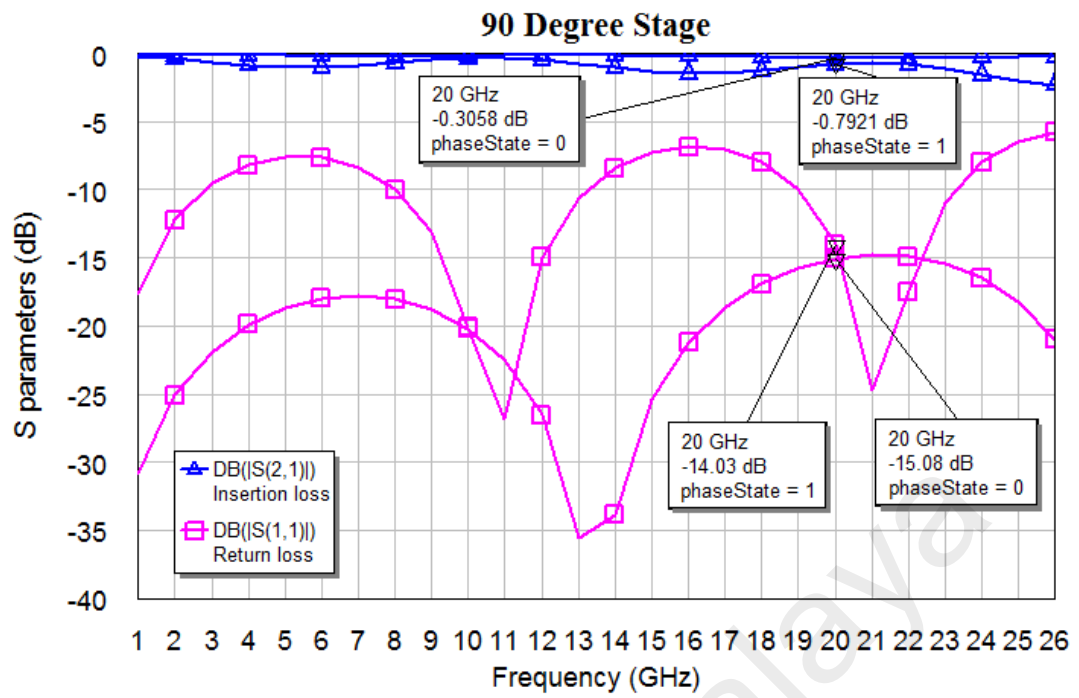
Figure 4.42: Phase error of the 3-bit DMTL phase shifter

The insertion loss and return loss of each stage of the DMTL phase shifter has been verified separately as shown in Figure 4.43. At 20 GHz, the maximum insertion loss and

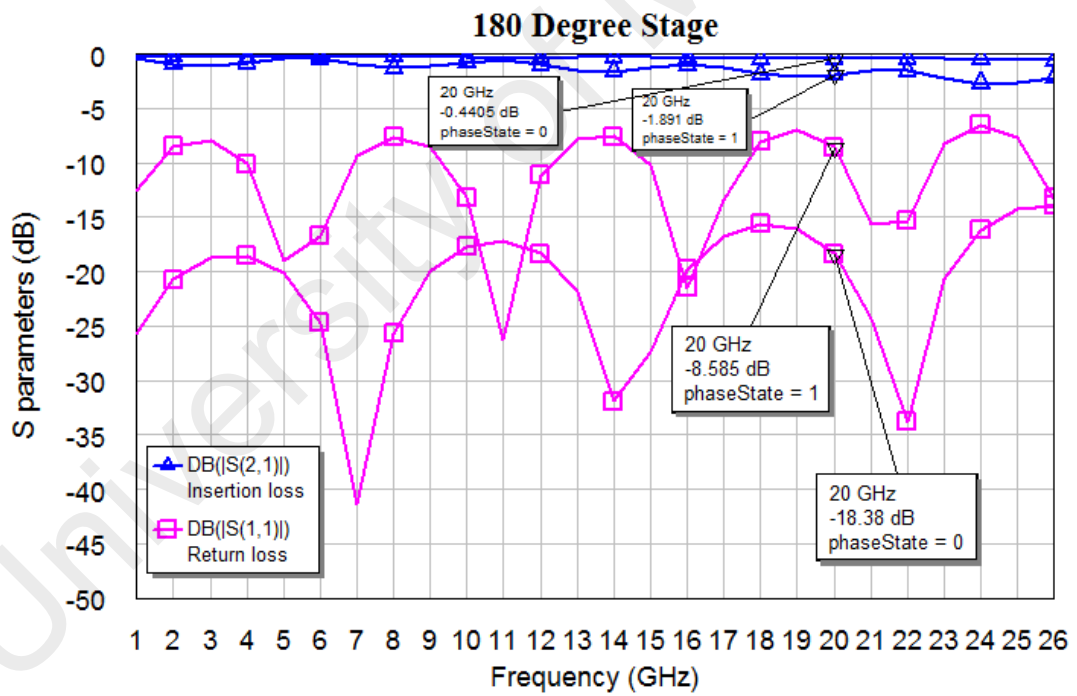
minimum return loss for 45° stage is -0.3179dB and -19.64dB, respectively; for 90° stage is -0.7921dB and -14.03dB, respectively; and for 180° stage is -1.891dB and -8.585dB, respectively. These results show that the insertion loss and return loss of the DMTL phase shifter will degrade by increasing the bit number since more RF-MEMS switches are used. The insertion loss and return loss of the whole 3-bit DMTL phase shifter for each phase delay state are also performed as shown in Figure 4.44 and Figure 4.44. The average insertion loss is -1.526dB, the best one is -0.6423dB, and the worst condition is -2.29dB at frequency of 20GHz. In Figure 4.45 it can be seen that for all the phase shift conditions, the return loss is better than -10.05dB, the best one is -28.86dB, and the average return loss is -17.73dB at frequency of 20GHz.



(a) 45° stage



(b) 90° stage



(c) 180° stage

Figure 4.43: Each stage insertion loss and return loss of the 3-bit DMTL phase shifter

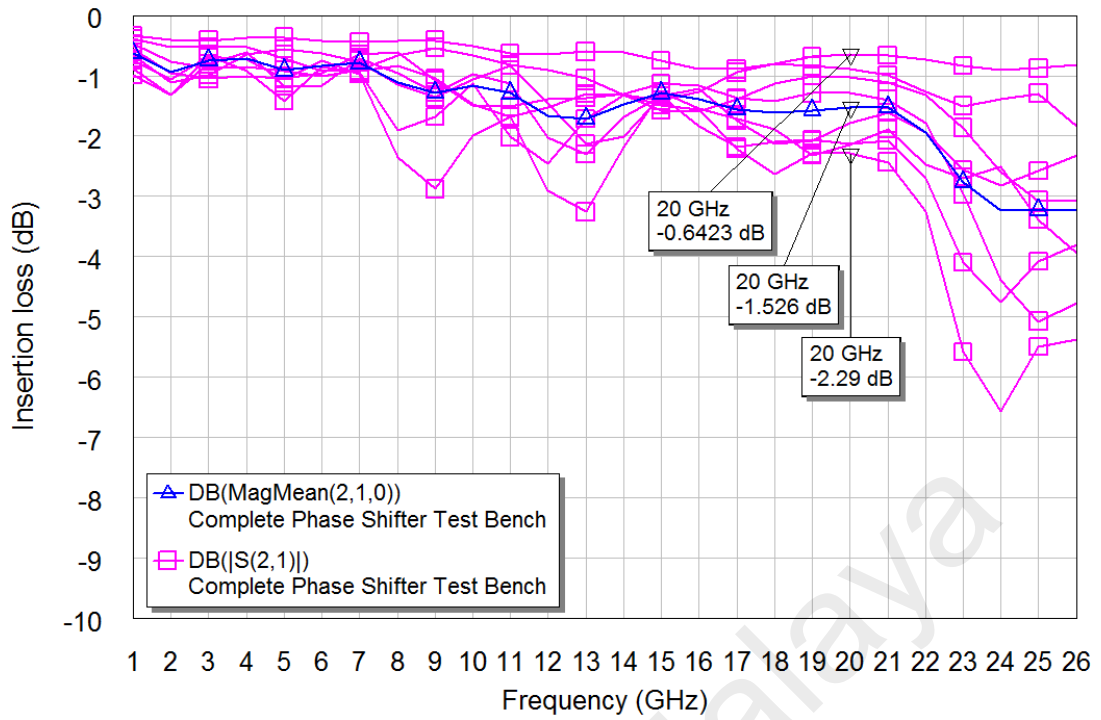


Figure 4.44: Insertion loss of the 3-bit DMTL phase shifter

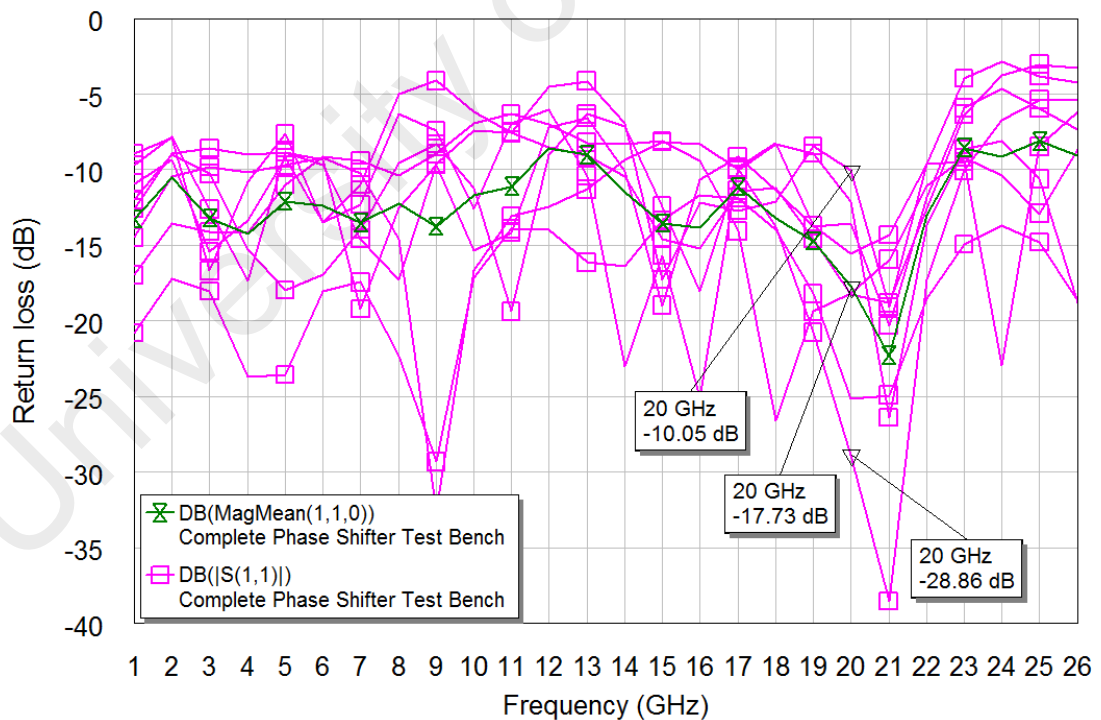


Figure 4.45: Return loss of the 3-bit DMTL phase shifter

A comparison of the proposed DMTL phase shifter with other related designs has been done and is summarized in Table 4.8. From this table, it can be seen that the

developed DMTL phase shifter has small pull-in voltage (namely 5V) and average insertion loss (namely, 1.526dB) compared to other designs. However, the average phase error is a bit large (6.032°) which can be improved in the future work.

Table 4.8: Comparisons of DMTL phase shifter designs

| Reference | (Barker & Rebeiz, 2000) | (Hung, Dussopt, & Rebeiz, 2004) | (Reinke, Wang, Fedder, & Mukherjee, 2011) | This work |
|------------------------|---|--|--|---|
| Frequency | 40~60, 75~110GHz | 75~110GHz | 32GHz | 20GHz |
| Switch type | Capacitive | Capacitive | Capacitive | Capacitive |
| $V_{pull-in}$ | 13 & 26V | 30V | 20V | 5V |
| T-line type | CPW | CPW | CPW | CPW |
| Substrate | 500 μ m, quartz | glass | Silicon | 500 μ m, high resistivity, Si |
| Bit No. | 1 | 3 | 4 | 3 |
| RMS phase error | - | 3° | - | 6.032° |
| Average insertion loss | 2.1dB | 2.7dB | 2.9dB | 1.526dB |
| Return loss | >15dB | >10dB | >10dB | >10dB |
| Design area | 6.5 \times 4.5mm ² (total) | 5.04 \times 1.92mm ² (total) | 2.42mm ² (total) | 12.8 \times 1.4mm ² (total) |
| Remark | A comprehensive optimization method for DMTL phase shifter has been introduced in the design. | A high-Q MAM capacitor was developed and used in the design. | The CMOS-MEMS process with maskless and post-CMOS etching technique is used in the design. | It is a low-voltage control and low-loss DMTL phase shifter; structure is simple. |

4.6 Summary

This chapter mainly talks about the simulation results of the designed RF-MEMS switches and MEMS phase shifters.

The optimized classic RF-MEMS capacitive switch has been simulated and analyzed from three aspects, namely static properties, dynamic properties and RF performance, by using Comsol Multiphysics[®] and AWR[®] software. For static analysis, the simulation results show that the optimized classic RF-MEMS switch has spring constant of 0.2378N/m, resonant frequency of 7.24 kHz, maximum von Mises stress of 14.031MPa,

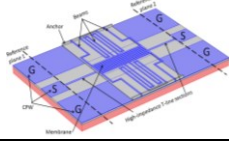
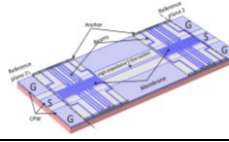
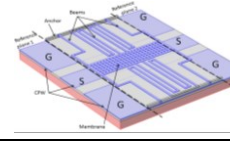
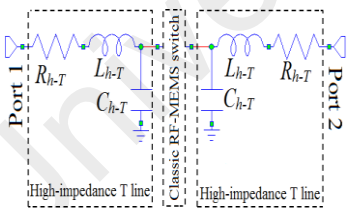
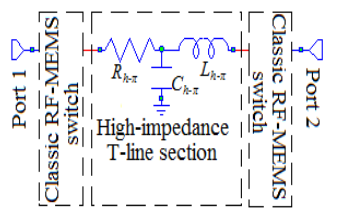
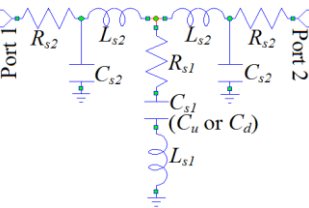
pull-in voltage of 3.06V, up-state and down-state capacitance of 87fF and 7.9pF, respectively. The residual stress and thermal effect on the pull-in voltage has been investigated. The results show that i) the pull-in voltage is increased with compressive stress and decreased with tensile stress; ii) the acceptable residual stress gradient range is $-16\text{MPa}/\mu\text{m}$ to $16\text{MPa}/\mu\text{m}$; iii) the maximum temperature change for the switch's robust operation should be kept within 16°C . For dynamic analysis, the simulated actuation time is $34\mu\text{s}\sim 19.5\mu\text{s}$ under bias voltage of $4\text{V}\sim 7\text{V}$ which agree with the calculated results. The releasing time has been discussed by employing the 1-D mass-spring-damper model; in order to get the shortest releasing time (around $143\mu\text{s}$), the critical damping condition of the membrane is preferred with damping coefficient of 8.81957^{-6} where the hole dimension on the membrane should be $7\mu\text{m}\times 7\mu\text{m}$ and distance between each two holes should be $12\mu\text{m}$. The pull voltages (namely pull-in voltage and pull-out voltage) under dielectric charging effect was investigated also where the pull voltages have been simulated in a time domain with bipolar triangular bias voltage. The parasitic charge density in the thin dielectric layer was estimated. In order to reduce the dielectric charging effect and obtain a long-lifetime design, a novel two-step bipolar rectangular waveform is proposed here. The RF performance of the optimized RF-MEMS switch was analyzed by AWR[®] EM simulator. The simulated impedance, return loss and insertion loss at switch-on state is $25.86-j20.58\Omega$, -7.879dB and -0.5487dB at 20GHz , respectively; and the simulated impedance, return loss and isolation at switch-off state is $25.86-j20.58\Omega$, -0.4557dB and -23.02dB at 20GHz , respectively. Here the switch-on-state return loss of -7.879dB is not satisfied with the design specification which can be improved by using T-match and π -match circuits. The switch's operation bandwidth was obtained as $17\text{GHz}\sim 22.8\text{GHz}$. The switch's power handling was estimated also with pull-down power of 284.17mW and hold-down power of 6.13mV

which shows the designed RF-MEMS switch is good to be used in the low-power applications.

In order to improve the up-state return loss of the optimized classic RF-MEMS switch, two improved low-loss RF-MEMS switches, namely T-match and π -match RF-MEMS switches have been introduced. Their RF performance (or S parameters) was simulated by AWR[®] EM simulator. Table 4.9 shows a comparison of the optimized classic RF-MEMS switch, T-match and π -match RF-MEMS switch, where their 3D structures, design areas, RF performance and equivalent circuits were included.

The last part of this chapter has introduced two different kinds of low-voltage control, low-loss, K-band MEMS phase shifters, which were a 3-bit MEMS switched-line phase shifter and a 3-bit DMTL phase shifter. Both of them have employed the previously (in Chapter 3) proposed novel capacitive RF-MEMS switch and CPW T line while the classic RF-MEMS switch has been modified a bit for DMTL phase shifter. Comparing the design results of these two different topologies MEMS phase shifter, each of them has their own merits and drawbacks. For MEMS switched-line phase shifter, it has very small phase error (0.2445°) and relatively small design area ($6 \times 4 \text{mm}^2$); however, its insertion loss is a bit high (2.447dB). For DMTL phase shifter, it has very small insertion loss (1.526dB); however, its phase error and design area is large, which are 6.032° and $12.8 \times 1.4 \text{mm}^2$, respectively. Each of them can be used in different purpose higher RF systems, such as phase-array antennas or reconfigurable antennas and further to be implemented in fixed satellite or mobile satellite (Monitoring systems).

Table 4.9: Comparisons of optimized T-match, π -match and classic RF-MEMS capacitive switches

| Parameter | | T-match RF-MEMS capacitive switch | Π -match RF-MEMS capacitive switch | Classic RF-MEMS capacitive switch |
|---|--------------------------------|--|--|---|
| 3D structure | |  |  |  |
| Whole area | | 626 μm \times 542 μm | 1002 μm \times 542 μm | 286 μm \times 542 μm |
| High-impedance T-line section | Width | 10 μm | 20 μm | - |
| | Length | 170 μm | 430 μm | - |
| | Impedance | 195 Ω | 89.5 Ω | - |
| S parameters @ 20GHz | S11 _{up} | -15.30dB | -26.51dB | -7.879dB |
| | S21 _{up} | -0.13dB | -0.1288dB | -0.5487dB |
| | S11 _{down} | -0.60dB | -0.7928dB | -0.4557dB |
| | S21 _{down} | -28.79dB | -20.54dB | -23.02dB |
| Improvement of S parameters | Δ S11 _{up} % | 94.19% | 236.46% | - |
| | Δ S21 _{up} % | 76.47% | 76.53% | - |
| | Δ S11 _{down} % | -31.01% | -73.97% | - |
| | Δ S21 _{down} % | 25.07% | -10.77% | - |
| | Total% | 164.72% | 228.24% | - |
| Equivalent modeling circuit | | Fig. a | Fig. b | Fig. c |
| Switch part | R_S | 0.9087 Ω | 2.43 Ω | 1.766 Ω |
| | L_S | 8.02pH | 21.8pH | 8.02pH |
| | C_S | $C_d=7.9\text{pF}$, $C_u=87\text{fF}$ | $C_d=7.9\text{pF}$, $C_u=87\text{fF}$ | $C_d=7.9\text{pF}$, $C_u=87\text{fF}$ |
| High-impedance part | R_h | 2.2 Ω | 0.4 Ω | - |
| | L_h | 278pH | 322pH | - |
| | C_h | 50fF | 0.05fF | - |
|  <p>Fig. a</p> | |  <p>Fig. b</p> | |  <p>Fig. c</p> |

CHAPTER 5: CONCLUSION AND FUTURE WORK

5.1 Conclusion

This thesis is about design, optimization, simulation and analyses and validation of low-voltage low-loss RF-MEMS switch.

The low-actuation voltage was achieved by employing eight folded beams. The folded beams were optimized using a novel multi-response optimization method, in order to obtain a low spring constant, low-actuation voltage, relatively short switching time, and robust structure design. The multi-response optimization method was developed by using Taguchi method and weighted principal component analysis. The simulated results show that the RF-MEMS switch's spring constant is 0.2378N/m; actuation voltage is 3.06V; switching time is 34 μ s~19.5 μ s with applied voltage of 4V~7V; and the maximum von Mises stress is 14.031MPa. Two inductive matching techniques, namely T-match and π -match circuits, have been used to improve the switch-on-state return loss and reduce the insertion loss of the low-voltage RF-MEMS switch. From the simulated result, it can be seen that i) for T-match RF-MEMS capacitive switch, by adding two optimized high-impedance T-line sections at both sides of the classic RF-MEMS switch with width of 10 μ m and length of 170 μ m, the up-state return loss, insertion loss and isolation can be improved by 94.19%, 76.47% and 25.07%, respectively, at 20GHz; ii) for π -match RF-EMMES capacitive switch, by inserting one optimized high-impedance T-line section between two classic RF-MEMS switches with width of 20 μ m and length of 430 μ m, the up-state return loss and insertion loss can be enhanced by 236.46% and 76.53%, respectively, at 20GHz.

In order to verify the function of the proposed RF-MEMS switch, two different MEMS phase shifters, namely MEMS switched-line phase shifter and DMTL phase

shifter, have been designed and simulated. The MEMS switched-line phase shifter is constructed by several T-match RF-MEMS switches and CPW lines on a high-resistivity silicon substrate. The simulated results show that i) its phase states are 0° , 45.03° , 88.09° , 136° , 180° , 225° , 268° , and 316° at 20GHz; ii) the average phase error is 0.5056° at 20GHz; iii) mean insertion loss is -1.51dB ; iv) both return loss and isolation is better than 11dB at a wideband frequency range of $18\text{GHz}\sim 22\text{GHz}$; v) and whole design area is $6\text{ mm} \times 4\text{ mm}$. The DMTL phase shifter is constructed by the modified classic RF-MEMS switches and one straight CPW line on a high-resistivity silicon substrate; its periodic space of each two switch is $312\mu\text{m}$. The simulated results show that i) its phase states are 0° , 46.68° , 93.54° , 140.1° , 186.5° , 2232.6° , 280.9° , and 328° at 20GHz; ii) average phase error is 6.032° at 20GHz and average 0° phase error is happened at 19.47GHz ; iii) average insertion loss is -1.526dB , the best is -0.6423dB , and the worst is -2.29dB at 20GHz; and iv) for all the phase shift conditions, the return loss is better than -10.05dB , the best is -28.86dB , and the average is -17.73dB at 20GHz.

A systematic design and optimization flow for developing a RF-MEMS capacitive switch was presented in this project. The main steps consist of i) identifying design specifications, ii) proposing a 3D structure design, iii) determining the switch's geometric dimensions, iv) simulating the RF-MEMS switch's electric, mechanic and RF properties, v) mechanical and electrical modeling, as well as vi) implementing the RF-MEMS switch into MEMS phase shifters to verify its functions. This methodology flow can be employed by other MEMS devices' development.

5.2 Thesis Contribution and Future Work

In this thesis, the most important original contributions can be summarized as following three points. i) The novel 3D structure design of the RF-MEMS switch can be used for low pull-in voltage and low-loss purpose which does not need very large design area comparing with other related designs. ii) The new optimization method for multiple responses which is based on Taguchi method and weighted principal component analysis is introduced for the first time. This method can be widely used in any other multi-response optimization condition which is not only easy to be understood, but also simple to be implemented. iii) The whole design methodology can be used for other MEMS devices' design or development.

The recommended future work of this project can be summarized into three aspects. One is about the experiment of the designed RF-MEMS switches which comprises their fabrication, measurement, and package. Since the limitation of the laboratory environment and equipment, the fabrication and measurement of the RF-MEMS switch is not included in this project's scope; however, it is an important content for MEMS devices' design. The proposed fabrication steps are presented in Figure 5.1, where a CMOS compatible process with surface micromachining technique is employed, aluminum is chosen for the material of CPW, beams and via, and SiO₂ is deposited for the coupling capacitor's thin dielectric layer. For the RF-MEMS switch's measurement, there are several parameters and their corresponding equipment which should be focused. The first one is membrane and beams' flatness which directly affect the switch's other properties; and an optical 3D profilometer can be used to measure this parameter which can avoid the touch effect on the suspended membrane and beams. The second one is the pull-in voltage and pull-out voltage of the RF-MEMS switch which can be obtained by measuring the switch-on and switch-off capacitance through Agilent B1505A. The third one is the switching time, namely switch-off time (or pull-down

time) and switch-on time (or release time) which can be measured by oscilloscope together with a RF source and a bias voltage source. The fourth one is the S parameters and impedance of the switch which can be obtained by using Agilent 8510C network analyzer. RF-MEMS capacitive switches are very small and sensitive to contaminants and humidity; therefore their packages are very important which make the devices have long lifetime and more reliable. Generally a hermetic dry nitrogen package for the RF-MEMS switch is needed. According to the interface circuit or the application, the requirement for the package should be different.

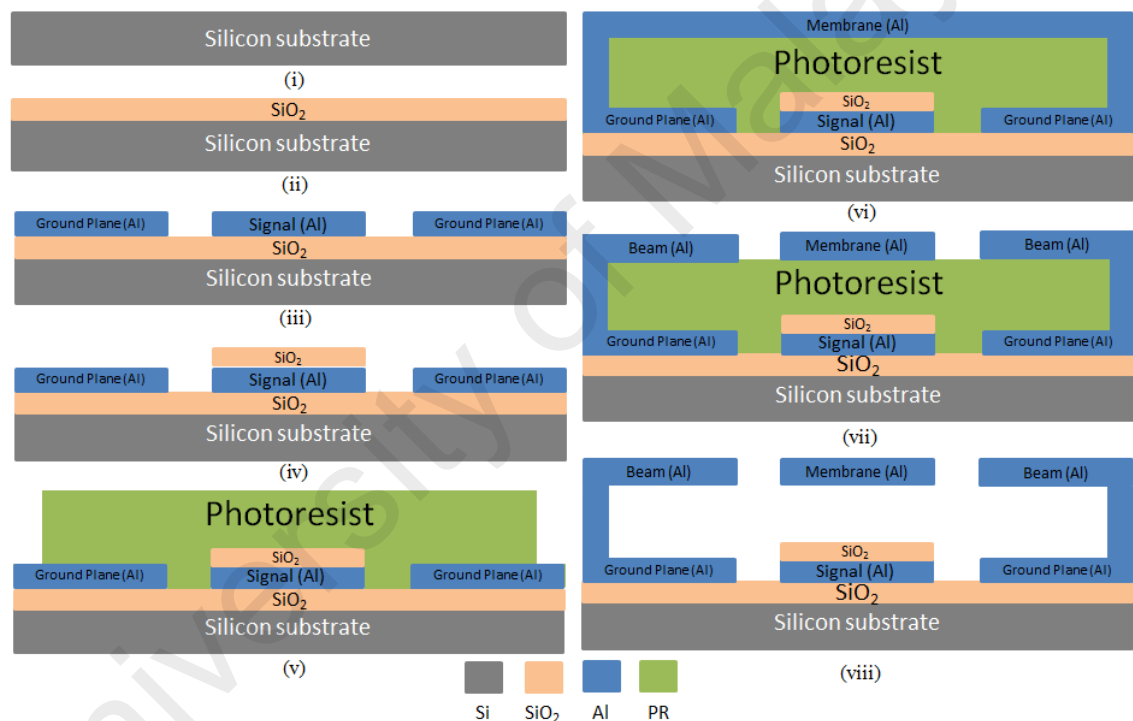


Figure 5.1: Fabrication steps of RF-MEMS capacitive switch

The second aspect of the recommended future work is about improving the power handling of the RF-MEMS switch. From Table 1.1, it can be seen that the RF-MEMS switch's power handling is much less than FET or p-i-n diode switches, which will limit it to be used in some communication circuits. Generally, increasing the thickness of the membrane or beams can improve the power handling capability; however, it will increase the pull-in voltage. So how to develop a RF-MEMS capacitive switch with

low-actuation voltage, low loss, and high power handling capability is a significant topic.

The third aspect of the recommended future work is about the application design of the RF-MEMS capacitive switch. The proposed low-voltage low-loss RF-MEMS switches can be used in different applications, such as MEMS phase shifters, switchable routing networks in RF system front-ends, reconfigurable antennas, tunable filters, MEMS-based voltage-controlled oscillators and digital capacitor banks. Except the MEMS phase shifters, many of these applications based on the RF-MEMS switch have not been developed or reported so far.

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