DEGRADATION ANALYSIS BASED ON DESIGN CONSIDERATIONS OF ADVANCED-PROCESS MOSFETS

AINUL FATIN BINTI MUHAMMAD ALIMIN

FACULTY OF ENGINEERING
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DEGRADATION ANALYSIS BASED ON DESIGN CONSIDERATIONS OF ADVANCED-PROCESS MOSFETS

ABSTRACT

The unceasing scaling of complementary metal-oxide-semiconductor (CMOS) technology has contributed to the steady increase in transistors performance for the past decades. However, it will also increase the power densities which will eventually leads to the increase in temperatures and other scaling effects, thus decrementing the lifetime reliability of transistors in the long-term usage. Reliability issues such as Negative Bias Temperature Instability (NBTI) and Hot Carrier Injection (HCI) impose challenges in the designing of CMOS devices as the device feature size enters the nanoscale regime. Therefore, there is a need to study the mechanism of the defects transformation process due to the variation of design considerations in the advanced-process CMOS devices in order to develop an effective aging aware design. This work presents a comprehensive simulation study on the effect of design considerations of the 32 nm advanced-process high-k p-channel metal-oxide-semiconductor field-effect transistor (pMOSFET) and n-channel laterally diffused metal-oxide-semiconductor (nLDMOS) with STI based structure on NBTI and HCI respectively. The design structures and analysis were simulated using Synopsis Sentaurus Technology Computer-Aided Design (TCAD) simulator based on standard CMOS manufacturing trends. This study composed of two parts. The first part focuses on the NBTI reliability issue where NBTI mechanism and defects were explored through varied design parameters of extensively wide range of values. NBTI simulation measurement in this work follows the on-the-fly (OTF) method to capture the mechanisms of the fast and slow traps. NBTI study in this work elaborates on the dependency of the threshold voltage (V_{th}) degradation on stress oxide field, stress temperature as well as investigation on the devices' Arrhenius plot. The second part of this study addresses the HCI reliability issue in nLDMOS devices. The design parameters

were varied in order to investigate the influence of these parameters on HCI. The nLDMOS device degradation due to HCI was simulated using stress-measure testing technique. The electrical analysis performed displays detailed insight into the impact ionization rate and electric field distribution apart from the on-resistance (R_{on}) and I-V characterization. From the NBTI study, it is found that the V_{th} degradation analysis at 1ks and 375K shows that changing the SiO_2 interfacial layer thickness affects the V_{th} degradation by 96.16% more than changing the HfO_2 thickness and by 80.67% more than changing the metal gate thickness. It is also found that the NBTI effect depends on process design considerations, where it was observed that higher boron dose and high metal work function may lead to higher V_{th} degradation. However, the halo doping concentration in the advanced 32 nm structure has an insignificant effect on NBTI. The HCI study shows that the drain current for device with 100º STI angle is reduced by 58.78% compared to device with 45º STI angle. Larger STI angle shows higher HCI degradation while larger STI depth as well as larger gate oxide thickness is observed to cause lower degradation. Process design wise, it is found that higher p-substrate doping concentration exhibit higher degradation and the HCI degradation is not significantly affected by the S/D implantation dose.

Keywords: NBTI, HCI, reliability, degradation, defects

ANALISA KEMEROSOTAN BERDASARKAN PERTIMBANGAN REKA BENTUK BAGI MOSFET DENGAN PROSES CANGGIH

ABSTRAK

Penskalaan teknologi semikonduktor oksida logam pelengkap (CMOS) yang berterusan telah menghasilkan peningkatan prestasi transistor yang mantap sejak dekad yang lalu. Bagaimanapun, ia juga akan meningkatkan ketumpatan kuasa yang pada akhirnya menyebabkan peningkatan suhu dan kesan penskalaan yang lain, lalu memudaratkan jangka panjang kebolehpercayaan hayat transistor. Isu kebolehpercayaan seperti ketidakstabilan kepincangan negatif suhu (NBTI) dan suntikan pembawa haba (HCI) memberikan cabaran dalam mereka bentuk peranti CMOS apabila ciri saiz peranti memasuki regim skala nano. Oleh itu, mempelajari mekanisme transformasi kecacatan disebabkan oleh variasi dalam pertimbangan reka bentuk peranti CMOS dengan proses canggih telah menjadi satu keperluan bagi membangunkan sebuah rekaan yang menitikberatkan jangka hayat yang berkesan. Kerja penyelidikan ini membentangkan kajian simulasi yang menyeluruh tentang kesan pertimbangan reka bentuk bagi transistor kesan medan semikonduktor oksida logam dengan proses canggih berteknologi 32 nm dengan saluran-p jenis k tinggi (pMOSFET) ke atas NBTI dan kesan struktur berasaskan STI semikonduktor oksida logam penyebaran sisi dengan saluran-n (nLDMOS) ke atas HCI. Rekaan struktur dan analisa telah disimulasi menggunakan simulator Synopsys Sentaurus Rekaan Teknologi Berbantukan Komputer (TCAD) berdasarkan trend piawaian pembuatan CMOS. Kerja penyelidikan ini mengandungi dua bahagian. Bahagian pertama tertumpu kepada isu kebolehpercayaan NBTI di mana mekanisme NBTI dan kecacatan telah diterokai dengan memvariasikan parameter reka bentuk dalam nilai julat yang besar. Simulasi NBTI dalam kerja penyelidikan ini menggunakan ukuran mengikut kaedah on-the-fly (OTF) bagi menangkap mekanisme perangkap laju dan perangkap perlahan. Kajian NBTI dalam kerja penyelidikan ini mengulas lanjut tentang

pergantungan kemerosotan voltan ambang (V_{th}) ke atas tekanan medan oksida, tekanan suhu dan siasatan juga dilakukan ke atas plot Arrhenius peranti. Bahagian kedua kerja penyelidikan ini menerangkan tentang isu kebolehpercayaan HCI dalam peranti nLDMOS. Parameter-parameter reka bentuk telah divariasikan bagi menyiasat pengaruh parameter-parameter ini ke atas HCI. Simulasi degradasi peranti nLDMOS disebabkan oleh HCI telah dilakukan mengikut teknik ujian tekanan-ukur. Analisa elektrik yang dilakukan memaparkan gambaran terperinci tentang kadar hentaman pengionan dan taburan medan elektrik selain rintangan hidup (R_{on}) dan pencirian I-V. Daripada kajian NBTI, analisa kemerosotan V_{th} pada 1ks dan 375K menunjukkan bahawa perubahan ketebalan lapisan antara muka SiO_2 memberi kesan ke atas kemerosotan V_{th} sebanyak 96.16% lebih daripada perubahan ketebalan HfO_2 dan 80.67% lebih daripada perubahan ketebalan pagar logam. Ia juga didapati bahawa kesan NBTI menunjukkan kebergantungan ke atas pertimbangan reka bentuk proses, dimana dos boron dan fungsi kerja logam yang tinggi boleh menjurus kepada kemerosotan V_{th} yang tinggi. Bagaimanapun, kepekatan campuran halo di dalam struktur canggih 32 nm menunjukkan kesan yang tidak penting ke atas NBTI. Kajian HCI menunjukkan bahawa aliran arus bagi peranti dengan sudut STI 100º berkurang sebanyak 58.78% berbanding peranti dengan sudut STI 45º. Sudut STI yang lebih besar menunjukkan kemerosotan HCI yang tinggi manakala kedalaman STI dan juga ketebalan oksida pagar yang besar dilihat telah menyebabkan kemerosotan yang lebih rendah. Dari segi reka bentuk proses, ia telah didapati bahawa kepekatan campuran substrat-p menunjukkan kemerosotan yang tinggi dan kemerosotan HCI tidak dijejaskan oleh dos implan S/D.

Kata kunci: NBTI, HCI, kebolehpercayaan, kemerosotan, kecacatan

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E_{ox}	:	Oxide field
I_d	:	Drain current
N_{it}	:	Interface trap density
T	:	Temperature
V_d	:	Drain voltage
V_g	:	Gate voltage
$V_{gstress}$	:	Stress gate voltage
V_{th}	:	Threshold voltage
ΔV_{th}	:	Threshold voltage shift
R_{on}	:	On-resistance
ΔR_{on}	:	On-resistance shift
g_m	:	Transconductance
L_g	:	Gate length
L_{ch}	:	Channel length
L_a	:	Accumulation length
I_{dsat}	:	Saturation current
ΔI_{dsat}	:	Saturation current shift
E_a	:	Activation energy
V_{gop_max}	:	Maximum operating gate voltage
t_{sti}	:	STI region depth
L_{sti}	:	STI region length

AlN	:	Aluminium Nitride
EOT	:	Equivalent Oxide Thickness
HCI	:	Hot Carrier Injection
HDD	:	Highly Doped Drain
HfO_2	:	Hafnium Oxide
IL	:	Interfacial Layer
MOSFET	:	Metal Oxide Semiconductor Field Effect Transistor
NBTI	:	Negative Bias Temperature Instability
OTF	:	On-the-fly
RD	:	Reaction Diffusion
CMOS	:	Complementary Metal Oxide Semiconductor
HKMG	:	High-k/Metal gate
LDMOS	:	Laterally Diffused Metal Oxide Semiconductor
STI	:	Shallow Trench Isolation
S/D	:	Source/Drain
WF	:	Workfunction
RT	:	Room Temperature
MG	:	Metal Gate
SiO_2	:	Silicon Dioxide
SiGe	:	Silicon-Germanium

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CHAPTER 1: INTRODUCTION

1.1 Background of study

For the last decades, up till now, the microelectronics industry has been enormously benefited from the scaling down of metal-oxide-semiconductor field effect transistor (MOSFET) devices. The path of this miniaturization thus far follows Gordon Moore's prediction, from 1965 where he predicted that the density of transistors on a chip would double for every 18 months (Moore, 1965) and this prediction has been adopted by existing key player of the industry in order to scaled down their most advanced technologies (Loughran, 2017; Pressman, 2017; Venkataraman, Venkataraman, Dew, & Dew, 2017). The shrinking of transistors has resulted in increased functionality as well as reducing the manufacturing cost of broad variety of integrated circuits and systems. Transistor scaling has also contributed to some other primary advantages such as boosting the speed of data transfer, improving computer processing power and enable multiple tasks to be accomplished simultaneously. Nonetheless, to maintain good performance whilst downsizing MOSFET devices has become increasingly challenging over time, unavoidably leading to the emerging of reliability concerns (Afacan, Yelten, & Dündar, 2017; Ndiaye et al., 2017; Prasad, Ramey, & Jiang, 2017) such as Negative Bias Temperature Instability (NBTI), Hot Carrier Injection (HCI), Time Dependent Dielectric Breakdown (TDDB) and many more. These reliability challenges will substantially affect the product cost and device performance requirements as designers will tend to under/overestimate the design margin if there are no appropriate reliability-design solutions (Blish et al., 2003; ISSI, 2016; Pollek & Wu, 2002).

As MOSFET devices enter the sub-micrometer regime, the gate oxide thickness is rapidly driven to below 2 nm (Taur et al., 1997), which consequently cause direct tunneling leakage current to rise exponentially as the gate oxide thickness is reduced (Lo, Buchanan, Taur, & Wang, 1997). In order to mitigate this leakage problem, materials

with higher dielectric constant (k) are introduced. Material having larger dielectric constant allows thicker film to be used while retaining the same gate capacitance (Hall, Buiu, Mitrovic, Lu, & Davey, 2007; Thompson, 1998; Wilk, Wallace, & Anthony, 2001). In turn, though the usage of high-k helps in reducing the leakage, its implementation encounters various difficulties which include mobility deterioration and threshold voltage instability due to the quality of interfacial oxide and charge trapping. This problem is known as Negative Bias Temperature Instability (NBTI) where the phenomenon will cause an increase in the threshold voltage (V_{th}) and decrease in transconductance (g_m) and drain current (I_d). NBTI degradation mechanism is widely known to engage with generation of interface trap (N_{it}) at the Si/SiO_2 interface and captures of hole at the oxide *E*' centers in high-k under negative bias gate voltage stress (Gao, Boo, Teo, & Ang, 2011; Teo, Ang, & Ng, 2010). Both of the traps, within Si/SiO_2 interfacial oxide layer and trap centers of high-k oxide may contribute to the stress-induced threshold voltage degradation, ΔV_{th} (Neugroschel et al., 2006). These defect sites escalate the threshold voltage, initiate parasitic capacitances or degrade channel mobility of the MOSFETs and deteriorate the device performance. On the whole, degradation of the performance metrics indicates shorter lifetime of the device and will therefore impose a challenge for the IC manufacturers.

Hot Carrier Injection (HCI) is another reliability concern involving defects creation at the Si/SiO_2 interface in the oxide bulk as well as near the drain edge (Chen et al., 2000). Similar to NBTI, the trap causes the device performance metrics to shift and consequently worsen the performance. Damage created near the drain edge of the MOSFET is due to high electric field in the drain side which lead to carrier heating. Hot carrier resulted in impact ionization, a process where one charge carrier acquire energy from the losing of energy by another energetic charge carrier and will subsequently contribute to degradation. Laterally diffused metal-oxide-semiconductor (LDMOS) transistors, which

are widely used in RF power applications present unique features where these features will substantially influence the hot-carrier phenomena (Chauhan et al., 2006). Due to lower effective mass of electrons compared to holes, HCI is found to be more significant in n-type MOSFETs (Song, MacWilliams, & Woo, 1997) and thus, the channel electric field can cause higher energy gain in the n-type devices.

Aggressive scaling of device feature sizes in CMOS semiconductor technology have been continuing to improve devices performance. However, the outbreak of problems due to long-term device failures or lifetime reliability have been accelerated due to CMOS scaling. Defects with the same size which are safe for former technologies may cause reliability concerns for advanced technologies due to the device scaling (White, 2010). For that reason, this study is carried out to find the best alternatives and potential solutions to overcome the challenges of device reliability. This dissertation highlights the device reliability issues of recent CMOS technology by addressing the impact of design parameter selection on device reliability performance using a numerical simulation approach based on the standard manufacturing trends. It is necessary to have a solid understanding of the phenomena that occurs in nanoscale transistors since it not only provides useful interpretation of the previous results but also the future possibilities and limitations of the device scaling.

1.2 Problem statement

Though the scaling down of CMOS devices have granted many advantages, there are also some drawbacks, notably in the reliability of the device. Aging due to NBTI and HCI is the main cause of performance failure in large scale logic circuits. Designers are driven to make use of an overly conservative design method which is known as guard-banding when there is no reliability modeling or simulation available. The guard-banding method will consequently degrade chip performance as well as risking early chip failures in the field. Designers can avoid problems that previously may only have been found during

chip burn-in by doing a more complete reliability assessment. JEDEC has produced standards for reliability test to meet the needs of microelectronics industry, where the measurements specified can be viewed as a root of device characterization as well as benchmark of the transistor manufacturing process. JEDEC states that at least 10% change in the device characteristics merits to the defects induced by reliability issues such as NBTI and HCI (JEDEC, 2001, 2004).

The technology scaling to date has reached the critical stage where any decrease in dimension may severely affect the transistor reliability performance (Lee et al., 2013; Ma et al., 2014; Mishra et al., 2017; Ramey, Prasad, & Rahman, 2018). Assessing reliability performance is utterly important in order to predict the lifetime of a device which enable consumer to obtain reliable end-product. However, comprehensive reliability modeling for advanced-process technology devices has not fully matured. In order to attain a comprehensive reliability modeling, deep understanding of defect characteristics and other factors which lead to device reliability degradation is certainly crucial.

Many published works are looking into the modeling of the mechanism and kinetics of charges that are responsible for degradation (Bina et al., 2014; Huard, 2010; Liao et al., 2017; Mahapatra et al., 2005; Mahapatra & Parihar, 2018; McMahon, Mamy-Randriamihaja, Vaidyanathan, Nigam, & Pimparkar, 2015; Moens & Groeseneken, 2004) and also significant research on the measurement technique of device degradation as well as device reliability performance (Boo & Ang, 2012; Du, Ang, Teo, & Hu, 2009; Moras et al., 2015; Reggiani et al., 2013; Ren et al., 2014; Wong, Ng, & Sim, 2016). The increasing number of publications related to reliability characteristics of MOSFET devices indicates increased interest to this area. However, it appears from the aforementioned investigations that most consideration has been paid to the modeling and measurement method of the device degradation. How the geometric and process design considerations affect the reliability of the device has not been thoroughly investigated.

Understanding the exact mechanism of the defects transformation process due to the variation of geometric and process design considerations in the advanced-process MOSFET devices is another aspect that need to be explored.

1.3 Aims and objectives

The aim of this project is to investigate the reliability performance of advanced-process MOSFETs based on geometric and process design considerations. The outcome of this study enables researchers to quantify defect characteristics and predict the lifetime of MOSFETs in order to assess the reliability of a device. This study could also help device designers to contemplate the best geometrical and process design considerations in order to minimize aging-related degradations and gate leakages in subsequent products. Avoiding a problem earlier is uttermost important, considering the cost of test-chip manufacturing. The ability to perceive reliability of devices is remarkably essential for integrated device manufacturers and foundries in order to allow them to achieve reliable yield and better end-products. The research objectives can be divided as follows:

1. To investigate the influence of geometrical and process design considerations on Negative Bias Temperature Instability (NBTI) of advanced-process high-k pMOSFET devices such that to cause more than 10% of threshold voltage degradation.
2. To analyse the discrete contribution of generated defects and as-grown defects on the performance of advanced-process high-k pMOSFET devices such that at least 10% of performance degradation can be observed for stress time less than 1ms and stress time more than 1ms for as-grown and generated defects respectively.
3. To investigate the influence of geometrical and process design considerations on Hot Carrier Injection (HCI) of STI-based laterally diffused MOSFET

(LDMOS) devices such that to cause more than 10% of on-resistance and saturation current degradation.

1.4 Scope of work

This study will look into reliability concerns in the advanced-process MOSFET technology, specifically the NBTI and HCI issues. The Technology Computer-Aided Design (TCAD) Synopsys Sentaurus device simulator will be used to its maximum capability in studying the characterization of advanced high-k MOSFET as well as STI-based LDMOS devices. Advanced physical models will be implemented in the TCAD simulator in order to imitate the real existing device structure, with various test conditions. The design consideration focuses on the geometrical and process design parameters, which follows the ITRS standards for the development of advanced high-k MOSFETs and STI-based LDMOS. Figure 1.1 presents the overview of the research methodology in this work. The devices under test are advanced-process high-k metal gate p-MOSFET for NBTI study and n-type STI-based LDMOS for HCI study. Critical device attributes such as threshold voltages degradation, saturation current degradation, on-resistance degradation and many more were analyzed to provide a comprehensive assessment of the device reliability performance. Current density distribution, electric field distribution as well as impact ionization rate using 2D Sentaurus techplot would provide a clear understanding of all the parameters dependency to devices' behavior.

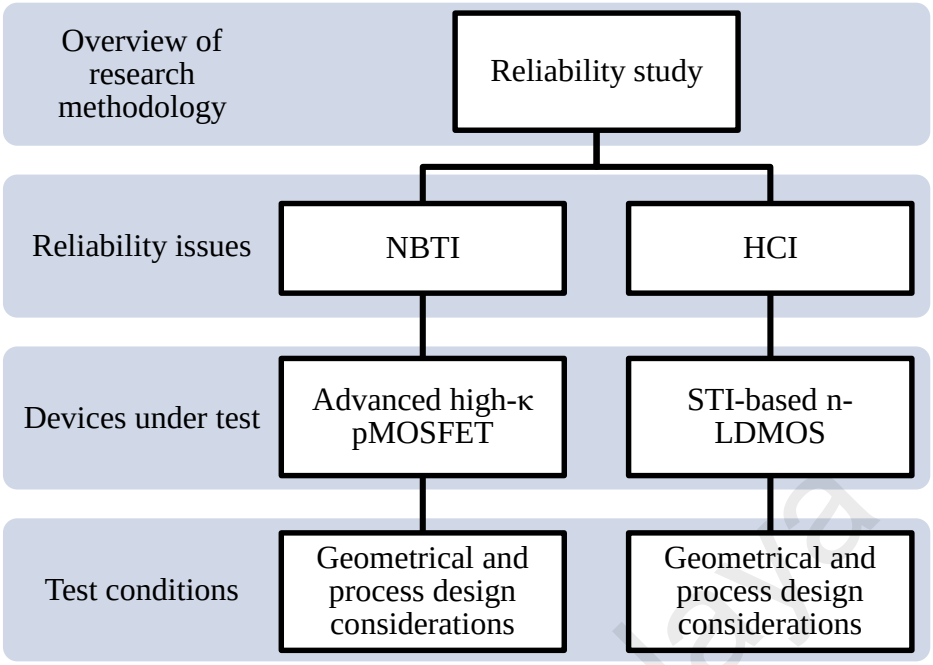

Figure 1.1 Overview of the methodology approach in this work.

1.5 Dissertation outline

The structure of this thesis is as follows:

Chapter 2 - Literature review section presents in depth literature study of the structure of advanced high-κ MOSFET and STI-based LDMOS as well as the scaling of MOS devices. The reliability issues in CMOS, particularly aging effects of NBTI and HCI are described in detail which include the origin and theory of the mechanisms involved in these phenomena. The reviews include earlier works from both simulation and experimental studies for advanced high-k MOSFET and STI-based LDMOS under geometrical and process design considerations.

Chapter 3 – Research methodology section comprises of the devices and simulation conditions in obtaining the reliability performance of devices under test in this study. This section begins with the explanation of the overall project methodology, followed by detailed description of each methodology flow which include simulation process flow of the device and illustration of the device design structures, specific investigated design parameters, simulation conditions applied and the advanced physical model implemented

in the TCAD. The measurement of the reliability performance carried out in this research are also further explained.

Chapter 4 – Results and discussion section features the findings acquired from this work. The different structures applied in each MOS technology had been demonstrated based on the standard manufacturing trends. The effect of geometrical and process design considerations of high-k MOSFET on NBTI and STI-based LDMOS on HCI are discussed. This section also shows the 2D view structure of devices during operation with respect to electrical parameters extracted including current distribution and the impact ionization rate. Selected results were validated with the experimental data reported from previous research. A table of summary based on geometric and process design consideration for general overview of NBTI and HCI impact is presented.

Chapter 5 – Conclusion and future works section summarizes this whole project and recommends possible future works. In this section, the work presented in this dissertation is concluded. The aspects of future research are discussed and a few recommendations were made.

CHAPTER 2: LITERATURE REVIEW

2.1 Introduction

This chapter describes in details on the reliability issues arise from the aggressive scaling of MOSFET devices over the years. Fundamental aspect of failure and degradation mechanism in semiconductor devices were explained thoroughly. Several findings from outstanding research were reviewed prior to simulation analysis in order to give clear understanding on the physical mechanism of device degradation and possible impact on the device reliability performance. The reviews take into consideration both experimental and simulation work based on device's geometrical and process design.

2.2 Challenges in MOS scaling

The scaling down of MOS devices does not only contributes to the improvement of devices' performance, but also possess undesirable drawback (Kuhn, 2011; McPherson, 2006; Russ, 2008). Some of the drawback includes increase in leakage current, threshold voltage shift, difficulty to further increase on-current and the most importantly, threatening the reliability of a device over time. The overview of scaling issues is presented in Figure 2.1. As the gate length enters nanometer regime, starting from the critical dimension of 130 nm technology generation and below, further scaling of the MOSFET devices are getting much more complicated to deal with. Figure 2.2 shows the comparison of reliability performance of two different process nodes. The transport property of Si started to meet its limitation at such dimensions and therefore, resulted in device performance degradation and eventually limits the device lifetime. This work will essentially focus on the reliability of device due to scaling.

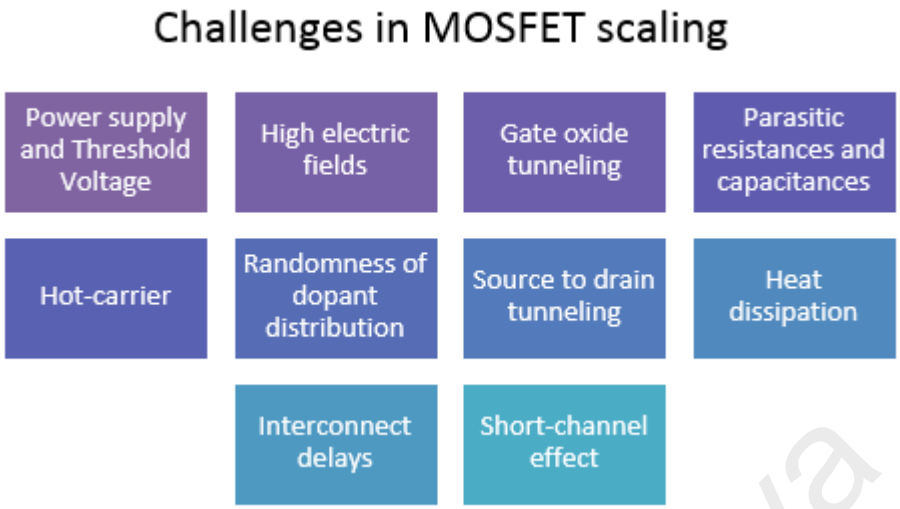

Figure 2.1 Overview of issues in MOSFET scaling (Chopra & Subramaniam, 2015).

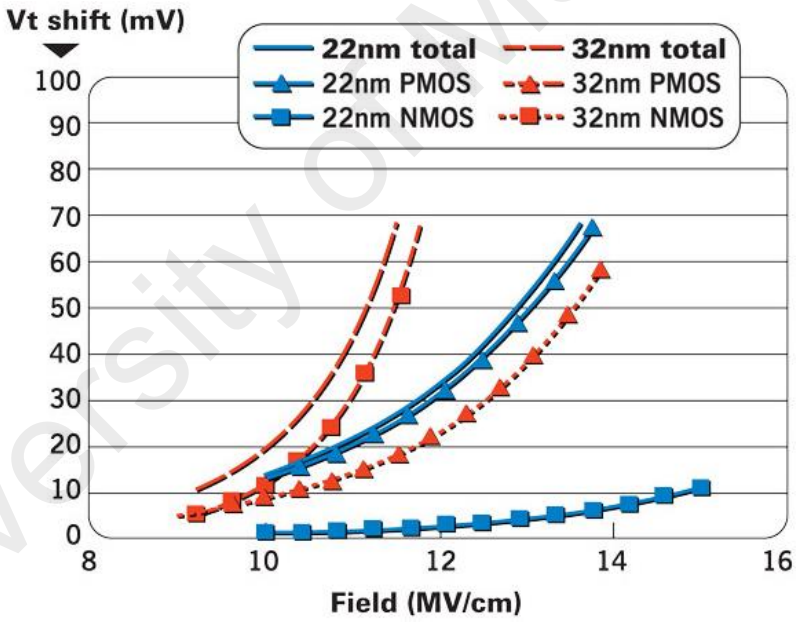

Figure 2.2 Reliability of PMOS devices are shown to be worst with scaling (Ramey et al., 2013).

2.3 CMOS reliability

Reliability from the semiconductor point of view is manifests as the ability of a device to comply with its electrical specifications under specified conditions and over a specified time span. Reliability issues are becoming even more significant for nanoscale MOS devices due to the small device size, high transistor densities as well as high-speed

performances. Reliability issues of MOS devices in sub-micrometer regime can be divided into two types, which are the spatial effects and temporal effects (Maricau & Gielen, 2013), as shown in Figure 2.3. Spatial effects are fixed in time and the defects are obtained during production process. There are two types of defects causing spatial effects, namely the random defects such as line edge roughness and random dopant fluctuation and the systematic defects such as gradient effect. Temporal effects differ from the spatial effects as it varies with time and the defects depend on operating conditions such as operating voltage and temperature. The damage caused by this effect can be permanent or temporary. Temporal effects can be divided into aging defects which include the NBTI and HCI as well as transient defects such as single event upsets and electromagnetic interference (Maricau & Gielen, 2013). In this study, the focus will be particularly on the aging effects of MOS devices.

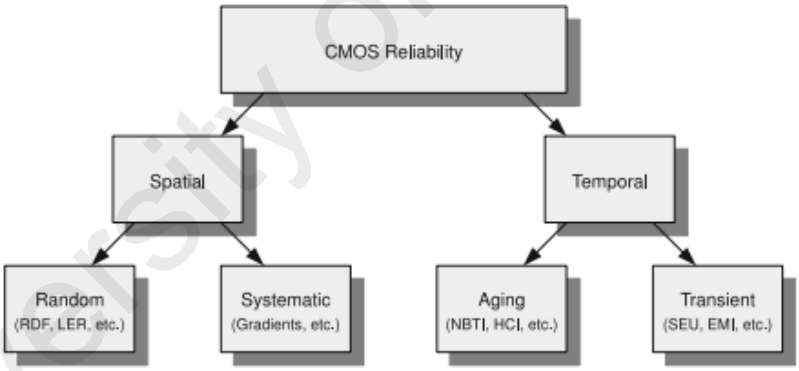

Figure 2.3 The overview of the type of MOS reliability issues (Maricau & Gielen, 2013).

2.4 Aging Effects

The aging phenomena has been studied by researchers since decades ago. Not until in the nineties where this effect has becoming more and more critical as the device dimensions are aggressively scaled down as well as the further increase in electric field. Entering 21st century, further scaling by introducing new materials has contributed to

additional failure mechanisms and consequently, making the reliability and lifetime of a device to be much more threaten. This section reviews two of the most significant aging phenomena observed in nanoscaled MOS technologies, namely the negative bias temperature instability (NBTI) and hot carrier injection (HCI).

2.4.1 Negative Bias Temperature Instability (NBTI)

Negative Bias Temperature Instability (NBTI) is a severe reliability concern in both analog and digital CMOS technologies (Abadeer & Ellis, 2003; Agostinelli et al., 2006; Chen, Zhou, Tedja, Hui, & Oates, 2001; Krishnan et al., 2003; Reddy et al., 2005). NBTI is a phenomenon where the threshold voltage deviates over time, followed by the reduction in drain current as well as reduction in transconductance of a device. This will eventually result in the degradation of circuit performance and deteriorates lifetime. The NBTI degradation are triggered by the application of high negative voltage or elevated temperature on the device, where the effect will be aggravated by the combination of both. The typical range of stress oxide electric field applied is from -8MV/cm to -12MV/cm (Ang, Teo, Ho, & Ng, 2011; Boo & Ang, 2012; Gao, Ang, Boo, & Teo, 2011; Gao, Boo, et al., 2011) and stress temperature ranging from room temperature to 220 °C (Ang et al., 2011; Boo & Ang, 2012; Gao, Ang, et al., 2011; Gao, Boo, et al., 2011). The impact of NBTI is much more dominant in p-type MOSFETs compared to the n-type MOSFETs since PMOS essentially always operate with negative gate-to-source voltage. NMOS is less significantly affected due to the fact that the fixed charges and interface states are of different polarity and therefore will cancel each other.

Conventionally, the NBTI degradation is assessed by the stress-measure-stress technique. Firstly, the initial device characteristics before exposing it to stress are measured. Then, the sample is stressed under constant negative bias and high temperature at a preset stress time before it is let to cool down to room temperature. The NBTI degradation is obtained by comparing the performance of a device after stress to the initial

performance. Critical device parameters include the threshold voltage, drain current, subthreshold slope, transconductance and mobility. The stress time is typically extend from 10^3 to 10^5 s. Figure 2.4 illustrates the NBTI phenomena occurring in PMOS devices.

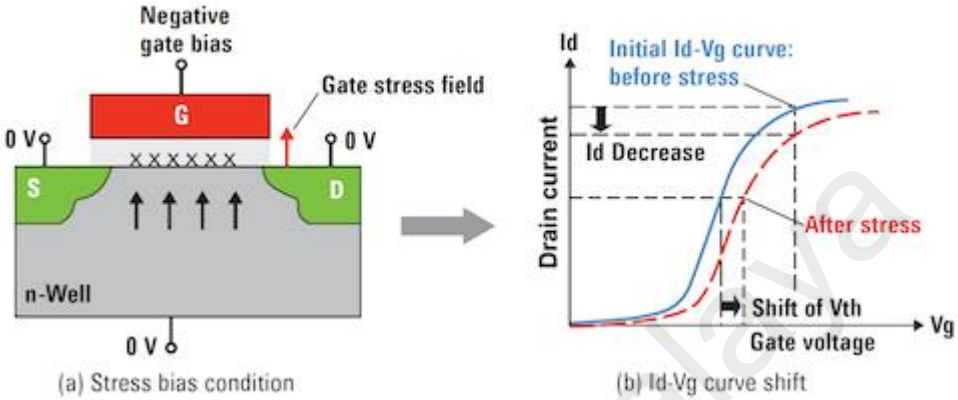

Figure 2.4 Negative bias temperature instability in PMOS devices (Nishimura, 2013).

It is universally accepted that the NBTI threshold voltage shift is resulted by the generation of interface traps caused by the dissociation of Si-H bonds along the silicon-oxide interface. Large stress bias as well as stress temperature resulted in the breaking of Si-H bond, creating dangling bond of silicon, namely interface trap and H^+. The interface trap cannot be recovered over a reasonable operation time. In addition, other than the interface traps, the as-grown traps located in the bulk of the dielectric also contributed to the threshold voltage shift. This as-grown trap captures hole which tunnels from the channel under the influence of gate electric field and can be emptied when the stress voltage is removed. The threshold voltage degradation is therefore can be recovered over time.

2.4.2 Hot Carrier Injection (HCI)

Hot carrier injection (HCI) in CMOS devices is a degradation mechanism associated with high energy carriers, commonly known as hot carriers accelerated by the high electric field in the channel before they are injected and trapped in the gate oxide. The

high channel electric field is obtained as a result from the extreme shrinking of device size. These trapped charges cause the generation of interface states and give rise to the shift in device parameters such as threshold voltage, transconductance, as well as linear and saturation drain current. HCI degradation is a prominent issue in n-type MOSFET devices (Lunenborg, De Graaff, Mouthaan, & Verweij, 1996; Parthasarathy et al., 2006) as holes are much heavier than electrons (Hu et al., 1985). HCI was first became a concern in the mid-eighties due to constant scaling of device dimensions without corresponding reduction of operating voltage (Hu et al., 1985; Takeda, Suzuki, & Hagiwara, 1983; Tam, Ko, & Hu, 1984). After a decade, this problem was mitigated by scaling down the operating voltage to reduce power consumption and by introducing graded drain junctions. For that reason, HCI became less of an issue. However, the scaling of operating voltage is slowing down over years due to the non-scalability of the subthreshold slope (Bravaix et al., 2009; Maricau, De Wit, & Gielen, 2008; Wang et al., 2007), hence making the HCI degradation to be a significant reliability issue once again. High operating voltage causes high electric field which triggers the hot carrier injection and trapping. This effect is much more aggravated in power devices such as LDMOS since they typically operate under high drain bias for maximum output power (Osburn & Huff, 2002).

2.5 Degradation mechanisms

2.5.1 Negative Bias Temperature Instability

The explanation on the physical mechanism behind NBTI has been proposed by many researchers through various NBTI model. Among the NBTI model proposed, the most attention is gained by Alam (Alam, 2003) which came up with the reaction-diffusion (RD) theory. In addition, another most prevalent report is by Huard (Huard, 2010) which suggests that there are two independent components coexist (recoverable and permanent component) causing NBTI degradation and theory by Grasser et al. (Grasser et al., 2009), suggesting NBTI mechanism involves two stage processes, where the first stage describes

hole-capture process into the deep near-interfacial states and the second stage involves the creation of permanent defects. Another well-known NBTI model is by Z. Ji et al. (Ji, Lin, Zhang, Kaczer, & Groeseneken, 2010) which demonstrates the NBTI kinetics by combining the effect of as-grown defects and generated defects (AG model) measured under the worst case condition.

2.5.1.1 Reaction-Diffusion (RD) model

The Reaction-Diffusion model, or universally known as RD model is described as the generation of interface trap governed by hydrogen diffusion through the gate oxide. RD model was first introduced in 1977, by Jeppson and Svensson (Jeppson & Svensson, 1977) and further developed by several other research group (Alam, 2003; Blat, Nicollian, & Poindexter, 1991; Ogawa & Shiono, 1995). This model is associated with stress time dependence of NBTI degradation under broad range of stress voltages and temperatures. The NBTI degradation trend is consistent with power-law, with a power factor depending on the type of hydrogen involved during the degradation process ranging from 0.16 to 0.3 (Chakravarthi, Krishnan, Reddy, Machala, & Krishnan, 2004). RD model, as suggested by its name consists of reaction and diffusion process. Reaction process is initiated by the electrochemical reaction at the Si/SiO_2 interface when a gate voltage is applied, causing the dissociation of the passivated Si-H bond. Interface state is created and hydrogenous species is released as a result from the bond breakage. Later, the hydrogenous species disseminate away from the Si/SiO_2 interface, where the process is known as the diffusion process. The generation of interface traps limit depends on the diffusion of the hydrogenous species. The interface reaction of the RD model is described by the kinetic equation below (Stathis & Zafar, 2006):

$$\frac{dN_{it}}{dt} = k_f(N_0 - N_{it}) - k_r N_{it}[N_{H*}]^{\frac{1}{a}} \qquad 2.1$$

where N_0 is the initial number of unbroken passivated Si-H bonds, N_{it} is the number of generated interface traps and N_{H*} is the number of hydrogenous species at the interface.

a denotes the reaction order where $a = 1$ is for atomic hydrogen and $a = 2$ is for molecular hydrogen. k_f represents the forward dissociation rate constant whereas k_r is the constant value for repassivation rate. These constant values are oxide field and temperature dependence. The hydrogen density at the interface dominate the forward and backward reaction. For that reason, the degradation mechanism in RD model is characterized by the transport mechanism of the hydrogen species.

The hydrogen species which disseminated away from the interface will recombine with atomic hydrogen to create molecular hydrogen. Different diffusing species is observed to have different NBTI time dependency, where the time dependent for atomic hydrogen model is $t^{0.25}$ and time dependent for molecular hydrogen is $t^{0.165}$ (Alam, 2003; Chakravarthi et al., 2004). Figure 2.5 below illustrates the overall RD model degradation mechanism due to NBTI.

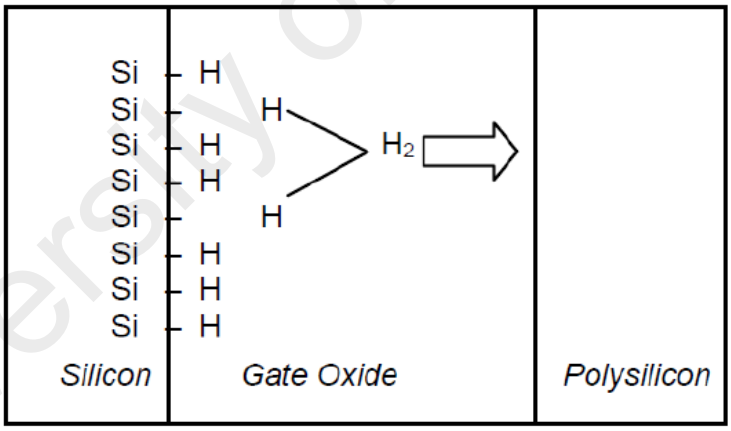

Figure 2.5 RD model schematic description to portray the generation of interface traps as a result of NBTI (Mahapatra, Bharath Kumar, & Alam, 2003).

Scaling down the oxide thickness have resulted in reduction of the distance between polysilicon gate and Si/SiO_2 interface, thus making the hydrogen diffuse much faster and consequently worsen the NBTI degradation (Mahapatra et al., 2003). It is apparent from the illustration in Figure 2.5 that shrinking of gate oxide to meet the current CMOS

technology demand would significantly increase the interface trap concentration and therefore, increasing NBTI.

2.5.1.2 Two-stage model

The two-stage NBTI model is associated with two degradation components which consists of recoverable component and permanent component (Ang, Gu, Tung, Boo, & Gao, 2014; Grasser et al., 2007; Huard, Denais, & Parthasarathy, 2006). Recoverable component is a component that can return to its original condition after stress is applied and are usually related to trapped holes. Permanent defect, on the other hand is a fixed or slowly recoverable component of NBTI which is associated with the interface trap (Huard & Denais, 2004; Huard et al., 2007). The two-stage NBTI model involves two stage processes, where the first stage describes hole-capture process into the deep near-interfacial states and the second stage involves the creation of permanent defects (Grasser et al., 2009). This model is associated with the kinetics of four states, namely S_1, S_2, S_3 and S_4 as illustrated in Figure 2.6. State S_1 consists of Si-Si dimer precursor which is generally known as the as-grown defect. State S_2 and S_3 consist of positively charged E' center and neutral E' center respectively. State S_4 consists of fixed positive charge and interface trap, P_b which is known to be permanent defect. In between the states, there are transitions from one state to another. Transition between states S_1 to S_2 occurs when the stress voltage is applied. The stress application will cause holes from the channel to obtain sufficient energy to tunnel into the precursor located near to the interface. The hole trapped in a precursor breaks up the bonds in the Si-Si dimer, causing a positively charged E' center and a silicon dangling bond created. The transition between state S_2 to S_3 and back to S_2 is during the emission and recapture of hole between state S_2 and S_3. Electrons tunneling back and forth of the dangling bond will cause the defect to be repeatedly charged and discharged. From state S_3, the neutral E' center will recover the Si-Si bond in a period of time and return back to the original precursor, state S_1. The transition from

S_2 to S_4 and back to S_2 embarks the second stage of the two-stage model (Grasser et al., 2009). In state S_2, there are a positively charged E' center and an unpassivated silicon dangling bond. This bond inside the E' center may become passivated by gaining a hydrogen which is removed from a passivated silicon dangling bond at the interface. The hydrogen locks in the positive charge and consequently delaying the recovery of the defect. The unpassivated dangling bond left by the hydrogen at the interface is known as interface trap (P_b) center.

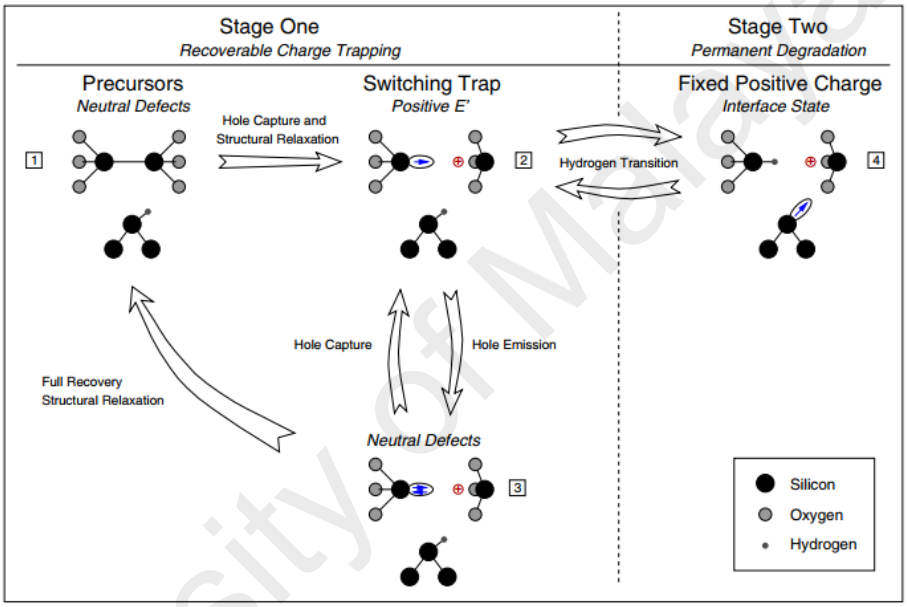

Figure 2.6 The mechanism of two-stage NBTI model (Grasser et al., 2009).

2.5.1.3 As-grown (AG) model

The As-grown-Generation (AG) model, as proposed by Ji et al. (Ji et al., 2013) is another NBTI model evolved from the insight of recoverable component and permanent component and is proven to be capable of predicting the device reliability and variability due to NBTI (Ji et al., 2015). The AG model is developed after a thorough understanding of the characteristics of different types of defects and their contributions to NBTI by direct measurements of each type of defects. In addition to the generated interface traps, this model takes into account another two group of defects in the Hf-based stacks, which contribute to NBTI, namely the as-grown hole trap (AHT) and generated defects (GD) (Ji

et al., 2013; Zhang, 2009; Zhang et al., 2008; Zhao et al., 2008). The GD are further divided into two types, the antineutralization positive charges (ANPC) and cyclic positive charges (CPC) (Ji et al., 2015). Each type of defect is attributed to its distinct signatures and properties. AHT is a defect originated from the device itself, no activation process is needed to trigger this type of defect, and will remain the same subsequent to stress. GD on the other hand, is generated by stress-activation and resulted in the increment of defects after stress. AHT possess an energy level below the silicon valence band E_v, thus making it unable to be charged without the presence of hot holes. The charging of AHT is slower than discharging (Ji et al., 2013; Ji et al., 2010; Ji et al., 2015) and therefore, does not significantly contributes to the aging kinetics. GD is divided into CPC and ANPC where the energy level of CPC is near silicon conduction band E_c while ANPC have an energy level above the E_c. Due to their respective energy level, CPC is observed to be capable of repeatedly charged and discharged whereas ANPC can be easily charged but difficult to neutralize. CPC is insensitive to temperature but ANPC is susceptible to temperature where it decreases at higher measurement temperature (Zhao et al., 2008).

At short stress time, the NBTI degradation is observed to saturate quickly and failed to follow power-law (Huard et al., 2006). This indicates the filling up of AHT. Previous literatures have reported that the charging of AHT follows the first-reaction model (Zhang et al., 2004; Zhang, Sii, Groeseneken, & Degraeve, 2001) while GD follows a power-law (Aoulaiche et al., 2008; Kumar et al., 2007; Tan et al., 2003). The power-law can be restored by removing AHT from the total degradation and the remaining part is the component of GD (Ji et al., 2013). Considering both first-reaction model and power-law, the AG model proposed the following NBTI kinetic expression:

$$\Delta V_{th} = At^n + c(1 - e^{-t/t^*}) \qquad 2.2$$

where A, n, c and t^* are constants for a given stress bias and temperature, acquired from experimental data fitting with the least-square errors (Ji et al., 2010).

The charging of AHT and generation of CPC will saturate with time during aging but ANPC does not saturate and thus dominates the long-term aging. GD is responsible for almost 90% of the total NBTI degradation toward the end of device lifetime under practical use-conditions (Gao et al., 2017). The AG model can accurately separate ANPC from the other defects, allowing a reliable NBTI lifetime prediction (Ji et al., 2015).

2.5.2 Hot Carrier Injection

Hot carrier injection (HCI) phenomena consists of four different mechanism, specifically the drain avalanche hot carrier (DAHC) injection, secondary generated hot electron (SGHE) injection, channel hot electron (CHE) injection and substrate hot electron (SHE) injection (Maricau & Gielen, 2013). DAHC injection mechanism revolved around high drain voltage application under non-saturated conditions ($V_d > V_g$) which contribute to very high electric field near the drain. This high electric field causes channel carriers to accelerate into the depletion region of the drain. Impact ionization occurs when the accelerated channel carriers collide with Si lattice atoms, creating electron-hole pairs. These generated electron-hole pairs can tunnel into the gate oxide if they gain sufficient energy to overcome the Si/SiO_2 electric potential barrier, leading to the creation of interface traps or charge trapping. A space charge is formed due to the trapped hot carriers in the Si/SiO_2 interface or within the oxide, and will eventually increase over time as more charges are trapped. These trapped charges are responsible for the deterioration of device performance. Additionally, most of the hole from electron-hole pairs generated by impact ionization flow back to the substrate, leading to an increase in bulk current. For that reason, hot carrier degradation can as well be determined by measuring the bulk current. The most relentless device degradation is caused by DAHC injection mechanism as compared to other HCI mechanism.

SGHE injection occurs as a result of the creation of new hot carriers by the carriers generated from DAHC impact ionization (Maricau & Gielen, 2013). The SGHE

mechanism is similar to DAHC where the drain voltage applied is high ($V_d > V_g$), which act as an impellent condition for impact ionization. The difference between SGHE and DAHC is the influence of the field created by substrate voltage. Field due to substrate voltage accelerates the first carriers and possibly generate the secondary carriers. The secondary carriers are further driven by the substrate voltage field towards the surface region, resulting in the carriers to further acquire kinetic energy to surpass the surface energy barrier. The effect of SGHE is fairly small and its contribution is insignificant to the degradation of the device.

CHE injection effect is at its maximum when significantly high gate and drain biases ($V_g \approx V_d$) are applied to the device (Maricau & Gielen, 2013). The high gate voltage causes channel carriers to deviate from their original path. Instead of moving from the source to drain, the channel carriers are driven to change direction towards the gate oxide before reaching the drain. SHE injection takes place when a high positive or negative bias ($|V_b| >> 0$) is applied to the substrate of the transistor (Maricau & Gielen, 2013). Carriers in the substrate are compelled toward the Si/SiO_2 interface by the substrate electrical field which causes carriers to further gain kinetic energy as they move toward the gate oxide interface. The energetic carriers potentially overcome the energy barrier at the channel/gate oxide interface and are injected into the gate oxide, where some of them are trapped. SHE injection is unusual from other HCI mechanisms in term of the effect distribution. SHE injection effect is uniformly distributed along the channel while the effect of other HCI mechanisms is concentrated near the drain of the device. The four different HCI mechanisms are illustrated as shown in Figure 2.7.

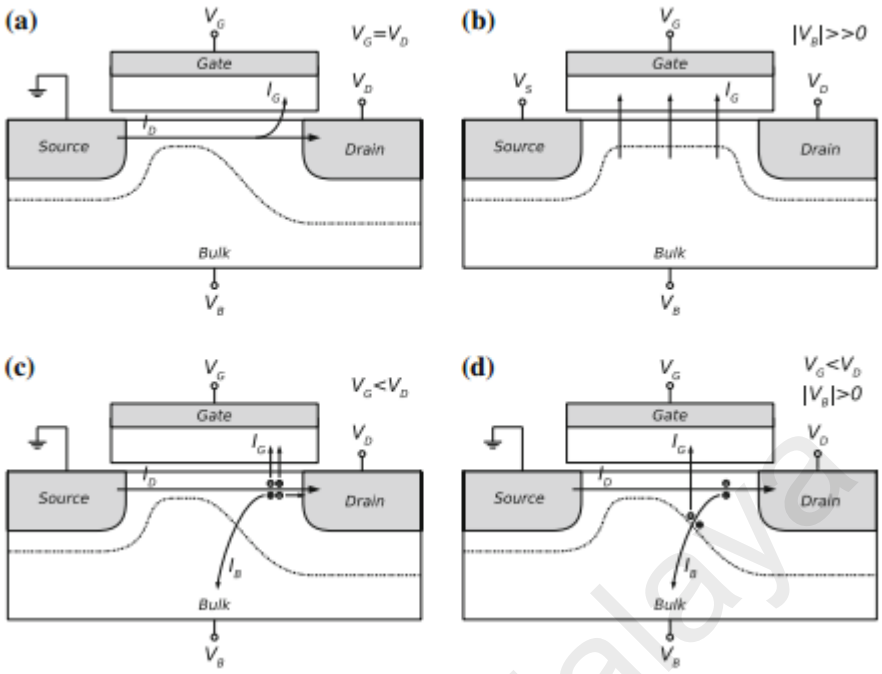

Figure 2.7 HCI mechanisms (a) Drain avalanche hot carrier (DAHC) injection (b) Channel hot electron (CHE) injection (c) Substrate hot electron (SHE) injection (d) Secondary generated hot electron (SGHE) injection (Maricau & Gielen, 2013).

The commonly used HCI model is the power law time dependence (Hu et al. 1985; Kufluoglu and Ashraful Alam 2004) as shown below:

$$\Delta V_{th} = A_{HCI} t^{n_{HCI}} \qquad 2.3$$

where ΔV_{th} is the threshold voltage shift due to HCI and n_{HCI} is the HCI time exponent.

2.6 NBTI reliability issue in high-k metal gate (HKMG) MOSFETs

Extreme gate dielectric scaling in conventional MOSFET has resulted in the domination of direct tunneling current through oxides thinner than 2 nm, consequently increasing the undesirable gate leakage current (Lee, King, & Hu, 1999; Lo, Buchanan, & Taur, 1999). For that reason, further gate dielectric scaling is becoming more and more challenging. As conventional MOSFET reached its scaling limits, high-k metal gate (HKMG) MOSFET was introduced to continue the trend of gate dielectric scaling in order to maintain favorable capacitive coupling between the gate and the channel potential (Shigyo & Hiraoka, 1999). Replacing SiO_2 gate dielectric with high-k material will make

it feasible to have a physically thicker dielectric layer while maintaining the same capacitive coupling, which in turn will reduce the gate tunneling followed by the lowering of gate leakage current (Figure 2.8). HfO_2 and its silicates with permittivity value ranging from 21 to 25 have been an appealing material compared to other various high-k dielectric materials. They exhibit excellent device characteristics and are adaptable to both metal gate and polysilicon gate process (Kang et al., 2000; Lee et al., 2000). Higher value permittivity is not implemented due to dielectric with higher permittivity would induce severe parasitic electron tunneling (Skotnicki et al., 2008). In order to enhance interface quality and acquire high barrier, an interfacial SiO_2 layer is added between the high-k dielectric and silicon in the gate stack. The relationship between high-k thickness and SiO_2 thickness is known as the equivalent oxide thickness (EOT), where the value of EOT is define as the thickness of SiO_2 needed to obtain the same gate capacitance as of high-k material dielectric. EOT is calculated by (Wong & Iwai, 2015),

$$\boldsymbol{EOT = \frac{\varepsilon_{ox}}{\kappa_{high-\kappa}} t_{high-\kappa}} \quad \textbf{2.4}$$

In addition, the usage of metal gate electrode was introduced in HKMG devices in order to overcome the polysilicon depletion. Specification that is needed to be taken into consideration for gate material selection includes suitable work function (WF), low resistivity, chemical stability with the dielectric materials, and process compatibility (Lee, Song, Choi, & Kirsch, 2008; Yeo, Ranade, King, & Hu, 2002). Performance of a device, for an instance, the threshold voltage can be directly affected by the gate WF since the metal gate is close to the channel (Chang, Tang, King, Bokor, & Hu, 2000; Mustafa, Bhat, & Beigh, 2013).

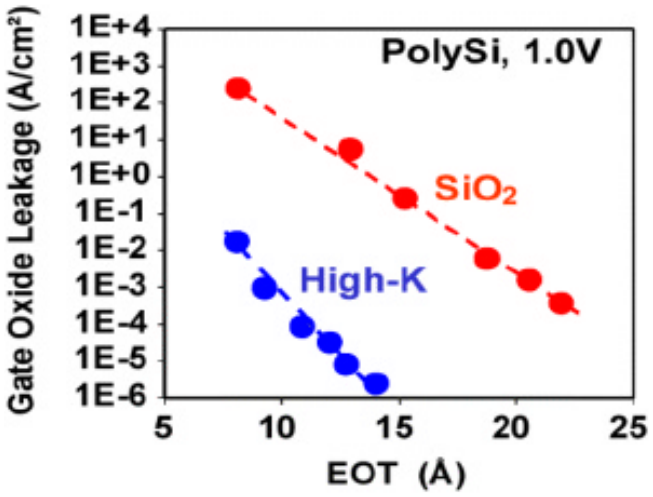

Figure 2.8 Comparison of gate oxide leakage between SiO_2 and high-k dielectrics (Doyle et al., 2002).

Even though HKMG device shows excellent device performance with continuous scaling, the major weakness suffered by this MOS technology is worsening of its NBTI reliability. The summary of work done by previous researchers are tabulated in Table 2.1. From comprehensive investigation done by previous researchers, NBTI reliability of a device can be affected by many factors, particularly the quality of interfacial layer and high-k layer (Heh et al., 2006; Ribes et al., 2005). Other factors dependence of NBTI include various process and device parameters such as hydrogen concentration (Chung et al., 2006), boron concentration (Brozek, Kyono, & Ilderem, 2001), nitrogen concentration (Chung et al., 2006; Garros, Casse, Rafik, et al., 2009; Garros et al., 2008), mechanical stress (Chung et al., 2005; Irisawa et al., 2007), oxide electric field, temperature (Appaswamy, Chakraborty, & Cressler, 2010) and so on (Schroder & Babcock, 2003). It is also found from previous literatures that there is a strong relationship between the physical thickness and NBTI degradation (Hatta, Soin, Hadi, & Zhang, 2010; Hussin, Soin, Bukhori, Hatta, & Abdul Wahab, 2014; Neugroschel et al., 2006). Reducing the thickness of high-k layer resulted in reduced number of bulk defects available to be charged (Ribes et al., 2005) and the charging and discharging of high-k defects depends on the thickness of SiO_2 interfacial layer (Leroux et al., 2004). Previous studies found

that the shift in threshold voltage increases with gate length decreasing (Cao et al., 2014; Lin, Lee, Ou, Chien, & Huang, 2003; Lu, Lin, & Lee, 2007). There is also some research revealed that decreasing gate length will reduce NBTI effect (Cellere, Valentini, & Paccagnella, 2004; Hong-Xia & Yue, 2007) which indicates a spatially uniform distribution of generated defects along the direction of the channel. The gate length dependence of NBTI remains unclear due to lack of detailed understanding. The trend of NBTI degradation correspond to physical thickness variation is observed to be inconsistent as it remarkably depends on the device technology and stress conditions. Most of the literatures focused mainly on the physical thickness of gate stacks while other device parameters have not been explored thoroughly, notably in the advanced features of HKMG devices. The study of reliability of the advanced geometric feature is another new direction that need to be explored. Considering this need, the effects of the advanced geometric features and process parameters on NBTI will be one of the main focus of this work as well as identifying the layer of gate stack which contributes the most to NBTI threshold voltage degradation.

Table 2.1 Summary of NBTI study by previous researchers.

Device under test	Design parameters varied		Effect on NBTI performance	Reference
	Geometry	Process		
SiON gate dielectric PMOS	-	nitrogen concentration (N%)	NBTI increased with N%	(Wu, Ma, Zhang, Lin, & Chan, 2015)
SiON and HKMG PMOS	- interfacial layer thickness	nitrogen concentration (N%)	NBTI increased with N% and IL scaling	(Joshi, Mukhopadhyay, Goel, Nanware, & Mahapatra, 2014)
Advanced process HKMG PMOS	- high-k thickness - interfacial layer thickness	-	NBTI increased with thicker high-k and thinner IL	(Hussin et al., 2014)
Advanced process HKMG PMOS	- interfacial layer thickness	-	NBTI increased with IL scaling	(Cartier et al., 2011)

Table 2.1 continued

Advanced process HKMG PMOS	- metal gate thickness - high-k thickness - interfacial layer thickness	laser annealing temperature	- NBTI increased with thicker metal gate, thicker high-k, and thinner IL - NBTI reduced with laser annealing	(Hatta et al., 2010)
90 nm process technology PMOS	- channel length - channel width	-	- NBTI increased with channel length reduction - NBTI effect can be either enhanced or reduced by decreasing channel width due to different factors	(Yan-Rong, Xiao-Hua, Yue, & Wen-Chao, 2010)
SiN capping layer PMOS	-	mechanical strain	NBTI worsened with strain	(Teo, Ang, See, & Yang, 2009)
SiON gate dielectric PMOS	-	biaxial tensile strain	NBTI worsened with strain	(Irisawa et al., 2007)
Polysilicon gate PMOS	-	boron concentration	Boron create significant reliability problem	(Brozek et al., 2001)

2.7 HCI reliability issue in shallow trench isolation (STI) based LDMOS

Laterally diffused metal-oxide-semiconductor (LDMOS) transistors are considered as promising device that are broadly used in high voltage, smart power technologies due to its low on-resistance (R_{on}) and it can be conveniently integrated within existing CMOS technologies (Whiston et al., 2000). As the technology is scaled down, the optimization of LDMOS becomes more challenging in term of obtaining comparable hot carrier injection (HCI) performance with the previous nodes. Scaling down of devices have resulted in higher electric field and worsen the HCI due to high concentration of well implantation and is closer to Si/SiO_2 interface. In an ideal situation, the device operating voltage should be reduced together with the dielectric thickness to remain the electric field across the gate dielectric to be constant. Nevertheless, LDMOS transistors are

usually operated under high drain and gate voltage for maximum output power under wide temperature range, thus making HCI to be a major reliability issue in LDMOS devices (Brisbin, Strachan, & Chaparala, 2005; Moens, De Keukeleire, Degraeve, Tack, & Groeseneken, 2004). A lightly doped drift region is commonly implemented near the drain of LDMOS device to sustain high breakdown voltage. Breakdown voltage can be improved by increasing the length of the drift region. However, increasing the drift region causes a tradeoff between voltage handling capability and the on-resistance performance. On-resistance increases with increasing drift region length. To balance the tradeoff, previous researchers have proposed several improvised structures (Kwon et al., 1991; Kwon & Ng, 1992; Lin, Tu, See, & Tam, 1995; Nezar & Salama, 1991; Zitouni et al., 1999). Shallow trench isolation (STI) based LDMOS is among the structures proposed, a device with STI structure in the drift region, where the STI is used to reduce the possibility of gate oxide breakdown at high drain voltages resulted from the decreased in peak electric field and potential crowding near the gate end (Moens & Van den Bosch, 2006; Xiao et al., 2008; Zitouni et al., 1999). Required breakdown voltage can be sustained as shorter drift region length is adequate with the usage of STI and therefore, on-resistance can be reduced without abandoning the voltage handling capability. The summary of work done by previous researchers are tabulated in Table 2.2. Most of the studies of STI-based LDMOS transistors focused primarily on the layout geometry effect on device electrical performance (Deivasigamani et al., 2016; Huang et al., 2014; Jin et al., 2017; Kamoulakos, Haniotakis, Tsiatouhas, Schoellkopf, & Arapoyanni, 2001) while the study of hot-carrier reliability of the device can hardly be found. The study of hot carrier reliability in STI-based LDMOS is of paramount importance due to the complex device architecture, making the degradation mechanism substantially differ from the standard CMOS devices (Hefyene, Anghel, Gillon, & Ionescu, 2005; Moens, Tack, Degraeve, & Groeseneken, 2001).

Table 2.2 Summary of HCI study by previous researchers.

Device under test	Design parameters varied		Effect on HCI performance	Reference
	Geometry	Process		
STI LDMOS	- channel length (L_{ch}) - drift region and polygate overlap (L_p) - drift region and p-well overlap (L_w) - STI width (L_s)	-	Small L_p and large L_w overlap size can greatly improve HCI performance	(Li et al., 2017)
Conventional LDMOS	-	LATID techniques	Good HCI performance for 30^o tilt and least for 60^o tilt implant technique	(Sheu et al., 2016)
Conventional LDMOS	- n-drift length (L_{drift}) - n-drift thickness (t_{drift})	n-drift doping concentration (N_d)	With a p-buried layer in the n-drift region, R_{on} can be further reduced through a "double RESURF" design by reducing L_{drift}, or increasing N_d or t_{drift}	(Liu & Chee, 2015)
20V and 50V rated STI LDMOS	STI depth	-	- STI depth variations show slight impact on the I_d degradation for 20V LDMOS - 50V LDMOS is insensitive to STI depth variations	(Shi et al., 2011)
STI LDMOS	- accumulation region length (L_A) - STI angle - STI thickness (t_{STI}) - field plate contact length (L_{fp})	-	- Strong dependence of the I_d shift is observed with L_A and STI angle variations - I_d shift is negligible to the t_{STI} and L_{fp} variations	(Reggiani et al., 2010)

2.8 Summary

This chapter gives an overview of challenges encountered by the scaling down of MOSFET devices. The most critical device aging degradation mechanisms, NBTI and HCI were described in details. To further evaluate the reliability performance of each technology node, a robust framework needs to be developed in order to understand the defects behavior with regards to the performance. Research works concerning device reliability performance by parametric design approach are limited, as most of the previous work mainly focuses on the reliability from a particular transistor design as shown in Table 2.1 and Table 2.2. This study will address the impact of specific design consideration on NBTI and HCI performance in much more detail by gaining insight into the current distribution density, impact ionization rate as well as electric field distribution using 2D TCAD contour plot. Since the evolution of technology node leads to higher device stress and consequently reducing the reliability safety margins in modern technologies, design for reliability has ever since became one of the most important aspect that must not be overlooked by design engineers. Understanding the reliability performance based on different design consideration and the underlying defects behavior are essential for the development of aging simulator, which helps in the early design phase towards designing a more reliable and competitive end-product.

CHAPTER 3: RESEARCH METHODOLOGY

3.1 Introduction

This chapter consists of devices' design considerations and simulation conditions to characterize the reliability performance of different type of advanced-process MOSFETs as well as method in analyzing the reliability performance of the device. The devices under study which were simulated using the Synopsys Sentaurus TCAD includes 32 nm technology high-k metal gate pMOSFET and n-type STI LDMOS. The device structures with its physical models and the simulation conditions employed in the Synopsys Sentaurus TCAD are discussed in depth in the following sections. The devices' design considerations as well as the reliability analysis method adopted in this work are specifically chosen to study the NBTI and HCI phenomena affecting advanced sub-nm devices.

3.2 Flow chart of overall project methodology

The workflow of the project as shown in Figure 3.1 were done by simulation approach using Synopsys Sentaurus TCAD. Sentaurus TCAD tools can be divided into Sentaurus Process, Sentaurus Device and Sentaurus Visual where they are used to simulate real fabrication process flow for a broad range of technologies, simulating the reliability performances of the device and extracting appropriate electrical parameters including 2D contour visualization of the operating device. Simulation models such as the drift-diffusion model, hydrodynamic model, enhanced Lombardi model as well as thermodynamic model were adopted in this work.

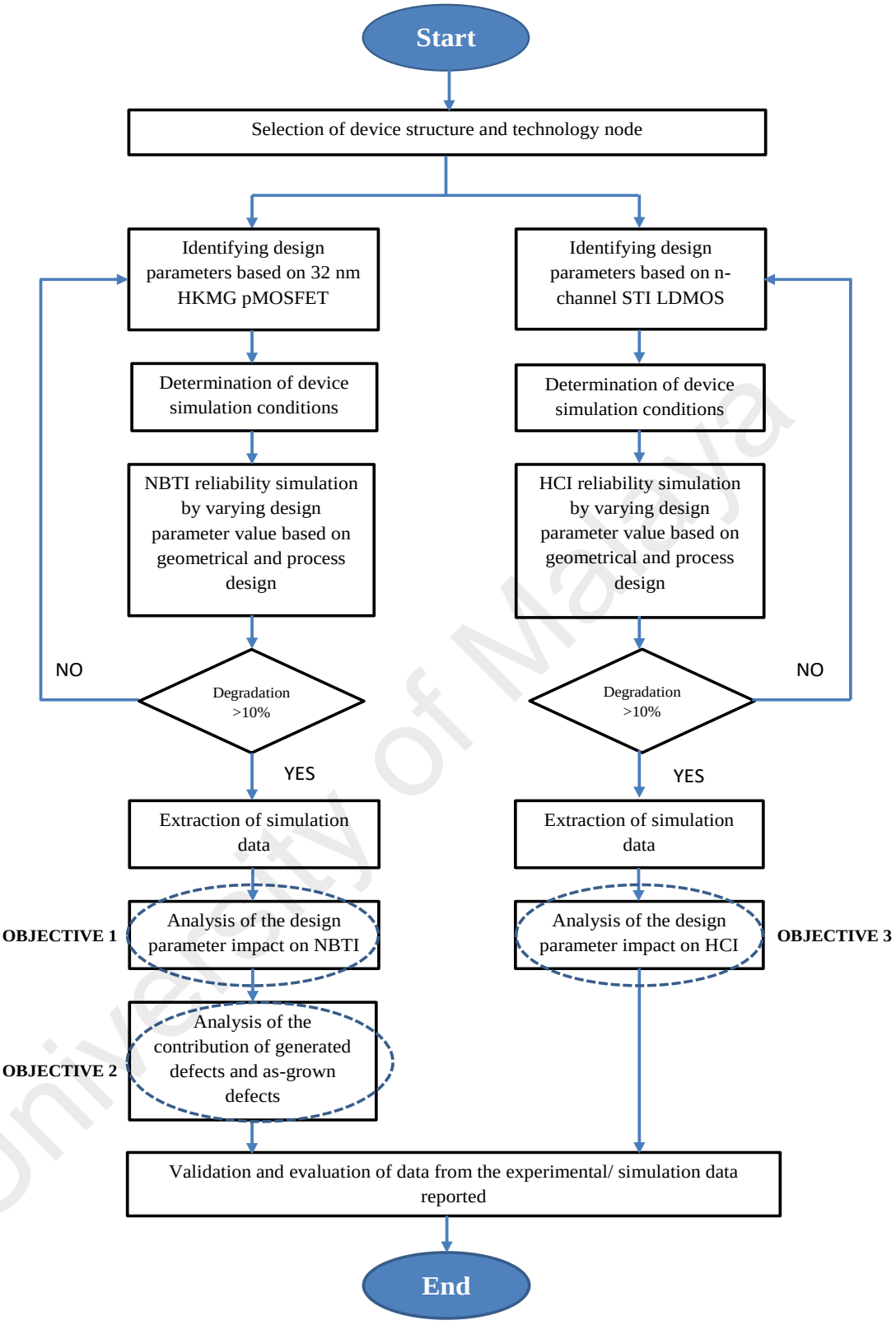

Figure 3.1 General overview of the project flow.

3.3 Selection of device structure and technology node

3.3.1 32 nm technology advanced process high-k pMOSFET

32 nm technology pMOSFET with hafnium-based high-k dielectric and aluminium nitride (AlN) metal gate as shown in Figure 3.2 is simulated by using the Synopsys TCAD Sentaurus simulator ("Sentaurus Technology Template : 32-nm Gate-First Flow and CMOS Processing," 2011). The devices used are based on the 32 nm technology gate-first CMOS process flow following the standard manufacturing trends for sub-micron devices. This fabrication process consolidates the shallow trench isolation (STI) formation, high-k gate dielectric and metal gate deposition, stress engineering application as well as the usage of laser annealing. The device fabrication process flow in this simulation is presented in Figure 3.3. The drive current can be improved as the leakage current is suppressed, and process-related problems such as ultra-shallow junction formation can be overcome by implementing the gate-first CMOS process scheme. Laser annealing process was adopted in order to suppress transient-enhanced dopant diffusion.

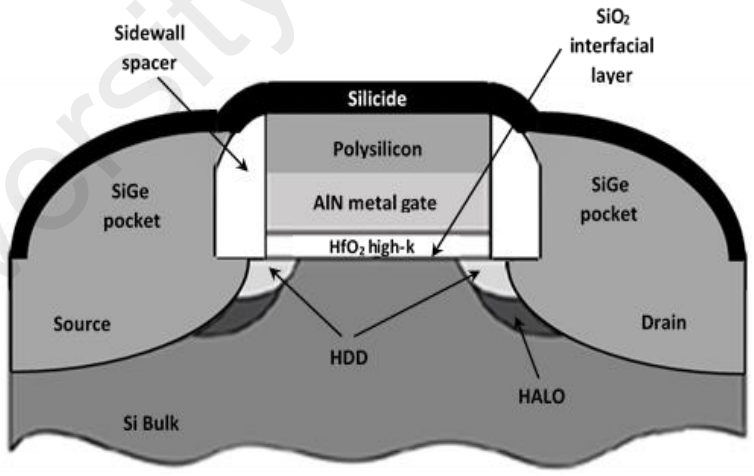

Figure 3.2 Cross-sectional structure of high-k gate stack.

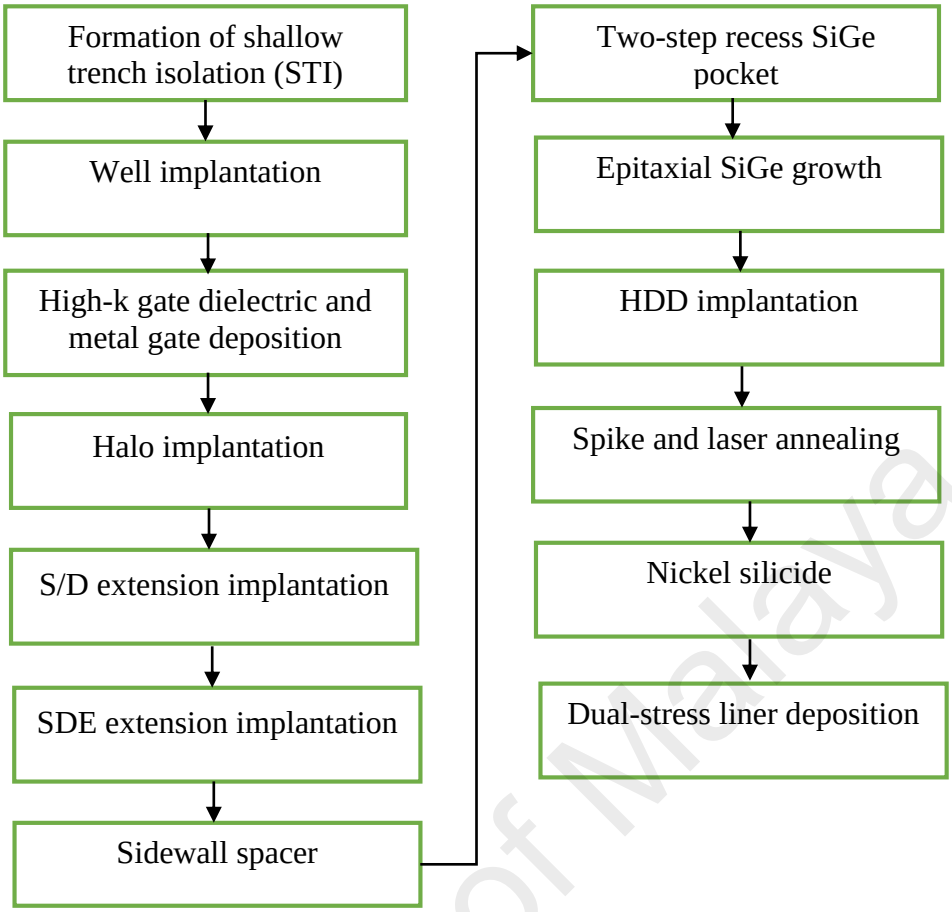

Figure 3.3 Flow of PMOS structure formation based on the process of 32 nm technology node.

Figure 3.4 shows the comparison of electrical characteristics between simulation results and experimental data from N.Yasutake et al. (Yasutake et al., 2007) whereby the process of fabrication of the device under test is similar to this work. The simulated device shows good compliance with experimental data, though small deviation is observed for Vg > -0.4 V. The deviation in the linear region is resulted from the difference of the level of interface state density (D_{it}) for both devices (Hsu & Li, 2014). This good agreement gives certainty that the model for the simulation used in this work is credible in order to ensure that the impact of NBTI degradation in this study is realistically assessed.

Though the device structure of this work and the cited work is slightly different, both of the devices have similar equivalent oxide thickness (EOT) value of 0.912 nm and 1.0 nm respectively. EOT is the thickness of silica that would give an equivalent capacitance

in accumulation to the device being measured (Mohsenifar & Shahrokhabadi, 2015). Since the EOT of both devices are similar, the electrostatic and on-current (I_d at $V_{gs} = V_{ds}$ = 1 V) properties of the transistors do not vary much, which keep the I_d–V_g characteristics similar in the interested range (Luisier & Schenk, 2008). The trend of the transfer curves is consistent with previous works (Petrosyants & Popov, 2015; Pradhan, Mohapatra, Sahu, & Behera, 2014).

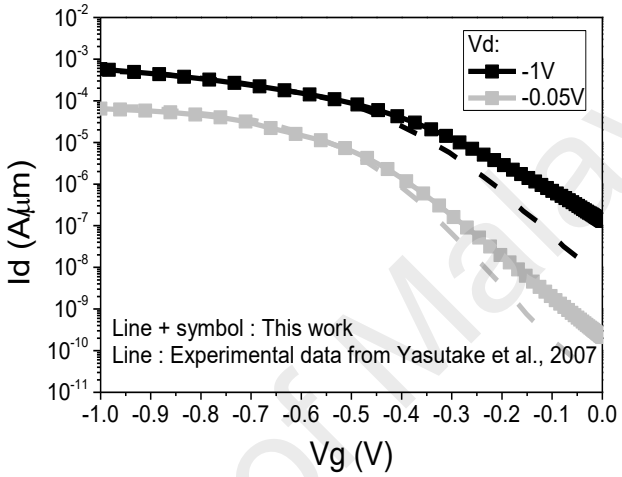

Figure 3.4 I_dV_g comparison between simulated device and experimental data.

3.3.2 Laterally diffused MOS with shallow trench isolation (STI LDMOS)

Two-dimensional STI LDMOS device structures are simulated through the device process simulator. The simulation process flow for STI LDMOS device is presented in Figure 3.5. The LDMOS fabrication processes are compatible with the standard CMOS process as the basic process steps for the fabrication of n-channel LDMOS devices are very similar to the n-channel MOSFET. The schematic cross section of the n-type STI LDMOS transistor used in this work is shown in Figure 3.6. The gate length and gate width of the device are 3 µm and 0.5 µm, respectively. The layout parameters L_{ch} (the length of channel region) and L_a (the length of accumulation region between channel and STI) are also shown in Figure 3.6. This device features a shallow trench isolation (STI) in n-drift region near the drain. STI plays an important role in improving the breakdown voltage of the device by taking advantage of the higher critical electric field of SiO_2 as

compared to silicon (Sunitha et al., 2017). Phosphorous implantation in the device structure simulation is carried out in two steps, where the first step is a lower energy implant and followed by a higher energy implant. More uniform doping profile for the same thermal budget can be achieved by this two-step implantation. The implantation process is followed by a three steps thermal annealing process: ramp up, constant temperature anneal and ramp down. Implantation of p^+ body contact defines the contact for body needed to connect to the substrate.

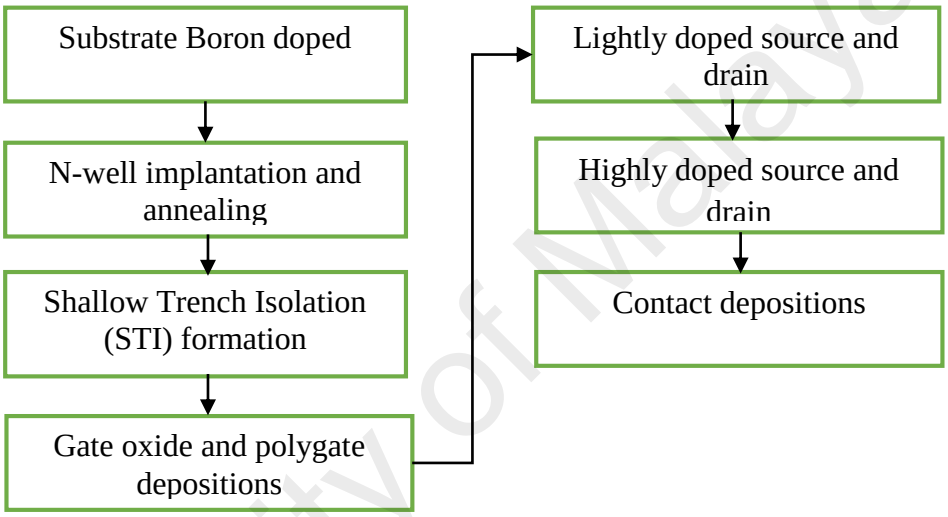

Figure 3.5 Simulation process flow for STI LDMOS device.

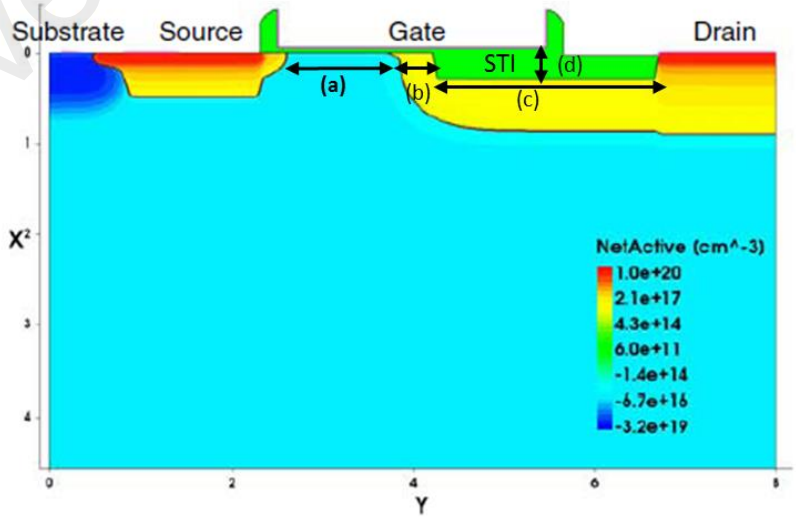

Figure 3.6 Cross-sectional structure of n-channel STI LDMOS. (a) Channel length, L_{ch} (b) Accumulation region length, L_a (c) STI region length, L_{sti} (d) STI region depth, t_{sti}.

3.4 Identifying design parameters

Broad range of geometric variations were simulated in order to study the impact of different structure of devices on NBTI. The geometric parameters varied include the thicknesses of the HfO_2 high-k layer (2 nm - 4 nm), SiO_2 interfacial layer (0.5 nm - 1 nm), AlN metal gate (1.8 nm - 6 nm) as well as additional advanced geometrical features which include polypitch, spacer length and SiGe pocket depth (Alam, Anand, & Dasgupta, 2012; Bae et al., 2000; Hatta et al., 2010; Hussin et al., 2014; Uchino et al., 1997; Yuan & Woo, 2004). The effect of a particular design parameter on NBTI was analysed by changing one parameter at a time while keeping the others constant. The degradation of the device with regards to process design considerations was studied by varying boron dose of highly doped drain (HDD), metal gate work function and halo doping concentration. Sole study of the impact of process variation on NBTI is achieved by keeping the geometric structure of the device to some fixed parameters.

As for the HCI study, the impact of different structure of devices on HCI was investigated by varying parameters which includes the STI depth, STI angle, gate oxide thickness, p-substrate doping as well as S/D implantation dose (Cortés, Fernández-Martínez, Flores, Hidalgo, & Rebollo, 2008; Park, Grasser, Kosina, & Selberherr, 2003; Toulon et al., 2011; Wu, Chen, Su, Lee, Lin, Hsu, et al., 2006). The effect of a particular design parameter on NBTI was analysed by changing one parameter at a time while keeping the others constant. Figure 3.7 below shows the overview of the overall design parameter considerations of the project.

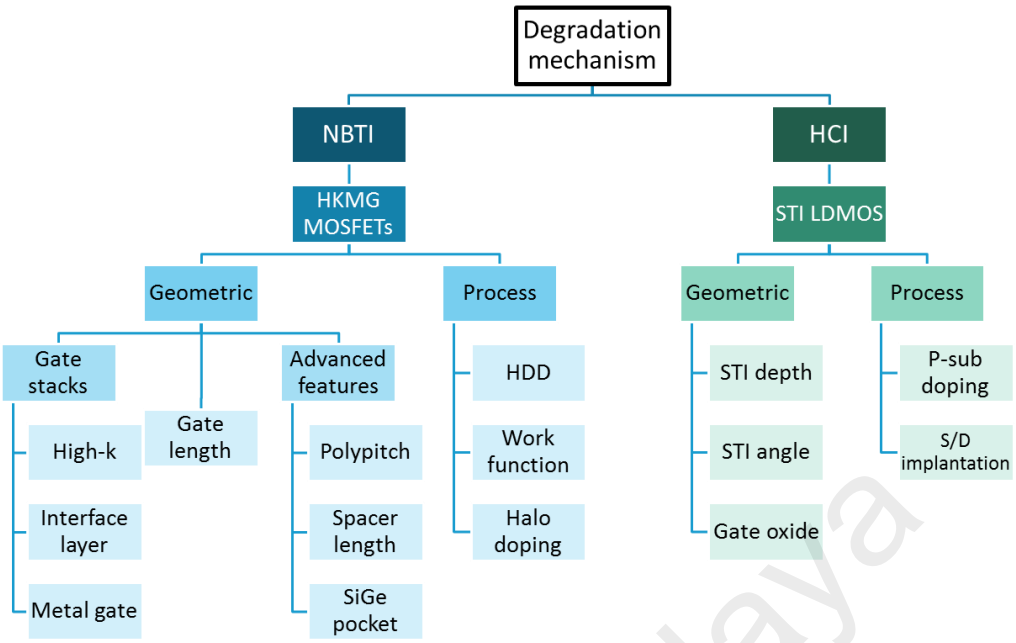

Figure 3.7 Design parameter considerations under study.

3.5 Determination of device simulation conditions

The NBTI stressing was performed under constant-voltage bias conditions at an elevated temperature. During the stress, the gate terminal was negatively biased, with respect to the source and the drain ($V_{gs} < 0$), while V_{ds} is fixed to zero ($V_{ds} = 0$). Application of pre-stress voltage is necessary as it governs the gate bias in specifying the initial conditions prior to the stress phase of the simulation. The NBTI effect was studied at high stress biases of oxide field (E_{ox}) ~ -8MV/cm to -12MV/cm (Ang et al., 2011; Boo & Ang, 2012; Gao, Ang, et al., 2011; Gao, Boo, et al., 2011) and at stress temperatures ranging from room temperature (RT) to 375K (Ang et al., 2011; Boo & Ang, 2012; Gao, Ang, et al., 2011; Gao, Boo, et al., 2011). The work aims to focus on looking at properties of the as-grown and generated defects hence the stress time investigated was set from 1 millisecond to 1000s.

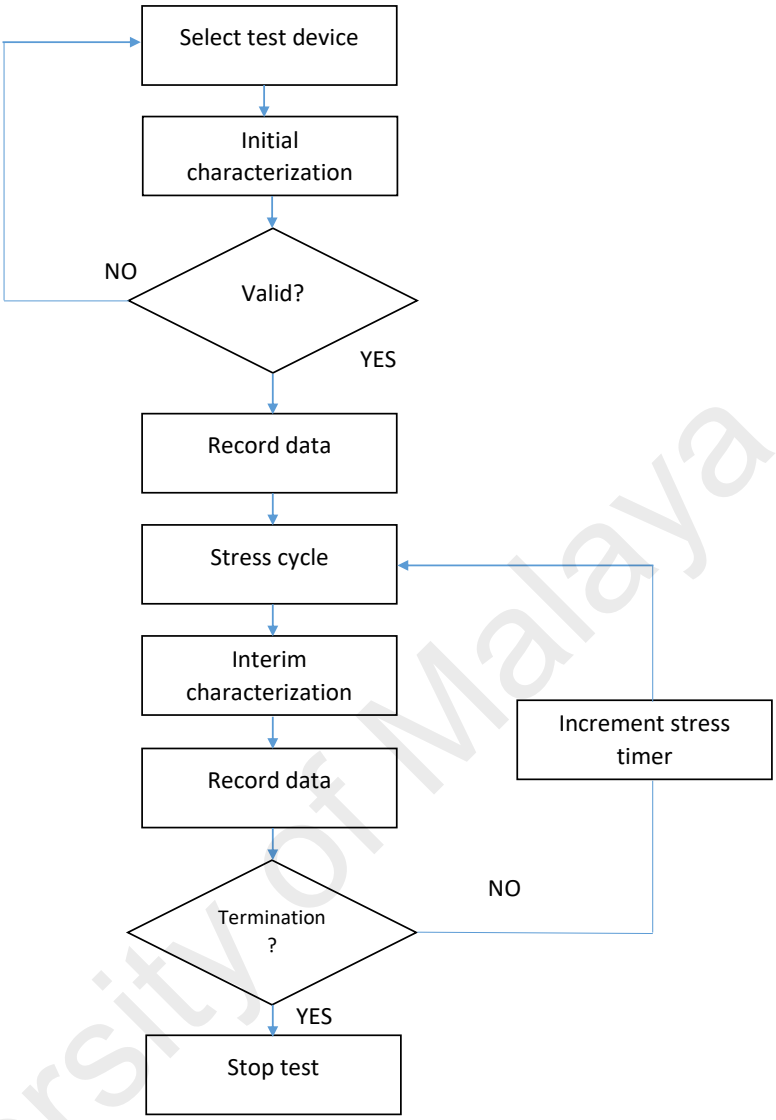

Figure 3.8 JEDEC standard for NBTI and HCI stress test procedure (JEDEC, 2001, 2004).

The HCI effect was studied by performing hot carrier stressing under constant voltage bias conditions (5V and 15V) at stress temperature of 300K and 400K with the substrate and source connected to ground. The drain and gate stress bias voltage must be established before hot carrier testing begins. The maximum drain stress bias voltage applied is set to be less than 90% of the device's drain-to-source breakdown voltage to guarantee realistic channel hot carrier conditions (Keithley Instruments, 2000). To monitor the degradation, electrical parameters of the device are measured at chosen time intervals. In this work,

the saturation current (I_{dsat} at V_{ds} = 10V and V_{gs} = 10V) is the controlled parameters for the hot carrier stress test. All of the reliability test implemented in this work follows the JEDEC standard stress test procedure as shown in Figure 3.8.

3.6 Reliability simulation by varying design parameter value

3.6.1 Negative Bias Temperature Instability simulation model

For the 32 nm technology high-k metal gate devices, both the Poisson equation and carrier continuity equations for 2D simulation involved in high-k devices are solved by the incorporation of drift diffusion and hydrodynamic models. The hydrodynamic model was only activated in the silicon region, while the drift diffusion model was activated for the entire region. The assignment of certain model according to the region is to ensure that the convergence in the simulation is achieved. The effects of carrier heating in a sub-micron device subjected to the NBTI stresses can be better understand by applying the hydrodynamic model compared to the drift-diffusion simulation model and will yield more physically-accurate simulation results.

This work implements the Philips Unified Mobility model, High-Field Saturation and Enhanced Lombardi model with High-k degradation. Philips Unified Mobility model consolidates the description of the majority and minority carrier bulk mobility. This model takes into account the clustering of impurities, mobility temperature dependence, screening of ionized impurities by charge carriers and electron-hole scattering. The carrier drift velocity is no longer proportional to the electric field at high electric field condition but saturates to a finite speed. Therefore, to tailor the carrier transport models, the Canali model for the actual mobility model was chosen. The Canali model based on the Caughey-Thomas formula is capable to model the carrier mobility during high electric fields.

The Enhanced Lombardi model with High-k degradation was adopted as the mobility degradation model at interfaces in this work. This model was selected considering the devices under test are high-k based device. The large transverse electric field forces

carriers to strongly interact with the semiconductor-insulator interface in the channel region of MOSFET and therefore, making the mobility degradation at the interface of this region important. The acoustic surface phonons and surface roughness will cause the carriers to be scattered. Two possible contributors which are remote Coulomb scattering (RCS) and remote phonon scattering (RPS) were taken into account in the Enhanced Lombardi model.

The generation and recombination simulation process in this work adopts the SRH model where the carriers' lifetime is calculated based on doping-dependent model. The doping-dependent of the SRH lifetimes is based on Scharfetter relation. The Scharfetter relation concludes that the solubility of a fundamental, acceptor-type defect is strongly correlated to the doping density.

3.6.2 Hot Carrier Injection simulation model

For the n-channel STI LDMOS devices, thermodynamic transport model was used in the simulation where the model enhances the drift-diffusion approach to solve the lattice temperature equation, assuming that the charge carriers are in thermal equilibrium with the lattice. The carrier temperatures and the lattice temperatures are therefore described by a single temperature. The drift-diffusion model which includes thermodynamic effects is usually sufficient in terms of accuracy since the size of power devices is remarkably large compared to that of CMOS devices. The inversion and accumulation layer mobility model was used together with the thermodynamic transport model as this model is able to describe the high transverse electric field that affects carriers to powerfully interact with the semiconductor–insulator interface. The inversion and accumulation layer mobility model is similar to the Lucent (Darwish) model (Darwish et al., 1997) but with the addition of terms which compose of 'two-dimensional' Coulomb impurity scattering in the inversion and accumulation regions of a MOSFET. The calculation of field perpendicular was activated based on perpendicular to semiconductor-insulator interface.

Shockley-Read-Hall recombination model adopted in this HCI simulation is similar to the SRH adopted in the NBTI simulation but with additional calculation of the carriers' lifetime based on temperature-dependent model. The Auger recombination model was also incorporated in this simulation. Auger recombination involves an electron and a hole which recombine in a band-to-band transition and the resulting energy is released to another electron or hole. The density of the electrons or hole which receive the released energy from electron-hole annihilation is used in the expression for the net recombination rate. Another generation-recombination model implemented in this simulation is the Avalanche generation. Electrical breakdown occurs when the charge is multiplied due to the width of a space charge region is larger than the mean free path between two ionizing impacts. Ionization coefficient is achieved from the reciprocal of the mean free path. The threshold behavior of the ionization coefficients follows van Overstraeten–de Man model, where the model expresses the temperature dependence of phonon gas against which carriers are accelerated. As for the hot-carrier injection model, Lucky Electron Injection model which resolves for the nonlocal effects subsequent to large variations in the electric field in submicron MOSFETs was adopted in the simulation. The Lucky Electron Injection model is formulated in terms of an effective electric field obtained from the average carrier energy in the device.

3.7 Extraction of simulation data

3.7.1 Negative Bias Temperature Instability

In the NBTI simulation of this work, the on-the-fly (OTF) measurement technique was applied to the test structure. The OTF technique is often regarded as the method of choice for experimentally investigating NBTI as it is capable to counter the unintentional measurement delay (Denais et al., 2004; Huard et al., 2006; Li et al., 2008; Mahapatra & Alam, 2008; Maheta et al., 2008). The conventional measurement method particularly the measure-stress-measure technique can result in significant underestimation of threshold

voltage shift, ΔV_{th} due measurement delay during the time interval between the removal of stress and the first measurement of the drain current (Reisinger, Blank, Heinrigs, Gustin, & Schlunder, 2007). In the OTF technique, the stress voltage is always applied to the gate, and the degradation of the drain current is measured at stress voltage. The OTF technique monitors both I_d and the transconductance, g_m, at preset intervals under a low drain bias. The ΔV_{th} is obtained from the relationship between the gm and the drain current change, ΔI_d. The stress V_g is perturbed by a small amount of drain bias and the corresponding current variation is recorded in order to evaluate g_m. Since g_m is given by,

$$\boldsymbol{g_m = \frac{dI_d}{dV_g}} \qquad \textbf{3.1}$$

and the degradation of drain current between two measurement points 't' and 't-1' is,

$$\boldsymbol{\Delta I_d(t) = I_d(t) - I_d(t-1)} \qquad \textbf{3.2}$$

Therefore, the shift of threshold voltage between these two points can be evaluated by,

$$\boldsymbol{\Delta V_{th}(t) = \frac{\Delta I_d(t)}{g_m(t)}} \qquad \textbf{3.3}$$

In order to find the lifetime of the device, graph of threshold voltage degradation (ΔV_{th}) versus stress time (s) was plotted and ΔV_{th} = 50mV was chosen as the lifetime criterion, which is in line with the standard criterion used by CMOS manufacturers (Stathis, 2002). The smooth functions available in Curve Fitting Toolbox of OriginPro 8 was utilized to obtain better accuracy of the extracted lifetime as shown in Figure 3.9. Lifetime of different gate bias as degradation of threshold voltage reaches 50mV were then extrapolated towards 10 years (3.154×10^8 s) to obtain the maximum operating voltage (V_{gop_max}) as demonstrated in Figure 3.10.

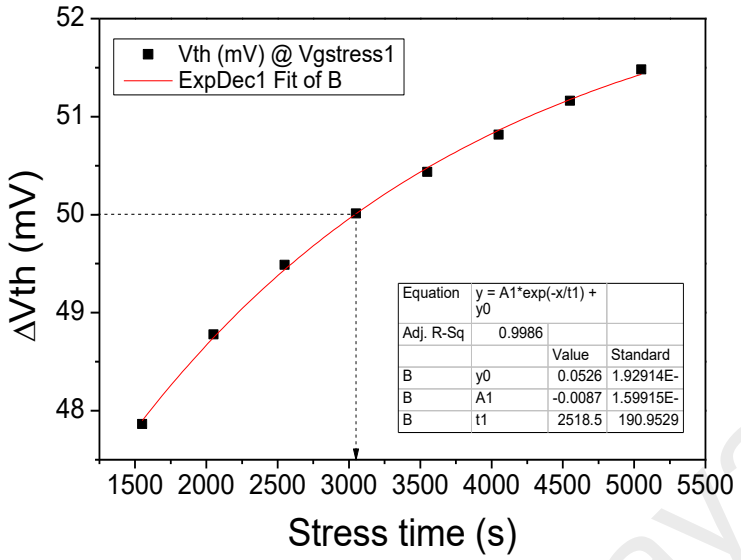

Figure 3.9 Data smoothing to extract device lifetime at ΔVth = 50mV.

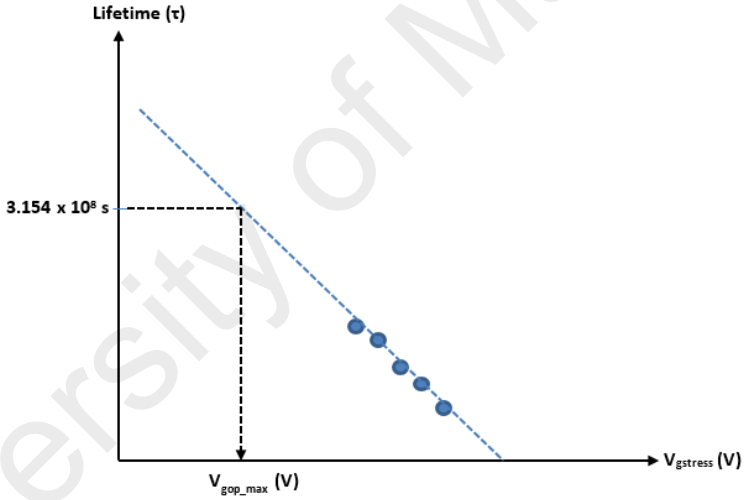

Figure 3.10 Extrapolation of device lifetime to 10 years.

3.7.2 Hot Carrier Injection

I-V measurement was simulated to give insight into the device behavior and allows to quantify some important electrical parameters before and after ageing test. The I-V characteristic is divided into I_d-V_g and I_d-V_d graph, where relevant electrical parameters such as saturation current and on resistance were extracted. Apart from the electrical analysis, the Sentaurus Visual is also use to visualize detailed insight into the impact

ionization rate and electric field distribution. The percentage of saturation current degradation, ΔI_{dsat} in this work is calculated by,

$$\Delta \boldsymbol{I_{dsat}}(\%) = \frac{(\boldsymbol{I_{dsat}(t) - I_{dsat}(0)})}{\boldsymbol{I_{dsat}(0)}} . \mathbf{100} \qquad \mathbf{3.4}$$

and the percentage degradation of on resistance, ΔR_{on} is calculated by,

$$\Delta \boldsymbol{R_{on}}(\%) = \frac{(\boldsymbol{R_{on}(t) - R_{on}(0)})}{\boldsymbol{R_{on}(0)}} . \mathbf{100} \qquad \mathbf{3.5}$$

where I_{dsat} (0) and R_{on} (0) are the initial drain saturation current and initial on resistance values, while I_{dsat} (t) and R_{on} (0) are the drain saturation current and on resistance values at time t. The power law time dependency function (JEDEC, 2001; Takeda et al., 1983) is used to describe the device degradation under hot carrier stress where the absolute value of the change in each parameter as a function of cumulative stress time t can be described as,

$$|\Delta \boldsymbol{I_{dsat}}(\%)| \; \boldsymbol{or} \; |\Delta \boldsymbol{R_{on}}(\%)| = \boldsymbol{C t^n} \qquad \mathbf{3.6}$$

Parameter C is dependent on stress conditions, device geometry, temperature, and technology and parameter n is a technology dependent parameter. The parameter degradation relatively saturates at long stress times, thus making this trend to specifically valid at only short stress times.

3.8 Summary

Devices' design structures of 32 nm technology node and STI LDMOS and have been identified as the investigated advanced-process MOSFET devices in this chapter. Sentaurus TCAD tools were used to simulate each of the devices with its own unique design structures and processes as well as advance physical models. To study the impact of different design parameters on NBTI and HCI, the simulations were conducted with wide range of design parameter values for specific design considerations based on its respective technology. The electrical performances analyzed in this work are important to determine the reliability of the device.

CHAPTER 4: RESULTS AND DISCUSSIONS

4.1 Introduction

Findings obtained in this work are discussed in this chapter. The results are divided into two parts based on different type of degradation studied: NBTI analysis on the advanced-process high-k pMOSFETs technology and HCI analysis on the n-channel STI LDMOS technology. The analysis will highlight on the critical degradation performance by taking into account the geometrical and process design considerations of each type of the device. Validation of simulation results with experimental results from other researchers were carried out, giving certainty that the results obtained in this work are credible.

4.2 NBTI analysis on advanced-process high-k pMOSFETs technology

4.2.1 Preliminary study

In this preliminary study, the degradation of parameter is based on numerical solution for the two-stage NBTI model mechanism. Figure 4.1 shows the threshold voltage degradation curve for different stress bias applied on the device and Figure 4.2 shows the curve of relaxation of threshold voltage after stress bias is removed. The slope increases as higher stress voltage is applied. Gate voltage is often associated with carrier-energy driven degradation (Huard et al., 2006). Higher oxide field due to high stress voltage causes more holes from the channel to obtain sufficient energy to tunnel into the precursor located near to the interface and hence, contribute to the degradation of the device.

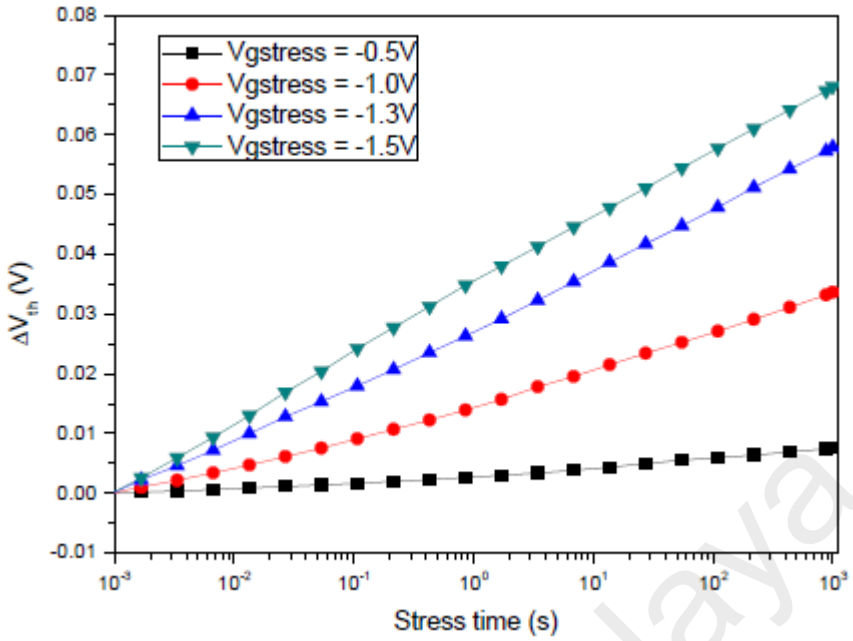

Figure 4.1 Threshold voltage degradation upon the application of stress biases.

The asymmetry between stress and relaxation curves is properly explained by the two-stage NBTI model. The relaxation phase, in which the phenomena of de-trapping of charges occur, intervals over a much larger period of time compared to the stress phase (trapping of charges). The threshold voltage after stress voltage is removed does not totally return to its original level due to the generation of permanent defects.

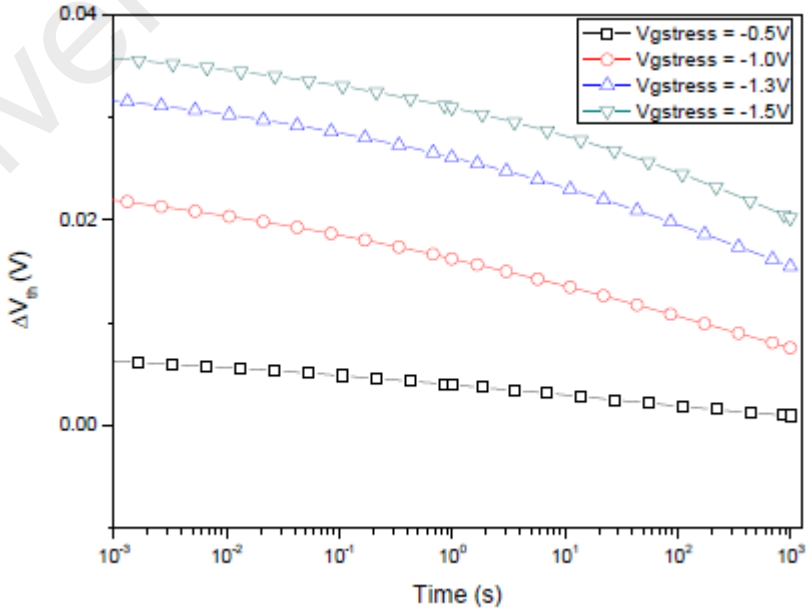

Figure 4.2 Threshold voltage degradation upon the removal of stress biases.

Interface trap, N_{it} is a defect located at the oxide/semiconductor interface in which the action of trapping and de-trapping charge carriers occur. Figure 4.3 shows the interface trap generation, ΔN_{it} (cm^{-2}) for different stress bias applied on the device and the interface trap after stress voltage is removed. The change in the average interface trap, ΔN_{it} clearly shows an increase in the interface state as the NBTI stress progresses and slowly recovers during the relaxation phase. The two-stage NBTI model is able to explain the behavior of the device excellently in which is proven from the agreement between the model and simulation results. The two-stage NBTI model involves the process of two stages which takes the permanent and recoverable defects into account. The threshold voltage after stress bias is removed is unable to entirely return to its original level due to the generation of permanent defects.

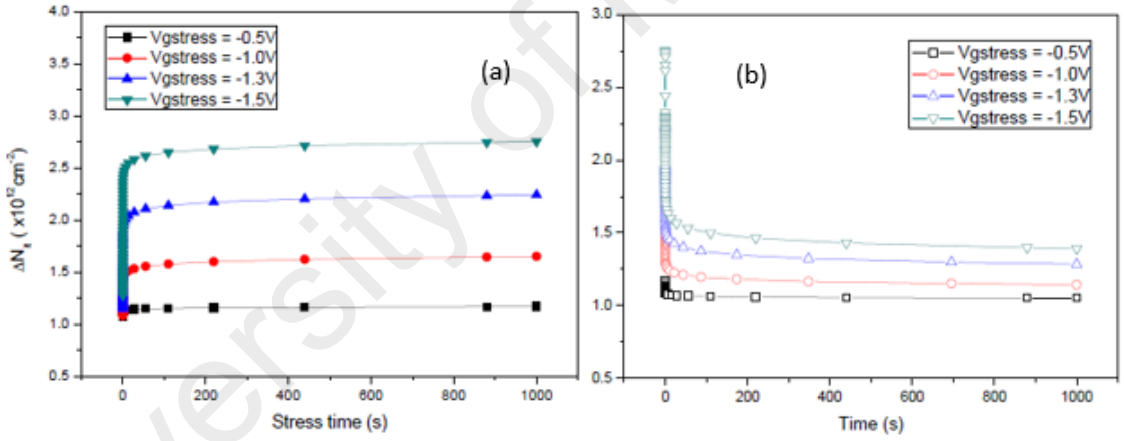

Figure 4.3 Threshold voltage degradation for different stress biases, (a) stress bias is applied and (b) stress bias is removed.

4.2.2 Influence of geometric considerations on NBTI

4.2.2.1 Effects of high-k metal gate stack variation on NBTI

The effect of NBTI can be different for different geometric considerations. Investigation on the impact of geometric considerations on NBTI were carried out by broadly changing the geometric parameters of HfO_2 high-k thickness, SiO_2 interfacial layer (IL) thickness, metal gate thickness, gate length as well as additional advanced features of 32 nm technology node which include polypitch, spacer length and SiGe

pocket depth. Figure 4.4, Figure 4.5 and Figure 4.6 shows threshold voltage degradation of different HfO_2, SiO_2 and metal gate thicknesses at 1 millisecond, 1s and 1000s stress time subsequent to different stress temperature. It has been reported that at short stress time specifically for 1 millisecond, NBTI is dominated by hole-trapping at the as-grown defects (Mahapatra et al., 2013; Veksler & Bersuker, 2014). It is apparent from Figure 4.4 (c), Figure 4.5 (c) and Figure 4.6 (c) that the degradation is consistently small for all thicknesses investigated and the as-grown defects are insensitive to temperature. At stress time of 1s and beyond, generated defects start to monopolize (Mahapatra et al., 2013). The difference between the room temperature and stress temperature at 375K for 1s stress time compared to 1000s stress time shows that generated defects are prone to increase at high temperature for high stress time. This difference however is distinctly smaller in the metal gate layer.

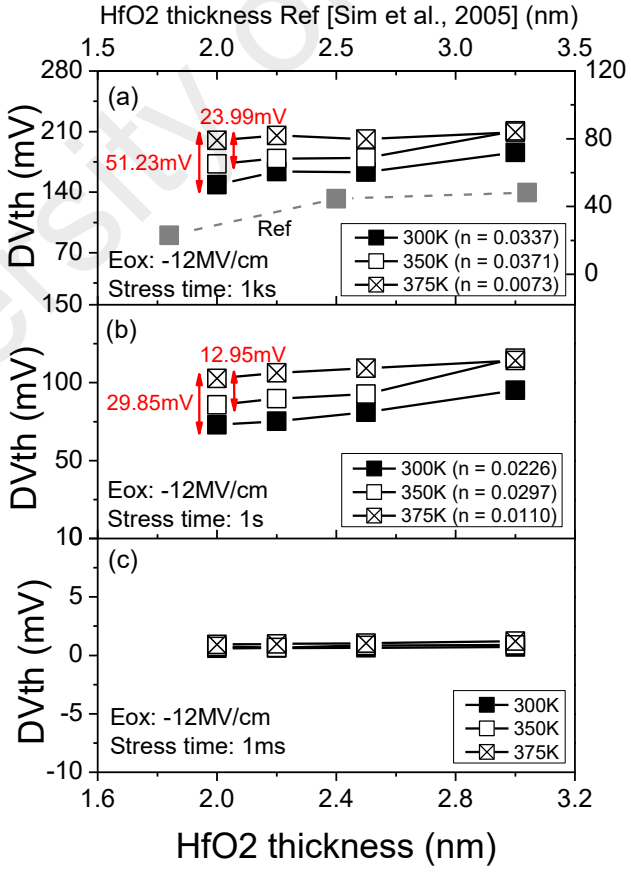

Figure 4.4 Vth degradation subsequent to different stress temperatures at 1 millisecond, 1s and 1000s stress time for different HfO_2 thickness.

The results obtained also suggest that the effect of temperature on thinner thicknesses is more significant than on the thicker for stress time of 1s and 1000s. This finding is in compliance with the findings of previous studies (Krishnan et al., 2005) which conclude that the leakage current mechanism is more temperature dependent in thinner oxide due to the increase in channel surface current caused by either the deep channel punch-through currents or drain-induced barrier lowering (DIBL) that is worsen at high temperature (Ohring & Kasprzak, 2014).

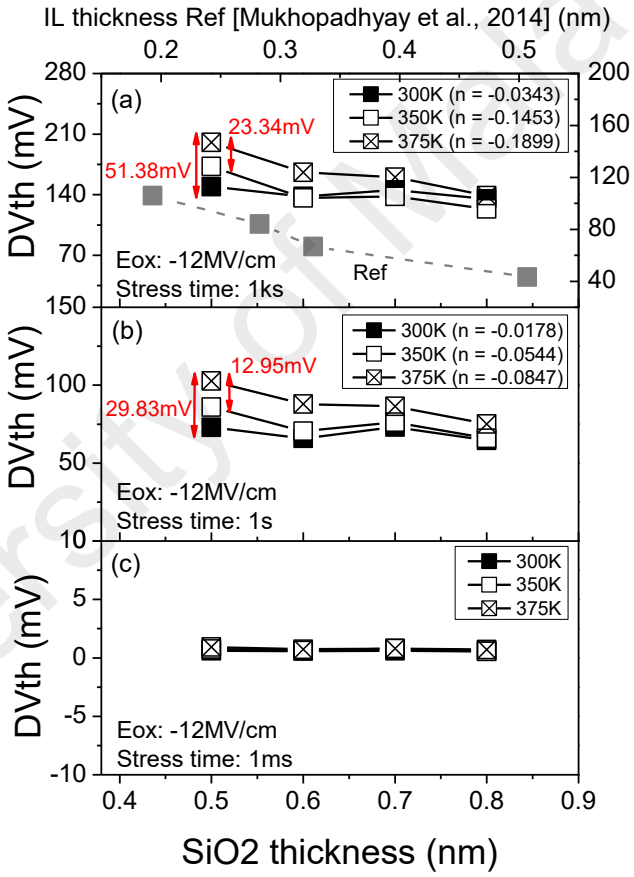

Figure 4.5 Vth degradation subsequent to different stress temperatures at 1 millisecond, 1s and 1000s stress time for different SiO_2 thickness.

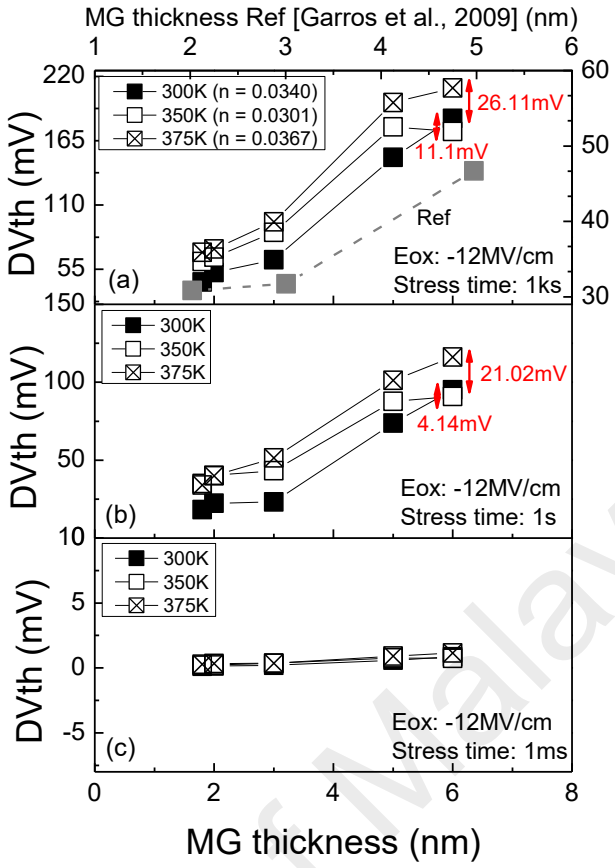

Figure 4.6 Vth degradation subsequent to different stress temperatures at 1 millisecond, 1s and 1000s stress time for different metal gate thickness.

The threshold voltage degradation of HfO_2 and metal gate indicates higher degradation for larger thicknesses while SiO_2 contradicts this observation where thinner SiO_2 seems to be having higher degradation compared to the thicker. Thicker HfO_2 thickness in Figure 4.4 (a) and Figure 4.4 (b) demonstrate higher V_{th} shift due to higher trapping in the bulk high-k layer (Neugroschel et al., 2006). This supports the finding that the defects are of a substantial amount in the bulk high-k layer due to the fact that degradation is highly dependent on the thickness of the bulk. On the contrary, thinner SiO_2 interfacial layer leads to larger V_{th} degradation which differs to HfO_2 due to higher fast transient charging (FTC) effect (Hussin et al., 2014; Neugroschel et al., 2006). FTC effect is more compelling in thinner equivalent oxide thickness (EOT), especially through the scaling of interfacial layer (Lee et al., 2004). The tunneling barrier for holes in the bulk is also

reduced as the SiO_2 IL thickness is reduced and therefore leads to higher probability of defects generation or hole trapping in the oxide bulk (Cho et al., 2012).

Figure 4.6 shows that V_{th} degradation increases as the metal gate thickness is increased. The result is verified with earlier literature (Garros, Casse, Rafik, et al., 2009; Garros, Casse, Reimbold, et al., 2009) where it is found that increasing the gate thickness will enhance the diffusion of nitrogen to the silicon interface which consequently add to degradations. Chemical analysis by performing ToF-SIMS measurement has been previously reported by (Gaumer et al., 2008) in order to investigate the nitrogen distribution in high-k metal gate stack. It is shown that during metal nitride and/or poly-Si deposition, the nitrogen diffuses from metal nitride into the stack. S. H. Bae et al. (Bae et al., 2006) reported that higher interface trap density is observed for thicker metal gate which is due to stress from metal nitride layer subsequent to high temperature annealing. High temperature annealing causes the crystallites of metal nitride films to build up, which is so called the agglomeration effect. Elastic deformation from the growing of the crystallites will result in stress introduction to the metal nitride layer. Thinner metal nitride layer would lead to lesser diffusion of nitrogen due to nitrogen deficiency as discussed in (Choi et al., 2005). The slope obtained from Figure 4.4, Figure 4.5 and Figure 4.6 shows that the change in SiO_2 IL thickness affects V_{th} degradation by 96.16% more than in HfO_2 and 80.67% more than in metal gate at stress temperature of 375K for 1000s stress time. Therefore, it can be summarized that SiO_2 IL appears to be a prominent layer that contributes the most to V_{th} degradation.

Figure 4.7 shows the oxide field dependence of different high-k HfO_2, SiO_2 IL and metal gate thicknesses at 1 millisecond and 1000s stress time. V_{th} degradation is observed to be highly dependent on oxide field but at lower oxide field, this dependency is not affected by the thickness of parameters. At higher oxide field, the thickness of SiO_2 and metal gate seems to affect the threshold voltage shift such that the V_{th} degradation

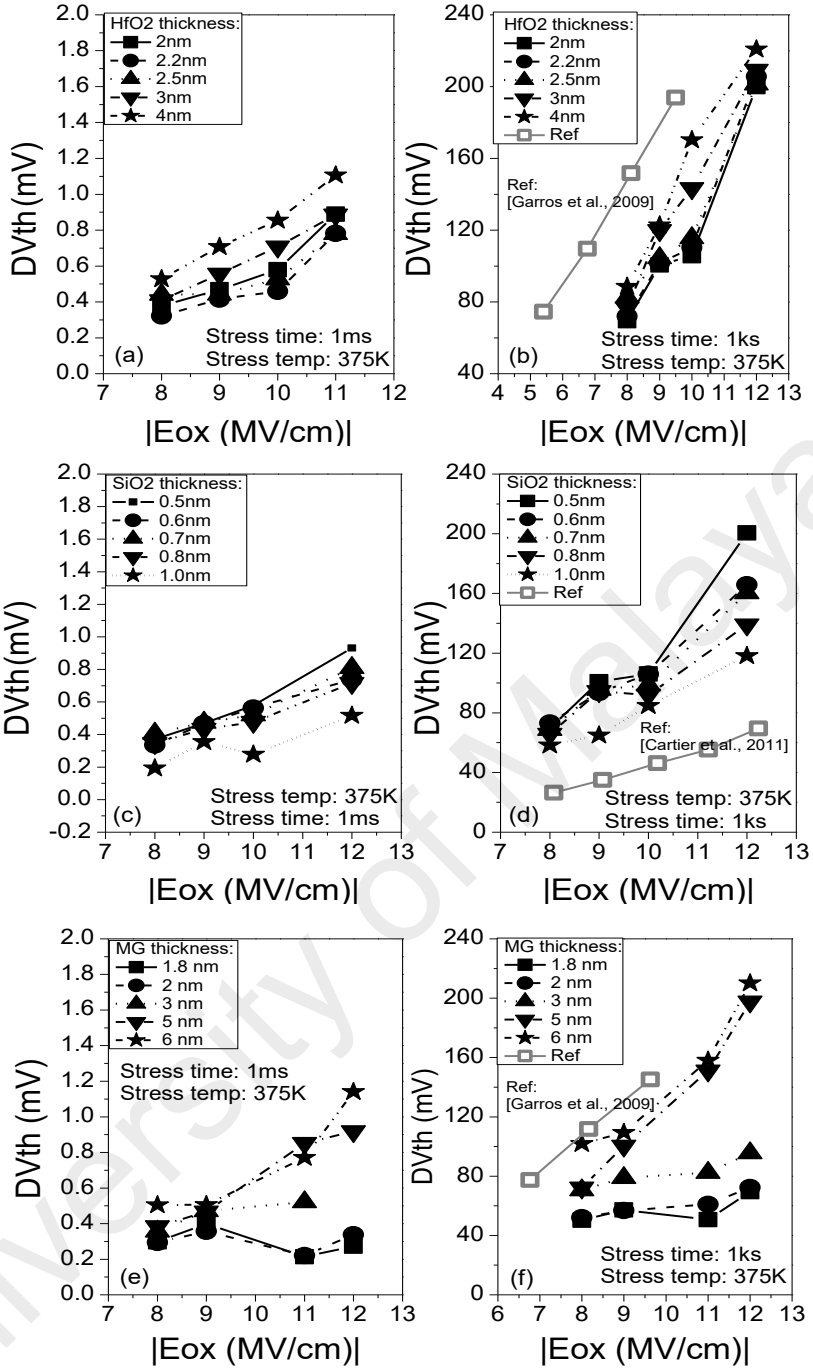

Figure 4.7 Oxide field dependence at 1 millisecond and 1000s stress time subsequent to 375K stress temperature for different (a)-(b) HfO_2 thickness, (c)-(d) SiO_2 thickness and (e)-(f) metal gate thickness.

is substantially increasing as the thickness is reduced for SiO_2 and increased for metal gate. The interface traps creation during NBTI degradation of pure oxides is found to be caused by the oxide field (Huard et al., 2006), and therefore suggest that for the result

obtained in Figure 4.7, more interface traps are created in thinner SiO_2 and thicker metal gate at the higher oxide field compared to lower oxide field.

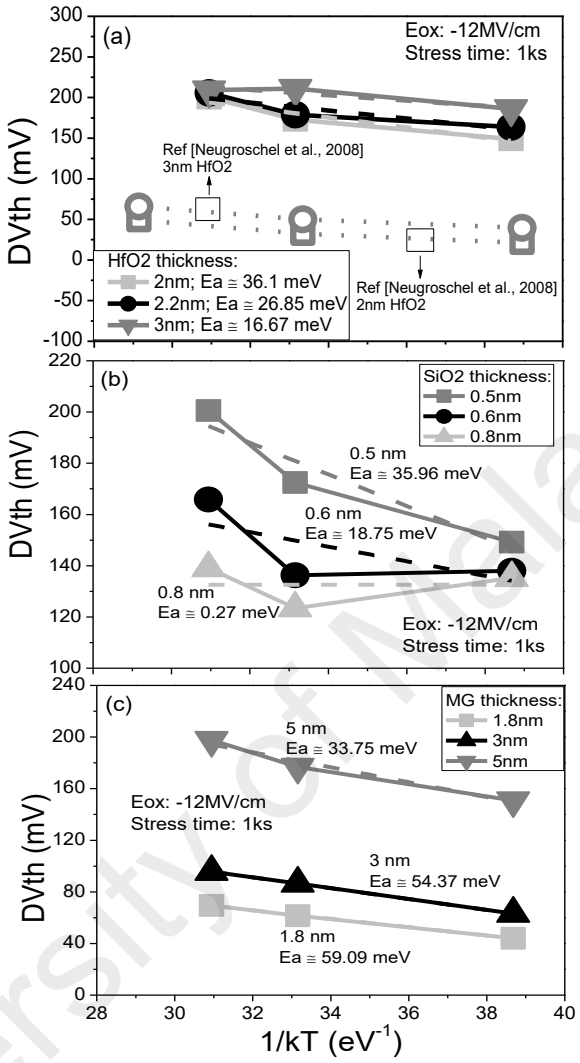

Figure 4.8 Arrhenius plot for various thicknesses of (a) HfO_2, (b) SiO_2 and (c) metal gate.

Arrhenius relation for different HfO_2, SiO_2 IL and metal gate thicknesses as shown in Figure 4.8 were plotted in order to obtain the activation energy (E_a). Figure 4.8 propose that the activation energy is incline to reduce as the thickness is increased which is in good compliance with earlier work (Neugroschel, Bersuker, Choi, & Lee, 2008). Previous studies (Alam & Mahapatra, 2005; Mahapatra et al., 2013) have found that the overall temperature activation reduces due to the presence of hole trapping. The hole trapping volume increases as the thickness of gate stack is increased thus lead to the lowering of

E_a (Mahapatra et al., 2007). Figure 4.9 shows the adjusted V_{th} shift where the fast and slow traps are separated. The fast trap contribution has to be subtracted in order to find the slope conforming to the long-term degradation processes (Neugroschel et al., 2006). Inset shows that the presence of fast

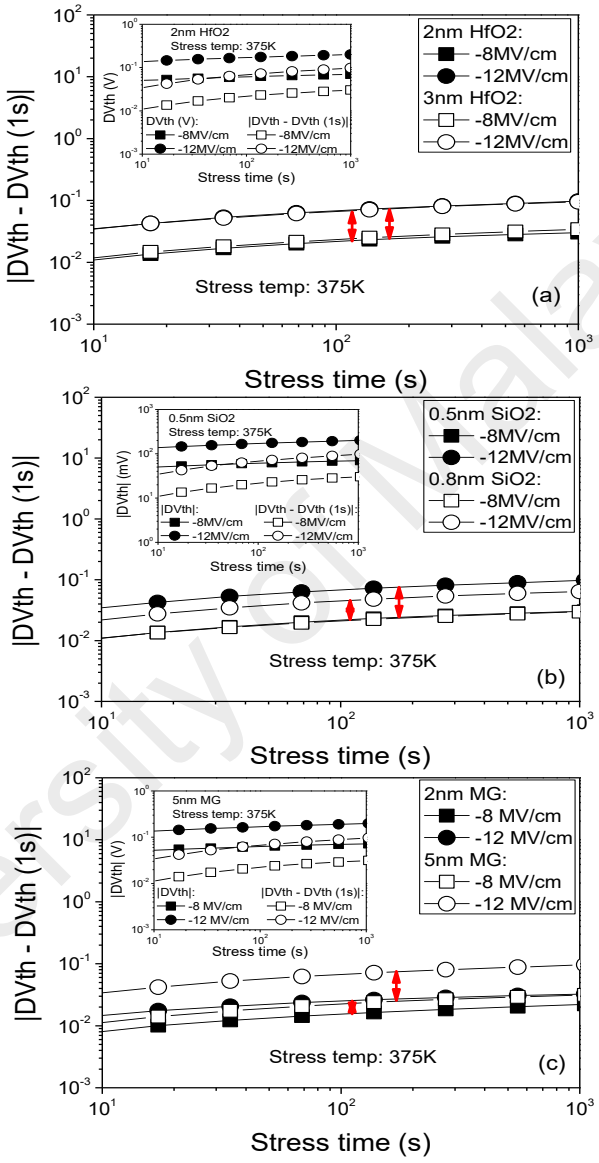

Figure 4.9 Adjusted V_{th} shift for (a) 2 nm and 3 nm HfO_2, (b) 0.5 nm and 0.8 nm SiO_2 IL, and (c) 2 nm and 5 nm metal gate thickness. The insets show the total V_{th} shift compared to $|DV_{th} – DV_{th}(1s)|$.

trap reduces the time dependence of overall NBTI. Figure 4.9 (a) indicates that not much difference in the adjusted V_{th} degradation can be seen between 2 nm and 3nm HfO_2. Figure 4.9 (b) shows the adjusted V_{th} degradation of two different SiO_2 IL thicknesses.

The V_{th} shift difference between 0.5 nm and 0.8 nm SiO_2 seems to be more significant at higher oxide field. Similar observation can be seen for metal gate in Figure 4.9 (c) where the difference in the adjusted V_{th} degradation at higher oxide field is more pronounce than in lower oxide field. These results clearly support the finding as discussed in Figure 4.7 where more slow traps/ interface traps are generated in thinner SiO_2 and thicker metal gate thickness at higher oxide field.

4.2.2.2 Effects of gate length variation on NBTI

Figure 4.10 shows the relationship between the threshold voltage degradation and the gate length at low (-8MV/cm) and high (-14MV/cm) oxide field, E_{ox}. It can be seen that the threshold voltage degradation increases with the decreasing gate length. Since there is no potential difference applied along the channel, it can be concluded that the degradation is not due to the lateral electric field, but may be resulted from the

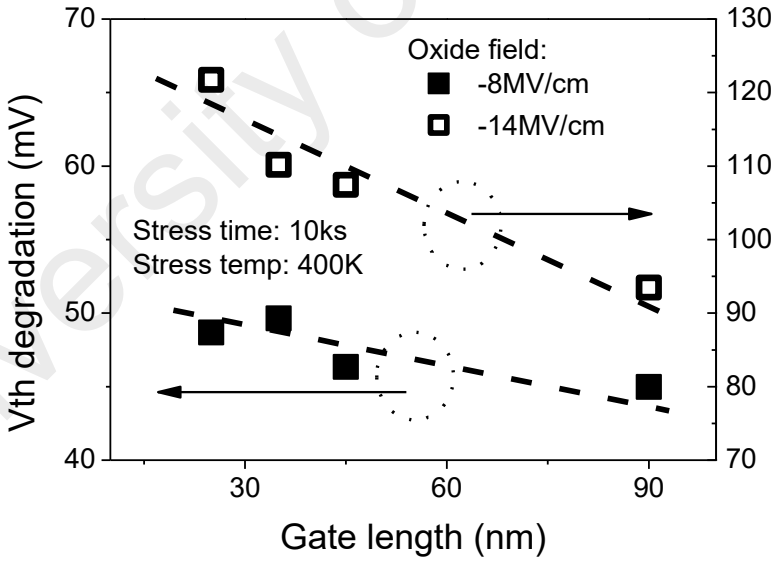

Figure 4.10 Relationship of V_{th} degradation and gate length after NBTI stress under the same NBTI condition.

non-uniform distribution of defects along the channel (Cao et al., 2014). At low E_{ox}, the V_{th} shift is observed to be less sensitive as the gate length is increased. The low sensitivity of gate length towards V_{th} shift at low E_{ox} can be understood by the suppressed defects generation near the gate edge due to the consolidation of fluorine (F) in the HDD structure

(Jin & Xu, 2008). Fluorine is widely known as NBTI suppressor (Inoue et al., 2005). However, at higher E_{ox}, V_{th} degradation dependence of gate length started to show. This might be due to the detrimental effect of boron (Schroder & Babcock, 2003) from BF_2 as higher E_{ox} will enhance boron diffusion into the gate oxide. The result at higher E_{ox} is in agreement with previous studies where the shift in threshold voltage increases with gate length decreasing (Cao et al., 2014; Cellere et al., 2004; Hong-Xia & Yue, 2007; Lin et al., 2003; Lu et al., 2007; Shih, Wang, Ken, Peng, & Yue, 2003).

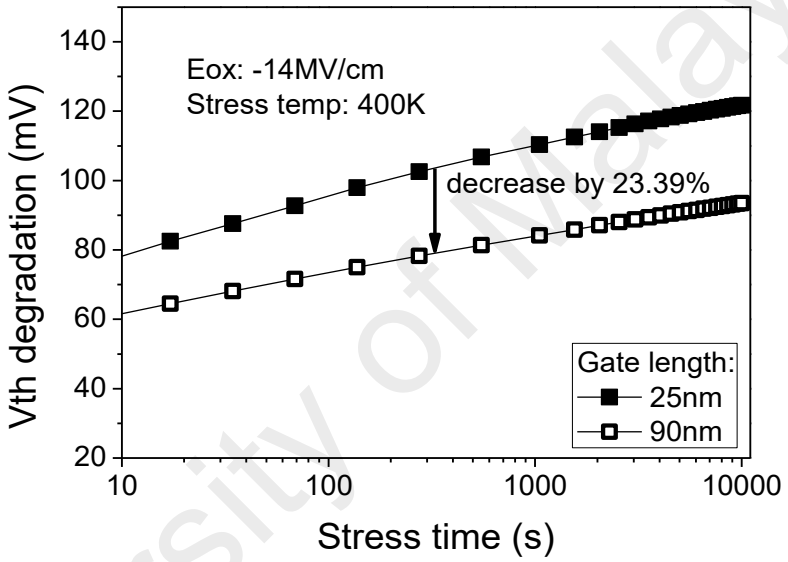

Figure 4.11 V_{th} degradation of short and long gate length under -14MV/cm oxide field at 400K stress temperature.

Figure 4.11 exhibits the threshold voltage degradation for 25 nm and 90 nm gate length subsequent to NBTI stress at -14MV/cm oxide field for 10ks stress time. Longer gate length shows lower V_{th} degradation which is about 23.39% less than the shorter gate length. Figure 4.12 demonstrates the extraction of V_{gop_max} from the lifetime of the device at 10 years. The device's lifetime was obtained from the plot of V_{th} shift as a function of stress time at 50mV. From Figure 4.12, the extrapolated lifetime for all different gate length only show small difference and therefore, it can be concluded that the gate length in nano-scaled pMOSFET does not gives strong impact on NBTI lifetime. As suggested

by (Schroder & Babcock, 2003), NBTI primarily depends on the oxide electric fields (direction from the channel to oxide) and not the lateral electric fields (direction from source to drain). The V_{gop_max} of different gate length is shown in Figure 4.13. The V_{gop_max} is almost similar for all of the different gate length which indicates that the gate length in 32 nm advanced technology PMOS gives negligible impact on NBTI lifetime.

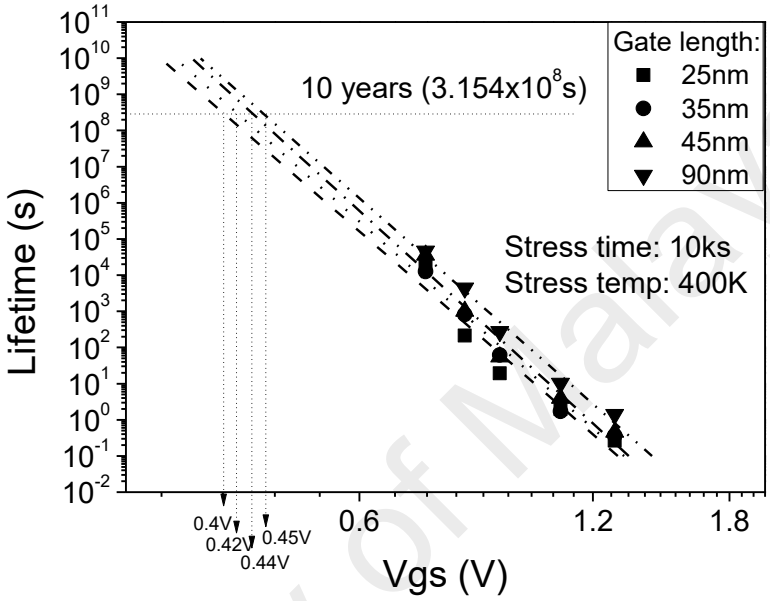

Figure 4.12 Effect of gate length on NBTI lifetime prediction.

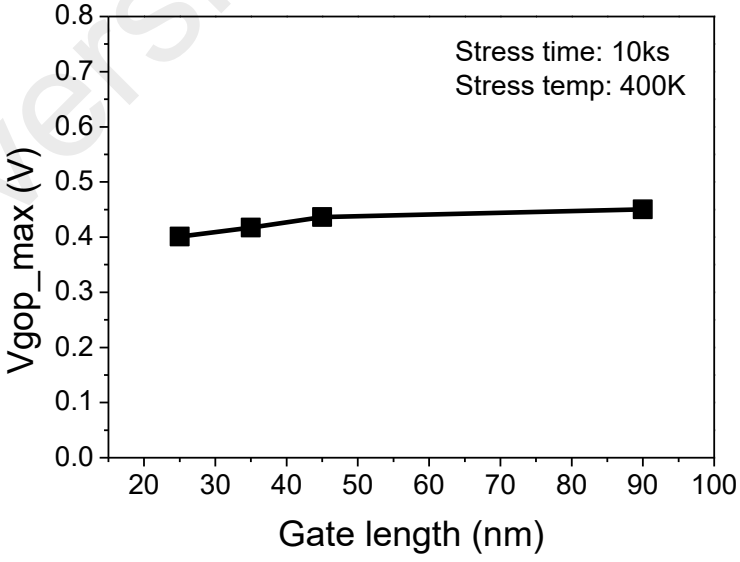

Figure 4.13 Extracted V_{gop_max} vs gate length.

4.2.2.3 Effects of advanced geometrical features variation on NBTI

In order to further investigate the influence of geometric considerations on NBTI, additional advanced geometrical features which consist of polypitch, spacer length and SiGe pocket depth are varied. Figure 4.14 depicts stress temperature dependency of different polypitch, spacer length and SiGe pocket depth. Smaller polypitch and spacer

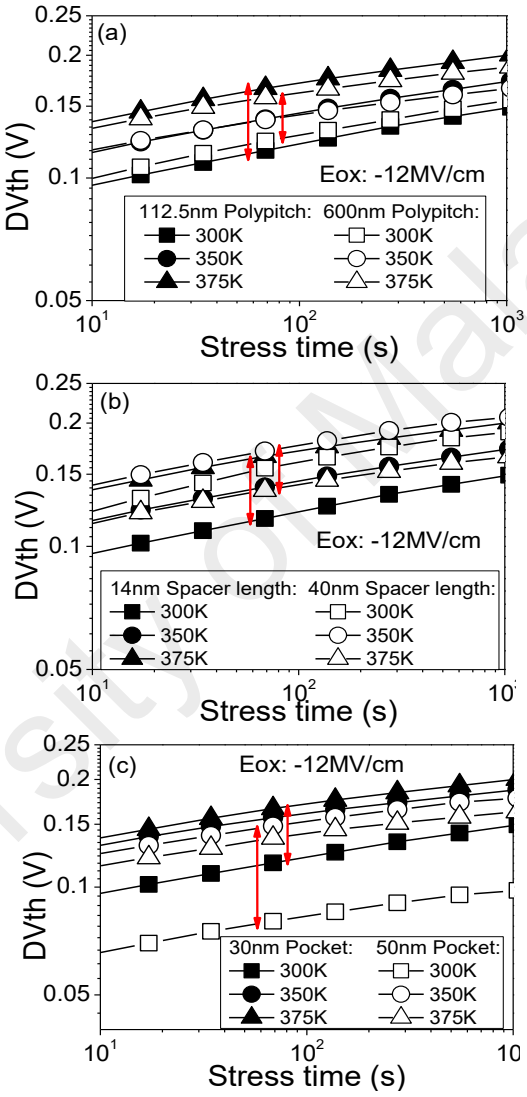

Figure 4.14 V_{th} degradation of (a) 112.5 nm and 600 nm polypitch, (b) 14 nm and 40 nm spacer length and (c) 30 nm and 50 nm SiGe pocket depth subsequent to 300K, 350K and 375K stress temperatures.

length shows higher sensitivity towards temperature, which is in contrast with SiGe pocket depth such that the larger SiGe pocket depth seems to be more susceptible to temperature. In the literature, it is reported that the channel stress is aggravated with polypitch scaling (Alam et al., 2012). The scaling of spacer length as well as SiGe pocket

depth could also contribute to the channel stress. Higher channel stress is caused by the reduction of the spacer length while the reduction of SiGe pocket depth will lead to the stress in the channel to decrease (Rodriguez et al., 2011). Channel stress causes the enhancement of hole tunneling probability thus making the Si-H bonds at the Si-SiO_2 interface become easier to break, creating more interface traps (Gong, Liu, & Yeo, 2013; Irisawa et al., 2007). Interface traps are sensitive towards temperature (Lee, Wu, Islam, Alam, & Oates, 2008) and the temperature sensitivity can be observed from the plots in Figure 4.14.

4.2.3 Influence on process considerations on NBTI

In addition to the geometric considerations, influence of process design considerations on NBTI have also been investigated by varying boron doses of the highly doped drain (HDD), changing the metal gate work function of the device and by varying halo doping concentration. Boron is broadly known to be the enhancer for NBTI degradation due to the easiness of boron penetration into the gate oxide (Schroder & Babcock, 2003). The increase in initial density of electrically activated defects at Si/SiO_2 near channel edges can be due to the boron diffusion from HDD region into the gate oxide (Djezzar, Tahi, Benabdelmoumene, & Chenouf, 2013). The threshold voltage degradation over stress time at 300K, 350K and 375K by varying HDD boron dose shown in Figure 4.15 is in compliance with previous study where the higher boron dose is observed to cause higher V_{th} degradation (Yamamoto, Uwasawa, & Mogami, 1999).

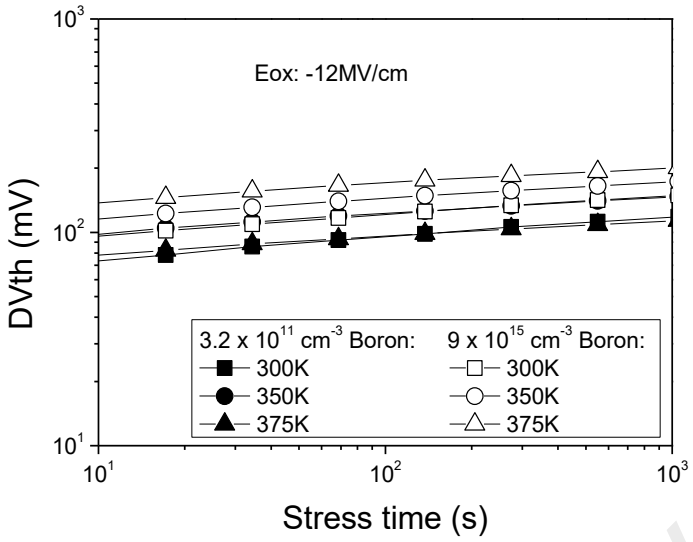

Figure 4.15 V_{th} degradation of HDD boron dose variation subsequent to 300K, 350K and 375K stress temperatures.

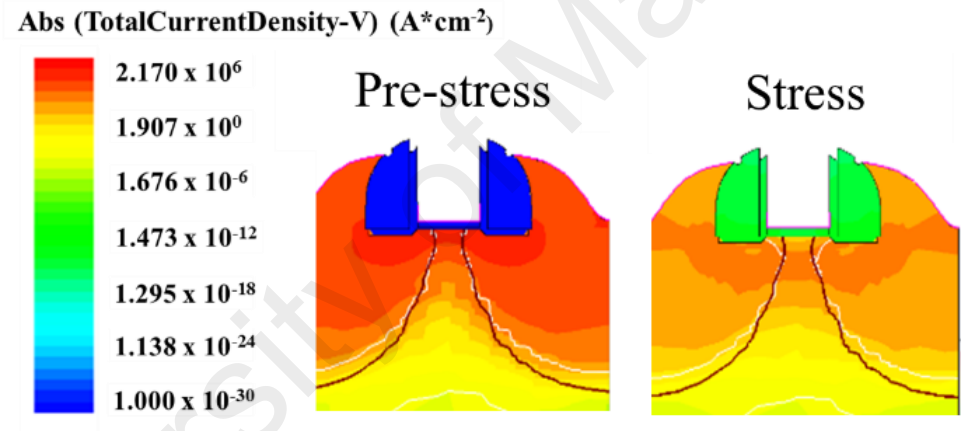

Figure 4.16 Total current density at 375K stress temperature for a device with metal gate work function of 3.0 eV (left: pre-stress ≈ -2.5MV/cm and right: stress at -12MV/cm).

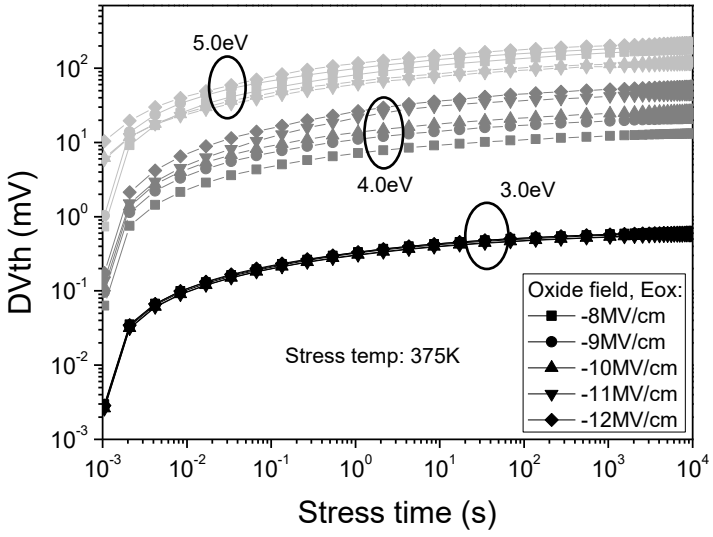

Figure 4.17 V_{th} degradation at 375K stress temperature with -12MV/cm oxide field for device with different metal gate work function.

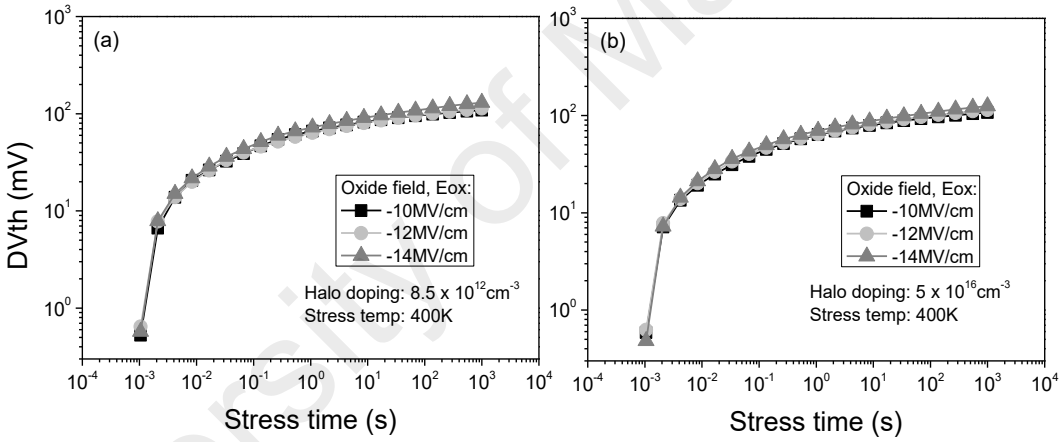

Figure 4.18 V_{th} degradation of PMOS device by varying halo doping (a) 8.5 x 10^{12} cm^{-3} (b) 5 x 10^{16} cm^{-3} at stress temperature of 400K for 1000s.

Figure 4.16 demonstrates the total current density of a device with metal gate work function of 3.0 eV stressed under -12MV/cm oxide field at 375K stress temperature. It can be clearly seen that the total current density deteriorates after the device was stressed for 1000s. The total current density in the channel is reduced by 64.15% after stress. The threshold voltage degradation obtained by varying metal gate work function is shown in Figure 4.17. It is found that higher metal gate work function has resulted in higher V_{th} degradation. The trapped electrons in HfO_2 that discharge to the substrate when the IL is thin causes V_{th} degradation to increase and this problem is severe for high metal gate

work function where more trapped electrons are free to discharge to the substrate as their energies are above the equilibrium fermi level (Schaeffer et al., 2007).

Figure 4.18 shows the V_{th} degradation of PMOS device by varying 8.5 x 10^{12} cm^{-3} and 5 x 10^{16} cm^{-3} halo doping at 400K stress temperature for 1000s. The finding reveals that the threshold voltage degradation shows no critical change by varying halo doping. This may be due to the halo structure which is slightly far from the SiO_2 bulk interface where most of the defects are located at (Zhang et al., 2008).

4.3 HCI analysis on n-channel STI LDMOS technology

4.3.1 Influence of geometric considerations on HCI

4.3.1.1 Variation of shallow trench isolation (STI) angle

Figure 4.19 shows the effect of different STI angle and temperature on I_d-V_g. The device was stressed under 300K and 400K temperature and it is observed that the drain current degrades with high stress temperature. LDMOS is eminently susceptible to temperature variation as high temperature will change the device behavior and consequently causes permanent degradation to the performance of the device (Belaïd et al., 2005). Smaller STI angle shows better current performance compared to the larger STI angle. From the result obtained, it is found that the drain current for device with 100^0 STI angle is reduced by 58.78% compared to device with 45^0 STI angle. The effect of different STI angle and stress temperature on I_{dsat} degradation (ΔI_{dsat}) is presented in Figure 4.20 where the I_{dsat} degradation is observed to be worse for the device with larger STI angle.

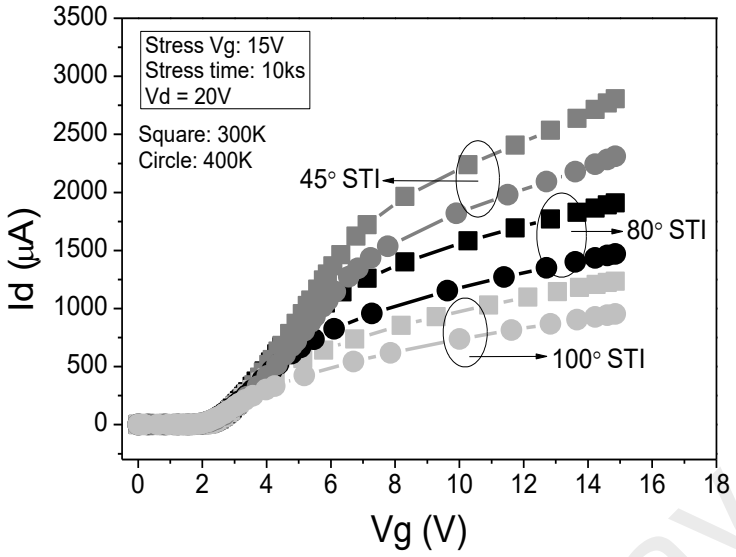

Figure 4.19 Effect of different STI angle and stress temperature on I_d-V_g curve.

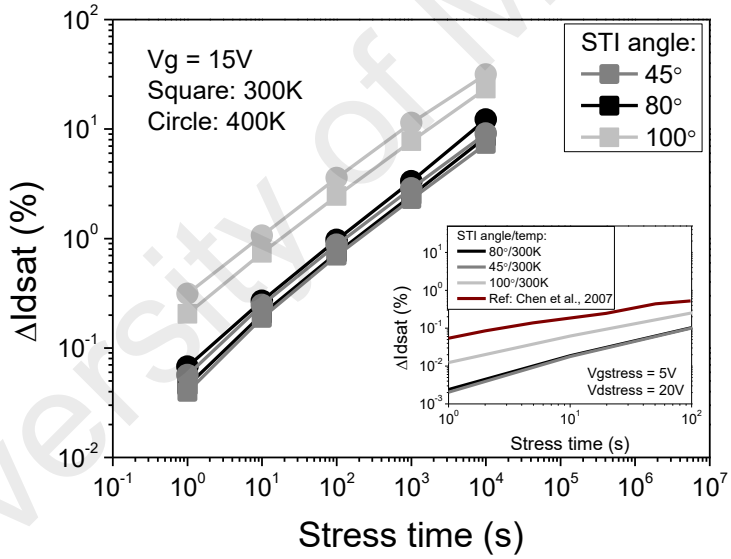

Figure 4.20 Effect of different STI angle and stress temperature on I_{dsat} degradation (ΔI_{dsat}). The inset shows that the trend of the results follows (Chen et al., 2007).

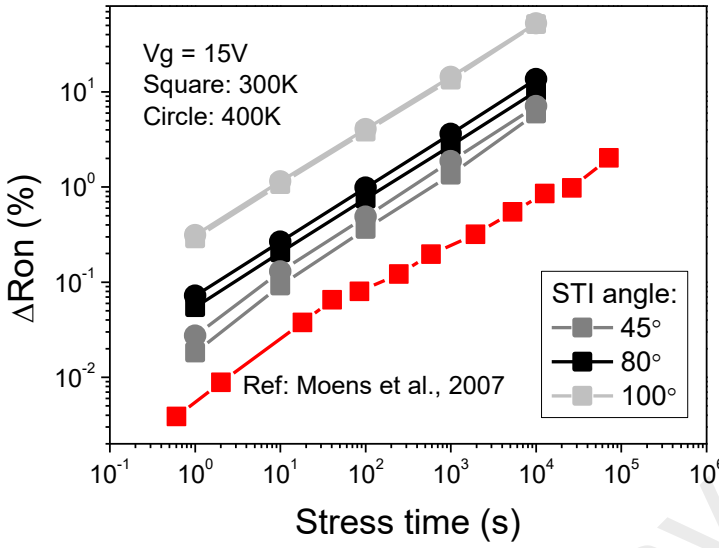

Figure 4.21 R_{on} degradation (ΔR_{on}) for different STI angle at 300K and 400K stress temperature. The trend of the results follows (Moens et al., 2007).

Figure 4.21 presents the R_{on} degradation (ΔR_{on}) as a function of stress time for the devices with different STI angles stressed under 300K and 400K stress temperature. It is observed that reducing the STI angle causes R_{on} degradation to decrease. Analysis on impact ionization are discussed in order to investigate the mechanism of R_{on} degradation due to variation of STI angle. It is well known that the hot carriers with high kinetic energy induced by high electric field can generate electron-hole pairs through impact ionization. Therefore, this section will look into the effect of STI angle variation on impact ionization in order to access the mechanism behind the device degradation. Figure 4.22 shows the 2D impact ionization generation rate distribution of 45^0, 80^0 and 100^0 STI angle at 400K stress temperature for 10ks stress time. The hot carrier stress creates damage bounded near the drain junction region due to the high electric field in that particular region. As a result, carriers are found to be the hottest in that region (Mistry & Doyle, 1995; Wu, Chen, Su, Lee, Lin, Shih, et al., 2006).

From Figure 4.22, it is observed that smaller STI angle shows less impact ionization generation peak at the STI bottom-left corner compared to the larger angle. Larger STI angle causes the effective accumulation length, L_a (poly gate and n-drift region overlap

size) to reduce, resulting current crowding effect to become worse, and subsequently increases the electric field magnitude which deteriorate the performance of the device.

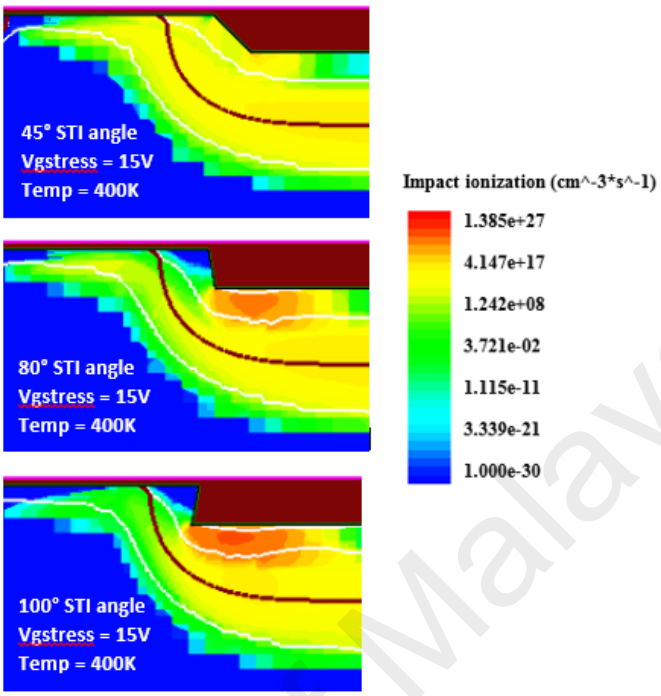

Figure 4.22 2D impact ionization generation rate distribution of 45°, 80° and 100° STI angle at 400K stress temperature for 10ks stress time.

Figure 4.23 depicts the interface trap concentration at the STI bottom-left corner of different STI angle at 300K and 400K temperature. The result shows that the interface trap concentration is higher at high temperature and larger STI angle. The shorter effective L_a of larger STI angle causes the current to flow very close to the STI interface, where both high current density and high electric field at the interface will lead to trap formation (Reggiani et al., 2010). Due to that, high interface trap concentration is observed for the device with short effective L_a (large STI angle) as shown in Figure 4.23.

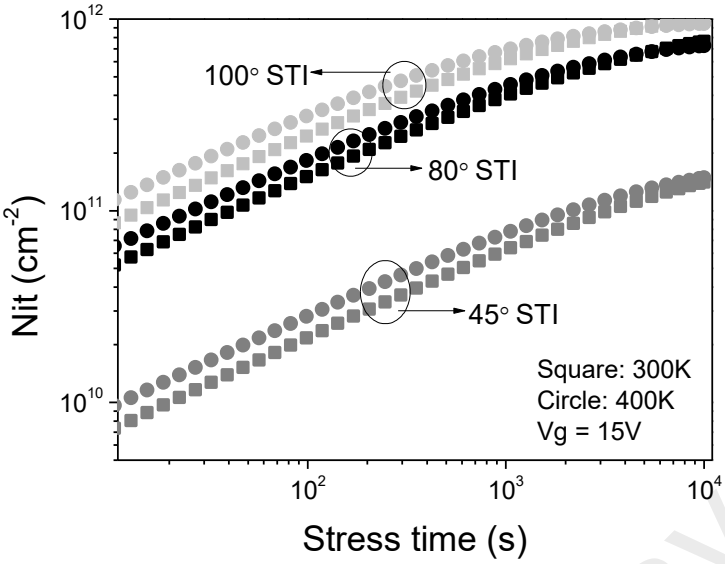

Figure 4.23 Interface traps for different STI angle at 300K and 400K stress temperature.

4.3.1.2 Variation of shallow trench isolation (STI) depth

The effect of different STI depth and temperature on I_d-V_g and I_d-V_d curve is presented in Figure 4.24. It is clear that the drain current degrades with high temperature. Lower STI depth shows better current performance compared to the larger STI depth. There is a very small difference in the degradation of saturation current (ΔI_{dsat}) of the devices with different STI depth, as shown in the inset of Figure 4.24 (b). It can be noted that degradation of I_{dsat} increases slightly as the STI depth is reduced.

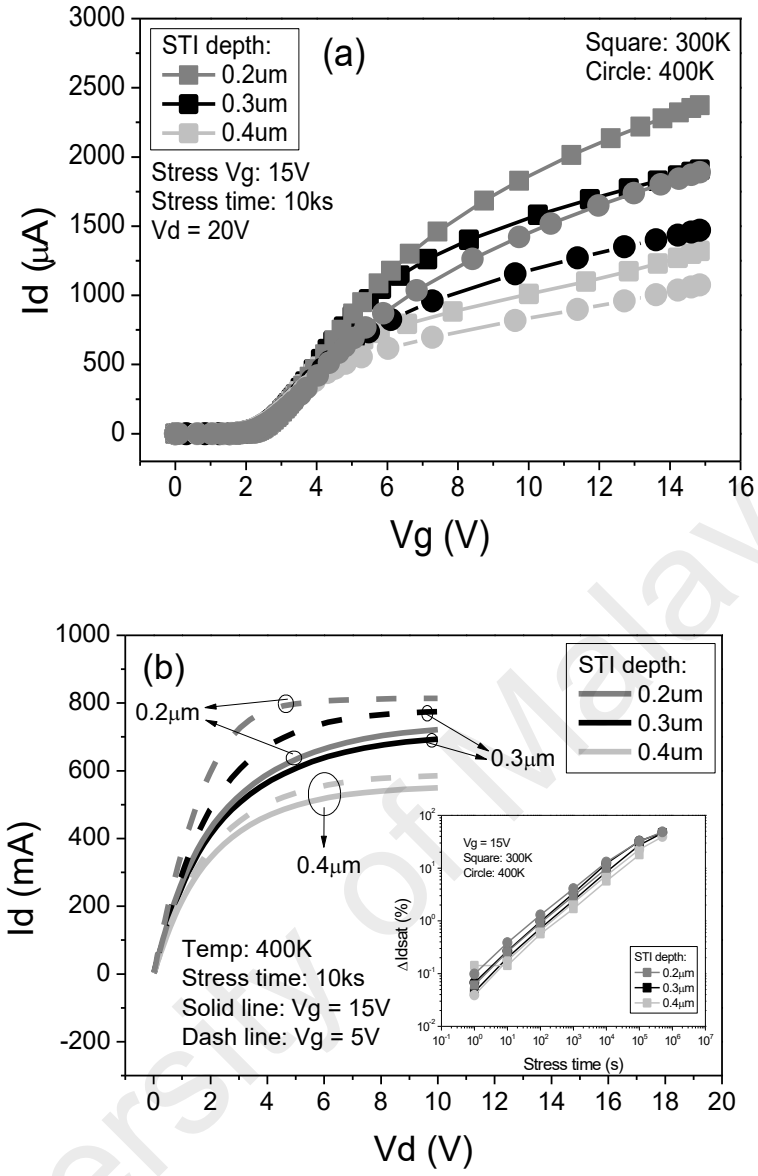

Figure 4.24 Effect of different STI depth and temperature on (a) I_d-V_g and (b) I_d-V_d curve.

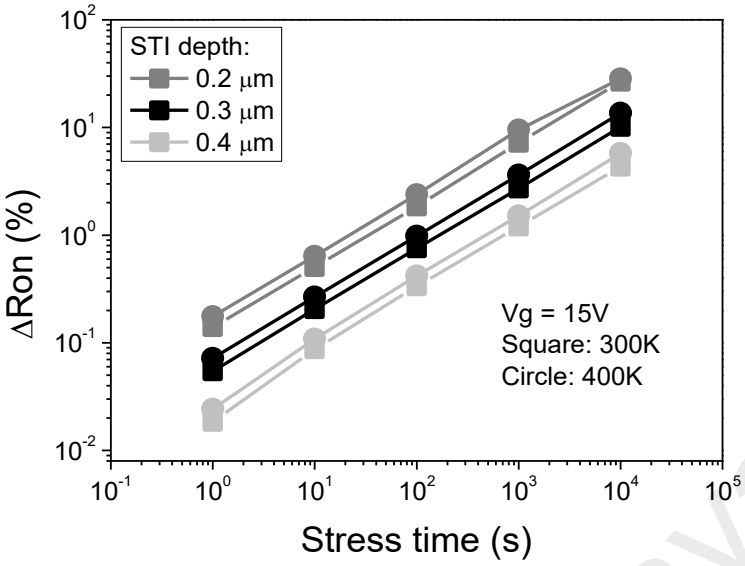

Figure 4.25 R_{on} degradation for different STI depth at 300K and 400K stress temperature.

Figure 4.25 depicts the R_{on} degradation (ΔR_{on}) as a function of stress time for the devices with different STI depth stressed under 300K and 400K stress temperature. Though smaller STI depth gives better I_d performance, it is observed that reducing the STI depth causes R_{on} degradation to increase. To investigate the mechanism of R_{on} degradation of devices with different STI depth, the impact ionization rate distribution is extracted as shown in Figure 4.26. It can be clearly seen that the highest damage created is at the STI bottom-left corner. The damage created at this location reduces as the STI depth is increased. The thicker STI causes the destructive electric field to move further away from the gate surface, thus resulted in the reduction of potential crowding at the body surface (Son, Kim, Sohn, & Choi, 2004; Zhu, Khemka, Bose, & Roggenbauer, 2006).

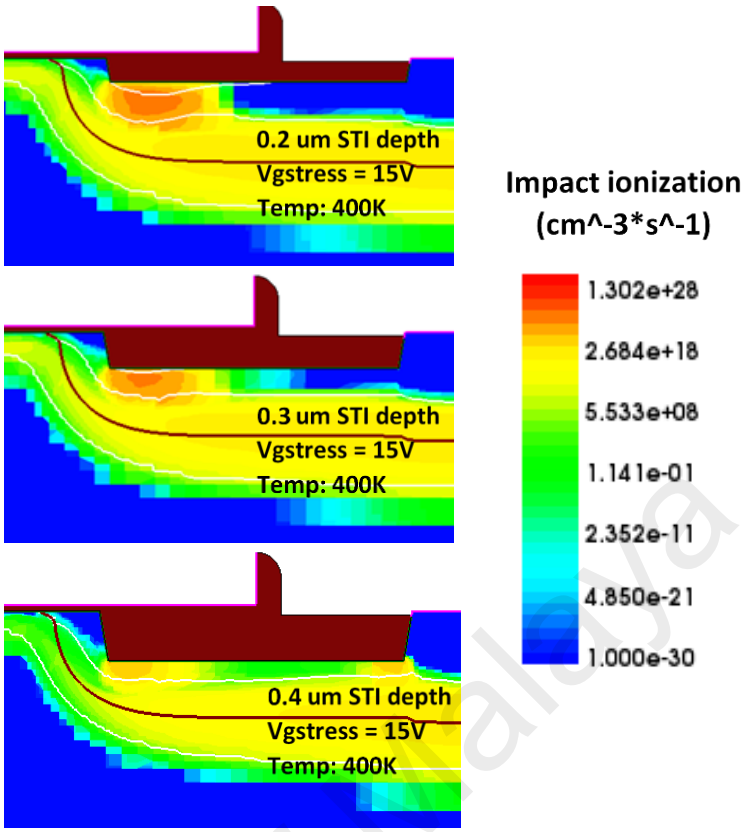

Figure 4.26 2D impact ionization generation rate distribution of 0.2 µm, 0.3 µm and 0.4 µm STI depth at 400K stress temperature for 10ks stress time.

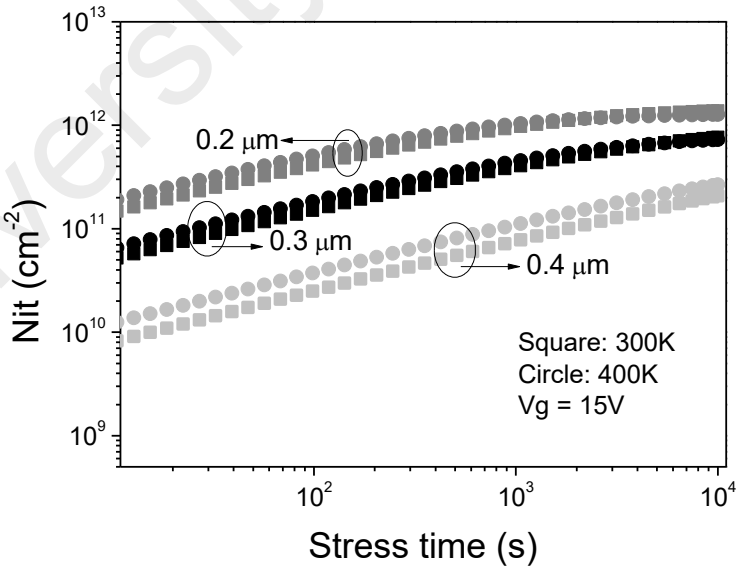

Figure 4.27 Interface traps at the STI bottom-left corner of different STI depth at 300K and 400K stress temperature.

Figure 4.27 shows the interface trap concentration located at the STI bottom-left corner for different STI depth at 300K and 400K temperature. The result shows that the interface trap concentration is higher at high temperature and smaller STI depth. High interface trap concentration for smaller STI depth is caused by the high rate of impact ionization occurred at this location, as shown in Figure 4.26.

4.3.1.3 Variation of gate oxide thickness

The influence of gate oxide thickness on STI-based LDMOS devices can be observed from the I_d-V_d curve presented in Figure 4.28. Drain current is reduced for larger gate oxide thickness. There is a very small effect of the variation of gate oxide thickness on R_{on} degradation (Figure 4.29) where the smaller gate oxide thickness causes slightly higher R_{on} degradation. Figure 4.30 shows the effect of different gate oxide thickness on I_{dsat} degradation. Smaller gate oxide thickness shows enhanced I_{dsat} degradation.

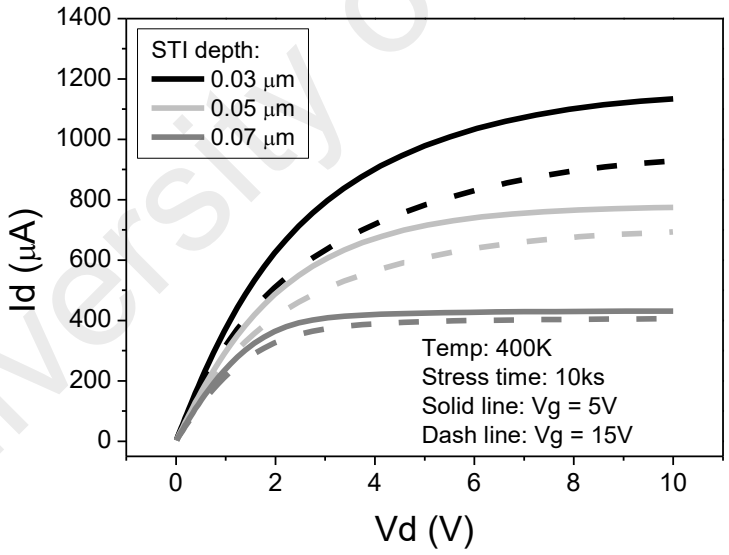

Figure 4.28 Effect of different gate oxide thickness on I_d-V_d curve.

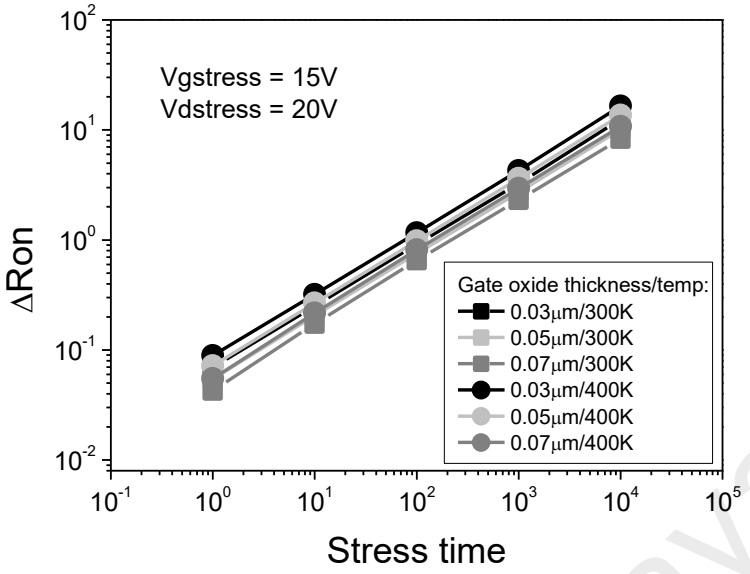

Figure 4.29 R_{on} degradation for different gate oxide thickness at 300K and 400K stress temperature.

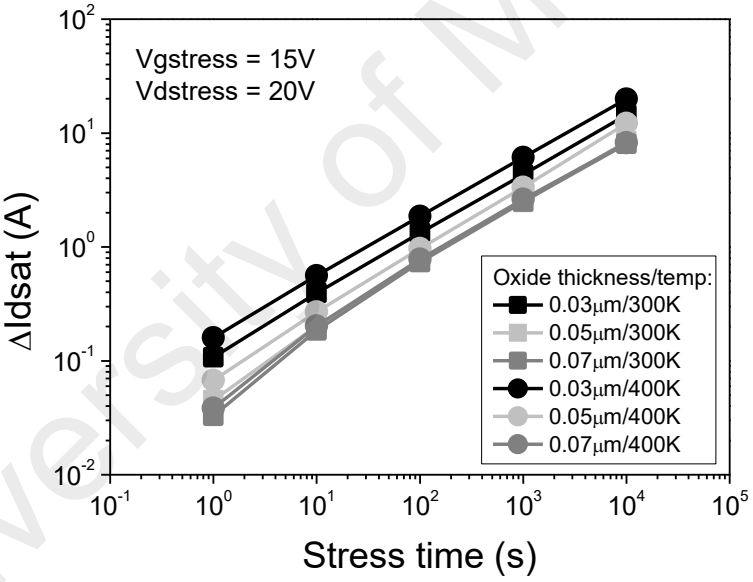

Figure 4.30 Effect of different gate oxide thickness and stress temperature on I_{dsat} degradation.

Figure 4.31 illustrates the 2D impact ionization generation rate distribution of 0.03 μm, 0.05 μm and 0.07 μm gate oxide thickness at 400K stress temperature for 10ks stress time. It is observed that smaller gate oxide thickness shows higher impact ionization generation peak at the STI bottom-left corner compared to the larger thickness. Higher impact ionization in smaller gate oxide causes higher interface traps concentration as

shown in Figure 4.32, and therefore giving rise to the R_{on} degradation as observed in Figure 4.29. Smaller gate oxide causes the current density to increased and therefore, increasing the generation of impact ionization (Chiu, 2014).

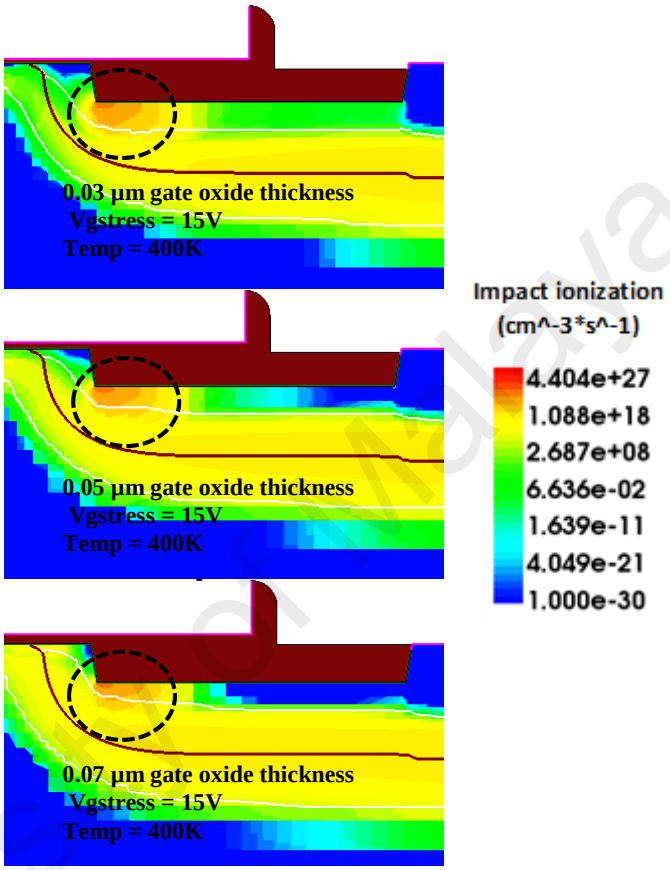

Figure 4.31 2D impact ionization generation rate distribution of 0.03 µm, 0.05 µm and 0.07 µm gate oxide thickness at 400K stress temperature for 10ks stress time.

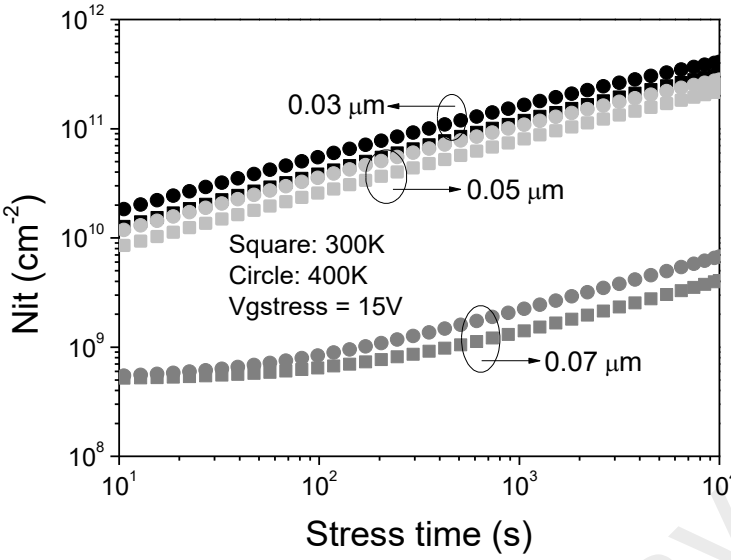

Figure 4.32 Interface traps at the STI bottom-left corner of different gate oxide thickness at 300K and 400K stress temperature.

4.3.2 Influence of process considerations on HCI

4.3.2.1 Variation of p-substrate doping

The effect of different p-substrate doping concentration and temperature on I_d-V_g and I_d-V_d curve is presented in Figure 4.33 and Figure 4.34. The drain current is observed to degrade with high temperature. Lower p-substrate doping concentration shows better current performance compared to the higher p-substrate doping. R_{on} degradation for different p-substrate doping concentration at 300K and 400K stress temperature is shown in Figure 4.35. Higher p-substrate doping concentration is observed to exhibit higher R_{on} degradation compared to the lower.

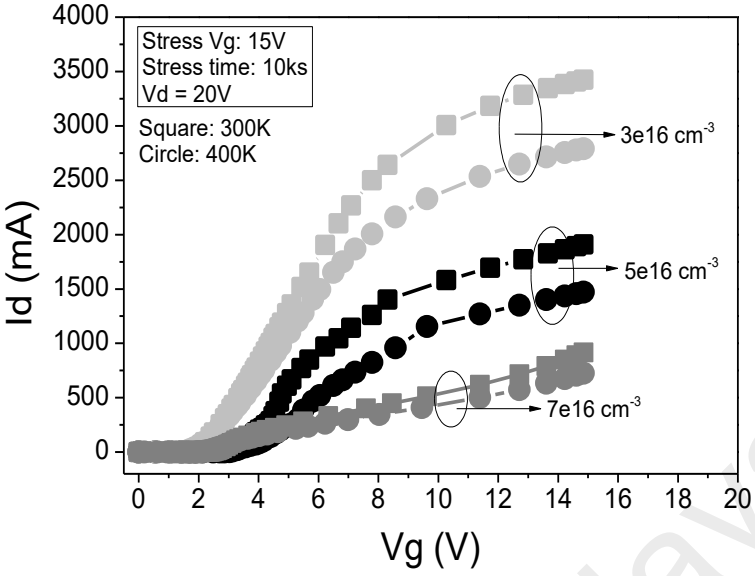

Figure 4.33 Effect of different p-substrate doping concentration and temperature on I_d-V_g

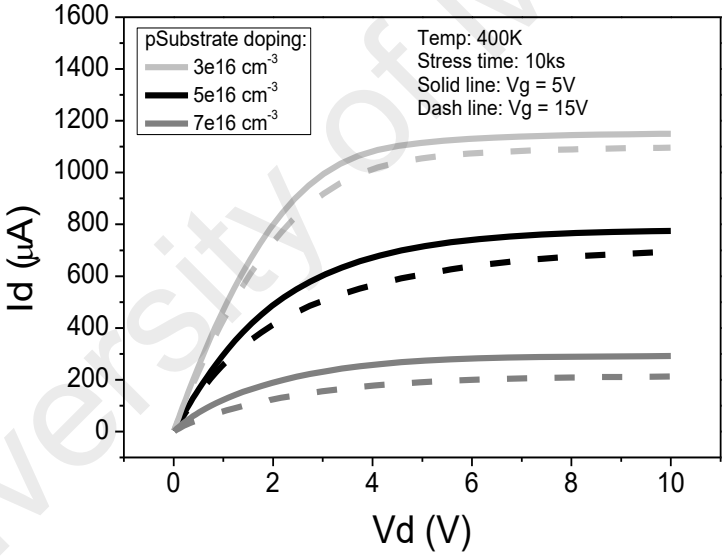

Figure 4.34 Effect of different p-substrate doping concentration on I_d-V_d curve.

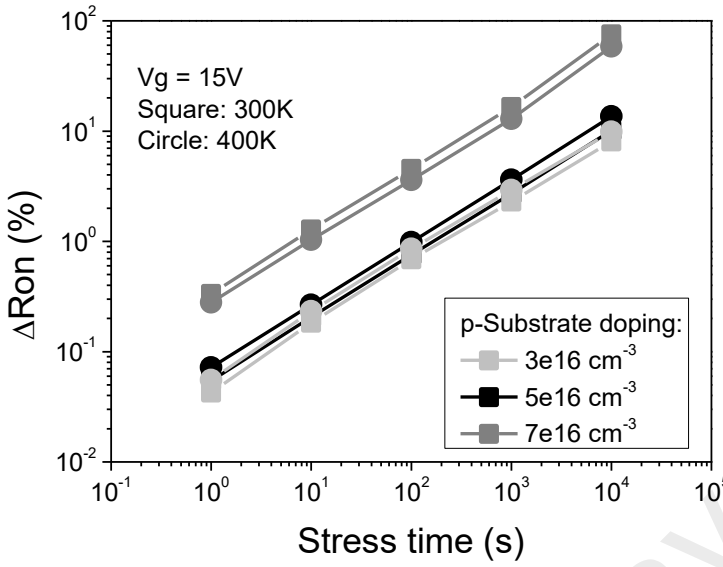

Figure 4.35 R_{on} degradation for different p-substrate doping concentration at 300K and 400K stress temperature.

Figure 4.36 depicts the 2D impact ionization generation rate distribution of $3x10^{16}$ cm^{-3}, $5x10^{16}$ cm^{-3} and $7x10^{16}$ cm^{-3} p-substrate doping at 400K stress temperature for 10ks stress time. From the figure, it is observed that the peak of impact ionization occurs at two location for the higher p-substrate concentration. The depletion region width is observed to reduce with doping concentration and therefore, allowing more electrons to be injected easily. Figure 4.37 shows the interface trap concentration at the STI bottom-left corner of different p-substrate doping at 300K and 400K temperature. The result shows that the interface trap concentration is higher at high temperature and larger p-substrate doping.

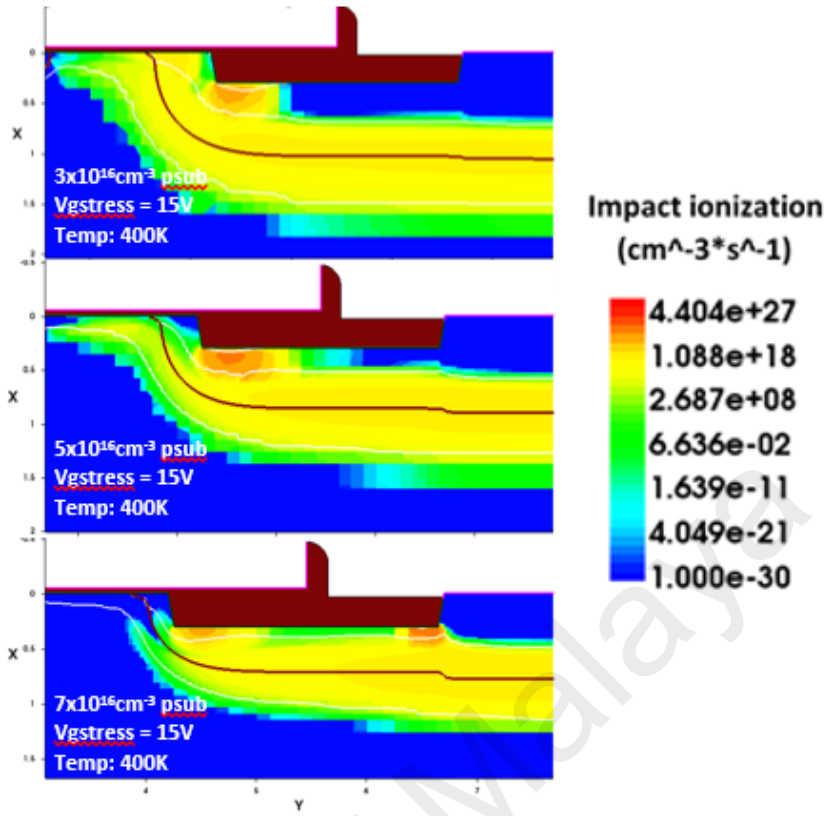

Figure 4.36 2D impact ionization generation rate distribution of $3x10^{16}$ cm^{-3}, $5x10^{16}$ cm^{-3} and $7x10^{16}$ cm^{-3} p-substrate doping at 400K stress temperature for 10ks stress time.

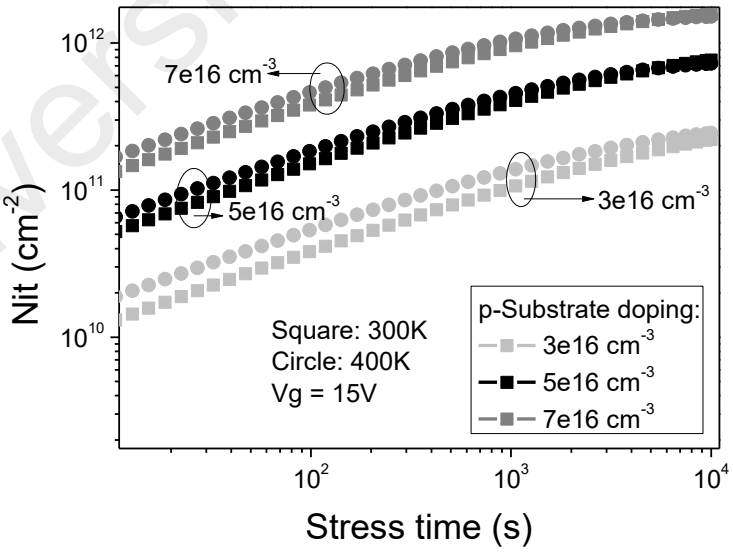

Figure 4.37 Interface traps at the STI bottom-left corner of different p-substrate doping at 300K and 400K stress temperature.

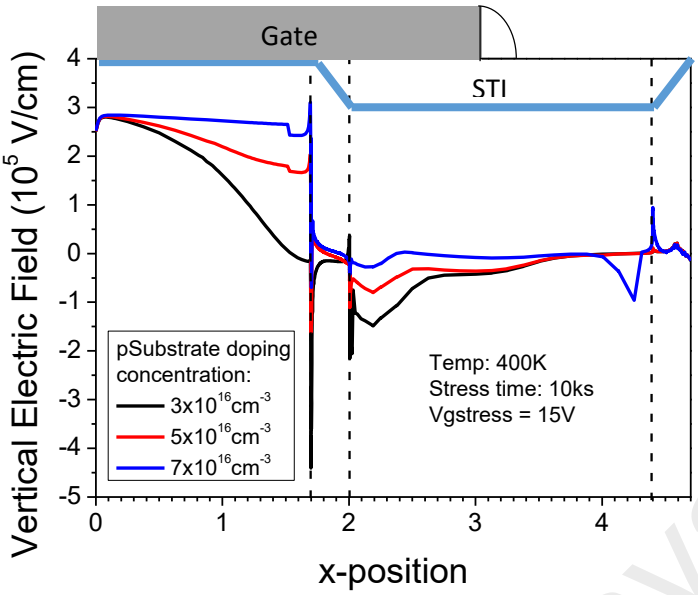

Figure 4.38 Electric field along Si/SiO2 interface under Vgstress = 15V for different p-substrate doping at 400K stress temperature.

Figure 4.38 shows the vertical electric field (E_y) along Si/SiO_2 interface for devices with different p-substrate doping. The direction of E_y pointing downward is signifies by positive E_y while negative E_y indicates the vice versa. Positive E_y is favourable for electron injection and negative E_y is favourable for hole injection (Chen, Tian, Chen, Wu, & Liu, 2008). From Figure 4.38, electrons are injected into STI (positive E_y) at the STI bottom-left corner, creating electron trapping and interface trap where trapping of electrons in STI will result in the increment of of R_{on}. Larger p-substrate concentration is observed to have higher positive E_y, hence resulted in a poor I_{dsat} and R_{on} performance.

4.3.2.2 Variation of Source/Drain (S/D) implantation dose

The effect of different Source/Drain (S/D) implantation dose and stress temperature on I_d-V_d curve is shown in Figure 4.39. The I_d-V_d curve for different S/D implantation dose shows very small difference as the dose is varied. Figure 4.40 and Figure 4.41 shows that the R_{on} and I_{dsat} degradation are not affected by the S/D implantation dose.

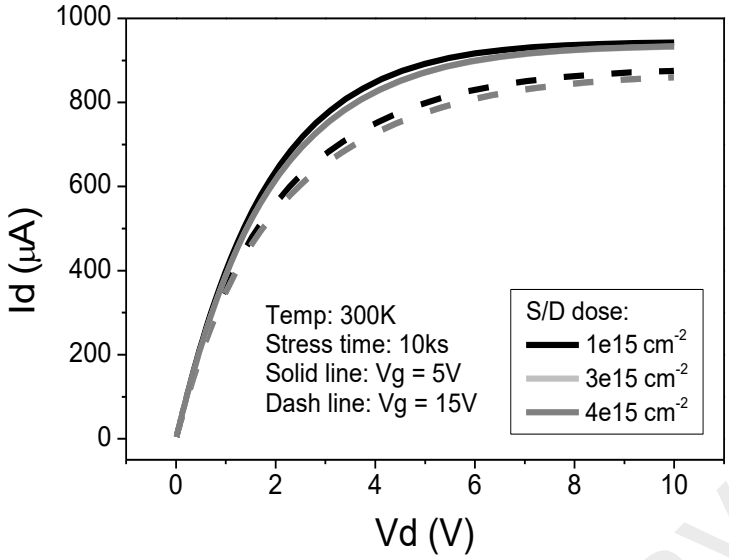

Figure 4.39 Effect of different S/D implantation dose on I_d-V_d curve.

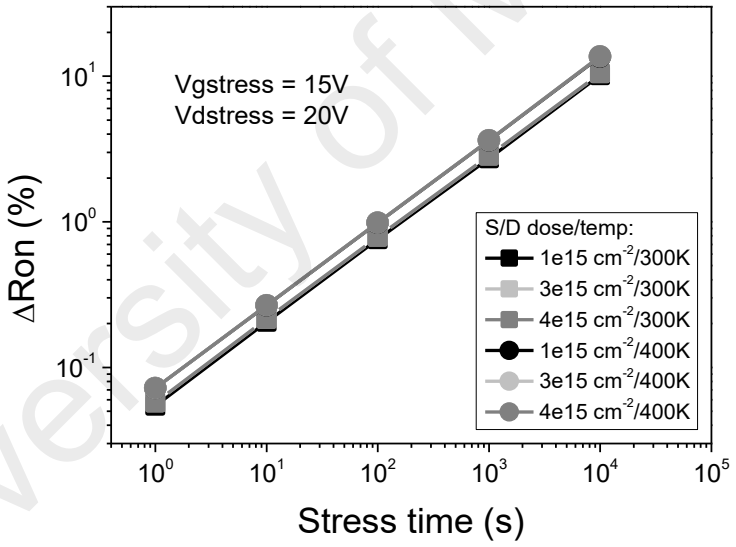

Figure 4.40 R_{on} degradation for different S/D implantation dose at 300K and 400K stress temperature.

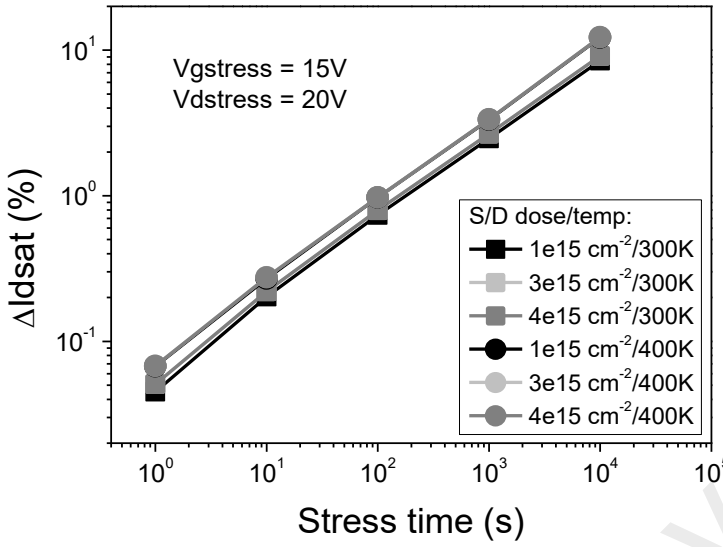

Figure 4.41 Effect of different S/D implantation dose and stress temperature on I_{dsat} degradation.

The impact ionization generation rate distribution of $1x10^{15}$ cm^{-2}, $3x10^{15}$ cm^{-2} and $4x10^{15}$ cm^{-2} S/D implantation dose at 400K stress temperature for 10ks stress time presented in Figure 4.42 shows that there is no significant difference in the impact ionization rate for different S/D doses. The interface states concentration in Figure 4.43 agrees well with the finding where S/D implantation dose does not influence the HCI degradation in STI-based LDMOS devices.

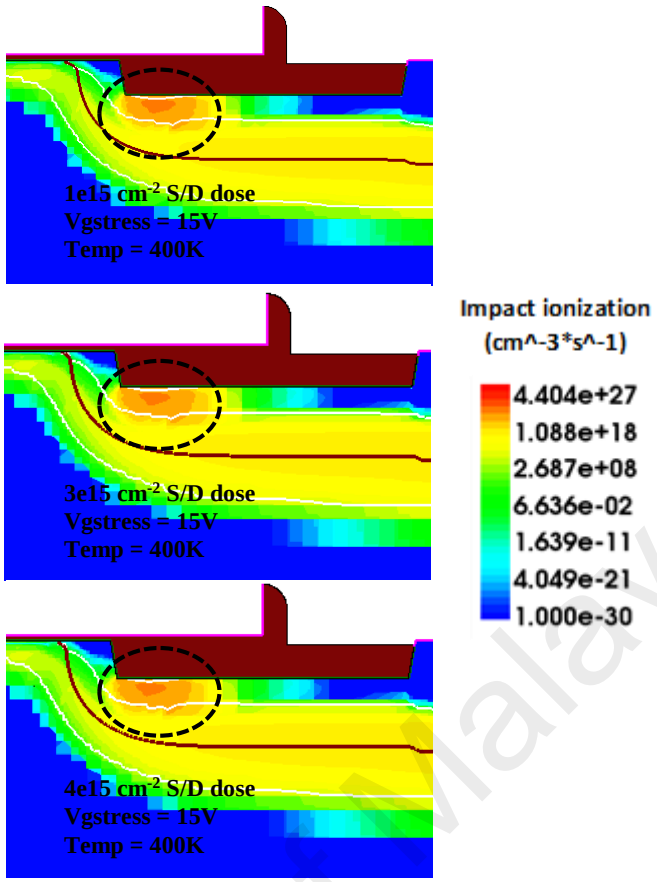

Figure 4.42 2D impact ionization generation rate distribution of $1x10^{15}$ cm^{-2}, $3x10^{15}$ cm^{-2} and $4x10^{15}$ cm^{-2} S/D implantation dose at 400K stress temperature for 10ks stress time.

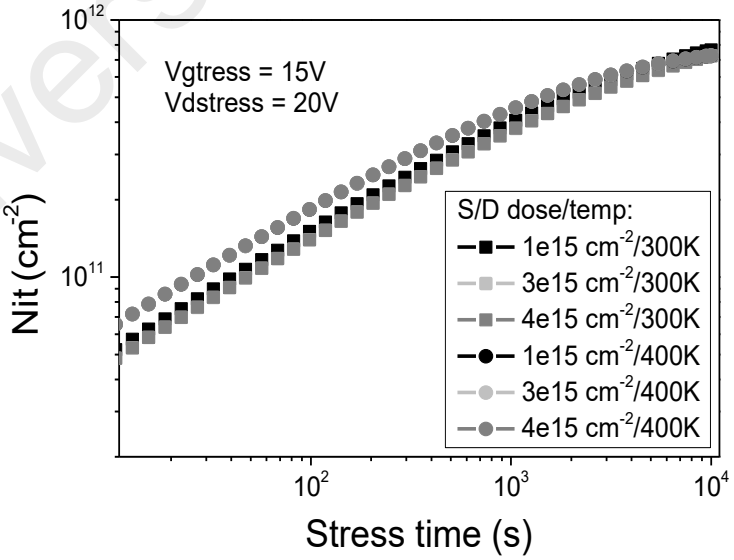

Figure 4.43 Interface traps at the STI bottom-left corner of different S/D implantation dose at 300K and 400K stress temperature.

4.4 Summary

The device reliability performance of advanced-process MOSFETs were investigated in this chapter, where degradation analysis on high-k metal gate pMOSFET and shallow trench isolation (STI) based nLDMOS were thoroughly studied. The study facilitates researchers to attain detailed understanding on the underlying physics of defects in the device and give an insight of design considerations impact on critical reliability performance parameters which includes threshold voltage (V_{th}), interface traps ($N_{it)}$, on-resistance (R_{on}), impact ionization rate, etc. The degradation behavior on parametric design considerations are summarized in the table as follows:

Table 4.1 Summary of NBTI analysis (↓ = decreasing, ↑ = increasing)

Design considerations	Parameters	NBTI effect on HKMG p-MOSFET
Geometric	Hf high-k ↓	↓
	SiO_2 interface layer ↓	↑
	Metal gate ↓	↓
	Gate length ↓	↑
	Polypitch	Temperature dependent
	Spacer length	Temperature dependent
	SiGe pocket	Temperature dependent
Process	HDD Boron ↓	↓
	Work function ↓	↓
	Halo doping ↓	No significant change

Table 4.2 Summary of HCI analysis (↓ = decreasing, ↑ = increasing)

Design considerations	Parameters	HCI effect on STI n-LDMOS
Geometric	STI angle ↓	↓
	STI depth ↓	↑
	Gate oxide thickness ↓	↑
Process	P-sub doping ↓	↓
	S/D implantation dose ↓	No significant change

In this work, it is observed that apart from stress voltage and stress temperature, the physical thickness and process parameters of high-k metal gate PMOS devices and STI-based LDMOS also exert a certain impact on the degree of NBTI and HCI degradation respectively. This is due to the existence of defect mechanism in the oxide bulk and/or interface region which was affected by the aforementioned factors. NBTI degradation due to gate stack scaling shows that the change in SiO_2 IL thickness affects V_{th} degradation by 96.16% more than in HfO_2 and 80.67% more than in metal gate at stress temperature of 375K for 1000s stress time. It can be summarized that SiO_2 IL appears to be a prominent layer of gate stack that contributes the most to V_{th} degradation. As for the HCI degradation of LDMOS, R_{on} degradation is observed to be most sensitive to the change in gate oxide thickness where the change in gate oxide thickness affects R_{on} degradation by 21.01% more than in STI depth and 99.48% more than in STI angle at stress temperature of 400K for 10ks stress time.

CHAPTER 5: CONCLUSION AND FUTURE WORKS

5.1 Conclusion

Negative bias temperature instability (NBTI) and hot carrier injection (HCI) have become among the most critical reliability issues due to the vast development of semiconductor devices technology nodes. The device parameters such as threshold voltage, mobility and drain current will deteriorate during the course of operation and eventually deteriorate the circuit performance over time. Practically, the realization of a designed device structure with good reliability performance is rather a complex and difficult process and therefore, utilizing TCAD tools is an excellent way to forecast the device potential performance and to study the physical defects. The reliability study in this work has been divided into two part, as follows:

The first part focused on the simulation study of the NBTI reliability on 32 nm technology node PMOSFET. Analysis on the effects of geometric and process parameters of advanced-process PMOS devices on NBTI and the contribution of defects on device reliability performance had been achieved in this section. The effect on the device parameters such as drain current (I_d), threshold voltage (V_{th}) as well as the lifetime of the device had been investigated and explained. When the high-k layer or metal gate layer thickness is increased, the threshold voltage degradation is observed to increase considerably. On the other hand, increasing the SiO_2 interfacial layer thickness resulted in the reduction of threshold voltage shift. It is found that the V_{th} degradation shows the strongest dependence on the SiO_2 IL thickness, compared with the HfO_2 high-k or metal gate thickness. Varying the SiO_2 IL thickness is shown to affect the V_{th} degradation by 96.16% more than varying the HfO_2 thickness and by 80.67% more than varying the metal gate, at stress temperature of 375K for stress time of 1000s. The temperature insensitivity indicates the absence of generated defects during short stress time of 1s and the presence of as-grown defects, as generated defects is strongly temperature dependence. More

generated traps are observed for thinner SiO_2 IL and thicker metal gate thickness at high oxide field. This signifies that the BTI effects is substantially affected by the inclusion of the metal gate after integration of high-k technology. Regarding the process design, higher HDD boron dose is shown to deteriorate the threshold voltage due to penetration of boron into the gate oxide. Our results also show that metal gate work function affects the attenuation of the threshold voltage as higher metal gate work function causes the exacerbation of trapped carriers in HfO_2. NBTI is found to be independent of the halo doping concentration, which may be due to the location of the halo structure slightly farther from the SiO_2 bulk interface of the device. In this study, it is also found that NBTI is less affected by the gate length variation at low oxide field (E_{ox}), but shows substantial effect at higher E_{ox} where the V_{th} degradation is shown to decrease with increasing gate length (decrease by 23.39%). Gate length is also found to exhibit really weak impact on NBTI lifetime such that it can be concluded that the effect of gate length of 32 nm technology advanced technology HKMG PMOS on NBTI lifetime is negligible.

In the second part of this work, a systematic study of HCI degradation has been investigated on the STI-based LDMOS devices. The study of geometrical and process design considerations of STI LDMOS devices influence on HCI has been achieved. LDMOS devices which possess lateral architecture allows current path to be mainly concentrated in a narrow region close to the silicon surface, resulted in the growing of degradation due to HCI. The application of high drain to source terminal potentials due to the architecture of LDMOS power devices has as well caused an alarming threat to the HCI reliability of the device. In this work, the STI angle of the simulated device was varied with three values, 45°, 80° and 100° in order to study the impact of STI angle of LDMOS devices on hot carrier stress. From the results obtained, it is found that the drain current for device with 100^0 STI angle is reduced by 58.78% compared to device with 45^0 STI angle. Larger STI angle shows higher HCI degradation due to the shorter

effective accumulation length (L_a) which cause higher trap formation. On the other hand, larger STI depth as well as larger gate oxide thickness is observed to cause lower degradation mainly because of the reduction of potential crowding at the body/drift surface for larger oxide. Process design wise, it is found that higher p-substrate doping concentration is observed to exhibit higher degradation as the depletion region width reduced with doping. It is also found that the HCI degradation is not significantly affected by the S/D implantation dose.

In conclusion, the reliability performance of devices is strongly dependent on the devices' design considerations. A framework to analyse the reliability of sub-nm devices, particularly NBTI and HCI have been developed. There are numerous reports of cases relating to electronic breakdown (due to heat, long period of usage) in electronic systems that are hazardous to the user. This work has successfully looked into the fundamental of how these defects had emerged and what factors that could trigger its generation. Optimizing the geometric and process design parameters of CMOS devices designed for reliability would be beneficial to ensure continuous scaling into the sub-nanometer technology nodes. The major achievement of this work is the publication in Journal of Electronic Materials. This work has also resulted in 3 conference presentations.

5.2 Future works

Deep understanding and accurate simulation of the influence of specific parameter selections on NBTI and HCI in the initial design phase are of paramount importance in order to assure that the operation of the devices and circuits are reliable within a specific lifetime criterion. This work has looked into the fundamental study that can be used as a framework to further accurately model devices' reliability in the future. The effect of design parameters on reliability performance and corresponding defects behavior can be used as an input to modify and improve the existing reliability model. A robust reliability model will be remarkably beneficial to the foundries as they will be able to eliminate the conservative guard-banding method which would directly impact the performance and power of devices.

Apart from that, the fundamental reliability study conducted in this project can also be used to minimize any design defects during advanced-process MOSFETs development. To date, experimental evidence of the geometry dependence on NBTI and HCI degradation have not been investigated and therefore, another possible future work is to experimentally examine the geometry effect. Further study on the optimization of performance and reliability can also be addressed in the future.

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LIST OF PUBLICATIONS AND PAPERS PRESENTED

Journal:

1. Ainul Fatin Muhammad Alimin, Anis Amiera Mohd Radzi, Nur Ashikin Fariza Sazali, Sharifah Wan Muhamad Hatta and Norhayati Soin, “Influence of Design Considerations of 32 nm Advanced Process High-k pMOSFETs on Negative Bias Temperature Instability and Study of Defects”, **Journal of Electronic Materials (2017), pp 1-8.**

Conference proceedings:

1. Alimin, AF Muhammad, SF Wan Muhamad Hatta, and N. Soin, "A study of the states kinetics in NBTI degradation by two-stage NBTI model implementation," in **2015 IEEE Regional Symposium on Micro and Nanoelectronics, Kuala Terengganu, Malaysia, 19-21 Aug 2015.**

2. Khafit, IN Abdullah, AF Muhammad Alimin, SF Wan Muhamad Hatta, and N. Soin, "Comparison of DC and pulse train analysis on submicrometer pMOSFETs lifetime prediction using on-the-fly method," in **2015 IEEE Regional Symposium on Micro and Nanoelectronics, Kuala Terengganu, Malaysia, 19-21 Aug 2015.**

3. Alimin, AF Muhammad, SF Wan Muhamad Hatta, and N. Soin, "Effect of gate length on Negative Bias Temperature Instability of 32nm advanced technology HKMG PMOSFET," in **2016 IEEE International Conference on Semiconductor Electronics, Kuala Lumpur, Malaysia, 17-19 Aug 2016.**

4. Alimin, AF Muhammad, SF Wan Muhamad Hatta, and N. Soin, "The Influence of Shallow Trench Isolation Angle on Hot Carrier Effect of STI-Based LDMOS Transistors," in **2017 IEEE Regional Symposium on Micro and Nanoelectronics, Pulau Pinang, Malaysia, 23-25 Aug 2017.**