BOUNDARY CONTROL OF A DUAL-OUTPUT BOOST CONVERTER WITH MULTILEVEL INVERTER TOPOLOGY

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ABSTRACT

With the development of power electronics applications and the usage of green power technology, many multilevel converters have been proposed. These topologies are mostly used in industrial applications such as photovoltaic and wind applications. However, the problem of DC-bus balancing is the most critical point on the control side of these inverters. In this work, a dual-output boost converter (DOBC) connected to a new topology of three-level inverter is evaluated. The DOBC is controlled is such a way to obtain a regulated capacitor voltage that feed the input voltage of the three-level inverter topology regardless of load changes. The control algorithm is based on second order switching surface which provides fast dynamic response during start-up and sudden loads' change. However, due to the need of many sensors, a sensorless boundary control method is developed. It predicts the inductor's current of the converter by measuring only the input and output voltages of the converter. A mathematical derivation of a sensorless second-order switching surface in the state-energy plane is carried out. The performance of the proposed topology is analyzed by using Matlab/Simulink software. Steady state characteristics and large signal stability analysis are carried out for the DOBC, the sensorless control algorithm is implemented in TMS320F2812. A three-level algorithm of SVPWM is implemented in Altera DE2 board to control the three-level inverter which ensures lower hardware resource usage and satisfy the switching time criteria. A hardware prototype of the proposed topology has been developed. Experimental results show good performance and fast transient response of the proposed configuration in term of DC-bus balancing and generation of the desired output.

ABSTRAK

Melalui aplikasi pembangunan kuasa elektronik dan penggunaan teknologi kuasa hijau, banyak Konvertor pelbagai peringkat telah dicadangkan. Topologi ini kebanyakannya digunakan dalam aplikasi perindustrian seperti fotovolta dan aplikasi wind. Bagaimanapun, masalah keseimbangan DC-Bas adalah yang paling dalam bahagian kawalan inverters ini. Dalam kerja ini, rangsangan converter output dual (DOBC) disambungkan kepada satu topologi tiga peringkat inventer telah dinilai. DOBC dikawal untuk mendapatkan suatu regulasi voltan kapasitor yang membekalkan voltan input topologi inventer tiga peringkat tanpa mengira perubahan beban. Algoritma kawalan adalah berdasarkan kepada peringkat kedua penukaran permukaan yang memberikan tindakbalas laju dinamik semasa permulaan dan perubahan muatan secara tiba-tiba. Bagaimanapun disebabkan keperluan berbilang sensor, kaedah mengawal sempadan tanpa sensor dibangunkan. Ia meramalkan arus induktor dengan hanya mengukur input dan output voltan konverter. Suatu derivasi matematik permukaan pensuisan peringkat kedua dalam kapal terbang state-energy dijalankan. Prestasi topologi yang dicadangkan dianalisis melalui perisian Matlab/ Simulink. Ciri-ciri keadaan mantap dan analisis kestabilan isyarat besar dijalankan untuk DOBC, algoritma kawalan tanpa sensor diimplementasi dalam TMS320F2812. Suatu algoritma tiga peringkat SVPWM diimplementasi dalam papan Altera DE2 untuk mengawal inventer tiga peringkat yang memastikan penggunaan sumber perkakasan yang lebih rendah dan memuaskan kriteria masa pensuisan. Suatu Prototaip perkakasan cadangan topologi telah dibina. Hasil eksperimen menunjukkan prestasi baik dan respon sementara yg laju bagi konfigurasi yang dicadangkan dalam DC pengimbangan bas dan generasi output yang dikehendaki.

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LIST OF SYMBOLS

$\alpha\beta$	:	Orthogonal set of axes
σ^2	:	Second order switching surface
$\dot{\sigma}^2$	:	The derivative of σ^2
$\sigma_+^2(t)$	:	Second order switching surface for the ON state
$\sigma_-^2(t)$	:	Second order switching surface for the OFF state
$a_0(k)$	:	Parameter used for inductance current estimation
α, β, μ	:	Coefficients used in state space solution
$b(k)$	:	Parameter used for inductance current estimation
Ceq	:	Equivalent capacitor
C_f	:	Filtering capacitor
ω_1	:	Angular frequency
$\frac{di_L}{dt}$	:	Inductor current derivative
$\frac{dV_0}{dt}$	:	Output voltage derivative
dPin	:	Input power derivative
ec, es	:	Coefficients used to simplify the solution of the state space
f_s, f_{sw}	:	Switching frequency
$H1, H2, H3$	:	Matrix for changing αβ axis to XY axis
h_{ON}	:	Time duration in the ON state
h_{OFF}	:	Time duration in the OFF state
i_L	:	Inductance current
i_{L_ref}	:	Reference inductance current
$i_L^L(t)$	:	Natural response solution of i_L in continuous-time domain
$i_L^F(t)$	:	Forced response solution of i_L in continuous-time domain

I_{ON}	:	The ON state current for the lower conventional boost converter
I_{OFF}	:	The OFF state current for the lower boost converter
Δi_{min}	:	Minimum current ripple
Δi_{max}	:	Maximum current ripple
$k1, k2, k3$	:	Coefficients that govern the stability of the DOBC
L_f	:	Filtering inductor
$M1, M2, M3, M4$	:	Fundamental matrix for each DOBC operating mode
Pin	:	Input power
Pout	:	Output power
dPin	:	The derivative of input power
S_{n1}-S_{n4}	:	Switches of the TLI ($n = A, B, C$)
$S_1(t), S1$	:	Second order switching surface criteria in region 1
$S_2(t), S2$	:	Second order switching surface criteria in region 2
$S_3(t)$	:	Second-order switching surface criteria for mode 1 and mode 4
Tco	:	Actual time utilized by the program in FPGA
T_{OFF}	:	Time duration in the OFF state
T_{ON}	:	Time duration in the ON state
Vao,	:	Voltage across phase node (a) and node (o)
Vbo	:	Voltage across phase node (b) and node (o)
Vdc	:	DC voltage
V_{in}, V_s , V_{dc}	:	Input DC voltage
V_1, v_1	:	Voltage output of capacitor C1
V_2, v_2	:	Voltage output of capacitor C2
V_0	:	Total output voltage of the DOBC
v_{0min}	:	Minimum output voltage of the DOBC
v_{omax}	:	Maximum voltage of the DOBC

$V_1^L(t)$	:	Natural response solution of V_1 in continuous-time domain
$V_1^F(t)$	:	Forced response solution of V_1 in continuous-time domain
$V_2^L(t)$	:	Natural response solution of the V_2 in continuous-time domain
$V_2^F(t)$	:	Forced response solution of the V_2 in continuous-time domain
$V1_{ESR}$	:	The output voltage of C1 with ESR effect
$V2_{ESR}$	:	The output voltage of C2 with ESR effect
V_{ON}	:	The output voltage in the ON mode
V_{OFF}	:	The output voltage in the OFF mode
V_{ab}, V_{bc}, V_{ca}	:	Inverter's line to line voltages
W	:	The energy of the DOBC
W_{ref}	:	The reference energy of the DOBC
ΔW	:	Energy band
W_{ESR}	:	The energy of the DOBC with ESR effect
XY	:	Non-orthogonal set of axes
X_i, Y_i	:	Projection on axes XY
$x^L(t)$	:	Natural response of the state space in continuous-time domain
$x^F(t)$	:	Forced response of the state space in continuous-time domain

LIST OF ABBREVIATIONS

AC	:	Alternating current
ACI	:	Asymmetric cascaded inverter
ADC	:	Analog to digital converter
ANPC	:	Active neutral point clamped
ASD	:	Adjustable speed drive
BC	:	Boundary Control
BM	:	Bidirectional moving
BS	:	Bidirectional stationary
CHB	:	Cascaded H-bridge converter
DC	:	Direct current
div	:	Per division
DOBC	:	Dual-output boost converter
DSP	:	Digital signal processor
EMI	:	Electromagnetic interference
ESR	:	Equivalent series resistance
EV	:	Electric vehicle
FC	:	Flying capacitor
FPGA	:	Field programmable cate arrays
GPIO	:	General purpose input/output
HEV	:	Hybrid electric vehicle
HV	:	High voltage
ISR	:	Interrupt service routine
JTAG	:	Joint test action group
LT	:	Laplace transformation

LV	:	Low voltage
ML	:	Multilevel
MLI	:	Multilevel inverter
MOB	:	Multi-output boost converter
MV	:	Medium voltage
NPC	:	Neutral point clamped
PLL	:	Phase locked loop
PV	:	Photovoltaic
PWM	:	Pulse width modulation
SIMO	:	Single inductor multiple-output
SPWM	:	Sine pulse width modulation
SVM	:	Space vector modulation
SVPWM	:	Space vector pulse width modulation
TLI	:	Three-level inverter
UM	:	Unidirectional moving
US	:	Unidirectional stationary
VAR	:	Volt ampere reactive
VHDL	:	VLSI hardware description language

CHAPTER 1: INTRODUCTION

1.1 Background

Power electronics have occupied for several years a progressively important place in the industry. Owing to their multiple topologies and the usage of more and more efficient control techniques, the application of power electronics in industrial processes had led to significant improvements in term of efficiency, power quality and equipment size and cost. In many industries, for example, automotive, aeronautics and green energy, the trend is to develop topologies with the distributed power supply system. These systems possess great flexibility to handle different types of loads efficiently. Generally, these systems are composed of static converters controlled in such a way to achieve desired operating criteria under various supplies and load conditions.

For the controller design, linear control methods are the most common tools used where the averaging techniques are employed, kept up by linearization and small signal determination, which allows the derivation of dynamic model for any converter topology. However, with these techniques, system parameters variations and large signal transients cannot be dealt which limit the controller performance and may result in system instability. In order to overcome these limitations and ensure system stability with good dynamic response, nonlinear control strategies are considered better applicant in converters control rather than other linear feedback controller.

1.2 Multilevel Inverters

Power converters are circuit devices that control the power flow through certain switches arranged in a specified form. The processed power can vary from milliwatts to megawatts. They manage the flow of energy between two structures to obtain the desired specification of the electrical energy. Since 1960, the principle of multilevel converters

is introduced and evaluated. It began with three-level circuit for computer applications, then a neutral point clamped (NPC) in 1980. Subsequently, different multilevel topologies have been proposed and used for all types of power conversion. The elementary concept of multilevel converter is to produce a desired shape of the output voltage from several voltage levels with minimum of distortion, lower switching frequency, better efficiency, and minimum numbers of switches. However, the control of these switches will be more complex proportionally with the augmentation of level's numbers, hence, the control technique of these converters will be more complex (Gupta, Ranjan, Bhatnagar, Sahu, & Jain, 2016).

Since the concept of multilevel is introduced, different published works have investigated the multilevel structures on AC/DC or DC/AC power converters. In addition, three major multilevel converter structures have been well described: the cascaded H-bridges converter, diode clamped or neutral clamped and flying capacitors power converter. Besides, the majority of these converters are utilized as a part of utility and substantial motor drive applications. Regarding the multilevel DC/DC converter, there are few published works that discuss this type of conversion (Adam, Gowaid, Finney, Holliday, & Williams, 2016; Fan, Peng, & Zhaoming, 2004). For multilevel DC/DC topologies, the magnetic elements may be reduced or even eliminated, which means an improvement in terms of size and cost. Nevertheless, the DC/DC multilevel converter will face the capacitors balancing problems compared to multilevel AC/DC or DC/AC converter. Besides, the redundant switching states are less due to the asymmetric DC output voltage. On the other hand, the difference between each individual component in term of characteristics, either on semiconductors or on passive elements, creates an unbalanced output voltage. Generally, a balanced control circuit is required to ensure a balanced and stable capacitors output voltages, that provides sufficient redundant switching states. Nevertheless, not all DC/DC multilevel converters topologies have

adequate switching states, which mean part of them cannot be applied in DC/DC applications (Bottion & Barbi, 2013; Fan et al., 2004).

1.2.1 Application of Multilevel Inverters

As mentioned earlier, multilevel inverters employ numerous DC voltages to produce a chosen AC voltage. Thus, multilevel inverters can be realized using different power resources, for example, photovoltaic and fuel cells in addition to ultra-capacitors and batteries (Vishvakarma, Singh, & Shukla, 2012). If a multilevel converter is employed to either absorb or produce purely reactive power, then the multilevel converter can be utilized as a reactive power compensator to enhance for instance the power factor of the load. They can also be used as active power filters to suppress harmonics from the utility by generating these harmonics and injecting them in opposite wave shape to mitigate them. As a result, the power quality of AC system is improved and more sinusoidal shapes are provided. If the DC sources of the multilevel converter are banks of batteries or capacitors, the multilevel converter can likewise be utilized to give ride-through capacity under critical conditions. This application is extremely useful when voltage sags or load swings are occurred at the utility connection (Sinsel, Ramsay, Hörger, Janke, & Alegria, 2014; X. Sun et al., 2016).

Multilevel converters are also used to construct back-to-back converters. For example, one multilevel diode-clamped converter acts as a rectifier for the utility interface while the other multilevel diode-clamped converter acts as an inverter to supply the desired AC load. The system can be used as a frequency changer, a phase shifter, or a power flow controller. Moreover, multilevel converters are used as adjustable speed drives (ASD). The input from the AC source can be a constant with defined frequency while the output of the ASD can be connected to an AC load whose magnitude and frequency are variable (Kouro et al., 2010). g Another conceivable use of multilevel converters is in electric

vehicles (EVs) and hybrid electric vehicles (HEVs) because they are all ideally suited to use a large number of relatively small-sized energy sources, such as batteries and fuel cells. In addition of that, multilevel converters generally permit the usage of smaller devices, hence reducing the converter weight (Raghi & Geisa, 2016).

1.2.2 Feeding Multilevel Inverters

Depending on the type of three-phase converter used, different voltage feeding sources are used to feed the multilevel converters. The simplest method is by using many isolated DC power sources. These DC power source can be several numbers of photovoltaic cells, DC current motors in power generation mode, fuel cells that have to be converted to three-phase AC system either to feed AC loads or to be connected with the grid. However, there are many cases where only one DC source is available such as in electric vehicles, locomotives, and other mobile systems. In these cases, the DC voltage has to be generated by a number of DC/DC converters or multilevel DC/DC converter to satisfy the DC bus voltage balancing (Elsied et al., 2015). On the other hand, if only one AC source is available to supply the multilevel inverter, a transformer with the needed number of secondary side is used with a rectifier to feed the DC side of the multilevel inverter. This type of transformer is called poly-phase transformer.

1.2.3 Merit and Demerit of Multilevel Converter

Multilevel converter topologies established distinct considerations attention during the last two decades due to their distinguish advantages in high-power high-voltage applications. Using them in such applications gives them the possibility of:

1) Eliminating the need of bulky and expensive step-up transformers.
2) Reducing wires and cable connections cross-sections.
3) Improving harmonics content on the output signals.

4) Reducing the size of the output filters, hence the cost is also reduced.
5) Improving the efficiency of the converter when low frequency switching is used.

Nevertheless, there are some drawbacks linked with the use of multilevel inverters such as:

1) The requirement of isolated DC power supplies in each voltage level.
2) Complexity of the control technique due to the increase of switches numbers.
3) Large numbers of components sometimes increase the probability of device failure.
4) DC-bus voltage balancing is highly required.

1.3 Control Techniques

Conversion and control of electrical energy using multilevel converters are a very important field of research due to the rapid growth of power demand with new requirements on power quality and efficiency. To fulfill these demands new switches, topologies, and control schemes have been developed. The classical method techniques used in controlling multilevel converter such as space vector modulation (SVM), sine pulse width modulation (SPWM) are widely used (Chinnaiyan, Jerome, Karpagam, & Suresh, 2007; Gaur & Singh, 2014). Besides that, the controls of these converters need to assume an optimizing performance and keeping the required robustness under different operation conditions. Regular methods based on small-signal linearization have been observed to be not able of accomplishing the necessary regulation, dynamic response, and stability requirements needed by these systems. Therefore, researchers focus on developing some advanced control techniques, which can fulfill the necessity of power conversion systems. Specifically, modern control techniques like sliding mode control, hysteresis control method, predictive control method, and graphical control method have

been put in practical to control these systems, and their practicability has been investigated (Silva, 2012) . In some recent work, boundary control technique with second-order switching surface has been tested and has shown to be an exceedingly encouraging solution for controlling power converters (He, Chung, Ho, & Wu, 2017). Boundary control is a geometric based control approach appropriate for switching converters, which has a distinguish feature of controlling converter operation without differentiating start-up, transient, and steady state mode. Hence, it has the ability to handle large-signal disturbances in the input and output sides (Chiu, Leung, & Chung, 2007).

1.4 Problem Statement

Multilevel power conversion is a promising technology in high power applications. Recently, several families of power converter have been presented to provide cleaner power source, higher output power, less losses and almost free harmonics. Although each category of multilevel converter has similar advantages, they might be appropriate for particular application caused by their structures and disadvantages. In order to enhance the performance of these type of converters, some problems necessitate the use of certain techniques to overcome them. For example, multilevel converters experience capacitors unbalance operation condition with regard to the modulation index and load power factor.

If the capacitors voltages are unbalanced, the converter output voltage will have unacceptable distortion. Indeed, even there are many topologies and control techniques for capacitors voltage balancing, but these methods are characterized by a complication in the controller side. Moreover, they are not appropriate for all system conditions. To cure this issue, distinctive control strategies and circuit topologies are verified and assessed based on the control complexity and the practical application of the converter. On the opposite side, the multilevel DC/DC converters are utilized as front-end converters certain applications to supply inverters' DC interface voltage. Consequently, capacitor

voltage balancing can be seen from the DC/DC side, rather than the inverter side. This part has motivated the exploration and development of economical multilevel DC/DC converters with fast and robust control technique.

1.5 Research Objectives

The main objective of this research is to develop and design a control algorithm, which is able to enhance the quality of a multilevel inverter in terms of DC bus balancing, fast dynamic response, and tight output voltage regulation. The developed control technique is based on boundary control using second-order switching surface and the proposed topology is a Dual-Output Boost Converter (DOBC) connected to a multilevel inverter. More specifically the objectives of this research are set out to:

1) Propose a sensorless boundary control method for the Dual-output Boost converter to reduce the number of sensors used in the control technique; hence reduce the control circuit cost.
2) Implement the proposed control strategy to control a DOBC connected to a three-level voltage source inverter.
3) Verify the performance of the proposed control techniques.

1.6 Thesis Organization

The thesis consists of six chapters. Chapter 2 is devoted to present various topologies of multilevel converters such as DC/AC and DC/DC conversion. Besides, a geometrical control technique based on switching boundary control is also presented. Its stability issue and control's robustness are highlighted as well at the end of this chapter. Chapter 3 covers the description of the proposed topology with its control strategy. The working principle of each part of the configuration is well discussed. In addition, the development of second-order switching surface in state-energy plane for a DOBC is presented as well

as the steady state analysis and the stability behavior of the converter are exposed. Chapter 4 is focused on sensorless control technique of the DOBC. A detailed development and investigation of sensorless boundary control is provided. Chapter 5 examines the details of hardware implementation of the proposed topology. Information about simulation and program code execution is provided. Relevant experimental results and analysis are presented and discussed in details. Finally, chapter 6 presents summary and general conclusions. The thesis is supplemented by three Appendices among which are: Matlab modeling code sources, DSP code source of the boundary control method, and the laboratory set-up of the proposed converter.

CHAPTER 2: LITERATURE REVIEW

2.1 Introduction

Multilevel converters are getting more consideration in industrial applications. Currently they are commercialized in a varied range of applications such as in high voltage direct current transmission, railway traction, solar and wind energy. They present a great deal of challenges and become more competitive than the conventional topologies. They have the advantage of synthesizing desired output voltage waveforms from various voltage levels with minimum distortion, less switching frequency, higher efficiency, and lower stress voltage on devices. They can provide the desired output voltage in all type of power conversions (Babaei, Buccella, & Saeedifard, 2016b; Kouro et al., 2010).

The technology of multilevel on AC/DC or DC/AC conversion have been discussed in many literatures, and the well-known topologies have been fabricated and used in industrial applications. On the other hand, only fewer research works propose and investigate multilevel DC/DC converters topologies. Recently, many useful works are carried out to investigate and analyze different types of multilevel converters in terms of operating principle, modulation schemes, control techniques, and good dynamic response (Babaei, Buccella, & Saeedifard, 2016a). In this chapter, a complete study of multilevel inverter from topology viewpoint is conducted, followed by a review of multilevel DC/DC converter topologies, applications and limitations. Furthermore, an overview of boundary control is presented.

2.2 Multilevel Inverters

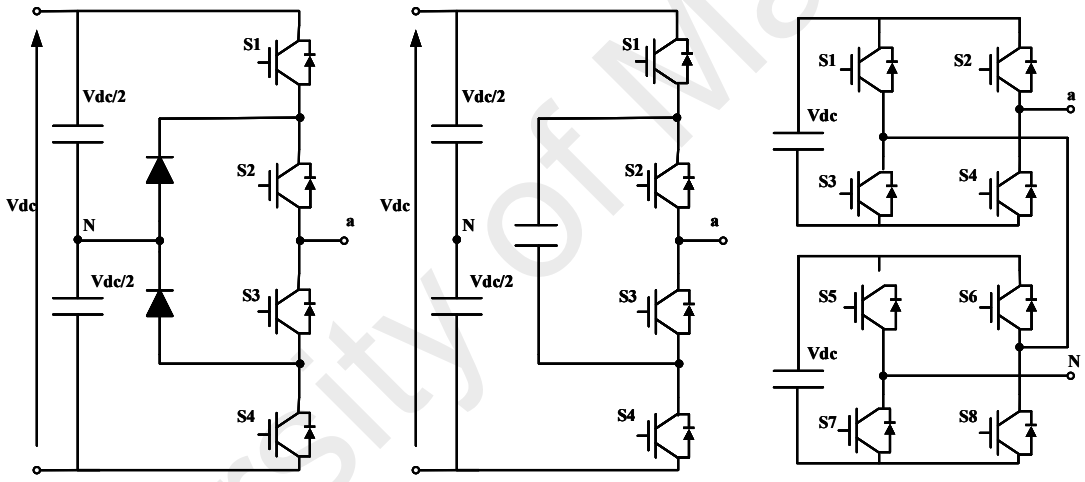
During last two decades, Multilevel inverters have gained a progressive development in term of topologies and area of applications. The effort made by researchers and industry has led to a rapid growth of different multilevel inverter topologies, modulation

techniques, and control strategies. In addition to other important research topics that attract researchers such as the fault tolerant operation, efficiency improvement, optimized control strategies, and new applications (Babaei et al., 2016a).

Multilevel converters are capable of generating higher levels in the output voltage waveform with low voltage stress on the switches. In addition to better waveform quality and lower total harmonic distortion in the phase voltages, they also have advantages of reduced electromagnetic interference, lower device voltage ratings, and lower switching frequency. Hence, they found widespread applications in motor drives (for fans, pumps, blowers, compressors, conveyors, laminators, traction systems, paper and metal mill systems), utility interface applications such as static var compensators, active filters, high-voltage DC transmission systems, rectifiers for telecommunication equipment, unified power-flow controllers, DC/DC converters with high frequency isolation, distributed energy generation systems from renewable energy sources (wind generators, photovoltaic panels, fuel cells), and superconducting magnetic energy storage systems (Rodriguez et al., 2009; V. N, A. R, Kaarthik, Kshirsagar, & Gopakumar, 2017).

Multilevel converter technology started with the introduction of the cascaded H-bridge converter, in the late 1960s and reintroduced again in the late 1980s due to the rapid growth in semiconductors and power electronics field. The cascaded H-bridge has gained more attention and industrial applications in the mid-1990. Through manipulation of the cascade inverter and adding diodes for voltage clamping, diode clamped multilevel inverter, known as neutral point clamped (NPC), was derived in 1975. The NPC multilevel inverter doubles the device voltage level without requiring precise voltage matching, the circuit topology had been prevailed in the 1980s. Nowadays, NPC is extensively used in industrial applications and commercialized by several manufacturers in the field. In the same way, the diodes in NPC were replaced by capacitors and new

topology called flying capacitor circuit was introduced (Prayag & Bodkhe, 2016; Rodriguez, Bernet, Steimer, & Lizama, 2010). Over the years, the FC has also been described as the imbricated-cell and multi-cell converter. These three multilevel converter topologies are known as traditional multilevel topologies and they had been used as real industrial products during the last two decades. Figure 2.1 shows the power circuits of one phase for each traditional topology. These power converters are commercialized by several manufactures in the field, offering different power ratings, front-end configurations, cooling systems, semiconductor devices with their control schemes, and other technical specifications (Kouro et al., 2010).



(a) NPC (b) Flying capacitor (c) Cascaded

Figure 2-1: Conventional three-level power converter topologies

In an attempt to augment the number of levels, several new topologies are introduced by modifying or hybridizing the above basic topologies. Researchers are seeking more effective designs in terms of overall cost, number of levels and losses. In the next section, some of the most common configurations are surveyed.

2.2.1 Recent Multilevel Inverters Topologies

Aside the topologies presented previously, there are also a couple of other multilevel topologies which exist. The Active Neutral Point Clamped (ANPC) topology shown in Figure 2.2 is a modification of the NPC structure offering an improvement from the point of view of the loss balancing within the semiconductor devices.

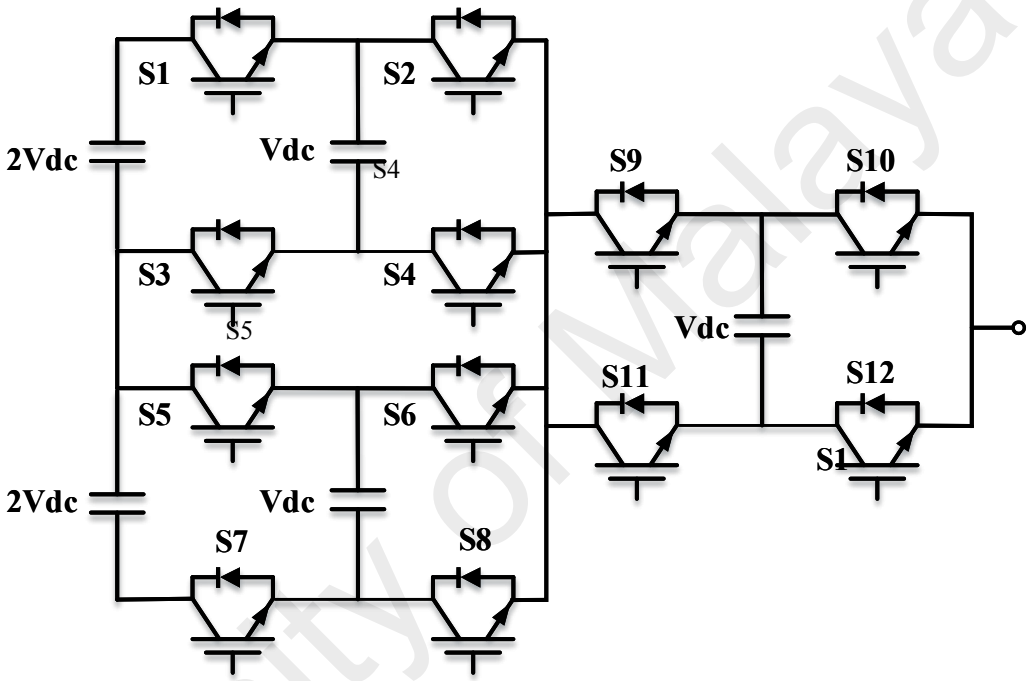


Figure 2-2: ANPC topology

The generalized multilevel inverter topology proposed by F. Z. Peng, shown in Figure 2.3, is another kind of multilevel topology. The disadvantage of this topology is the very large number of active and passive components. It is quite likely not suitable for MV and HV applications. The topology was initially designed for LV applications (Fang Zheng, 2001).

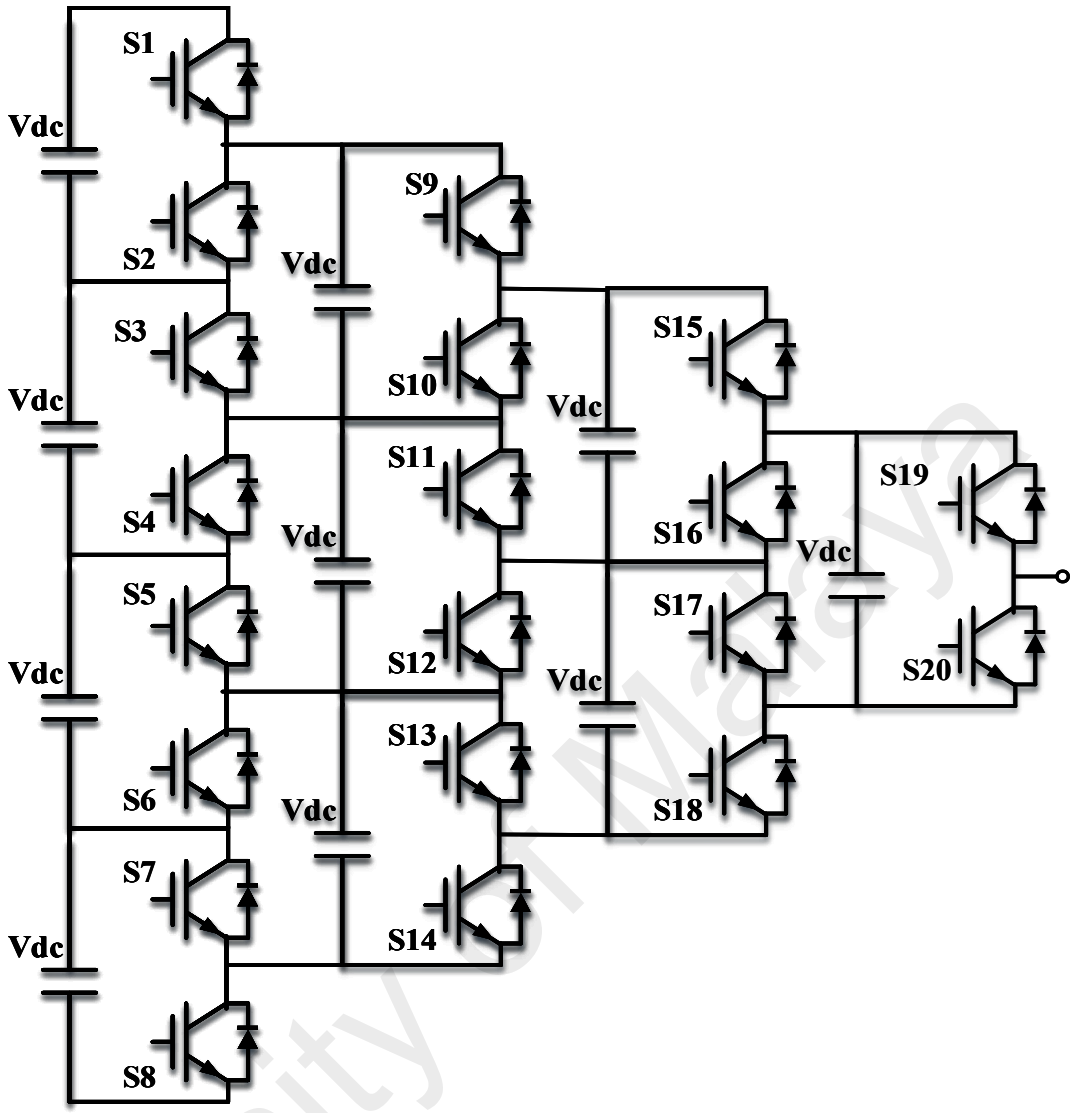


Figure 2-3: Generalized MLI topology

Another configuration is the cascaded multilevel inverter which commonly use the same DC-link voltage value for each and every cell. Additional voltage levels can be seen in the inverter output if the cells are taken with dissimilar DC voltages as shown in Figure 2.4. In the literature, the configuration that uses different DC-link voltages are referred as asymmetric cascaded inverters (ACI). Asymmetric DC-bus in MLIs helps to minimize the number of the utilized switching devices to reach a given number of steps. Moreover, in asymmetrical configurations, high power cells may switch in fundamental frequency that implies optimized switching losses (Malinowski, Gopakumar, Rodriguez, & Perez, 2010).

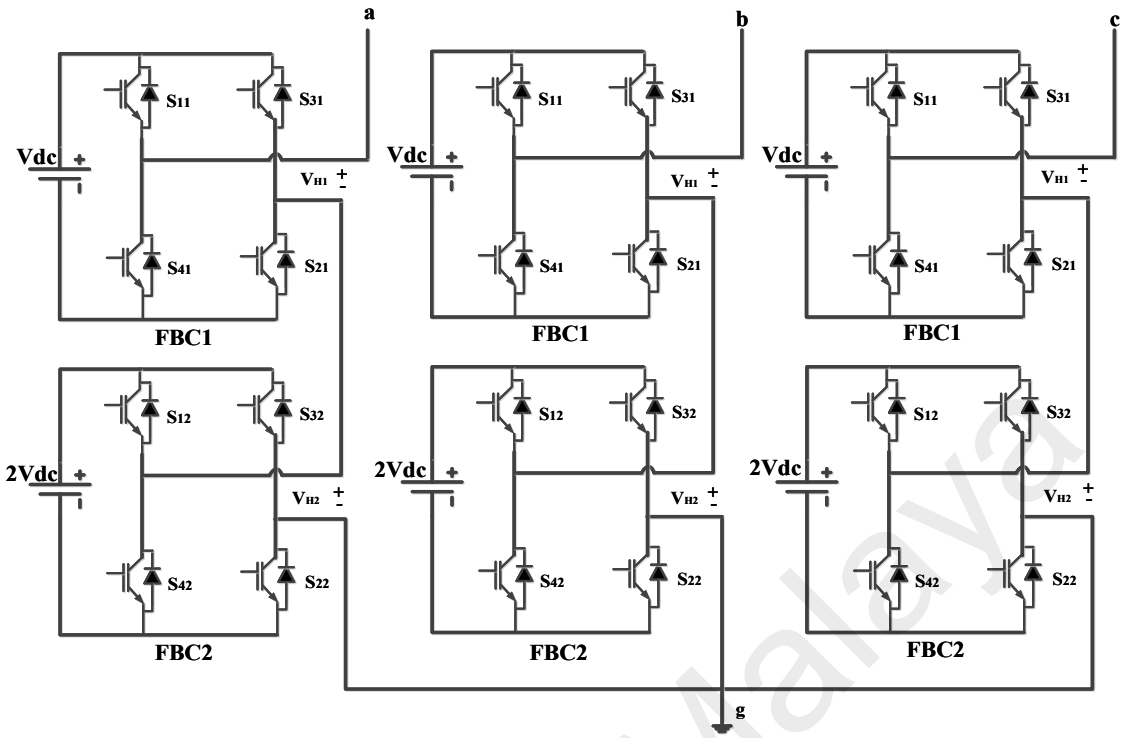


Figure 2-4: Asymmetrical seven-level CHB inverter

On the other hand, the full bridge cell in the cascaded converter can be replaced by diode clamped or capacitor clamped converter as shown in Figure 2.5 to minimize the number of separate DC sources for high-voltage and high-power applications. This topology is called mixed level hybrid multilevel inverter, it requires less DC separate sources but leads to complex control circuit due to its hybrid network (Bayhan, Trabelsi, Ellabban, Abu-Rub, & Balog, 2016; Chattopadhyay, Chakraborty, & Pal, 2012)

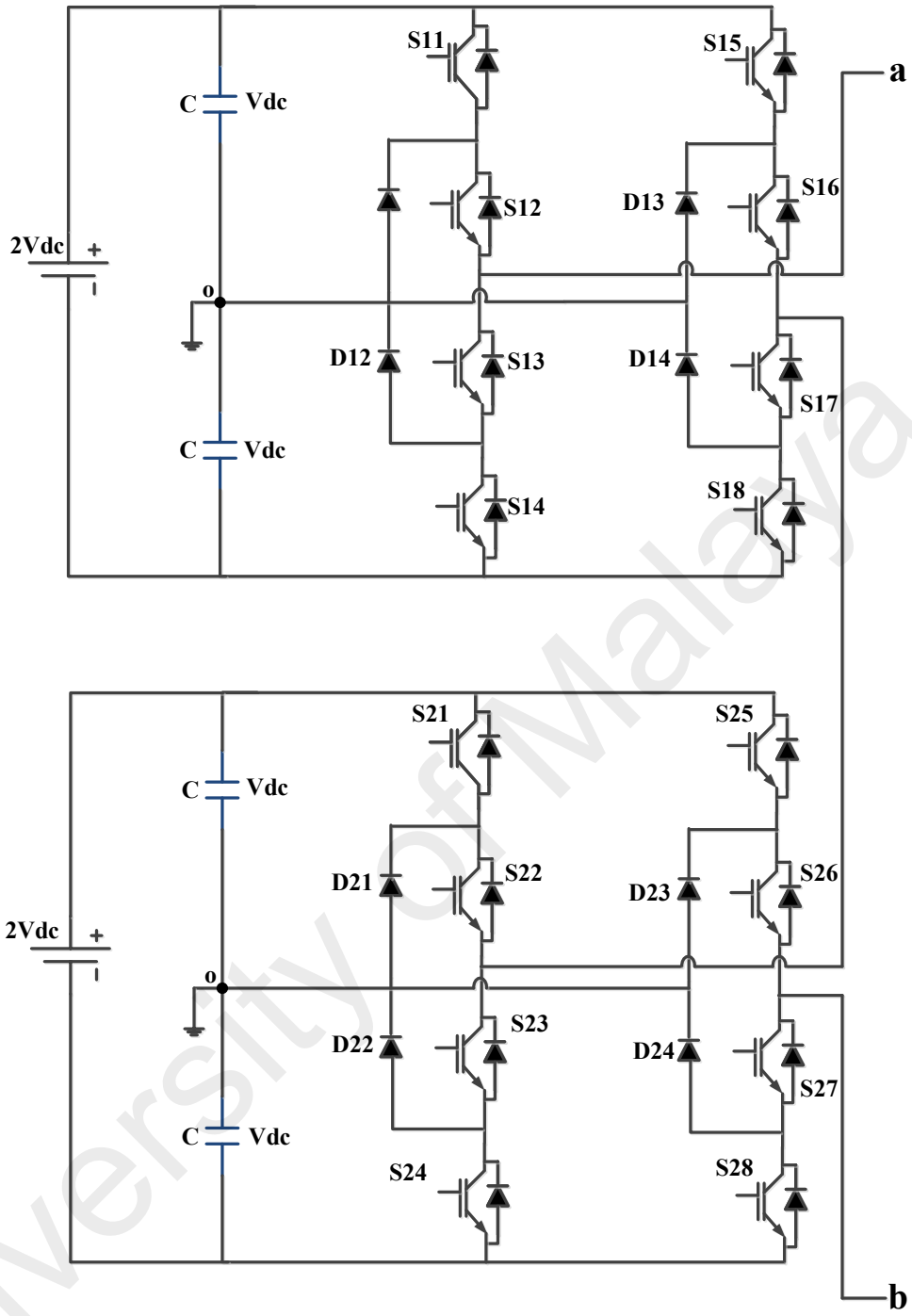


Figure 2-5: Mixed level hybrid unit configuration

The design of MLIs can be further optimized based on hybridization. In such specificity, smaller dissimilar inverter circuits are cascaded and some modifications are done on basic MLI topologies. Cascaded stages of different topologies in hybrid inverters make a significant reduction in the number of switching devices, system cost, EMI problem, device losses, and increasing the dynamic performance of the converter. Among

these hybrid topologies, Figure 2.6 shows a three-phase hybrid MLI proposed for grid integrated photovoltaic central inverter systems. This topology is a combination of CHB and NPC circuit. The proposed configuration uses an asymmetric structure of DC-bus voltage to increase the number of levels at the output of the inverter. The topology is made of six units H-bridge converters and one three-phase three-level NPC inverter to obtain 29-levels at the output voltage (Hasan, Mekhilef, & Ahmed, 2014; Mekhilef, Kadir, & Salam, 2013).

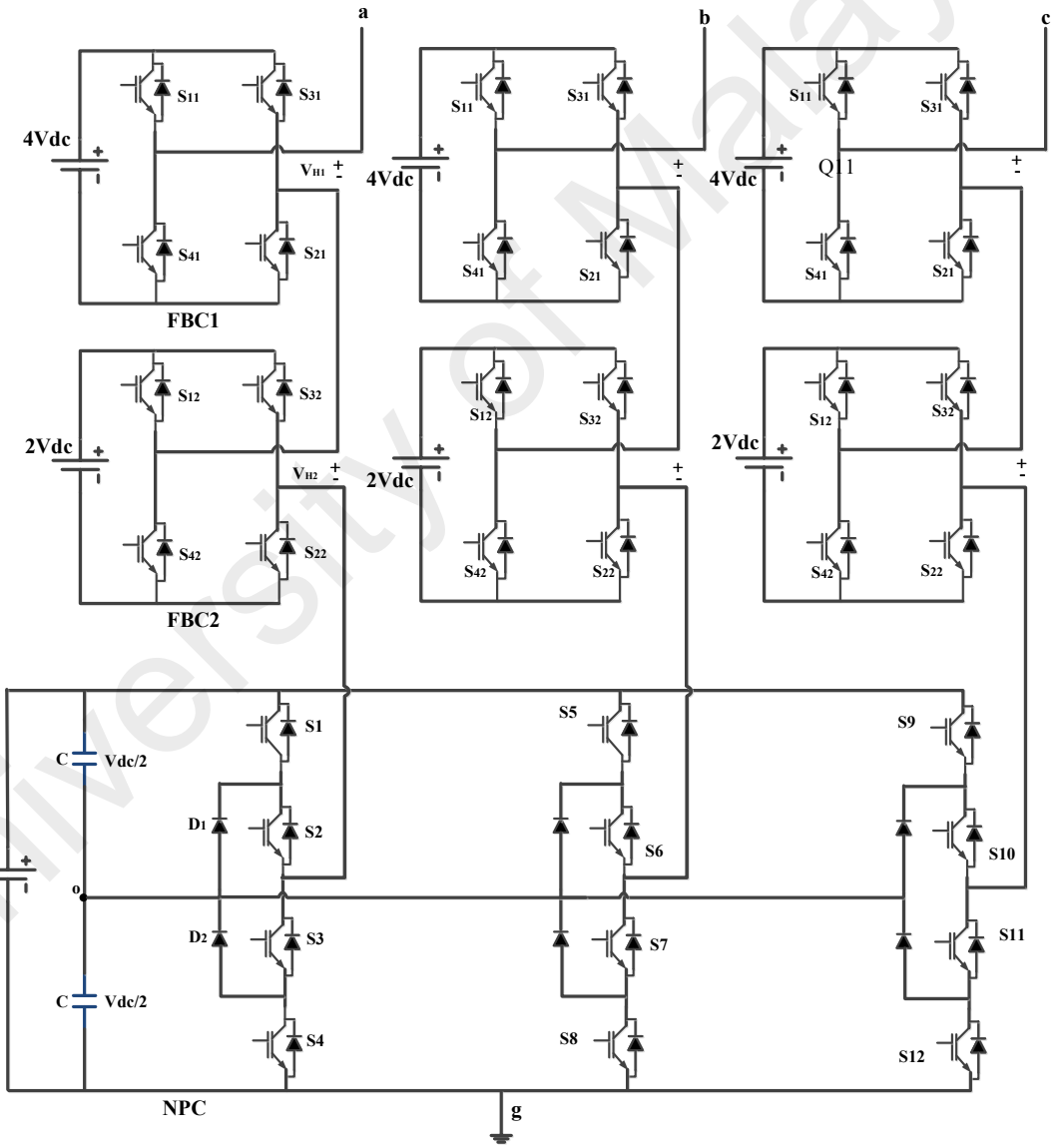


Figure 2-6: NPC-CHB hybrid multilevel inverter

Recent works in (Samadaei, Gholamian, Sheikholeslami, & Adabi, 2016) shows a new module for cascaded multilevel inverter. The module is shown in Figure 2.7, it can generate 13 levels and called an envelope type (E-Type) module.

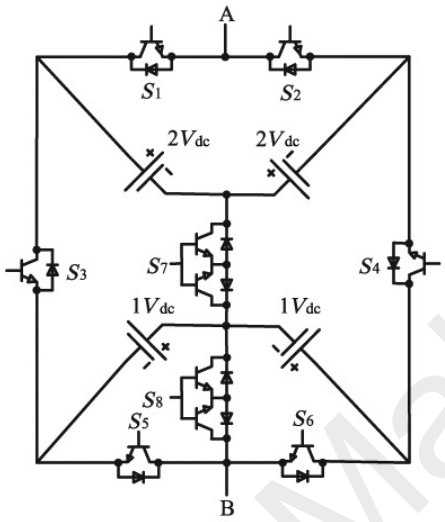


Figure 2-7: Proposed E-type module of multilevel inverter

Another configuration proposed in (Alishah, Hosseini, Babaei, & Sabahi, 2016) is shown in Figure 2.8. The topology is built using cascaded connection of sub-multilevel units with reduced switching components and DC voltage sources. It is suitable for high voltage applications as it employs switches with low voltage rating.

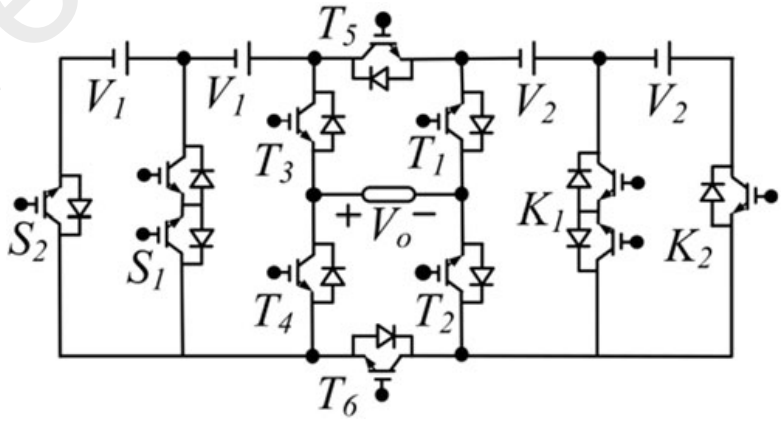


Figure 2-8: Basic unit topology of the multilevel inverter

Besides, a π-type five-level inverter is proposed in (Hu, Xie, Fu, & Cheng, 2016). The proposed topology is considered as a variant of T-type three-level structure or dual-buck inverter with coupled inductors. It is suitable for multilevel power conversion with low DC-bus voltage. The proposed topology has the benefit to obtain five-level output voltage using only four active power switches. The topology exhibits low harmonic distortion and good efficiency.

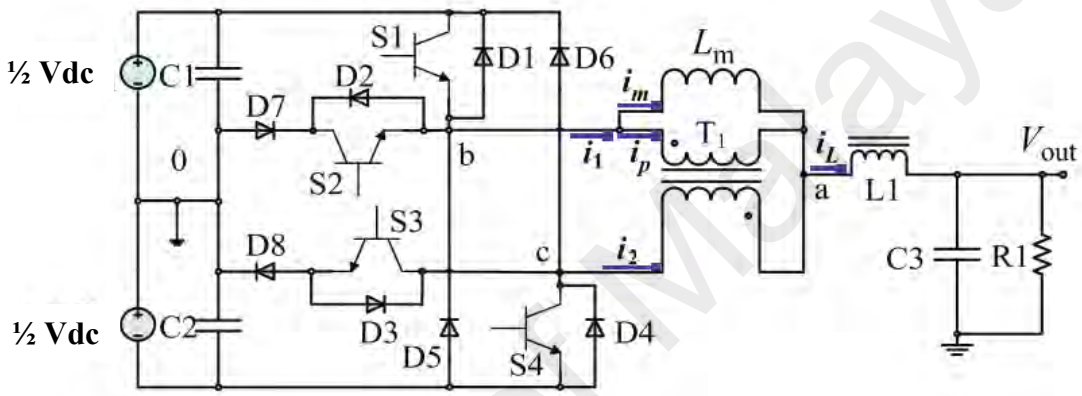


Figure 2-9: Single phase *π*-type five-level inverter

Besides, a cascaded seven-level inverter with single DC source is presented in (X. Sun et al., 2016). Compared with the traditional cascaded multilevel inverter, the proposed topology replaces all the separate DC voltage sources with capacitors. Also in (Le & Lee, 2016) a new topology of six-level inverter for medium-voltage high power applications is proposed. As shown in Figure 2.10, it consists of inner flying capacitor inverter units and outer two-level inverter units.

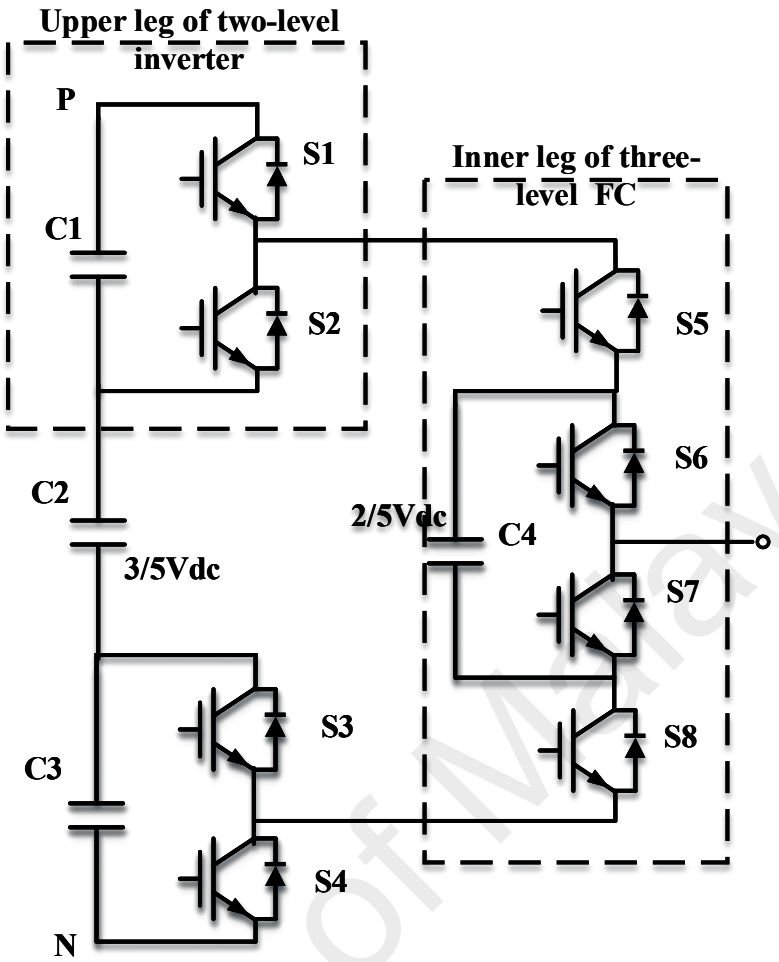


Figure 2-10: Single phase six-level inverter

In (Samanbakhsh & Taheri, 2016), a new structure for symmetric cascade multilevel inverters is proposed. This structure requires the least power electronic components, gate driver circuits, power diodes, and DC voltage sources. To better illustrate the characteristics of recent multilevel topologies, it is important to compare them with the conventional one and classify them in term of component requirement. Table 2.1 is prepared to indicate the number of switches, diodes, capacitors and DC supply per phase in some chosen topologies. As N is the number of levels in phase voltage, Table 2.1 shows that for the same number of output voltage levels the conventional topologies need 2(N-1) main switches, while (N+5)/2 is needed in (Ceglia et al., 2006), 3(N-1)/2 is needed in (Babaei, Laali, & Alilu, 2014), $(2N + 2\sqrt{2N + 4} + 4)$ is needed in (Amamra, Meghriche, Cherifi, & Francois, 2016), and 5(N-1)/6 in (Samadaei et al., 2016).

Table 2-1: Generalized comparison for different MLI

MLI Topology	Main Switches	Main diodes	Clamping diodes	DC bus	Flying capacitors
NPC	2(N-1)	2(N-1)	(N-1) (N-2)	(N-1)	0
FC	2(N-1)	2(N-1)	0	(N-1)	3/2(N-1). (N-2)
CHB	2(N-1)	2(N-1)	0	(N-1)	0
(Ceglia et al., 2006)	(N+5)/2	2(N-1)	0	(N+1)/2	0
(Babaei et al., 2014)	3(N-1)/2	3(N-1)/2	0	(N-1)/2	0
(Amamra et al., 2016)	$(2N + 2\sqrt{2N+4} + 4)$	$(2N + 2\sqrt{2N+4} + 4)$	0	$\frac{1}{2}\sqrt{2N+4}$	0
(Samadaei et al., 2016)	5(N-1)/6	5(N-1)/6	0	(N-1)/3	0

2.3 Multilevel DC/DC Converters

Multilevel power converters have been generally utilized in high power conversion. Regularly, the majority of research works are presented for AC/DC or DC/AC conversion. Recently, some research works have proposed the application of multilevel structure to DC/DC conversion to bring its advantages in the DC applications, which can appear in removing the magnetic inductors and improving the dynamic performance of the converters. Figure 2.11 shows the most recent topologies for DC/DC converter. These multilevel DC/DC converters employ the minimum number of devices without using immoderate capacitors or complicated matrix arrangements which are used in the traditional switched capacitor. Therefore, the size of converters is reduced, so the cost is dropped and the efficiency is improved (Peng, Qian, & Cao, 2010). Nevertheless, multilevel DC/DC converter will encounter more balanced capacitors issues compared to other AC/DC or DC/AC conversions.

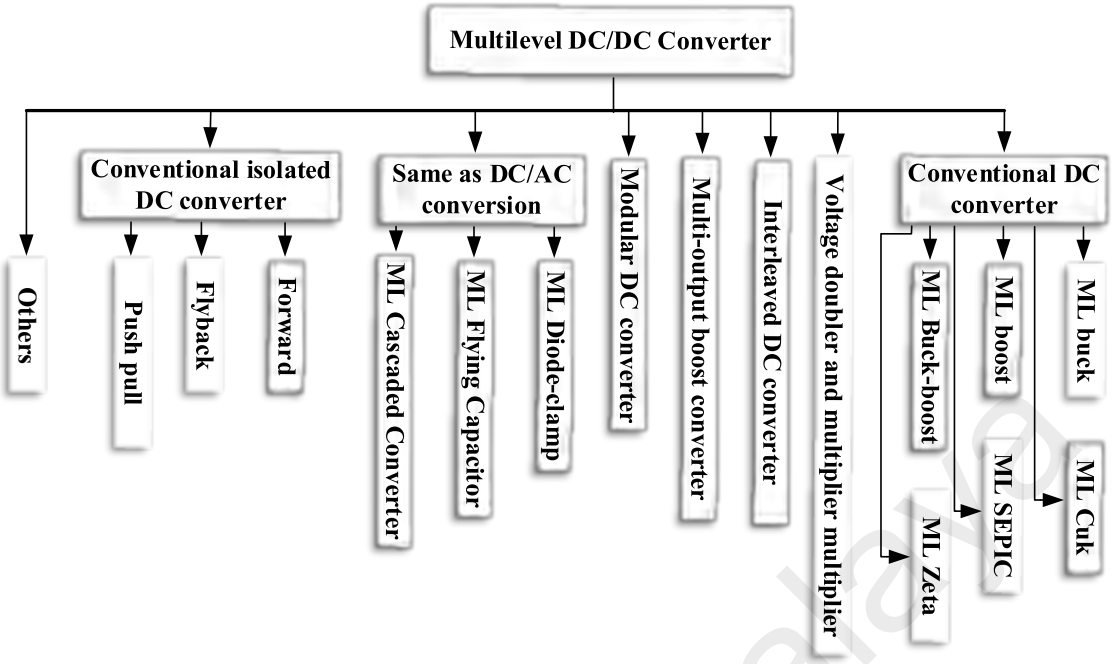


Figure 2-11: Different topologies of multilevel DC/DC converter

On the other hand, the multilevel DC/DC converter has fewer redundant switching states compared to other type of conversion due to the asymmetric DC output voltage. Additionally, unbalanced capacitors voltages are produced due to the difference in characteristics of utilized semiconductors and passive elements. To overcome this problem, an additional control system is provided, either by manipulating the redundant switching states or including other external circuits in the topology. For the first case (using the redundant switching states), there are some multilevel topologies which don't have sufficient switching states, hence they can't be utilized in DC/DC applications (Fan et al., 2004; Shen, Peng, & Tolbert, 2008).

Normally, the traditional multilevel topologies, diode-clamp, flying-capacitor, and cascaded converter, have their corresponding topologies in DC/DC applications. In the next section, these converters are surveyed and analysed. For simplicity, multilevel DC/DC converters presented here are step-down converters, although some of them may

have a bidirectional transfer of energy. The input voltage is set ($3V_{dc}$) and the output voltage is ($1V_{dc}$).

2.3.1 Diode-Clamp Multilevel DC/DC Converters

Figure 2.12 presents a four-level diode clamped multilevel converter, which is typically used in DC/AC applications. If the diode clamp topology is utilized for DC/DC application, a diminution in the redundant switching states will appear, which lead to a problem in keeping a balanced voltage at the output side. To get an output voltage equal to ($1V_{dc}$), the voltage V_{ao} has to be greater than V_{bo}. Moreover, to obtain a minimum voltage ripple with smaller filter size at the output side, the chosen control technique has to fulfil (V_{ao} - V_{bo}) equal to ($1V_{dc}$). Therefore, only some specific combinations of switching states can be chosen. Table 2.2 provides all the switching states in phase (a) and phase (b). To get V_{ab} equal to ($1V_{dc}$) three switching states can be used, and every one runs under 1/3 duty cycle to permit balanced output voltages (Fan et al., 2004; Sun, Zhang, Cai, & Shi, 2016).

If the converter input and output side are connected directly to the same ground, V_{bo} have to be set to zero, which means that only the last switching state can be applied. Therefore, there is no real way to maintain balanced output voltages. The lower capacitor will be discharged till zero and the upper two capacitors remain charging (Dong, Deng, & Chen, 2016).

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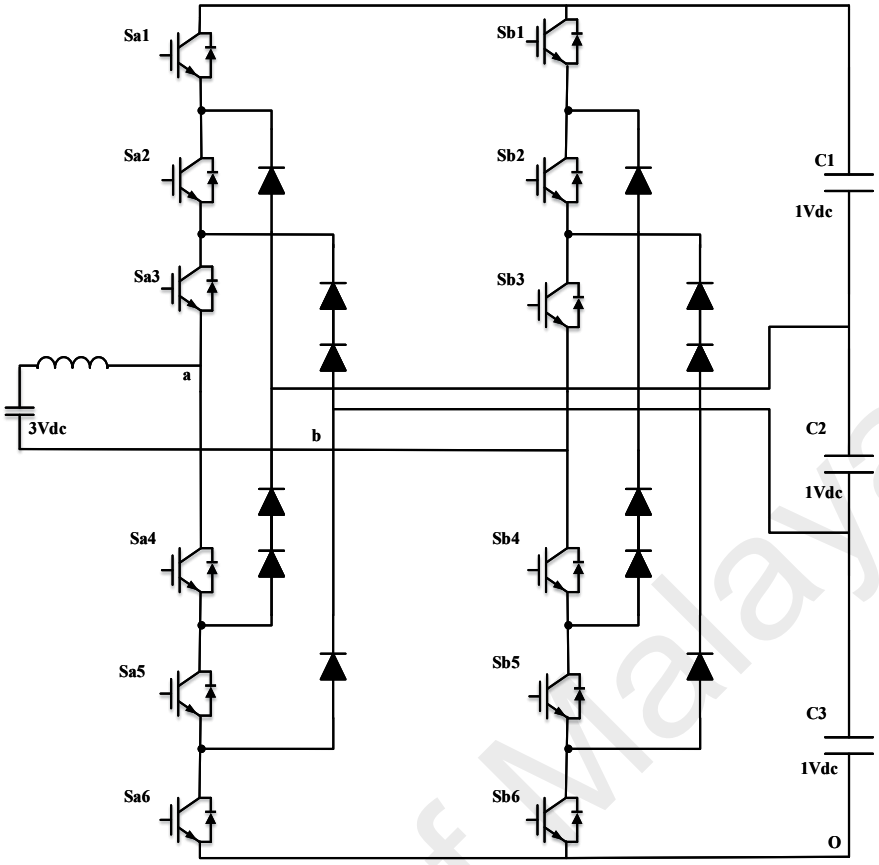


Figure 2-12: Four-level diode clamp DC/DC converter

Table 2-2: Combination of switching states Diode Clamp

Vao	Switching state (a)		
	Sa1	Sa2	Sa3
3Vdc	1	1	1
2Vdc	0	1	1
1Vdc	0	0	1
0	0	0	0

Vbo	Switching state (b)		
	Sb1	Sb2	Sb3
3Vdc	1	1	1
2Vdc	0	1	1
1Vdc	0	0	1
0	0	0	0

2.3.2 Flying Capacitor Multilevel DC/DC Converter

Figure 2.13 presents the four-level flying capacitor DC/DC converter. Following the diode clamp study, the switching states of the flying capacitor can be derived as stated in Table 2.3. It is obvious that this type of converter has additional redundant switching states. Grouping the switching state of V_{ao} equals to (2 V_{dc}) with V_{bo} equals to (1 V_{dc})

actually results in nine combinations of switching states to obtain V_{ab} equals to (1 V_{dc}), at the output side.

Table 2-3: Combination of switching states flying capacitor

Vao	Switching state (a)		
	Sa1	Sa2	Sa3
3Vdc	1	1	1
2Vdc	1	1	0
	1	0	1
	0	1	1
1Vdc	1	0	0
	0	1	0
	0	0	1
0	0	0	0

Vbo	Switching state (b)		
	Sb1	Sb2	Sb3
3Vdc	1	1	1
2Vdc	1	1	0
	1	0	1
	0	1	1
1Vdc	1	0	0
	0	1	0
	0	0	1
0	0	0	0

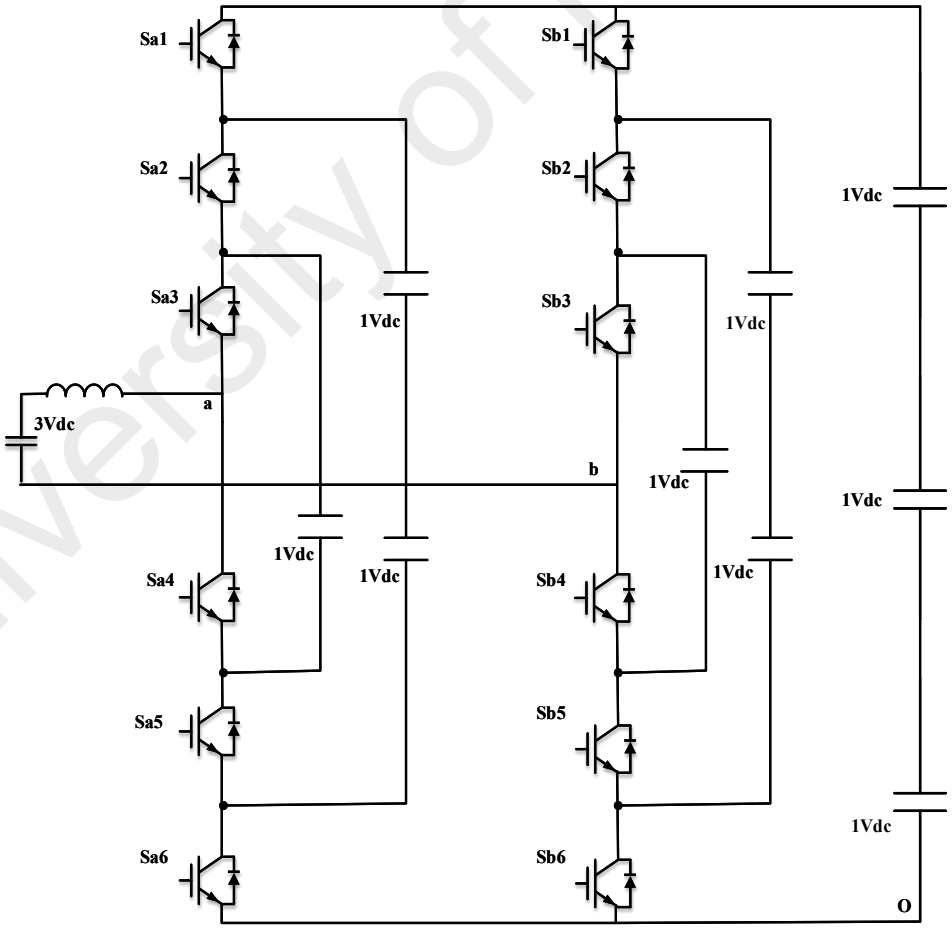


Figure 2-13: Four-level flying capacitor DC/DC converter

The other combination has three combinations of the switching states. Hence, additional redundant switching states are obtained, which simplify the selection of a proper switching states that maintain balanced voltages. Assuming that the converter's output and input are connected to the same ground, the voltage V_{bo} is equal to zero, which means that only the following combinations of the switching states (Sa1, Sa2, Sa3 = 100, 010, 001) are used to preserve the voltages balanced. Based on that, another topology of a four-level flying capacitor is derived as shown in Figure 2.14 (Adam et al., 2016; Fan et al., 2004).

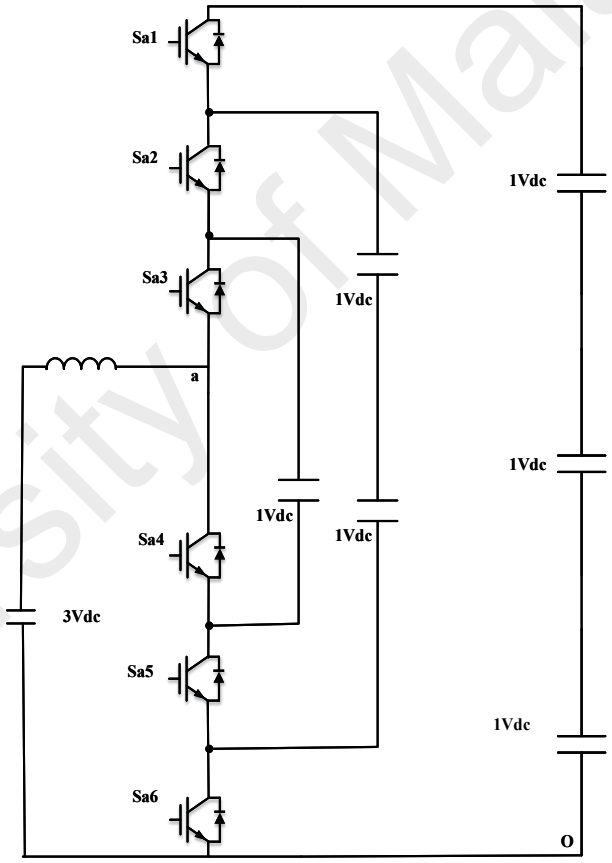


Figure 2-14: Four-level flying capacitor with the same grounding

There are some topologies which have a similar structure as the obtained flying capacitor converter such as the three-level DC/DC converter, which is similarly identical to the voltage doubler topology. Figure 2.15 illustrates it.

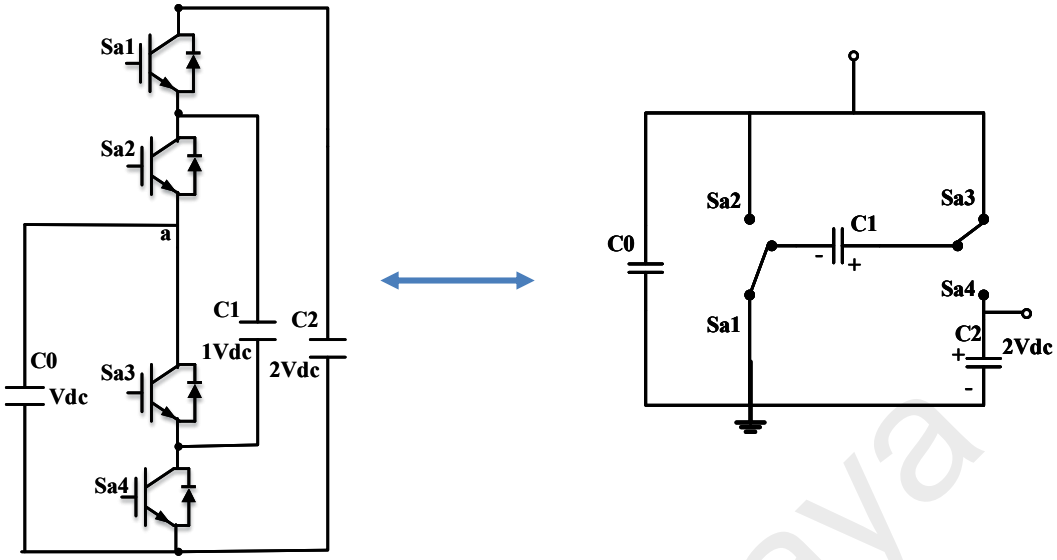


Figure 2-15: Three-level flying capacitor and traditional voltage doubler

2.3.3 Cascaded Multilevel DC/DC Converter

The cascaded DC/DC converters utilize two or more identical topologies to generate multilevel voltages. This topology offers many advantages like symmetrical element structure, self-feeding capability, and less voltage stress on power devices. A typical cascaded multilevel converter is shown in Figure 2.16. it is made from six cells. The control strategy is similar to the flying capacitor type converter and table 2.3 describes the different switching states available. Likewise, when the same grounding is needed, we just use the following switching states (Sa1, Sa2, Sa3 = 100, 010, 001). According to that, both point (a) and (b) are connected together, so the voltage V_{bo} is viewed as an output voltage. Therefore, a new topology can be obtained as shown in Figure 2.17. The control of this topology is very easy, just applying a 50% duty cycle to all switches with (Sa1) complements (Sa1'). After many cycles, every capacitor will be charged with the same voltage. Compared to the converter exposed in Figure 2.14, it has the same number of switches, but the number of capacitors is lower (Fan et al., 2004; Guo & Sun, 2016).

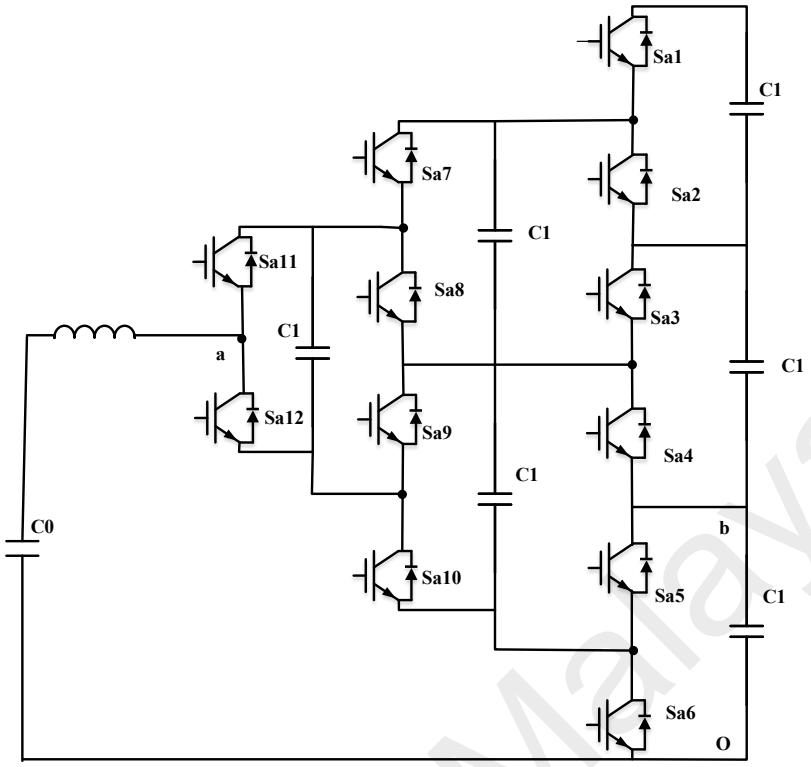


Figure 2-16: Generalized multilevel DC/DC converter

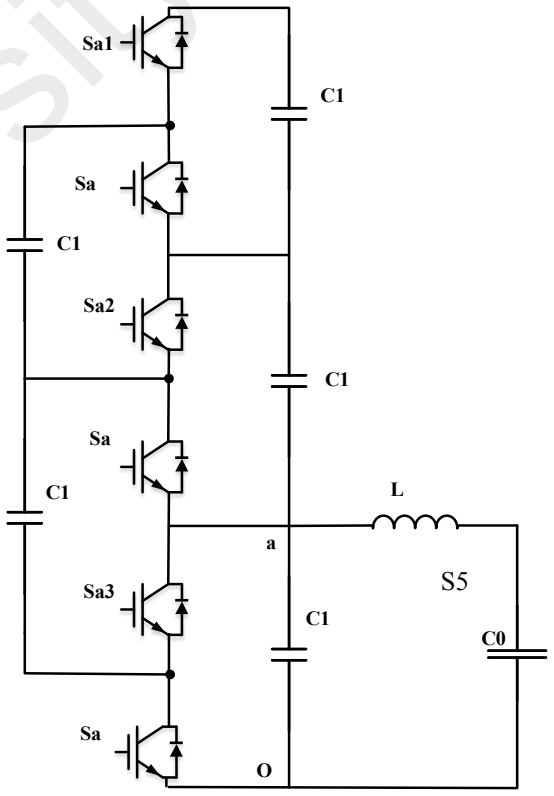


Figure 2-17: Simplified circuit from the generalized topology

Another configuration of cascaded converter can be seen in Figure 2.18. It has cascaded configuration in the high voltage part and parallel configuration in the low voltage part. It is suitable where high level of power is needed. Also, it can be fed by only one transformer or by several ones. The cascaded power converters in DC/DC applications have many advantages in term of modulation strategy and lower voltage stress, etc. It is one of the most suitable multilevel power converter for DC/DC applications (Filsoof & Lehn, 2016; C. Sun et al., 2016).

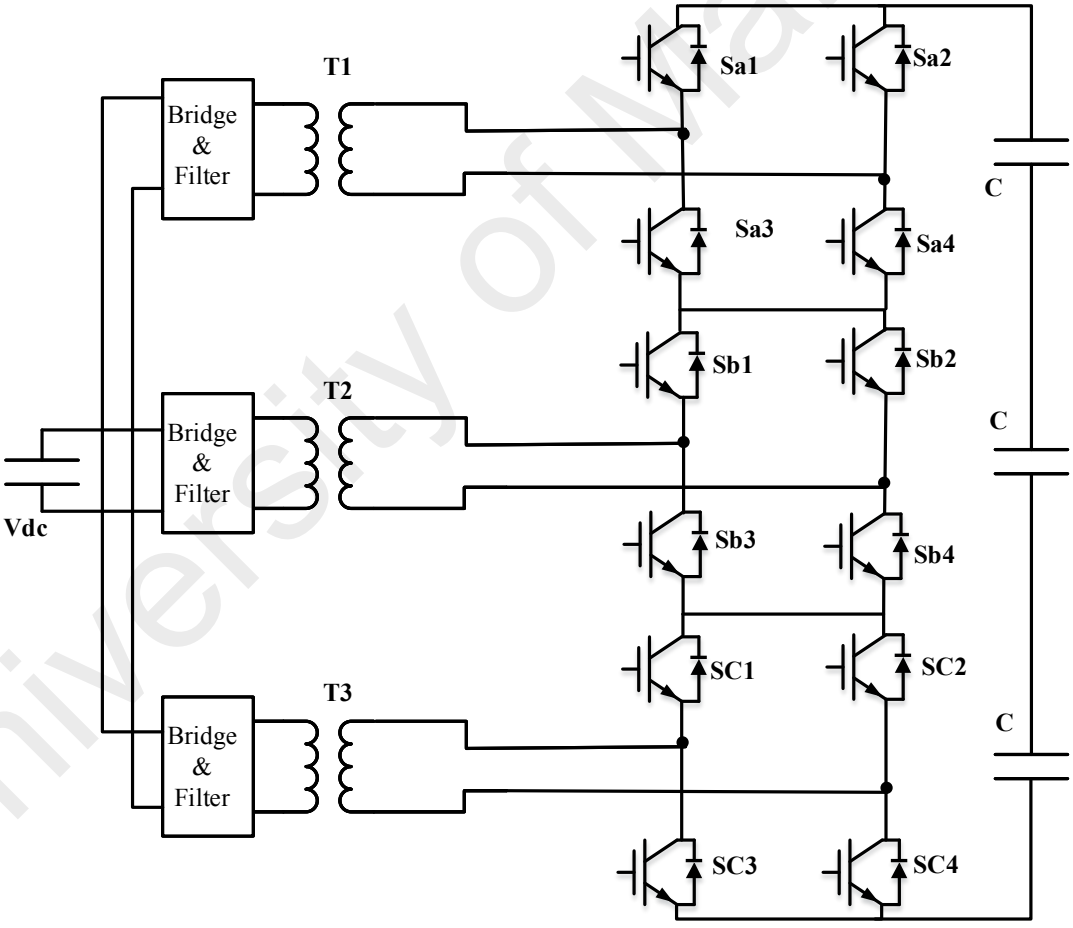
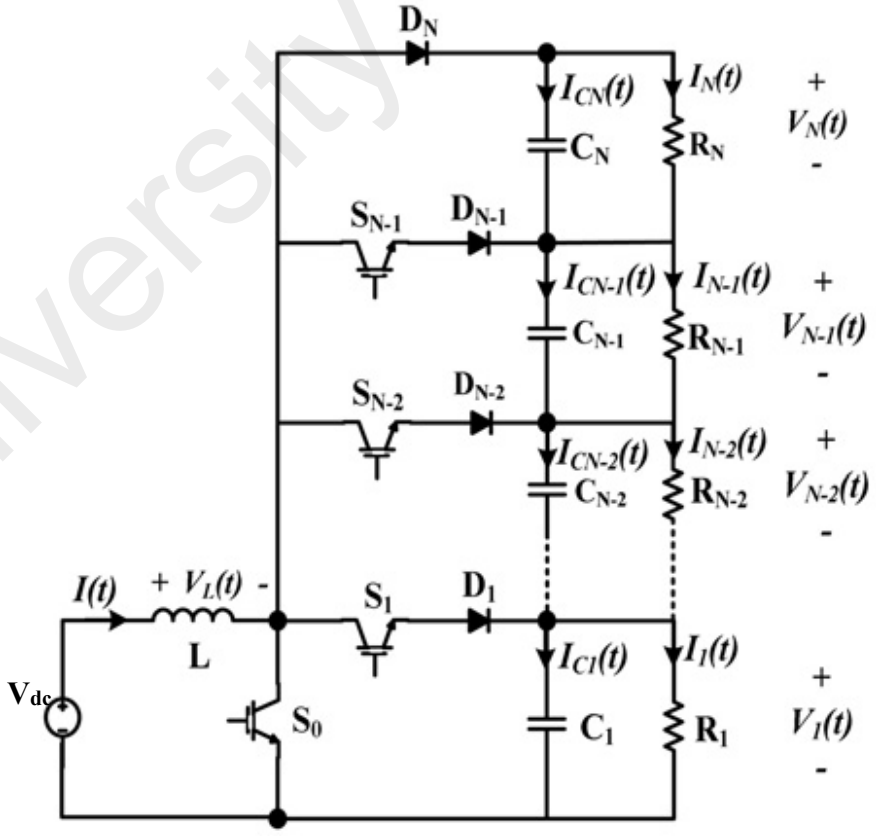


Figure 2-18: Cascaded multilevel DC/DC converter

2.4 Multi-Output DC/DC Converter

A new generation of single-inductor multiple-output (SIMO) DC/DC converters, based on buck or boost or buck-boost topologies, have been addressed in (Wing-Hung & Dongsheng, 2001). This approach has the advantage of reducing the number of external bulky components such as inductors and power switches to reduce the cost and losses in the system.

One of the most attractive topologies of this new DC/DC family is the multi-output boost (MOB) converter. The MOB shares the total voltage output with the series capacitors' voltages in low or high-power level. The N-output boost circuit diagram is exposed in Figure 2.19(a). The operation of a double-output boost converter is presented in Figure 2.19(b-d). It has three switching states as S1 cannot be Turned ON while S_0 is ON. This topology can be used to replace several DC power supplies to boost and regulate



(a)

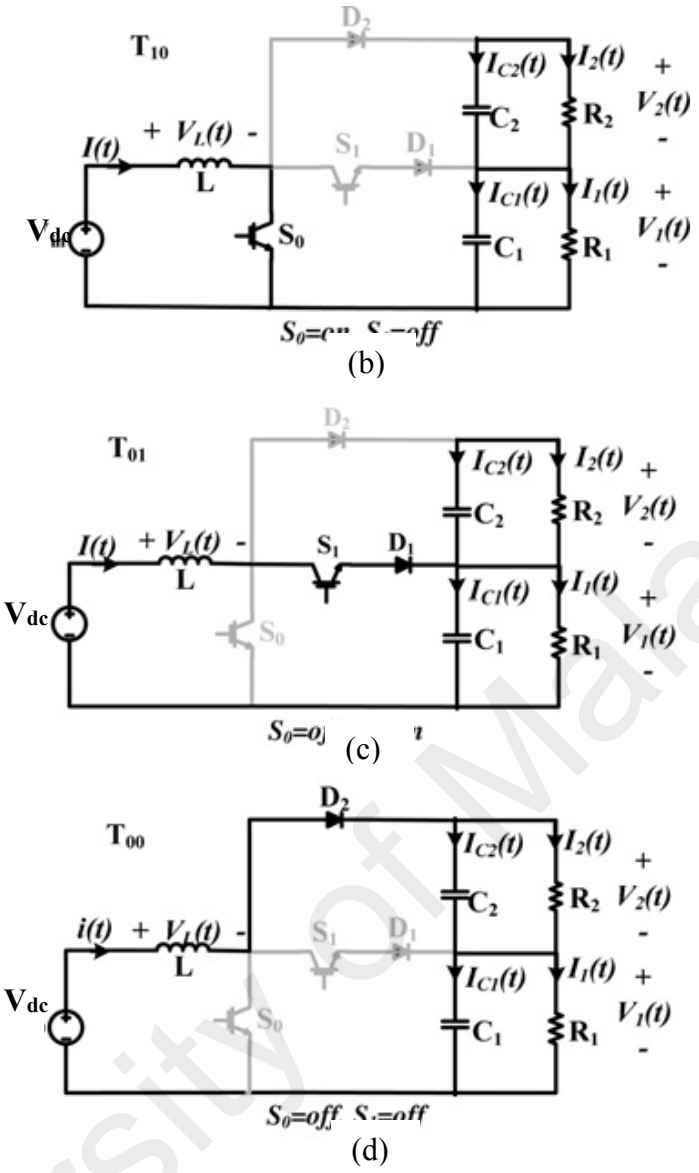


Figure 2-19: Multi-output boost converter

the low and variable output voltage from renewable energy system (Nami, Zare, Ghosh, & Blaabjerg, 2010). Moreover, using MOB converter at the DC link voltage of multilevel inverter can improve the DC-bus voltage balance in the inverter side, and even it can simplify the control of this multilevel inverter. Figure 2.20 shows the proposed DC/DC converter connected to a three-level diode-clamped inverter.

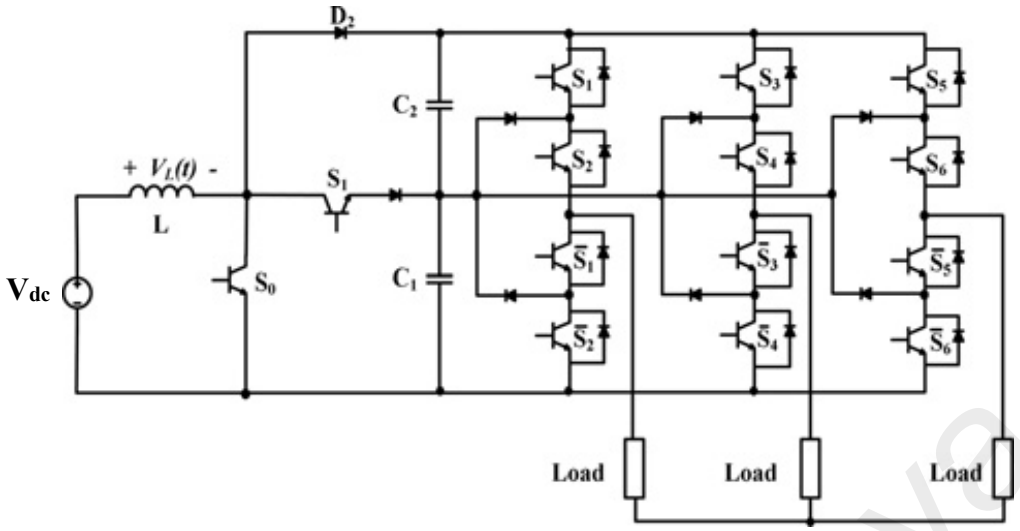


Figure 2-20: MOB connected to three-level NPC

2.5 Three-Level DC/DC Converter

In 1969, the three-level (TL) circuit topologies were developed for PC applications. They were to change normal calculation procedure from parallel rationale frame to ternary shape. It was first applied in inverters topologies then it was generalized to other type of conversion. A multilevel DC/DC converter is proposed by Pinheiro and Barbi to minimize the voltage stress of the switches. One way to reduce the voltage stress of a switch is by replacing the single switch with two switches connected in series and introducing some clamping diodes to have an equal distribution of voltage stresses between the series power devices (Narimani, Moschopoulos, & Wijeratne, 2013; Ruan, Li, Chen, Tan, & Tse, 2008). It is better to mention that the three-level technique in DC/DC conversion do not generate three-level output voltage as in DC/AC conversion (three-level inverters). For instance, the next section shows how to transform a single output buck converter to a three-level one.

2.5.1 Three-Level Buck Converter

To obtain a three-level buck converter from the conventional buck converter the following steps are used (Ruan et al., 2008):

- First replace the switch Q in the buck converter shown in Figure 2.21(a) by two switches Q1 and Q2 as appeared in Figure 2.21 (b).
- Secondly, connect a series of voltage sources at the input side of the converter to obtain a clamped voltage level. As the buck converter has a DC input source, the clamped voltage level is realized by putting in parallel with the DC input source two series capacitor so that the voltage input will be divided by 2, thus the voltage of each capacitor will be ($V_{dc}/2$). This changes the converter to that appeared in Figure 2.21 (c).
- Finally, bring a clamping diode D_c to attach the middle point of the voltage sources and the two switches together. The finished type of the three-level buck is appeared in Figure 2.21(d).

Referring to Figure 2.21(d), if the switches Q1 and Q2 are switched ON and OFF together simultaneously, the obtained output voltage over the LC filter will be identical to the normal buck converter that appeared in Figure 2.22(a). For this situation, the two-voltage level are (V_{dc}) and (0). Then again, if the converter works with Q2 is dependably ON and Q1 has a PWM control, the output voltage over the LC filter will be like that appeared in Figure 2.22(b). For this situation, the two voltages are (V_{dc}) and ($V_{dc}/2$). In this way, Three-level voltage are generated (Bottion & Barbi, 2013; Ruan et al., 2008).

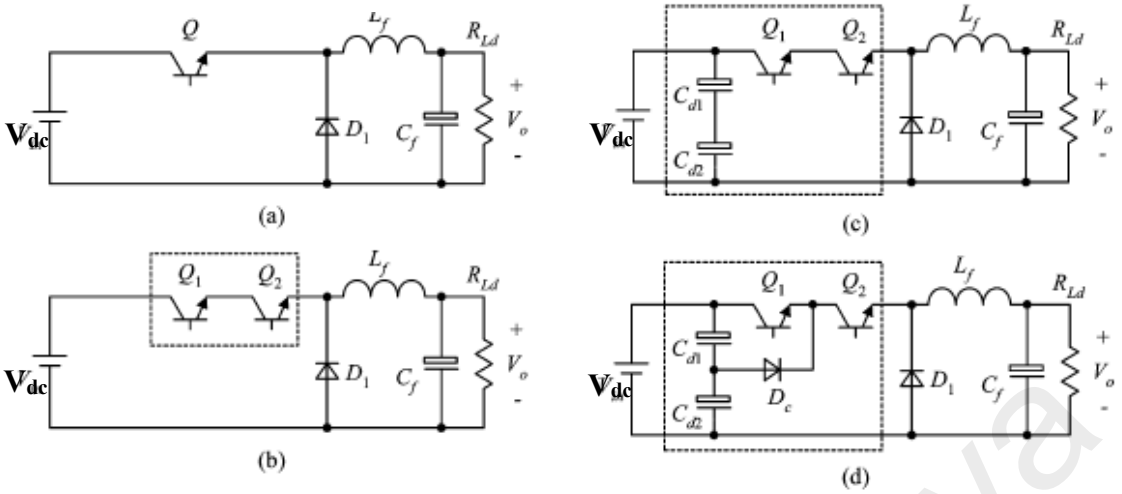
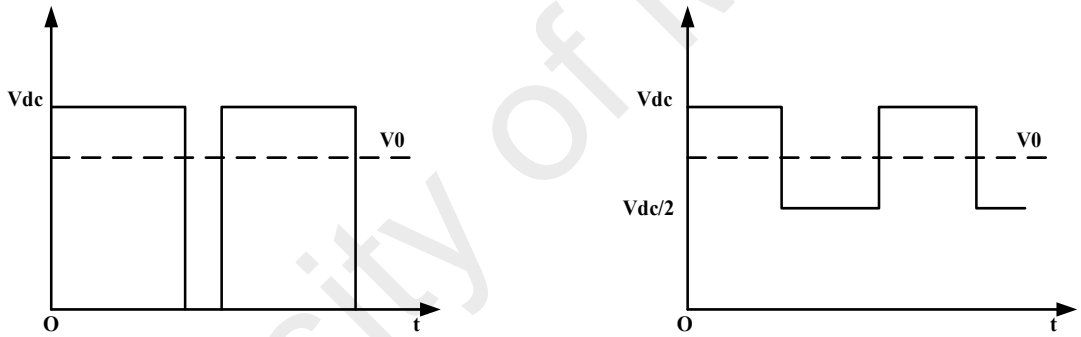


Figure 2-21: Construction of three-level buck converter from the conventional one



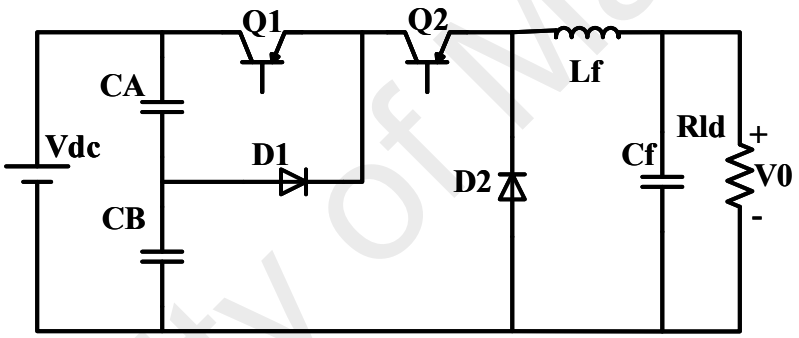
(a) Conventional buck converter (b) Three-level buck converter

Figure 2-22: Voltage across the filter

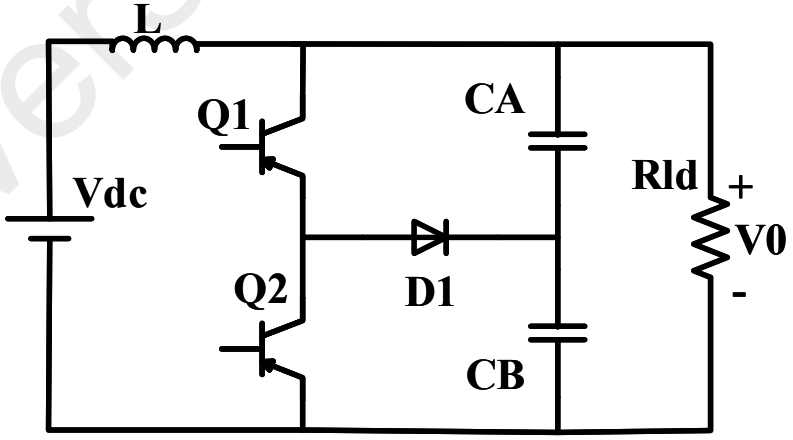
2.5.2 Family of Three-Level Converters

In view of the approach proposed for determining the three-level buck converter, a whole group of three-level converters for different topologies can be obtained. Figure 2.23 demonstrates the group of six non-isolated three-level converters; the buck, the boost, the buck-boost, Cuk, SEPIC, and Zeta converter. Concerning boost converter, the output voltage V_o is the switch's voltage stress. In this way, V_o is utilized as the clamping voltage source. Regarding the buck–boost, SEPIC, and Zeta converters, (V_{dc}+V_o) is the voltage stress on the switches. After all, in some circuit such voltage

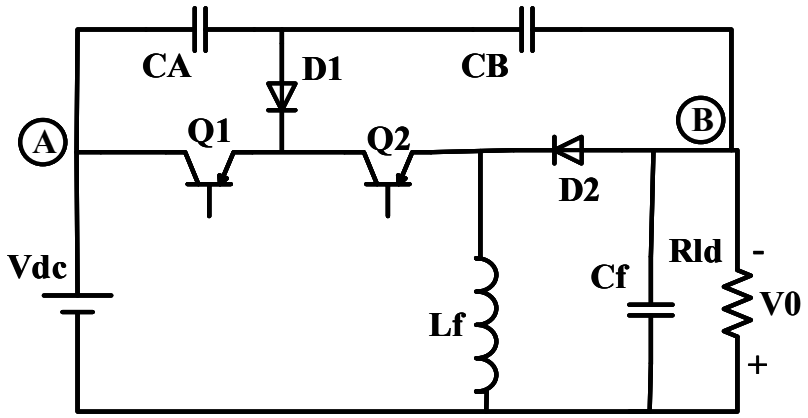
source is not easily obtainable, so it is important to produce it. Realizing that (V_{dc}+V_o) is evenly the voltage between points (A) and (B), to identical capacitors connected in series and put in parallel with the two-connecting point (A) and (B) are used to generate the clamping voltage sources as appeared in Figures 2.23[(c), (e), and (f)]. With respect to the Cuk converter, the switch's voltage stress is as well (V_{dc}+V_o), and such a voltage source is originated from the energy transfer capacitor. Consequently, this capacitor can be divided into two series capacitors (C_{b1}) and (C_{b2}), which are then utilized as the clamping voltage source appeared in Figure 2.23(b) (Bottion & Barbi, 2013; Narimani et al., 2013).



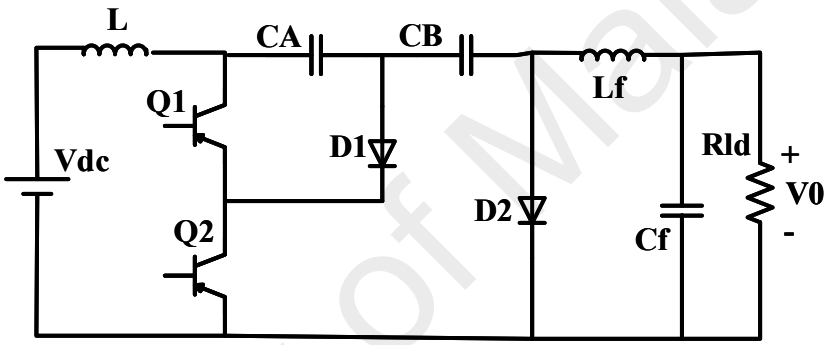
(a) Buck converter



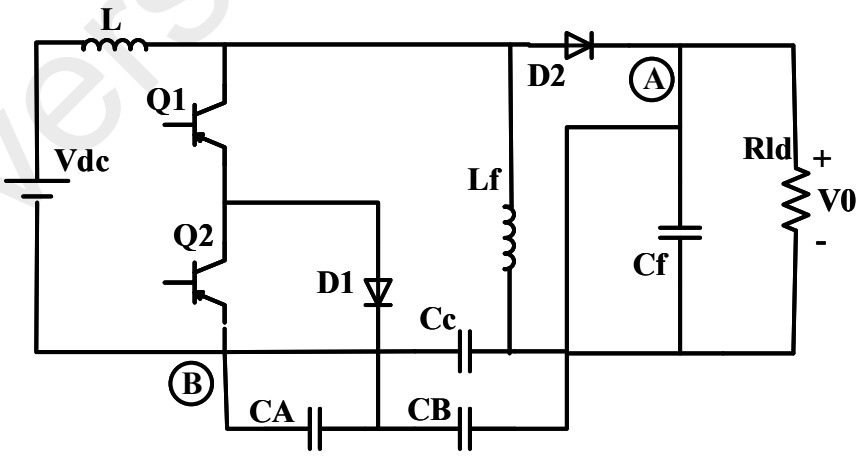
(b) Boost converter



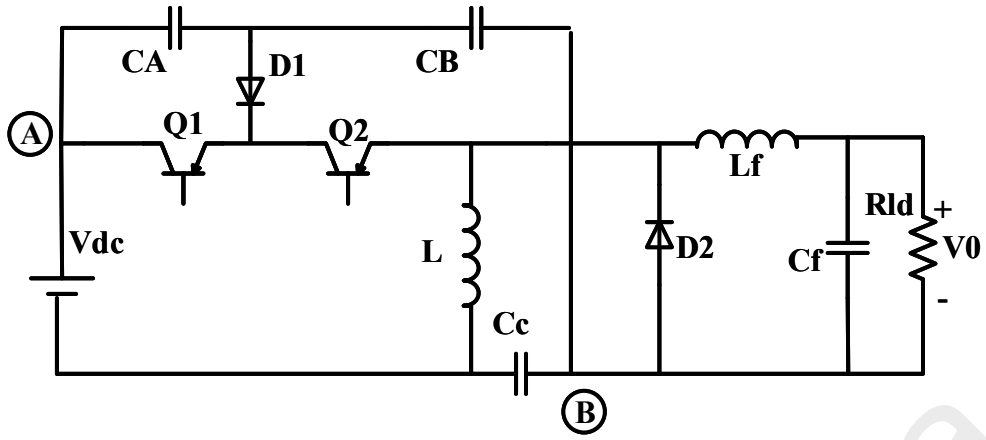
(c) Buck-boost converter



(d) Cuk converter



(e) SEPIC converter



(d) Zeta converter

Figure 2-23: Six non-isolated three-level DC/DC converter

2.6 Boundary Control Method

Controllers are an essential component in power conversion systems that have a significant impact on characteristic features such as performance, efficiency, size, and cost, among many others. During the last four decades, countless efforts have been made to find better controllers for power electronics systems in order to improve the converters steady state and dynamic behaviour, increase power densities and reduce losses in the system (C. Y. Chan, 2012; Konstantopoulos & Zhong, 2016).

Small-signal based linear controllers have been the preferred alternative during decades. This technique is characterized by fixed switching frequency and low computation/sensing requirements, while the dynamic response can be enhanced to just a restricted degree and the global stability cannot be guaranteed (Cvetkovic, Boroyevich, Mattavelli, Lee, & Dong, 2013). Further, exceptional dynamic performances and global stability are achieved by boundary controllers, in which the switching frequency is variable and faster sensors are required. Among the non-linear techniques, boundary controllers (BC) are a popular alternative for controlling DC/DC converters. Typically, the main benefit of this type of controllers is its fast and predictable transient response,

which in some cases reaches the physical limit of performance (He & Chung, 2015; I. Galiano Zurbriggen & Ordonez, 2014).

Switching boundary control is a geometric method. It was initially presented to power electronic system by Burns and Wilson in 1976 (Burns & Wilson, 1976). In boundary control, a state-plane is formulated to analyze the switching boundary of the power electronic system. It allows us to visualize the behavior of a nonlinear system commencing from different initial conditions, without solving the nonlinear system systematically (Munzert & Krein, 1996). A switching boundary denoted by σ is utilized to split the state-plane into two regions, one is the ON-state region and the other is the OFF-state region, so that the converter switching is moving between them. Derivation of switching boundary depends on the system behaviour appeared in state-plane analysis (Onwuchekwa & Kwasinski, 2011). In the following, a concise outline of the basic concepts of boundary control comprising state-plane, switching boundary, and stability analysis.

2.6.1 State Plane Analysis

State-plane analysis is a graphical technique for reviewing a second-order system. The fundamental concept of this technique is to develop the system's state-plane by plotting the motion trajectories of a system with different initial conditions, and then to inspect the standard characteristics of these trajectories (Wang, Chung, & Presse, 2009). The dimension of state plane is equivalent to the number of state variables in the system, and the number of switching combination is equal to the trajectory families' number. Concerning the family of DC/DC converters, almost all the trajectories have spiral forms or hyperbolae one. The ON and OFF state trajectories are interconnected at the equilibrium points of the converter (I. Galiano Zurbriggen & Ordonez, 2014).

On the other hand, based on the study of the state-plane, if the converter's switching frequency goes to for a specific duty ratio, the converter converges to only one operational point which is present in the state-plane. A loadline is a curve formed from these operating points which are obtained during the duty cycle value variation. The switching surface together with the loadline determine the power converter's operating point at the steady-state. Figure 2.24 presents a family of state-trajectory relating to a conventional boost converter (K. K. S. Leung & Chung, 2004a; Yan, Ho, Chung, & Au, 2009).

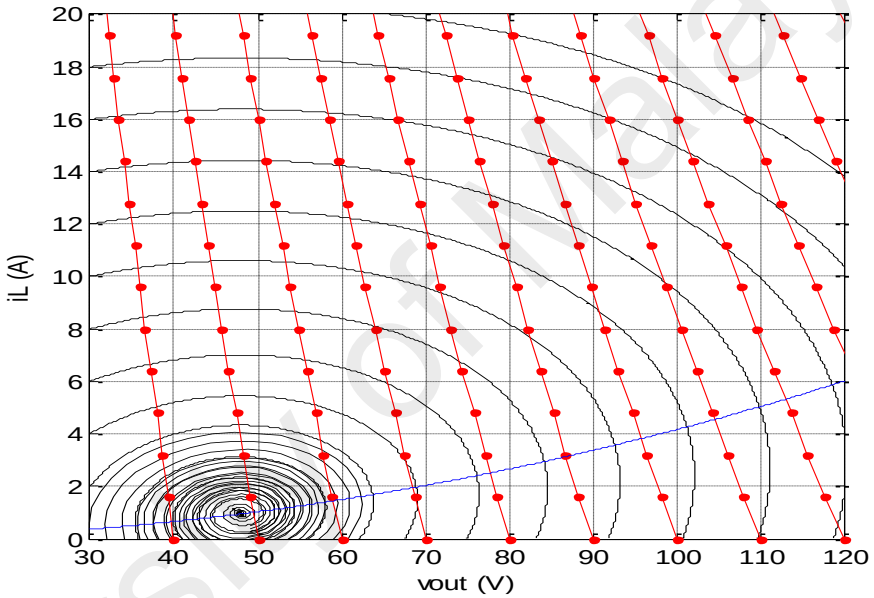


Figure 2-24: State plane of boost converter

2.6.2 Switching Surface

A switching boundary denoted by σ is a surface which is exploited to divide the state-plane into disjointed areas. According to Bass and Krein, 1990, the switching boundaries that appear in power electronic systems can be classified into four categories. They are bidirectional stationary (BS), bidirectional moving (BM), unidirectional stationary (US) and unidirectional moving (UM). The commonly used switching boundary is a sliding surface in sliding mode control. It is classified as bidirectional boundary that the switching action occurs on both sides of the surface (I. G. Zurbriggen, Ordonez, &

Bianchi, 2015). Sliding properties give robust performance. Nevertheless, when the converter is working in different conditions its dynamic performance will be differed. Consequently, adaptable hysteresis or adaptive controller are proposed to maintain the good dynamic performance of the system (P. K. W. Chan, Chung, & Hui, 2007). Another switching boundary is hysteresis band control. It is considered as a unidirectional boundary that the switching action occurs in only one side of the surface. Most of these controller are classified as first-order switching surface (Munzert & Krein, 1996; Schild, Lunze, Krupar, & Schwarz, 2009).

Another technique based on state-trajectory prediction is proposed by Leung and Chung, 2004, and is further developed to second-order switching surface. The proposed method is closed to the ideal switching surface. It is used to estimate the state-trajectory movement of the system after a hypothesized switching action. It is load-independent and does not require sophisticated calculation (K. K. S. Leung & Chung, 2004b). A comparative study between first-order and second-order switching surface was carried out in buck converter by the same authors. The investigation showed that the converter with second-order switching surface exhibits a better dynamic response (K. K. S. Leung & Chung, 2007; K. S. Leung & Chung, 2005).

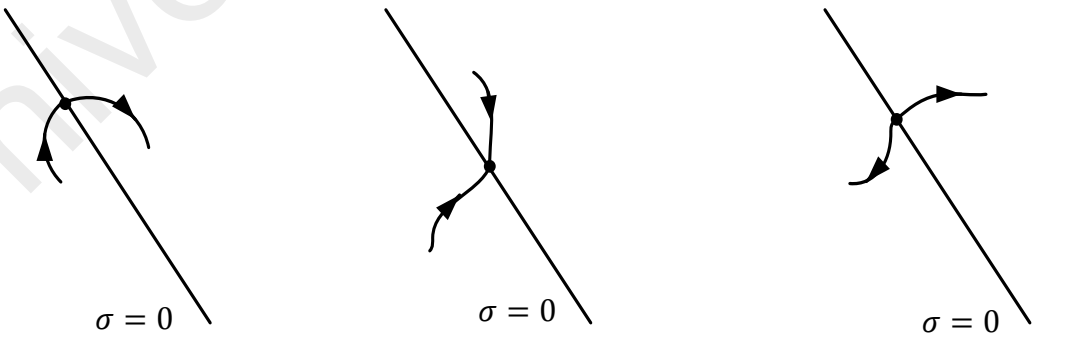
2.6.3 Stability and Switching Surface Behaviour

With regard to trajectory formation behaviour at the boundary, a given point along the switching surface σ has to be categorized as one of the following three categories (Munzert & Krein, 1996):

- **Refractive points**: is a point on the switching surface that has refractive behaviour. Figure 2.25(a) illustrates this mode where the trajectories approach the switching surface σ in one side of the boundary and go away from σ on the other

side. This expands the refractive behaviour, where the system trajectory suddenly shifts the direction at a boundary crossing. A system operates in refractive mode is considered as large-signal stable if and only if the successor points from one side of the boundary are moving toward the target operating point. Otherwise, the system is considered as large-single unstable (Ordonez, Iqbal, & Quaicoe, 2006).

- **Reflective points**: in this case, the state trajectory is oriented in the direction of the switching surface on both sides. For this situation, the switching action directly diverts the system back without permitting the boundary to be crossed. The control of converters functioning in this mode is recognized as sliding regime. Figure 2.25(b) demonstrates this mode; the converter will exhibit robust control and large signal stability (Munzert & Krein, 1996).
- **Rejective points**: trajectories are moving away from both sides of the boundary as shown in Figure 2.25(c). Switch action can't impose the state to go toward the boundary, hence the state will never reach the operating point. It makes the system unstable. In practice, it is preferable to prevent the converter from operating in this mode in order to achieve a controllable system (Peña-Alzola, Ksiazek, Ordonez, Wang, & Blaabjerg, 2015).



(a) Refractive (b) Reflective (c) Rejective

Figure 2-25: Trajectory behavior along the switching surface

Despite the fact that stability and robustness are the benefits of boundary control method, other factors like variation of the switching frequency, errors in the steady-state output voltage, and the needs of measuring all state variables are the problems of this technique (He, Chung, Ho, & Wu, 2016; Munzert & Krein, 1996). Practically, the bidirectional stationary switching surface can't be used as a straight application for controlling circuits. Theoretically in the case of a stable switching surface, the process of turning ON and OFF the switches goes very fast when the converter functions within the sliding region or close to converter's operating point in refractive region, this phenomenon is known as chattering. Chattering effect is undesirable in practice and is considered as the main drawback in standard sliding mode control. It includes high control activity which can bring high frequency to the system and consequently lead to high switching losses and electromagnetic interference problem (Galvez, Ordonez, Luchino, & Quaicoe, 2011; Nie & Brown, 2015).

2.7 Summary

In this chapter, the theoretical concept of multilevel converter is presented. It starts with a description of the basic traditional multilevel inverters, followed by the recent topologies proposed by researchers in the field of DC/AC conversion. In addition, a detailed description of multilevel DC/DC converter is carried out. It focuses on the demonstration of different types of conventional multilevel DC/DC converter such as diode clamped, flying capacitor, and cascaded configurations. Other topologies made from the well-known DC/DC converters (buck, boost, cuk …) are also presented. Besides that, a detailed explanation of the control technique used in this work is provided. The control technique is based on boundary control using second-order switching surface. Furthermore, stability analysis within this control is explained.

CHAPTER 3: PROPOSED MULTILEVEL TOPOLOGY

3.1 Introduction

Multilevel converters that produce AC voltage waveforms from DC sources are very useful in several industrial applications. An ordinary multilevel inverter contains a power converter and a controller. The power converter treats the power; it is typically executed by specific topologies that produced multilevel voltages. The controller governs the operation of the power converter and it is an essential variable that has an impact in the converter's performance.

Since the idea of multilevel converter was presented, different control methods have been proposed and evaluated in details, for example, multilevel sinusoidal PWM, multilevel selective harmonic elimination, and space vector modulation. Among these techniques, the space vector PWM (SVPWM) has attracted attention due to its higher output voltage for the same DC-bus voltage, reduced switching losses, improved harmonic performance and provides important flexibility in choosing between different redundant switching states, as well as its suitability for digital implementation (Gaur & Singh, 2014; Maheshwari, Busquets-Monge, & Nicolas-Apruzzese, 2016).

Depending on the type of the multilevel converter, different voltage feeding sources are used to feed the multilevel converters. The simplest method is by using many isolated DC power sources, but in some applications, different DC power sources are not wanted to keep up every voltage level in these multilevel converters. Instead, each voltage level can be maintained by a capacitor and a voltage balancing circuit that keep each voltage level. In this aspect, a new topology is proposed which is based on a multilevel inverter fed by multilevel DC/DC converter (Alishah et al., 2016). A complete study of the proposed configuration from topology viewpoint is conducted, followed by designing a

space vector modulation to control the multilevel inverter. Furthermore, a control strategy for the multilevel DC/DC converter based on switching boundary control is presented.

3.2 Description of the New Topology

The proposed three-level topology is shown in Figure 3.1. It is formed of a Dual-Output Boost Converter (DOBC), known as three-level inverter, connected to a three-level voltage source inverter. The DC/DC boost converter is used to increase the DC input voltage and maintain a balanced DC output voltage between the two capacitors C1 and C2, while the three-level inverter (TLI) generates the desired three-level output voltage. This configuration is well suitable for renewable energy systems such as PV and wind turbine systems. As the output voltage from these sources are not constant and have low level of voltage, the DC/DC converters are used to boost and regulate these voltages, then feed the DC-bus voltage of the multilevel inverter.

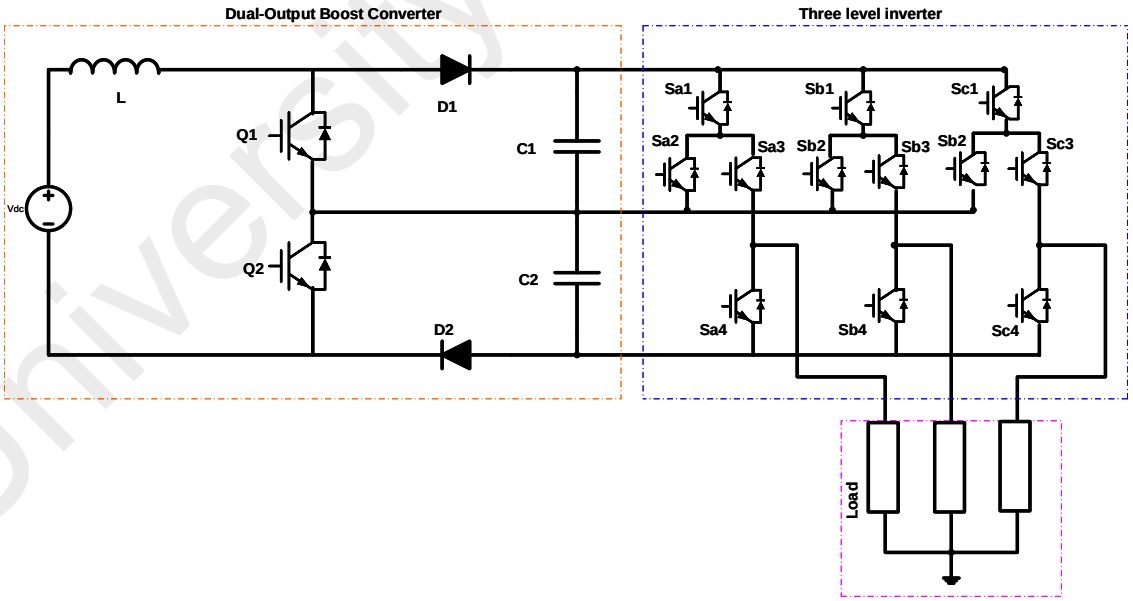
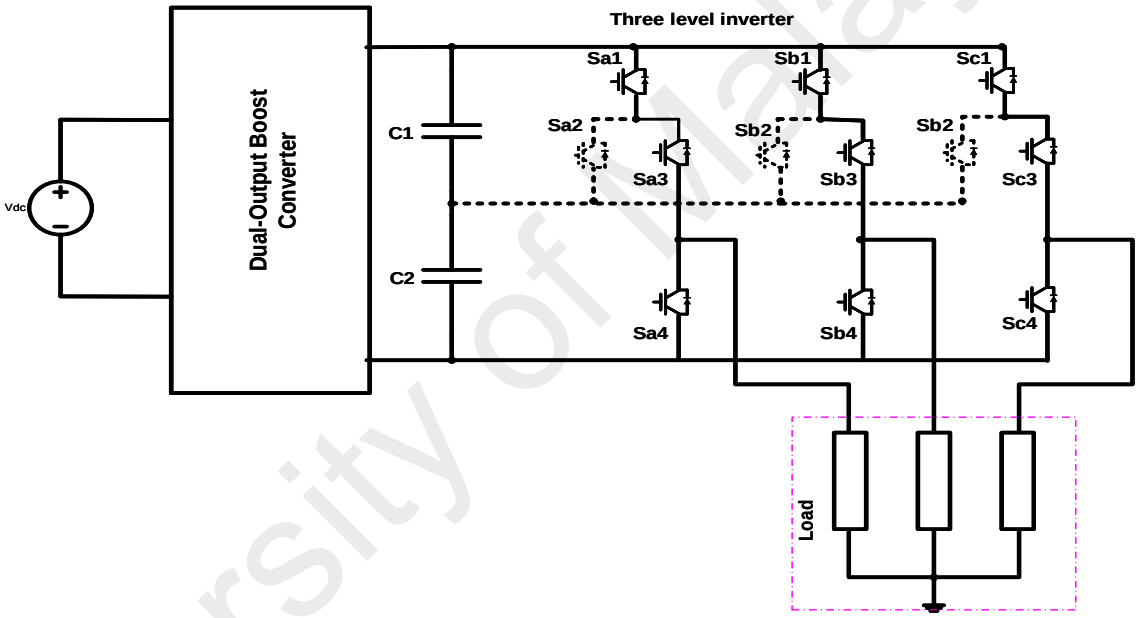


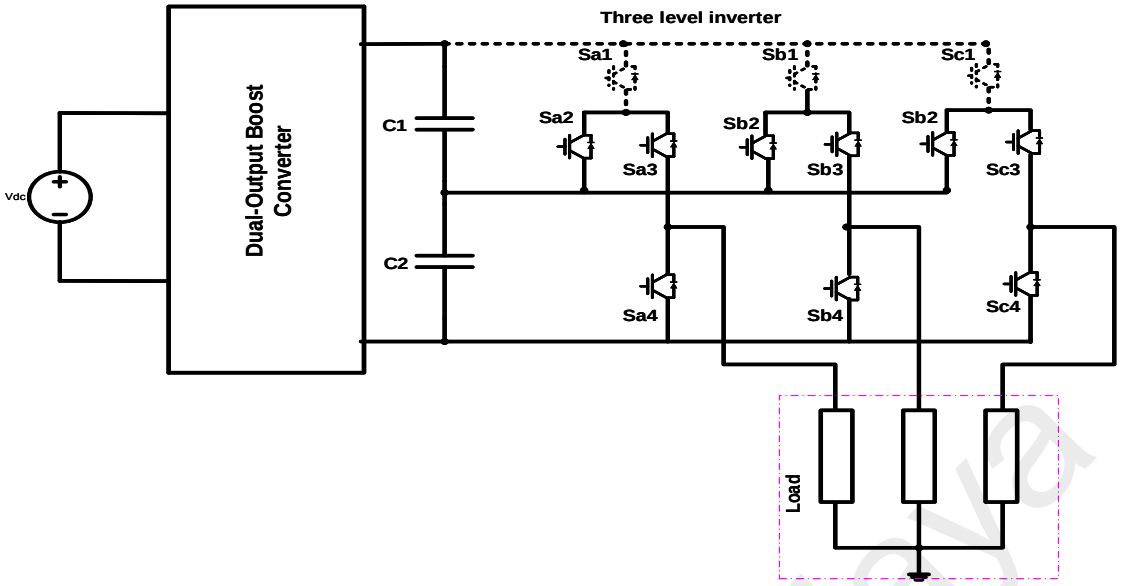
Figure 3-1: The proposed Three-Level inverter topology

3.2.1 TLI Working Principle

Referring to Figure 3.2 if the pair of switches in the TLI ((Sa1, Sa3), (Sb1, Sb3), (Sb1, Sb3)) are used the configuration looks like a two-level inverter with full DC bus. Otherwise, if ((Sa2, Sa3), (Sb2, Sb3), (Sb2, Sb3)) are used the configuration also looks like a two-level inverter with half DC-bus. A combination of these switching states will lead to an output voltage of (–V, -V/2, 0, V/2, V). However, this topology needs to maintain an equal DC-bus voltage, which will be carried out by controlling the dual-output boost converter.



(a) Equivalent two-level inverter with full DC bus



(b) Equivalent two-level inverter with half DC bus

Figure 3-2: Operation Principle for the three-level inverter

3.2.2 Dual-Output Boost Converter Operation Mode

The circuit configuration of the proposed DOBC is shown in Figure 3.3. It consists of a DC source V_{dc}, two power switching devices (Q1, Q2), one inductor L, two fast-recovery diodes (D1, D2), two DC capacitors (C1, C2) and two loads (R1, R2).

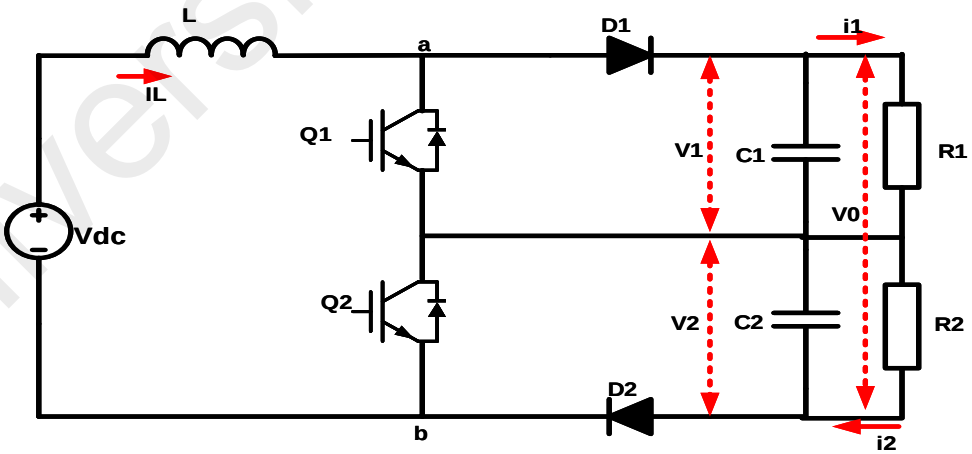


Figure 3-3: Proposed DOBC topology

The proposed configuration has the benefit of having less current ripple about four times if compared to the conventional boost converter, hence four times less inductance than it, which mean high efficiency and low cost. According to Figure 3.4, the output voltage of this converter is governed by the switching pair {(Q1, Q2), (D1, D2)}, and

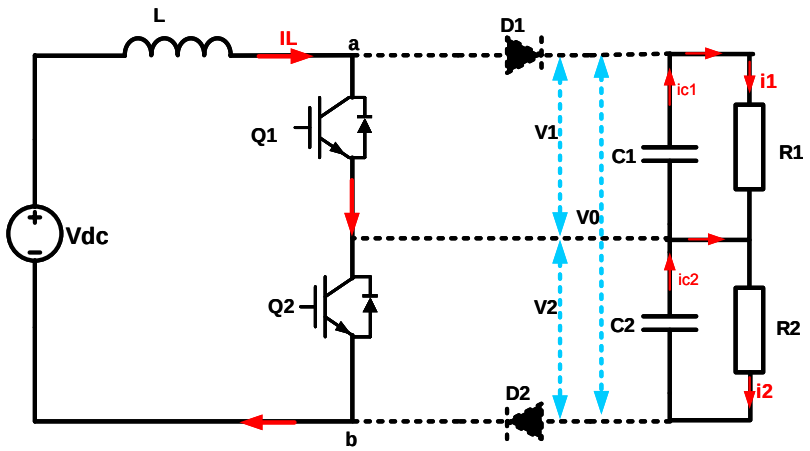
hence four modes can be observed according to switches' state (Bor-Ren & Hsin-Hung, 2000);

- **Mode 1:** Switches (Q1, Q2) are turned ON and diodes (D1, D2) are OFF. The inductor current is increasing and the two capacitors are discharged to supply the load. Figure 3.4(a) illustrates this mode and the state-space equation is:

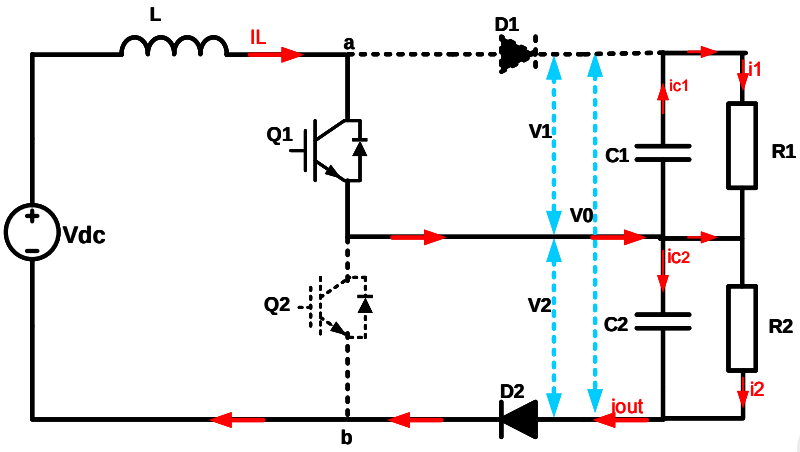
$$\begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix}' = \begin{bmatrix} 0 & 0 & 0 \\ 0 & -\frac{1}{R_1 C_1} & 0 \\ 0 & 0 & -\frac{1}{R_2 C_2} \end{bmatrix} \begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix} V_{dc} \tag{3.1}$$

- **Mode 2**: Switch Q1 is turned ON, Q2 is turned OFF, diode D1 is reverse biased and D2 conducts current. The input source is delivering energy to C2. The input slope is positive if V_{dc} is higher than V_2 and negative in otherwise. Figure 3.4(b) presents this mode and the state-space equation is defined as

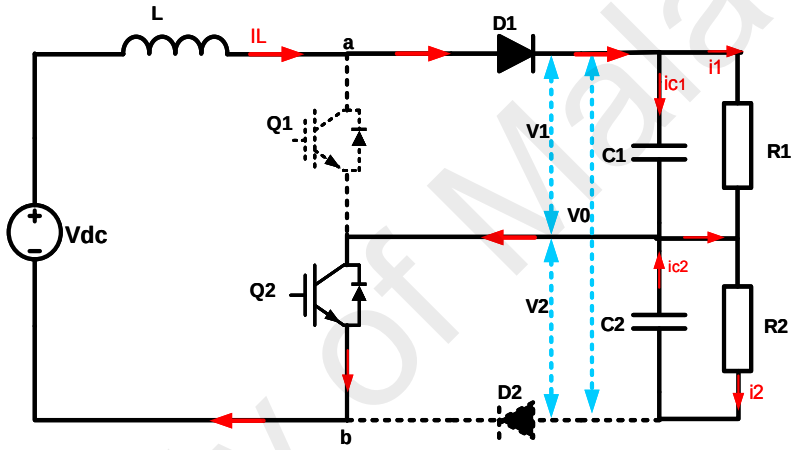
$$\begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix}' = \begin{bmatrix} 0 & 0 & -\frac{1}{L} \\ 0 & -\frac{1}{R_1 C_1} & 0 \\ \frac{1}{C_2} & 0 & -\frac{1}{R_2 C_2} \end{bmatrix} \begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix} V_{dc} \tag{3.2}$$



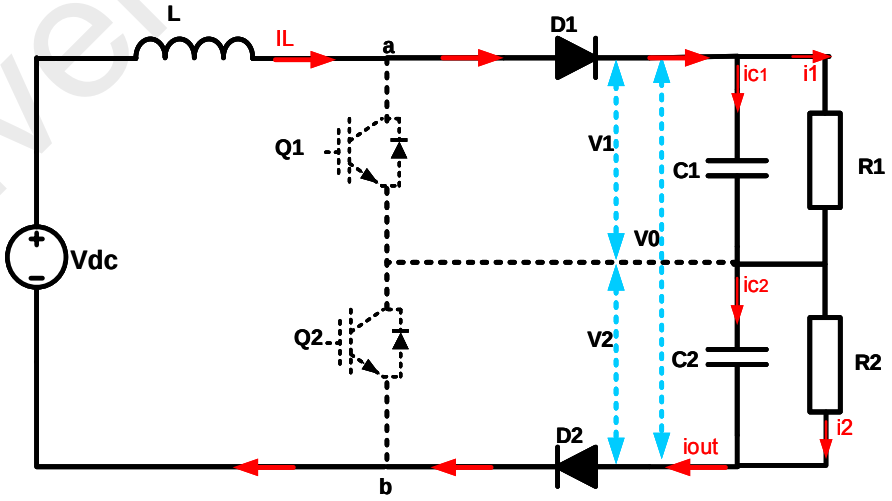
(a) Mode 1



(b) Mode 2



(c) Mode 3



(d) Mode 4

Figure 3-4: Operation modes of the DOBC

- **Mode 3:** As shown in Figure 3.4 (c), Q2 is turned ON, Q1 is turned OFF, D2 is reverse biased and D1 conducts current. The input current flows through the output of C1. If the input voltage is lower than V_1, the input current is negative, otherwise it is positive. The state-space equation is defined by

$$\begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix}' = \begin{bmatrix} 0 & -\frac{1}{L} & 0 \\ \frac{1}{C_1} & -\frac{1}{R_1 C_1} & 0 \\ 0 & 0 & -\frac{1}{R_2 C_2} \end{bmatrix} \begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix} V_{dc} \tag{3.3}$$

- **Mode 4:** As presented in Figure 3.7(d), Switches (Q1, Q2) are turned OFF and diodes (D1, D2) are ON. The input current flows through both capacitors and the input current is negative. The state-space equation is:

$$\begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix}' = \begin{bmatrix} 0 & -\frac{1}{L} & -\frac{1}{L} \\ \frac{1}{C_1} & -\frac{1}{R_1 C_1} & 0 \\ \frac{1}{C_2} & 0 & -\frac{1}{R_2 C_2} \end{bmatrix} \begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix} V_{dc} \tag{3.4}$$

3.2.2.1 DOBC Working Principle

Assuming a balanced output voltage for the DOBC where V_1 is equal to V_2, it is basically clear that the converter has two possible operating regions defined as follows (Bor-Ren & Hsin-Hung, 2000):

- **Region I ($V_{dc} < V_1$ & $V_{dc} < V_2$):** when this condition is satisfied. the inductor gets charged to a level of voltage equal to V_{dc}, which can be discharged to feed any chosen capacitor. As shown in Figure 3.5, during the starting time t_0 both switches Q1 and Q2 are in the ON state. The inductor is charged to (V_0-V_{dc}). At time t_1, which is determined by the control algorithm, Q2 is changed to the OFF state, obliging the current to pass through the capacitor C2 and Diode D2. Thus, ($V_0/2$ - V_{dc}) is the obtained discharge voltage. At time t_2, also determined by the control algorithm, Q2 is returning to its previous state which is the ON state. At certain time t_3, Q1 is turned

OFF, the inductor current passes by the diode D1, capacitor C1, and switch Q2; the discharged voltage is also equal to ($V_0/2 - V_{dc}$). Then at certain time t_4 Q1 is turned ON again. As consequence, the capacitors voltages are theoretically balanced because the inductor's gained energy is alternatively used to charge the upper and lower capacitors.

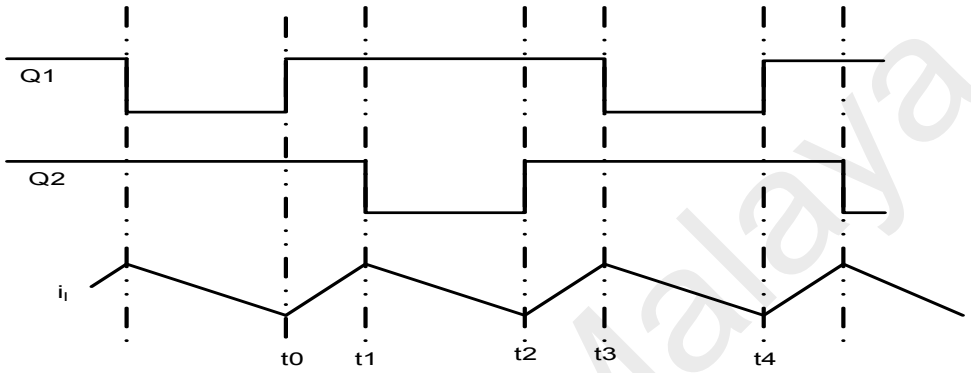


Figure 3-5: Switching sequence in region I

- **Region II ($V_{dc} > V_1$ & $V_{dc} > V_2$):** when this condition is fulfilled, the charging voltage is ($V_{dc} - V_0/2$), and the discharging voltage is ($V_0 - V_{dc}$). As shown in Figure 3.6, at the beginning of the switching cycle t_0 one switch is ON the other is OFF, for example Q1 is ON and Q2 is OFF, the input current passes through Q1, C2 and D2 and the charging voltage is set to be ($V_{dc} - V_0/2$). At a certain time t_1 decided by the controller, Q1 is turned OFF, so the current flows through D1, C1, C2 and D2, and the discharge voltage is ($V_0 - V_{dc}$). At certain time t_2, the same process will be repeated for Q2 and a balanced output is achieved.

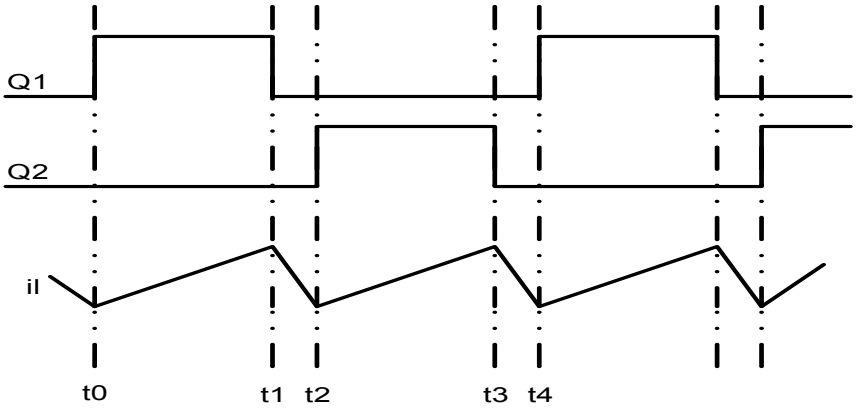


Figure 3-6: Switching sequence in region II

Based on the operation mode analysis, Table 3.1 summaries the working principle of the DOBC. A comparison between the input voltage and the output voltages V_1, V_2 will determine the region of operation. If the DOBC operates in region I, the boost ON mode will charge the voltage with Vdc and the OFF mode discharge it either by (V_1 - V_{dc}) or (V_2 - V_{dc}). On the other hand, if the converter is controlled in region II, the boost ON mode will be charged with either (V_{dc} - V_1) or (V_{dc} - V_2) and the OFF mode discharge it by (V_0 - V_{dc}).

Table 3-1 Working Principle of the DOBC

	Satisfied conditions	Boost state	Switches state (Q1,Q2)	Mode of operation
Region I	$V_{dc} < V_1$ & $V_{dc} < V_2$	ON	(1,1)	Mode 1
		OFF	(1,0) or (0,1)	Mode 2 or Mode 3
Region II	$V_{dc} > V1$ & $V_{dc} > V2$	ON	(1,0) or (0,1)	Mode 2 or Mode 3
		OFF	(0,0)	Mode 4

3.3 Control Law of the Proposed Configuration

Figure 3.7 illustrates the full topology and control of the proposed three-level inverter. As mentioned before, the configuration is composed of a new topology of three-level voltage source inverter (TLI) fed by a dual-output boost converter to maintain the capacitor voltage balancing of the inverter. The control Law for the proposed configuration can be divided in two parts, one is the control of the DC/DC converter to achieve a balanced DC-bus, and the second is the control of the three-level voltage source inverter. As the DC/DC converter side is required to boost and regulate the input voltage of the TLI, the control of the three-level inverter will be simplified to a conventional space vector modulation.

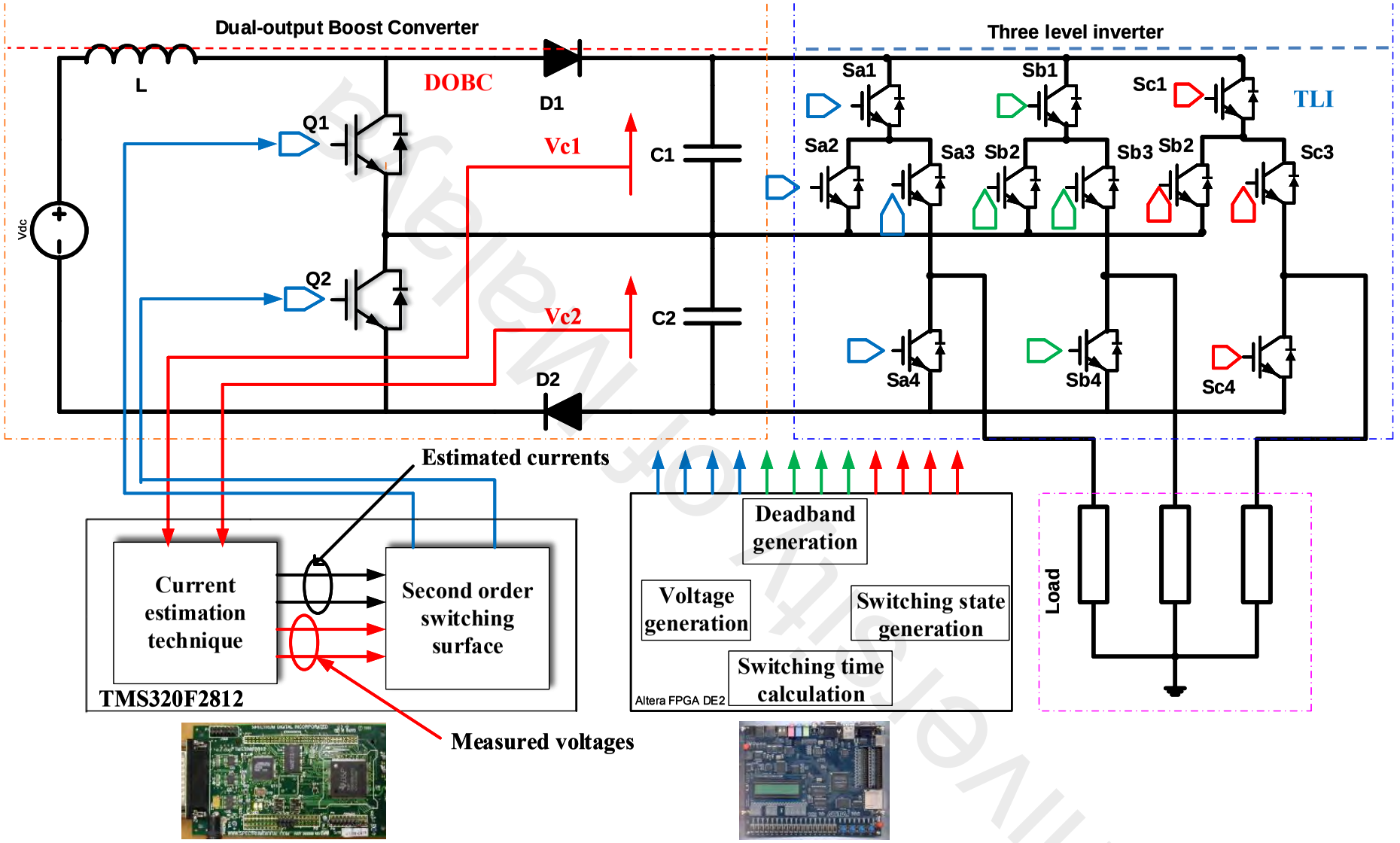


Figure 3-7: The proposed control of the three-level voltage source inverter

3.3.1 Control of the Three-Level Inverter

The control of the proposed three-level inverter is based on space vector modulation. The application of space vector modulation for a three-level topology requires a vector V_{ref} rotates within a hexagon. This vector represents the instantaneous three-phase output voltage. As shown in Figure 3.8, the hexagon is divided into six sectors and each sector contains four triangles that describe the switches ON and OFF states. Identifying the immediate sector and triangle where V_{ref} is positioned, will synthesize the switching sequence and allow the calculation of each vector component with its modulating period. Regarding the first issue which is sector and triangle identification many techniques have been proposed and applied by researcher, the one adopted in this work is as follows:

1. Mapping the orthogonal set of axes (αβ) onto three non-orthogonal set of axes (XY) shown in Figure 3.4 using the following three matrixes

$$H1 = \begin{bmatrix} 1 & -\frac{1}{\sqrt{3}} \\ 0 & \frac{2}{\sqrt{3}} \end{bmatrix},\ H2 = \begin{bmatrix} 1 & \frac{1}{\sqrt{3}} \\ -1 & \frac{1}{\sqrt{3}} \end{bmatrix}, H3 = \begin{bmatrix} 0 & \frac{2}{\sqrt{3}} \\ -1 & -\frac{1}{\sqrt{3}} \end{bmatrix}$$

2. Using simple mathematical procedure with sign checking as illustrated in Figure 3.9 the sector is identified.

3. Within the sector a new origin is set in the non-orthogonal axes XY which lead to new Xi and Yi components.

4. Repeating the same procedure (2), the triangle where the vector is situated is identified.

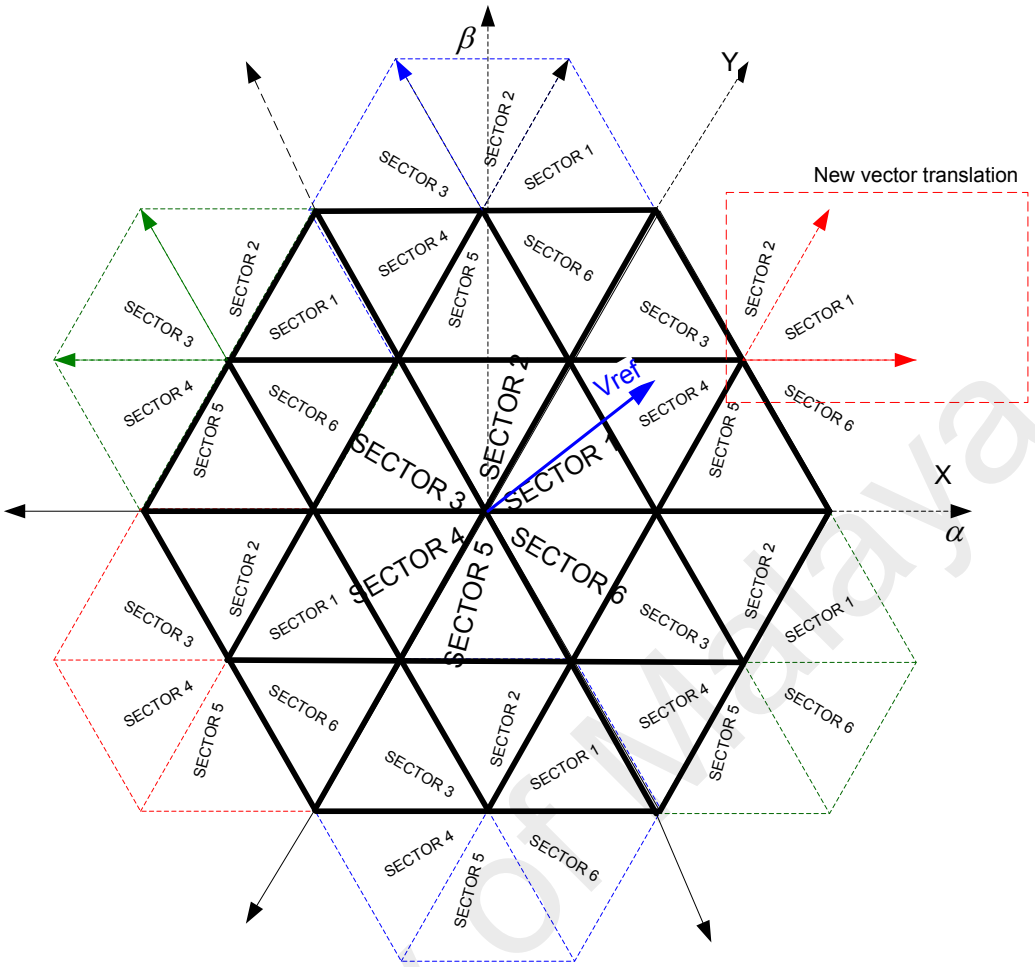


Figure 3-8: Principle of multilevel Space vector modulation

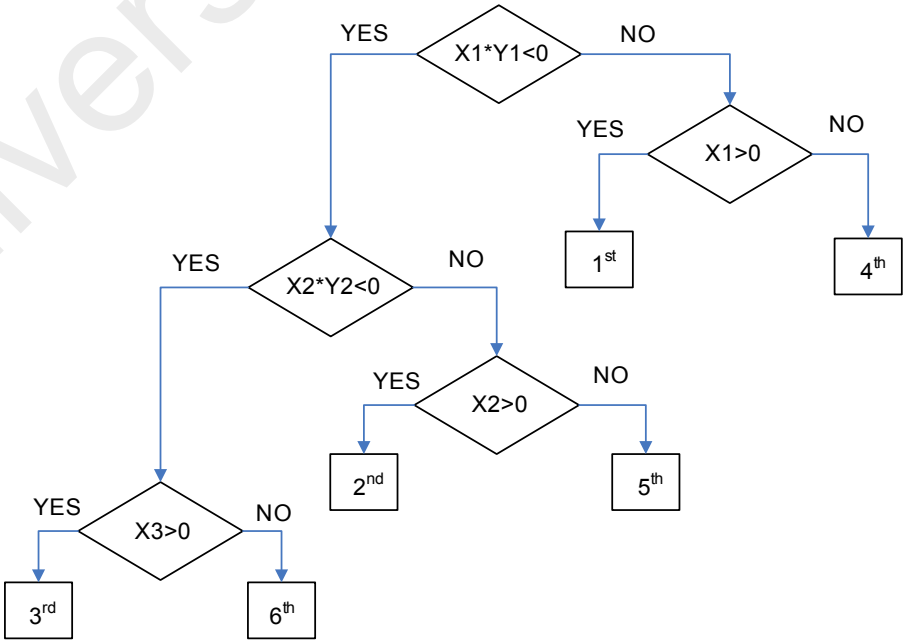


Figure 3-8: Sector and Triangle identification

For the second part of the algorithm, which is the sequence chosen and the duty cycle, it is clear that the duty cycle is the Xi and Yi projection while the sequence is determined by the triangle where the voltage reference is positioned. For example, if V_{ref} is in sector 1, as shown in Figure 3.8, applying the procedure (3) a new coordinate is set for a smaller two-level hexagon, using the sign checking described in Figure 3.9 will determine triangle number 5, 4, and 3. If triangle number 6, 1, and 2 are detected, the inverter is in saturation mode or over modulation, otherwise the inverter will generate two-level if no triangle is identified.

3.3.2 Control of Dual-Output Boost Converter

Generally, the control of conventional boost type converters has a superior technical challenge because of the discontinuity in the output capacitor current. This is caused because of the engagement and disengagement of the LC filter and the load on every switching cycle. A significant improvement was attained under boundary control technique using second-order switching surface. Boundary control technique is among the geometrical techniques applied in the control of DC/DC converters (He et al., 2017). It addresses the complete operation of the converter without differentiating between startup, transient, and steady-state modes. Boundary control technique uses the state plane to depict the ON and OFF trajectories then a switching surface is defined to impose the switching action. Using this technique, the converter can revert to the steady state in two switching actions under large signal disturbances (Song & Chung, 2008). In the next section, a detailed study of the dual-output boost converter control technique based on second-order switching surface is presented.

3.4 Boundary Control of the DOBC

Boundary control utilizing second-order switching surface is a close-loop modulation technique that requires measuring the state variables of the system. It has a basic concept which use and expect the natural movement of the system state trajectories to formulate a second-order switching surface. Such switching surface is a curved surface which is usually close to the system trajectory and near the target operating point. The formulation of the switching boundary and evaluation of the system performance are deduced from the trajectories evolution. The state equation is utilized to generate a family of system trajectories (Onwuchekwa & Kwasinski, 2011).Generally, the direct approach to formulate the system trajectories is to get the solution in time-domain of these state space equations with different initial conditions. Consequently, to obtain the DOBC system trajectories in state-plane (i_L, V_0), the DOBC operation modes defined in equations (3.1) to (3.4) have to be solved with different initial conditions. However, in Song and Chung research work it is specified that it is difficult in case of boost converter to formulate a simple mathematical function for the optimal switching surface as in buck converter due to the spiral shape of the OFF state (Song & Chung, 2008). To overcome that, a solution was proposed that use the state-plane rather than energy plane. As consequence, it is preferable to use the state-energy plane (i_L, W) of the DOBC rather than the state-plane (i_L, V_0) and formulate the system equations. To do that, the instantaneous energy W is defined as:

$$W = \frac{1}{2}Li_L^2 + \frac{1}{2}C_1v_1^2 + \frac{1}{2}C_2v_2^2 \tag{3.5}$$

Using Mallab software, the geometrical representation of the switching trajectory in the state-plane, $\{(i_L, V_1), (i_L, V_2), (i_L, V_0)\}$, and the state-energy plane (i_L, W) are obtained with the initial condition set to zero for each variable. The converter is simulated with the parameters given in Table 3.2. From Figure 3.10, it can be observed that the ON and OFF

trajectories in state-energy plane are not parallel, which will result in a slower response to the reference point. Particularly, the OFF state is slower than the ON state which yield a slower time to reach the intersection point with the detection curve σ^i .Therefore, to improve the response of the system, a possible solution is to multiply the OFF state coefficient with a desired positive value.

Table 3-2: DOBC Parameters Values

Components	Values
Load	R1=R2=250Ω
Capacitor	C1=C2=200 uF
Inductance	L=3 mH
Reference Voltage for each C	V1=V2=150 V
Input voltage	V_{dc}=100 in region I V_{dc}=180 V in region II

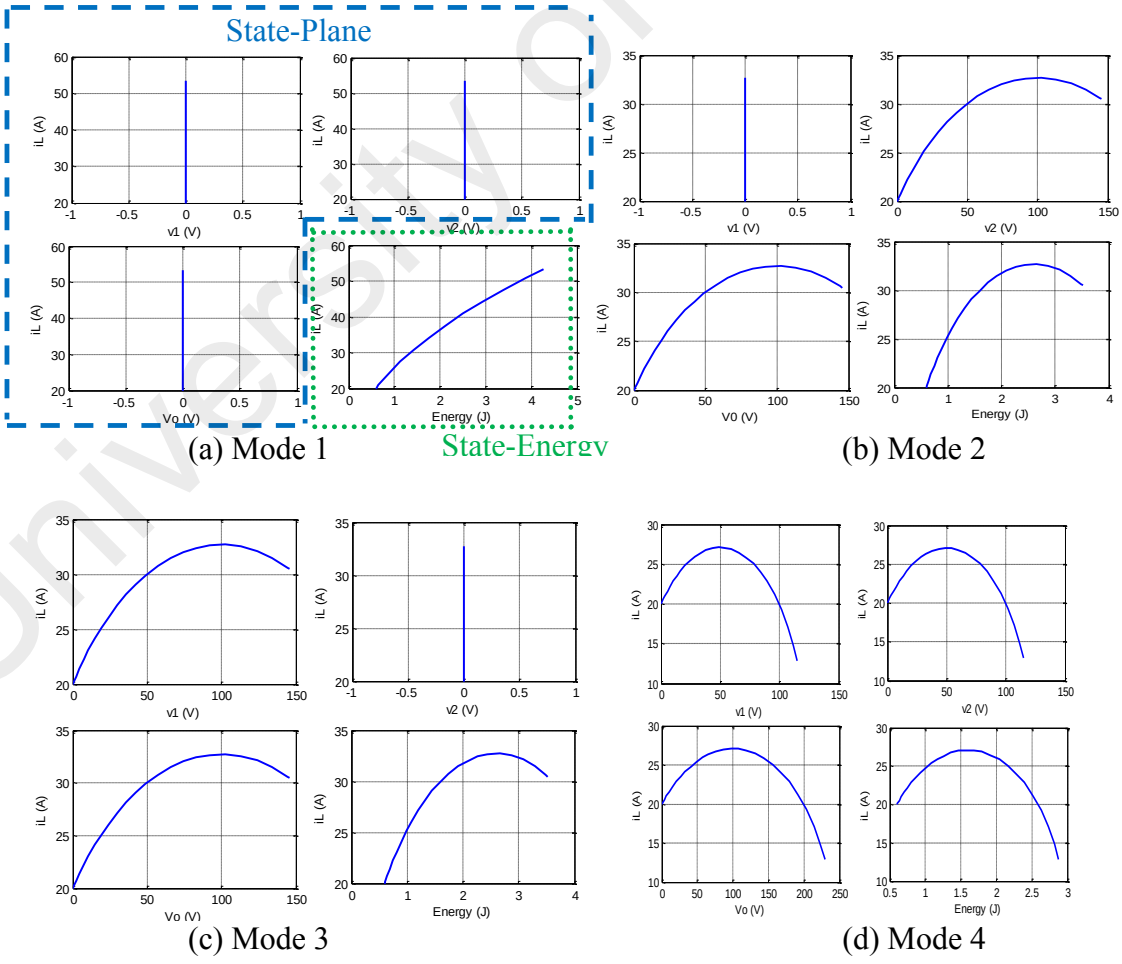


Figure 3-9: Switching trajectory under state-plane and state-energy plane

3.4.1 Formulation of Switching Surfaces in State-Energy Plane

As shown in Figure 3.6, the control algorithm based on state-energy plane tries to express the energy error ΔW, defined by $\Delta W = W - W_{ref}$, as a quadratic function of the current error by imposing the use of certain surface forms deduced from the four operation modes. Choosing $C1 = C2, R1 = R2$, and C_{eq} is the total equivalent capacitance, the instantaneous and reference energies obtained can be formulated based on the total output voltage V_0 as follows:

$$W = \frac{1}{2} L i_L^2 + \frac{1}{2} C_{eq} V_0^2 \tag{3.6}$$

$$W_{ref} = \frac{1}{2} L i_{L\_ref}^2 + \frac{1}{2} C_{eq} V_0^2 \tag{3.7}$$

$$i_{L\_ref} = \frac{P_{out}}{V_{dc}} \tag{3.8}$$

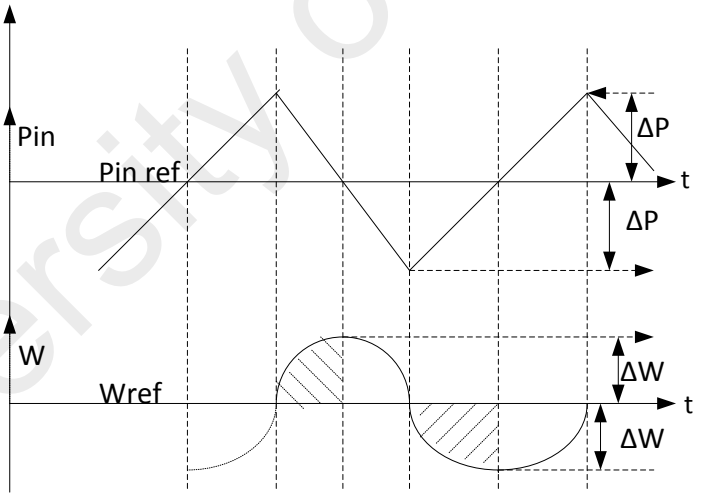


Figure 3-10: Energy profile of the converter

Derivation both of (3.6) and (3.7), then replacing both of $\frac{di_L}{dt}$ and $\frac{dV_0}{dt}$ by their respective equivalent value from each operation mode will lead to the following energy error ΔW:

$$\Delta W = W - W_{ref} = \int_{t1}^{t2} (dW - dW_{ref})dt = \int_{t1}^{t2} (P_{in} - P_{ref})dt \tag{3.9}$$

Applying the trapezoidal method to solve the integral yield

$$\Delta W = \int_{t1}^{t2} P_{in}dt + \int_{t1}^{t2} P_{ref}dt = (t2 - t1)\frac{P_{in}(t2) + P_{in}(t1)}{2} - P_{ref} \times (t2 - t1) \tag{3.10}$$

Given that

$$(t2 - t1) = \frac{P_{in}(t2) - P_{in}(t1)}{dP_{in}} \tag{3.11}$$

Therefore

$$\Delta W = \frac{1}{2}\frac{1}{dP_{in}}\left\{(P_{in}(t2) - P_{ref})^2 - (P_{in}(t1) - P_{ref})^2\right\} \tag{3.12}$$

dP_{in} is obtained for each operation mode from the equation that describes the inductance current variation. In Mode 1,

$$L\frac{di_L}{dt} = V_{dc} \Rightarrow V_{dc}L\frac{di_L}{dt} = V_{dc}^2 \Rightarrow dP_{in} = \frac{V_{dc}^2}{L} \tag{3.13}$$

From (3.12), the ON and OFF trajectories can be derived. Hence the criteria for switching (Q1, Q2) ON and OFF are established. The ideal switching surface have to go through the operating point (i_{L_ref}, W_{ref}), and along the ON-state trajectory when the state is over the load line; along the OFF state trajectory when the state is under the load line as exposed in Figure 3.10.

3.4.2 Derivation of Second-order Switching Surface

Assuming that $v_1 = v_2$, the DOBC operates in two regions which depends whether the input voltage is lower or higher than half of the output voltage V_0. If the converter operates in region I, $(V_{dc} < \frac{V_0}{2})$, Mode 1 with Mode 2 or Mode 3 are used, otherwise Mode 4 with Mode 2 or Mode 3 are used when the converter operates in region II $(V_{dc} > \frac{V_0}{2})$. Simplifying the equation (3.12) for each mode yields the following second-order switching surface:

- **Region I:** Combination of Mode 1 with Mode 2 or 3 will be similar as a normal boost converter. The DC-bus balancing is achieved by comparing the voltage of each capacitor then enabling the discharge through the lower or upper boost converter to compensate the voltage difference between the two capacitors. S_1 is the derived switching surface and is defined as

$$S_1(t) = \begin{cases} 0 \;\; if \;\; \sigma_+^2(t) = \Delta W(t) - k_2\left[i_L(t) - i_{L\_ref}(t)\right]^2 > 0 \;\; \& \;\; i_L(t) > i_{L\_ref}(t) \\ 1 \;\; if \;\; \sigma_-^2(t) = \Delta W(t) - k_1\left[i_L(t) - i_{L\_ref}(t)\right]^2 < 0 \;\; \& \;\; i_L(t) < i_{L\_ref}(t) \end{cases} \quad (3.14)$$

where: $k_1 = \frac{L}{2}$ and: $k_2 = \frac{LV_s}{V_{dc} - v_1}$

- **Region II:** Grouping of Mode 4 with Mode 2 or 3 will allow the voltage input to be higher than one capacitor voltage, the voltage balancing is achieved in the same manner by enabling Mode 2 or 3. The derived switching surface S_2 is defined as:

$$S_2(t) = \begin{cases} 0 \; if \;\; \sigma_+^2(t) = \Delta W(t) + k_3\left[i_L(t) - i_{L\_ref}(t)\right]^2 > 0 \;\; \& \;\; i_L(t) > i_{L\_ref}(t) \\ 1 \; if \;\; \sigma_-^2(t) = \Delta W(t) + k_2\left[i_L(t) - i_{L\_ref}(t)\right]^2 < 0 \;\; \& \;\; i_L(t) < i_{L\_ref}(t) \end{cases} \quad (3.15)$$

where: $k_2 = \frac{LV_{dc}}{V_{dc} - v_1}$ and $k_3 = \frac{LV_{dc}}{V_{dc} - (v_1 + v_2)}$

In the case where the converter works as normal boost converter, Mode 1 and 4 are grouped and the switching surface S_3 is described by:

$$S_3(t) = \begin{cases} 0 \; if \;\; \sigma_+^2(t) = \Delta W(t) - k_3\left[i_L(t) - i_{L\_ref}(t)\right]^2 > 0 \;\; \& \;\; i_L(t) > i_{L\_ref}(t) \\ 1 \; if \;\; \sigma_-^2(t) = \Delta W(t) - k_1\left[i_L(t) - i_{L\_ref}(t)\right]^2 < 0 \;\; \& \;\; i_L(t) < i_{L\_ref}(t) \end{cases} \tag{3.16}$$

where: $k_1 = \dfrac{L}{2}$ and $k_3 = \dfrac{LV_{dc}}{V_{dc} - (v_1 + v_2)}$

3.4.3 Control Algorithm Implementation

It is possible to simplify the analysis of the control algorithm which aims to regulate the output voltage by distinguishing the total area, described in S_1 and S_2, where the converter is functioning. Therefore, if the DOBC operates in region 1 and according to previous analysis the control algorithm follows these steps:

1) Enable Mode 1 to obtain a sufficient current to generate the desired boost voltage.
2) Verify the DC-bus balance
3) Enable Mode 2 or Mode 3 to achieve a DC-bus balancing
4) Enable Mode 1 to follow the i_L reference current
5) Repeat steps 2 until 4 until the desired output is obtained

On the other hand, if the DOBC operates in region II, the steps are as follows:

1) Enable stage 2 to increase the inductance current.
2) Compare between the voltage of one capacitor and its reference voltage
3) Verify the DC-bus balance
4) Enable stage 4 for voltage discharge and capacitors charging.
5) Verify the DC-bus voltage

6) If there is no balance, enable stage 3 or stage 2 to increase the capacitor voltage to the reference voltage.
7) Repeat sequences 4 until 6 to reach the desired output and achieve a balanced DC-bus voltage

At the end, the pulse patterns of the two switches are generated through an RS flip-flop function and a decoder as detailed in Table 3.3. Figure 3.11 illustrates the flowchart of the DOBC control. As it can be seen, the control algorithm starts with setting the converter parameters such as the inductance value, the capacitor values, and the desired voltage output references. After that, it collects the measurement of voltages and currents needed, proceeds with the calculation of needed energies and inductance current reference, then determines the region of control based on the sensed input voltage and the output reference voltage of each capacitor. When the control region is determined, the control algorithm will compare between the voltage of each capacitor to determine which mode will be activated either (mode 1, mode 2) or (mode 1, mode 3) in region I or either (mode 3, mode 4) or (mode 2, mode 4) in region II. Finally, the switching criteria stated in S1 or S2 are evaluated to generate the desired pulses.

Table 3-3: Switching actions of the DOBC

	Vdc>V0/2	Flip flop	V1>V2	Q1	Q2
Region I	1	1	1	1	1
			0	1	1
		0	1	1	0
			0	0	1
Region II	0	0	1	0	0
			0	0	0
		1	1	1	0
			0	0	1

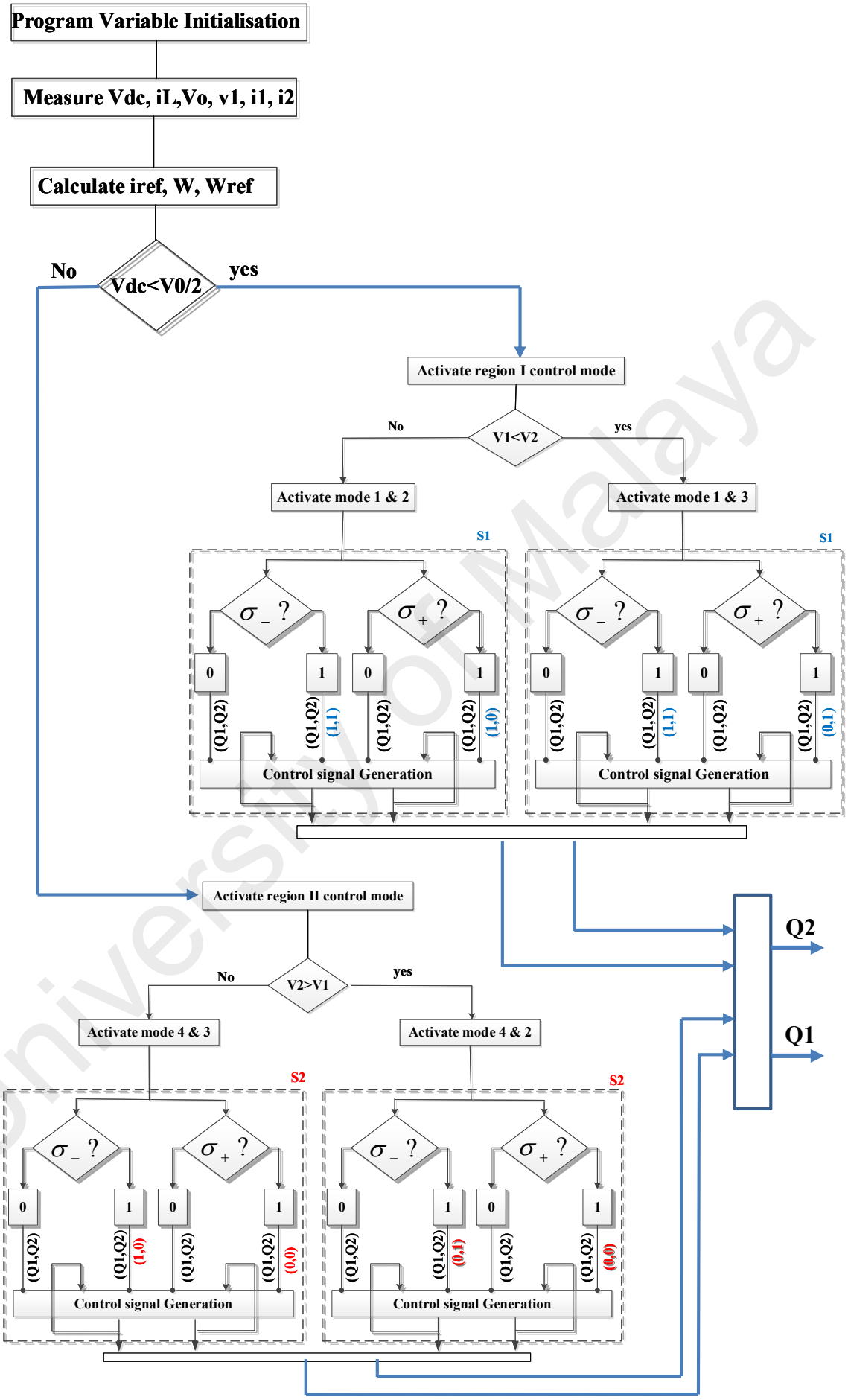


Figure 3-11: Flowchart of the DOBC control algorithm

3.5 Steady State Characteristics

The control scheme in the boundary control theory does not differentiate between steady state and transient operation. However, the steady state operation requires a detailed analysis to establish the relation between ripples and the selected switching surface boundaries. Assuming two points (x_1, x_2) on the ON and OFF trajectories with the desired coordinate (i_{Lmax} ,W_1) and (i_{Lmin} ,W_2), it can be shown from Figure 3.10 and based on each control region that:

- **In region I**: At the steady state, the ripple current $(i_{L\max} - i_{L\_ref})$ and $(i_{L\min} - i_{L\_ref})$ have the same value. Points *(x_1, x_2)* are both on the ON and OFF state trajectories, hence $W_1 = W_2$. Based on (3.10), the ON and OFF trajectories are defined as follows:

$$\begin{cases} W_1 - W_{ref} - k_2(i_{L\max} - i_{L\_ref})^2 - \Delta w = 0 \\ W_2 - W_{ref} - k_1(i_{L\min} - i_{L\_ref})^2 + \Delta w = 0 \end{cases} \tag{3.17}$$

Therefore, it is easy to demonstrate that the ripple current is equal to:

$$\Delta i_{\min} = \Delta i_{\max} = \sqrt{\frac{2}{k_1 - k_2}\Delta w} \tag{3.18}$$

In the same manner, it is clear that the energy at both points is equal to:

$$W_1 = W_2 = W_{ref} + \frac{k_1 + k_2}{k_1 - k_2}\Delta w \tag{3.19}$$

Using (3.5) and (3.17) the ripple voltage can be demonstrated to be

$$\begin{aligned} v_{0\min} &= \sqrt{\frac{4}{C}W_{ref} + \frac{4}{C}\frac{k_1 + k_2}{k_1 - k_2}\Delta w - \frac{2L}{C}(i_{L\_ref} + \Delta i_{\max})^2} \\ v_{0\max} &= \sqrt{\frac{4}{C}W_{ref} + \frac{4}{C}\frac{k_1 + k_2}{k_1 - k_2}\Delta w - \frac{2L}{C}L(i_{L\_ref} - \Delta i_{\min})^2} \end{aligned} \tag{3.20}$$

The switching frequency is the reciprocal of the time that the converter needs to perform one switching action in steady state. Hence the switching frequency is equal to:

$$f_s = \frac{1}{T_{on} + T_{off}} = \frac{V_{dc}(V_0 - 2V_{dc})}{2LV_0\sqrt{\frac{2}{k_1 - k_2}\Delta w}} \tag{3.21}$$

- **In region II**: Following the same procedure in region I, the ON and OFF trajectories at points *(x_1, x_2)* is defined as:

$$\begin{cases} W_1 - W_{ref} + k_3(i_{L\max} - i_{L\_ref})^2 - \Delta w = 0 \\ W_2 - W_{ref} + k_2(i_{L\min} - i_{L\_ref})^2 + \Delta w = 0 \end{cases} \tag{3.22}$$

Thus, the current ripple can be expressed as

$$\Delta i_{\min} = \Delta i_{\max} = \sqrt{\frac{2}{k_2 - k_3}\Delta w} \tag{3.23}$$

which produces an energy equal to:

$$W_1 = W_2 = W_{ref} - \frac{k_2 + k_3}{k_2 - k_3}\Delta w \tag{3.24}$$

Using (3.5) and (3.22), the voltage ripple can be easily determined by:

$$\begin{aligned} v_{0\min} &= \sqrt{\frac{4}{C}W_{ref} - \frac{4}{C}\frac{k_2 + k_3}{k_2 - k_3}\Delta w - \frac{2L}{C}(i_{L\_ref} + \Delta i_{\max})^2} \\ v_{0\max} &= \sqrt{\frac{4}{C}W_{ref} - \frac{4}{C}\frac{k_2 + k_3}{k_2 - k_3}\Delta w - \frac{2L}{C}(i_{L\_ref} - \Delta i_{\min})^2} \end{aligned} \tag{3.25}$$

The ON and OFF time is determined by the inductor ripple current; thus, the switching frequency is equal to:

$$f_s = \frac{1}{T_{on} + T_{off}} = \frac{(2V_{dc} - V_0)(V_0 - V_{dc})}{2LV_0\sqrt{\frac{2}{k_2 - k_3}\Delta w}} \tag{3.26}$$

3.6 Large Signal Stability Analysis

Based on the trajectory behavior at the boundary, the point along the switching surface σ^2 is classified into three categories: refractive point, reflective point and rejective point. These three possibilities govern the stability of a system. The type of point can be determined by analyzing σ^2 and $\dot{\sigma}^2$.

The dynamic performance of the system will differently exhibit in the respective modes. In the rejective mode, the trajectories on both sides of the switching surface move away from the switching surface. The converter will be in unstable operation. In the reflective mode, the converter will be in the sliding mode, hence the trajectory will move along the surface to the operating point through several switching actions. In the refractive region, the state will move around the operating point. Therefore, by differentiating the switching surfaces *(S_1, S_2)* and evaluating the ON and OFF trajectories in term of ($\sigma_i^2, \dot{\sigma}_i^2$) polarities, the coefficients (*k_1, k_2, k_3)* will govern the system's stability.

The derivation of σ_1^2 for the ON and OFF trajectories in region I can be obtained as follows:

$$S_1(t)=\begin{cases}\sigma_1^2=\begin{cases}\sigma_+^2(t)=\Delta W(t)-k_2\left[i_L(t)-i_{L\_ref}(t)\right]^2>0 \;\;\&\;\; i_L(t)>i_{L\_ref}(t)\\ \sigma_-^2(t)=\Delta W(t)-k_1\left[i_L(t)-i_{L\_ref}(t)\right]^2<0 \;\;\&\;\; i_L(t)<i_{L\_ref}(t)\end{cases}\\ \dot{\sigma}_1^2=\begin{cases}\dot{\sigma}_+^2(t)=V_{dc}(i_L-i_{L\_ref})(1-\dfrac{2k_2}{L})>0 \;\;\&\;\; i_L(t)>i_{L\_ref}(t)\\ \dot{\sigma}_-^2(t)=V_{dc}(i_L-i_{L\_ref})(1-\dfrac{2k_1}{L})<0 \;\;\&\;\; i_L(t)<i_{L\_ref}(t)\end{cases}\\ \dot{\sigma}_1^2=\begin{cases}\sigma_+^2(t)=(i_L-i_{L\_ref})(V_{dc}-\dfrac{2k_2(V_{dc}-v_1)}{L})>0 \;\;\&\;\; i_L(t)>i_{L\_ref}(t)\\ \sigma_-^2(t)=(i_L-i_{L\_ref})(V_{dc}-\dfrac{2k_1(V_{dc}-v_1)}{L})<0 \;\;\&\;\; i_L(t)<i_{L\_ref}(t)\end{cases}\end{cases} \tag{3.27}$$

In region II the derivation of σ_2^2 for the ON and OFF trajectories is as follows:

$$S_2(t)=\begin{cases}\sigma_2^2=\left\{\begin{matrix}\sigma_+^2(t)=\Delta W(t)-k_3\left[i_L(t)-i_{L\_ref}(t)\right]^2>0 \;\;\&\;\; i_L(t)>i_{L\_ref}(t)\\ \sigma_-^2(t)=\Delta W(t)+k_2\left[i_L(t)-i_{L\_ref}(t)\right]^2<0 \;\;\&\;\; i_L(t)<i_{L\_ref}(t)\end{matrix}\right\}\\ \dot{\sigma}_2^2=\left\{\begin{matrix}\sigma_+^2(t)=(i_L-i_{L\_ref})(V_{dc}-\dfrac{2k_3(V_{dc}-v_1-v_2)}{L})>0 \;\;\&\;\; i_L(t)>i_{L\_ref}(t)\\ \sigma_-^2(t)=(i_L-i_{L\_ref})(V_{dc}+\dfrac{2k_2(V_{dc}-v_1-v_2)}{L})<0 \;\;\&\;\; i_L(t)<i_{L\_ref}(t)\end{matrix}\right\}\\ \dot{\sigma}_2^2=\left\{\begin{matrix}\sigma_+^2(t)=(i_L-i_{L\_ref})(V_{dc}-\dfrac{2k_3(V_{dc}-v_1)}{L})>0 \;\;\&\;\; i_L(t)>i_{L\_ref}(t)\\ \sigma_-^2(t)=(i_L-i_{L\_ref})(V_{dc}+\dfrac{2k_2(V_{dc}-v_1)}{L})<0 \;\;\&\;\; i_L(t)<i_{L\_ref}(t)\end{matrix}\right\}\end{cases} \tag{3.28}$$

Assuming that the converter is in region I, the condition for reflective mode is attained when the product of σ_i^2 and $\dot{\sigma}_i^2$ is negative. Therefore, for the S_1 ON-state the condition is:

$$\begin{cases}k_1>\dfrac{L}{2} \;\; when \;\; i_L(t)<i_{L\_ref}(t)\\ k_2<0 \;\; when \;\; i_L(t)>i_{L\_ref}(t)\end{cases} \tag{3.29}$$

Similarly, for S_1 OFF-state the condition is

$$\begin{cases}k_1>0 & when \;\; i_L(t)<i_{L\_ref}(t)\\ k_2<\dfrac{LV_{dc}}{2(V_{dc}-v_1)} & when \;\; i_L(t)>i_{L\_ref}(t)\end{cases} \tag{3.30}$$

By combining the two conditions stated in (3.29) and (3.30), the required values of k1 and *k2* that ensure the converter in the reflective mode are:

$$\begin{cases}k_1>\dfrac{L}{2}\\ k_2<\dfrac{LV_{dc}}{2(V_{dc}-v_1)}\end{cases} \tag{3.31}$$

In the same way the conditions of the three coefficients (k1, k2, k3) that ensure the operation in the refractive, reflective and rejective mode are as follows:

- The condition for reflective mode is satisfied when

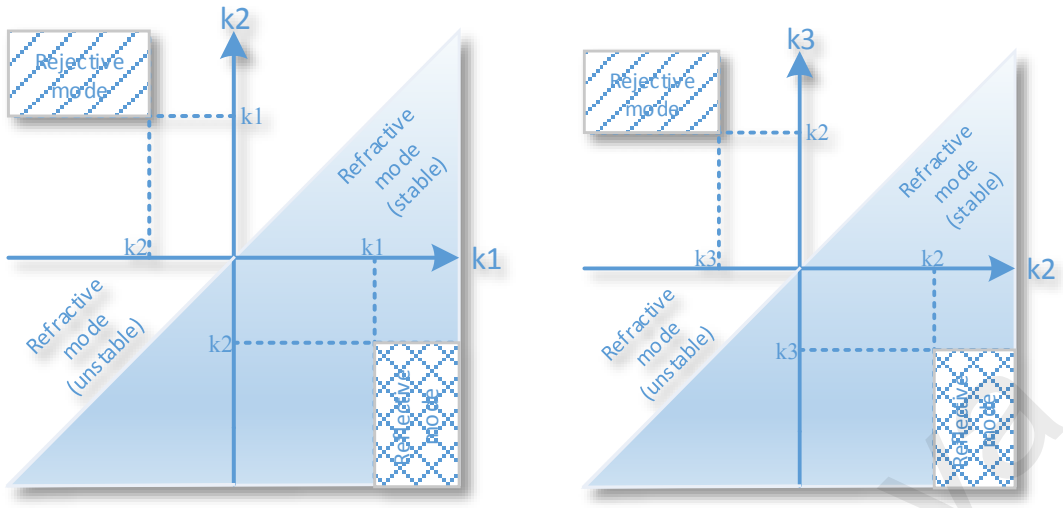
$$\begin{cases} k_1 > \dfrac{L}{2} \;\; \& \;\; k_2 < \dfrac{LV_{dc}}{2(V_{dc} - V_0/2)} & in\ region\ I \\ k_2 > \dfrac{LV_{dc}}{2(V_{dc} - V_0/2)} \;\; \& \;\; k_3 < \dfrac{LV_{dc}}{2(V_{dc} - V_0)} & in\ region\ II \end{cases} \tag{3.32}$$

- The condition for rejective mode is satisfied when

$$\begin{cases} k_1 < -\dfrac{L}{2} \;\; \& \;\; k_2 > \dfrac{LV_{dc}}{2(V_0/2 - V_{dc})} & in\ region\ I \\ k_2 < \dfrac{LV_{dc}}{2(V_0/2 - V_{dc})} \;\; \& \;\; k_3 > \dfrac{LV_{dc}}{2(V_0 - V_{dc})} & in\ region\ II \end{cases} \tag{3.33}$$

- The conditions for refractive mode are within the one outside the condition of reflective and rejective mode. Moreover, another condition should be satisfied which is the distance S_n between the target operating point and the switching state. The distance has to decrease for two successive points on the same side of the target. By selecting a random point (i_{Ln}, W_n) in the switching surface σ^2 and using the procedure detailed in (Song & Chung, 2008), it is easy to demonstrate that $S_{n+2} < S_n$ holds true. Hence, the convergence of the system is inherently ensured by the control principle.

The converter will exhibit fast dynamic response, when the switching surface is chosen to be along the boundary of the reflective and refractive regions. Figure 3.12 shows the stability analysis in each control region of the DOBC.



(a) Control region I (b) Control region II

Figure 3-12: Stability variation based in control region

3.7 Summary

This chapter has provided the theoretical concept of the proposed three-level converter. Beside the description of the operation principle of the proposed configuration, a control method based on space vector modulation is applied to the three-level inverter and a second-order switching surface is applied to the dual-output boost converter. Furthermore, a detailed design of the DC/DC converter is presented. It started with the formulation of switching state, then derivation of the second-order switching surface based on the state-energy plane. As mentioned earlier, the converter can be controlled in two regions, hence the proposed control algorithm is adapted to identify the control region, then used the appropriate switching surface criteria stated in S1 and S2 to generate the desired pulses. The generalized control algorithm, described in the flowchart of Figure 3.11, can be implemented in digital signal processor to overcome the complexity of the analogue implementation. In addition to a steady state analysis a detailed investigation on the converter stability behaviour is performed.

CHAPTER 4: SENSORLESS BOUNDARY CONTROL METHOD

4.1 Introduction

It is desirable that controls for power converters be robust to noise, have good dynamic performance, and be simple to design. Boundary control using second-order switching surface, as described in the previous chapter, needs to sense three signals; inductance current, load current, and output voltage in addition to input voltage if the boost converter is fed through a variable DC source. Since the number of sensors used is high, it is preferable to adopt some sensorless voltage or current techniques. Many research activities are carried out to propose the diminution of input signals (Chen, Lu, Li, & Chen, 2017; Q. Tong, Chen, C., Zhang, Q., & Zou, X., 2015; Q. Tong et al., 2014). As the reduction of the sensor number is of utmost concern to industrial users', due to its significant cost advantage as well as a reliability issue, an interesting approach is to apply sensorless current mode technique where the inductor current is estimated from the sensed input and output voltages.

In its simplest form, the sensorless current control method predicts the inductor current directly by integrating the inductor voltage. As the inductor voltage in a DC/DC converter is usually a much larger signal than the output of a current sensor, and its range does not change much as a function of loading. The integral of the inductor voltage contains all the dynamic information of the current signal (Zheng, Ho, Leung, Guo, & Chen, 2015). Combining a sensorless current method with boundary control technique will develop a control that has the advantages of boundary control without using the current sensors. Additionally, the proposed control will have a very good potential for both academic and practical applications.

In the subsequent sections, the modeling of the DOBC is described and used to set the current estimation equations in the ON and OFF state. Following by incorporating the boundary control technique with it.

4.2 Mathematical Modelling of the DOBC

Figure 4.1 describes the circuit topology of the DOBC, where we assumed that $C_1 = C_2 = C$ and $R_1 = R_2 = R$. These conditions are also used in both simulation and hardware analysis through this research work. To have an adequate control of the dual-output boost converter, it is useful first to develop a mathematical model that describes its output variables in terms of its input variables and system's initial conditions. This development can be done by determining the state space equations that describe the system operation, then solving them. As the state space equations of the proposed DOBC are simple to define, it remains only the search of their solutions.

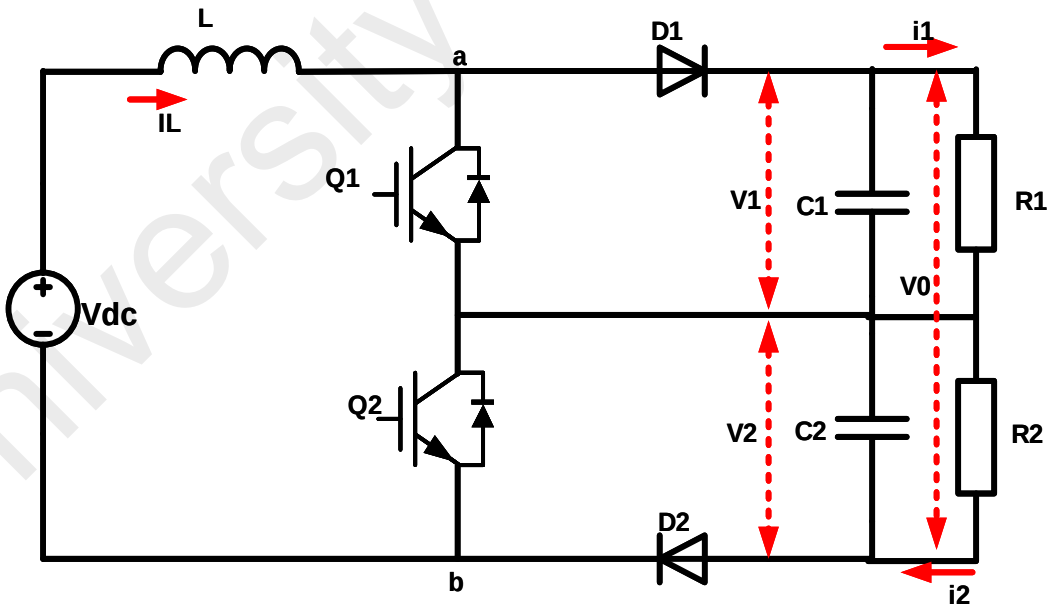


Figure 4-1: The adopted boost topology

As we know, the general solution of the following form of the state space equation

$$x' = A \cdot x + B \cdot u \tag{4.1}$$

is written in the form of:

$$x(t) = x^L(t) + x^F(t)$$

$$x^L(t) = \exp(A(t - t_0))x(t_0) \tag{4.2}$$

$$x^F(t) = \int_{t_0}^{t} \exp(A(t-\tau))Bu(\tau)d\tau$$

where A and B are constant and $x(t_0)$ is the initial condition value. The general solution is the sum of two components: The first component $x^L(t)$, called natural response due to a simple operation of multiplication, while the second component $x^F(t)$, called forced response, results from complex operation of convolution. To solve equation (4.1) using equation (4.2), it is necessary to go through the fundamental matrix's calculation given by $M = \exp(At)$. Therefore, the use of Laplace transformation (LT) and its inverse simplify the calculation of this matrix and assist us in natural and forced response evaluations'. The following steps have been proposed as follows:

- Development of state space equations
- Determination of the fundamental matrix
- Identifying the natural and forced responses of the system.

4.2.1 Formulation of State Space Equations

The DOBC can operate in four modes as demonstrated in chapter 3. The mathematical model related to each operating mode is given by the following matrices relations where $i_L, V_{1,}, V_2$, and V_{dc} are current inductor, capacitors C1 and C2 voltages, and the input voltage respectively.

$$\text{Mode 1: } \begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix}' = \begin{bmatrix} 0 & 0 & 0 \\ 0 & -\frac{1}{R_1 C_1} & 0 \\ 0 & 0 & -\frac{1}{R_2 C_2} \end{bmatrix} \begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix} V_{dc} \tag{4.3}$$

$$\text{Mode 2: } \begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix}' = \begin{bmatrix} 0 & 0 & -\frac{1}{L} \\ 0 & -\frac{1}{R_1 C_1} & 0 \\ \frac{1}{C_2} & 0 & -\frac{1}{R_2 C_2} \end{bmatrix} \begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix} V_{dc} \tag{4.4}$$

$$\text{Mode 3: } \begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix}' = \begin{bmatrix} 0 & -\frac{1}{L} & 0 \\ \frac{1}{C_1} & -\frac{1}{R_1 C_1} & 0 \\ 0 & 0 & -\frac{1}{R_2 C_2} \end{bmatrix} \begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix} V_{dc} \tag{4.5}$$

$$\text{Mode 4: } \begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix}' = \begin{bmatrix} 0 & -\frac{1}{L} & -\frac{1}{L} \\ \frac{1}{C_1} & -\frac{1}{R_1 C_1} & 0 \\ \frac{1}{C_2} & 0 & -\frac{1}{R_2 C_2} \end{bmatrix} \begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix} V_{dc} \tag{4.6}$$

With the simplifications adopted ($C_1 = C_2 = C$ and $R_1 = R_2 = R$) the equations simply become

$$\text{Mode 1: } \begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix}' = \begin{bmatrix} 0 & 0 & 0 \\ 0 & -\frac{1}{RC} & 0 \\ 0 & 0 & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix} V_{dc} \tag{4.7}$$

Mode 2: $$\begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix}' = \begin{bmatrix} 0 & 0 & -\frac{1}{L} \\ 0 & -\frac{1}{RC} & 0 \\ \frac{1}{C} & 0 & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix} V_{dc} \quad (4.8)$$

Mode 3: $$\begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix}' = \begin{bmatrix} 0 & -\frac{1}{L} & 0 \\ \frac{1}{C} & -\frac{1}{RC} & 0 \\ 0 & 0 & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix} V_{dc} \quad (4.9)$$

Mode 4: $$\begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix}' = \begin{bmatrix} 0 & -\frac{1}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} & 0 \\ \frac{1}{C} & 0 & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix} V_{dc} \quad (4.10)$$

The application of Laplace transformation (LT) to equations (4.7) till (4.10) gives:

Mode 1:

$$\begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} p & 0 & 0 \\ 0 & p+\frac{1}{RC} & 0 \\ 0 & 0 & p+\frac{1}{RC} \end{bmatrix}^{-1} \begin{bmatrix} i_L(0) \\ v_1(0) \\ v_2(0) \end{bmatrix} + \begin{bmatrix} p & 0 & 0 \\ 0 & p+\frac{1}{RC} & 0 \\ 0 & 0 & p+\frac{1}{RC} \end{bmatrix}^{-1} \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix} V_{dc} \quad (4.11)$$

Mode 2:

$$\begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} p & 0 & \frac{1}{L} \\ 0 & p+\frac{1}{RC} & 0 \\ -\frac{1}{C} & 0 & p+\frac{1}{RC} \end{bmatrix}^{-1} \begin{bmatrix} i_L(0) \\ v_1(0) \\ v_2(0) \end{bmatrix} + \begin{bmatrix} p & 0 & \frac{1}{L} \\ 0 & p+\frac{1}{RC} & 0 \\ -\frac{1}{C} & 0 & p+\frac{1}{RC} \end{bmatrix}^{-1} \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix} V_{dc} \quad (4.12)$$

Mode 3:

$$\begin{bmatrix} \mathrm{i_L} \\ \mathrm{v_1} \\ \mathrm{v_2} \end{bmatrix} = \begin{bmatrix} p & \frac{1}{L} & 0 \\ -\frac{1}{C} & p+\frac{1}{RC} & 0 \\ 0 & 0 & p+\frac{1}{RC} \end{bmatrix}^{-1} \begin{bmatrix} \mathrm{i_L}(0) \\ \mathrm{v_1}(0) \\ \mathrm{v_2}(0) \end{bmatrix} + \begin{bmatrix} p & \frac{1}{L} & 0 \\ -\frac{1}{C} & p+\frac{1}{RC} & 0 \\ 0 & 0 & p+\frac{1}{RC} \end{bmatrix}^{-1} \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix} V_{dc} \quad (4.13)$$

Mode 4:

$$\begin{bmatrix} \mathrm{i_L} \\ \mathrm{v_1} \\ \mathrm{v_2} \end{bmatrix} = \begin{bmatrix} p & \frac{1}{L} & \frac{1}{L} \\ -\frac{1}{C} & p+\frac{1}{RC} & 0 \\ -\frac{1}{C} & 0 & p+\frac{1}{RC} \end{bmatrix}^{-1} \begin{bmatrix} \mathrm{i_L}(0) \\ \mathrm{v_1}(0) \\ \mathrm{v_2}(0) \end{bmatrix} + \begin{bmatrix} p & \frac{1}{L} & \frac{1}{L} \\ -\frac{1}{C} & p+\frac{1}{RC} & 0 \\ -\frac{1}{C} & 0 & p+\frac{1}{RC} \end{bmatrix}^{-1} \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix} V_{dc}$$

(4.14)

Then an inversion of the following matrix is necessary

$$\text{Mode 1: } \mathrm{F} = \begin{bmatrix} p & 0 & 0 \\ 0 & p+\frac{1}{RC} & 0 \\ 0 & 0 & p+\frac{1}{RC} \end{bmatrix} \quad \text{Mode 2: } \mathrm{G} = \begin{bmatrix} p & 0 & \frac{1}{L} \\ 0 & p+\frac{1}{RC} & 0 \\ -\frac{1}{C} & 0 & p+\frac{1}{RC} \end{bmatrix} \quad (4.15)$$

$$\text{Mode 3: } N = \begin{bmatrix} p & \frac{1}{L} & 0 \\ -\frac{1}{C} & p+\frac{1}{RC} & 0 \\ 0 & 0 & p+\frac{1}{RC} \end{bmatrix} \quad \text{Mode 4: H} = \begin{bmatrix} p & \frac{1}{L} & \frac{1}{L} \\ -\frac{1}{C} & p+\frac{1}{RC} & 0 \\ -\frac{1}{C} & 0 & p+\frac{1}{RC} \end{bmatrix} \quad (4.16)$$

The general formula used to inverse 3x3 matrix A is as follows:

$$A = \begin{bmatrix} a & b & c \\ d & e & f \\ g & h & i \end{bmatrix}$$

Its invers is:

$$A^{-1} = \frac{1}{|A|}\begin{bmatrix} ei-fh & ch-bi & bf-ce \\ fg-di & ai-cg & cd-af \\ dh-eg & bg-ah & ae-bd \end{bmatrix} \tag{4.17}$$

where $|A| = aei + dhc + gbf - gec - dbi - afh$

Applying this formula to inverse the matrices F, G, N and H give:

$$F^{-1} = \frac{1}{|F|}\begin{bmatrix} \left(p+\frac{1}{RC}\right)^2 & 0 & 0 \\ 0 & p\left(p+\frac{1}{RC}\right) & 0 \\ 0 & 0 & p\left(p+\frac{1}{RC}\right) \end{bmatrix} \tag{4.18}$$

$$|F| = p\left(p+\frac{1}{RC}\right)^2$$

$$G^{-1} = \frac{1}{|G|}\begin{bmatrix} \left(p+\frac{1}{RC}\right)^2 & 0 & -\frac{1}{L}\left(p+\frac{1}{RC}\right) \\ 0 & p\left(p+\frac{1}{RC}\right)+\frac{1}{LC} & 0 \\ \frac{1}{C}\left(p+\frac{1}{RC}\right) & 0 & p\left(p+\frac{1}{RC}\right) \end{bmatrix} \tag{4.19}$$

$$|G| = p\left(p+\frac{1}{RC}\right)^2 + \frac{1}{LC}\left(p+\frac{1}{RC}\right)$$

$$N^{-1} = \frac{1}{|N|}\begin{bmatrix} \left(p+\frac{1}{RC}\right)^2 & -\frac{1}{L}\left(p+\frac{1}{RC}\right) & 0 \\ \frac{1}{C}\left(p+\frac{1}{RC}\right) & p\left(p+\frac{1}{RC}\right) & 0 \\ 0 & 0 & p\left(p+\frac{1}{RC}\right)+\frac{1}{LC} \end{bmatrix} \tag{4.20}$$

$$|N| = p\left(p+\frac{1}{RC}\right)^2 + \frac{1}{LC}\left(p+\frac{1}{RC}\right)$$

$$H^{-1} = \frac{1}{|H|}\begin{bmatrix} \left(p+\frac{1}{RC}\right)^2 & -\frac{1}{L}\left(p+\frac{1}{RC}\right) & -\frac{1}{L}\left(p+\frac{1}{RC}\right) \\ \frac{1}{C}\left(p+\frac{1}{RC}\right) & p\left(p+\frac{1}{RC}\right)+\frac{1}{LC} & -\frac{1}{LC} \\ \frac{1}{C}\left(p+\frac{1}{RC}\right) & -\frac{1}{LC} & p\left(p+\frac{1}{RC}\right)+\frac{1}{LC} \end{bmatrix} \tag{4.21}$$

$$|H| = p\left(p+\frac{1}{RC}\right)^2 + \frac{2}{LC}\left(p+\frac{1}{RC}\right)$$

4.2.2 Determination of the Fundamental Matrix

Using Laplace transformation inverse, the fundamental matrix of each mode can be obtained as follows:

Mode 1: $$TL(M1) = F^{-1} = \begin{bmatrix} \frac{1}{p} & 0 & 0 \\ 0 & \frac{1}{p+\frac{1}{RC}} & 0 \\ 0 & 0 & \frac{1}{p+\frac{1}{RC}} \end{bmatrix} \tag{4.22}$$

Mode 2: $$TL(M2) = G^{-1} = \begin{bmatrix} \frac{p+\frac{1}{RC}}{p^2+\frac{1}{RC}p+\frac{1}{LC}} & 0 & \frac{-\frac{1}{L}}{p^2+\frac{1}{RC}p+\frac{1}{LC}} \\ 0 & \frac{1}{p+\frac{1}{RC}} & 0 \\ \frac{\frac{1}{C}}{p^2+\frac{1}{RC}p+\frac{1}{LC}} & 0 & \frac{p}{p^2+\frac{1}{RC}p+\frac{1}{LC}} \end{bmatrix} \tag{4.23}$$

Mode 3: $TL(M3) = N^{-1} = \begin{bmatrix} \dfrac{p+\dfrac{1}{RC}}{p^2+\dfrac{1}{RC}p+\dfrac{1}{LC}} & \dfrac{-\dfrac{1}{L}}{p^2+\dfrac{1}{RC}p+\dfrac{1}{LC}} & 0 \\ \dfrac{\dfrac{1}{C}}{p^2+\dfrac{1}{RC}p+\dfrac{1}{LC}} & \dfrac{p}{p^2+\dfrac{1}{RC}p+\dfrac{1}{LC}} & 0 \\ 0 & 0 & \dfrac{1}{p+\dfrac{1}{RC}} \end{bmatrix}$ (4.24)

Mode 4:

$$TL(M4) = H^{-1} = \begin{bmatrix} \dfrac{p+\dfrac{1}{RC}}{p^2+\dfrac{1}{RC}p+\dfrac{2}{LC}} & \dfrac{-\dfrac{1}{L}}{p^2+\dfrac{1}{RC}p+\dfrac{2}{LC}} & \dfrac{-\dfrac{1}{L}}{p^2+\dfrac{1}{RC}p+\dfrac{2}{LC}} \\ \dfrac{\dfrac{1}{C}}{p^2+\dfrac{1}{RC}p+\dfrac{2}{LC}} & \dfrac{p^2+\dfrac{1}{RC}p+\dfrac{1}{LC}}{\left(p+\dfrac{1}{RC}\right)\left(p^2+\dfrac{1}{RC}p+\dfrac{2}{LC}\right)} & \dfrac{-\dfrac{1}{LC}}{\left(p+\dfrac{1}{RC}\right)\left(p^2+\dfrac{1}{RC}p+\dfrac{2}{LC}\right)} \\ \dfrac{\dfrac{1}{C}}{p^2+\dfrac{1}{RC}p+\dfrac{2}{LC}} & \dfrac{-\dfrac{1}{LC}}{\left(p+\dfrac{1}{RC}\right)\left(p^2+\dfrac{1}{RC}p+\dfrac{2}{LC}\right)} & \dfrac{p^2+\dfrac{1}{RC}p+\dfrac{1}{LC}}{\left(p+\dfrac{1}{RC}\right)\left(p^2+\dfrac{1}{RC}p+\dfrac{2}{LC}\right)} \end{bmatrix} \quad (4.25)$$

To calculate each fundamental matrix (M1, M2, M3, and M4), we apply the inverse LT assuming the existence of two conjugated complex poles for an elementary system of higher order than or equal to 2. Indeed, we have:

- Calculation of M1:

$$M1 = e^{At} = \begin{bmatrix} m_{11}(t) & m_{12}(t) & m_{13}(t) \\ m_{21}(t) & m_{22}(t) & m_{23}(t) \\ m_{31}(t) & m_{32}(t) & m_{33}(t) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \exp\left(-\dfrac{1}{RC}t\right) & 0 \\ 0 & 0 & \exp\left(-\dfrac{1}{RC}t\right) \end{bmatrix} \quad (4.26)$$

- Calculation of M2:

$$M2 = e^{At} = \begin{bmatrix} m_{11}(t) & m_{12}(t) & m_{13}(t) \\ m_{21}(t) & m_{22}(t) & m_{23}(t) \\ m_{31}(t) & m_{32}(t) & m_{33}(t) \end{bmatrix} = \begin{bmatrix} m_{11}(t) & 0 & m_{13}(t) \\ 0 & \exp\left(-\frac{1}{RC}t\right) & 0 \\ m_{31}(t) & 0 & m_{33}(t) \end{bmatrix}$$

$$M(p) = \frac{n_0 p + n_1}{p^2 + d_1 p + d_2} = \frac{2A_1 p + 2A_1 a_0 - 2A_2 \omega_0}{(p + a_0)^2 + \omega_0^2}$$

$$a_0 = d_1 / 2 = 1/(2RC)$$

$$\omega_0 = \sqrt{d_2 - a_0^2} = \sqrt{1/(LC) - 1/(4R^2C^2)}$$

$$A_1 = \frac{1}{2} n_0$$

$$A_2 = \frac{1}{2\omega_0}(a_0 n_0 - n_1)$$

$$m(t) = 2A_1 \exp(-a_0 t)\cos(\omega_0 t) - 2A_2 \exp(-a_0 t)\sin(\omega_0 t) \qquad (4.27)$$

$$m_{11}(t) = \exp(-a_0 t)\cos(\omega_0 t) + \frac{a_0}{\omega_0}\exp(-a_0 t)\sin(\omega_0 t)$$

$$m_{13}(t) = -\frac{1}{\omega_0 L}\exp(-a_0 t)\sin(\omega_0 t)$$

$$m_{31}(t) = \frac{1}{\omega_0 C}\exp(-a_0 t)\sin(\omega_0 t)$$

$$m_{33}(t) = \exp(-a_0 t)\cos(\omega_0 t) - \frac{a_0}{\omega_0}\exp(-a_0 t)\sin(\omega_0 t)$$

- Calculation of M3:

$$M3 = e^{At} = \begin{bmatrix} m_{11}(t) & m_{12}(t) & m_{13}(t) \\ m_{21}(t) & m_{22}(t) & m_{23}(t) \\ m_{31}(t) & m_{32}(t) & m_{33}(t) \end{bmatrix} = \begin{bmatrix} m_{11}(t) & m_{12}(t) & 0 \\ m_{21}(t) & m_{22}(t) & 0 \\ 0 & 0 & \exp\left(-\frac{1}{RC}t\right) \end{bmatrix}$$

$$M(p) = \frac{n_0 p + n_1}{p^2 + d_1 p + d_2} = \frac{2A_1 p + 2A_1 a_0 - 2A_2 \omega_0}{(p + a_0)^2 + \omega_0^2}$$

$$a_0 = d_1/2 = 1/(2RC)$$

$$\omega_0 = \sqrt{d_2 - a_0^2} = \sqrt{1/(LC) - 1/(4R^2C^2)}$$

$$A_1 = \frac{1}{2}n_0$$

$$A_2 = \frac{1}{2\omega_0}(a_0 n_0 - n_1)$$

$$m(t) = 2A_1 \exp(-a_0 t)\cos(\omega_0 t) - 2A_2 \exp(-a_0 t)\sin(\omega_0 t) \tag{4.28}$$

$$m_{11}(t) = \exp(-a_0 t)\cos(\omega_0 t) + \frac{a_0}{\omega_0}\exp(-a_0 t)\sin(\omega_0 t)$$

$$m_{12}(t) = -\frac{1}{\omega_0 L}\exp(-a_0 t)\sin(\omega_0 t)$$

$$m_{21}(t) = \frac{1}{\omega_0 C}\exp(-a_0 t)\sin(\omega_0 t)$$

$$m_{22}(t) = \exp(-a_0 t)\cos(\omega_0 t) - \frac{a_0}{\omega_0}\exp(-a_0 t)\sin(\omega_0 t)$$

- Calculation of M4:

$$M4 = e^{At} = \begin{bmatrix} m_{11}(t) & m_{12}(t) & m_{13}(t) \\ m_{21}(t) & m_{22}(t) & m_{23}(t) \\ m_{31}(t) & m_{32}(t) & m_{33}(t) \end{bmatrix}$$

$$M(p) = \frac{n_0 p + n_1}{p^2 + d_1 p + d_2} = \frac{2A_1 p + 2A_1 a_0 - 2A_2 \omega_0}{(p + a_0)^2 + \omega_0^2}$$

$$a_0 = d_1/2 = 1/(2RC)$$

$$\omega_1 = \sqrt{d_2 - a_0^2} = \sqrt{2/(LC) - 1/(4R^2C^2)}$$

$$A_1 = \frac{1}{2}n_0$$

$$A_2 = \frac{1}{2\omega_1}(a_0 n_0 - n_1)$$

$$m(t) = 2A_1 \exp(-a_0 t)\cos(\omega_1 t) - 2A_2 \exp(-a_0 t)\sin(\omega_1 t)$$

$$m_{11}(t)=\exp(-a_0t)\cos(\omega_1 t)+\frac{a_0}{\omega_1}\exp(-a_0t)\sin(\omega_1 t) \tag{4.29}$$

$$m_{12}(t)=m_{13}(t)=-\frac{1}{\omega_1 L}\exp(-a_0t)\sin(\omega_1 t)$$

$$m_{21}(t)=m_{31}(t)=\frac{1}{\omega_1 C}\exp(-a_0t)\sin(\omega_1 t)$$

$$M(p)=\frac{n_0p^2+n_1p+n_2}{p^3+d_1p^2+d_2p+d_3}=\frac{A_0}{(p-s_1)}+\frac{2A_1p+2A_1a_0-2A_2\omega_1}{(p+a_0)^2+\omega_1^2}$$

$$s_1=-1/(RC)=-2a_0$$

$$A_0=\frac{n_0s_1^2+n_1s_1+n_2}{s_1^2+2a_0s_1+a_0^2+\omega_1^2}$$

$$A_1=\frac{n_0\left(a_0^2+\omega_1^2+2a_0s_1\right)-n_1s_1-n_2}{2\left((a_0+s_1)^2+\omega_1^2\right)}$$

$$A_2=\frac{n_0\left(a_0^3+a_0^2s_1+a_0\omega_1^2-\omega_1^2s_1\right)-n_1\left(a_0^2+s_1a_0+\omega_1^2\right)+n_2(a_0+s_1)}{2\omega_1\left((a_0+s_1)^2+\omega_1^2\right)}$$

$$m(t)=A_0\exp(s_1t)+2\exp(-a_0t)\left[A_1\cos(\omega_1 t)-A_2\sin(\omega_1 t)\right]$$

$$m_{22}(t)=m_{33}(t)=\frac{1}{2}\exp(-2a_0t)+\frac{1}{2}\exp(-a_0t)\left[\cos(\omega_1 t)-\frac{a_0}{\omega_1}\sin(\omega_1 t)\right]$$

$$m_{23}(t)=m_{32}(t)=-\frac{1}{2}\exp(-2a_0t)+\frac{1}{2}\exp(-a_0t)\left[\cos(\omega_1 t)-\frac{a_0}{\omega_1}\sin(\omega_1 t)\right]$$

4.2.3 Identifying the Natural and Forced Response

4.2.3.1 Natural Response Solution

With the notation $h=t-t_0$, the calculation of the natural response is then done using:

$$\begin{bmatrix} \mathrm{i}_{\mathrm{L}}^{\mathrm{L}}(t) \\ \mathrm{v}_1^{\mathrm{L}}(t) \\ \mathrm{v}_2^{\mathrm{L}}(t) \end{bmatrix}=\begin{bmatrix} m_{11}(h) & m_{12}(h) & m_{13}(h) \\ m_{21}(h) & m_{22}(h) & m_{23}(h) \\ m_{31}(h) & m_{32}(h) & m_{33}(h) \end{bmatrix}\begin{bmatrix} \mathrm{i}_{\mathrm{L}}(t_0) \\ \mathrm{v}_1(t_0) \\ \mathrm{v}_2(t_0) \end{bmatrix} \tag{4.30}$$

4.2.3.2 Forced Response Solution

The forced response of the system can be calculated as follows:

$$\begin{bmatrix} i_L^F(t) \\ v_1^F(t) \\ v_2^F(t) \end{bmatrix} = \int_{t_0}^{t} e^{A(t-\tau)} Bu(\tau) d\tau = \int_{t_0}^{t} \begin{bmatrix} m_{11}(t-\tau) & m_{12}(t-\tau) & m_{13}(t-\tau) \\ m_{21}(t-\tau) & m_{22}(t-\tau) & m_{23}(t-\tau) \\ m_{31}(t-\tau) & m_{32}(t-\tau) & m_{33}(t-\tau) \end{bmatrix} \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} u(\tau) d\tau$$

$$\begin{bmatrix} i_L^F(t) \\ v_1^F(t) \\ v_2^F(t) \end{bmatrix} = \int_{t_0}^{t} \begin{bmatrix} m_{11}(t-\tau) \\ m_{21}(t-\tau) \\ m_{31}(t-\tau) \end{bmatrix} u(\tau) d\tau = \begin{bmatrix} \int_{t_0}^{t} m_{11}(t-\tau) u(\tau) d\tau \\ \int_{t_0}^{t} m_{21}(t-\tau) u(\tau) d\tau \\ \int_{t_0}^{t} m_{31}(t-\tau) u(\tau) d\tau \end{bmatrix} = \frac{V_{dc}}{L} \begin{bmatrix} \int_{t_0}^{t} m_{11}(t-\tau) d\tau \\ \int_{t_0}^{t} m_{21}(t-\tau) d\tau \\ \int_{t_0}^{t} m_{31}(t-\tau) d\tau \end{bmatrix} \quad (4.31)$$

Therefore ;

- Mode 1 :

$$\begin{bmatrix} i_L^F(t) \\ v_1^F(t) \\ v_2^F(t) \end{bmatrix} = \frac{V_s}{L} \begin{bmatrix} \int_{t_0}^{t} m_{11}(t-\tau) d\tau \\ \int_{t_0}^{t} m_{21}(t-\tau) d\tau \\ \int_{t_0}^{t} m_{31}(t-\tau) d\tau \end{bmatrix} = \begin{bmatrix} \frac{V_{dc}}{L} h \\ 0 \\ 0 \end{bmatrix} \quad (4.32)$$

- Mode 2 :

$$\begin{bmatrix} i_L^F(t) \\ v_1^F(t) \\ v_2^F(t) \end{bmatrix} = \begin{bmatrix} -\frac{V_{dc}}{R} \left\{ -1 + 1\exp(-a_0 h)\cos(\omega_0 h) + \frac{1}{2}\left(\frac{a_0}{\omega_0} - \frac{\omega_0}{a_0} \right) \exp(-a_0 h)\sin(\omega_0 h) \right\} \\ 0 \\ -V_{dc} \left\{ -1 + \exp(-a_0 h)\cos(\omega_0 h) + \frac{a_0}{\omega_0} \exp(-a_0 h)\sin(\omega_0 h) \right\} \end{bmatrix} \quad (4.31)$$

- Mode 3 :

$$\begin{bmatrix} i_L^F(t) \\ v_1^F(t) \\ v_2^F(t) \end{bmatrix} = \begin{bmatrix} -\frac{V_{dc}}{R} \left\{ -1 + 1\exp(-a_0 h)\cos(\omega_0 h) + \frac{1}{2}\left(\frac{a_0}{\omega_0} - \frac{\omega_0}{a_0} \right) \exp(-a_0 h)\sin(\omega_0 h) \right\} \\ -V_{dc} \left\{ -1 + \exp(-a_0 h)\cos(\omega_0 h) + \frac{a_0}{\omega_0} \exp(-a_0 h)\sin(\omega_0 h) \right\} \\ 0 \end{bmatrix} \quad (4.32)$$

- Mode 4 :

$$\begin{bmatrix} \mathrm{i}_{\mathrm{L}}^{\mathrm{F}}(t) \\ \mathrm{v}_{1}^{\mathrm{F}}(t) \\ \mathrm{v}_{2}^{\mathrm{F}}(t) \end{bmatrix} = \begin{bmatrix} -\frac{V_{dc}}{4R}\left\{-2+2\exp(-a_0 h)\cos(\omega_1 h)+\left(\frac{a_0}{\omega_1}-\frac{\omega_1}{a_0}\right)\exp(-a_0 h)\sin(\omega_1 h)\right\} \\ -\frac{V_{dc}}{2}\left\{-1+\exp(-a_0 h)\cos(\omega_1 h)+\frac{a_0}{\omega_1}\exp(-a_0 h)\sin(\omega_1 h)\right\} \\ -\frac{V_{dc}}{2}\left\{-1+\exp(-a_0 h)\cos(\omega_1 h)+\frac{a_0}{\omega_1}\exp(-a_0 h)\sin(\omega_1 h)\right\} \end{bmatrix} \quad (4.33)$$

4.2.4 The approximate Solution of the System

For each Mode, the system response is ultimately found by summing of the natural response and the forced one;

$$\begin{bmatrix} \mathrm{i}_{\mathrm{L}}(t) \\ \mathrm{V}_{1}(t) \\ \mathrm{V}_{2}(t) \end{bmatrix} = \begin{bmatrix} \mathrm{i}_{\mathrm{L}}^{\mathrm{L}}(t) \\ \mathrm{v}_{1}^{\mathrm{L}}(t) \\ \mathrm{v}_{2}^{\mathrm{L}}(t) \end{bmatrix} + \begin{bmatrix} \mathrm{i}_{\mathrm{L}}^{\mathrm{F}}(t) \\ \mathrm{v}_{1}^{\mathrm{F}}(t) \\ \mathrm{v}_{2}^{\mathrm{F}}(t) \end{bmatrix} \quad (4.34)$$

4.2.4.1 Solution of Mode I

The solution for Mode 1 is very simple and has the following form:

$$\begin{aligned} i_L(t) &= i_L(t_0)+\frac{V_{dc}}{L}h \\ v_1(t) &= v_1(t_0)\exp(-2a_0 h) \\ v_2(t) &= v_2(t_0)\exp(-2a_0 h) \end{aligned} \quad (4.35)$$

4.2.4.2 Solution of Mode 2

For Mode 2;

$$\begin{aligned} i_L(t) = i_L(t_0)&\left[\exp(-a_0 h)\cos(\omega_0 h)+\frac{a_0}{\omega_0}\exp(-a_0 h)\sin(\omega_0 h)\right]-v_2(t_0)\frac{1}{\omega_0 L}\exp(-a_0 h)\sin(\omega_0 h) \\ &-\frac{V_{dc}}{R}\left\{-1+\exp(-a_0 h)\cos(\omega_0 h)+\frac{1}{2}\left(\frac{a_0}{\omega_0}-\frac{\omega_0}{a_0}\right)\exp(-a_0 h)\sin(\omega_0 h)\right\} \end{aligned}$$

$$v_1(t) = v_1(t_0)\exp(-2a_0h) \tag{4.36}$$

$$v_2(t) = i_L(t_0)\frac{1}{\omega_0 C}\exp(-a_0h)\sin(\omega_0h) + v_2(t_0)\left[\exp(-a_0h)\cos(\omega_0h) - \frac{a_0}{\omega_0}\exp(-a_0h)\sin(\omega_0h)\right]$$
$$-V_{dc}\left\{-1+\exp(-a_0h)\cos(\omega_0h)+\frac{a_0}{\omega_0}\exp(-a_0h)\sin(\omega_0h)\right\}$$

By doing some simplifications;

$$i_L(t) - \frac{V_{dc}}{R} = \left[i_L(t_0) - \frac{V_{dc}}{R}\right]\exp(-a_0h)\cos(\omega_0h) + \left[\frac{a_0}{\omega_0}i_L(t_0) - \frac{1}{\omega_0 L}v_2(t_0) - \left(\frac{a_0}{\omega_0} - \frac{\omega_0}{a_0}\right)\frac{V_{dc}}{2R}\right]\exp(-a_0h)\sin(\omega_0h)$$

$$v_1(t) = v_1(t_0)\exp(-2a_0h) \tag{4.37}$$

$$v_2(t) - V_{dc} = [v_2(t_0) - V_{dc}]\exp(-a_0h)\cos(\omega_0h) + \frac{a_0}{\omega_0}[2Ri_L(t_0) - v_2(t_0) - V_{dc}]\exp(-a_0h)\sin(\omega_0h)$$

Then

$$i_L(t) - \frac{V_{dc}}{R} = \left[i_L(t_0) - \frac{V_{dc}}{R}\right]\exp(-a_0h)\cos(\omega_0h) + \left[\frac{a_0}{\omega_0}\left[i_L(t_0) - \frac{V_{dc}}{R}\right] - \frac{1}{2R}\left(\frac{a_0}{\omega_0} + \frac{\omega_0}{a_0}\right)(v_2(t_0) - V_{dc})\right]\exp(-a_0h)\sin(\omega_0h)$$

$$v_1(t) = v_1(t_0)\exp(-2a_0h) \tag{4.38}$$

$$v_2(t) - V_{dc} = [v_2(t_0) - V_{dc}]\exp(-a_0h)\cos(\omega_0h) + \frac{a_0}{\omega_0}\left[2R\left[i_L(t_0) - \frac{V_{dc}}{R}\right] - (v_2(t_0) - V_{dc})\right]\exp(-a_0h)\sin(\omega_0h)$$

If we set $v_2(t_0) - V_{dc} = 2R\alpha\left[i_L(t_0) - \frac{V_{dc}}{R}\right]$ and $i_L(t_0) - \frac{V_{dc}}{R} \neq 0$, then we obtain

$$i_L(t) - \frac{V_{dc}}{R} = \left[i_L(t_0) - \frac{V_{dc}}{R}\right]\exp(-a_0h)\left(\cos(\omega_0h) + \left[\frac{a_0}{\omega_0} - \left(\frac{a_0}{\omega_0} + \frac{\omega_0}{a_0}\right)\alpha\right]\sin(\omega_0h)\right)$$

$$v_1(t) = v_1(t_0)\exp(-2a_0h) \tag{4.39}$$

$$v_2(t) - V_{dc} = 2R\left[i_L(t_0) - \frac{V_{dc}}{R}\right]\exp(-a_0h)\left(\alpha\cos(\omega_0h) + \frac{a_0}{\omega_0}[1-\alpha]\sin(\omega_0h)\right)$$

Approximation for a sufficiently small-time step h as:

$$i_L(t)-\frac{V_{dc}}{R}\approx\left[i_L(t_0)-\frac{V_{dc}}{R}\right]f(h)$$

$$v_1(t)\approx v_1(t_0)(1-2a_0h)$$

$$v_2(t)-V_{dc}\approx 2R\left[i_L(t_0)-\frac{V_{dc}}{R}\right]g(h) \tag{4.40}$$

$$f(h)=(1-a_0h)\left(1+\left[\frac{a_0}{\omega_0}-\left(\frac{a_0}{\omega_0}+\frac{\omega_0}{a_0}\right)\alpha\right](\omega_0h)\right)$$

$$g(h)=(1-a_0h)\left(\alpha+\frac{a_0}{\omega_0}[1-\alpha](\omega_0h)\right)$$

$$v_2(t_0)-V_{dc}=2R\alpha\left[i_L(t_0)-\frac{V_{dc}}{R}\right]$$

4.2.4.3 Solution of Mode 3

The same manner as Mode 2, the solution of Mode 3 can be written as:

$$i_L(t)=i_L(t_0)\left[\exp(-a_0h)\cos(\omega_0h)+\frac{a_0}{\omega_0}\exp(-a_0h)\sin(\omega_0h)\right]-v_1(t_0)\frac{1}{\omega_0L}\exp(-a_0h)\sin(\omega_0h)$$
$$-\frac{V_{dc}}{R}\left\{-1+\exp(-a_0h)\cos(\omega_0h)+\frac{1}{2}\left(\frac{a_0}{\omega_0}-\frac{\omega_0}{a_0}\right)\exp(-a_0h)\sin(\omega_0h)\right\}$$

$$v_1(t)=i_L(t_0)\frac{1}{\omega_0C}\exp(-a_0h)\sin(\omega_0h)+v_1(t_0)\left[\exp(-a_0h)\cos(\omega_0h)-\frac{a_0}{\omega_0}\exp(-a_0h)\sin(\omega_0h)\right]$$
$$-V_{dc}\left\{-1+\exp(-a_0h)\cos(\omega_0h)+\frac{a_0}{\omega_0}\exp(-a_0h)\sin(\omega_0h)\right\}$$

$$v_2(t)=v_2(t_0)\exp(-2a_0h) \tag{4.41}$$

Simplifying the equation yields

$$i_L(t)-\frac{V_{dc}}{R}=\left[i_L(t_0)-\frac{V_{dc}}{R}\right]\exp(-a_0h)\cos(\omega_0h)+\left[\frac{a_0}{\omega_0}\left[i_L(t_0)-\frac{V_{dc}}{R}\right]-\frac{1}{2R}\left(\frac{a_0}{\omega_0}+\frac{\omega_0}{a_0}\right)(v_1(t_0)-V_{dc})\right]\exp(-a_0h)\sin(\omega_0h)$$

$$v_2(t)=v_2(t_0)\exp(-2a_0h) \tag{4.42}$$

$$v_1(t)-V_{dc}=\left[v_1(t_0)-V_{dc}\right]\exp(-a_0h)\cos(\omega_0h)+\frac{a_0}{\omega_0}\left[2R\left[i_L(t_0)-\frac{V_{dc}}{R}\right]-\left(v_1(t_0)-V_{dc}\right)\right]\exp(-a_0h)\sin(\omega_0h)$$

Assuming that $v_1(t_0)-V_{dc}=2R\beta\left[i_L(t_0)-\frac{V_{dc}}{R}\right]$ with $i_L(t_0)-\frac{V_{dc}}{R}\neq 0$, we obtain:

$$i_L(t)-\frac{V_{dc}}{R}=\left[i_L(t_0)-\frac{V_{dc}}{R}\right]\exp(-a_0h)\left(\cos(\omega_0h)+\left[\frac{a_0}{\omega_0}-\left(\frac{a_0}{\omega_0}+\frac{\omega_0}{a_0}\right)\beta\right]\sin(\omega_0h)\right)$$

$$v_1(t)-V_{dc}=2R\left[i_L(t_0)-\frac{V_{dc}}{R}\right]\exp(-a_0h)\left(\beta\cos(\omega_0h)+\frac{a_0}{\omega_0}[1-\beta]\sin(\omega_0h)\right) \quad (4.43)$$

$$v_2(t)=v_2(t_0)\exp(-2a_0h)$$

Therefore, if the time step h is sufficiently small, the solution can be approximated to:

$$i_L(t)-\frac{V_{dc}}{R}\approx\left[i_L(t_0)-\frac{V_{dc}}{R}\right]f(h)$$

$$v_1(t)-V_{dc}\approx 2R\left[i_L(t_0)-\frac{V_{dc}}{R}\right]g(h)$$

$$v_2(t)\approx v_2(t_0)(1-2a_0h) \quad (4.44)$$

$$f(h)=(1-a_0h)\left(1+\left[\frac{a_0}{\omega_0}-\left(\frac{a_0}{\omega_0}+\frac{\omega_0}{a_0}\right)\alpha\right](\omega_0h)\right)$$

$$g(h)=(1-a_0h)\left(\alpha+\frac{a_0}{\omega_0}[1-\alpha](\omega_0h)\right)$$

$$v_1(t_0)-V_{dc}=2R\beta\left[i_L(t_0)-\frac{V_{dc}}{R}\right]$$

4.2.4.4 Solution of Mode 4

In Mode 4, the values of inductor current and output voltages can be written as:

$$i_L(t) = i_L(t_0)\left[\exp(-a_0 h)\cos(\omega_1 h) + \frac{a_0}{\omega_1}\exp(-a_0 h)\sin(\omega_1 h)\right] - (v_1(t_0) + v_2(t_0))\frac{1}{\omega_1 L}\exp(-a_0 h)\sin(\omega_1 h)$$
$$-\frac{V_{dc}}{2R}\left\{-1 + \exp(-a_0 h)\cos(\omega_1 h) + \frac{1}{2}\left(\frac{a_0}{\omega_1} - \frac{\omega_1}{a_0}\right)\exp(-a_0 h)\sin(\omega_1 h)\right\}$$

$$v_1(t) = i_L(t_0)\frac{1}{\omega_1 C}\exp(-a_0 h)\sin(\omega_1 h) + v_1(t_0)\left[\frac{1}{2}\exp(-2a_0 h) + \frac{1}{2}\exp(-a_0 h)\left[\cos(\omega_1 h) - \frac{a_0}{\omega_1}\sin(\omega_1 h)\right]\right]$$
$$+ v_2(t_0)\left[-\frac{1}{2}\exp(-2a_0 h) + \frac{1}{2}\exp(-a_0 h)\left[\cos(\omega_1 h) - \frac{a_0}{\omega_1}\sin(\omega_1 h)\right]\right] \quad (4.45)$$

$$v_2(t) = i_L(t_0)\frac{1}{\omega_1 C}\exp(-a_0 h)\sin(\omega_1 h) + v_1(t_0)\left[-\frac{1}{2}\exp(-2a_0 h) + \frac{1}{2}\exp(-a_0 h)\left[\cos(\omega_1 h) - \frac{a_0}{\omega_1}\sin(\omega_1 h)\right]\right]$$
$$+ v_2(t_0)\left[\frac{1}{2}\exp(-2a_0 h) + \frac{1}{2}\exp(-a_0 h)\left[\cos(\omega_1 h) - \frac{a_0}{\omega_1}\sin(\omega_1 h)\right]\right]$$
$$-\frac{V_{dc}}{2}\left\{-1 + \exp(-a_0 h)\cos(\omega_1 h) + \frac{a_0}{\omega_1}\exp(-a_0 h)\sin(\omega_1 h)\right\}$$

Applying some simplifications, equation (4.45) can be written as:

$$i_L(t) - \frac{V_{dc}}{2R} = \left[i_L(t_0) - \frac{V_{dc}}{2R}\right]\exp(-a_0 h)\cos(\omega_1 h) + \left[+\frac{a_0}{\omega_1}i_L(t_0) - \frac{1}{\omega_1 L}(v_1(t_0) + v_2(t_0)) - \left(\frac{a_0}{\omega_1} - \frac{\omega_1}{a_0}\right)\frac{V_{dc}}{4R}\right]$$
$$\exp(-a_0 h)\sin(\omega_1 h)$$

$$v_1(t) - \frac{V_{dc}}{2} = \frac{1}{2}[v_1(t_0) + v_2(t_0) - V_{dc}]\exp(-a_0 h)\cos(\omega_1 h) + \frac{a_0}{\omega_1}\left[2Ri_L(t_0) - \frac{1}{2}v_1(t_0) - \frac{1}{2}v_2(t_0) - \frac{V_{dc}}{2}\right]$$
$$\exp(-a_0 h)\sin(\omega_1 h) + \frac{1}{2}[v_1(t_0) - v_2(t_0)]\exp(-2a_0 h) \quad (4.46)$$

$$v_2(t) - \frac{V_{dc}}{2} = \frac{1}{2}[v_1(t_0) + v_2(t_0) - V_{dc}]\exp(-a_0 h)\cos(\omega_1 h) + \frac{a_0}{\omega_1}\left[2Ri_L(t_0) - \frac{1}{2}v_1(t_0) - \frac{1}{2}v_2(t_0) - \frac{V_{dc}}{2}\right]$$
$$\exp(-a_0 h)\sin(\omega_1 h) - \frac{1}{2}[v_1(t_0) - v_2(t_0)]\exp(-2a_0 h)$$

We note from (4.46) that the formula of $v_1(t)$ and $v_2(t)$ are the same for the first two terms and differ only by the sign for the last term. For a large enough period of time, $v_1(t)$ and $v_2(t)$ tend to have the same values as:

$$\Delta(t) = v_1(t) - v_2(t) = (v_1(t_0) - v_2(t_0))\exp(-2a_0 h).$$

Therefore

$$i_L(t)-\frac{V_{dc}}{2R}=\left[i_L(t_0)-\frac{V_{dc}}{2R}\right]\exp(-a_0h)\cos(\omega_1h)+$$
$$\left[+\frac{a_0}{\omega_1}\left[i_L(t_0)-\frac{V_{dc}}{2R}\right]-\frac{1}{4R}\left(\frac{a_0}{\omega_1}+\frac{\omega_1}{a_0}\right)(v_1(t_0)+v_2(t_0)-V_{dc})\right]\exp(-a_0h)\sin(\omega_1h)$$
$$v_1(t)-\frac{V_{dc}}{2}=\frac{1}{2}[v_1(t_0)+v_2(t_0)-V_{dc}]\exp(-a_0h)\cos(\omega_1h)+$$
$$\frac{a_0}{\omega_1}\left[2R\left[i_L(t_0)-\frac{V_{dc}}{2R}\right]-\frac{1}{2}(v_1(t_0)+v_2(t_0)-V_{dc})\right]\exp(-a_0h)\sin(\omega_1h) \quad (4.47)$$
$$+\frac{1}{2}[v_1(t_0)-v_2(t_0)]\exp(-2a_0h)$$

$$v_2(t)-\frac{V_{dc}}{2}=\frac{1}{2}[v_1(t_0)+v_2(t_0)-V_{dc}]\exp(-a_0h)\cos(\omega_1h)+$$
$$\frac{a_0}{\omega_1}\left[2R\left[i_L(t_0)-\frac{V_{dc}}{2R}\right]-\frac{1}{2}(v_1(t_0)+v_2(t_0)-V_{dc})\right]\exp(-a_0h)\sin(\omega_1h)$$
$$-\frac{1}{2}[v_1(t_0)-v_2(t_0)]\exp(-2a_0h)$$

By setting $v_o(t_0)=v_1(t_0)+v_2(t_0)$ and $v_o(t_0)-V_{dc}=4R\gamma\left[i_L(t_0)-\frac{V_{dc}}{2R}\right]$ with

$i_L(t_0)-\frac{V_{dc}}{2R}\neq 0$ it gives:

$$i_L(t)-\frac{V_{dc}}{2R}=\left[i_L(t_0)-\frac{V_{dc}}{2R}\right]\exp(-a_0h)\cos(\omega_1h)$$
$$+\left[+\frac{a_0}{\omega_1}\left[i_L(t_0)-\frac{V_{dc}}{2R}\right]-\frac{1}{4R}\left(\frac{a_0}{\omega_1}+\frac{\omega_1}{a_0}\right)(v_o(t_0)-V_{dc})\right]\exp(-a_0h)\sin(\omega_1h)$$
$$v_o(t)-V_{dc}=[v_o(t_0)-V_{dc}]\exp(-a_0h)\cos(\omega_1h) \quad (4.48)$$
$$+\frac{a_0}{\omega_1}\left[4R\left[i_L(t_0)-\frac{V_{dc}}{2R}\right]-(v_o(t_0)-V_{dc})\right]\exp(-a_0h)\sin(\omega_1h)$$

Therefore

$$i_L(t)-\frac{V_{dc}}{2R}=\left[i_L(t_0)-\frac{V_{dc}}{2R}\right]\exp(-a_0h)\left(\cos(\omega_1h)+\left[+\frac{a_0}{\omega_1}-\left(\frac{a_0}{\omega_1}+\frac{\omega_1}{a_0}\right)\gamma\right]\sin(\omega_1h)\right)$$
$$v_o(t)-V_{dc}=4R\left[i_L(t_0)-\frac{V_{dc}}{2R}\right]\exp(-a_0h)\left(\gamma\cos(\omega_1h)+\frac{a_0}{\omega_1}[1-\gamma]\sin(\omega_1h)\right) \quad (4.49)$$

For an approximation of time h, results can be as follows:

$$i_L(t) - \frac{V_{dc}}{2R} \approx \left[i_L(t_0) - \frac{V_{dc}}{2R} \right] f(h)$$

$$v_o(t) - V_{dc} \approx 4R \left[i_L(t_0) - \frac{V_{dc}}{2R} \right] g(h)$$

$$f(h) = (1 - a_0 h) \left(1 + \left[\frac{a_0}{\omega_1} - \left(\frac{a_0}{\omega_1} + \frac{\omega_1}{a_0} \right) \gamma \right] (\omega_1 h) \right) \tag{4.50}$$

$$g(h) = (1 - a_0 h) \left(\gamma + \frac{a_0}{\omega_1} [1 - \gamma] (\omega_1 h) \right)$$

$$v_o(t_0) - V_{dc} = 4R\gamma \left[i_L(t_0) - \frac{V_{dc}}{2R} \right]$$

4.2.5 Evaluation of the System Solutions

The dynamic modeling of the DOBC with the proposed solution given in (4.35), (4.40), (4.44), and (4.50) is validated by Matlab software. The set of parameters for the system is given as follows:

$$L = 0.003\, mH, C1 = C2 = 200\ \mu F, R1 = R2 = 250\,\Omega,$$
$$V_{dc} = 100\, V, V_{ref} = 300\, V$$

Figure 4.2 shows the results of each mode with initial condition set to $V_1 = V_2 = 100V$ From that, it can be observed that in mode 1 the inductor current is increasing and the capacitor voltages discharged through the load, while in modes 2, 3, and 4 the inductor current is discharged through one capacitor (C1 or C2) if modes 2 and 3 are set or through both of them like a normal boost converter in mode 4. Therefore, based on the initial conditions and the relation between the input voltage and the desired output voltage of each capacitor, the control of power flow through the desired mode will achieve fast control and balanced DC-bus voltage.

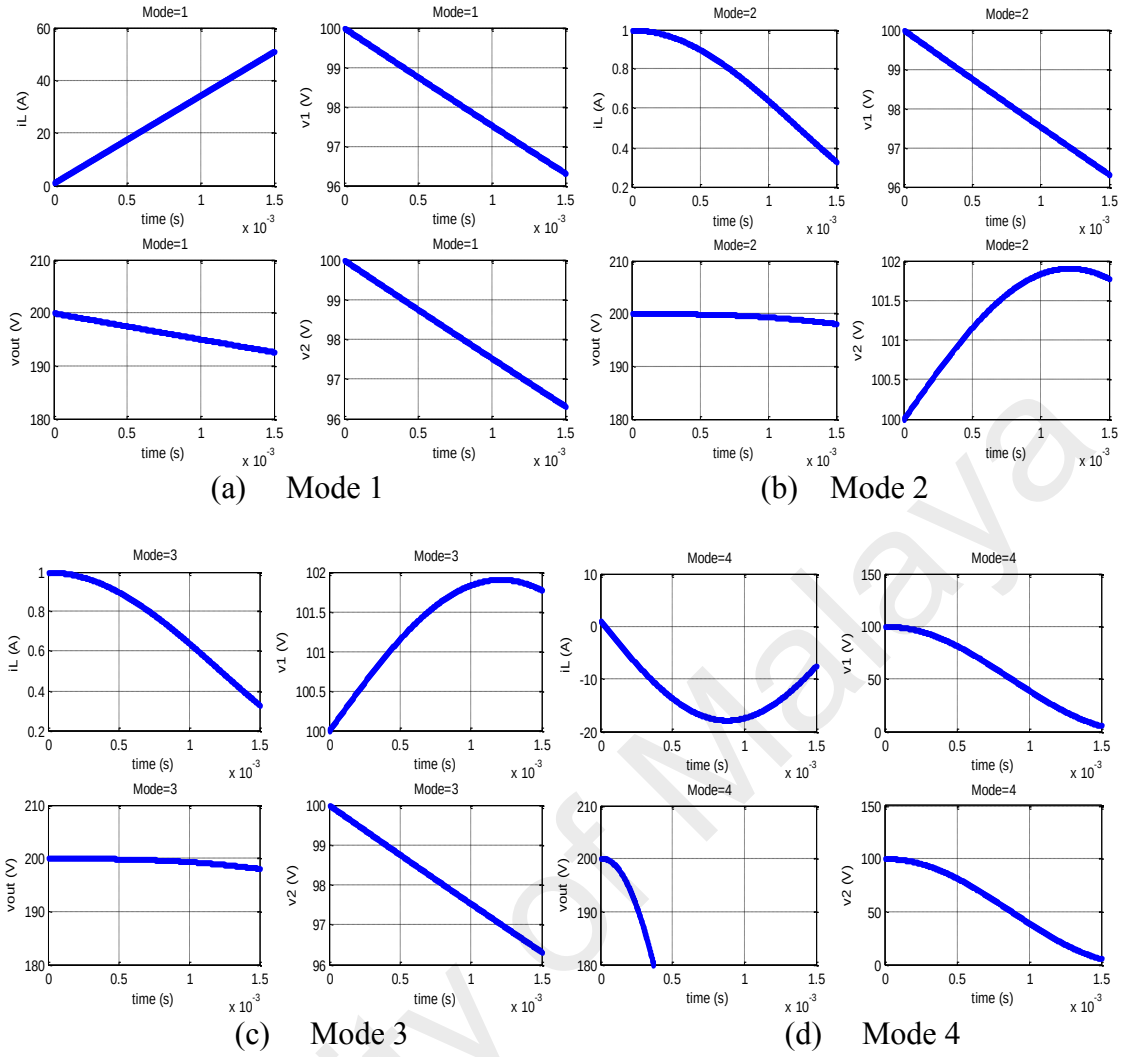


Figure 4-2: DOBC response in each mode with initial condition 100 V

4.3 Sensorless Boundary Control Method

Sensorless boundary control method is a sensorless current method that provides the operating benefits of boundary control without current sensing. From the state space of the converter, a mathematical model is developed that describes the behaviours of the converter under different conditions. From the mathematical model, the unmeasurable variables are estimated. In sensorless current method the inductor current is predicted by integrating the inductor voltage. The integral of the inductor voltage contains all the dynamic information of the current signal.

In order to realize a sensorless boundary control for the DOBC, an accurate modelling system as described in the previous section is needed. However, for simplification purpose, the following assumptions are made:

- The DOBC is working in region I where the constant input voltage V_{dc} is less than V_1 and also than V_2
- The converter works in the continuous current mode to overcome the case where all switches are OFF
- The main control of the converter is based on boundary control using state-energy plane, the sensorless method is used to estimate the inductor current needed for the application of boundary control.

With reference to Figure 4.3, the output voltage of the DOBC is governed by the switching pair {(Q1, Q2), (D1, D2)}, and hence a balanced output voltage can be achieved by operating the converter in Mode 1 and Mode 2 or Mode 1 and Mode 3 simultaneously, which means either {(1, 1), (0,0)}and {(1, 0), (0,1)} or {(1, 1), (0,0)}and {(0,1), (1,0)}. Consequently, it is clear that the DOBC is controlled as two conventional boost converter each one is used to maintain the same output voltage. Therefore, for simplification reasons, the sensorless boundary control is described only for a simple conventional boost converter then it will be generalized for the full DOBC.

For example, using the conventional lower boost 1 and neglecting the output voltage of the capacitor C1, the state space obtained are:

$$\textbf{Stage 1: } (Q_1, Q_2) = (1,1): \begin{bmatrix} \mathrm{i_L} \\ \mathrm{v_2} \end{bmatrix}' = \begin{bmatrix} 0 & 0 \\ 0 & -\dfrac{1}{RC} \end{bmatrix} \begin{bmatrix} \mathrm{i_L} \\ \mathrm{v_2} \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} v_{dc} \tag{4.51}$$

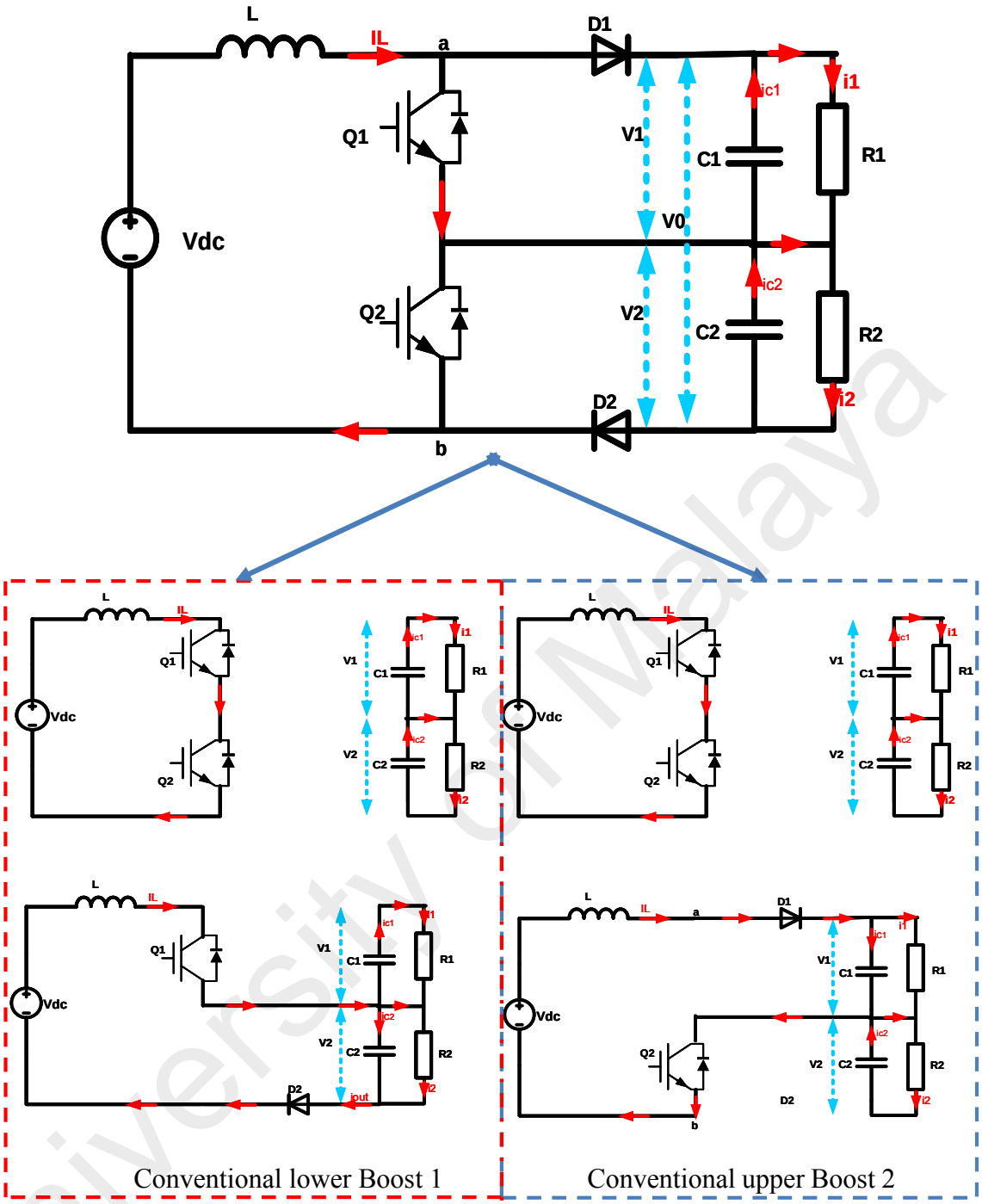


Figure 4-3: Control of DOBC in region I

$$\textbf{Stage 2: } (Q_1,Q_2)=(1,0):\begin{bmatrix} i_L \\ v_2 \end{bmatrix}' = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}\begin{bmatrix} i_L \\ v_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_{dc} \tag{4.52}$$

The state space solutions can be obtained directly from the previous analysis (equations (4.35) and (4.40)) as follows:

- **Stage 1:**

$$i_L(t) = i_L(t_0) + \frac{V_{dc}}{L} h \tag{4.53}$$

$$v_2(t) = v_2(t_0)\exp(-2a_0 h)$$

- **Stage 2 :**

$$\mathrm{i}_L(t) = i_L(t_0)\exp(-a_0 h)\left[\cos(\omega_0 h) + \frac{a_0}{\omega_0}\sin(\omega_0 h)\right] + \frac{1}{\omega_0 L}[V_{dc} - v_2(t_0)]\exp(-a_0 h)\sin(\omega_0 h)$$

$$\mathrm{v}_2(t) = \frac{1}{\omega_0 C} i_L(t_0)\exp(-a_0 h)\sin(\omega_0 h) + v_2(t_0)\exp(-a_0 h)\left[\cos(\omega_0 h) - \frac{a_0}{\omega_0}\sin(\omega_0 h)\right]$$
$$- V_{dc}\exp(-a_0 h)\left[\cos(\omega_0 h) + \frac{a_0}{\omega_0}\sin(\omega_0 h)\right] + V_{dc}$$

$$a_0 = \frac{1}{2RC} \tag{4.54}$$

$$\omega_0 = \sqrt{\frac{1}{LC} - a_0^2}$$

The successive activation of stage 1 and 2 leads to the following model by assuming that: $ec = \exp(-a_0 h_{off})\cos(\omega_0 h_{off})$, and $es = \exp(-a_0 h_{off})\sin(\omega_0 h_{off})$

- Activation of stage 1:

$$I_{on} = i_L(t_0 + h_{on}) = i_L(t_0) + \frac{V_{dc}}{L} h_{on}$$

(4.55)

$$V_{on} = v_2(t_0 + h_{on}) = v_2(t_0)\exp(-2a_0 h_{on})$$

- Activation of stage 2:

$$\alpha = ec + \frac{a_0}{\omega_0} es$$

$$i_L(t_0 + h_{on} + h_{off}) = \alpha I_{on} + \frac{1}{\omega_0 L}(V_{dc} - V_{on})es \tag{4.56}$$

$$v_2(t_0 + h_{on} + h_{off}) = \frac{1}{\omega_0 C} I_{on} es + V_{on}\left(\alpha - 2\frac{a_0}{\omega_0} es\right) - V_{dc}(-1+\alpha)$$

4.3.1 Approximate Model of the Converter

Adapting the following approximations:

For $\omega_0 h < 0.25$ & $a_0 << \omega_0$

$$e^{-a_0 h}\sin(\omega_0 h) \approx (1 - a_0 h)\omega_0 h \approx \omega_0 h$$

$$e^{-a_0 h}\cos(\omega_0 h) \approx (1 - a_0 h)(1 - 0.5\omega_0^2 h^2) \tag{4.57}$$

$$\alpha \approx (1 - a_0 h)(1 - 0.5\omega_0^2 h^2) + a_0 h = 0.5 a_0 \omega_0^2 h^3 - 0.5\omega_0^2 h^2 + 1 \approx 1 - 0.5\omega_0^2 h^2$$

then applying them in equation (4.54) with $h = h_{off}$ yield

$$I_{on} = i_L(t_0) + \frac{V_{dc}}{L} h_{on}$$

$$I_{off} = i_L(t_0 + h_{on} + h_{off}) \approx \alpha I_{on} + \frac{1}{L}(V_{dc} - V_{on}) h_{off} \tag{4.58}$$

$$V_{off} = v_0(t_0 + h_{on} + h_{off}) \approx \frac{h_{off}}{C} I_{on} + V_{on}(\alpha - 2a_0 h_{off}) - V_{dc}(-1+\alpha)$$

Where

$$I_{on} = i_L(t_0) + \frac{V_{dc}}{L} h_{on}$$

$$I_{off} = i_L(t_0 + h_{on} + h_{off}) \approx I_{on} - 0.5\omega_0^2 I_{on} h_{off}^2 + \frac{1}{L}(V_{dc} - V_{on}) h_{off} \tag{4.59}$$

$$V_{off} = v_0(t_0 + h_{on} + h_{off}) \approx \frac{h_{off}}{C} I_{on} + V_{on}(1 - 0.5\omega_0^2 h_{off}^2 - 2a_0 h_{off}) + V_{dc}(0.5\omega_0^2 h_{off}^2)$$

If we neglect the second term in I_{off} to the third term the overall approximate model becomes:

$$I_{on} = i_L(t_0) + \frac{V_{dc}}{L} h_{on}$$

$$V_{on} = v_2(t_0)(1 - 2a_0 h_{on})$$

$$I_{off} = i_L\left(t_0 + h_{on} + h_{off}\right) \approx I_{on} + \frac{1}{L}\left(V_{dc} - V_{on}\right)h_{off} \tag{4.60}$$

$$V_{off} = v_0\left(t_0 + h_{on} + h_{off}\right) \approx 0.5\omega_0^2\left(V_{dc} - V_{on}\right)h_{off}^2 + \left(\frac{1}{C}I_{on} - 2a_0V_{on}\right)h_{off} + V_{on}$$

The final approximate model can be written as:

- **Stage 1**

  For $2a_0h_{on} << 1$

  $$I_{on} = i_L\left(t_0\right) + \frac{V_{dc}}{L}h_{on}$$

  (4.61)

  $$V_{on} \approx v_2\left(t_0\right) - 2a_0v_0\left(t_0\right)h_{on}$$

- **Stage 2**

  For $\omega_0 h < 0.25$ & $a_0 << \omega_0$

  $$I_{off} = I_{on} + \frac{V_{dc} - V_{on}}{L}h_{off}$$

  $$V_{off} \approx V_{on} + 0.5\omega_0^2\left(V_{dc} - V_{on}\right)h_{off}^2 + \left(C^{-1}I_{on} - 2a_0V_{on}\right)h_{off} \tag{4.62}$$

  $$a_0 = \frac{1}{2RC}$$

  $$\omega_0 = \sqrt{\frac{1}{LC} - a_0^2}$$

4.3.2 Inductance Current Estimation in Stage 1

A deep analysis of the approximate Model proposed for the conventional boost model shows the possibility of estimating the inductor current using only the measurement of the input and output voltages of the converter. To perform this estimation, the time axis is divided into small steps of time Δt with identical duration. The successive activation between the two operating modes is done by assuming a time $t = m\Delta t,\ m \in \mathrm{N}$. In stage 1,

the measured output voltage stated on the suggested model (4.60) is used to estimate the value of a_0 , ω_0, and the inductance current I_L. The estimation algorithm proposed in (4.63) required only the measurement value of the output voltage at the beginning and at the end of each elementary interval, in addition also to the interval time Δt .

$$a_0(k+1)=(1-\mu)a_0(k)+\mu\frac{1}{2\Delta t}\left(1-\frac{v_2(k+1)}{v_2(k)}\right)$$

$$\omega_0(k+1)=\sqrt{(LC)^{-1}-a_0(k+1)^2}$$

$$I(k+1)=I(k)+\frac{V_{dc}}{L}\Delta t \qquad (4.63)$$

$$b(k+1)=b(k)$$

$$I_L(k+1)=I(k+1)+b(k+1)$$

At the end of Mode 1, $v_2(k+1)=V_{on}$ and $I_L(k+1)=I_{on}$. If $I(1)=0$, $b(k)$ represents an estimate of the unknown initial value of the inductance current.

4.3.3 Inductance Current Estimation in Stage 2

In Stage 2, the converter output voltage from the approximate model (4.60) is utilized to estimate the inductance current. At this time, a combination between the value of current in stage 1 with an unknown initial value *b(k)* and the output voltage in stage 2 is made as follows:

$$I(k+1)=I(k)+\frac{V_{dc}-v_2(k)}{L}\Delta t$$

$$I_L(k+1)=I(k+1)+b(k) \qquad (4.64)$$

$$C\frac{v_0(k+1)-v_2(k)}{\Delta t}+2a_0(k)Cv_2(k)-I(k)\approx 0.5\omega_0(k+1)^2\,C(V_{dc}-v_2(k))\Delta t+b(k)$$

As Δt is small, then the term $0.5\omega_0(k+1)^2\,C(V_{dc}-v_0(k))\Delta t$ can be ignored and *b(k)* can be estimated by:

$$b(k+1)=(1-\mu)b(k)+\mu\left(C\frac{v_2(k+1)-v_2(k)}{\Delta t}+2a_0(k+1)Cv_2(k)-I(k)\right) \tag{4.65}$$

According to the proposed method, it is possible to estimate the inductance current by measuring only the input and output voltages of the converter. As described in Figure 4.4, the operation in stage 1 allows us to correctly estimate the value of $a_0(k)$ while stage 2 permits to estimate the initial value *b(k)* of the inductance current.

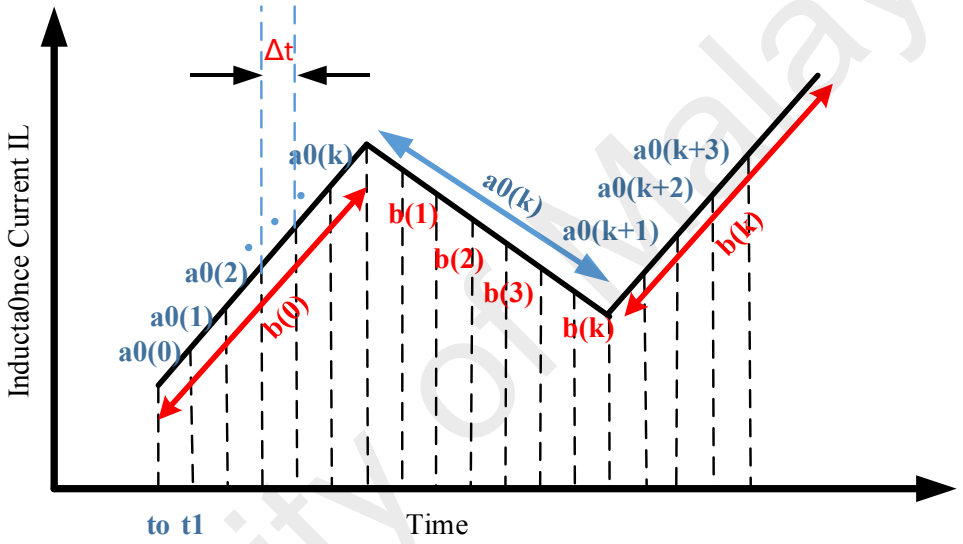


Figure 4-4: Process of estimating the inductance current

4.3.4 Boundary Control with Inductance Current Estimation

To remove the current's measurement in the boundary control of the converter using state-energy plane, we have to use a combination between the ON and OFF equation of the converter, stated in (4.66), with the estimated formula of the inductance current in equations (4.63) and (4.64). According to the boundary control the ON and OFF of the switches is performed as follows:

$$S_1(\tau)=\begin{cases}(Q1,Q2)=(1,0) \quad if \quad \sigma_+^{\,2}(\tau)=W(\tau)-W_{ref}(\tau)+k_1\left[i_L(\tau)-I_{ref}(\tau)\right]^2>0 \;\&\; i_L(\tau)>I_{ref}(\tau) \\ (Q1,Q2)=(1,1) \quad if \quad \sigma_-^{\,2}(\tau)=W(\tau)-W_{ref}(\tau)-k_2\left[i_L(\tau)-I_{ref}(\tau)\right]^2<0 \;\&\; i_L(\tau)<I_{ref}(\tau)\end{cases} \tag{4.66}$$

A general form of the control algorithm can be identified by the following steps:

1) If the converter is in the OFF state, goes to step (9)
2) Enable the ON mode of the converter
3) Use the equation (4.63) to estimate the inductance current
4) Calculate the parameter needed to apply the boundary control theory
5) Verify the condition $i_L(t) > I_{ref}$
6) If step (5) is satisfied, then check if

$$W(t) - W_{ref}(t) + k_1\left[i_L(t) - I_{ref}(t)\right]^2 > 0$$

7) If step (6) is satisfied, then generate the needed pulses to all switches
8) If one of the previous steps (5 and 6) is not satisfied, then goes to the OFF state.
9) Activate the OFF state of the converter.
10) Use equation (4.64) to estimate the inductance current
11) Calculate the parameter needed to apply the boundary control theory
12) Verify the condition $i_L(t) < I_{ref}$
13) If step (12) is satisfied, then check if

$$W(t) - W_{ref}(t) - k_2\left[i_L(t) - I_{ref}(t)\right]^2 < 0$$

14) If step (13) is satisfied, then generate the needed pulses to all switches.
15) If one of the previous steps (12 and 13) is not satisfied, then goes to step (2).

4.4 Implementation of Sensorless Boundary Control

The sensorless control of the DOBC can be generalized as described in the flowchart of Figure 4.4. According to the proposed method, the output voltages are measured, then a comparison between V_1 and V_2 is verified to enable either mode 1 and mode 2 or mode 1 and mode 3. After that, the calculation of the needed variables and verifying the switching surface S1 conditions will generate the desired switching pulses.

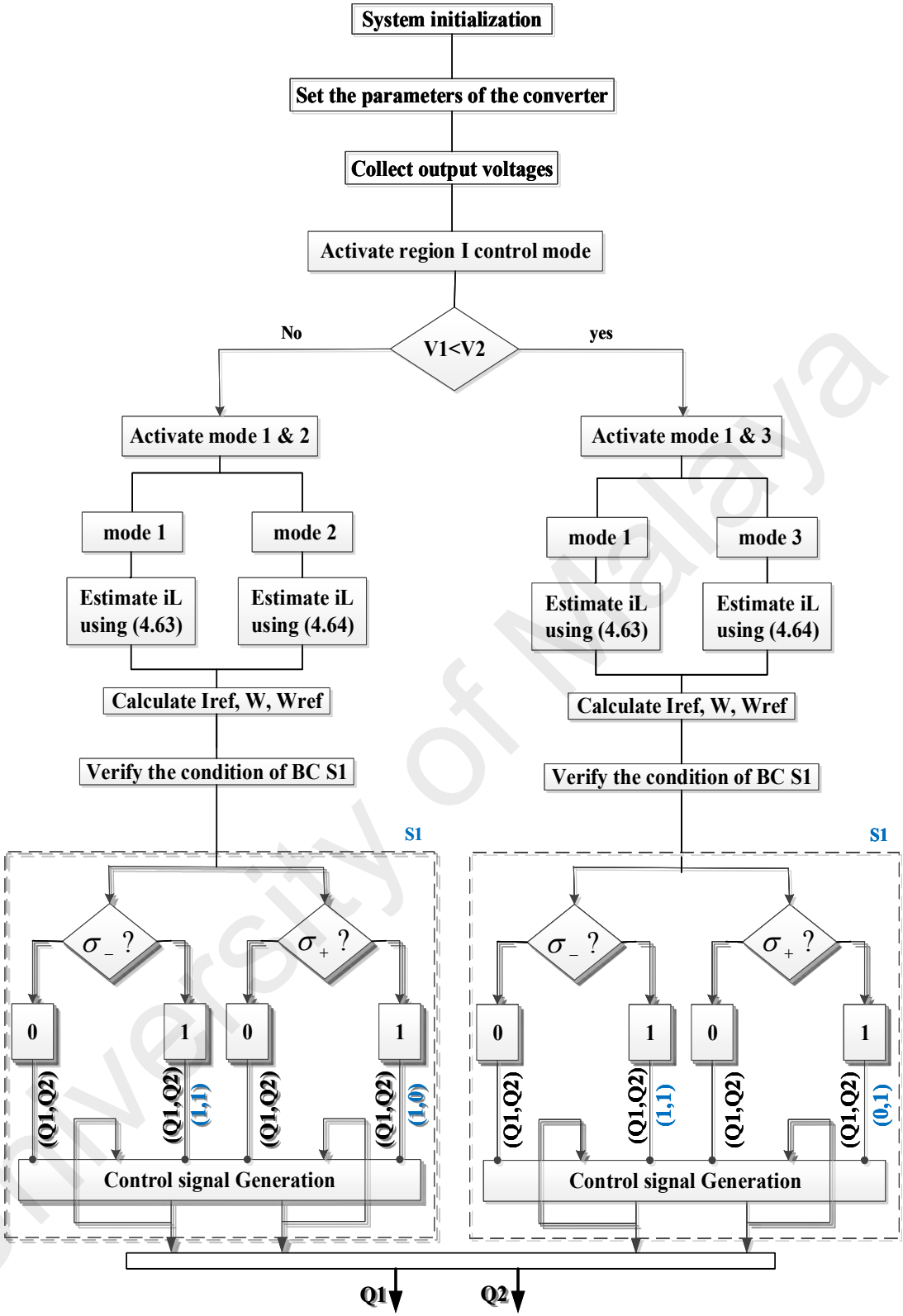


Figure 4-5: Flowchart of sensorless boundary control of the DOBC

4.5 Summary

Within this chapter a sensorless boundary control in the state-energy plane for the dual-output boost converter is presented. A deep analysis of the state space equations with the development of their solutions are carried out. An estimated model is proposed for the converter which help to identify the relation between the inductance current and the output voltages. Based on the region of control, a method to estimate the inductance current in the ON state (inductance current is increasing with time) and the OFF state (inductance current is decreasing with time) is proposed. Then the estimated currents are used to determine and satisfy the second-order switching surface criteria using state-energy plane. The proposed sensorless boundary control will preserve the good dynamic performance of the normal boundary control technique without using current sensors.

CHAPTER 5: RESULTS AND DISCUSSION

5.1 Introduction

In the previous two-chapters, a general approach to control the proposed three-level voltage source inverter has been presented. This chapter will discuss and verify the developed control methods by performing several simulations and testing processes. The control strategy has been tested under steady state and transient conditions to check the performance of the system. Moreover, experimental studies are performed on laboratory prototype which consists of a dual-output boost converter connected to a three-level voltage source inverter. The control of the dual-output boost converter is implemented on digital signal controller TMS320F2812 and the control of the three-level inverter is implemented on Altera FPGA DE2 board. Furthermore, a stability analysis of the system is presented.

5.2 Control Implementation of the Proposed Converter

Based on the description made in chapter 3, the control of the dual-output boost converter connected to a three-level inverter are implemented in TMS320F2812 and Altera FPGA DE2 board respectively. In the next section, a description of the process of control's implementation is presented.

5.2.1 Control implementation of the TLI

The control of the proposed three-level inverter is based on space vector modulation. Using Field-Programmable Gate Arrays (FPGA) to realize and implement SVPWM algorithm offers many advantages such as higher switching frequency, the execution of many functions at the same time, and simple design of the software using either schematic, VHDL programming or combination between them. An Altera DE2 board is

used for SVPWM implementation, a fixed-point arithmetic is adopted for calculation procedure by considering the processing speed, simplicity and flexibility of the circuit parameters. In order to insure an efficient way for implementing the three-level space vector modulation the following points have been taken in consideration:

- The circuit design is mixed between schematic and VHDL programming due to the fact that Quartus software from Altera offers some optimized functions such as PLL, counters, and comparators.
- The execution of some functions is simultaneously and some others are sequentially executed
- Fixed point arithmetic is adopted, the fractional part with other important parameters are accessible without changing inside the main program.

As shown in Figure 5.1, the top-level design of SVPWM consists of several functions that implement this algorithm. These functions can be defined as follows:

- **IntFreDiv:** it divides the internal frequency of ALTERA Cyclone II board to two main frequencies. One is chosen to be 9 kHz to process sector, triangle and duty cycle calculation, while the second is 900 kHz, to generate the switching sequences and dead time.
- **Ph_Vabc:** It generates a balanced three phase system with desired amplitude, in addition to a test circuit for 50 Hz frequency control.
- **SecTriDuty:** it projects the vector voltage V_{abc} to $\alpha\beta$ reference frame, then maps them using matrixes H1, H2 and H3, after that detects sector with only checking the sign of projection. In addition of that a reference transformation is made, and checking also the sign of these transformations will determine the triangle and the duty cycle. This process will be repeated for each sampling time of the V_{abc}

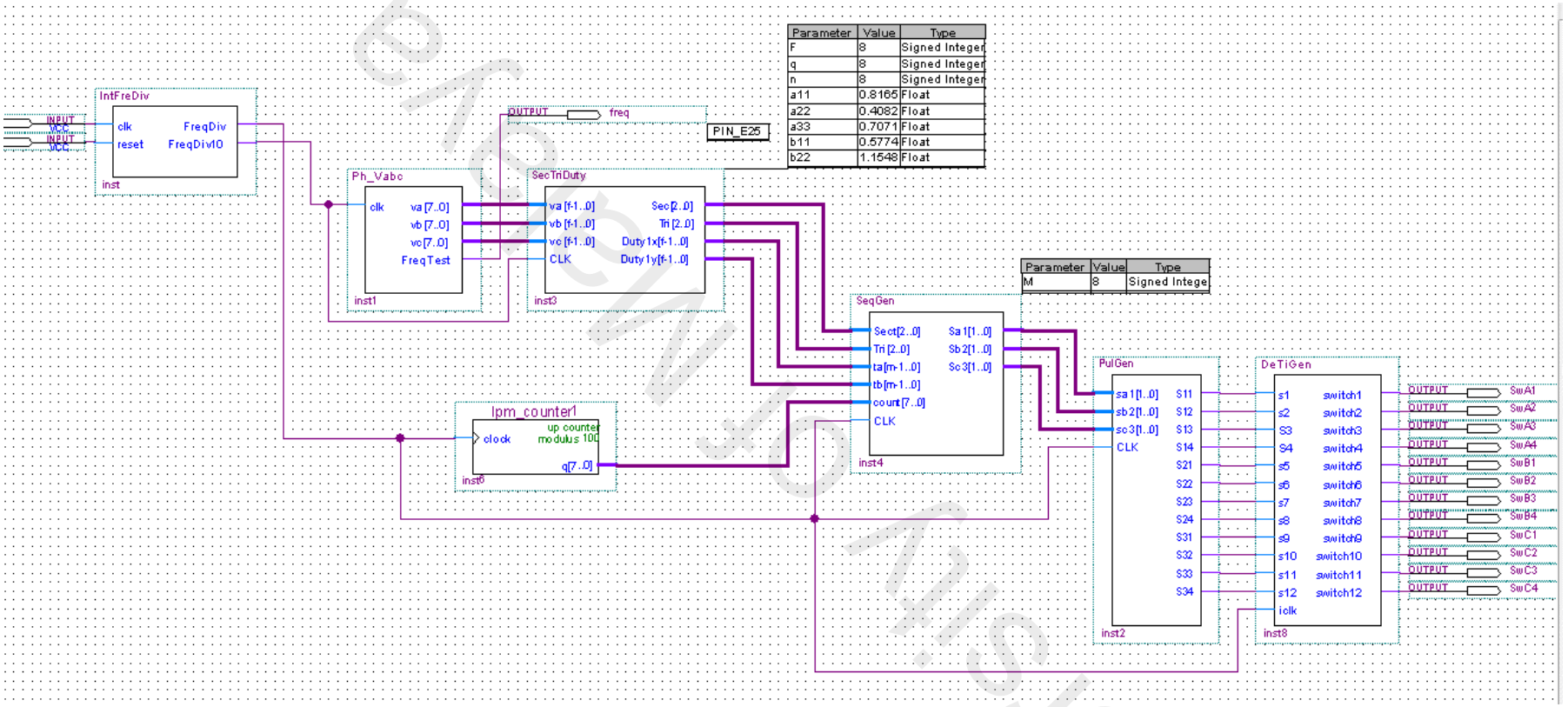


Figure 5-1: Three levels SVPWM implemented in Altera Cyclone II FPGA

- **SeqGen**: Based on the sector, triangle, and the duty cycle, this function selects the appropriate sequence defined by each triangle and generates the states 2, 1 or 0 for inverter's phases.
- **PulGen:** It generates the appropriate pulses for the proposed three-level inverter based on SeqGen's function results.
- **DeTiGen:** It generates the deadband related to switches located in the same inverter leg.

5.2.2 Algorithm Implementation for the DOBC

According to the previous study, it is clear that by controlling the proposed DC/DC converter, the DC-link of the three-level inverter can be regulated to the desired voltage level. Therefore, the proposed boost converter can address the capacitor voltage balancing in the new three-level inverter, which then will decrease the complexity of the inverter control strategy. The proposed control technique of the DC/DC converter is well described in chapter 3 where a boundary control based on second-order switching surface is adopted. As you can see in Figure 5.2, the implementation of this control technique needs two voltage sensors and three current sensors to obtain the desired parameters from the hardware. The capacitors voltages and the inductance current with the output current of each load are obtained to calculate the converter's energy, the converter's reference energy, and the inductance reference current. The results obtained will be evaluated by the second-order switching criteria which are defined by the switching state $S_1(t)$ if the converter work in region I or by the switching state $S_2(t)$ if the converter work in region II. The output pulses (Q1, Q2) will be generated as stated in Table 5.1.

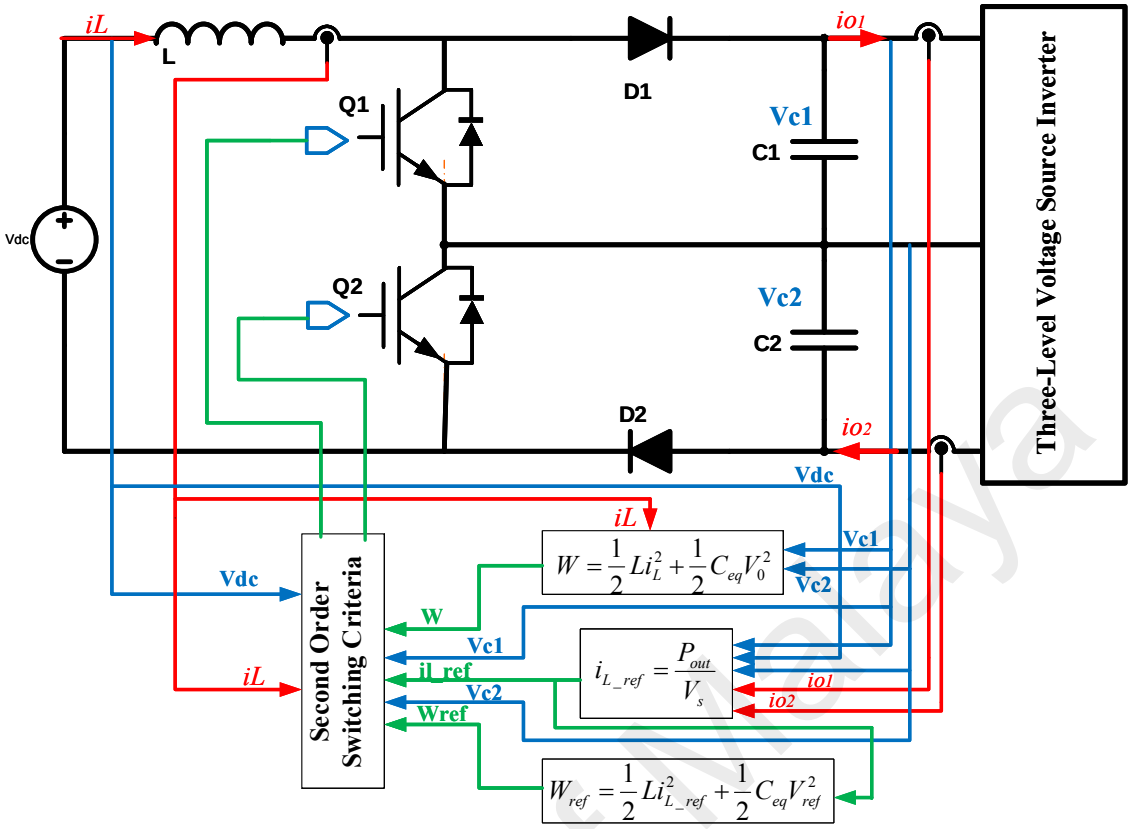


Figure 5-2: Proposed control of the proposed converter

$$S_1(t) = \begin{cases} (1,0)\ or\ (0,1) & if\ \ \sigma_+^2(t) = \Delta W(t) - k_2\left[i_L(t) - i_{L\_ref}(t)\right]^2 > 0\ \ \&\ \ i_L(t) > i_{L\_ref}(t) \\ (1,1) & if\ \ \sigma_-^2(t) = \Delta W(t) - k_1\left[i_L(t) - i_{L\_ref}(t)\right]^2 < 0\ \ \&\ \ i_L(t) < i_{L\_ref}(t) \end{cases} \quad (5.1)$$

$$S_2(t) = \begin{cases} (0,0) & if\ \ \sigma_+^2(t) = \Delta W(t) + k_3\left[i_L(t) - i_{L\_ref}(t)\right]^2 > 0\ \ \&\ \ i_L(t) > i_{L\_ref}(t) \\ (1,0)\ or\ (0,1) & if\ \ \sigma_-^2(t) = \Delta W(t) + k_2\left[i_L(t) - i_{L\_ref}(t)\right]^2 < 0\ \ \&\ \ i_L(t) < i_{L\_ref}(t) \end{cases} \quad (5.2)$$

Table 5-1: Switching state for (Q1, Q2)

	Flip Flop output	Converter working Mode	Q1	Q2
Region I	1	Mode 1	1	1
	0	Mode2	1	0
		Mode 3	0	1
Region II	0	Mode 4	0	0
	1	Mode 2	1	0
		Mode 3	0	1

As stated by the theory this control method will exhibit good dynamic response due to the fact that it makes the converter revert to the steady state in two switching actions under large signal disturbances. However, for the proposed configuration there are considerable numbers of sensors which really increase the cost of the converter. Therefore, an adaptation of a sensorless technique will be preferable. As explained in chapter 4, a proposition to a sensorless method is adopted and well explained. Figure 5.3 summary the proposed sensorless control technique where only the output voltages are sensed, then the region of control is detected, after that using the method of current predicting in the ON state and OFF states of the converter, the inductor current is obtained. The estimation current is obtained by calculating the desired parameters stated in equations (4.63) and (4.64), which are as follows:

$$a_0(k+1) = (1-\mu)a_0(k) + \mu\frac{1}{2\Delta t}\left(1 - \frac{v_2(k+1)}{v_2(k)}\right)$$

$$\omega_0(k+1) = \sqrt{(LC)^{-1} - a_0(k+1)^2}$$

For the ON state:

$$I(k+1) = I(k) + \frac{V_{dc}}{L}\Delta t$$

$$b(k+1) = b(k)$$

$$I_L(k+1) = I(k+1) + b(k+1)$$

For the OFF state:

$$I(k+1) = I(k) + \frac{V_{dc} - v_2(k)}{L}\Delta t$$

$$I_L(k+1) = I(k+1) + b(k)$$

$$C\frac{v_0(k+1) - v_2(k)}{\Delta t} + 2a_0(k)Cv_2(k) - I(k) \approx 0.5\omega_0(k+1)^2\, C(V_{dc} - v_2(k))\Delta t + b(k)$$

We have to mention here that the ON state is $(Q1, Q2) = (1, 1)$, and the OFF state is either $(Q1, Q2) = (1, 0)$ or $(Q1, Q2) = (0, 1)$. After obtaining the needed currents, the control technique of the converter will follow the same steps described previously such as calculating the converter energy, the reference current and the energy reference which will feed the second-order switching criteria to generate the desired pulses.

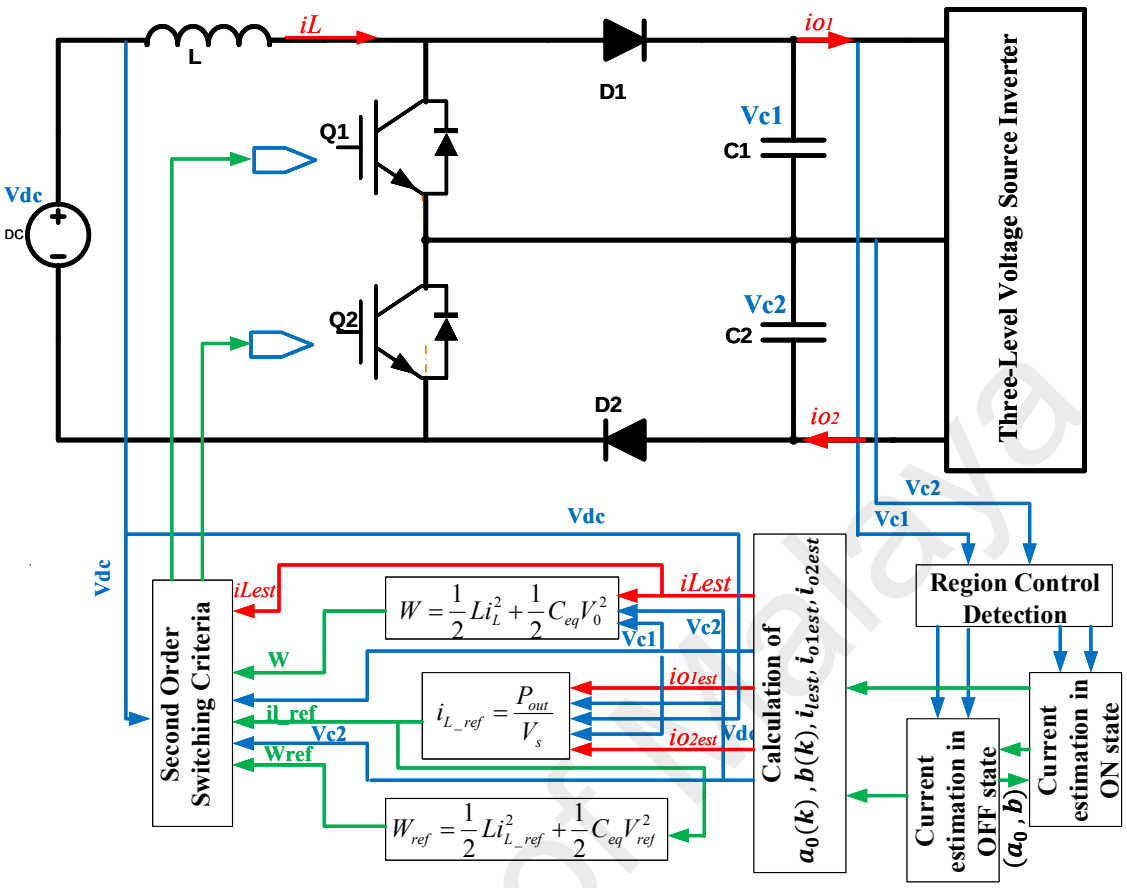


Figure 5-3: Sensorless boundary control using state energy plane

5.2.2.1 Program Structure of DOBC

The overall program structure that summarizes the control of the DOBC is shown in Figure 5.4. Once the program starts to run, the first task was to initialize the DSP Macros, then set the global variables such as the input voltage, inductance and capacitances values, and other parameters. The event manager module was initialized to define the sampling and switching frequency, which was determined by the period of the general-purpose timers. A GPIO function is set to enable the output pulses. The analog to digital conversion was set to be in the continuous conversion mode.

After the configuration of the DSP was complete, an interrupt was enabled to allow the main algorithm to run. The interrupt subroutine was executed every sampling period.

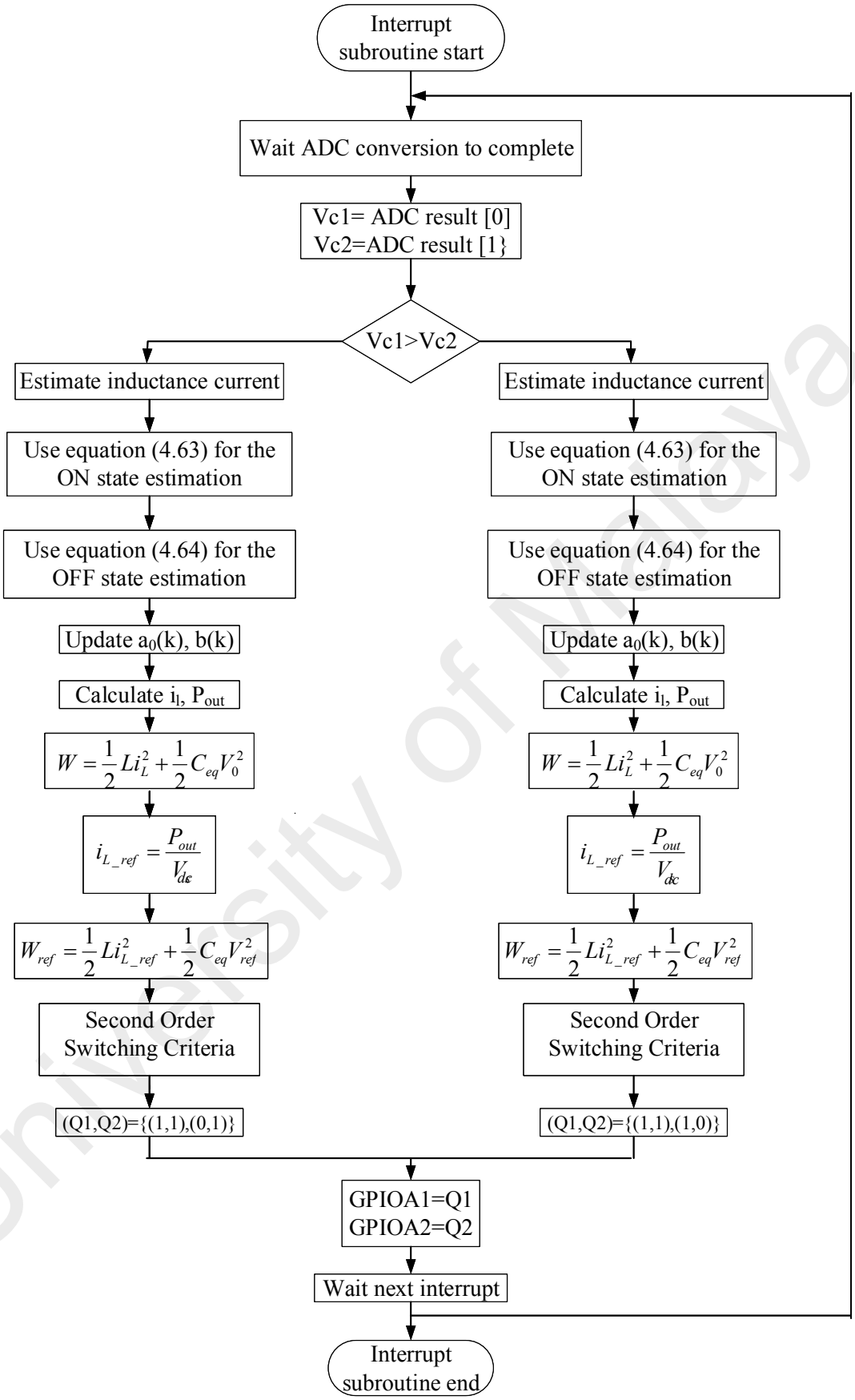
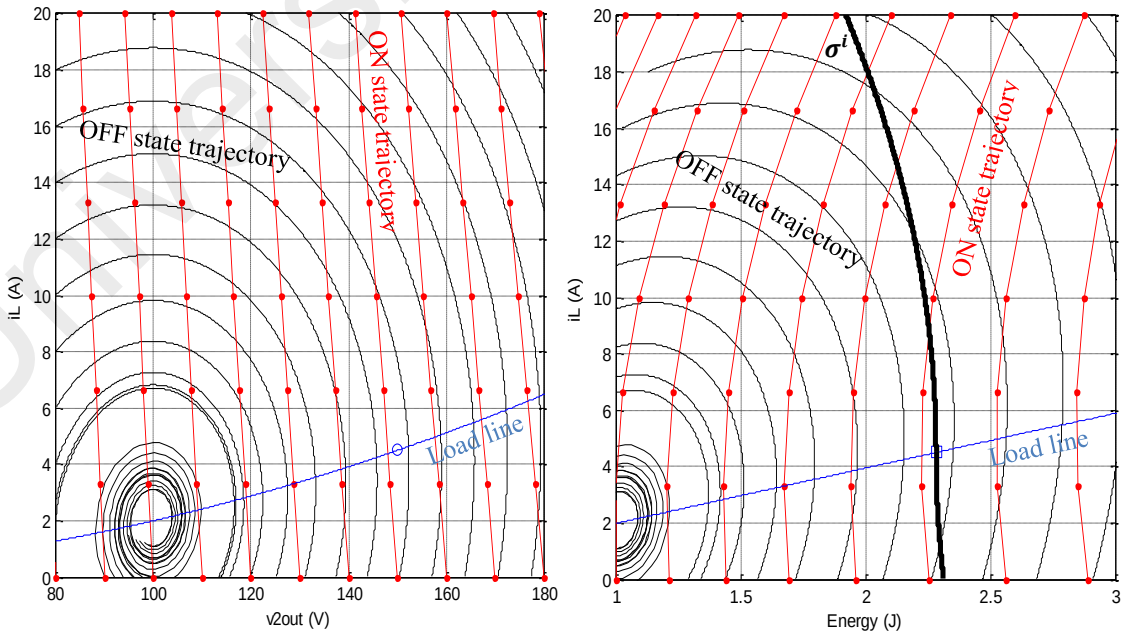


Figure 5-4: Sensorless current control implemented in TMS320F2812

It collects the value of voltages from the ADC results, then proceed with the calculation of current estimation parameters. Finally, a second-order switching criteria will be applied to generate the desired output pulses and updates the GPIO function output. The interrupt subroutine returned to the main program and waited for a request for the next interrupt to run the same process.

5.3 Simulation Results

Using Matlab software the proposed topology is simulated. The control algorithm is implemented following the description made in the previous sections. The DOBC is controlled in region I where the input voltage is set to be 100V and its total output voltage will be 300 V, hence each capacitor can handle a voltage level of 150 V. As the control of the DOBC is simplified to the control of two conventional boost converter, the state plane of the lower boost 1 (see Figure 4-3) and its modification to state-energy plane is displayed in Figure 5.5. The ON state trajectories are derived by putting (Q1, Q2) = (1, 1), while the OFF trajectories are derived by putting (Q1, Q2) = (1, 0).



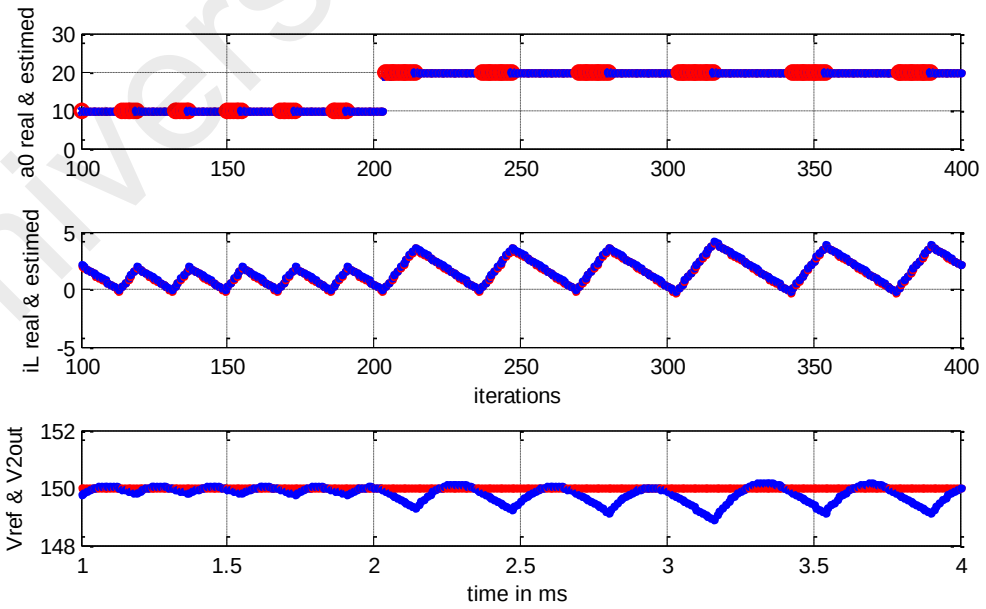
(a) State plane (i_l, v_2) (b) state-energy plane (i_l, w_2)

Figure 5-5: State trajectories on state plane and state-energy plane

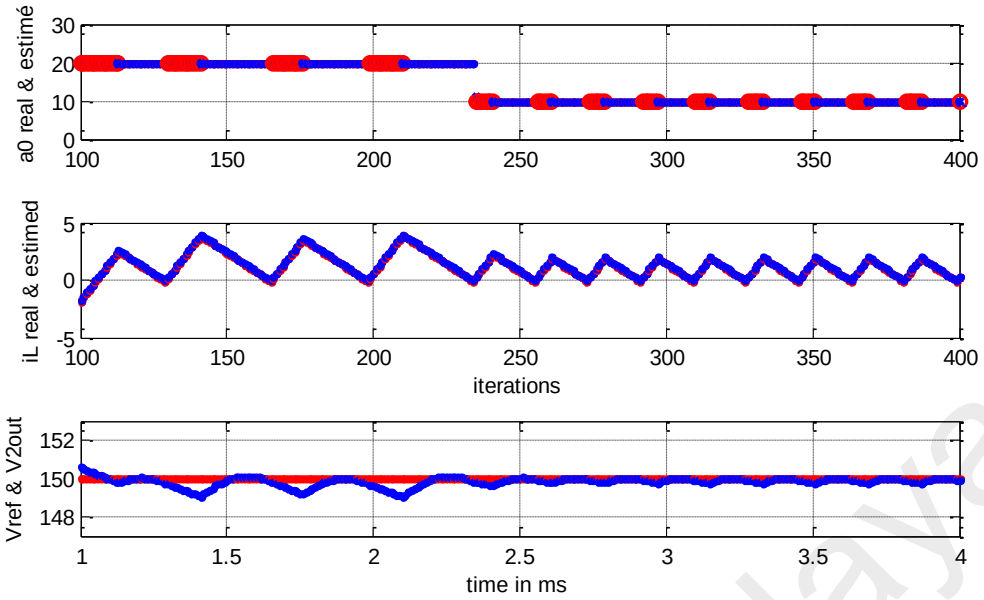
As stated by the theory, a sensorless boundary control on state-energy plane is applied with the parameters stated in Table 5.2. The simulation results of the control algorithm without using any current sensors is shown in Figure 5.6. Varying the resistance value from 250 Ω to 125 Ω and vice versa, the results show that the estimation values of $a_0(k)$ and the inductance current i_{L_est} are almost equal to the real one. Moreover, the output voltage of each capacitor follows its reference voltage with some differences in the ripple voltage value when the variation occurs. As consequence, the results obtained confirm the feasibility of the proposed estimation method.

Table 5-2: Component values of the DOBC

Parameter	value	parameter	value
v_{dc}	100 V	C	200 uF
v_{1_ref}	150 V	W	4.50 J
v_{2_ref}	150 V	ΔW	0
v_{0_ref}	300 V	k_1	1.5e-3
L	3 mH	k_2	3e-3
R_c	0.2 Ω	k_3	7.5e-4
Δt	50 uS	μ	0.9



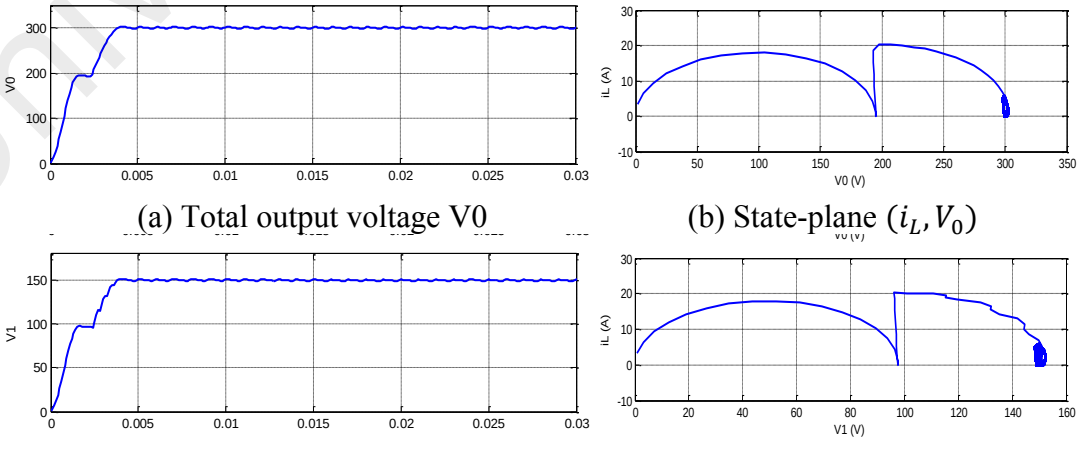
(a) Resistance variation from 250 Ω to 125 Ω



(b) Resistance variation from 125 Ω to 250 Ω

Figure 5-6: Sensorless control technique verification

On the other hand, at the start-up, the control algorithm attempts to reach the reference voltage (in our case is 300 V) rapidly by increasing the inductor current i_L at the beginning. This increase is necessary to reach the desired energy that boost the voltage to the steady state level. Then, the inductor current comes back to its normal value that kept the boost voltage to its desired output voltage. These variations can be seen in Figure 5.7 especially in the state plane and state-energy plane of the converter.

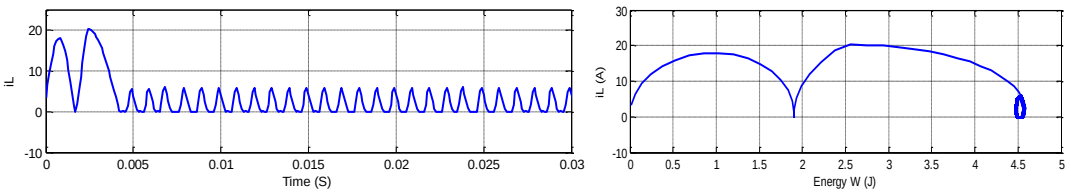


(a) Total output voltage V0

(b) State-plane (i_L, V_0)

(C) Output voltage V1

(d) State-plane (i_L, V_1)



(e) Inductor current of The DOBC (F) State-energy plane (i_L, W_0)

Figure 5-7: Steady state simulation results of the DOBC controlled in Region I

After obtaining a balanced DC-bus, the DOBC is connected to the proposed topology of a three-level voltage source inverter. A conventional three-level space vector modulation is used to control the TLI. The top-level design shown in Figure 5.1 for the three-level SVPWM is built, then compiled, optimized and synthesized with Quartus II 9.2 web edition software, which Altera offers for employing FPGAs.

In order to confirm and verify the algorithm implementation inside the FPGA, the Altera simulation tool is used. Each functional block from the design is verified trough the simulator tool and evaluated based on the results obtained from Matlab software. As an example, Figure 5.8 shows the output results of the sector and triangle identification function named SecTriDuty, while Figure 5.9 displays the switches' pulses output of each phase.

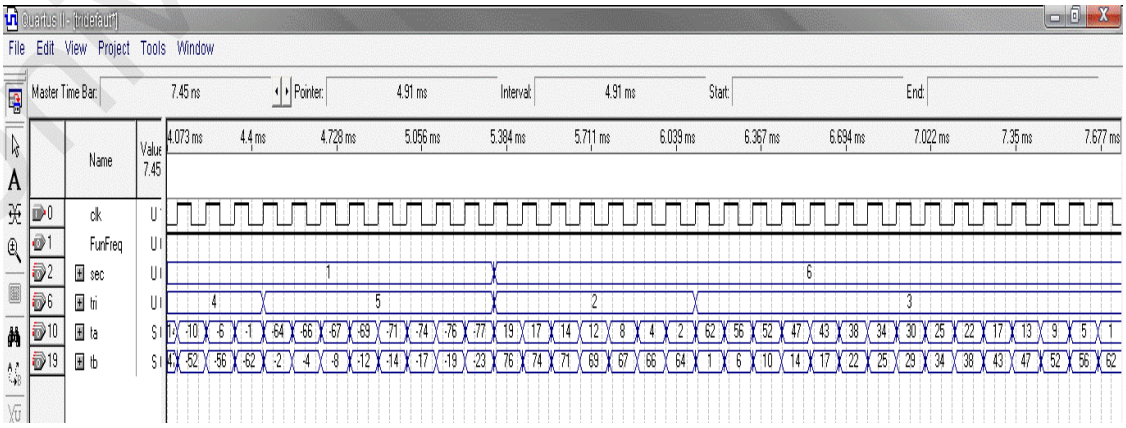


Figure 5-8: Sector and triangle determination using Quartus II software

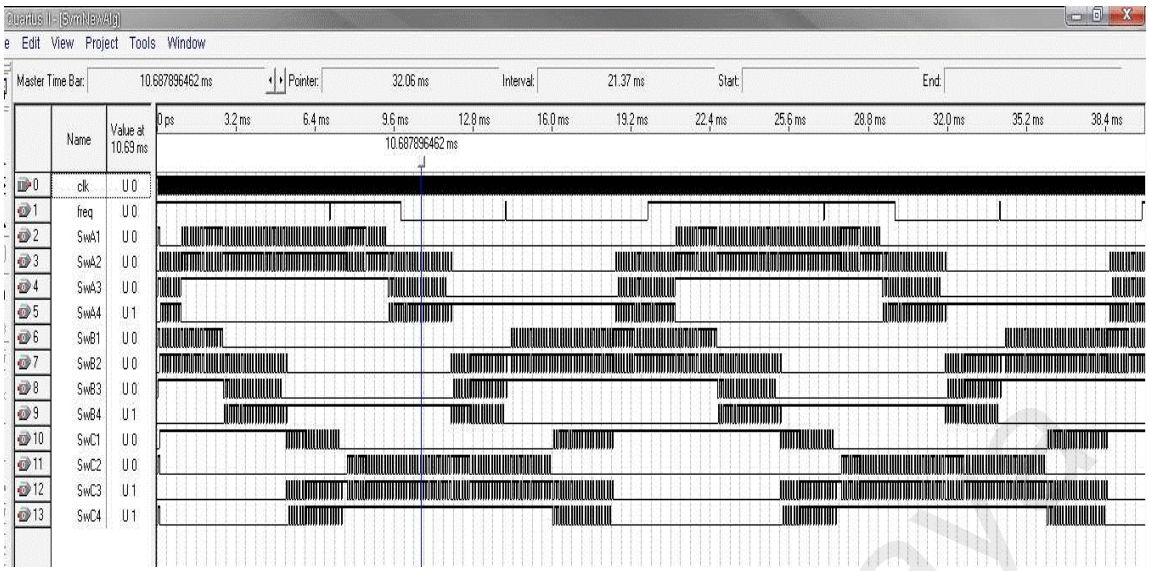


Figure 5-9 Switches' pulses output using Quartus II software

The hardware resource occupied by the developed three-level SVPWM in Cyclone II FPGA EP2C35F672C6 is summarised in Table 5.3. The SecTriDuty function uses more logical resources compared to other functions due to the fact that all calculations are made there. The algorithm uses only one PLL to generate the desired clock. Moreover, the actual time (Tco) used is equal to 4.628 ns which is lower than the FPGA clock period (50 ns).

Table 5-3: Three-level SVPWM resources summary

	Total Logic Elements	Total Register	Total memory bits	Emb. Multiplier 9-bit elements	Total PLLs
Total FPGA resource	33216	33216	483840	70	4
IntFreDiv	0.0008	0.0005	0	0	0.25
Ph_Vabc	0.0005	0.0002	0.0089	0	0
SecTriDuty	0.0669	0.0011	0	0.1143	0
SeqGen	0.0059	0.0002	0	0	0
PulGen	0.0004	0.0004	0	0	0
DeTiGen	0.0036	0.0025	0	0	0
svpwm	0.0807	0.005	0.0089	0.1143	0.25

On the other side, Simulation with Matlab/Simulink software is carried out. Figure 5.10 presents the generated pulses for phase A. these pulses are identical to the one obtained from Quartus simulator tool. Also, the steady state three-phase line voltages and phase voltages are presented in Figure 5.11 and Figure 5.12 respectively. The proposed configuration generates the desired output voltage as stated by the theory.

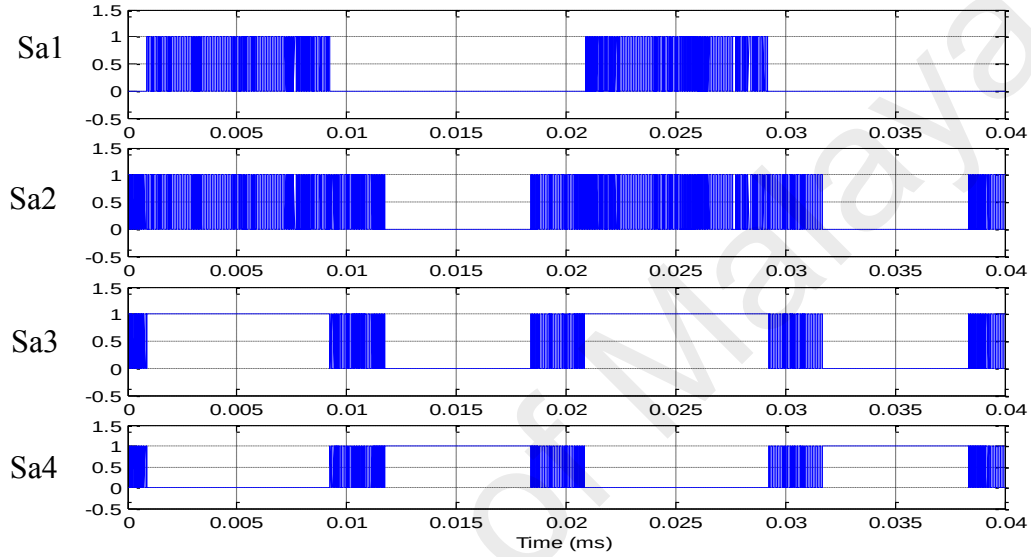


Figure 5-10: Phase A pulses for the three-level inverter

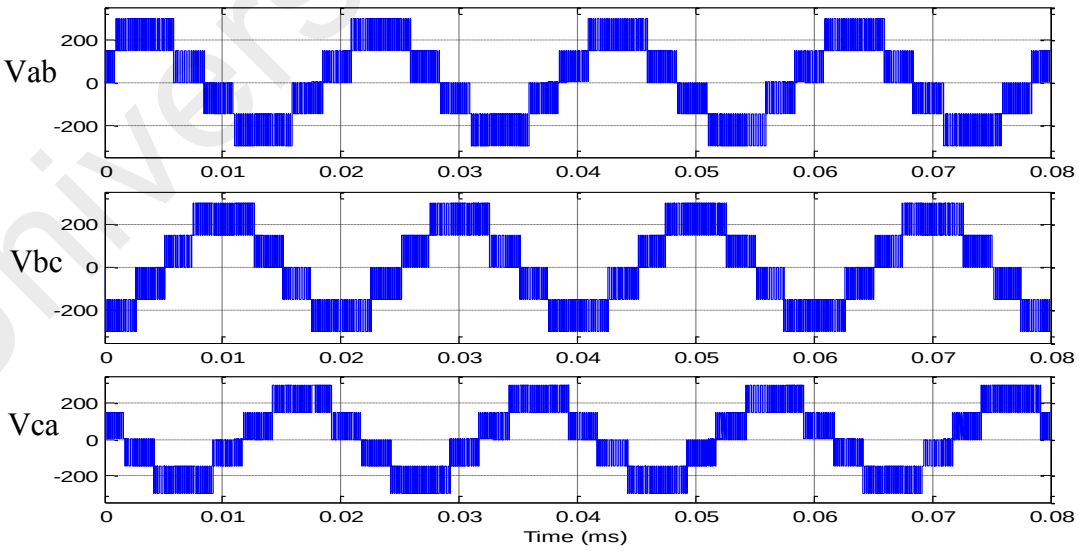


Figure 5-11: Three-level inverter line voltage output

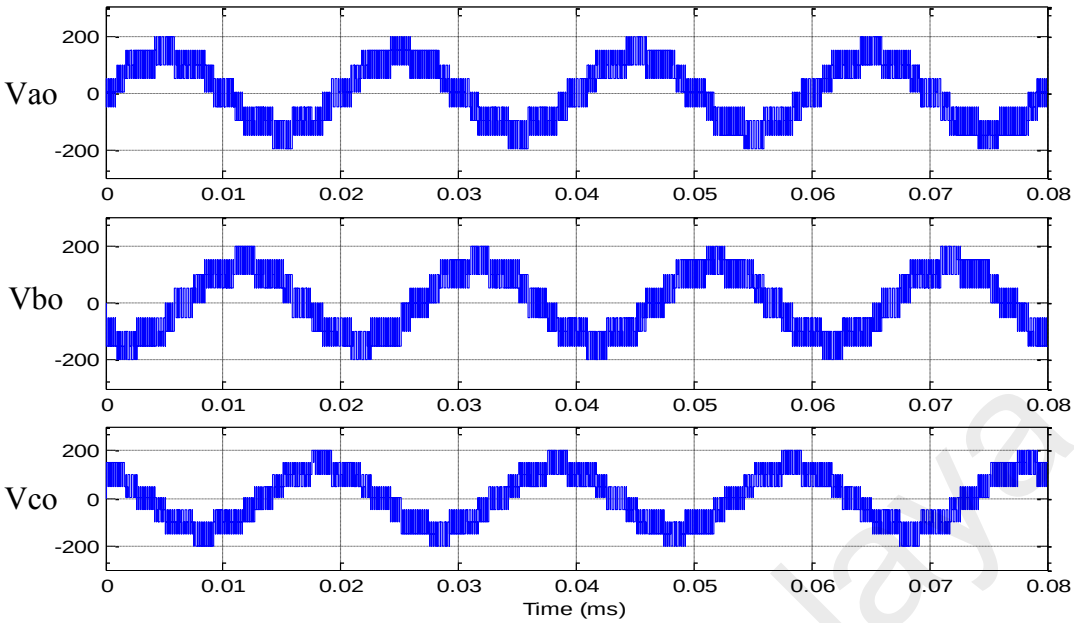


Figure 5-12: three-level inverter phase voltage output

5.4 Hardware results

A low power laboratory prototype shown in Figure 5.13 was built to evaluate the proposed topology performance. Part of the control algorithm is built in DSP TMS320F2812, and the other part in Altera FPGA DE2 board. The parameters of the hardware are similar to the one stated in Table 5.2.

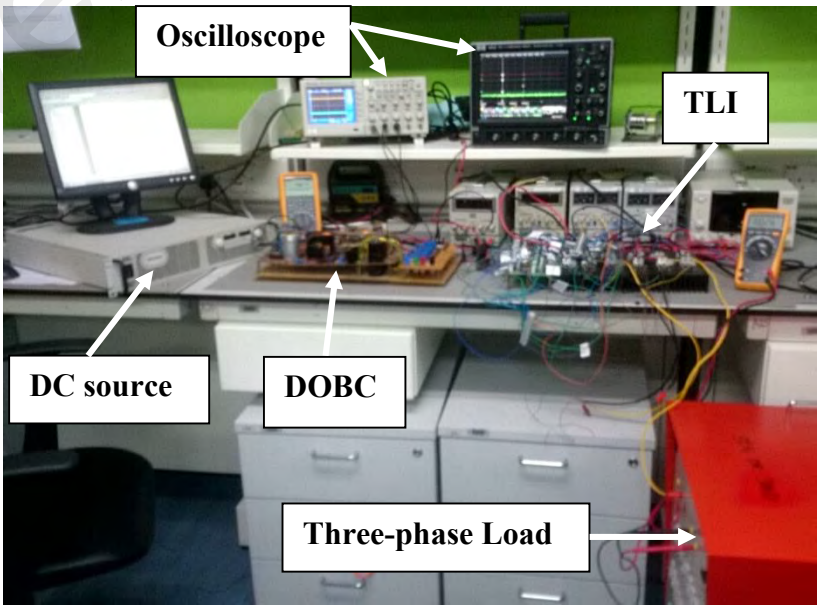


Figure 5-13: Laboratory prototype

To verify the working principle of the dual-output boost converter, the input voltage is varied from 100 V to 180 V. As consequence, the DOBC will satisfy the criteria of control in both regions. Figure 5.14 shows the results of the converter controlled in region I while Figure 5.15 displays the converter's results controlled in region II. The results of the input

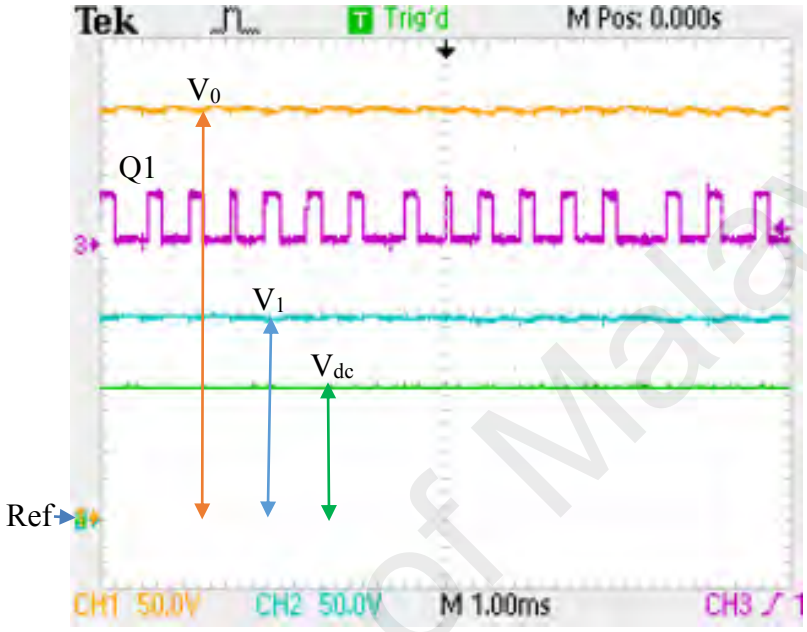


Figure 5-14: DOBC controlled in region I

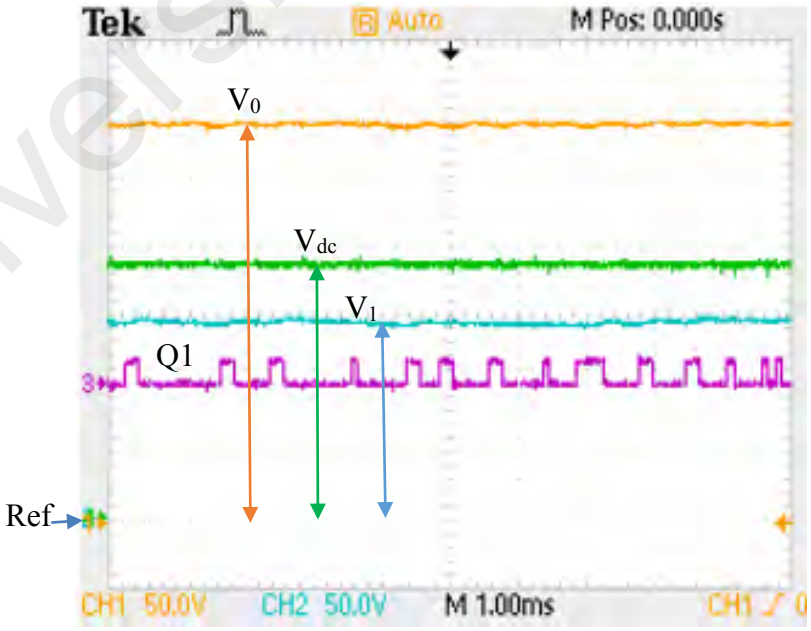


Figure 5-15: DOBC controlled in region II

voltage (V_{dc}), the total output voltage (Vo), the capacitor C1 voltage (V1), and the pulse of switch Q1 are collected in both control regions. The results obtained satisfy the theoretical study demonstrated in chapter 3. Moreover, the difference in pulse width and switching frequency is well observed in the two regions.

Once the control region is verified, the control of the DOBC is set to be in region I where the input voltage is less than the output voltage of each capacitor. Referring to Figure 5.16 that shows the converter start-up, it is clear that the converter reaches the steady state output voltage at almost 6 ms. The time taken is not only for the purpose of getting the desired energy to reach the steady state value but also related to the convergence of the sensorless algorithm parameters that estimate the inductance current.

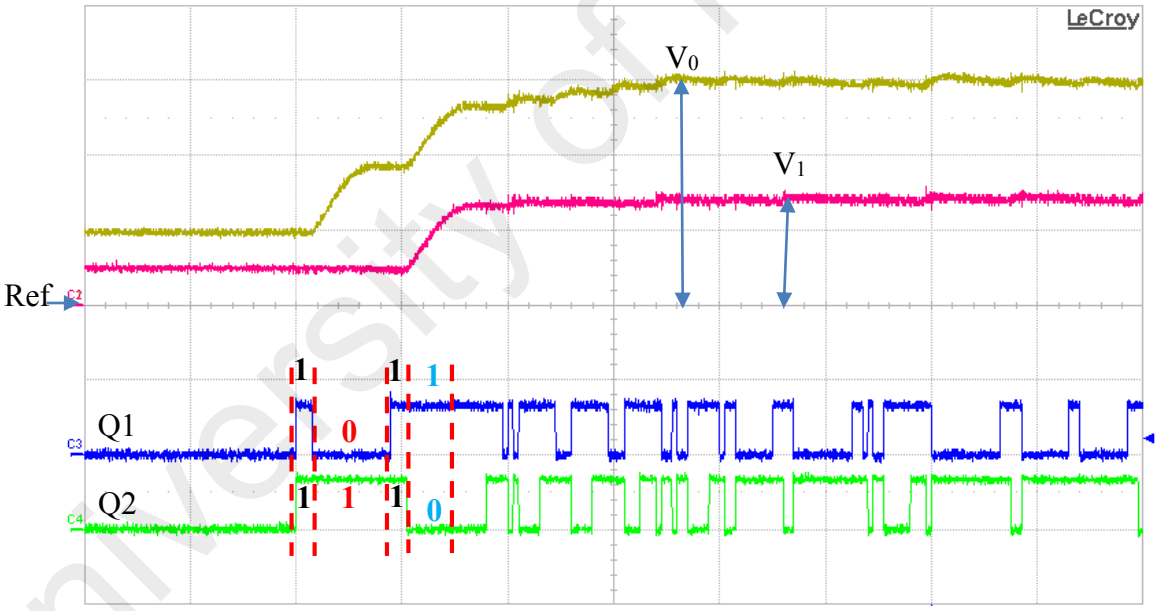


Figure 5-16: Dynamic behavior at the start-up of the converter

Here we have to mention that the control algorithm is modified slightly to include a condition to limit the rising of the inductance current to cope with the inductance limited current design. Also, to limit the switching frequency and to prevent the chattering in the output voltage, a hysteresis band Δw is added into the ideal switching surface σ^2 as stated in equation (3.17).

Looking for the output pulses, it can be seen that the switching signals satisfy the criteria of switching state in region I, as (Q1, Q2) starts with (1, 1), then moves to (0, 1), after that returns to (1, 1), then goes to (1, 0) and so on. Furthermore, there is an amelioration of the overshoot at the start-up behavior of the converter.

Regarding the three-level inverter, the explained space vector modulation is implemented in Cyclone II FPGA EP2C35F672C6. The switches' pulses are generated from the FPGA after allocating the pins using assignment editor. A programming file is generated after a successful compilation, then downloaded directly to FPGA via a JTAG using Quartus II programmer. The switches' pulses of phase A are shown in Figure 5.17. The generated pulses are similar to the one obtained by Simulink software. Besides, the DC-bus of the Three-level voltage source inverter with the inductance current are shown in Figure 5.18. The steady state results show a balanced DC side in accordance with the theoretical study. Using isolated differential probes (1000 V/ 15 MHZ) and putting a resistive load, the three-phase output voltage of the three-level inverter is shown in Figure 5.19. The results obtained are similar to the theoretical investigation.

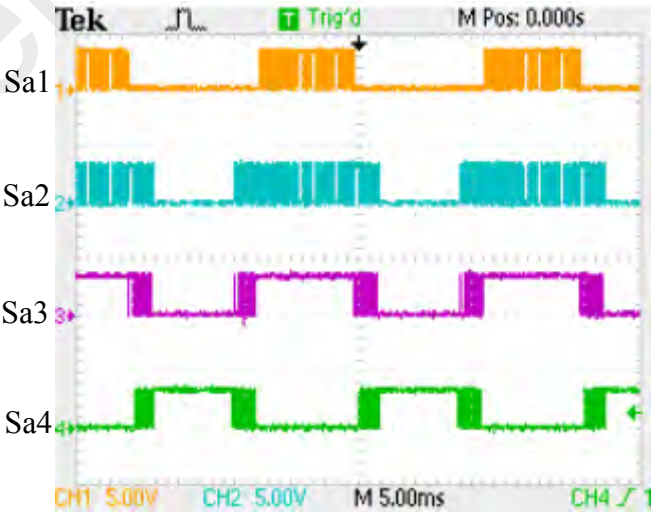


Figure 5-17: Phase A pulses from Altera FPGA

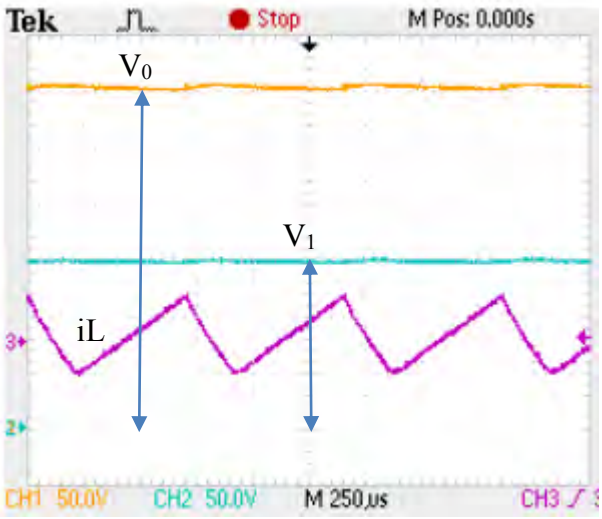


Figure 5-18: steady state results of the DC side

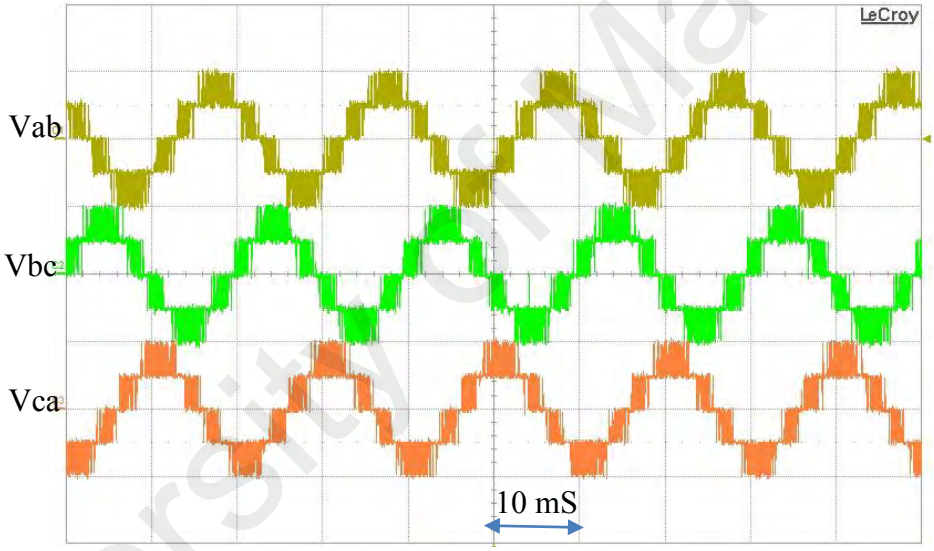
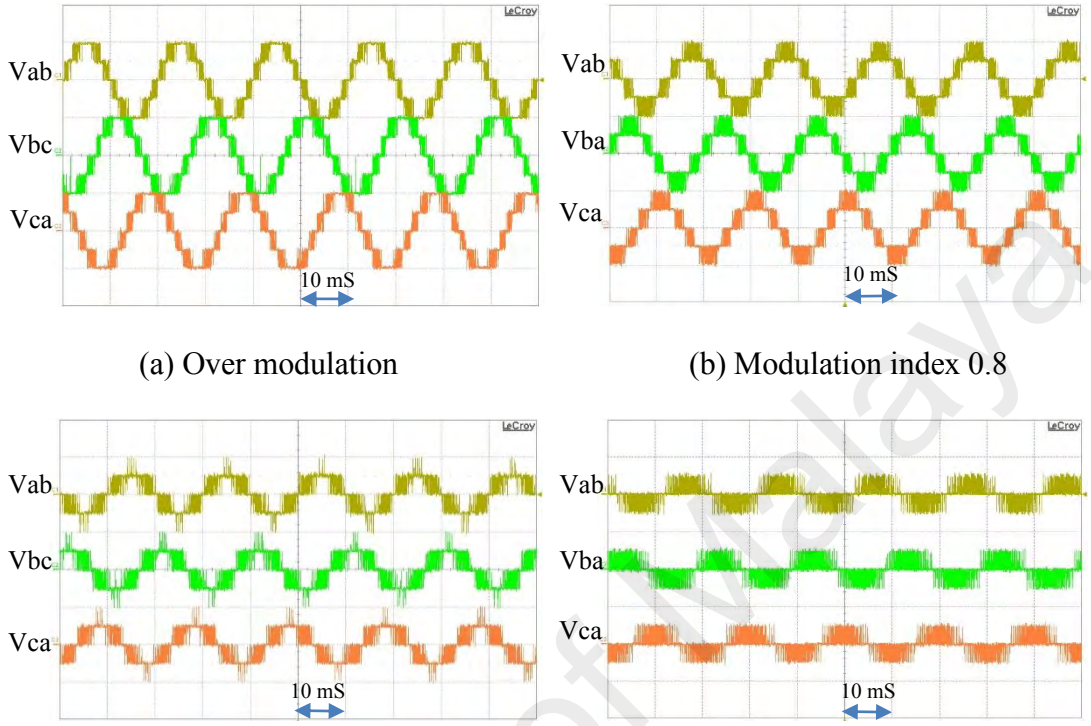


Figure 5-19: Steady state three-level line voltage output

5.4.1 TLI Results Analysis

To investigate the proposed three-level inverter, the output voltage with different modulation index are generated. This can be done by multiplying the stored sinewave with constant values and the results are shown in Figure 5.20. As it can be seen, when the modulation index is low, the reference voltage is situated on the lower hexagon; hence the inverter will generate only two-level of voltage. Increasing the modulation index will map the reference voltage between the upper and lower hexagon; hence the inverter will

generate three-level of voltage. If the reference voltage exceeds the upper hexagon, the inverter is in the over modulation region, so it will generate a distorted waveform.

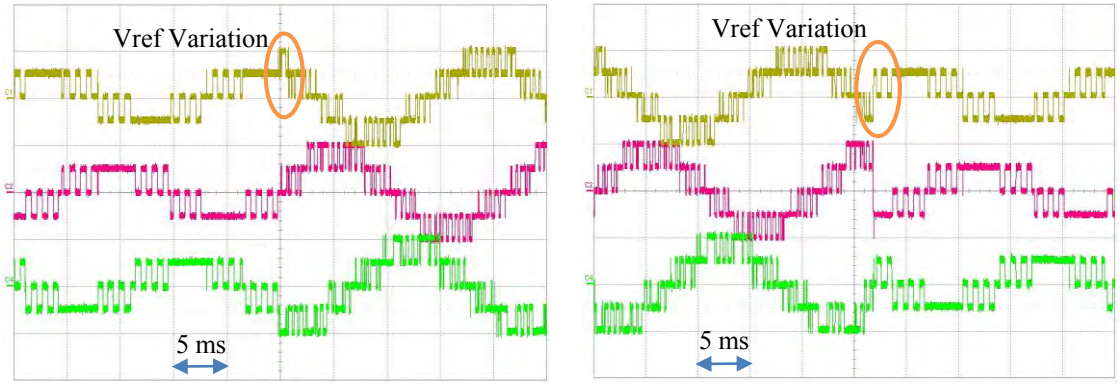


(a) Over modulation (b) Modulation index 0.8

(c) Modulation index 0.4 (d) Modulation index 0.2

Figure 5-20: Output line voltage with different modulations index

On the other side, variation of the voltage reference within the two hexagons is investigated. Referring to Figure 5.21, firstly the inverter is set to generate a two-level output voltage then a sudden increase of the reference voltage is carried out. The results show that the inverter reverts to three-level output voltage rapidly. In the same manner, the inverter is set to generate three-level output voltage, suddenly a decrease of the voltage reference to a vector within the small hexagon is carried out. The output voltage is quickly returned to two-level voltage. Thus, the proposed configuration controlled with the SVPWM algorithm accurately generates the desired output voltage with the desired frequency.



(a) Variation from two-level to three-level (b) Variation from three-level to two-level

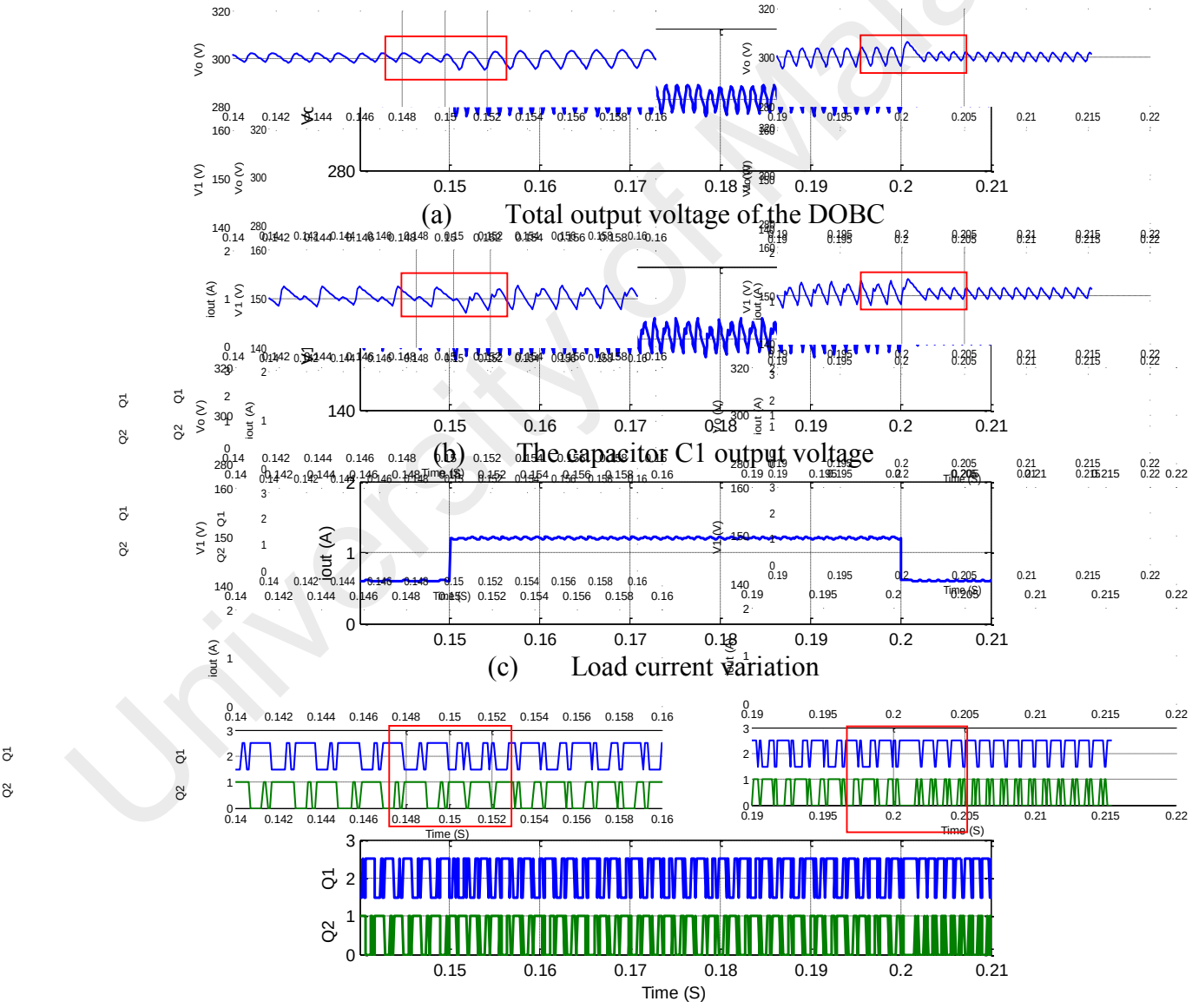
Figure 5-21: Inverter behavior under voltage reference change

5.5 Results Analysis of the DOBC

The main drawback in multilevel inverter is the DC- bus capacitor balancing, which can be achieved by two methods; one is adding external circuit, to maintain the desired level of voltage and the second is by changing the switching sequences or rearranging the time distribution of the redundant vectors. In this research work, an external circuit which is composed of a boost converter with two output voltage, called dual-output boost converter is connected with the proposed inverter topology. The converter is controlled to increase the output voltage and maintain a balanced output DC voltage, hence the inverter SVPWM sequence can be chosen separately without taking consideration of the capacitors charging state. Moreover, the non-symmetrical configuration seen between the upper and lower switches in one leg leads to a different charging and discharging time of the capacitors. This problem has to be solved by a fast and efficient control of the DOBC.

The sensorless boundary control technique with second-order switching surface formulated for a DOBC exhibits fast transient response; the output voltage is generally reverted to the steady state in two switching actions during large-signal disturbances. To verify the robustness of the control technique, a 50% load change is applied.

Simulation results shown in Figure 5.22 displays the transient response of the converter under sudden load variation. If the load current is increased the voltage output still follows the reference voltage with an increase in the ripple voltage. Likewise, if the load current is decreased, the output voltage is maintained to the reference voltage with reduction of ripple voltage. The time of reaching the steady state voltage when the load is increased is faster than the one when the load is decreased because the inductor current has enough energy at the moment of the current drop (load is increased) while it needs more energy when the current is increased (load is reduced).



(a) Total output voltage of the DOBC

(b) The capacitor C1 output voltage

(c) Load current variation

(d) The Generated pulses

Figure 5-22: Simulation results under 50% load change

Using the hardware prototype, the dynamic response due to 50% load change is tested. Referring to Figure 5.23, the decreasing or increasing of load didn't affect much the output voltage of the converter. The system has a fast-transient response, the desired output voltage recovers to steady state after a small switching time around 2 ms. The ripple voltage observed is balanced between 14 V to 8V respectively.

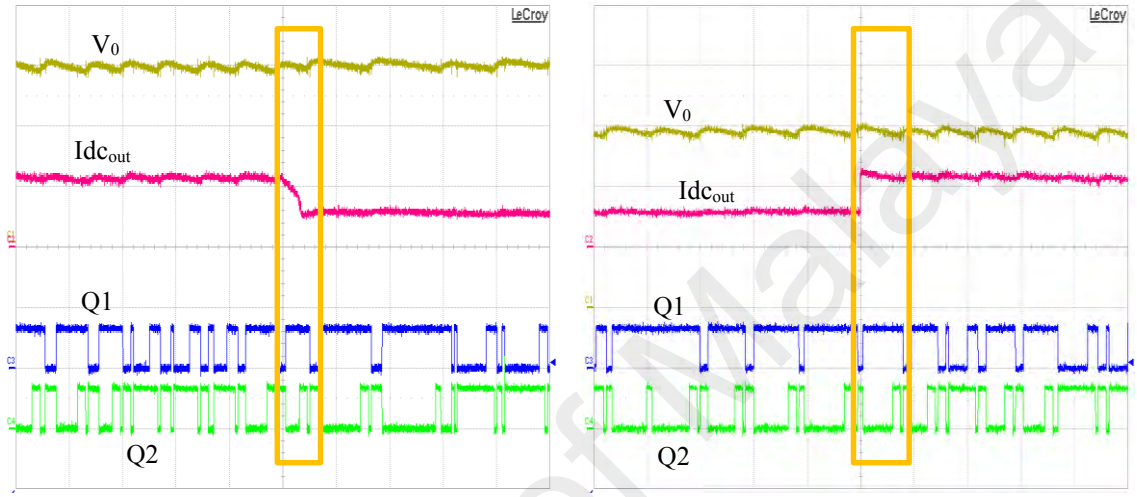


Figure 5-23: Dynamic response under 50% load change

(Vo: 100 V/div, Idc_{out}: 1 A/div, Q: 5 V/div, Time: 2ms/div)

Another important point is the effect of equivalent series resistance (ESR) on the capacitor voltage output. Practical capacitors are not ideal components, they can be treated as being ideal capacitors in series with a resistance. This resistance is defined as the equivalent series resistance (R_c). Therefore, the output voltage and the current in each capacitor can be defined as:

$$V1_{ESR} = V1_{act} + R_c i_{c1}$$

$$i_{c1} = i_L - i_{01} \tag{5.1}$$

$$V2_{ESR} = V2_{act} + R_c i_{c2}$$

$$i_{c2} = i_L - i_{02}$$

Therefore, considering the equivalent series resistance, the measured energy is defined as:

$$W_{ESR} = \frac{1}{2}Li_L^2 + \frac{1}{2}CV1_{ESR}^2 + \frac{1}{2}CV2_{ESR}^2 \tag{5.2}$$

Following the same procedure in steady state analysis (chapter 3), all the needed parameters can be easily calculated. An important parameter is the switching frequency, equation (5.3) determines the relation between the equivalent series resistance and the switching frequency when the converter is controlled in region I. Figure 5.24 illustrates the relation between the switching frequency and the hysteresis band Δw for different values of ESR. From the graph, it is clear that the switching frequency decreases as the equivalent series resistance increases.

$$f_s = \frac{V_{in}(V_0 - 2V_{in})}{2LV_0 \frac{\sqrt{\left((C_{eq}V_{ref}R_c)^2 + 4(C_{eq}V_{ref}R_c i_{L_{ref}} + 2\Delta w)(k_1 - k_2)\right)} - (C_{eq}V_{ref}R_c)}{(k_1 - k_2)}} \tag{5.3}$$

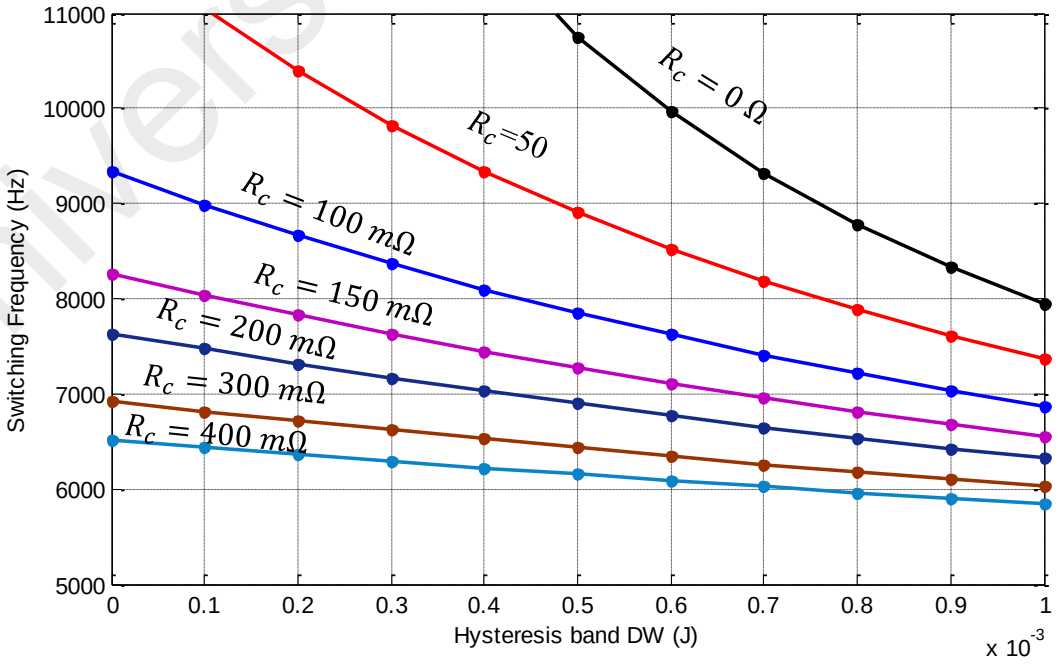


Figure 5-24: Switching frequency versus energy band ΔW

5.6 Comparative studies

In the determination of new inverter configurations, usually a comparison with other topologies has to be performed. As stated in this work, the proposed configuration is composed of a dual-output boost converter connected to a three-level voltage source inverter. A comparison between some three-phase three-level inverter topologies and the suggested topology with regards to power component requirements is presented in Table 5.4. The TLI uses less components due to its asymmetrical topologies. However, its lower switches (Sa4, Sb4, Sc4) have to withstand the full DC-bus voltage rather than half of it.

Table 5-4: Needed components in different three-level topologies

MLI Topology	Main Switches	diodes	DC bus	Flying capacitors	Total Element
NPC	12	6	2	0	20
FC	12	0	2	3	17
CHB	24	0	6	0	30
(Ceglia et al., 2006)	9	12	2	0	23
Proposed Topology	12	0	2	0	14

On the other side, voltage balancing is a key point for any new topology analysis. In this research work, the balancing capacitors is accomplished by a dual-output boost converter. This converter increases the input voltage and regulate the two capacitors output voltages that feed the new three-level inverter topology. In fact, the full configuration is well suitable for renewable energy, the DC/DC converters are utilised to adjust the low and unregulated output voltage of the renewable sources for the inverter DC side. The most utilized DC/DC converters that can feed other three-level inverter topologies are two separate conventional boost converters and two-interleaved boost

converter. Table 5.5 provides a comparison between a conventional boost converter, two-interleaved boost converter, and the dual-output boost converter. The inductor current ripple in dual-output boost converter is one fourth of that of the conventional one. For the same current ripple, the DOBC requires four times less inductance than the conventional boost converter. As consequence for the same input current, the inductor size in the DOBC has about one fourth the size of the inductor in boost converter.

Table 5-5: Comparison between some topologies of boost converter

Boost converter	**Interleaved boost converter**		**Dual-Output Boost converter**	
	D<0	D>0	Reg. I	Reg. II
Duty cycle				
$1-\frac{V_{dc}}{V_0}$	$1-\frac{V_{dc}}{V_0}$		$1-2\frac{V_{dc}}{V_0}$	$2-2\frac{V_{dc}}{V_0}$
Ripple current				
$\frac{V_{dc}D}{f_{sw}L}$	$\frac{(2V_{dc}-V_0)}{2Lf_{sw}}\ x\ (1-\frac{V_{dc}}{V_0})$	$\frac{V_{dc}(V_0-2V_{dc})}{2Lf_{sw}V_0}$	$\frac{V_{dc}(V_0-2V_{dc})}{V_0Lf_{sw}}$	$\frac{2V_{dc}(V_0-V_{dc})}{V_0Lf_{sw}}$
Condition for maximum ripple current				
$V_{dc}=0.5V_0$	$V_{dc}=0.75V_0$	$V_{dc}=0.25V_0$	$V_{dc}=0.25V_0$	$V_{dc}=0.75V_0$
Maximum ripple current				
$\frac{V_0}{4f_{sw}L}$	$\frac{V_0}{16f_{sw}L}$		$\frac{V_0}{16f_{sw}L}$	

On the other part, the more competitive counterpart of the DOBC is the two-interleaved boost converter. The input current ripple of the DOBC is the same as that of the two-interleaved boost converter. However, the two-interleaved boost converter has some weakness compared to the DOBC such as it needs two inductors, two controllers with a proper interleaving and current sharing, in addition that the switches have to withstand the full voltage. These drawbacks make the two-interleaved boost converter much less competitive than the DOBC for high power and/or high input voltage.

A related and supportive comparison can be made with the topology presented in (Nami et al., 2010) where a MOB is connected to a three-level NPC. Table 5.6 provides a comparison between the MOB and the DOBC used in this work. Both converter can boost and regulate the output voltage even if the connected load is not identical ($R_1 \neq R_2$). Both converters have the same number of elements, but all components in the DOBC have to withstand a voltage equal to (Vo/2), while for the MOB the upper diode have to withstand the full voltage. Besides that, and based on the switching state for each converter, the MOB can charge capacitor C1 only or C1 and C2 together, while the DOBC can charge each capacitor separately.

Table 5-6: Comparison between MOB and DOBC

Multi-output boost converter	Dual-output boost converter
Achieve a balanced DC-bus for the TLI even if the two loads are not identical Controlled with a constant switching frequency	Achieve a balanced DC-bus for the TLI even if the two loads are not identical. Controlled with variable switching frequency
Same components; one inductance, two switches, two diodes, and two capacitors. Not all components have the same voltage rating	Same components; one inductance, two switches, two diodes, and two capacitors. All components have the save voltage rating (Vo/2)
Based on switching state, can charge either C1 only or C1 and C2 together. Hence, the inductance current decreases with two different slopes (V_{dc}-V_1-V_2) and (V_{dc}-V_1) together	Based on the switching state, it can charge each capacitor alone. Hence the inductance current decreases with the same slope (V_{dc}-V_1) or (V_{dc}-V_2)
Suitable for renewable energy system	Suitable for renewable energy system

5.7 Summary

Within this chapter, the simulation and experimental results of the proposed topology are presented. The proposed topology is composed of a DOBC connected to a three-level inverter. The DOBC not only boosts the input voltage but also generates a balanced DC-bus voltage that fed the three-level inverter. Therefore, the imbalance problem in the TLI

could be avoided, which leads to a decrease in the complexity of the inverter control. A sensorless boundary control in the state-energy plane is developed and used to control the DOBC, while a three-level space vector modulation is chosen to control the TLI. Simulation and experimental results show that the DOBC generates an output voltage tightly regulated with a balanced voltage between the two capacitors. Under the sensorless control method, the converter exhibits fast transient response; the output voltage is generally reverted to the steady state in two switching actions during large-signal disturbances. In addition, the control of the TLI permits to generate the desired output voltage as the capacitor voltage imbalance problem is solved by the control method of the DOBC. Moreover, some comparisons with other topologies are performed. Results obtained show a good agreement between the theoretical prediction and experimental measurement results.

CHAPTER 6: CONCLUSION

6.1 Conclusion

Power electronic converters are employed in countless applications that require electrical energy conversion. With the recent fast evolution of energy systems and their associated complexity, power electronic topologies face ever increasing performance requirements. Multilevel converters topologies caught great attention in the field of high-power and high-voltage applications. Improving the transient performance of these converters results in a number of important advantages including reduction of passive components in the system, cost reduction, and increase in power density.

Small signal analysis is the traditional theory that has been used for a long time to design controllers for power electronics converters. Although it is useful in many cases, this theory fails to predict large-signal transients, leading to limited dynamic performance and establishing the need for new control schemes to improve the transient behavior. An alternative approach is to use the large signal state space geometric analysis which provides a more complete picture of the stability and performance for power electronic systems. Switching boundary control is a geometric approach, which uses a state-plane to analyze the switching boundary of the power electronic system. Its concept is based on utilizing and predicting the natural movement of the system state trajectories to derive a second-order switching surface. This control addresses the complete operation of the converter and does not differentiate between the start-up, the transient, and the steady state modes. The distinctive feature of this proposed method is that the converter has fast dynamic response and the system under this control can ideally settle at the steady point in two switching actions after large-signal disturbances.

The work presented in this thesis provides two important contributions; the first one is the proposition of new topology of three-level inverter fed by three-level boost converter, and the second is the application of high performance control technique for the boost converter to accomplish fast dynamic response during large-signal disturbance. As mentioned before, the proposed configuration consists of three-level boost converter that boost the input voltage and generate two balanced capacitors voltages that fed the three-level inverter topology. Therefore, the proposed boost converter can address the capacitor voltage balancing in the new three-level inverter, which will simplify the control of the inverter to simple space vector modulation to generate the desired voltage.

In this thesis, the control of the dual-output boost converter, known as three-level boost converter, is based on boundary control using second-order switching surface. The DOBC have the benefit to use four (4) times less inductance current ripple compared to a conventional boost converter. This gives the advantage of having low losses and reduced cost in addition to a balanced output voltage. The control algorithm also is flexible with input voltage variation which can be suitable for PV application. However due to the need of many sensor, a sensorless current method with a second-order switching surface is adopted. According to the proposed method, it is possible to predict the inductor's current of the converter by measuring only the input and output voltages of the converter. By using the obtained data, the energy error is expresses as a quadratic function of the current error by imposing the use of certain surface forms deduced from the four operation modes of the converter. These switching surfaces pass through the operating point (i_{L_ref}, W_{ref}), which will lead to the generation of the desired pulses.

The theoretical and practical investigations of the proposed configuration show the following points:

1) The proposed estimation method for the inductance current can successfully follow and predict the actual value of the current. Two parameters $(a_0(k), b(k))$ are introduced to estimate it. The operation in the ON state allows to estimate correctly the value of $(a_0(k))$, whereas The OFF state makes it possible to estimate the initial value $(b(k))$ of the inductor's current.
2) Development of second order switching surface based on state energy plane for the three-level boost converter.
3) Formulation of new control technique by combining the sensorless current control method and the second order switching surface.
4) The DOBC will exhibit fast dynamic response if the switching surface is chosen to be along the boundary of the reflective and refractive regions. The choice of the coefficients (k_1, k_2, k_3) values will manage the system stability of the converter.
5) The entire control algorithm developed for the DOBC is implemented in a Texas Instrument digital signal processor eZdsp^{TM} F2812 to overcome the complexity of the control circuit in analogue configuration.
6) The control technique for the three-level inverter is based on a three-level space vector modulation implemented in Altera Cyclone II FPGA EP2C35F672C6.
7) Even the real-time implementation is different from the simulation; the steady state results of the capacitor voltages, the inductance current and the three-level inverter output obtained in simulation and hardware verification are almost the same.
8) The DOBC is controlled in region I. when it is tested for 50% sudden load change, the results show that the system can recover to steady state in a short time with an augmentation or reduction of ripple voltage from 8V to 14 v and vice versa. Also with load change the pulses width also change to cope with the new reference current. The converter reaches the steady state within almost two switching actions.

9) Beside it fast transient response the control using second-order switching has improved the overshoot at the start-up.

6.2 Author's Contributions

The contribution of the presented research work can be viewed from different aspects namely the three-level converter topology and its control method technique. The important contribution of this thesis can be identified as follows:

1) Extend the boundary control technique using second-order switching surface in the state energy plane to control a three-level boost converter.
2) Develop the concept of sensorless boundary control using second-order switching surface in the state energy plane.
3) Study the steady state and large signal analysis for the proposed three-level converter.
4) Propose a new topology for three-level voltage source inverter.
5) Implementation of the sensorless boundary control technique in DSP TMS320F2812 and the developed space vector modulation in Altera FPGA DE2 board.
6) The feasibility of the proposed control strategy was confirmed using computer simulation and experimental work obtained from a prototype converter.

6.3 Area of Future Work

Although the study objectives have been achieved as highlighted in this work contributions, several issues have been detected and are listed here as possibly upgrading for future work in this area:

1) Extend the study of boundary control technique to high order switching surface to analyze the dynamic response of the system.
2) Extend the boundary control method with second order switching surface to control three-phase three-level inverter. Even the control here will be more complex but using a discontinuous pulse width modulation will reduce the complexity of the control algorithm to only controlling two phase three-level buck converter.
3) Due to its topology, the proposed configuration is well suitable for renewable energy systems such as PV and wind turbine systems, the DC/DC converters are utilized to adjust the low and unregulated output voltage of the renewable sources for the inverter DC side. For that future work can investigate the inclusion of maximum power point tracking in the formulation of the second-order switching surface.
4) Boundary control technique is a powerful control tool that can be employed to control any possible power converter. So, benefiting from the insight gained from the analysis of existing converters, new configuration and topologies can apply this control technique.

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2) T. Messikh, Nasrudin Abd. Rahim, Saad Mekhilef "A sensorless Boundary control of Dual-Output boost converter using state-energy plane" under review IEEE power electronics
3) T. Messikh, Nasrudin Abd. Rahim, Saad Mekhilef "Control strategy of a dual output boost converter connected to three-level inverter" under review Turkish Journal of Electrical Engineering & Computer Science.
4) MD. Mubashwar Hasan, Saad Mekhilef, Mahrous Ahmed, Tarek Messikh "Three-phase multilevel inverter with high value of resolution per switch employing a space vector modulation control scheme" Turk J Elec Eng & Comp Sci, 24, (2016), pages 1993-2009.