EFFECT OF OXIDATION TEMPERATURE ON THE THIN FILM SAMARIUM (III) OXIDE GROWTH ON GERMANIUM SUBSTRATE

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ABSTRACT

Searching for high-κ gate oxide has been an important task in the semiconductor industry for further downscaling. In this study, pure samarium (Sm) metal was first sputtered on germanium (Ge) substrate, and then proceeded to thermal oxidation for 15 minutes at varying oxidation temperatures of 300°C, 400°C, 500°C, 600°C and 700°C. The oxidized samples were then characterized by means of X-ray diffraction spectroscopy (XRD) and Fourier transform infrared (FT-IR) spectroscopy. According to the XRD results, the intensity of Sm_2O_3 phase recorded the highest value at 500°C among the experimental oxidation temperatures, and the interfacial layer compound, $Sm_2Ge_2O_7$ was observed to exhibit the highest peak intensity at 300°C and decreases as the oxidation temperature increases. On the other hand, the intensity of GeO_2 phase was observed to increase with the oxidation temperature, and showed the highest value at 700°C. Besides, a rapid increment in the amount of GeO_2 phase grown was noticed starting from 600°C, and a relatively huge quantity of GeO_2 is determined at 700°C. From Debye-Scherrer equation, the crystallite size first increases from 300°C and reaches a peak at 400°C, then decreases afterwards. Besides, the crystallite size and microstrain obtained through Williamson-Hall (W-H) analysis were observed to exhibit a decreasing trend from 600°C to 700°C for GeO_2 phase. The FT-IR results give information on the existence of the Sm-O and Ge-O bonds in the resulting films. By peak matching approach, Sm-O bonds were detected in 300°C, 400°C, 500°C and 600°C samples, showing the highest intensity at 500°C, while Ge-O bonds were also detected in all samples and read the highest intensity at 700°C. Both of the characterization analyses suggest that 500°C would be the optimum oxidation temperature to grow Sm_2O_3 on Ge substrate.

ABSTRAK

Pencarian lapisan oksida κ yang tinggi merupakan tugas yang penting dalam industri semikonduktor untuk pengurangan saiz yang selanjutnya. Dalam kajian ini, logam samarium (Sm) tulen mula-mula dipancarkan pada substrat germanium (Ge), dan kemudian meneruskan pengoksidaan haba selama 15 minit pada suhu pengoksidaan yang berbeza, iaitu 300°C, 400°C, 500°C, 600°C dan 700°C . Sampel yang teroksidasi telah dicirikan dengan cara spektroskopi difraksi sinar X (XRD) dan spektroskopi inframerah Fourier (FT-IR). Menurut keputusan XRD, intensiti fasa Sm_2O_3 mencatatkan nilai tertinggi pada suhu 500°C di antara suhu pengoksidaan eksperimen dan sebatian lapisan interfacial, $Sm_2Ge_2O_7$ diperhatikan menunjukkan keamatan puncak tertinggi pada suhu 300°C dan menunjukkan penurunan apabila suhu pengoksidaan dinaikan. Sebaliknya, intensiti fasa GeO_2 diperhatikan meningkat dengan suhu pengoksidaan, dan menunjukkan nilai tertinggi pada 700°C. Selain itu, peningkatan pesat dalam jumlah fasa GeO_2 yang dikembangkan diperhatikan bermula dari 600°C, dan kuantiti GeO_2 yang agak besar ditemui pada 700°C. Saiz kristal bermula meningkat dari 300°C dan mencapai puncak pada 400°C, dan menurun selepas itu. Selain itu, saiz kristal dan ketegangan mikro yang diperoleh melalui analisis W-H diperhatikan menunjukkan aliran menurun dari 600°C hingga 700°C untuk fasa GeO_2. Keputusan FT-IR memberikan maklumat mengenai kewujudan ikatan Sm-O dan Ge-O dalam filem-filem yang dihasilkan. Dengan pendekatan padanan puncak, ikatan Sm-O dikesan dalam 300°C, 400°C, 500°C dan 600°C, menunjukkan keamatan tertinggi pada 500°C, manakala ikatan Ge-O juga dikesan dalam semua sampel dan membaca intensiti tertinggi pada 700°C. Kedua-dua analisis pencirian menunjukkan bahawa 500°C adalah suhu pengoksidaan yang optimum untuk mengembangkan Sm_2O_3 pada substrat Ge.

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I would like to dedicate this research work to God, my parents and my supervisor.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS AND ABBREVIATIONS

κ	:	Dielectric constant
ε_0	:	Absolute permittivity (8.854 pF/m or pC/V.m)
ε	:	Microstrain
λ	:	Wavelength (nm)
β	:	Peak broadening
β_D	:	Peak broadening due to crystallite size
β_ε	:	Peak broadening due to microstrain
θ	:	Diffraction angle (°)
μ_e	:	Electron mobility ($cm^2\ V^{-1}\ s^{-1}$)
μ_h	:	Hole mobility ($cm^2\ V^{-1}\ s^{-1}$)
A	:	Area of oxide layer (cm^2)
a	:	Lattice constant (nm or Å)
C	:	Capacitance (pF)
D	:	Crystallite size
D_{it}	:	Interface trap density ($eV^{-1}\ cm^{-2}$)
d	:	Interplanar spacing (nm)
E_g	:	Bandgap energy (eV)
h, k, l	:	Miller indices
J_g	:	Leakage current density ($A\ cm^{-2}$)
K	:	Shape factor
n	:	Integer (1, 2, 3…)
t	:	Oxide thickness
ALD	:	Atomic layer deposition

ATR	:	Attenuated total reflection
CMOS	:	Complementary metal oxide semiconductor
CVD	:	Chemical vapor deposition
EOT	:	Equivalent oxide thickness
FT-IR	:	Fourier transform-infrared spectrometry
FWHM	:	Full width half maximum
IC	:	Integrated circuit
MOCVD	:	Metal organic chemical vapor deposition
MOS	:	Metal oxide semiconductor
MOSFET	:	Metal oxide semiconductor field effect transistor
PECVD	:	Plasma enhanced chemical vapor deposition
PLD	:	Pulsed laser deposition
PVD	:	Physical vapor deposition
REO	:	Rare earth oxide
RF	:	Radio frequency
T_m	:	Melting temperature (°C)
TEM	:	Transmission electron microscopy
TMO	:	Transition metal oxide
VFB	:	Valence flatband
W-H	:	Williamson-Hall method
XPS	:	X-ray photoelectron spectroscopy
XRD	:	X-ray diffraction/diffractometer

CHAPTER 1: INTRODUCTION

1.1 Background

In the era of advanced technologies, electronic semiconductor devices play a vital role in human daily life and they had become the relevant tools for the mankind to carry out their daily activities. Portable devices like smart phones and tablets, displays, detectors, and photonics devices require high end semiconductor technologies in order to work in a more efficient way. For the intention to have a more efficient electronic device, researchers are focusing on the performance aspects such as nano-scale size (Cui & Lieber, 2001; Matsui, 2005), low cost (Habas, Platt, van Hest, & Ginley, 2010), high speed (Liao et al., 2010; Mueller, Xia, & Avouris, 2010), low power consumption and energy efficient from year to year (Asghari & Krishnamoorthy, 2011; S. Kim et al., 2012). These aspects are very important and compulsory when coming into the designing of integrated circuit (IC) so that devices with a higher performance can be produced. Moore's law has predicted that the density of the components together with the performance of the IC doubles every two years, which means the scale of the components must be small enough so that more components can be located on the IC (Kish, 2002; Thompson & Parthasarathy, 2006). In today semiconductor industries, the complementary metal-oxide-semiconductor (CMOS) transistor technology has come to a nanoscale size of less than 30 nm as compared to the transistor size in 2002 which is around 100 nm (Kish, 2002; Levisse, Giraud, Noel, Moreau, & Portal, 2017). This indicates that as time goes by, the size of the transistor decreases, however there comes a limit for the size reduction of the transistor.

The size of the transistor is highly depending on the dimension of the gate oxide layer, especially the thickness. The downscaling of the gate oxide has nearly comes to an end due to the excessive gate leakage current in ultrathin oxide (≤1 nm) (Bohr & Young, 2017; Chien-Hao et al., 2002). Through the ultrathin gate oxide, electrons can then pass through it by tunneling effect, causing a leakage current. Since the capacitance of CMOS is directly proportional to dielectric constant (κ) and inversely proportional to thickness, when the reduction of thickness has come to a plateau, the only way to increase the capacitance is by replacing a material that possesses a high value of κ. The native gate oxide growth on the silicon (Si) wafer, silicon dioxide (SiO_2) was once widely used in the semiconductor industries because of its ability to grow natively on the Si substrate and therefore a low defect density interface can be produced, its high melting point (1713 ^{o}C), high resistivity ($\geq 10^{15}$ Ω-cm), great dielectric strength (10^7 V/cm) and large energy band gap (9 eV) (El-Kareh, 1995; Green et al., 1999). Apart from that, mass production is possible for SiO_2 gate oxide and most importantly the cost of manufacturing is low. Nevertheless, SiO_2 gate oxide shows a high leakage current characteristic due to severe electron tunneling when it is thin enough (≈1.2 nm) and has a κ-value of 3.9, which is considered a low-κ dielectric material (Bohr & Young, 2017; Green et al., 1999). Although there are numerous researches done to further downscaling the gate oxide thickness and to reduce the leakage current issues (J.-G. Lee, Kim, Seo, Cho, & Cha, 2016; Matsumoto et al., 2016; Sharma & Rana, 2015), selecting the high-κ materials has become a huge concern among the researchers in the semiconductor industry.

1.2 Problem statement

As the technology getting more and more advanced these days, electronic device utilization is essential and therefore the performance of the device must be very high. In order to have high performance device, IC with high density of electronic component, i.e. transistor must be implemented. To be able to do so, the dimension of the transistor has to be downscaled especially the reduction in gate oxide thickness, so that more components can be implemented to the circuit. While the gate oxide thickness is no longer can be reduced due to high leakage current in the oxide layer, a substitution of materials with high-κ value without further decreasing in thickness has to be done to replace the existing SiO_2 gate oxide (D. Gilmer et al., 2002).

Germanium (Ge) had raised a discussion among researchers and they are putting more interests into Ge because of it possesses a high carrier mobility over Si. Moreover, Ge shows some other advantages as well, such as smaller band gap that enables the device to work at a lower voltage, thus less power is consumed. Although it has a smaller band gap than Si, it is still high enough to prevent the instabilities through thermionic emissions and band-to-band tunneling (Pillarisetty, 2011). However, the native oxide of Ge, germanium oxide (GeO_2) has poor electrical property which lead to a hardship in fabricating Ge MOSFET (Xie, Yu, Lai, Chan, & Zhu, 2008). Also, GeO_2 interface show a higher defect densities due to its lower stability as compared to SiO_2 (Afanas'ev et al., 2008).

To solve the problem above, there are several researches done by applying the technology of high-κ dielectric used in Si MOS field-effect transistor (MOSFET) on Ge substrate. Since Ge requires only a lower temperature to activate the dopants which is good for combining with high-κ materials, the technology can be applied well on the substrate (Houssa et al., 2007). The reason why applying high-κ materials on Ge is to

obtaining a low equivalent oxide thickness (EOT) and also a thermally stable passivation layer rather than Ge oxide (Kamata, 2008). Many high-κ materials have been investigate on Ge substrate such as aluminium oxide (Al_2O_3), zirconium oxide (ZrO_2), hafnium oxide (HfO_2), titanium oxide (TiO_2), etc. However some of them show some undesirable results for the high-κ/Ge gate stack. HfO_2 is unfavorable to be applied on Ge substrate due to its high leakage current (J_g) without an intentional interfacial layer such as germanium oxinitride (GeON)(Yoshiki, Yuuichi, Tsunehiro, & Akira, 2005).

The emerging rare earth oxides (REO) have shown promising results on the high-κ/Ge gate stack. Lanthanum oxide (La_2O_3), cerium oxide (CeO_2), gadolinium oxide (Gd_2O_3) and dysprosium oxide (Dy_2O_3) are used as the candidates for high-κ materials used on Ge substrate and the others REO are still being investigated on their performance when applying on Ge substrate (Afanas'ev et al., 2006; Dimoulas et al., 2007; Jaeyeol et al., 2007; Mavrou et al., 2008; Rahman, Evangelou, Androulidakis, & Dimoulas, 2009). It is predicted that samarium oxide (Sm_2O_3) is suitable to be used as promising REO gate oxide on Ge substrate because of its high-κ properties, low leakage current at high electrical field, large band gap energy and low losses at low frequencies (Constantinescu, Ion, Galca, & Dinescu, 2012).

In this research, Sm_2O_3 is grown on the Ge substrate by first sputtered the pure metal samarium (Sm) on the substrate and the stack then underwent thermal oxidation to develop Sm_2O_3/Ge gate stack. Since there are still no related researches on the effect of oxidation temperature on the growth of Sm_2O_3 on Ge substrate, hence the oxidation temperature will be investigated in this research and the optimum temperature for the growth of the thin film will be proposed after the characterization is done.

1.3 Objectives

The core objective of this research is to develop a layer of Sm_2O_3 on the Ge substrate by first sputtering of pure rare earth Sm metal on the substrate and then followed by thermal oxidation in the furnace with oxygen (O_2) flow. Concurrently, the sub-objectives to be achieved of this research are as shown as below:

1. To investigate the effect of oxidation temperature to the growth of Sm_2O_3 on Ge substrate by varying the temperature for the thermal oxidation, and observe which temperature works the best for the optimum growth of the oxide layer.
2. To characterize the Sm_2O_3 thin film growth on the Ge substrate at 300 °C, 400 °C, 500 °C, 600 °C and 700 °C.

1.4 Scope of study

In this research, Sm_2O_3 film is grown on Ge substrate by thermal oxidation. Before subjecting to thermal oxidation, pure Sm metal was first sputtered on the substrate. The Sm-sputtered-Ge substrate is proceeded to the furnace for thermal oxidation in fixed O_2 gas flow (150 cc/min), pressure (1 atm) and oxidation time (t = 15 minutes) to grow Sm_2O_3 thin film. By varying the parameter of oxidation temperature (T = 300°C, 400°C, 500°C, 600°C and 700°C), the properties of the oxide film layer is investigated (Goh, Haseeb, & Wong, 2016). The physical characterization is carried out by using X-ray diffraction (XRD) to observe the composition found in the samples and predict the thickness of the oxide layer formed. Furthermore, Fourier-transform infrared spectroscopy (FT-IR) is performed to obtain the transmittance spectra of the oxide thin film.

1.5 Outline

The outline of this research project is arranged in the systematic ways to provide a clear vision of the researched work. Chapter 1 mentions a general introduction about the background, current scenario and limitation of semiconductor technologies in the recent years, problem statement, objective and scope of study of this research. Chapter 2 explains further the literature review on first a detailed introduction about CMOS/MOSFET and the limitation faced by existing SiO_2, followed by Ge as substrate material, various high-κ materials and Sm_2O_3 as gate oxide. Then it proceeds to the deposition methods of the thin film and finally the effect of temperature on the deposition method (thermal oxidation). While in Chapter 3, a well-ordered methodology of this researched is shown and described in detailed. Chapter 4 presents the results, analysis and discussion of the samples that are thermally oxidized by varying the time parameter. In Chapter 5, the research project is concluded together with the limitation and future prospect of present research.

CHAPTER 2: LITERATURE REVIEW

2.1 Introduction

MOSFET IC technologies grows in a tremendous speed and thus more and more powerful electronic components like capacitors and transistors have to be implemented into the IC in order to cope up with those technologies and to produce a high efficiency and high performance electronic device. Based on Gordon Moore's prediction, the components per chip increase by a factor of two every two years as shown in Fig 2.1 (Alferov, 2013; Cheng & Jay Guo, 2004). However, the famous prediction is almost coming to an end, which means that the further downscaling of the components has reached a limit (Im et al., 2000; Pei, Bin, Zhiyin, & Sheng, 2011).

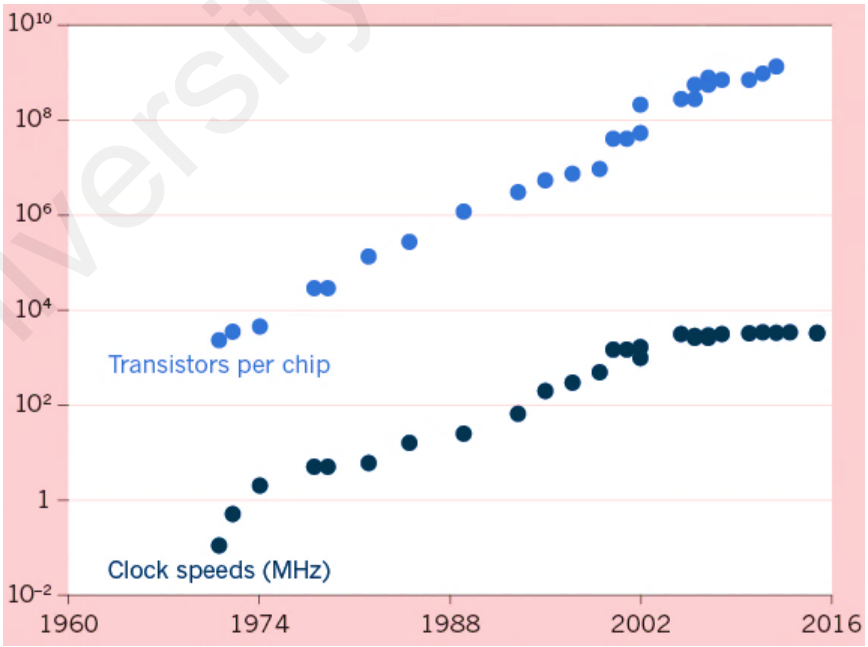

Figure 2.1: Increasing of transistors per chip and clock speeds with respect to year by Moore's law (Cheng & Jay Guo, 2004).

The downscaling of MOSFET requires the reducing of oxide thickness in the transistor. As the thickness is reduced, the capacitance increases with respect to the formula given below:

$$Capacitance, C = \frac{\kappa\, \varepsilon_0\, A}{t} \qquad \text{(Equation 2.1)}$$

where C is the oxide capacitance, κ is the oxide dielectric constant, ε_0 is the absolute permittivity with a constant value (8.854 pF/m or pC/V.m), A is the area of the oxide layer and t is the oxide thickness (Wilk, Wallace, & Anthony, 2001; Zecheng et al., 2015). From the equation above, since the area of the oxide cannot be increased due to downscaling, thickness reduction is preferable in order to increase the capacitance and performance of the transistor. Si wafer is widely used in the semiconductor industries and its native oxide, SiO_2 is used as the gate oxide because of the ease of the growth of SiO_2 on Si substrate by just thermal oxidation, and therefore a larger batch can be produced and thus a low production cost can be possible (Wilk et al., 2001). Moreover, the thermal oxide grown possessed a higher quality and therefore it has gained the popularity in semiconductor sectors (Usui et al., 2013).

2.2 Silicon dioxide (SiO_2)

Although there are advantages of SiO_2 for being used for the past few decades, however, for further downscaling of the transistor, the performance of SiO_2 as gate oxide has reached a limit due to its high leakage current (K. Kakushima et al., 2010). As the thickness decreases, especially when it is reduced to 1 nm, the gate tunneling in SiO_2 is very severe and therefore inducing a high leakage current in the gate oxide (Salmani-Jelodar et al., 2016). This will cause a significant drop in the magnitude of capacitance as bias increases due to high gate tunneling current(Yang & Hu, 1999).

Given a gate bias of 1 V, the reduction of SiO_2 gate oxide thickness from 3.0 nm to 1.0 nm causes an increment in gate current density (J_g), from 1 x 10^{-6} A/cm^2 to ≈1 x 10^4 A/cm^2 as shown in Fig. 2.2 (Misra, Iwai, & Wong, 2005; Yeo, King, & Hu, 2002).

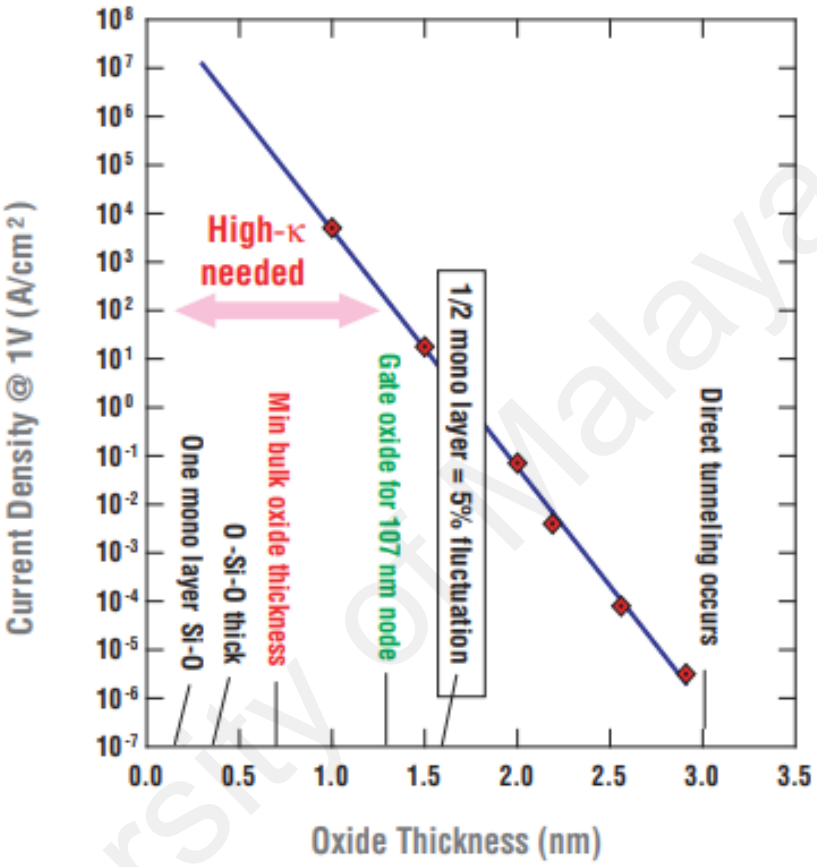

Figure 2.2: Increase in tunneling current density as the oxide thickness decreases (Misra et al., 2005).

Gate oxide function is to insulate the gate terminal and the connecting channel of the source-drain terminals of the MOSFET as shown in Fig. 2.3. With high leakage current, it will definitely decreases the performance and often resulting in intolerable power consumption and causes malfunction to the electronic device (D. C. Gilmer et al., 2002). Since that the thickness of gate oxide has to be reduced for further downscaling purpose, the alternative way to maintain the high capacitance is by substituting the

relatively low-κ SiO_2 (κ = 3.9) to a higher permittivity κ candidates based on Eq. 2.1. As κ increases, the capacitance remains unchanged despite further decreasing of oxide thickness. When coming into design purposes of using high permittivity dielectrics than that of SiO_2, equivalent oxide thickness (EOT) magnitude is much more relevant than dielectric film thickness,

$$EOT = \frac{\kappa_{high-\kappa}}{\kappa_{SiO_2}} . t_{SiO_2} \qquad \text{(Equation 2.2)}$$

which is the new high-κ oxide layer thickness with $\kappa_{high\text{-}\kappa}$ requires to achieve the same capacitance given SiO_2 thickness, t_{SiO_2} with κ_{SiO_2}(Goh, 2017; He, Sun, Liu, & Zhang, 2012). Therefore, there are a lot of experimental works focusing on selecting the right high-κ materials for MOSFET gate oxide, instead of SiO_2.

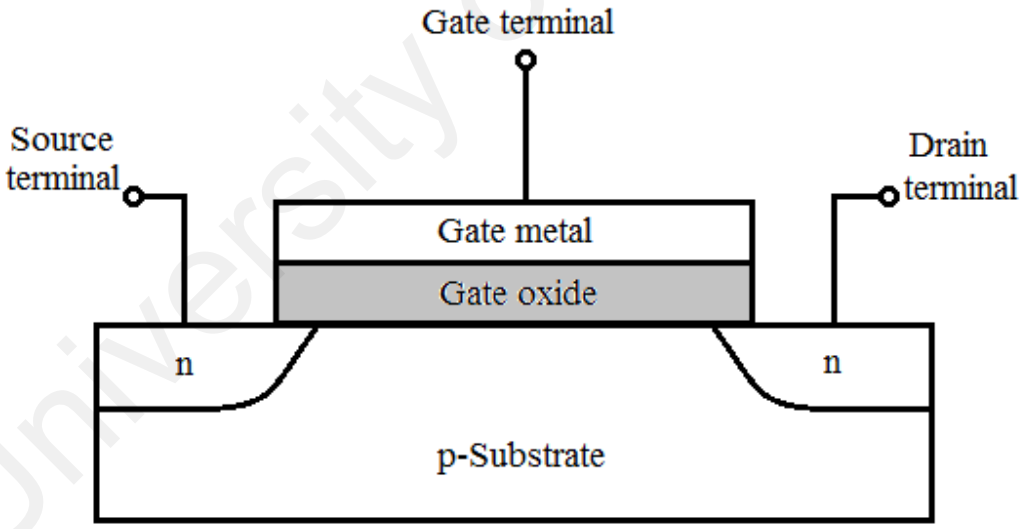

Figure 2.3: Schematic diagram of an n-p-n MOSFET transistor

2.3 Ge as substrate material

Although Si has been used for the substrate material due to the ease of high quality SiO_2 by thermal growing for the past decades, however recently researchers are putting more emphasizes on the Ge substrate as it had been shown to possess more advantages than Si when coming to the MOSFET applications (Houssa et al., 2007). In fabrication of the high speed and high efficiency IC, the carrier mobility plays a vital role in manipulating the aspect. Ge shows the greatest advantage over Si in terms of its superior carrier mobility, especially the electron mobility. Houssa et al. mentioned that the high carrier mobility of Ge gives an allowance to the boosting of drive current of the transistors. Band gap of Ge is relatively lower than Si, which allows a lower power consumption since the power supply voltage, V_{DD} can be further scaling (Houssa et al., 2007; Kamata, 2008). Table 2.1 shows the comparison between Ge and Si in terms of carrier mobility and other important parameters.

Ge was once used in the semiconductor industry and getting replaced by Si due to its high thermodynamically unstable native oxide GeO_2. Unlike Si, Ge does not have a stable native oxide to passivate its surface. During the operation temperature above 450 °C, unstable GeO_2 tends to form GeO and thermally desorbed from the oxide interface (Ogawa et al., 2015). The formation of GeO leads to high defect densities at GeO_2/Ge interface. However, several buffer technologies have been discovered to actually suppress the growth of GeO_2 layer, and Ge surface passivation such as NH_3 gas treatment (Cheng & Jay Guo, 2004; Pei et al., 2011), S-passivation (Zecheng et al., 2015), wet-NO treatment (L. Wang et al., 2015), CF_4 treatment (Xie et al., 2008) and etc. With proper surface treatment, high-κ/Ge stack can be realized without any interfacial layers which enables the further scaling of gate EOT and effectively obtaining a higher mobility (Kamata, 2008; L. Wang et al., 2015). Also, the lower

dopant activation temperatures enables the ease of integrating with a high-κ materials (Ogawa et al., 2015).

Table 2.1: Comparison between Ge and Si as substrate material (Kamata, 2008).

	Ge	Si
Band gap (eV)	0.66	1.12
Electron mobility, μ_e (cm^2/V.s)	3900	1500
Hole mobility, μ_h (cm^2/V.s)	1900	450
Lattice constant, a (Å)	5.65	5.43
Melting point, T_m (°C)	937	1412

2.4 Properties of a high-κ dielectric

Several articles had pointed out various high-κ (κ > 10) materials to be applied on the MOSFET as gate dielectric as a means to provide a considerably thicker EOT dielectric to minimize leakage current and improve gate capacitance (Misra et al., 2005; Wilk et al., 2001). In order to be successfully implemented into the MOSFET application, high-κ materials must possessed the following criteria such as high permittivity, large band gap, high thermal stability and excellent surface quality (Chiu, Mondal, & Pan, 2012; Lu & Zhang, 2012).

2.4.1 High permittivity, κ value

High-κ value ensures the high capacitance with respect to reduction in oxide thickness. However, the κ value cannot be extremely large because it may cause a large fringing field at the source and drain terminals.

2.4.2 Insulator property with larger band gap (E_g)

The gate dielectric should have a larger band gap (E_g > 5 eV) since it required a larger band offset to hinder the Schottky emission of electron/hole of substrate-oxide interface. With a good band offset, the leakage current can be minimized.

2.4.3 High thermal stability

Gate dielectric with high thermal stability is strongly required in MOSFET application. During high temperature operations, formation of other layer like native oxide at the high-κ/substrate interface is not preferable since it will reduce the efficiency of the high-κ dielectric. Also with high thermal stability, the high-κ oxide material will not decompose easily under high temperature.

2.4.4 Excellent interface quality and film morphology

For the high performance CMOS device, the oxide/substrate must possess a high quality and must be free from interfacial defects. It is desired to select a high-κ material that remains amorphous state since it can improve the electrical performance of the device by minimizing the defect state through self-interfacial bonding.

2.5 High-κ metal oxide and transition metal oxides (TMOs)

There are numbers of researches done to seek for the high-κ candidates to substitute SiO_2, mostly are TMO (except Al_2O_3). When applied the high-κ TMO on Si substrate, unfortunately, there are several issues associates with the ionic high-κ oxides, which are mainly cause by the nature of TM-oxygen bond. TM oxidizes easily by transferring electrons from d and s-sub shell to oxygen 3s and 3p orbital, and the oxide film formed contains a large amount of oxygen voids that are easier to be partly crystallized, and thus leads to a higher trap density in the film (Misra et al., 2005). The information and further discussion on issues of TMO/Si are arranged and tabulated in Table 2.2.

However, in high-κ/Ge stack, the issues found are mostly on the high interface state density (10^{12} - 10^{13} / eV.cm2) and the diffusion of Ge into high-κ oxides due to the direct junction of high-κ/Ge (Shibayama et al., 2012). The most severe problem found in high-κ/Ge stack is the desorption of GeO at the interface as shown in Fig. 2.4, that causes the drop in surface quality and deteriorates the surface, and thus proposing a hard times in developing insulating TMO on the Ge substrate (S. K. Wang et al., 2010). HfO_2 is the common TMO used in the high-κ/Ge stack; however it cannot be directly deposited on the Ge substrate, as it will degrade the electrical properties of the HfO_2/Ge system (Ogawa et al., 2015). Ogawa et al. mentioned that the insertion of GeO_2 into the HfO_2/Ge stack is not enough to increase the performance of Ge-MOS stack, and proposed by introducing a thin layer of Al_2O_3 into the HfO_2/GeO_2/Ge stack, the Ge out-diffusion is suppressed and the GeO desorption can be controlled (Ogawa et al., 2015). Another high-κ gate oxide material used to study high-κ/Ge stack would be ZrO_2 because it shows no increment in leakage current in ZrO_2/Ge stack as compared to the HfO_2/Ge (Yoshiki et al., 2005). Yoshiki et al. also declared that the inter-diffusion of

Ge-rich interfacial layer into ZrO_2 after annealing making the direct deposition of ZrO_2 on Ge possible (Yoshiki et al., 2005). Nevertheless, there are past papers that mentioned the direct deposition of ZrO_2 on Ge by atomic layer deposition (ALD) had a large lattice mismatch with Ge and failed to obtain a high quality epitaxy over the whole film, and thus lower the electrical performance of the gate dielectric (H. Kim, Chui, Saraswat, & McIntyre, 2003).

Table 2.2: Summary of the common high-κ metal oxide and TMOs (Goh, 2017; J Robertson, 2004; John Robertson & Wallace, 2015).

Materials	κ	Band gap (eV)	Band Offset with Si (eV)	Issues
Al_2O_3	9	8.8	2.8	Large interfacial trap density, large flat band voltage (V_{FB}) shift, large fixed charge.
ZrO_2	25	5.8	1.5	Interfacial layer formed easily and high interface state density, lateral oxidation at the edge of gate, growth of microcrystal after heat treatment, fixed charges exist and large V_{FB} shift, in addition, HfO_2 has high concentration of oxygen vacancies causes a huge amount of trapped charges.
HfO_2	25	5.8	1.4	
TiO_2	80	3.5	0	Zero conduction offsets with Si, low thermodynamic stability, and low crystallization temperatures limit MOSFET fabrication process temperatures.
Ta_2O_5	22	4.4	0.35	Low conduction offsets with Si, low thermodynamic stability.
Y_2O_3	15	6	2.3	Low crystallization temperatures, higher interface density than SiO_2 and undesirable interfacial layers formed easily.

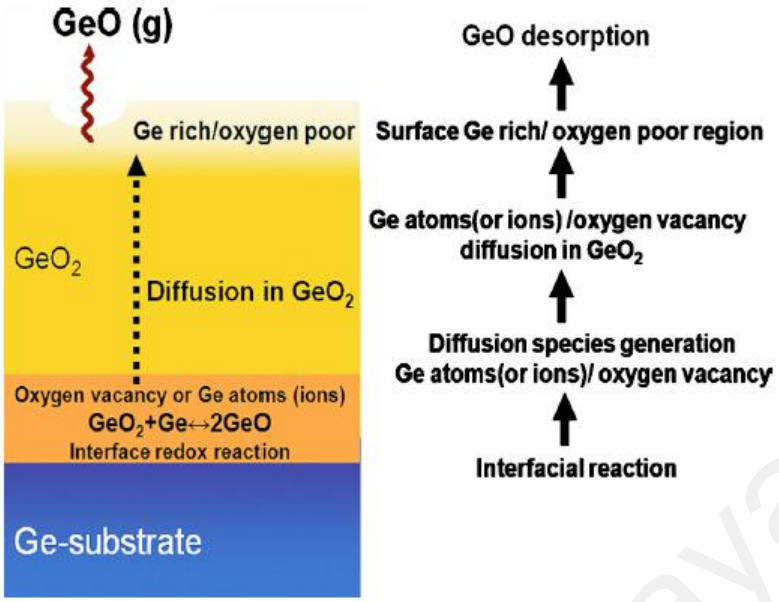

Figure 2.4: Schematic diagram of GeO desorption mechanism (S. K. Wang et al., 2010).

2.6 Rare earth oxides (REOs)

As the most promising high-κ TMO, HfO_2 and ZrO_2 show a downside in the degradation of electrical properties of the gate oxide, the rare earth metal oxide (REO) had grown a huge popularity among the high-κ dielectric researchers. REO is explored and emerged as high-κ candidate, and believed to show better results in MOSFET application due to its superior intrinsic characteristics (Chin, Cheong, & Hassan, 2010). Rare earth elements, also known as lanthanides are relatively abundant in the earth crust, despite the name "rare earth". Lanthanides consist of 15 elements from atomic number 57 to 71, lanthanum (La), cerium (Ce), praseodymium (Pr), neodymium (Nd), promethium (Pm), samarium (Sm), europium (Eu), gadolinium (Gd), terbium (Tb), dysprosium (Dy), holmium (Ho), erbium (Er), thulium (Th), ytterbium (Yb), and lutetium (Lu). Pm exhibits radioactive property and does not occur naturally. Lanthanide oxide (LnO_x) exists in different stoichiometries (LnO, LnO_2, Ln_2O_3) owing

to different oxidation states of rare earth metals (+2, +3, +4). Due to the non-insulating properties of lanthanide (II) oxides (LnO_2), they are thus not suitable to be used as gate dielectric (Osten et al., 2008).

Lanthanide (III) oxides (Ln_2O_3) are given a large attention for the MOSFET application since they satisfied the required criteria for high-κ dielectric materials: high κ value, high band gap and band offset, thermodynamically and chemically stable, and high interface quality. Moreover, Ln_2O_3 shows good electrical properties and low density of interfacial states (D_{it}) when direct deposited on Ge substrate without any intermediate layer passivation (Mavrou et al., 2007). Fig. 2.5 shows the dielectric constant and band gap for various Ln_2O_3. From Fig. 2.5, the high-κ candidates can be narrowed down into 5 (Tm_2O_3, Ho_2O_3, Ee_2O_3, Sm_2O_3 and La_2O_3) after considering the κ value and band gap ($\kappa > 12$, $E_g > 5$ eV).

From the aspect of high permittivity, numerous works are done on La_2O_3/Si and La_2O_3/Ge since it has the largest κ value among the REO (≈ 19) and possessed a large band gap (> 5eV) (Chang, Endo, Kato, Takenaka, & Takagi, 2017; Kuniyuki Kakushima et al., 2010). While utilizing REO as gate dielectric, high hygroscopic property is always the concern which the REO tends to absorb moisture from the environment, forming hydrate ($Ln_2O_3.H_2O$). The hydrate is then forming the hydroxide ($Ln(OH)_3$) layer that causes the EOT to be increased and reduces the κ of the REO. The hygroscopic property of REO highly depends on its lattice energy and electronegativity. As the electronegativity decreases and the lattice energy increases, the moisture reactivity with REO increases, meaning that, La_2O_3 has the highest hygroscopic behavior while Lu_2O_3 has the lowest hygroscopic behavior, based on Fig. 2.6 (Goh, 2017).

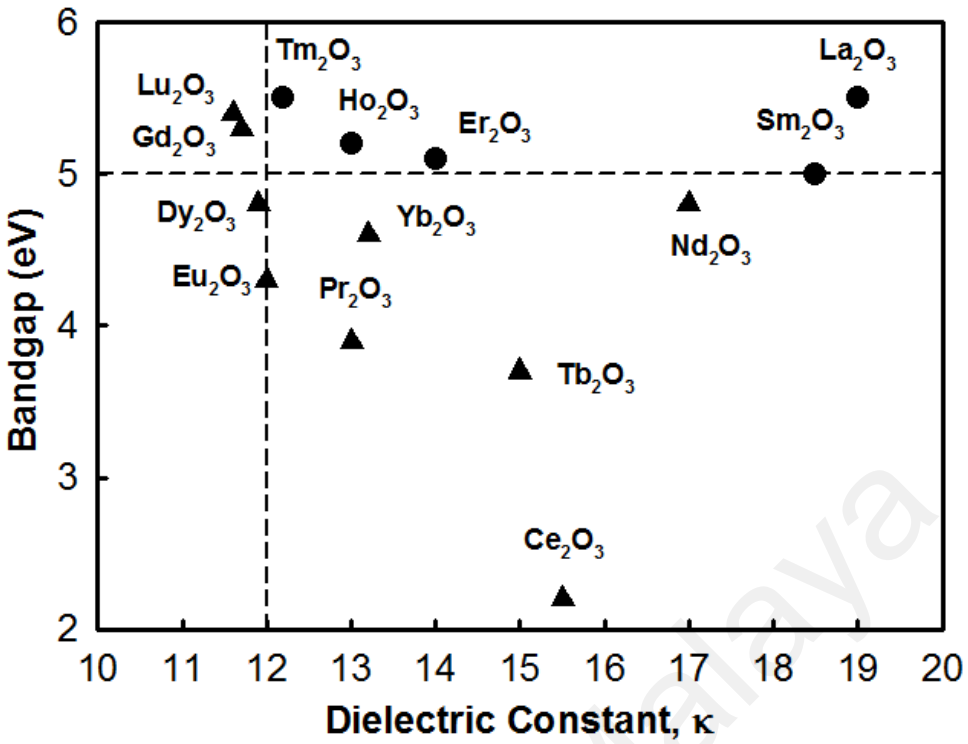

Figure 2.5: Dielectric constant and band gap of various lanthanide (III) oxides (Goh, 2017).

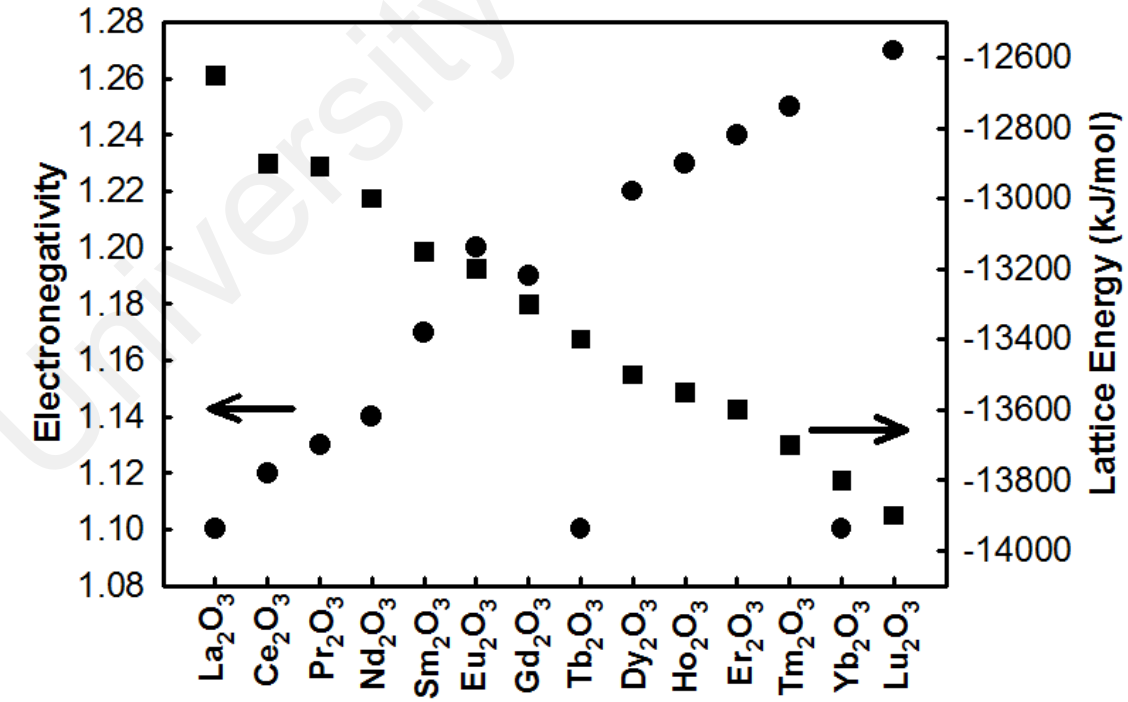

Figure 2.6: Electronegativity and lattice energy of various lanthanide (III) oxides (Goh, 2017).

2.7 Samarium (III) oxide (Sm_2O_3)

While La_2O_3 possessed the highest κ value but exhibits the highest hygroscopic behaviour, there is a need to seek for another REO, and Sm_2O_3 is the best alternative REO since it has a high κ value as well, after La_2O_3. Not only that, amorphous oxide of Sm shows superior electrical properties such as low leakage current, high oxide capacitance and also thermodynamically stable on Si (Päiväsaari, Putkonen, & Niinistö, 2005). Moreover, Päiväsaari et al. also stated that Sm_2O_3 has the lowest VFB shift and lowest leakage current density when comparing with another REO thin films of 50 nm deposited on Si by ALD method. When comparing La_2O_3/Si and Sm_2O_3/Si, again Sm_2O_3 shows the lowest leakage current(Chin et al., 2010). Also to be mentioned, Sm_2O_3 possessed a lower hygroscopic behaviour as compare to La_2O_3 which makes Sm_2O_3 a suitable REO gate dielectric. Although there are still no published materials that mentioned about the performance of Sm_2O_3/Ge stack, but Sm_2O_3 is believed and predicted to be well implemented on Ge substrate and thermodynamically stable on Ge.

2.8 Deposition method for REO thin film

There are two major types of REO thin film deposition method, which are chemical vapour deposition (CVD) and physical vapour deposition (PVD). Fig. 2.7 illustrates the various methods under the two main categories of thin film deposition method (Toshiyuki, 2014). The ultimate structure and the electrical performance of the gate oxide highly depending on the deposition method of the thin film and therefore the research purpose has to be taken into consideration while choosing the deposition method for gate oxide fabrication (Chin et al., 2010).

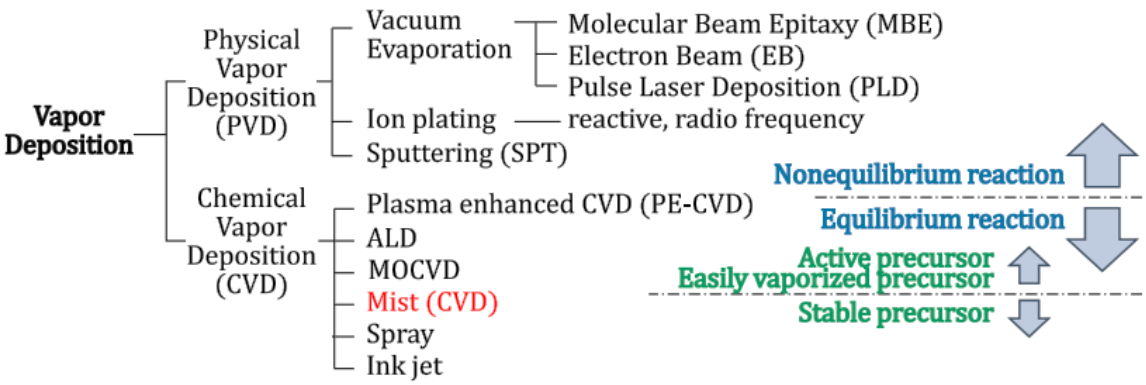

Figure 2.7: Various types of vapor deposition method (Toshiyuki, 2014).

2.8.1 Chemical vapour deposition (CVD)

CVD involves precursors and chemical reactions between gases and vapours during the deposition process. Plasma enhanced CVD (PECVD), metal organic CVD (MOCVD) and ALD are the most common CVD methods used in thin film fabrication process. PECVD is the deposition method where a plasma of the reacting gases is generated, and the chemical reaction between the gases and the substrate takes place. PECVD method has the advantage that it only requires a low deposition temperature therefore defect formation, diffusion and metal layers degradation can be avoided(Ceiler, Kohl, & Bidstrup, 1995; W. G. Lee, Woo, Kim, Choi, & Oh, 1994). In MOCVD, elements that will be deposited on the substrate are combined with complex organic gas molecules, and passed over the hot surface of the substrate to promote reaction. By using MOCVD, multi-layer stacks can be realizable with each of a precise controlled thickness, thus the electrical and optical performance of the oxide is likely to be controlled. Also the main advantages of MOCVD are again low operation temperature using metalorganic precursors, conformal surface coverage and able to fill the vias with no defects(Gross, Fleming, Cheung, & Heimbrook, 1991).

ALD is widely used in the thin film deposition and it involves alternative pulsing and purging of two or more precursors gases and vapours, promotes chemisorption and surface reaction on the substrate in a sequential manner (Chin et al., 2010; Leskelä & Ritala, 2002). The deposition of thin film is done with several cycles, as shown in Fig. 2.8, thus the growth stability and film thickness in each cycle can be easily controlled. Previous journal mentioned about the deposition of Sm_2O_3 via ALD method showed a good result in low leakage current (Päiväsaari et al., 2005). However, the presence of the unwanted contaiminants on the precursors and reactors caused a drawback in ALD method (Chin et al., 2010).

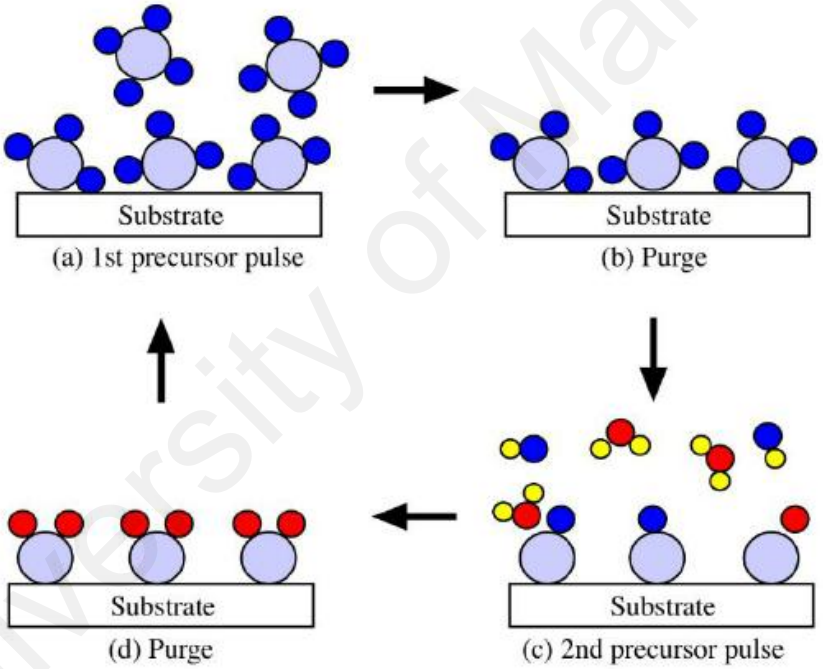

Figure 2.8: Mechanism for one cycle of ALD (M Rosa, Lin, Pfeffer, Nielsen, & Dai, 2018).

2.8.2 Physical vapour deposition (PVD)

PVD possesses various vaccum deposition methods that transform the solid/liquid target into gas state and finally deposited on the substrate as thin film. Sputtering (RF magnetron), evaporation method and pulsed laser deposition (PLD) are the common representatives for PVD method. Evaporation method consists of the traditional thermal evaporation and electron beam (E-beam) evaporation. Both evaporation methods share the same principle, the target material is heated up in a vacuum chamber, either by hot filament or E-beam, the gaseous target material is then evaporates and deposited on the substrate located at the top. The only difference between these two evaporation methods is in traditional thermal evaporation, heat is used to evaporate the target while bombardation of electrons causing the heating and evaporating of the target in E-beam evaporation, therefore thermal evaporation often requires a higher operating temperature which are sometimes not preferable in thin film deposition. PLD method utilizes the high energy pulsed laser beam to focus and strike on the desired target material, causing ablation of the target and being deposited on the substrate. As the parameter of the laser beam can be manipulated (pulse intensity, wavelength, etc.), the thin film deposition process can also be controlled (Chin et al., 2010). Moreover, PLD method is simple, where stoichiometric deposition can be made possible by using multiple target at one time, and also multi-layer hetero-structures can be done by in-situ processing (Shan, Shin, Jang, & Yu, 2004). Nevertheless, the highly forward directed laser plume during laser ablation process causes the thickness of thin film to be greatly non-uniform and the composition varies across the film has limit the use of PLD in thin film deposition (Chin et al., 2010).

Radio frequency (RF) magnetron sputtering is believed to be highly utilized in thin film studies and industries. In basic sputtering process, high voltage is applied on

the negative terminal (target material) and positive terminal (substrate). Due to the high voltage applied, the argon (Ar) gas in the chamber ionizes and forms plasma. The high energetic Ar^+ ions are then bombarded to the target and causes the removal of the target material. The removed target material and some electrons are then accelerates to the substrate and deposited as thin film. While in RF magnetron sputtering, a strong magnetic field is generated around target area and cause the electrons to spiral along the magnetic field as shown in Fig. 2.9. Hence, it reduces the damage implied to the thin film on the substrate, maintain the stoichiometry and ensure an even thickness distribution of the thin film (Maurya, Sardarinejad, & Alameh, 2014). Also, this method is beneficial for deposition of non-metallic element such as oxide since non-conductive materials can be used as target materials.

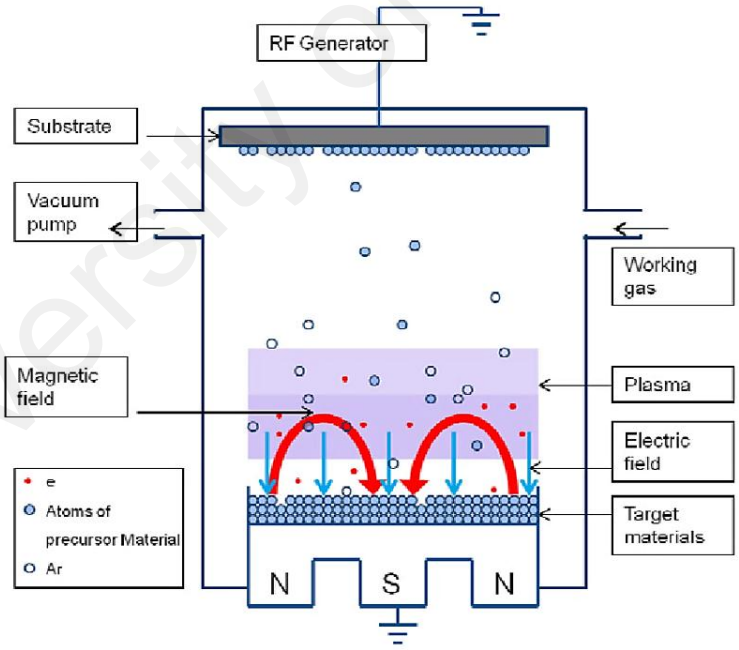

Figure 2.9: Schematic illustration of RF magnetron sputtering(Bosco, van den Beucken, Leeuwenburgh, & Jansen, 2012).

2.9 Thermal oxidation method

Thermal oxidation involves the flow of oxygen (O_2) gas to the substrate or metal-sputtered substrate and being heated up in a furnace as shown in Fig. 2.10. Thermal oxidation method exhibits several advantages: low operation cost, simple to perform and does not require high temperature or catalyst usage during thermal processing (Park, Kim, & Leem, 2015). Moreover, thermal oxidation has confirmed to be a simple ex-situ method to grow metal oxide films and enhance metal crystallinity(De Los Santos Valladares et al., 2014). While utilizing the thermal oxidation method, it is very important to recognize the parameters such as oxidation temperature, oxidation duration and O_2 gas flow rate or gas ratio. According to Goh et al., Sm_2O_3 that grown on Si substrate by thermal oxidation method, at 700°C for 15 minutes had shown a superior electrical performance and thicker Sm_2O_3 film grown with minimum thickness of interfacial layer and had smoother and uniform surface (Goh, 2017).

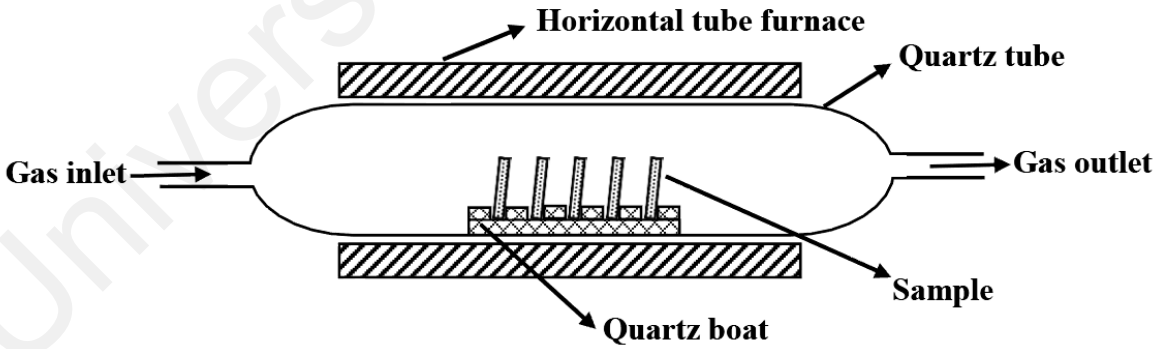

Figure 2.10: Schematic diagram for thermal oxidation method(Goh, 2017).

CHAPTER 3: MATERIALS AND METHODOLOGY

3.1 Introduction

This chapter will discuss in detailed on the materials and methodology used in this research project. The chapter is arranged in following sequence as shown:

i. Materials

ii. Procedures for thin film fabrication

iii. Characterization methods

3.2 Materials

3.2.1 Substrate

The substrate used is Ge wafer supplied by Wafer World, Inc. The properties of the Ge wafer used are as shown in Table 3.1.

Table 3.1: Properties of Ge wafer used

Properties	Description
Diameter	100.0 ± 0.5 mm
Type	n-Ge doped with antimony (Sb)
Orientation	(100) ± 5°
Thickness	500 – 550 μm
Surface	single side polished
Resistivity	0.005 – 0.02 Ω.cm

3.2.2 Chemicals used in dip-cleaning process

The chemicals used for dip-cleaning process are hydrofluoric acid (HF) solution with ratio of (1: 50 HF: H_2O) and deionized (DI) water.

3.2.3 Materials used in sputtering process

By using TF 450 PVD RF sputtering system, Sm metallic layer is sputtered on the sample by utilizing pure Sm metal (Kurt J. Lesker, USA, 99.99% purity) as the target material and Ar gas as sputtering gas.

3.2.4 Materials used in thermal oxidation

The Sm-sputtered samples are place on the quartz boat before placing into the quartz tube inside the Carbolite CTF tube furnace. After that pure O_2 gas is flow through the quartz tube for thermal oxidation to be taken place.

3.3 Procedures for thin film fabrication

3.3.1 Dip-cleaning of Ge substrate

The Ge wafer is cut into samples of 1 cm x 1 cm each, and underwent dip-cleaning process for the preparation of impurity-free samples. First, two beakers containing one with HF acid solution and another one with DI water are prepared, then

a sample is immersed in HF acid solution and is taken out after about 10 seconds. After that, it is again immersed in DI water for another 10 seconds, removed and then wiped with clean paper towel. The whole dip cleaning process is then repeated for all the samples.

3.3.2 Sputtering of Sm metal on Ge substrate

During the RF sputtering process, metallic Sm layer is sputtered on the samples from the Sm target with the flow of Ar gas at room temperature. The pressure in the chamber, power supply, and Ar gas flow rate are set to 3×10^{-5} mbar, 170 W and 25 ml/minute, respectively for the whole sputtering process.

3.3.3 Thermal oxidation of Sm_2O_3

First, the flow of O_2 gas through the furnace is checked to ensure smooth flow without the flow of other gases and the O_2 flow rate is set to 150 ml/minute. Then the furnace is set up and the temperature increment of the furnace is set to 10 °C/minute until the desired temperature for thermal oxidation. In this research project, the parameter to be varied is the oxidation temperature and the temperature variations are 300 °C, 400 °C, 500 °C, 600 °C, and 700 °C. Once the temperature of the furnace reached the set temperature, the Sm-sputtered samples are placed carefully on the quartz boat and is put in the middle part of the quartz tube inside the furnace. After 15 minutes of thermal oxidation, the samples are let cool down to room temperature, then are carefully taken out and kept in dry container containing silica gel to prevent moisture absorption. After that, the samples of different oxidation temperature are proceeded

with the physical characterization. The whole procedure of the gate oxide thin film fabrication is illustrated in Fig. 3.1.

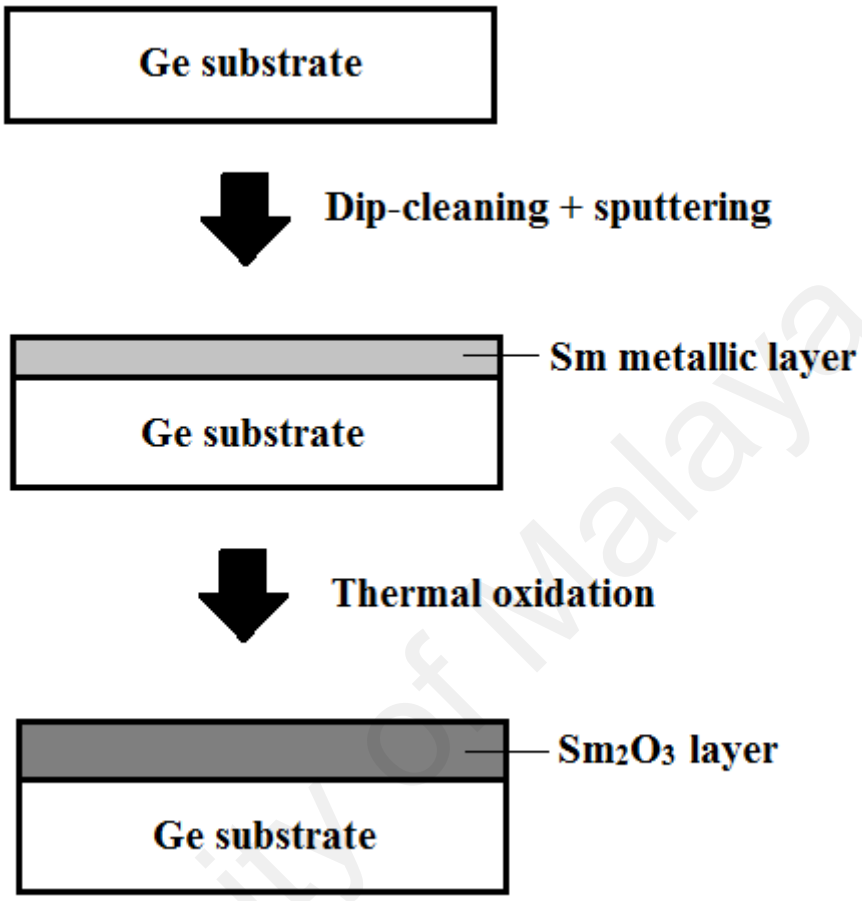

Figure 3.1: Schematic diagram of procedures for Sm_2O_3 thin film fabrication.

3.4 Characterization of Sm_2O_3 thin film

3.4.1 X-ray diffraction (XRD)

XRD is a powerful technique to study the structural properties of a material, such as surface and morphology (Birkholz, Fewster, & Genzel, 2005). This technique is

widely used in thin film studies, especially to study the composition and crystallite size of the thin film developed. Generally XRD equipment consists of x-ray source and a detector, the X-ray is focused on the sample and scattered to be detected by the detector as shown in Fig. 3.2. The detector move in a circle around the sample and the position of it is recorded as 2θ. At each 2θ angle, the intensity of the scattered X-ray is recorded by the detector in the form of "counts" or "counts per second". The sample rotates to accurately reflect each wavelength and satisfied Bragg's law:

$$n\lambda = 2dsin\theta \qquad \text{(Equation 3.1)}$$

For a crystal with *d* spacing (nm), when an X-ray beam with wavelength λ (nm) is directed to the crystal, reflection only occurs at a precise angle θ (°) for n ordered reflection that obeyed the Eq. 3.1. Therefore, through XRD analysis of an unknown composition in materials can be identified by the known lattice constant of the composition in the database. Eq. 3.2 shows the relationship between interplanar spacing, *d* with the lattice constant, *a*, where *h*, *k*, and *l* are the miller indices of a plane.

$$d = \frac{a}{\sqrt{h^2+k^2+l^2}} \qquad \text{(Equation 3.2)}$$

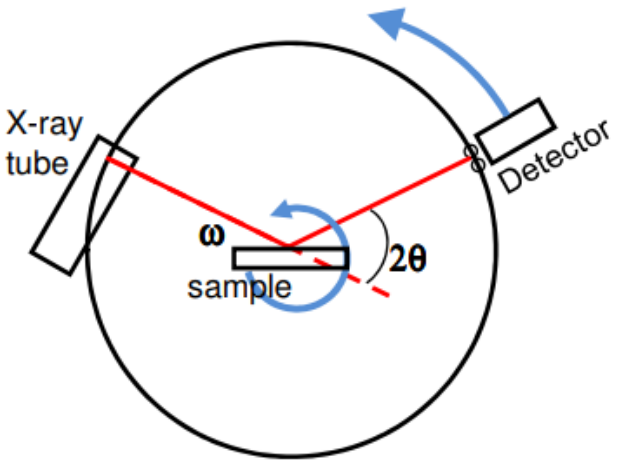

Figure 3.2: Basic working mechanism of XRD equipment. (*Source: http://prism.mit.edu/xray/ accessed on May, 2018*)

Besides knowing the composition of the materials, the crystallite size (*D*) and microstrain (ε) of the materials due to crystal defects and dislocation can be known by analyzing the XRD peak broadening (β) (Goh, 2017). This is because the nanocrystallite size, non-uniform lattice strain and defects will cause peak broadening that can be quantified. The broadening caused by strain is due to non-uniform distributions of atoms with respect to their own lattice position while broadening caused by crystallite size is due to the incoherent diffraction of finite size components with each other (Bushroa, Rahbari, Masjuki, & Muhamad, 2012). Among the techniques to analyze the peak broadening, e.g. Fourier method, Warren-Averbach method, Rietveld refinement and etc., Williamson-Hall (W-H) method is mostly used owing to its simplicity.

Since crystallite size (*D*) and microstrain (ε) are mainly contributed to the peak broadening, crystallite size of Sm_2O_3 is estimated simply by the Scherrer equation in Eq. 3.3 from the Debye-Scherrer analysis and microstrain is estimated through strain-induced broadening equation as in Eq. 3.4 (Goh, 2017; Maniammal, Madhu, & Biju, 2017).

$$D = \frac{K\lambda}{\beta_D cos\theta} \qquad \text{(Equation 3.3)}$$

$$\varepsilon = \frac{\beta_\varepsilon}{4tan\theta} \qquad \text{(Equation 3.4)}$$

From the Scherrer equation, *K* is the constant of shape factor that varies from 0.9 to 1.15, (in this case, *K* = 0.9), λ is the wavelength of x-ray used (nm), β_D is the full width half maximum (FWHM) of the peak for *D* at diffraction angle θ. While in Eq. 3.4, β_ε is the FWHM of the peak for ε at peak position θ.

According to W-H method, it is assumed that the two components of β_D and β_ε are independent to each other, hence both components can be added up that yields:

$$\beta_{hkl} = \beta_D + \beta_\varepsilon \qquad \text{(Equation 3.5)}$$

By substituting Eq. 3.3 and Eq. 3.4 into Eq. 3.5, the equation can be expressed as Eq. 3.6 and can be further simplified as Eq. 3.7.

$$\beta_{hkl} = \frac{K\lambda}{Dcos\theta} + 4\varepsilon\ tan\theta \qquad \text{(Equation 3.6)}$$

$$\beta_{hkl}cos\theta = \frac{K\lambda}{D} + 4\varepsilon\ sin\theta \qquad \text{(Equation 3.7)}$$

The oxidized Sm_2O_3 film is characterized using PANalytical Empyrean X-ray diffractometer (XRD) system in a scan ranging from 5° to 90° for 2θ, step size of 0.026 and time per step of 0.75 second. Copper radiation (Cu-Kα) with wavelength (λ = 0.15406 nm) is used as the X-ray source in the system.

3.4.2 Fourier-transform infrared (FTIR) spectroscopy

FTIR spectroscopy is used to identify the organic and inorganic components in unknown materials by using the infrared ranged light. It is a powerful tool for identifying the types of bonds of molecule by producing infrared absorption or emission spectrum and the wavelength of light absorbed characterizes the chemical bonding through the spectrum. As shown in Fig 3.3, the moving mirror produces a difference in optical path, light energy is absorbed or transmitted throughout the process and finally the transmitted part reached the detector. The detector is then Fourier-transforms the signal into frequency domain, which wavenumber is corresponds to optical path difference in time domain. Then, an infrared transmittance spectrum can be produced as transmittance-wavenumber plot (Smith, 2011).

In this research project, FT-IR analysis is done by using Bruker Tensor 27 FT-IR spectroscope. The analysis is done with 32 scans per sample and attenuated total reflection (ATR) mode is employed.

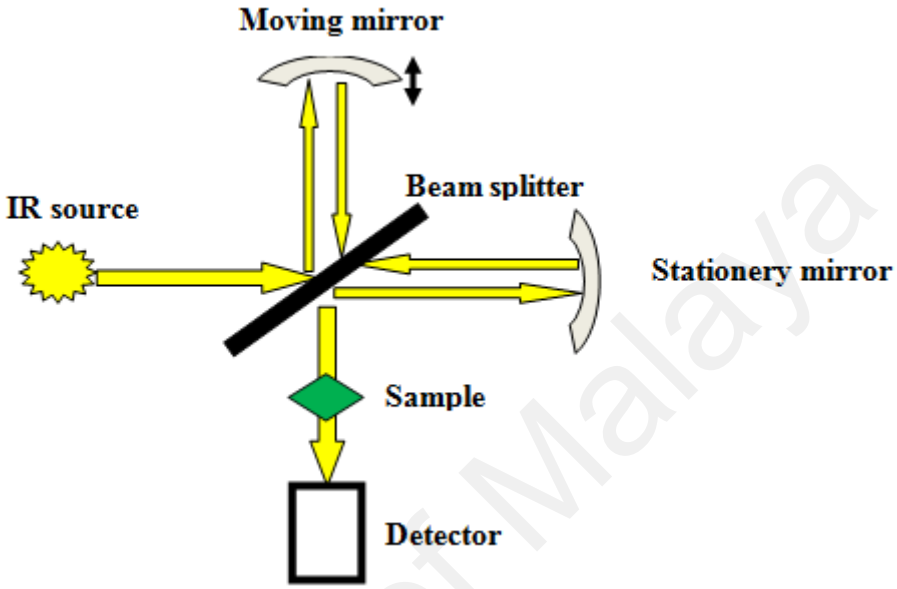

Figure 3.3: Simple illustration of FT-IR instrumentation (Source: *http://nptel.ac.in accessed on May, 2018*)

CHAPTER 4: RESULTS AND DISCUSSION

4.1 Introduction

In Chapter 4, the results collected from (i) XRD and (ii) FT-IR analysis are evaluated based on the effect of thermal oxidation temperature to the growth of Sm_2O_3 film. Then, the results analysis is followed by discussion on the physical properties of the Sm_2O_3 film grown on Ge substrate and the optimum temperature for the growth of the thin oxide film is predicted according to the discussion.

4.2 XRD analysis

Fig. 4.1 shows the XRD patterns of the thermal oxidized samples for 300 °C, 400 °C, 500 °C, 600 °C and 700 °C. The peak for interfacial disamarium germanium oxide, $Sm_2Ge_2O_7$ is detected at 54.19° for 300 °C, 400 °C, 500 °C, 600 °C and 700 °C samples, are confirmed by ICSD reference code of 00-031-1208 (Fig 4.1, cyan dashed line). As the oxidation temperature increases, the intensity of the peak for the interfacial layer decreases. For 700°C sample, hexagonal GeO_2, *h*-GeO_2 peaks are found at 20.52°, 25.95°, 35.93°, 37.94°, 39.37°, 41.81°, 44.96°, 48.66°, 53.39°, 56.24°, 58.81°, 61.67°, 65.96°, 67.11°, 69.97°, 73.82°, 76.26°, 77.51°, 78.55° and 79.94° corresponding to (010), (011), (110), (102), (111), (020), (021), (112), (202), (210), (211), (113), (122), (031), (014), (302), (220), (114), (221) and (130), respectively (Fig. 4.1, black dotted lines). These peaks are confirmed by ICSD with reference code 98-005-9624 (Haines, Cambon, Philippot, Chapon, & Hull, 2002). For 600 °C sample, *h*-GeO_2 peaks are observed at 20.52°, 25.95°, 53.39° and 65.96°, corresponding to (010), (011), (202) and

(122), respectively. Besides that, for 500 °C sample, a small intensity of *h*-GeO_2 peak is found at 53.39° as plane (202) while for 400 °C sample, a relatively high peak of *h*-GeO_2 is detected at the same plane. Last but not least, a peak that represents *h*-GeO_2 (202) is detected at 53.39° for 300 °C sample. From this, as the temperature increases, the peak of *h*-GeO_2 increases owing to the diffusion of O_2 gas into the substrate and formed the native oxide. On the other hand, cubic Sm_2O_3, *c*-Sm_2O_3 peak is observed at 51.73° as plane (611) for 300 °C and 500 °C (Fig. 4.1, green dashed line). The peak is confirmed by ISCD with reference code of 01-076-0153. It is observed that from the XRD patterns, there exists only *h*-GeO_2 and a small amount of $Sm_2Ge_2O_7$ for the 700 °C samples, and it is confirmed that there is no *c*-Sm_2O_3 present in the 700 °C samples. In other words, oxidation temperature of 700 °C is not suitable for the growth of Sm_2O_3 oxide layer on Ge substrate. Further exploration on the effect of the presence of $Sm_2Ge_2O_7$ interfacial layer on the gate oxide's effectiveness is required to strengthen the findings on this study.

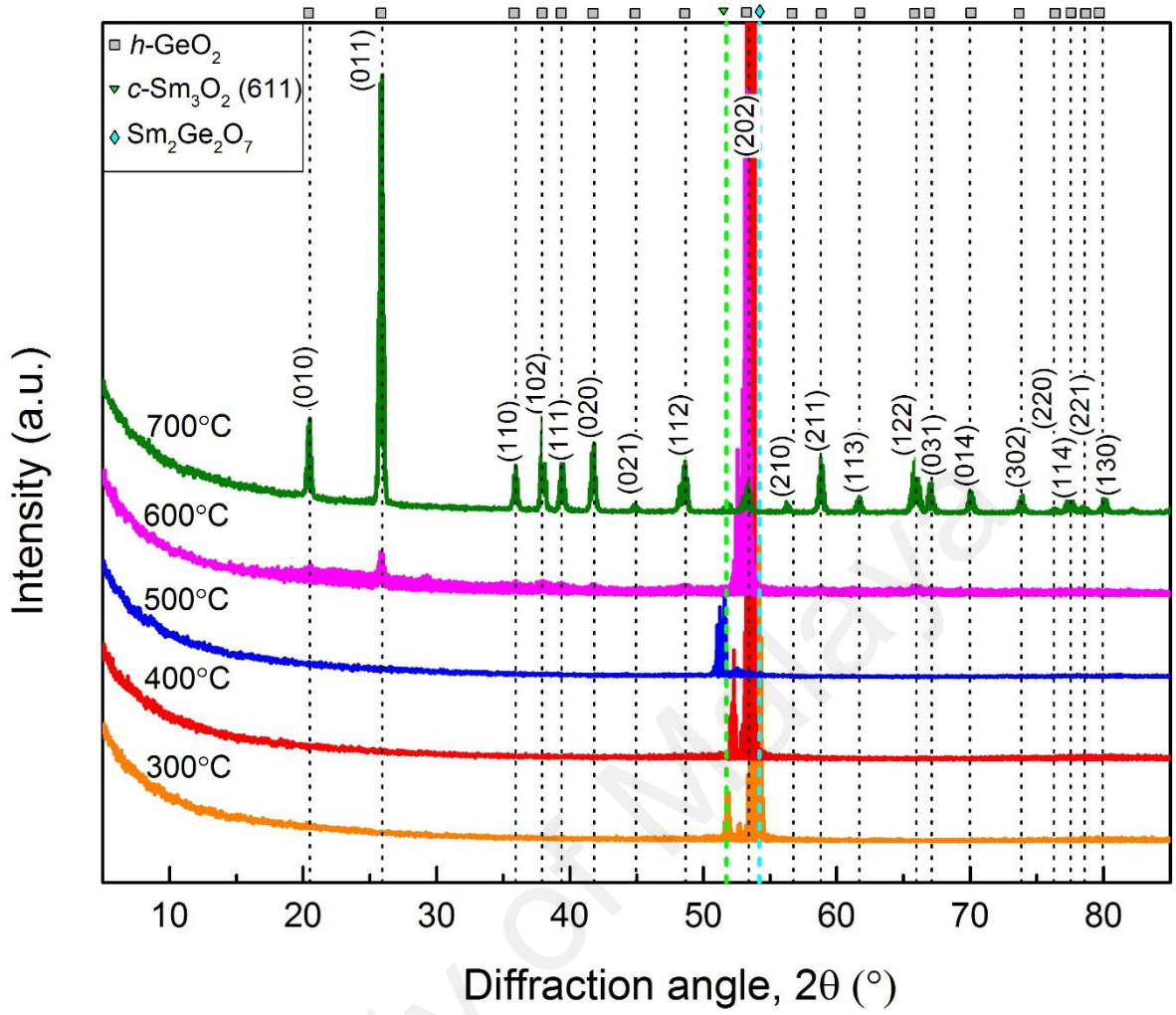

Figure 4.1: XRD patterns for thermal oxidized samples at various temperatures.

Fig. 4.2 shows the intensity-temperature plot for *h*-GeO_2 (011) and *c*-Sm_2O_3 (611). For the case of *h*-GeO_2 (011), the intensity is very low from 300 °C to 500 °C and slightly increased at 600 °C. At 700 °C, the plot shows a tremendous increase in intensity for *h*-GeO_2 (011). From Fig. 4.2, as the temperature increases from 300 °C to 700 °C, the intensity for *h*-GeO_2 (011) increases exponentially meaning that the crystallinity of *h*-GeO_2 is increasing over temperature and implies that the growth of *h*-GeO_2 at plane (011) is the highest at 700 °C. While for *c*-Sm_2O_3, the plot shows a relatively high intensity at 300°C and 500°C, and a low intensity at 400 °C, 600 °C, and 700 °C. After 500 °C, the intensity of *c*-Sm_2O_3 started to decrease and this may be

caused by the desorption of GeO, which causes defects in the form of scattered blisters on the film (Lei, Goh, Zainal Abidin, & Wong, 2017). Apart from that, $Sm_2Ge_2O_7$ peak shows the highest intensity at 300 °C sample, and shows a huge decline at 400 °C, followed by 500 °C, 600 °C and 700 °C.

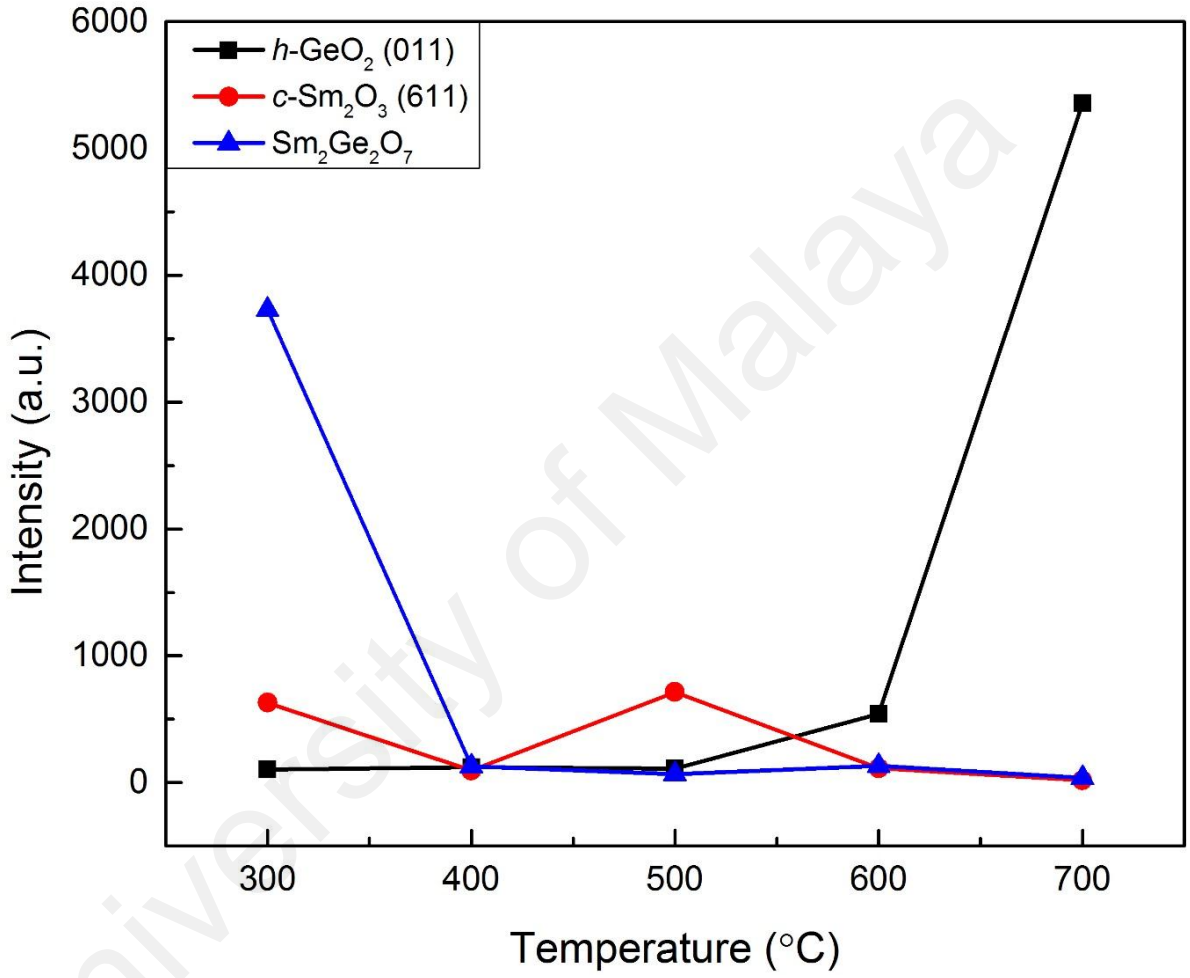

Figure 4.2: Plot of intensities for GeO_2 (011), Sm_2O_3 (611) and $Sm_2Ge_2O_7$ at various temperatures.

By utilizing the Debye-Scherrer equation (Eq. 3.3), crystallite size of the particles can be determined. Fig. 4.3 shows the crytallite size of *h*-GeO_2 for samples at various temperatures (300 °C to 700 °C). Based on the calculation, the crystallite size at 300 °C is 9.68 nm, 27.45 nm at 400°C and 22.93 nm at 500°C. The average crystallite

size at 600 °C is 20.86 nm with a size distribution of 5.67 nm, while at 700 °C, the average crystallite size is 19.66 nm with a size distribution of 4.60 nm. From 300 °C to 400 °C, the crystallite size of *h*-GeO_2 increases sharply, while as the temperature continues to increase from 400 °C to 700 °C, the crystallite size for *h*-GeO_2 reduces and a smaller size distribution indicates the homogeneous crystallite size (Goh et al., 2016). The average crystallite size of *c*-Sm_2O_3 cannot be calculated due to the inadequate information from the XRD data. For a more accurate way to determine crystallite size, transmission electron microscopy (TEM) should be carried out to observe and measure the crystallite size. Besides that, Williamson-Hall (W-H) analysis is done to estimate the crystallite size and the microstrain of the thin film.

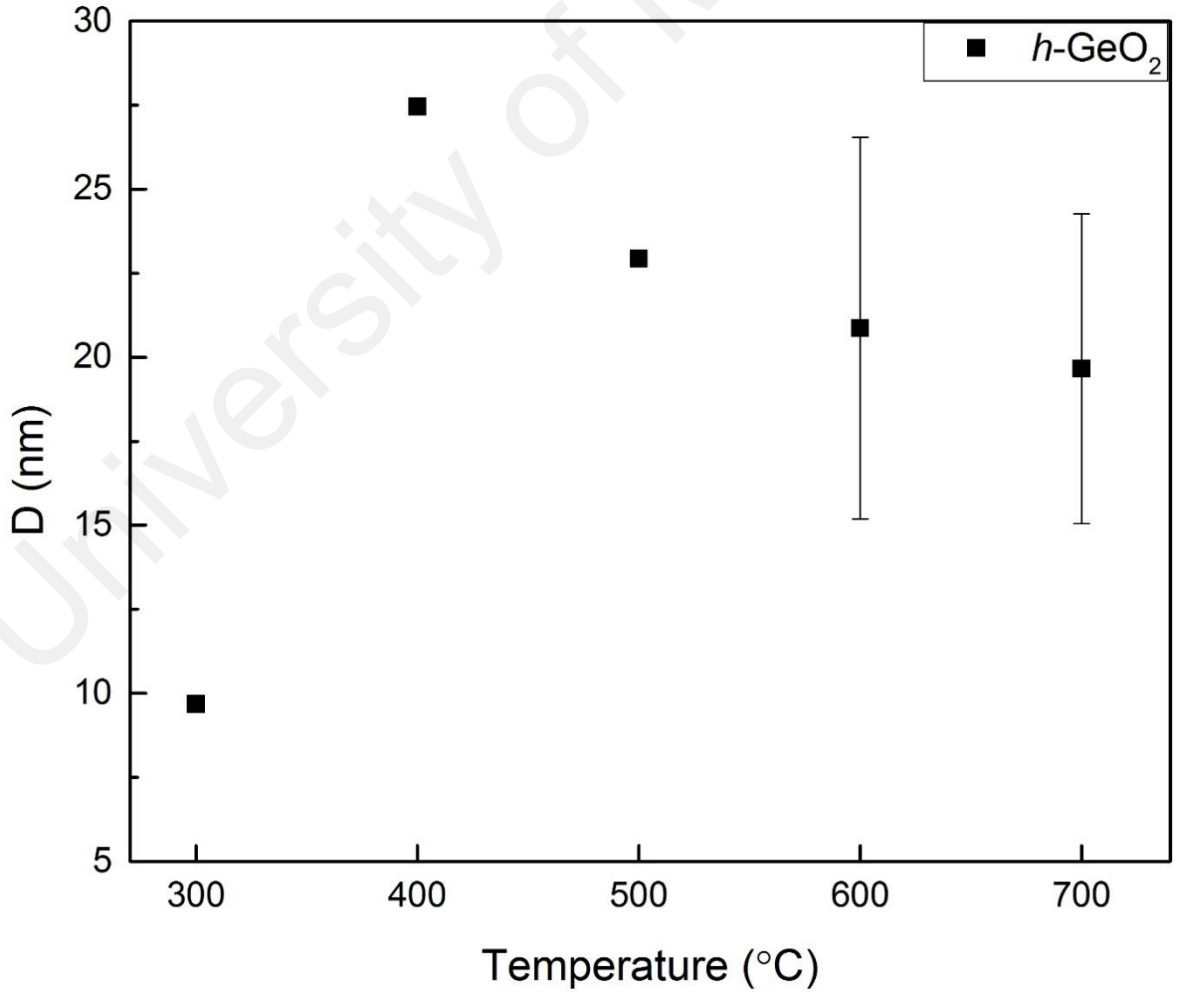

Figure 4.3: Crystallite size of *h*-GeO_2 at various temperatures.

For W-H analysis, Fig. 4.4 shows the W-H plot of the *h*-GeO_2 for the thermal oxidized samples at 600 °C and 700 °C. For 300 °C to 500 °C samples, the analysis cannot be done due to the insufficient peaks of the *h*-GeO_2. Also, the W-H analysis is not done for *c*-Sm_2O_3 and $Sm_2Ge_2O_7$ as well owing to the same reason as mentioned above. In W-H analysis, the results are plotted in $\beta_{hkl}\ cos\theta$ against $4\ sin\theta$, where β_{hkl} is the total broadening for crystallite size and microstrain. From Eq. 3.7, the equation can actually be expressed in straight line equation, which is as shown in Eq. 4.1,

$$y = mx + c \qquad \text{(Equation 4.1)}$$

where y corresponds to $\beta_{hkl}\ cos\theta$, m is the gradient of the plot which is corresponding to microstrain (ε), x corresponds to $4\ sin\theta$ and c is the y-intercept which is corresponding to $\frac{K\lambda}{D}$, therefore the microstrain (ε) and the crystallite size (D) of the thin film grown can be calculated through the W-H plot. From Fig.4.4, ε and D calculated from the plot for 600 °C and 700 °C samples, and the results are tabulated in Table 4.1.

Table 4.1: ε and D for 600 °C and 700 °C samples

Temperature (°C)	y-intercept of W-H plot	Gradient of W-H plot	$D = \frac{K\lambda}{y-intercept}$ (nm)	ε
600	0.00319	0.00229	43.46	0.00229
700	0.00453	0.00184	30.61	0.00184

As compared with the crystallite size calculated by the Debye-Scherrer equation, the results from the W-H plot show the same trend, which the crystallite size of *h*-GeO_2 decreases as the temperature increases from 600 °C to 700 °C. Also, the microstrain of *h*-GeO_2 decreases as well as the temperature decreases.

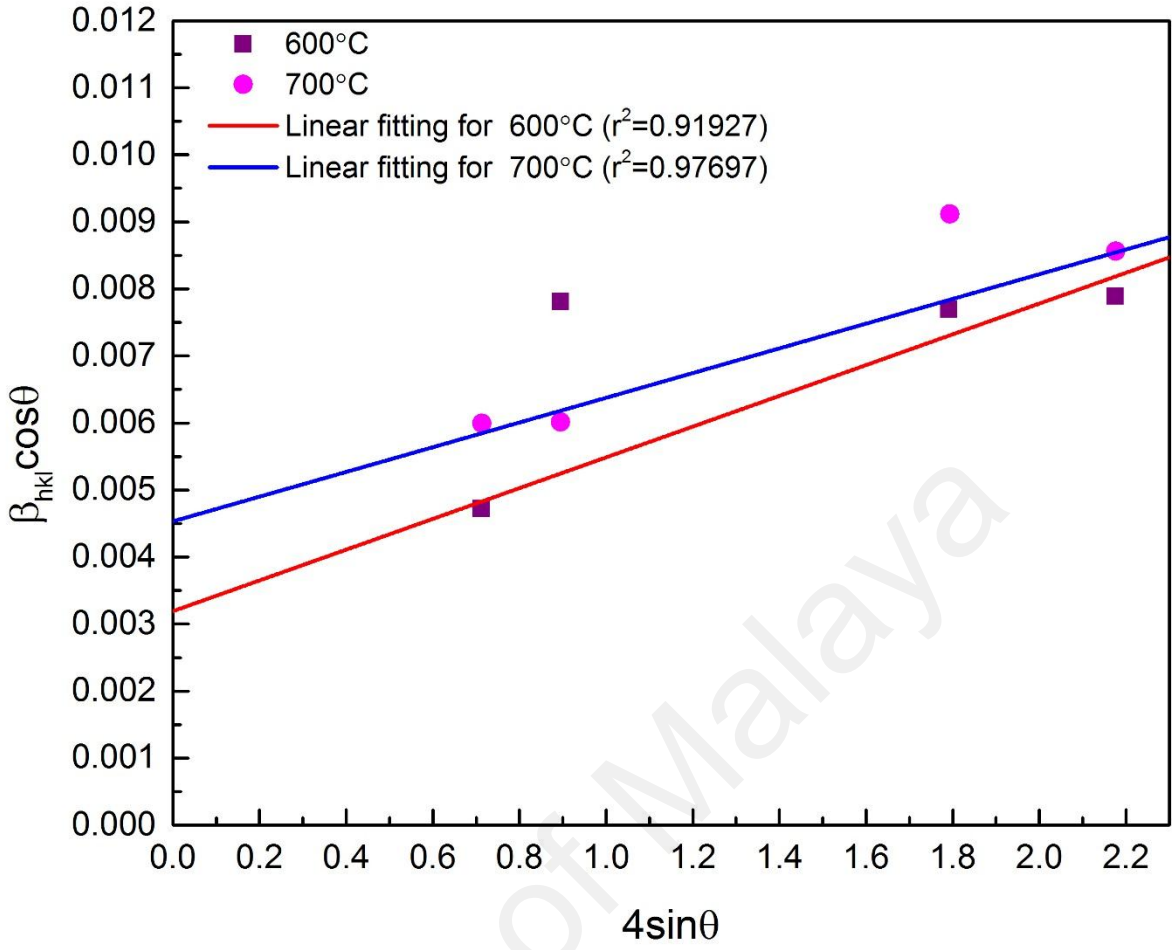

Figure 4.4: W-H plot of *h*-GeO_2 for thermal oxidized samples at 600 °C and 700 °C.

4.3 FT-IR spectroscopy analysis

For FT-IR spectroscopy analysis, the results are plotted in a graph as shown in Fig. 4.5 and hence the chemical bonds involved in the thin film can be detected. The graph is plotted on transmittance with arbitrary unit against the wavenumber (cm^{-1}) in the range of 400 cm^{-1} to 2000 cm^{-1}. In this research project, the major interest is to focus on the growth of Sm_2O_3 and GeO_2, therefore primary concerns are put on the Sm-O and Ge-O bonds. Based on previous findings, the FT-IR spectrum for pure Sm_2O_3 crystal shows significant peaks at 665 cm^{-1}, 730 cm^{-1}, 860 cm^{-1} and 975 cm^{-1}, which describe

the stretching vibration of the Sm-O bond(Gao et al., 2003). Sone et al. stated that the modes for Sm-O are found at 419 cm^{-1}, 475 cm^{-1}, and 539 cm^{-1} (Sone, Manikandan, Gurib-Fakim, & Maaza, 2015). Besides that, Goh et al. mentioned that Sm-O bands can be found at the wavenumber 409 cm^{-1}, 418 cm^{-1}, 432 cm^{-1}, 439 cm^{-1}, 473 cm^{-1}, 482 cm^{-1} and 502 cm^{-1} (Goh et al., 2016). On the other hand, Ge-O vibration modes can be found at 518 cm^{-1}, 589 cm^{-1}, 903 cm^{-1}, 927 cm^{-1} and 959 cm^{-1} (Lei et al., 2017).

From Fig. 4.5, for 300 °C sample, Sm-O peak is detected at 416 cm^{-1}, Ge-O peaks are detected at 509 cm^{-1}, 580 cm^{-1}, 876 cm^{-1} and 960 cm^{-1}. For 400 °C and 500 °C samples, Sm-O bands are found at 416 cm^{-1} and 444 cm^{-1} while Ge-O are detected at 509 cm^{-1}, 580 cm^{-1}, 840 cm^{-1}, 876 cm^{-1}, 913 cm^{-1} and 960 cm^{-1}. For 600 °C, small peaks of Sm-O can be observed at 416 cm^{-1} and 444 cm^{-1} as in 400 °C and 500 °C samples, whereas Ge-O shows bands at 580 cm^{-1}, 840 cm^{-1}, 913 cm^{-1} and 960 cm^{-1}. Lastly for 700 °C sample, the spectrum shows only the presence of Ge-O peaks in the range of 500 to 1000 cm^{-1} with very high intensity.

From the results, it is clearly shown that at 400 °C, there shows no large peak in the range of 500 to 1000 cm^{-1} which corresponds to the Ge-O bond, meanwhile a relatively large peak is observed for the other samples and the peaks are shifted to the left as the temperature increases from 500 °C to 700 °C. The large peak of Ge-O is shifted to a smaller wavenumber side and increased in peak intensity owing to the growth in mass of GeO_2 as the temperature increases. As the mass increases, the vibration frequency decreases and thus results in a smaller wavenumber and larger peak intensity. When comparing the 400 °C and 500 °C samples, the intensity of the peak for Sm-O is higher in 500 °C sample. Overall, as the temperature increases from 300 °C to 700 °C, the intensity for the Ge-O peaks increases, and the intensity of Sm-O peaks increases from 300 °C to 500 °C, then decreases above 500 °C. As discussed in the XRD analysis, there shows no presence of Sm_2O_3 in the FT-IR analysis as well for

700 °C sample, meaning that 700 °C is not suitable to grow the thin Sm_2O_3 oxide film on Ge substrate.

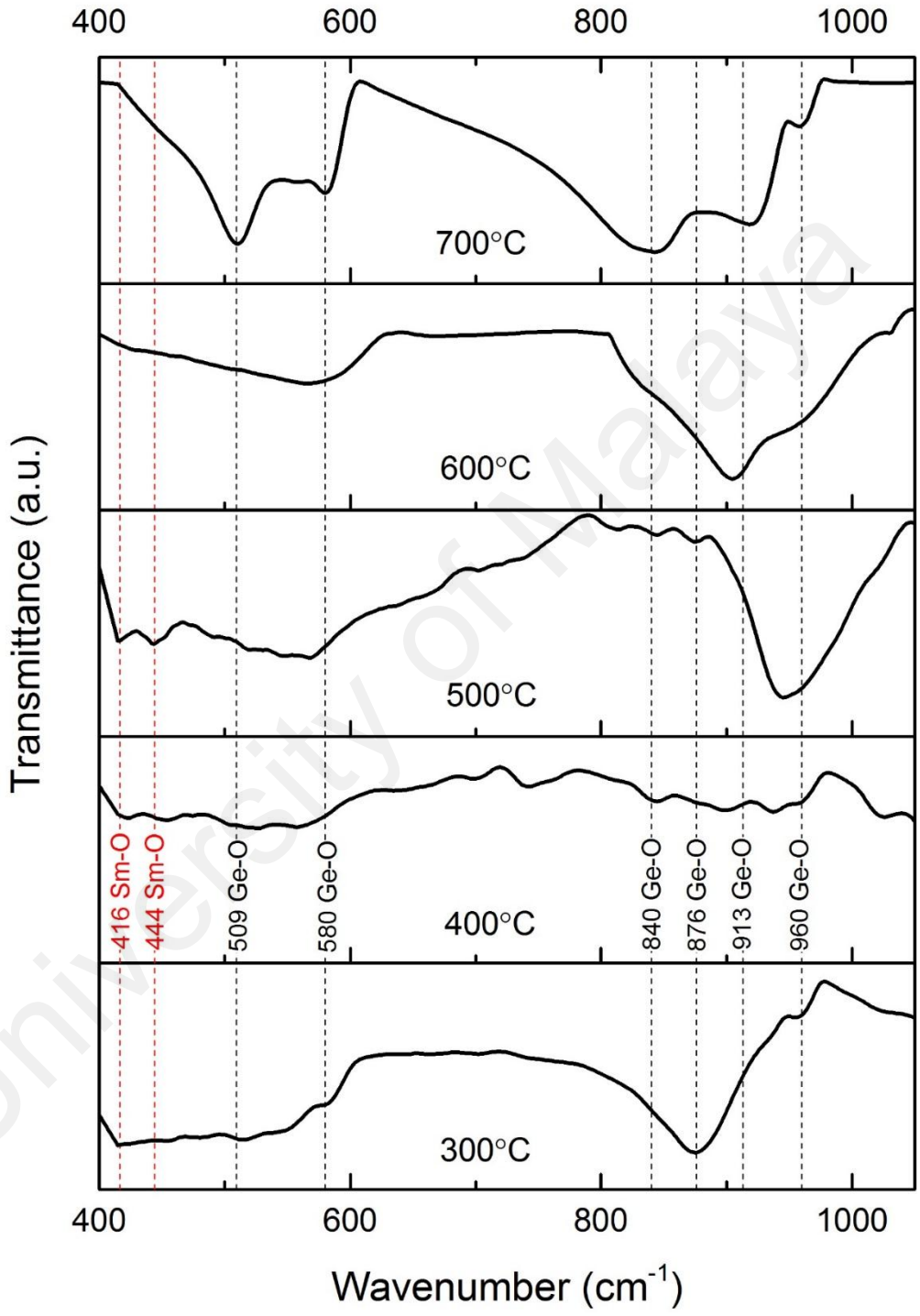

Figure 4.5: FT-IR spectrum of thermal oxidized samples for various temperatures.

CHAPTER 5: CONCLUSION AND FUTURE RECOMMENDATION

5.1 Conclusion

In this entire research project, Sm_2O_3 film was successfully grown on Ge substrate by thermal oxidation process and the effect of oxidation temperature on the thin oxide film grown was studied. Then the physical properties of the thin oxide film were determined. Sm metal was sputtered onto the Ge substrate, and thermally oxidized at various temperatures, from 300°C to 700°C for 15 minutes. Characterization methods of XRD and FT-IR analysis were carried out to study the physical properties of the thin oxide film. From XRD analysis, GeO_2 started to grow at 300°C, and grow intensively starting at 600°C. By calculating the crystallite size of GeO_2 by Debye-Scherrer equation, it showed the smallest crystallite size at 300°C, and a sharp increase at 400°C, followed by a decreasing trend after 400°C to 700°C. After W-H analysis for GeO_2 at 600°C and 700°C, the results showed that the crystallite size and the microstrain of GeO_2 decreases as the temperature increases from 600°C to 700°C. For Sm_2O_3 thin film, the intensity shows the highest value at 500°C. From FT-IR analysis, Sm-O bond(s) was found for 300°C, 400°C, 500°C and 600°C samples. Among them, 500°C sample shows the highest peak intensity for Sm-O bonds. For 700°C sample, Ge-O peaks showed a very high intensity and no Sm-O bond was detected for 700°C sample. Based on these two analysis, 500°C can be said to be the optimum oxidation temperature for the growth of Sm_2O_3 thin film on Ge substrate.

5.2 Future recommendation

To further proceed with the thin film analysis, other characterization methods have to be done such as Raman spectroscopy to identify molecules and study chemical bonding, X-ray photoelectron spectroscopy (XPS) to analyze the surface chemistry and binding energy of electronic states, TEM to observe the surface roughness, to calculate the true crystallite size and the thickness of the thin film grow, and various electrical tests to test for the capacitance, breakdown current and breakdown electric field of the oxide film. By further undergoing the characterization processes as mentioned above, more information about the Sm_2O_3 thin film can be known. Last but not least, as a recommendation for future research, the thermal oxidation method of Sm_2O_3 on Ge substrate can be replaced by other deposition methods such as ALD since ALD method can produce a superior thin oxide film with a very low level of impurities.

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