

**DEPOSITION AND CHARACTERIZATION OF  
GERMANIUM NITRIDE FILM USING DIFFERENT  
THERMAL NITRIDATION TEMPERATURE**

**LOW YAN JIE**

**FACULTY OF ENGINEERING  
UNIVERSITY OF MALAYA  
KUALA LUMPUR**

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THERMAL NITRIDATION TEMPERATURE**

**LOW YAN JIE**

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Name of Candidate: **LOW YAN JIE**

(I.C/Passport No:

Matric No: **KQJ170002**

Name of Degree: **MASTER IN MATERIALS ENGINEERING**

Title of Project Paper/Research Report/Dissertation/Thesis (“this Work”):

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FILM USING DIFFERENT THERMAL NITRIDATION TEMPERATURE**

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## ABSTRACT

This study is aimed at investigating the effect of thermal nitridation temperature on the growth of germanium nitride ( $\gamma$ -Ge<sub>3</sub>N<sub>4</sub>) thin film and its effectiveness as a buffer layer to suppress the growth of unwanted germanium oxide (GeO<sub>2</sub>) interfacial layer. The  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> films were grown on germanium substrate (Ge) by thermally nitriding Ge with nitrogen (N<sub>2</sub>) gas purging for 15 minutes at 400, 500 and 600°C. The temperature dependence of the growth of  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> films under pure N<sub>2</sub> gas purge was studied profoundly through X-ray diffraction (XRD) and Fourier transform infrared (FTIR) characterization. The physical, chemical and compositional properties of 400, 500 and 600°C thermally nitrided Ge samples were analyzed through the resulting XRD and FTIR spectra. The resulting XRD spectra give information on the intensity of  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> and *t*-GeO<sub>2</sub> phases, microstrain embedded in each phase, and crystallite size of the phases by means of Debye-Scherrer equation and Williamson-Hall (W-H) analysis. The intensities of  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> phases were found to first increase from 400°C and reach a peak at 500°C, gradually declining thereafter at 600°C. This suggests that the optimum growth of  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> phases is at 500°C as the  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> phases are appeared to be unstable at 400 and 600°C. The  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> was determined to exhibit the largest crystallite size and highly homogeneous size distribution at 500°C indicating the highly uniform growth rate at 500°C. Tensile microstrain embedded in  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> layer was only observed at the highest growth rate temperature, 500°C. The tensile microstrain indicates the  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> phase islands has grown into a uniform film by forming grain boundary. The compressive microstrain in 400 and 600°C  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> layer was expected to be attributed to the disruption of  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> thin film growth by formation of *t*-GeO<sub>2</sub>. Based on the FTIR results, the 500°C nitrided sample was found to have a substantial number of

Ge-N characteristic peaks consecutively over the wavenumber range of 400 to 1300  $\text{cm}^{-1}$  and a very small number of low intensity peaks which are indicative of Ge-O bond. Unlike 500°C nitrated sample, relatively high intensity peaks of Ge-O bond are observed in the spectra of 400 and 600°C nitrated samples. Broadly translated, the result findings indicate 500°C as the optimal thermal nitridation temperature of  $\gamma\text{-Ge}_3\text{N}_4$  thin film growth.

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## ABSTRAK

Kajian penyelidikan ini bertujuan untuk menguji pengaruh suhu penitridaan terma terhadap pertumbuhan filem nipis germanium nitrida ( $\gamma\text{-Ge}_3\text{N}_4$ ) dan keberkesanannya sebagai lapisan penimbal untuk menyekat pertumbuhan lapisan interfacial germanium oksida ( $\text{GeO}_2$ ) yang tidak dikehendaki. Filem  $\gamma\text{-Ge}_3\text{N}_4$  telah ditumbuh di atas substrat germanium (Ge) melalui proses penitridaan terma dengan mengalirkan gas nitrogen ( $\text{N}_2$ ) selama 15 minit pada 400, 500 dan 600°C. Pergantungan pertumbuhan filem  $\gamma\text{-Ge}_3\text{N}_4$  terhadap suhu di bawah pengaliran gas  $\text{N}_2$  telah dipelajari dengan mendalam dengan menggunakan analisis Pembelauan Sinar-X (XRD) dan spektroskopi inframerah transformasi Fourier (FTIR). Ciri-ciri fizikal, kimia dan komposisi bagi sampel-sampel 400, 500 dan 600°C yang telah dinitridasi dianalisis melalui hasil spektrum XRD dan FTIR. Spektrum XRD yang dihasilkan memberikan maklumat mengenai intensiti fasa  $\gamma\text{-Ge}_3\text{N}_4$  dan  $t\text{-GeO}_2$ , mikro-terikan yang dibenamkan dalam setiap fasa, dan saiz kristal fasa dengan mengaplikasikan persamaan Debye-Scherrer dan analisis Williamson-Hall (W-H). Intensiti fasa  $\gamma\text{-Ge}_3\text{N}_4$  didapati meningkat pada awal dari 400°C dan mencapai puncak pada 500°C, secara beransur-ansur merosot selepas itu pada 600°C. Ini menunjukkan bahawa 500°C merupakan suhu optimum untuk pertumbuhan fasa  $\gamma\text{-Ge}_3\text{N}_4$  kerana fasa  $\gamma\text{-Ge}_3\text{N}_4$  kelihatan tidak stabil pada 400 dan 600°C.  $\gamma\text{-Ge}_3\text{N}_4$  juga didapati mempunyai saiz kristal yang terbesar dan distribusi saiz yang sangat homogen pada 500°C. Ini bermakna bahawa pertumbuhan fasa  $\gamma\text{-Ge}_3\text{N}_4$  mempamerkan kadar pertumbuhan yang sangat seragam pada 500°C. Selain itu, juga didapati bahawa lapisan  $\gamma\text{-Ge}_3\text{N}_4$  hanya mempunyai mikro-terikan tegangan pada suhu penitridaan terma yang menunjukkan kadar pertumbuhan tertinggi, 500°C. Mikro-terikan tegangan ini melambangkan bahawa fasa  $\gamma\text{-Ge}_3\text{N}_4$  yang kecil telah berkembang

menjadi filem yang seragam melalui pembentukan sempadan bijian. Di samping itu, mikro-terikan mampatan yang dilihat pada lapisan 400 dan 600°C  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> dijangka disebabkan oleh gangguan pertumbuhan filem nipis  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> oleh pembentukan *t*-GeO<sub>2</sub>. Berdasarkan hasil spektra FTIR, sampel 500°C didapati mempunyai banyak karakteristik puncak bagi ikatan Ge-N secara berturut-turut pada daerah 400 hingga 1300 cm<sup>-1</sup> dan karakteristik puncak bagi ikatan Ge-O yang berjumlah kecil dan berintensiti rendah. Sebaliknya, banyak karakteristik puncak bagi Ge-O yang berintensiti tinggi diperhatikan dalam spektra bagi sampel-sampel 400 dan 600°C. Secara amnya, hasil-hasil penemuan ini menunjukkan bahawa 500°C ialah suhu penitridaan terma yang optimum untuk pertumbuhan filem  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub>.

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## LIST OF SYMBOLS AND ABBREVIATIONS

$\kappa$	:	Dielectric constant
$\varepsilon$	:	Microstrain
$\beta_c$	:	Crystallite size peak broadening
$\beta_s$	:	Microstrain peak broadening
$\beta_t$	:	Total peak broadening
$\mu_e$	:	Electron mobility ( $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ )
$\mu_h$	:	Hole mobility ( $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ )
$\lambda$	:	Wavelength (nm)
$\theta$	:	Diffraction angle ( $^\circ$ )
$a$	:	Lattice constant (nm or $\text{\AA}$ )
$D$	:	Crystallite size
$D_{it}$	:	Interface trap density ( $\text{eV}^{-1} \text{cm}^{-2}$ )
$d$	:	Interplanar spacing (nm)
$E_g$	:	Bandgap energy (eV)
$h, k, l$	:	Miller indices
$I_{on}$	:	Saturation drive current (A)
$J_g$	:	Leakage current density ( $\text{A cm}^{-2}$ )
$k$	:	Shape factor constant
$n$	:	Integer (1, 2, 3...)
$V_{DD}$	:	Power supply voltage
ALD	:	Atomic layer deposition
ATR	:	Attenuated total reflection
CET	:	Capacitance equivalent oxide thickness
CMOS	:	Complementary metal oxide semiconductor



CVD	:	Chemical vapor deposition
EOT	:	Equivalent oxide thickness
FET	:	Field-effect transistor
FinFET	:	Fin field effect transistor
FTIR	:	Fourier transform-infrared spectrometry
HPGe	:	High-purify Ge
IC	:	Integrated circuit
I/O	:	Maximum input/output pins
ITRS	:	International technology roadmap for semiconductors
LT-Si	:	Low-temperature Si
MOS	:	Metal oxide semiconductor
$N_C$	:	Effective density of states in conduction band ( $\text{cm}^{-3}$ )
NMOS	:	N-type metal oxide semiconductor
PMOS	:	P-type metal oxide semiconductor
PSC	:	Polymer solar cell
SCE	:	Short channel effect
S/D	:	Source/drain
sSOI	:	Strained silicon-on-insulator
$T_m$	:	Melting temperature ( $^{\circ}\text{C}$ )
TEM	:	Transmission electron microscopy
UHV	:	Ultra-high vacuum
W-H	:	Williamson-Hall method
XRD	:	X-ray diffraction/diffractometer

## CHAPTER 1: INTRODUCTION

### 1.1 Theoretical Background

Semiconductor industry plays a crucial role in this 21<sup>st</sup> century development of all nations in the world (Ferry, 2013). Every country is non-stop investing time, money and human resource in development of semiconductor industry. Until today, its evolution is still actively happening. Nowadays, electronics are strongly dependent of sheer computation power which has brought about to combined form and function as the key driver of large consumer markets. People believe that the way society interacts with each other and the way society acts in its surroundings is going to face major changes over the next decades due to the demand for small, portable and omnipresent electronics equipped with advanced functionality. In order to keep abreast of such fast and ceaseless evolutionary changes, continuous improvements in electronic devices industry are necessary to provide the unique and particular functionality in the compliant form factor demanded accordingly. Especially in conventional high performance low power electronics for informatics as well as absolutely new device technologies based emerging electronic materials and novel integration methods. Atomic, molecular, organic, atomic layer two-dimensional semiconductors, III-V (groups 13–15 semiconductor materials), and metal oxide based transistors, optronics, and gas sensors are the representative examples of the new electronic materials and devices (O. Madelung, 2012).

As new findings are being uncovered and new concepts are being verified and developed by scientists and researchers, a close coupling of technology and metrology development is also needed for manufacturing and innovation of emerging electronic

devices. Stepping into 2018, each of us who is constantly in the science and technology society are clear about that micro-electronics' as well as nano-electronics' astonishingly rapid growth and evolution from the conventional electronics have boggled everyone minds (Ferry, 2013). They have also genuinely revolutionized our ordinary day-to-day lifestyle. Underlying the electronics revolution has been a remarkable evolutionary trend known as Moore's Law. Moore's Law introduced by G. Moore in 1965 has come to bring us a conviction of incredible and seemingly bottomless capacity for exponential growth in electronics. It started out as a simple observation that the number of components, for example transistor, integrated into a semiconductor integrated circuit (IC) doubled each year for the first few years of the industry, which means the size of the components must be scaled down to reach a size so small that it would be possible to obey the trend of Moore's Law by integrating more components in IC (Kish, 2002; S. E. Thompson & Parthasarathy, 2006). Accordingly, the transistor has been continuously scaling down into sub-micron and then to nanoscale region for the requirement of higher compactness and speed. However, the pace of scaling down has been impeded because of some contrary issues related to excessive power consumption and heat generation in IC emerging when it reaches certain limit of size reduction in nanoscale (Chaudhry, 2012). Nevertheless, in the past 53 years, Moore's Law observation has expanded far beyond its realms of original intentions, with the risk of losing its inherent meaning and usefulness (Bondyopadhyay, 1998; Mack, 2011).

According to the 2015 International Technology Roadmap for Semiconductors (ITRS), a collaborative report released and published in 2016 by the Semiconductor Industry Association (SIA), it is predicted that the transistor could stop downscaling in 2020 (Gargini, 2017). Thus, the semiconductor industry is seeking for alternate performance boosters, in particular by coming out with new materials and new device architecture in lieu of traditional and standard silicon Complementary Metal Oxide

Semiconductor (CMOS) technology. It took a number of research groups and centers nearly a decade in conducting research and development with the aim of being well-prepared with other promising options and alternatives to stick at scaling during such a circumstances. However, some traditional scaling rules like reduction in thickness of gate oxide can no longer be practical and cannot be applied as an effective solution due to the rapid increase in power consumption and the leakage current of downscaled transistors (Kamata, 2008; Nirmal, 2012; Shauly, 2012; Suehle et al., 2001). The alternative approaches are by introducing high dielectric constant ( $\kappa$ ) dielectrics, low  $\kappa$  interconnects, replacement of bulk silicon with strained silicon-on-insulator (sSOI), high mobility channel material such as germanium (Ge), gallium arsenide (GaAs) and grapheme, and non-planar CMOS device structures, for example, Fin Field Effect Transistor (FinFET) (Houssa, 2003).

When the downscaling has evidently reached the fundamental material limits, particularly for gate oxide, further downscaling can be only realized through introduction of new dielectric materials which possess higher  $\kappa$  values. For example, when the thickness of the standard silicon dioxide ( $\text{SiO}_2$ ) based gate dielectrics is reduced below the tunneling limit, the gate leakage current will be increased tremendously. In addition, an oxide thickness of 1.5 nm has been analyzed at 1.5 V and the results demonstrate that the leakage current density ( $J_g$ ) would be  $100\text{A}/\text{cm}^2$  which is manifestly undesirable intended for low power applications (Allan et al., 2002). Accordingly, thicker dielectric layers are physically required in order to avoid tunneling currents. As the thickness of gate dielectrics is physically increased, a material with high  $\kappa$  is highly required by the transistor so that its electrical characteristics can be maintained. In aiding and facilitating the purpose of achieving high  $\kappa$  gate stack, a synergistic effect of high  $\kappa$  dielectrics and buffer layer is crucial for suppressing the

growth of low  $\kappa$  interfacial layer and resulting in a reduction in capacitance equivalent oxide thickness (CET) and gate current leakage (W.-C. Wang et al., 2016).

## 1.2 Problem statement

As the ICs are getting smaller and smaller to meet the requirements of IC design and development, reduction of thickness of the gate oxide layer has been considered desirable in the interest of engineers (Haukka, Shero, Pomarede, Maes, & Tuominen, 2004). Accordingly, ultra-thin gate oxides of MOS structures have been modeled with the purpose of reducing thickness of gate oxide layer. Ultra-thin gate oxides are necessary to enhance the performance of CMOS devices in consequence of continuous downscaling of the critical dimensions of transistor (W.-C. Wang et al., 2016). Nevertheless, high defect densities such as pinholes and charge trapping states are found in the ultra-thin gate oxides. It has been also found that ultra-thin gate oxides are highly susceptible to hot carrier injection effects. Leakage currents across the gate dielectrics due to high defect densities and rapid breakdown of device due to hot carrier are undesirable for IC design (Haukka et al., 2004). Such high leakage current is affirmed to be the main cause that contributed to power dissipation of CMOS circuits with reduced threshold voltage, channel length, and gate oxide thickness. Thus, reducing thickness of gate oxide layer is no longer a promising solution.

Based on the issues arising from downscaling, it is believed that the conventional silicon dioxide ( $\text{SiO}_2$ ) gate oxide has reached its fundamental limit, resulting in detectable leakage current and thus power dissipation of the devices (Wilk, Wallace, & Anthony, 2001). Accordingly, many efforts have been made and various approaches have been intensively and extensively investigated. Suppositiously, integrating high dielectric permittivity materials as gate oxide layer into the gate

dielectric instead of  $\text{SiO}_2$  has great potential to open the door to further device downscaling and meet the requirement of low gate leakage current. Some newly emerging high  $\kappa$  materials have been extensively investigated experimentally, for example,  $\text{Al}_2\text{O}_3$ ,  $\text{HfO}_2$ , and  $\text{ZrO}_2$ .  $\text{ZrO}_2$  is considered to be one of the potential alternatives for the conventional  $\text{SiO}_2$  gate oxide because of its high  $\kappa$ . Besides, improving carrier mobility in the channel region is also one of the promising solutions by increasing the saturation current.

Germanium (Ge) is an attractive material for high performance MOSFET channels because it has higher intrinsic carrier mobility than Si, about three times and four times for electrons and holes respectively. Therefore, it has been considered as one of the promising candidate to substitute the conventional silicon (Si) substrate. Its higher intrinsic carrier mobility is attributable to its higher low-field carrier mobility and smaller mobility band gap for supply voltage scaling (Kim, Chui, Saraswat, & McIntyre, 2003). However, Ge has not been widely applied to replace Si in CMOS technology due to the existence of substandard low  $\kappa$  Ge native oxide, germanium oxide ( $\text{GeO}_2$ ) interfacial layer. A low  $\kappa$  Ge native oxide interfacial layer is formed spontaneously due to oxygen diffusion during the deposition of high  $\kappa$  metal oxide layer on the Ge substrate and thermal treatment. The naturally grown  $\text{GeO}_2$  interfacial layer not only has undesirable physical and electrical properties but also induces high surface states in MOS stack and tends to become the recombination-generation centers as the band gap energy of Ge is small (Oh & Campbell, 2010). Most crucial drawback of having low  $\kappa$   $\text{GeO}_2$  is that, the effective dielectric constant will be reduced.

In order to overcome the as-mentioned problem arising from the grown low  $\kappa$   $\text{GeO}_2$  interfacial layer, introduction of a stable buffer layer between the high  $\kappa$  oxide layer and Ge substrate is necessary to suppress the growth of low  $\kappa$  germanate interfacial layer, and thus leading to both enhancement of effective dielectric constant

and reduction in capacitance equivalent thickness (CET) or equivalent oxide thickness (EOT). Even though some research studies on high  $\kappa$ /Ge gate stacks with various interfacial layers such as germanium nitride and oxynitride have been done, however, their roles as a buffer layer in suppressing the low  $\kappa$  germanate interfacial layer were not clearly defined (Maeda, Nishizawa, Morita, & Takagi, 2007; Oshima et al., 2008; Otani et al., 2007; S. Takagi et al., 2007). It has been also reported that nitrogen incorporation during the deposition can effectively suppress the thickness of the interfacial layer and leakage current density ( $J_g$ ) but there is no detailed discussion on the binding states of Ge in the buffer layer and the reliability of the buffer layer on interfacial layer suppression (Dai et al., 2013; Jeon, Choi, Seong, & Hwang, 2001). In this study, germanium nitride ( $\text{Ge}_3\text{N}_4$ ) is grown on the Ge substrate through nitrogen incorporation during deposition and thermal treatment process. Optimum temperature for growth of  $\text{Ge}_3\text{N}_4$  on Ge substrate will be investigated. As there is no temperature dependence study of behavior of  $\text{Ge}_3\text{N}_4$  buffer layer in suppressing native interfacial oxide layer, the optimum effective temperature of  $\text{Ge}_3\text{N}_4$  buffer layer for  $\text{GeO}_2$  interfacial layer suppression will be also investigated. Furthermore, the binding states of Ge in the  $\text{Ge}_3\text{N}_4$  layer and the reliability of  $\text{Ge}_3\text{N}_4$  layer will be examined by subjecting  $\text{Ge}_3\text{N}_4$  layer grown Ge substrate to a series of characterization and analysis.

### **1.3 Research Objectives**

The primary objective of this study is to grow germanium nitride thin films on germanium substrate by means of direct thermal nitridation reaction with high purity nitrogen gas ( $\text{N}_2$ ) at temperatures ranging from 400 to 600°C. This research is not only aimed at achieving the previously as-mentioned primary objective but also the following key objectives.

1. To investigate the effects of direct thermal nitridation in nitrogen gas ambient at different nitriding temperatures under fixed durations on the growth of germanium nitride thin films on germanium substrate.
2. To determine the effect of thermal nitriding temperature on the surface morphology, composition, and electrical properties of germanium nitride thin films deposited on germanium substrate.
3. To study the role of germanium nitride as buffer layer to suppress the formation of unwanted germanium oxide layer on germanium substrate upon thermal nitridation.

#### **1.4 Scope of study**

This study is strikingly different from what has been done by researchers. Instead of using nitrogen-containing gas such as ammonia gas ( $\text{NH}_3$ ) and nitric oxide gas ( $\text{NO}$ ), pure  $\text{N}_2$  gas is used as the source of nitrogen radicals to form nitridated layer on germanium substrate. In this study, germanium nitride thin films are grown on germanium substrate by means of thermal nitridation reaction. Before germanium substrates are subjected to thermal nitridation, germanium substrates are cleaned by dilute hydrofluoric acid (HF) dipping and dionized water (DI) rinsing and followed by drying. The cleaned germanium substrates are subsequently proceeded to the furnace for thermal nitridation at different nitriding temperature ( $T = 400, 500, 600^\circ\text{C}$ ) under constant  $\text{N}_2$  gas flow rate of 150cc/min with constant pressure of 1atm for constant nitridation time of 15minutes. The nitridated germanium substrates of different nitriding temperatures are subjected to a series of characterization techniques for both quantitative and qualitative analysis.

The physical properties of the nitridated germanium substrates are probed and measured by using X-ray diffraction (XRD) and Fourier-transform infrared



spectroscopy (FTIR). With XRD techniques, the structure of samples is elucidated and the conformational properties are explored by referring to the resulting XRD patterns or spectra as the XRD patterns carry the characteristic of chemical composition and phase present in the samples. Apart from that, film thickness as well as the roughness can also be deduced from the XRD patterns. Besides, FTIR is performed to obtain the transmittance or absorbance spectra of  $\text{Ge}_x\text{N}_y$  thin films deposited on Ge substrate for evaluating the binding states of Ge in the  $\text{Ge}_3\text{N}_4$  thin films.

## 1.5 Thesis Outline

The structure of this research is formulated according to the hourglass model to give better understanding to the readers. The research starts off broad by taking the readers into research study, then turns narrow from a very general overview of the topic to the specific thesis statement under examination through discussion on research findings and relationships to previous work, and then broadens again towards the bottom through the applications and wider implications of the research work. Accordingly, this research is mainly comprised of six chapters. Starting with chapter one, general introduction including background, current trends and issues of thin film technology in semiconductor industry, problem statement, research objectives, and scope is elaborated. In chapter two, literature review on a brief introduction about the obstacles faced on the path of MOSFET downscaling and the concept of gate leakage is presented, followed by thoroughly explanation of the newly emerging Ge semiconductor materials, limitations of Si substrate, and enhancement of Ge electrical and interfacial properties. Then Ge oxide interfacial layers grown in high  $\kappa/\text{Ge}$  system are discussed by including some findings from the relevant previous studies, and lastly the thermal nitridation method using  $\text{N}_2$  as source gas in depositing  $\text{Ge}_3\text{N}_4$  buffer layer

on Ge is discussed. In chapter three, methodology and metrologies adopted in the research are discussed in detailed. In chapter four, results and discussion of the nitridated germanium samples are well-illustrated with the aid of graphs, figures, and tables. In last chapter - chapter six, the research work is not merely concluded with summary of the main points covered and restatement of research problem, but also with recommendation for future research.

University of Malaya

## CHAPTER 2: LITERATURE REVIEW

### 2.1 Introduction

The continuous development in IC density and speed is at the heart of the rapid growth of electronics. Today, the electronic industry has undoubtedly become second to none among other industries either in terms of output or in terms of employment in country all over the world (Hu, 1993). The significant evolution brought about by electronics in economic, social as well as political development over the world is believed to be continuously moving on. The evolution acts as a formidable driving force which keeps pushing forward the IC integration density and speed in a continual improvement process. The improvement in circuit complexity and speed are along with the MOSFET scaling (Dennard, Gaensslen, Rideout, Bassous, & LeBlanc, 1974; Masuda, Nakai, & Kubo, 1979). The past trend of MOSFET scaling over years is shown in Fig. 2.1 (Yeo, King, & Hu, 2003). Based on Fig. 2.1, the past trend of transistor scaling can be roughly summarized in the following manner:

- Every three years, a new generation of technology was introduced.
- The memory chip density was increased by four while the logic circuit density was increased by two to three for every generation of technology.
- Every six years, the feature size of device was decreased by two while the transistor current density, circuit speed or clock rate, area and current dissipation of chip, and maximum input/output (I/O) pins were increased by two.

The aim and challenge of MOSFET scaling are clearly defined as a continuous increase in IC density and speed which is driven by inter-corporation competition,

customer demand and it is also treated as a test for the limit of human ingenuity. Generally, the aims and challenges on the path of MOSFET scaling can be sorted into two aims and two sets of limits. First, the MOSFET scaling is aimed at increasing the transistor current to accelerate the charging and discharging parasitic capacitances by having a short channel and high gate oxide field since the inversion layer charge density is strongly proportional to the gate oxide field. Second, the transistor scaling is intended for reducing size of IC in order to increase the packing density which requires smaller channel length and width. Besides, there are two major limitations which have to be taken into consideration upon downscaling. The leakage current when the transistor is off must not exceed the acceptable range, and the reliability lifetime such as hot-carrier, oxide, metallization reliabilities and failure rate must be also controlled within the acceptable range.

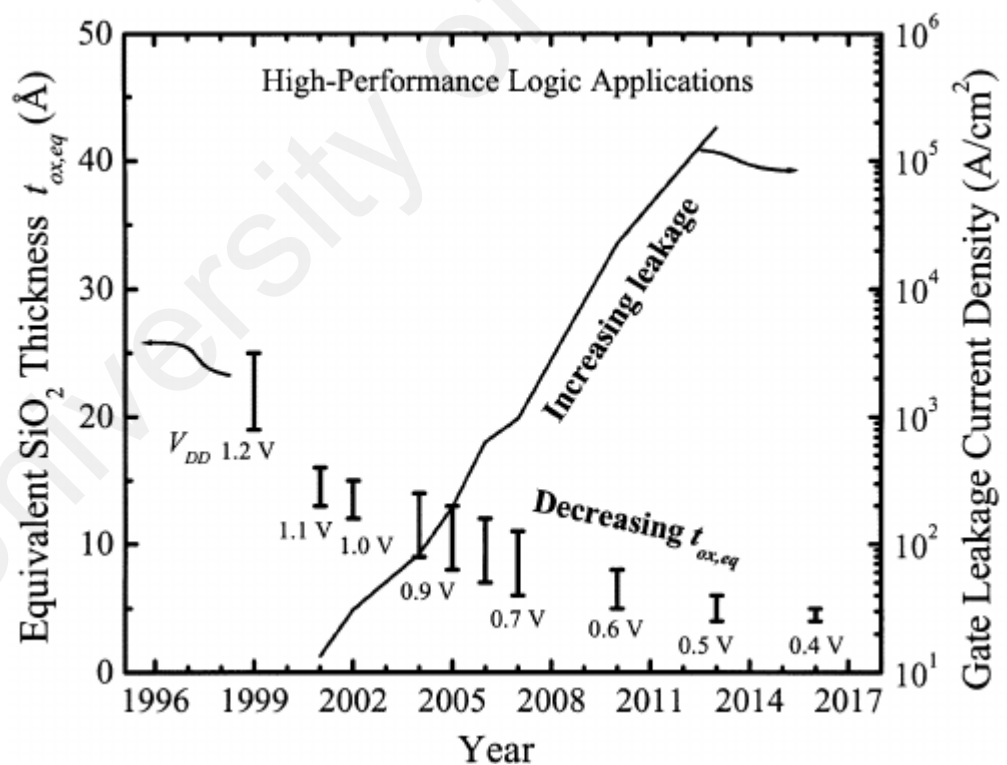


Figure 2.1: Scaling trend of the MOSFET gate dielectric thickness (Yeo et al., 2003)

## 2.2 Gate leakage

Undeniable that power consumption is the crucial issue faced by the semiconductor industry today. There are two major sources of power consumption, namely off-state leakage current and dynamic power. Off-state leakage current is simply known as static power or it can be understood as the current which leaks through the transistors even though the transistors are turned off. The static power consumption is comprised of two principal components, sub-threshold leakage and gate leakage. Sub-threshold leakage represents the weak inversion current across the device, while gate leakage is the tunneling current across the gate oxide insulation. On the other hand, dynamic power is the power loss due to the repeated capacitance charge-discharge on the output of the hundreds of millions of gates in chips when the transistors are turned on.

The dynamic power was the significant source of power dissipation as compared to static power, however, Moore's law has managed to control it by controlling the supply voltage. By reducing the supply voltage, the dynamic power will be reduced significantly, leading to reduction in power consumption. Despite, as the device sizes keep on shrinking into much smaller geometry, leakage has been provoked and the power consumption has been dominated by the static power. Upon downscaling, the power consumption increases drastically as the chip density and device speed increase. The total chip dynamic and static power consumption trends according to 2002 statistics normalized to 2001 ITRS are shown in Fig. 2.2 (Association, 2001). The projection shows a decrease in dynamic power per device over time, but if the number of on-chip devices is doubled every two years, the total dynamic power will be increased on a per-chip basis. Moreover, projection of exponential increase in both sub-threshold leakage and gate oxide leakage is shown in the Fig. 2.2.

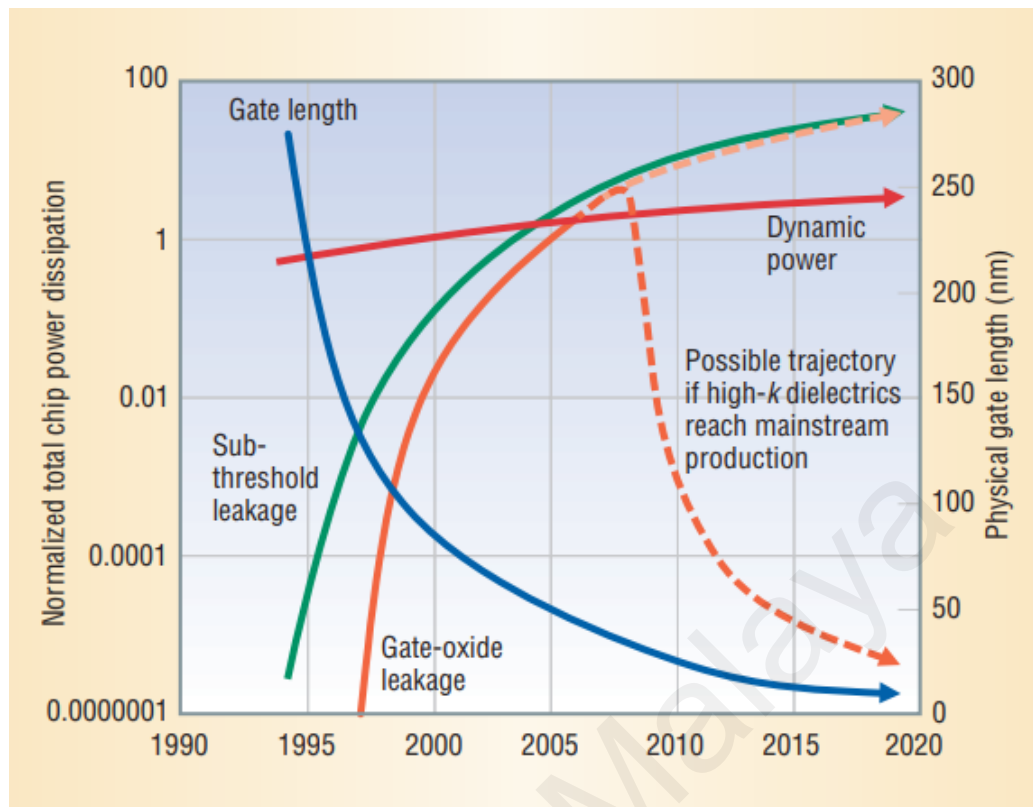


Figure 2.2: Power dissipation trends of dynamic power and static power based on ITRS (Association, 2001)

Along the continuing downscaling trend of device, the thickness of gate oxide has to be reduced constantly, resulting in very thin or ultra-thin gate oxides. The ultra-thin gate oxides allow the leakage current to flow from the channel to the gate comes into the order of the sub-threshold leakage current and as a consequence the gate oxides can no longer be considered as an ideal insulated electrode. Accordingly, the circuit functionality is greatly affected, and standby power consumption is increased. Moreover, the maximum clock cycle time is dramatically increased by the gate leakage current (N. Wang, 1989).

The gate leakage current mechanism can be elucidated using two tunneling mechanisms, namely Fowler-Nordheim tunneling and direct tunneling (Schenk & Heiser, 1997). The gate leakage and oxide thickness possess exponential relationship in

which as the gate oxide thickness decreases, the gate leakage current increases exponentially. For that reason, the downscaling of oxide thickness is limited to a range of 1.5 to 2 nanometers while considering the total standby power consumption of a chip (Lieber, 2001; Taur, 1999). Nonetheless, further device downscaling can still be realized by mean of high  $\kappa$  materials (Shero & Pomarede, 2005; S. Thompson, 1998). By incorporating alternative high  $\kappa$  dielectric oxides which have higher permittivity than  $\text{SiO}_2$  into the gate dielectric, a lower EOT can be achieved without tunnel-limited behavior. The higher  $\kappa$  values make possible the further reducing EOT because the alternative materials can exhibit the equivalent capacitance as a thinner  $\text{SiO}_2$  layer.

### **2.3 Germanium as a newly emerging semiconductor material**

A great amount of effort has been put in by researchers to explore the alternative substrates which have higher mobility channel and thus have great possibilities to replace Si in the future CMOS technology (Del Alamo, 2011; Pillarisetty, 2011). Saturation drive current ( $I_{\text{on}}$ ) is one of the crucial performance metrics for FET devices which is closely associated with the carrier mobility in FET. However, this relation has become ambiguous and no longer sustainable as the devices are being downscaled. In view of this relation, introduction of alternative materials with high mobility channel is required for further transistor downscaling. Germanium (Ge) and III-V compounds are the examples of potential candidates. They preponderate over the strained silicon for their higher carrier mobility and thus they are able to increase  $I_{\text{on}}$  even under lower supply voltages.

According to the CMOS device architecture evolution and metrology, Si transistors are predicted to have limited newly improved generations of technology. On the contrary, Ge-based transistors are predicted to have more generations of technology

which have great potential for further CMOS development. As compared to Si, electron mobility of Ge is two-fold greater, and hole mobility of Ge is four-fold greater. This statement can be further consolidated by Fig. 2.3 showing Si substrates exhibit lower hole mobility and scalability in relative to Ge substrates (Kuhn, 2012). While Ge substrates can provide both outstanding intrinsic hole mobility and scalability than Si substrates which means that Ge is capable of opening the door to further device scaling if all the limitations related to Ge can be solved.

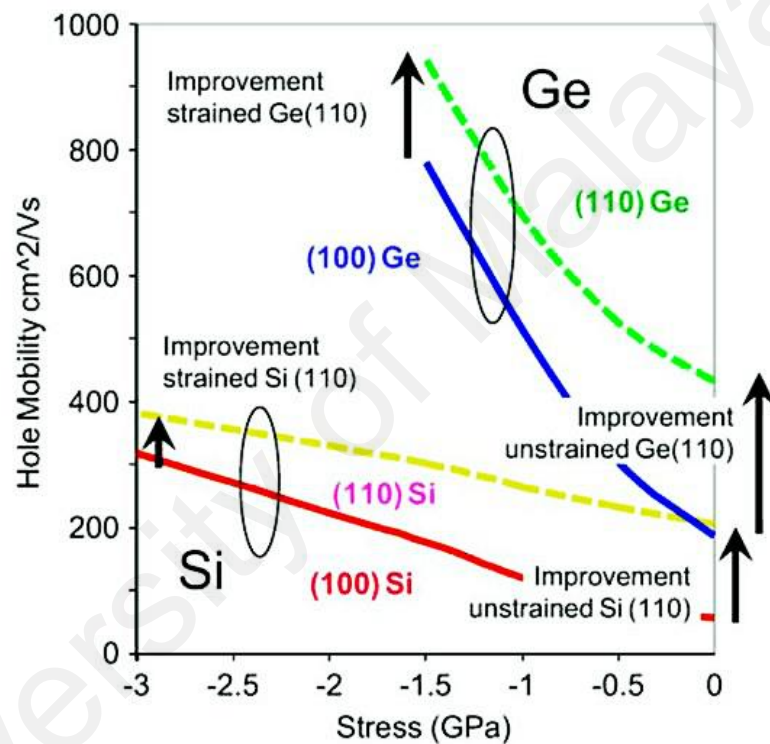


Figure 2.3: A graph of hole mobility against stress on unstrained and strained Si and Ge with different wafer orientation (Kuhn, 2012)

The physical and electrical properties of several alternative semiconductor materials at 300K or ambient conditions are described in Table 2.1 (M. Sze, 1981; Otfried Madelung, Rössler, & Von der Osten, 1987). As can be seen in Table 2.1, Ge exhibits smaller bandgap ( $E_g$ ) than Si, and this enables further scaling of power supply voltage ( $V_{DD}$ ) (S.-i. Takagi, Takayanagi, & Toriumi, 2000). Nevertheless, this will also



bring about a significant boost in the reverse-saturation current densities in a Ge pn junction (Claeys & Simoen, 2011; Kamata et al., 2006). In accordance with Fig. 2.3, Table 2.1 also indicates that both bulk hole and electron mobility of Ge are far greater than those of Si, 4.2 and 2.6 times respectively. Among the semiconductor materials, remarkably, Ge exhibits the greatest bulk hole mobility of 1900 cm<sup>2</sup>/V.s. Although most III-V compounds possess higher bulk electron mobility than Ge, it is comparably difficult to fabricate III-V materials-based MOSFETs than Ge-based. The reason is that there are several major technical issues regarding surface passivation of III-V materials that make them impractical for mainstream use today (Passlack, Hong, & Mannaerts, 1996; Ren et al., 1997). As already discussed previously that saturation drive current is an important key parameter for FET performance, Ge is advantaged by having very high density of states in the conduction band which allows high saturation drive current to be achieved. Furthermore, Ge also exhibits a large dielectric constant which makes it more susceptible to Short Channel Effects (SCE). Another important characteristic of Ge is the low melting temperature of 937°C, leading to low-temperature source/drain (S/D) dopant activation (Chui, Kim, et al., 2002; Kamata et al., 2006). Accordingly, high- $\kappa$ /metal gate stacks that cannot tolerate high temperature can be used with Ge substrate.

Table 2.1: A comparison of electrical and physical properties of semiconductor materials

	Ge	Si	III-V materials		
			GaAs	InSb	InP
Bandgap, $E_g$ (eV)	0.66	1.12	1.42	0.17	1.35
Dielectric constant, $\kappa$	16.0	11.9	13.1	17.7	12.4
Hole mobility, $\mu_h$ ( $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ )	1900	450	400	1250	150
Electron mobility, $\mu_e$ ( $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ )	3900	1500	8500	80000	4600
Effective density of states in conduction band, $N_C$ ( $\text{cm}^{-3}$ )	$1.04 \times 10^{19}$	$2.8 \times 10^{19}$	$4.7 \times 10^{17}$	$4.2 \times 10^{16}$	$5.7 \times 10^{17}$
Melting point, $T_m$ ( $^\circ\text{C}$ )	937	1412	1240	527	1060

On account of hole mobility of Ge is higher than that of Si, Ge has been regarded as the most highly potential alternative to take over Si as the channel material in future CMOS technology. As a matter of fact, bulk Ge was used as the semiconductor material in fabricating the first transistor by Bell Laboratories in 1947, however, Ge is disadvantaged by its substandard Ge native oxide layer,  $\text{GeO}_2$  which is thermodynamically unstable and water-soluble and thus not suitable to be adopted in CMOS device applications (Bardeen & Brattain, 1948; Jackson, Ransom, & DeGelormo, 1991). And besides this, in relative to Si, attaining stable oxides which exhibit low interfacial defect density can be tricky particularly on Ge owing to the inherent electrical and chemical instabilities of the  $\text{GeO}_2/\text{Ge}$  system. The issues associated with impractical  $\text{GeO}_2/\text{Ge}$  system make Ge was inadequate to be implemented as a CMOS channel material and Si was continuously used over the last 40 years. Accordingly,

improvement of effective electrical passivation of Ge and high  $\kappa$  gate dielectrics are the two necessary complementary strategies to pave the way for Ge-based MOSFET.

#### **2.4 Enhancement of interfacial and electrical properties using Ge passivation**

As Ge is introduced as a channel material, passivating Ge surface from oxidation and contamination is necessary to reduce interface as well as surface recombination. Hence, many researches have been done over years to find a proper chemically stable passivation treatment. Hydrogen passivation is the most common conventional method in the early period. This method is further applied on Ge substrate after Si substrate has been successfully passivated using hydrogen in the semiconductor industry (Deegan & Hughes, 1998). In this method, surfaces of Ge substrate are passivated in such a way that the dangling Ge bonds on the surfaces are saturated with hydrogen and forming Ge-H bonds. In addition, hydrofluoric acid (HF) solutions are also used to clean the Ge substrate in order to give rise to a clear oxide-free (H-terminated) Ge surfaces. Unfortunately, the hydrogen passivation method was later found to be ineffective on Ge surfaces. The ineffectiveness is said to be due to the unstable H-terminated Ge surfaces under ambient conditions and rapid absorption of hydrocarbons (Bodlaki, Yamamoto, Waldeck, & Borguet, 2003; Rivillon, Chabal, Amy, & Kahn, 2005).

Other than that, sulfur passivation is another promising approach. Sulfur passivation is similar to the previous hydrogen passivation method but the S-passivated Ge surfaces are more stable under ambient conditions as compared to H-terminated Ge surfaces (Bodlaki et al., 2003). In sulfur passivation method, the sulfur atoms are adsorbed on the clean Ge surfaces in the form of monolayer by forming S-Ge bonds at low pressure (Krüger & Pollmann, 1990; Weser et al., 1988). The layer formed can act as a buffer layer suppressing the growth of native Ge oxide interfacial layer. Aqueous

ammonium sulfide solutions  $(\text{NH}_4)_2\text{S}$  has lately been used as the sulphur-containing precursor used to treat the Ge surfaces (Frank et al., 2006).

Among the passivation approaches, nitride passivation can be considered as the highly probable one which can give rise to effective Ge surface passivation, hence the reliability of Ge-based MOSFET can be enhanced. In nitride passivation, the Ge substrates are subjected to nitridation involving reaction between nitrogen and Ge and formation of strong Ge-N bonds (Kim, McIntyre, Chui, Saraswat, & Cho, 2004; Shang et al., 2002). As a result of nitridation, either a layer of germanium nitride ( $\text{Ge}_3\text{N}_4$ ) or germanium oxynitride (GeON) will be grown on the Ge substrate (Hymes & Rosenberg, 1988). These layers offer better thermal as well as chemical stability as compared to native Ge oxide layer. Generally, the nitriding agents that used for nitrogen incorporation are nitrogen-containing compounds such as ammonia ( $\text{NH}_3$ ), nitrous oxide ( $\text{N}_2\text{O}$ ) and nitric oxide (NO). The nitride passivation technique has shown satisfactory results by reducing the film thickness to a level that the EOT is merely 1.9 nm while maintaining leakage in the acceptable range (Chui, Ito, & Saraswat, 2004). Apart from that, the ammonia-nitrided interface has shown better result than the wet chemical treated interface.

## **2.5 Ge oxide interfacial layers grown in high $\kappa$ /Ge system**

### **2.5.1 Native Ge oxide interfacial layer**

The superior carrier mobility of Ge has gained tremendous attention among researchers in semiconductor industry in recent years. Ge-based MOSFETs incorporating different gate dielectrics, for example pyrolytic  $\text{SiO}_2$ , CVD  $\text{SiO}_2$ , high-

pressure oxidation of Ge, GeON, and Ge<sub>3</sub>N<sub>4</sub>, have been investigated (Chang & Yu, 1965; Crisman, Ercil, Loferski, & Stiles, 1982; Hymes & Rosenberg, 1988; Rzhhanov & Neizvestny, 1979; K. Wang & Gray, 1975). It has been observed that Ge-based MOSFETs have poor interface properties with high mid-gap interface and bulk trap densities in spite of their carrier mobility is higher than Si-MOSFETs'. These interface and bulk traps are the sources of leakage current that give rise to poor sub-threshold characteristics. In addition, the existence of unstable Ge oxide layer is one of the important reasons why Ge substrate is not preferred over Si substrate in integrating MOSFETs.

Under a variety of environmental conditions, Ge can easily be oxidized to form Ge oxides which are comprised of different oxide species such as germanium monoxide (GeO) and germanium dioxide (GeO<sub>2</sub>) (Prabhakaran & Ogino, 1995; Tabet, Al-Sadah, & Salim, 1999). According to the studies have been conducted by others, transformation of GeO<sub>2</sub> to GeO takes place on the Ge surface upon annealing, and desorption of Ge oxides takes place as temperature reaches up to 425°C (Prabhakaran, Maeda, Watanabe, & Ogino, 2000b). The consecutive occurrence of the two processes thermal oxidation and desorption of Ge oxides are proclaimed to cause a decline in Ge of the surface (Oh & Campbell, 2004). Additionally, it has been found that both GeO and GeO<sub>2</sub> are soluble in dilute acidic and alkaline solutions as well as warm water, and the solubility is attributable to their amphoteric behavior (Prabhakaran & Ogino, 1995). SiO<sub>2</sub>, conversely, is only soluble in hydrofluoric acid (HF). Accounts for the difference in solubility, both Ge oxides have lower chemical stability than SiO<sub>2</sub>. Aside from the solubility difference, Ge oxides are physically and chemically far different from SiO<sub>2</sub>. All these together make Si as the primary semiconductor material used in CMOS technology, for decades.

GeO<sub>2</sub> is a representative native oxide of germanium (Ge), also called germania. Recently, a lot of efforts have been made in studying and characterizing the GeO<sub>2</sub>, and it is affirmed that GeO<sub>2</sub> has different level of complexity and stability compared to SiO<sub>2</sub>. It can be understood as GeO<sub>2</sub> is more complicated and behaves less stable than SiO<sub>2</sub>. According to a research conducted by Laubengayer in 1930, GeO<sub>2</sub> is found to exhibit two crystalline phases which are hexagonal and tetragonal crystal structure respectively, and also an amorphous phase (Laubengayer & Morton, 1932). Among these three different crystalline phases, only tetragonal crystalline phase is insoluble in water while the other two are soluble in water. Besides, the Ge and oxygen (O) atom are deemed to be covalently bonded with covalent bonds. GeO<sub>2</sub> is hygroscopic which means it has a strong affinity for water, and it is also water-soluble which means it can dissolve easily in water (Da Silva et al., 2012). Thermal desorption of GeO<sub>2</sub> is a result of reaction with Ge substrate and diffusion of oxygen vacancies taking place at the interface of GeO<sub>2</sub>/Ge (Kita et al., 2008). Moreover, thermal desorption of GeO<sub>2</sub> is facilitated at higher oxidation temperature and lower oxygen pressure. The appearance of GeO<sub>2</sub>/Ge layers varies depending on the thickness of the GeO<sub>2</sub>. With increasing oxide thickness, the GeO<sub>2</sub>/Ge layers appear brown, yellow brown followed by light blue (Nunley et al., 2016).

### **2.5.2 Effect of interfacial oxide layer on high $\kappa$ /Ge system**

It has been investigated that a thin low  $\kappa$  interfacial oxide layer is present in both high  $\kappa$ /Ge and high  $\kappa$ /Si systems, flanked by high  $\kappa$  dielectric and substrate. The formation of the interfacial oxide layer is described as an ineluctable and insuppressible event. In high  $\kappa$ /Si system, the interfacial layer formation significantly hinders the further EOT scaling, and this can directly influence the performance of CMOS device

(Lee, Jeon, Kwong, & Clark, 2002; Wilk et al., 2001). On the other hand, in high  $\kappa$ /Ge system, the native Ge oxide interfacial layer is a double-edged sword because of its instability. Even though the formation of unstable Ge oxide interfacial layer gives rise to inadequacies of Ge to be used as CMOS substrate material, however the removal of the interfacial layer is made easier by the unstable nature of Ge oxide interfacial layer. The role of the unstable Ge oxide interfacial layer in assisting the removal process as well as facilitating further EOT scaling is further explained and described in several experiments (Chui, Ramanathan, Triplett, McIntyre, & Saraswat, 2002; Delabie et al., 2005; Van Elshocht et al., 2004). Incorporating hafnium(IV) oxide ( $\text{HfO}_2$ ) as the high  $\kappa$  material, an experimental result has shown the interfacial oxide layer developed in high  $\kappa$ /Ge system is much thinner than that in high  $\kappa$ /Si system with aid of TEM characterization in Fig. 2.4 (Van Elshocht et al., 2004).

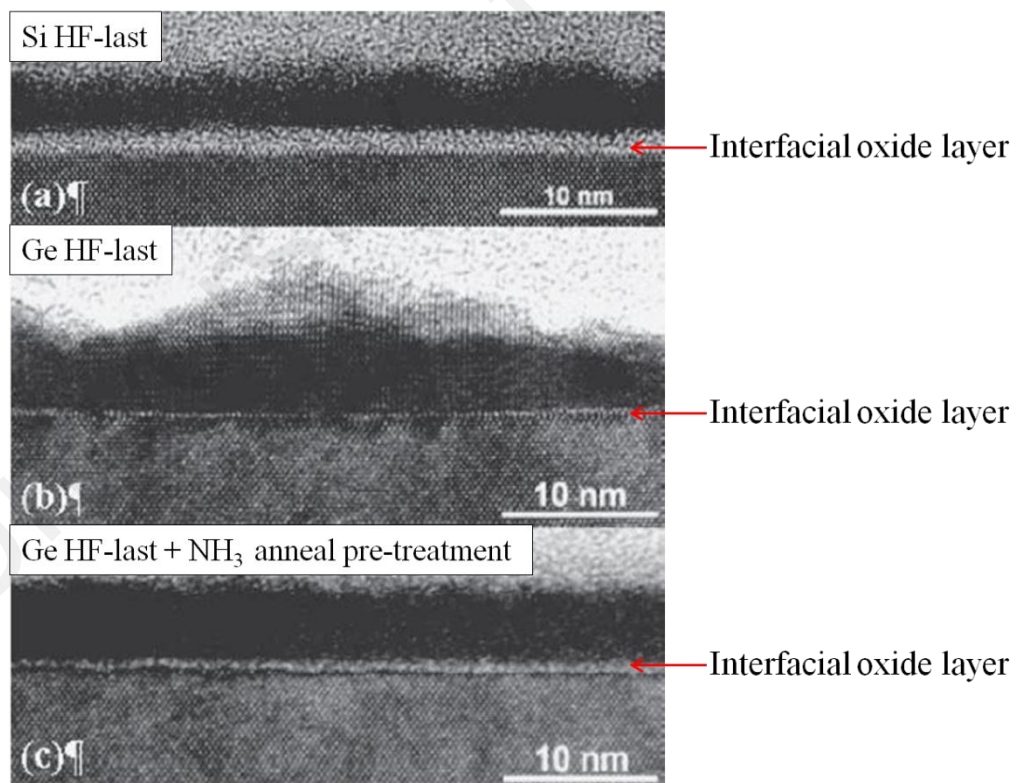


Figure 2.4: TEM images of various  $\text{HfO}_2/\text{Si}$  and  $\text{HfO}_2/\text{Ge}$  systems (Van Elshocht et al., 2004)

Despite being advantaged in further EOT scaling, there are some downsides to the high  $\kappa$ /Ge system too. Unlike high  $\kappa$ /Si system, high  $\kappa$ /Ge system exhibits greater roughness on the interfaces between adjacent layers in the layer stack, ALD-HfO<sub>2</sub>/interfacial layer and HfO<sub>2</sub>/HF-last Ge, respectively (Kim et al., 2004; Van Elshocht et al., 2004). Likewise, it has been ascertained that there is no noticeable interfacial layer between the epitaxially grown zirconium oxide (ZrO<sub>2</sub>) high  $\kappa$  films and the Ge substrate in the high  $\kappa$ /Ge system (Kim et al., 2003). This observation can be explained by the instability of the GeO<sub>2</sub> interfacial layer. As shown in Fig. 2.5, upon heating to approximately 430°C, the intensity of GeO increases while the intensity of GeO<sub>2</sub> decreases. These changes are attributed to the GeO<sub>2</sub> desorption and formation of GeO as the desorption product through the reaction between unstable GeO<sub>2</sub> and Ge substrate followed by sublimation of GeO<sub>2</sub> into GeO sublimate at low temperature (Prabhakaran, Maeda, Watanabe, & Ogino, 2000a). Alternatively, it might be due to a partial reaction between GeO<sub>2</sub> and the high  $\kappa$  films at low atomic layer deposition (ALD) temperature, thus causing the interfacial layer to decrease in thickness and increase in roughness (Kim et al., 2004).



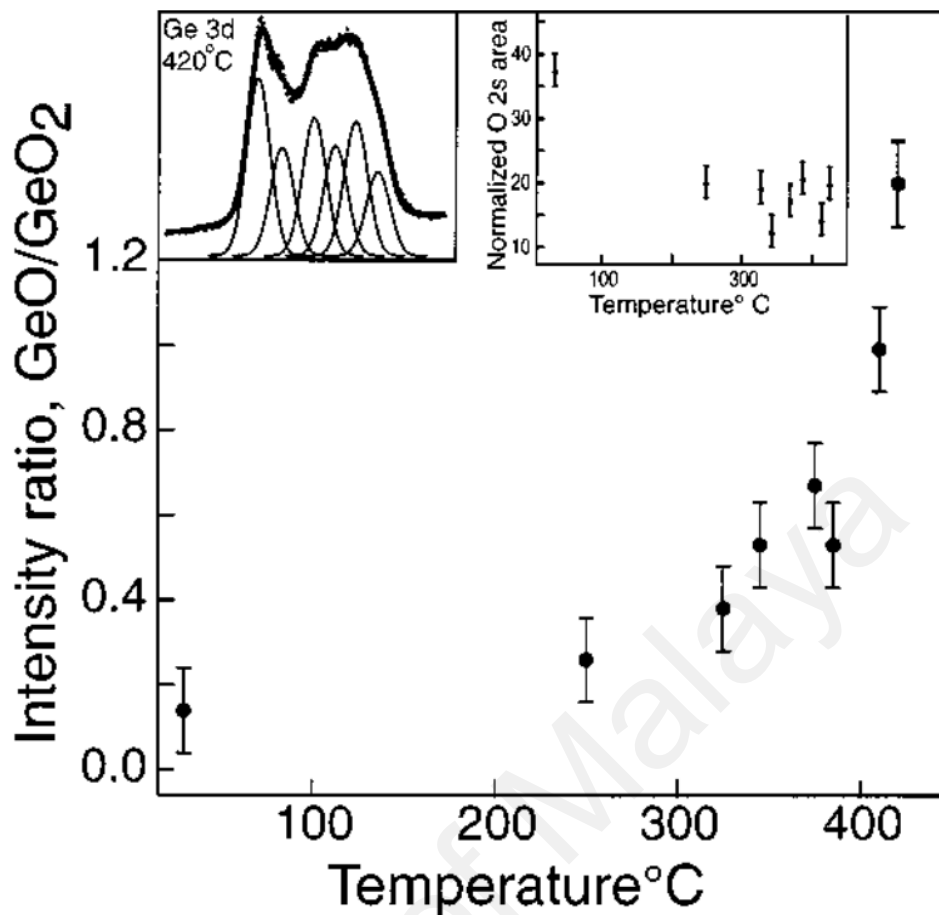


Figure 2.5: A graph of ratio of GeO/GeO<sub>2</sub> against temperature and an inset indicating the nearly constant oxygen concentration upon the transformation of GeO<sub>2</sub> to GeO

(Prabhakaran et al., 2000a)

Besides, local epitaxial growth of high  $\kappa$  films on Ge substrate exhibits poor alignment quality due to the presence of little amount of oxygen and impurities. Moreover, a high areal interfacial dislocation density is induced during the epitaxial growth process due to the large intrinsic lattice mismatch and large difference in intrinsic bonding (Kim et al., 2003). On the other hand, high  $\kappa$  dielectric material incorporated in MOS device is problematic to attain the accepted threshold voltage due to the presence of interfacial oxide layers and undesirable reaction between substrate metal and high  $\kappa$  dielectric. The gate dielectric stacks incorporated with high  $\kappa$

dielectrics exhibit a large shift in threshold voltage in NMOS as well as PMOS devices. The poor epitaxial alignment of high  $\kappa$  films on Ge substrate and poor interfacial quality of Ge oxides have significant impact on the electrical properties as well as performance of CMOS device. Accordingly, an emerging solution to the conundrum is to incorporate an additional layer which acts as a buffer layer to suppress the growth of low  $\kappa$  native Ge oxide interfacial layer and at the same time accommodate the lattice mismatch.

## **2.6 Suppression of native Ge oxide interfacial layer using buffer layer**

In recent years, there have been many studies which demonstrate the significant effects of buffer layers on the dielectric properties of high  $\kappa$  dielectric films and also electrical performance of the CMOS devices. Based on a 1996 research, incorporation of a low-temperature Si (LT-Si) buffer layer at the SiGe/Si interface helps in relieving misfit dislocations and suppressing threading dislocations at SiGe/Si interface (Chen et al., 1996). Also by inserting an additional aluminum nitride (AlN) sub-buffer layer in AlGaN/GaN MOSFET, the resulting AlGaN/GaN transistor shows a significant enhancement in transistor performance (Shealy et al., 2002). Incorporating a thin zinc oxide (ZnO) buffer layer in the polymer solar cells (PSCs) with an inverted device structure has been demonstrated to be very effective in suppressing the leakage current at the active layer/ITO interface (Yang et al., 2010). Furthermore, barium titanate ( $\text{BaTiO}_3$ ) (BT) thin films were developed as a buffer layer sandwiched between the sodium bismuth titanate ( $\text{Na}_{0.5}\text{Bi}_{0.5}\text{TiO}_3$ ) (NBT) and Pt-coated Si substrate via pulsed laser deposition (PLD). The study demonstrated a remarkable improvement in the dielectric properties of NBT thin films with the integration of BT buffer layer (Daryapurkar, Kolte, & Gopalan, 2012).

Besides, according to a recent study by researchers from National Taiwan University, AlN was integrated as a buffer layer in the crystalline ZrO<sub>2</sub>/Si gate stack with the aim of suppressing the growth of low  $\kappa$  Si oxides interfacial layer and thus reducing capacitance equivalent thickness (CET). The results from the study show that the buffer layer incorporation effectively suppresses the growth of silicate interfacial layer, and thus causes leakage current density ( $J_g$ ) to decrease by three orders of magnitude. Aside from  $J_g$ , the resulting crystalline ZrO<sub>2</sub>/AlN buffer layer/Si gate stack also shows a pronounced reduction on the CET and interfacial state density ( $D_{it}$ ) (W.-C. Wang et al., 2016).

## **2.7 Ge<sub>3</sub>N<sub>4</sub> as buffer layer grown on Ge through thermal nitridation**

The effective of suppressing Ge oxidation and interdiffusion across the high  $\kappa$ /Ge interface of nitrated Ge surfaces has been drawn deliberative attention from researchers (Chun-Rong, Zhao-Qi, Jing-Zhou, & Zheng, 1991; Maeda et al., 2004; Miotto, Miwa, & Ferraz, 2003; Sanders & Craig Jr, 2001). In earlier 1960s and 1970s, growth of germanium nitride films were conducted, however, the outcomes were not meet the requirement. Generally, the nitridation of Ge surfaces is by passing the ammonia gas in the form of either NH<sub>3</sub> or N<sub>2</sub>H<sub>4</sub> over the Ge substrate, or alternatively (Tindall & Hemminger, 1995), through nitrogen implantation. In addition, most of the previous studies and researches were conducted in ultra-high vacuum (UHV) at relatively low temperature with the intent of investigating the dissociative chemisorption of NH<sub>3</sub> on clean Ge(100) surface. There are three different resulting adsorption regimes, monolayer, second layer and condensed multilayer, respectively (Ranke, 1995).

Undoubtedly, many alternative approaches have been developed in recent years for nitriding Ge substrate, for example, thermal nitridation, chemical vapour deposition (CVD), low pressure CVD, magnetron sputtering, direct atomic source nitridation, and the most common ammonolysis method (Chambouleyron & Zanatta, 1998). The earlier published study has been investigated on the growth of  $\text{Ge}_3\text{N}_4$  films on Ge substrate by using germanium chloride ( $\text{GeCl}_4$ ) and  $\text{NH}_3$  as the source gases in LPCVD (Young, Rosenberg, & Szendro, 1987). Despite the deposition method accompanied by the production of undesirable ammonium chloride ( $\text{NH}_4\text{Cl}$ ), it is believed that there will be no incorporation of  $\text{NH}_4\text{Cl}$  happen if the temperature is controlled above  $335^\circ\text{C}$  which is the sublimation temperature for the  $\text{NH}_4\text{Cl}$ . Aside from that, amorphous  $\text{Ge}_3\text{N}_4$  layers grown crystalline Ge substrate has been also demonstrated through CVD by using germane gas ( $\text{GeH}_4$ ) instead of  $\text{GeCl}_4$ , together with  $\text{NH}_3$  (Alford & Meiners, 1987). A great degree of improvement in interfacial as well as electrical properties has been observed on Ge by integrating  $\text{Ge}_3\text{N}_4$  in the gate stack.

Moreover, the sputtering of  $\text{Ge}_3\text{N}_4$  films on the substrate through reactive RF magnetron sputtering has been demonstrated by making Ge as the target while  $\text{N}_2$  gas and Ar gas are made as the sputtering gases (G. Maggioni, Carturan, S., Fiorese, L., Napoli, D., Giarola, M., Mariotto, G., 2012). In the study, the  $\text{Ge}_3\text{N}_4$  layers grown functions as a barrier preventing oxygen diffusion across the interface. Also, according to a recent research study in 2017,  $\text{Ge}_3\text{N}_4$  films were deposited for passivating the surface of a high-purify Ge (HPGe) diode (G. Maggioni et al., 2017). The results indicate an improvement on the electrical performance, and the  $\text{Ge}_3\text{N}_4$  integrated diode possesses lower leakage current. Unlike  $\text{GeO}_2$ , the  $\text{Ge}_3\text{N}_4$  films are water-insoluble, and  $\text{Ge}_3\text{N}_4$  exhibit higher  $\kappa$  and thermal deposition temperature. In addition,  $\text{Ge}_3\text{N}_4$  layers can be adopted not only as a buffer layer for high  $\kappa$  dielectric grown on Ge metal substrate but also as an effective approach for passivating Ge surface. Many studies

have been performed on the preparation of  $\text{Ge}_3\text{N}_4$  layers on Ge substrate through *in situ* direct atomic source nitridation in the in UHV chamber (Maeda et al., 2004; S. Wang, Chai, Pan, & Huan, 2006; Yashiro, 1972). Besides, ammonolysis method that uses  $\text{NH}_3$  gas as the nitrogen-containing source gas is also widely applied in depositing  $\text{Ge}_3\text{N}_4$  layers on Ge substrate (Igarashi, Kurumada, & Niimi, 1968; Nakhutsrishvili, Dzhishiashvili, Miminoshvili, & Mushkudiani, 2000; Synorov, Kuznetsova, & Aleinikov, 1967).

In contrast to those previous works, the easiest and primitive thermal nitridation method using  $\text{N}_2$  as the source gas is adopted in this study.  $\text{N}_2$  gas is adopted for its environmental friendly behavior and cost effective benefit. Additionally, it is believed that the results of this study will become a significant and useful resource for researchers in exploring and discovering more possibilities for evolutionary change in CMOS technology.

## CHAPTER 3: MATERIALS AND METHODOLOGY

### 3.1 Introduction

In Chapter 3, lists of materials and methodology are explained in detailed. The first part introduces the materials used in each process; the second part illustrates the steps for the experimental procedures and the third part mentions about the characterization techniques used in this research project.

### 3.2 Materials

#### 3.2.1 Substrate

The antimony (Sb) doped n-Ge wafer used as substrate material is supplied by Wafer World, Inc. with diameter of  $100.0 \pm 0.5$  mm and  $500 - 550$   $\mu\text{m}$  thick,  $(100) \pm 5^\circ$  orientation, single side polished and resistivity of  $0.005 - 0.02$   $\Omega\cdot\text{cm}$ .

#### 3.2.2 Materials used in dip cleaning process

Diamond cutter is used to cut the Ge wafer into small samples, the chemicals used in dip cleaning process are hydrofluoric (HF) acid solution with ratio of 1 (HF) to 50 ( $\text{H}_2\text{O}$ ) and deionized (DI) water.

### 3.2.3 Materials used for thermal nitridation

Pure N<sub>2</sub> gas (99.99%) is used to flow through the quartz tube inside the Carbolite CTF tube furnace during the thermal nitridation process. Prior to thermal nitridation, the samples are held in a quartz boat and carefully put into the quartz tube.

## 3.3 Procedures for Ge<sub>3</sub>N<sub>4</sub> buffer layer growth

### 3.3.1 Dip cleaning of Ge substrate

Prior to dip cleaning, Ge wafer is cut into small pieces samples by using diamond cutter, 2 beakers containing HF acid solution and DI water respectively are prepared for the deep cleaning process. Generally, a sample is first immersed in the HF acid solution for about 10 seconds, taken out and immersed in DI water for another 10 seconds. Finally, the sample is dried off by using clean paper towel and the process is repeated for the rest of the samples.

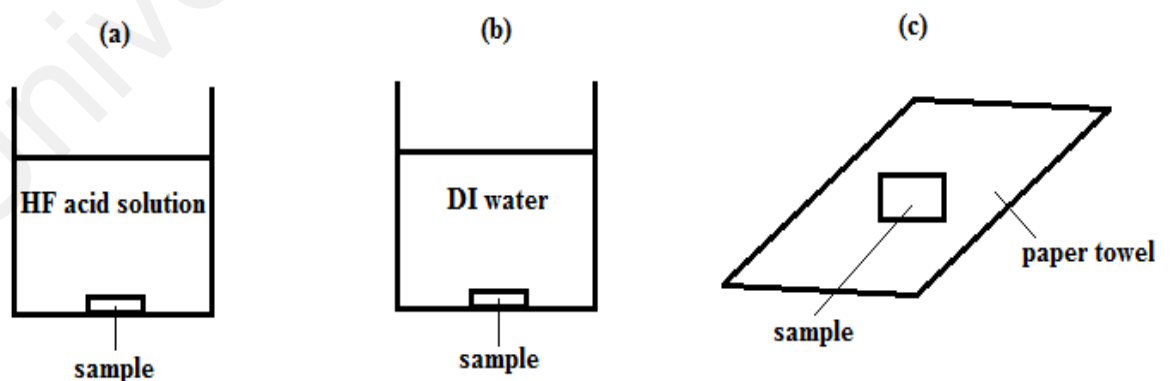


Figure 3.1: Steps for dip cleaning process, (a) sample is immersed in HF acid solution, (b) sample is immersed in DI water and (c) sample is dried off using paper towel

### 3.3.2 Thermal nitridation of $\text{Ge}_3\text{N}_4$

After the impurities-free samples are prepared, they are proceeded with thermal nitridation process for  $\text{Ge}_3\text{N}_4$  growth on the samples. Before that, the flow of  $\text{N}_2$  gas is checked and set to a fixed flow rate of  $150 \text{ ml}\cdot\text{min}^{-1}$ . Then, the furnace is heated up with  $10^\circ\text{C}\cdot\text{min}^{-1}$  increment in temperature. The experimental nitridation temperature is varying with 400, 500 and  $600^\circ\text{C}$ . Once the temperature of the furnace reached the set temperature, samples are placed on the quartz boat and carefully put into the middle of the quartz tube inside the furnace and the smooth flow of  $\text{N}_2$  gas is checked. The thermal nitridation process lasted for 15 minutes and the samples are let cooled down before removal. The samples are then well kept in a dry cool storage.

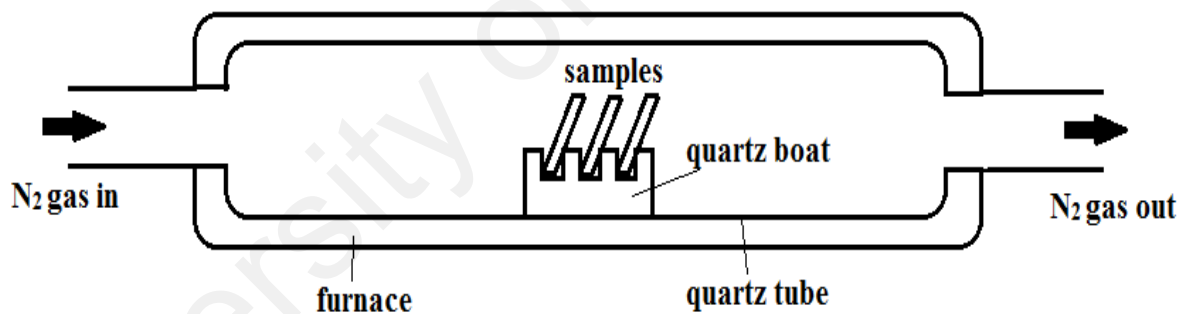


Figure 3.2: Illustration of thermal nitridation process for  $\text{Ge}_3\text{N}_4$  buffer growth



## 3.4 Characterization techniques

### 3.4.1 X-ray diffraction (XRD) analysis

XRD method is a powerful tools to analyze the phase identification of the crystalline structure and provide the information of the unit cell of the materials. Besides that, XRD is used to study the material, to identify the components in the materials and it is widely applied in the thin film analysis to study the surface characteristics and morphology (Stanjek & Häusler, 2004). X-ray diffractometer consists mainly of an X-ray tube, a sample holder and a detector as shown in Fig. 3.3. An X-ray beam is produced at the X-ray tube, directed to the sample and scattered. The diffracted X-ray beam is then detected by the detector at an angle of  $2\theta$  and a plot of X-ray intensity- $2\theta$  can be produced after the analysis. Based on the peaks found in the plot, the components can be identified by comparing the data with the database.

XRD works dependently with Bragg's law, which says that the 2 conditions must be satisfied when an X-ray is scattered from a crystal lattice: angle of incidence equal to the angle of scattering and the difference in path length is equal to an integer number of wavelengths. By looking at the Bragg's equation, as in Eq. 3.1,

$$n\lambda = 2d\sin\theta \quad (\text{Equation 3.1})$$

$n$  is the integer number,  $\lambda$  is the wavelength of the X-ray used for the analysis,  $d$  is the interplanar spacing of the sample materials, and  $\theta$  is the diffracting angle. The term  $2d\sin\theta$  is actually the path length difference. With the known  $\lambda$  and the diffracting angle  $\theta$ , the spacing  $d$  can be obtained and the unknown components of the materials can be identified by identifying the lattice constant,  $a$  of the components at plane (hkl).

$$a = d \cdot \sqrt{h^2 + k^2 + l^2} \quad (\text{Equation 3.2})$$

Besides the identification of unknown materials, the peak line broadening of the plot is also important to be studied in the XRD analysis. Generally, the peak line broadening is mostly affected by the nano-crystallite size (D) and lattice strain ( $\epsilon$ ). When the crystallite size is smaller than 100 nm, there exists very small a number of parallel diffraction planes and therefore the peak produced is broaden instead of sharp peak, also a lattice strain can broadens the peak as well (Endla & Gopi Krishna, 2013). There are several methods can be employed to estimate the 2 parameters. In this research project, Williamson-Hall (W-H) method is used to estimate the crystallite size and the lattice strain of the sample.

The broadening due to crystallite size can be determined by the Scherrer equation, and expressed as:

$$\beta_c = \frac{k\lambda}{D \cos\theta} \quad (\text{Equation 3.3})$$

where  $\beta_c$  is the peak broadening due to crystallite size, k is a constant usually defined as  $k = 0.9$ ,  $\lambda$  is the wavelength of X-ray radiation, D is the crystallite size and  $\theta$  is the diffraction angle. While broadening due to lattice strain is determined by the equation as shown in Eq. 3.4,

$$\beta_s = 4\epsilon \tan\theta \quad (\text{Equation 3.4})$$

where  $\beta_s$  is the peak broadening due to lattice strain,  $\epsilon$  is the lattice strain and  $\theta$  is the diffraction angle. Based on W-H method, the total peak broadening,  $\beta_t$  is the sum of both Eq.3.3 and Eq. 3.4 as shown:

$$\beta_t = \beta_s + \beta_c \quad (\text{Equation 3.5})$$

$$\beta_t = 4\epsilon \tan\theta + \frac{k\lambda}{D \cos\theta} \quad (\text{Equation 3.6})$$

and Eq. 3.6 can be further simplified into Eq. 3.7, thus a W-H plot can be produced by plotting  $\beta_t \cos\theta$  against  $4 \sin\theta$ , with  $\varepsilon$  as gradient and  $\frac{k\lambda}{D}$  as the y-intercept of the plot (Prabhu, Rao, Vemula, & Siva Kumari, 2014). With the information, the crystallite size and the lattice strain of the sample can be estimated.

$$\beta_t \cos\theta = 4\varepsilon \sin\theta + \frac{k\lambda}{D} \quad (\text{Equation 3.7})$$

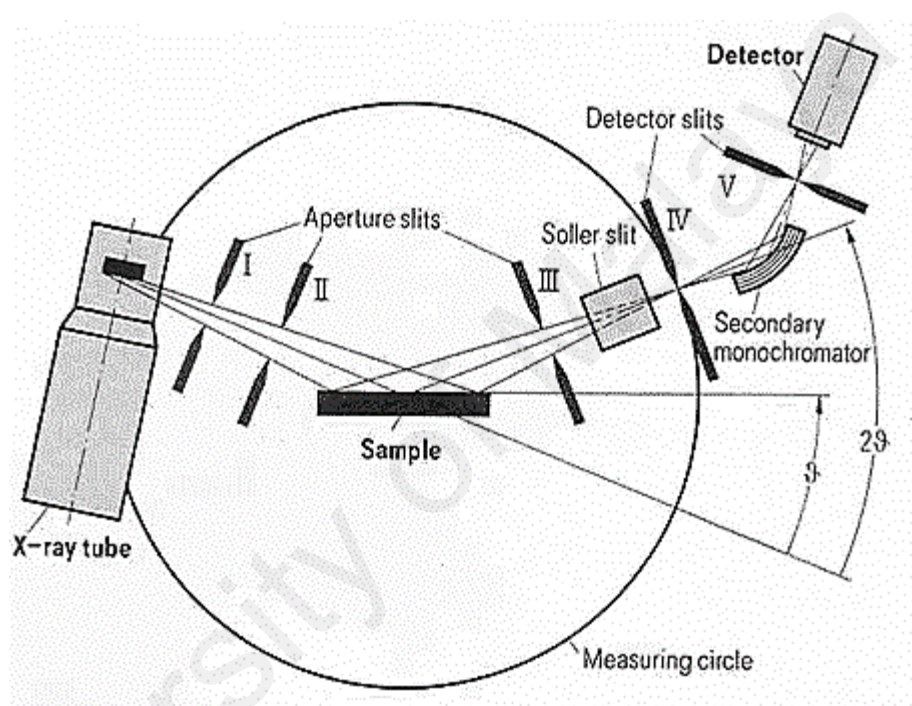


Figure 3.3: Schematic diagram of an XRD instrumentation (Source:

[www.ksanalytical.com](http://www.ksanalytical.com) accessed on May, 2018)

The X-ray diffractometer (XRD) used for this analysis is Rigaku MiniFlex Benchtop XRD, using Cu-K $\alpha$  radiation with  $\lambda = 1.5406 \text{ \AA}$  and scanning range from  $3^\circ$  to  $90^\circ$  for  $2\theta$ . The scan speed is  $10^\circ$  per minute with a scan width of  $0.0250^\circ$ .

### 3.4.2 Fourier-transform infrared (FTIR) spectroscopy analysis

FTIR spectroscopy analysis is used to identify the chemical bonds in a molecule through an infrared absorption spectrum. FTIR spectroscopy uses infrared-ranged electromagnetic wave to analyze the scan sample and observes the chemical properties of the sample. Since it is based on the infrared absorption by the sample and determines the chemical bonding by detecting the vibrations of the characterized bond, FTIR analysis causes no destruction to the sample. Moreover, FTIR analysis is an effective way to detect the functional groups and to characterize the information of the covalent bonds. Through the absorption peak of the infrared spectra, it actually acts as the fingerprint of a sample which corresponds to the frequency for the vibration of the bonding. The core component of a FTIR spectroscope is the interferometer as shown in Fig. 3.4. It consists of a beam splitter that splits the infrared beam into two beams with a difference in optical path. Then the beams recombined as a repetitive interference pattern and detected by the detector. When the beam passed through the sample, the sample will somehow absorbs some of the infrared, and the infrared transmittance signal can be obtained in the function of optical path difference. After that, the signal undergoes Fourier transformation done by interferogram and finally a transmittance versus wavenumber plot is produced (Kumar, Singh, Bauddh, & Korstad, 2015). In this research project, the equipment used for FTIR analysis is Bruker Tensor 27 FTIR spectroscope and the scanning parameter for the analysis is 32 scans per sample using attenuated total reflection (ATR) mode.

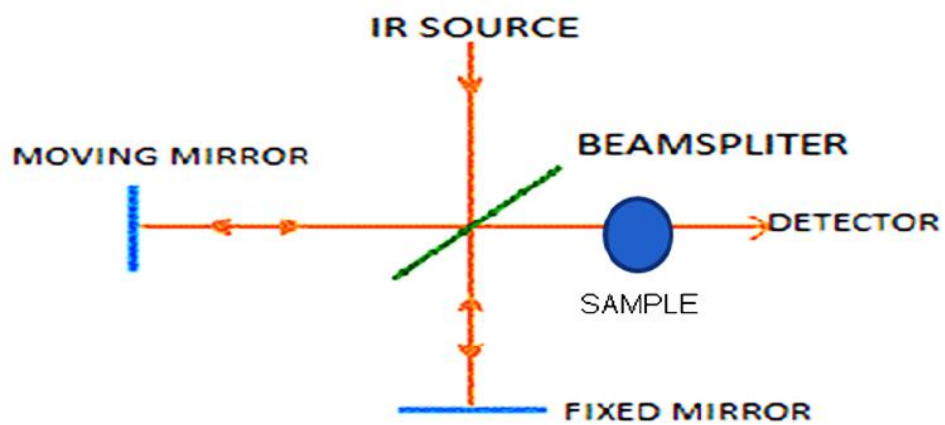


Figure 3.4: Schematic diagram of interferometer in FTIR spectroscope (Kumar et al., 2015)

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## CHAPTER 4: RESULTS AND DISCUSSION

### 4.1 Introduction

In Chapter 4, XRD patterns and FTIR absorption spectra were measured to analyze the phase structure of  $\text{Ge}_3\text{N}_4$  films and ascertain how nitrogen atoms are incorporated in the  $\text{Ge}_3\text{N}_4$  thin films. Basically, the resulting XRD patterns and FTIR spectra are interpreted and analyzed to determine the structural quality, the composition of the grown thin films as well as the presence of  $\text{Ge}_3\text{N}_4$  films, followed by discussion on the growth kinetics of the grown  $\text{Ge}_3\text{N}_4$  films and the optimum temperature for the growth of  $\text{Ge}_3\text{N}_4$  buffer layer is deduced from the interpretation of XRD and FTIR results. The results of XRD and FTIR measurements are evaluated based on the effect of thermal nitridation temperature on the deposition of  $\text{Ge}_3\text{N}_4$  films.

### 4.2 XRD analysis

The XRD patterns of the resulting films are measured to confirm the formation of  $\text{Ge}_3\text{N}_4$  buffer layer and for the purpose of structural characterization of the as-grown thin films. The  $2\theta$ -scan XRD patterns of the as-grown thin films which are thermally nitrided at 400, 500 and 600°C are shown in Fig. 4.1. From the XRD patterns shown in Fig. 4.1, it can be observed the presence of Ge substrate peak with a (110) preferred orientation at 38.94°. Seven characteristic peaks for tetragonal  $\text{GeO}_2$  (*t*- $\text{GeO}_2$ ) ( $2\theta$ ) at 28.96°, 35.52°, 47.05°, 48.07°, 56.08°, 64.39° and 81.27° are clearly detected for the 400°C sample showing that 400°C is not the optimum temperature for the growth of  $\text{Ge}_3\text{N}_4$  buffer layer, so that the formation of  $\text{GeO}_2$  interfacial layer cannot be effectively

suppressed. Furthermore, six characteristic peaks for  $t$ -GeO<sub>2</sub> ( $2\theta$ ) at 29.43°, 47.43°, 60.27°, 61.66°, 66.26° and 72.3° are observed for the 600°C sample demonstrating the irrepressible growth of GeO<sub>2</sub> interfacial layer and also the ineffectiveness of Ge<sub>3</sub>N<sub>4</sub> buffer layer at 600°C. Unlike 400 and 600°C, the XRD pattern of 500°C sample exhibits relatively lesser number of  $t$ -GeO<sub>2</sub> characteristic peaks which is only three characteristic peaks ( $2\theta$ ) at 28.65°, 42.43° and 65.39° indicating that the Ge<sub>3</sub>N<sub>4</sub> thin films deposited has come into play as a buffer layer to suppress the growth of unwanted GeO<sub>2</sub> interfacial layer.

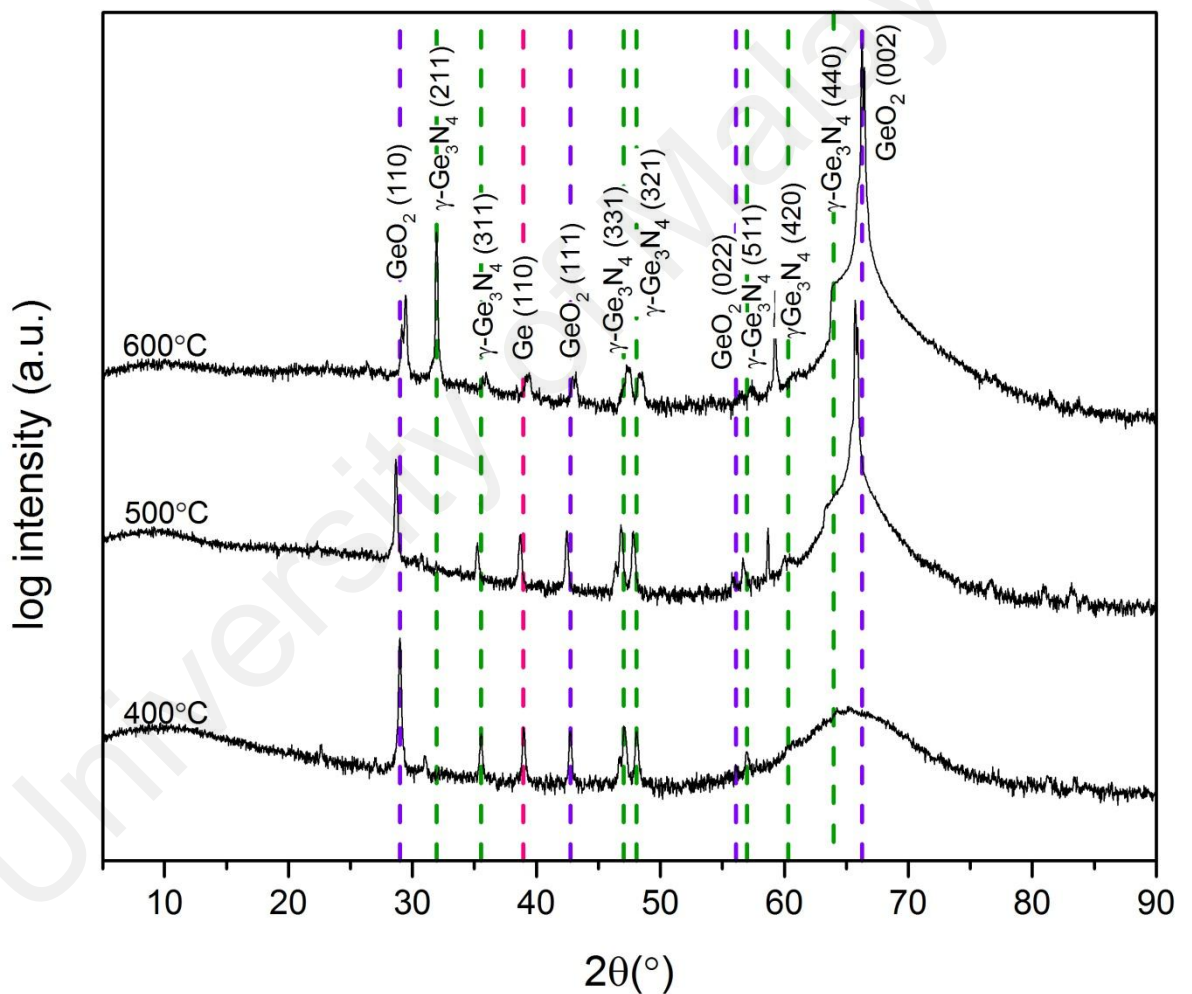


Figure 4.1: XRD patterns of thin films thermally nitrided at various temperatures for 15 minutes

The XRD peak positions for 500°C sample match well to the  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> with cubic spinel structure (PDF-2 01-075-8457), and this convincingly confirms that 500°C thermally nitrated sample exhibits strong  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> peaks at 35.18°, 46.81°, 56.66° and 65.39°, which are assignable to (311), (331), (511) and (531) facets, respectively. Unlike 500°C sample, instead of exhibiting peaks solely attributed to  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> in range of 47° to 49°, *t*-GeO<sub>2</sub>(102) is present in 400°C sample at 47.05° and 48.07°, while the XRD spectrum of 600°C sample shows strong *t*-GeO<sub>2</sub>(102) phase at 47.43° and 48.07°. These co-occurring peaks can be further individually identified by means of rescaling the 2 $\theta$  axis range to enlarge the specific axis range as shown in Fig. 4.2. Since a broad hump appearing in the 2 $\theta$  range from 60° to 70° in the XRD pattern for 400°C sample indicates characteristic amorphous phases which are made up of  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> and *t*-GeO<sub>2</sub>, the comparison is only made between the 500 and 600°C samples.

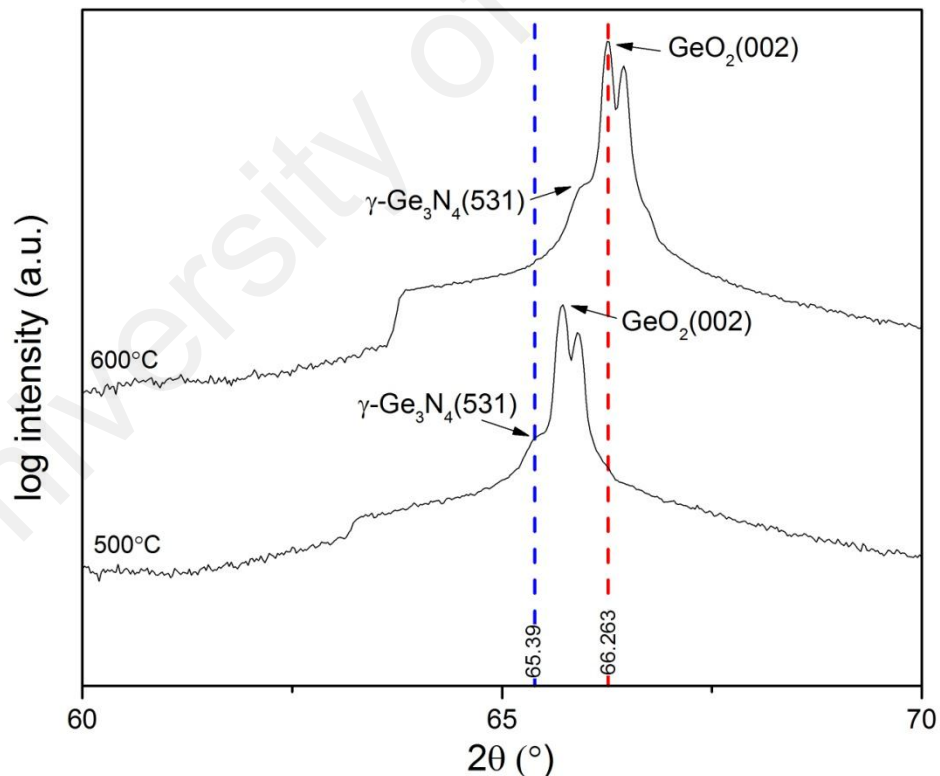


Figure 4.2: Enlarged XRD patterns in the 2 $\theta$  range between 60° and 70°



When looking closer at the peaks shown in Fig. 4.2, it can be observed that thermal nitriding the Ge at 500°C makes the *t*-GeO<sub>2</sub> (002) diffracted peak tends to move away from its standard XRD peak at 66.26° towards lower 2θ position, and thermal nitriding the Ge at 600°C makes the γ-Ge<sub>3</sub>N<sub>4</sub> (531) diffracted peak tends to move away from its standard XRD peak at 65.39° toward higher 2θ position. These diffracted peak position shifting phenomena are expected to be attributed to the effect of lattice strain. Shifting to lower diffraction angles is regarded as a result of compressive stress, while shifting to higher diffraction angles is considered as a result of tensile stress (Bandyopadhyay, Selbo, Amidon, & Hawley, 2005). Accordingly, the *t*-GeO<sub>2</sub> (002) phase is under compression at 500°C by the newly developed γ-Ge<sub>3</sub>N<sub>4</sub> (531) phase. On the other hand, a tensile stress has been introduced by the *t*-GeO<sub>2</sub> (002) peak onto the γ-Ge<sub>3</sub>N<sub>4</sub> (531) phase at 600°C, which indicates the *t*-GeO<sub>2</sub> phase islands has grown into a uniform film (Chason & Guduru, 2016).

In Fig. 4.3, the logarithm of the intensity of *t*-GeO<sub>2</sub> and γ-Ge<sub>3</sub>N<sub>4</sub> phases of various crystallography planes is plotted against the thermal nitridation temperature. From the plot, it can be noticed that thermally nitriding Ge at 500°C gives the highest intensities of γ-Ge<sub>3</sub>N<sub>4</sub> phases at (331), (311) and (511) planes. While, the lowest intensities of γ-Ge<sub>3</sub>N<sub>4</sub> phases at corresponding crystallographic planes are found in the 600°C nitrided films. A clear trend can be seen from the plot on which the intensity profiles of the γ-Ge<sub>3</sub>N<sub>4</sub> phases at (331), (311) and (511) planes show an almost consistent fluctuation in the temperature range. The intensities of γ-Ge<sub>3</sub>N<sub>4</sub> phases on various planes are found to first increase from 400°C and reach a peak at 500°C, gradually declining thereafter at 600°C. This implies that the optimum growth of γ-Ge<sub>3</sub>N<sub>4</sub> phases is at 500°C, and the γ-Ge<sub>3</sub>N<sub>4</sub> phases are appeared to be unstable at 400 and 600°C.

However, there is no absolute trend but ambiguous trends for describing the intensity profiles of the  $t$ -GeO<sub>2</sub> phases at (110), (111) and (022) planes. As shown in the plot, the  $t$ -GeO<sub>2</sub> phases with preferred orientation at (110) and (022) planes show a gradual decreasing intensity over the temperature range from 400 to 600°C, which means the 600°C nitrided films exhibit the lowest  $t$ -GeO<sub>2</sub> intensities at both (110) and (022) planes. This might be due to the transformation of GeO<sub>2</sub> to GeO on the Ge surface upon annealing and might also be due to the desorption of Ge oxides as temperature increases. Nevertheless, the  $t$ -GeO<sub>2</sub> phase at (111) plane shows a similar trend as the  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> intensity profiles in which the  $t$ -GeO<sub>2</sub> (111) intensity reaches the highest point at 500°C. This can be explained as such; nitrogen is not readily adsorbed on the more densely packed crystallographic planes, and the oxygen uptake is the greatest on the densely packed (111) plane (Germer, Scheibner, & Hartman, 1960). Generally, (111) plane exhibited the highest growth rate because (111) plane has the highest planar densities with more bonds for the greatest oxygen uptake (Gregory, Pruitt, Crisman, Roberts, & Stiles, 1988). Hence, the growth rate of  $t$ -GeO<sub>2</sub> phase is much higher than that of  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> phase on (111) plane which makes  $t$ -GeO<sub>2</sub> phase hard to be suppressed by the  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> phase. Also, further investigation on the temperature dependence of solubility of oxygen in germanium is needed.

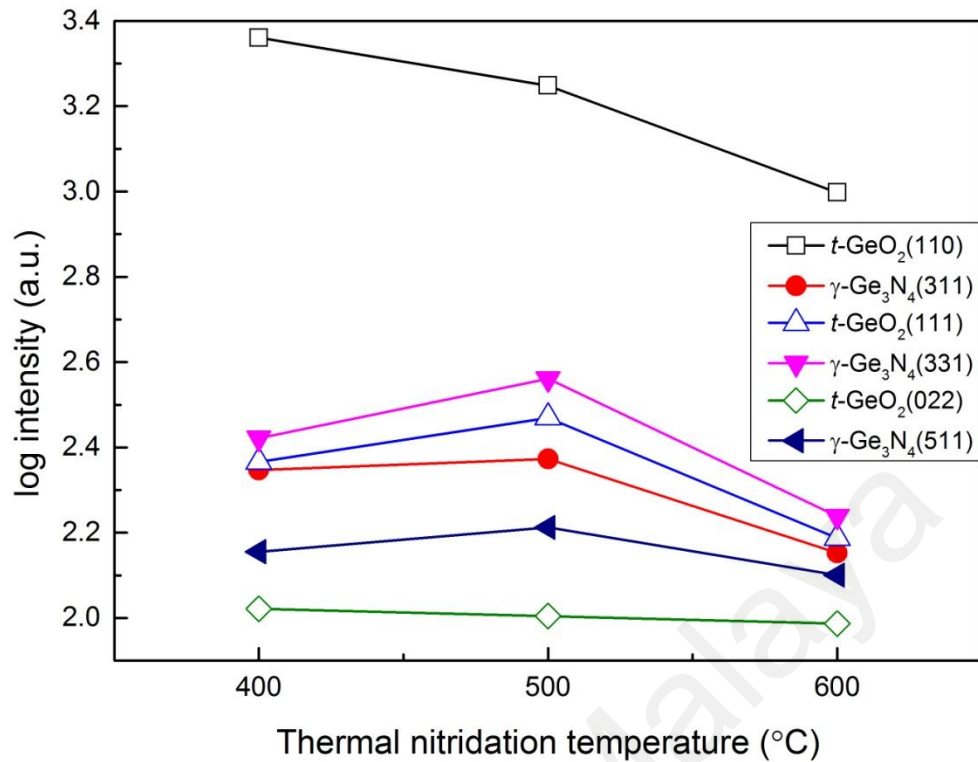


Figure 4.3: Logarithm of intensity of  $\gamma\text{-Ge}_3\text{N}_4$  and  $t\text{-GeO}_2$  phases at various planes at 400, 500 and 600°C

The Full Width at Half Maximum (FWHM) values measured for two set of planes of reflection, namely (110), (111), (022) and (311), (331), (511) are used with the Debye-Scherrer equation (Eq. 3.3) to evaluate the crystallite size of the  $t\text{-GeO}_2$  and  $\gamma\text{-Ge}_3\text{N}_4$  nanoparticles, respectively. The Eq. 3.3 is rearranged so that average crystallite size ( $D$ ) is solved by  $D = k\lambda / \beta_c \cos\theta$  where  $\beta_c$  is the FWHM of the peak in radians. The average crystallite sizes of  $t\text{-GeO}_2$  and  $\gamma\text{-Ge}_3\text{N}_4$  of various thermally nitrided films are illustrated in Fig. 4.5 and Fig. 4.6, respectively.

The  $D$  values of  $t\text{-GeO}_2$  for 400, 500 and 600°C thermally nitrided films are 41.20, 42.36 and 28.67 nm with corresponding size distribution of 6.86, 6.54 and 16.8 nm. Besides, the  $D$  values of  $\gamma\text{-Ge}_3\text{N}_4$  for 400, 500 and 600°C resulting films are 32.32, 35.38 and 16.43 nm with corresponding size distribution of 5.02, 3.33 and 3.60 nm. A slight fluctuation with a peak of  $D$  at 500°C and the 400 and 600°C give smaller  $D$  than

500°C can be similarly observed in both Fig 4.5 and Fig. 4.6. This signifies that both  $t$ -GeO<sub>2</sub> and  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> exhibit highest growth rate at 500°C and lowest growth rate at 600°C. A homogenous size distribution is noticed for 500°C  $t$ -GeO<sub>2</sub> films with the smallest standard deviation of 6.54 nm, whereas the 600°C  $t$ -GeO<sub>2</sub> films are calculated to have the largest standard deviation of 16.8 nm indicating highly heterogeneous crystallite size. Despite the  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> films grown in temperature range 400 to 600°C are not much different in size distribution, the 500°C  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> films are observed to have a highly homogenous size distribution with the smallest standard deviation value of 3.33 nm. Further investigation on the effect of crystallite size of  $t$ -GeO<sub>2</sub> and  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> on dielectric properties nitrided Ge is required to refine this research.

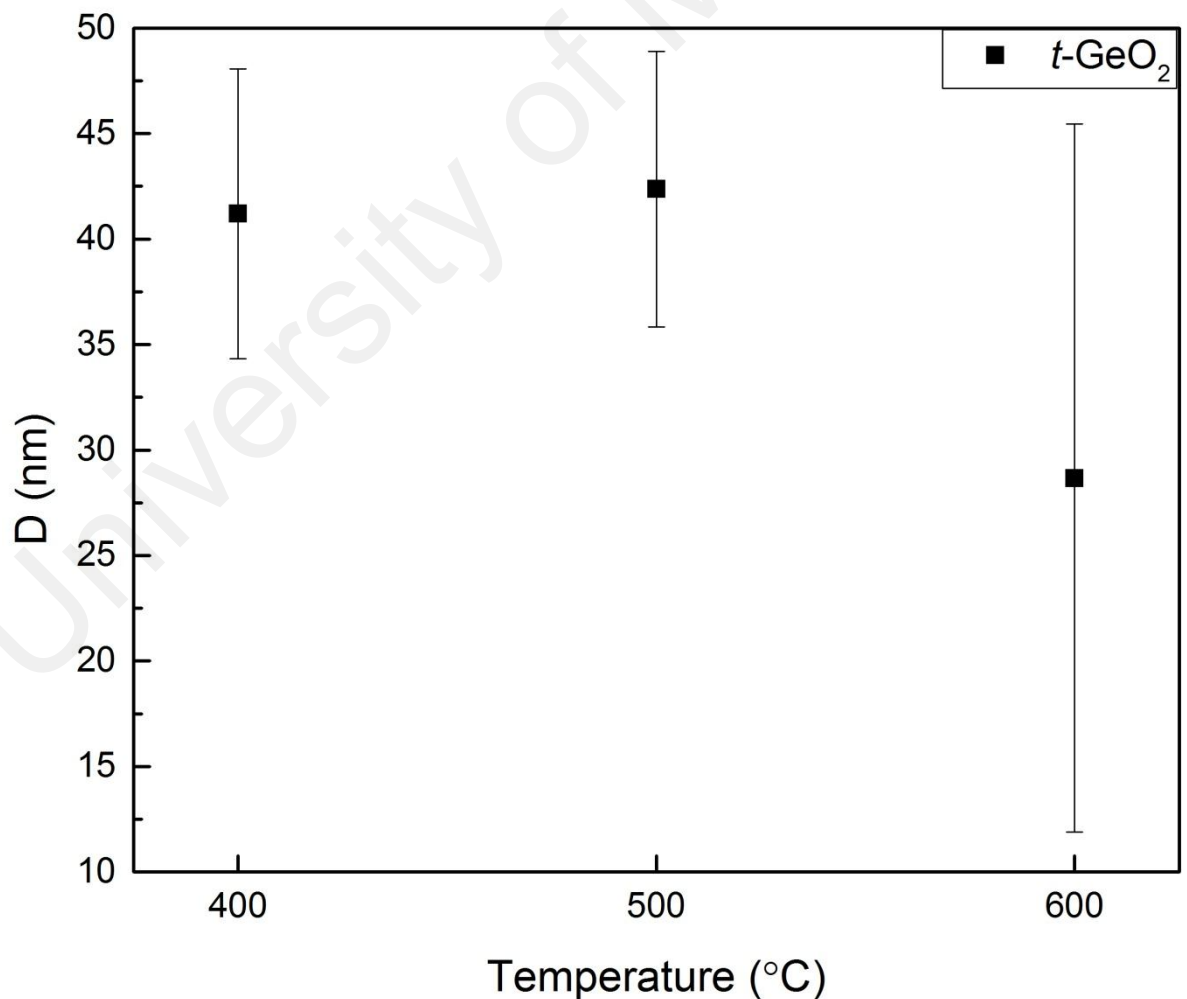


Figure 4.5: Crystallite size of  $t$ -GeO<sub>2</sub> over a temperature range of 400 to 600°C

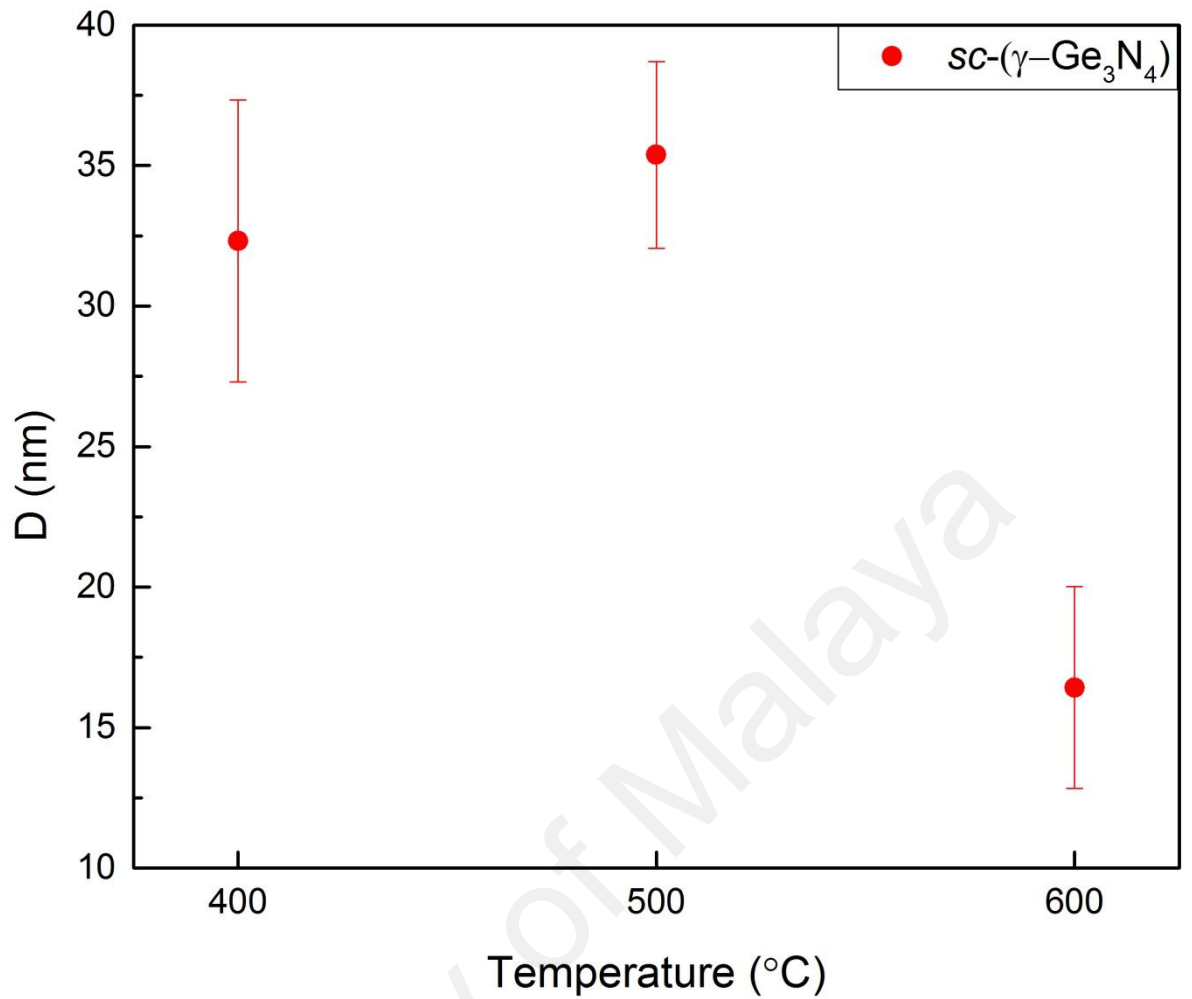


Figure 4.6: Crystallite size of  $\gamma\text{-Ge}_3\text{N}_4$  over a temperature range of 400 to 600°C

In order to determine the crystallite size and lattice strain of the thin film samples, a W-H plot is drawn with  $\beta_t \cos\theta$  along the y-axis and  $4\sin\theta$  along the x-axis for the  $\gamma\text{-Ge}_3\text{N}_4$  films grown at various thermal nitridation temperatures as shown in Fig. 4.7. After plotting the  $\beta_t \cos\theta$  and  $4\sin\theta$  values in a scatter plot, straight line equations are obtained through linear regression on each set of values as the Eq. 3.7 corresponds to a straight line equation with slope of  $\varepsilon$  and intercept of  $k\lambda/D$ . Thus, the  $\gamma\text{-Ge}_3\text{N}_4$  crystallite size ( $D$ ) and microstrain ( $\varepsilon$ ) on the  $\gamma\text{-Ge}_3\text{N}_4$  films can be deduced from the intercept ( $k\lambda/D$ ) and the slope ( $\varepsilon$ ) of the W-H plot respectively, by comparing the rearranged form of Eq. 3.7 to Eq. 4.1 which is a standard straight line equation where  $m$

represents the gradient and  $c$  represents the y-intercept. The foregoing crystallite size and microstrain deduction is summarized as follows.

$$\beta_t \cos\theta = 4\varepsilon \sin\theta + \frac{k\lambda}{D} \quad (\text{Equation 3.7})$$

$$\beta_t \cos\theta = \varepsilon (4 \sin\theta) + \frac{k\lambda}{D} \quad (\text{Rearranged form of Eq. 3.7})$$

$$y = mx + c \quad (\text{Equation 4.1})$$

The comparison gives  $y = \beta_t \cos\theta$ ;  $m = \varepsilon$ ;  $x = 4 \sin\theta$ ;  $c = \frac{k\lambda}{D}$ . The values of  $D$  and  $\varepsilon$  for 400, 500 and 600°C samples deduced from the W-H plot are tabulated in Table 4.1. The microstrains on the  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> layer are found to be negative (compressive) at 400 and 600°C, and positive (tensile) at 500°C. Those compressive microstrains indicate that the  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> layers are being compressed by the  $t$ -GeO<sub>2</sub> at 400 and 600°C, while the tensile microstrain indicates  $\gamma$ -Ge<sub>3</sub>N<sub>4</sub> islands has grown into a uniform layer and a tensile stress is generated during the growth process at 500°C.

Table 4.1: The deduced values of  $\varepsilon$  and  $D$  for 400, 500 and 600°C samples

Temperature (°C)	$\varepsilon$	y-intercept, $c = k\lambda/D$	$D$ (nm), $D = k\lambda/c$
400	$-4.10326 \times 10^{-5}$	0.00401	34.58
500	0.00117	0.00252	55.02
600	-0.00391	0.01489	9.312

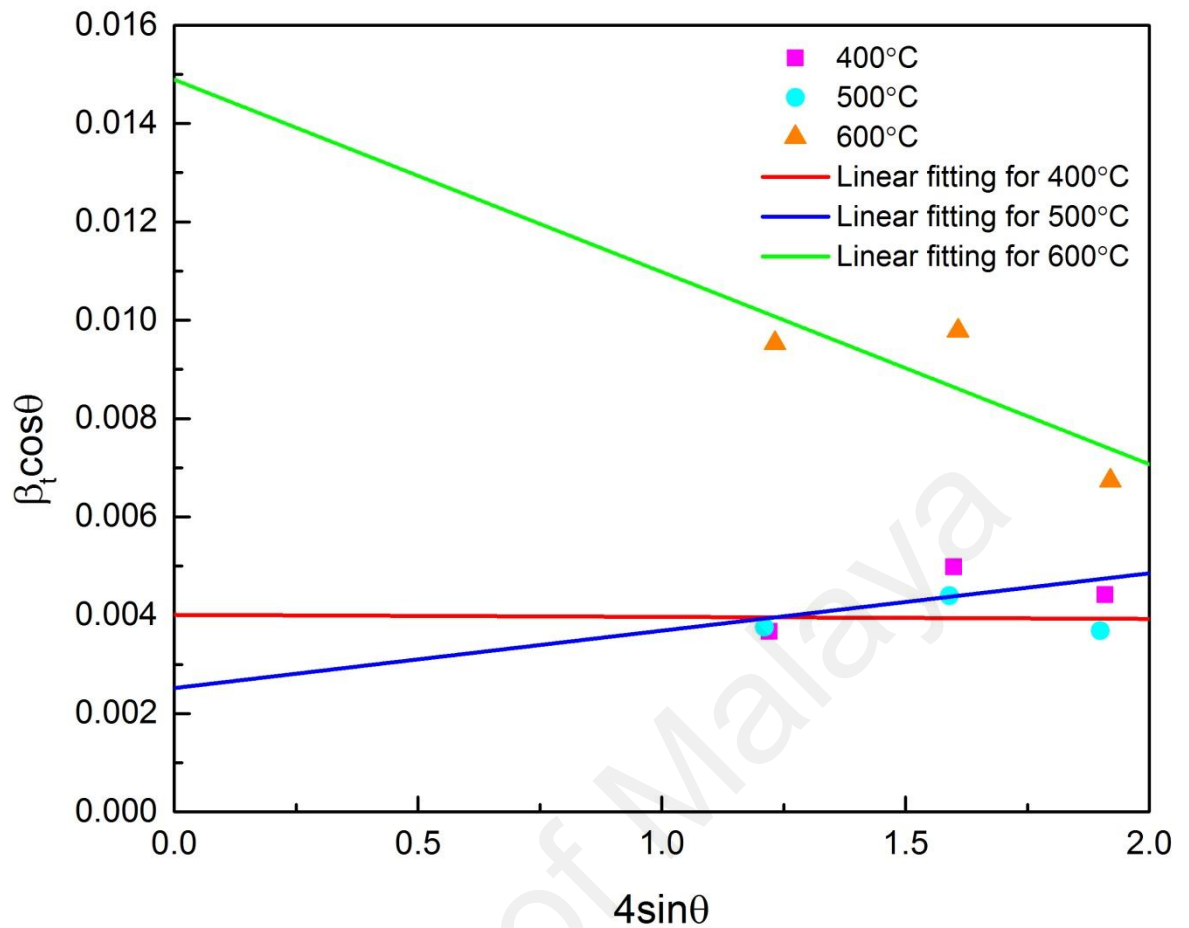


Figure 4.7: W-H plot of  $\gamma$ - $\text{Ge}_3\text{N}_4$  films grown at various thermal nitridation temperatures

### 4.3 FTIR spectrum analysis

In FTIR spectrum analysis, the optical signatures of  $\text{Ge}_3\text{N}_4$  vibrational modes are obtained in the transmission mode using  $\text{Ge}_3\text{N}_4$  films. The FTIR spectra of the resulting nitrided films are shown in Fig. 4.8 which plots the transmittance expressed in arbitrary units within the wavenumber range of 400 to 2000  $\text{cm}^{-1}$ . The chemical bonds in the resulting films are characterized and identified by referring to the infrared absorption spectra at specific wavenumber range. As mentioned in the introduction to this research study, the particular research interest focus on developing a highly effective  $\text{Ge}_3\text{N}_4$

buffer layer to suppress the formation of unwanted GeO<sub>2</sub> layer, hence, it is essential to identify crucial Ge-N and Ge-O bonds.

According to previous studies related to Ge<sub>3</sub>N<sub>4</sub> films, an absorption peak appearing at 300 cm<sup>-1</sup> has been affiliated to the disorder induced breathing mode vibrations of Ge-Ge dipole, and followed by an absorption peak associating with the symmetric in-plane stretching mode of Ge<sub>3</sub>N skeletal group appears at 450 cm<sup>-1</sup>. In addition, an absorption band observed at 690 cm<sup>-1</sup> signifies the Ge-N asymmetric stretching in-plane vibrational mode (Zanatta & Chambouleyron, 1993). Also, it has been reported that the Ge-N stretching vibrational mode can be found at 720 cm<sup>-1</sup> (Sandu et al., 2006). Some research studies on the effect of nitrogen concentration on the infrared absorption of Ge<sub>3</sub>N<sub>4</sub> show that an absorption peak characterizing the in-plane asymmetric stretching mode vibration of Ge-N bond can be observed at 700cm<sup>-1</sup> at nitrogen concentration above ~ 0.5 at.%. Moreover, two absorption peaks will be observed at 870 cm<sup>-1</sup> and 1100 cm<sup>-1</sup> respectively indicating in-plane asymmetric stretching mode vibration of Ge-N bond as the absolute nitrogen concentration increases up to 35 at.% (Zanatta, Freire Jr, & Chambouleyron, 1993).

Besides, some studies show that the isotopes of N arising from Ge<sub>3</sub>N<sub>4</sub> at high temperature can impose its pair defect on the infrared absorption of Ge-N bond by which <sup>14</sup>N-nitrided germanium sample gives four local vibrational modes (LVM) which are observed at 577, 590, 660 and 825 cm<sup>-1</sup> respectively, while <sup>15</sup>N-nitrided germanium sample shows shifted absorption bands appearing at 559, 573, 641 and 801 cm<sup>-1</sup> correspondingly. Among the absorption peaks, the stretching mode vibration of Ge-N bond can be evinced by the peaks appearing at 577 and 590 cm<sup>-1</sup>, and the absorption peaks arising from the N-pair defects are signified by the other modes at 660 and 825 cm<sup>-1</sup>. Upon annealing, the FTIR results demonstrate the transformation of <sup>14</sup>N-Ge to



$^{15}\text{N-Ge}$  and the appearance and disappearance of the intermediate mode of  $^{14,15}\text{N}$  at 654 and  $810\text{ cm}^{-1}$  at  $450^\circ\text{C}$  and  $700^\circ\text{C}$  respectively (Rasmussen, Jones, & Öberg, 1994).

On the other hand, the recent studies show that the Ge-O bands symbolizing the presence of  $\text{GeO}_2$  films can be evinced by the bands showing up at  $524$  and  $825\text{ cm}^{-1}$ , however, these bands are observed to shift towards higher wavenumber such that  $524$  to  $570\text{ cm}^{-1}$  and  $824$  to  $870\text{ cm}^{-1}$  upon annealing (Ardayanian, Rinnert, Devaux, & Vergnat, 2006). Also, Lei et al. ascertained that Ge-O bands can be detected at  $518$  and  $903\text{ cm}^{-1}$  for  $600^\circ\text{C}$  thermal oxidized sample, and Muthuswamy et al. stated that the Ge bands can be observed at  $510$ ,  $869$ ,  $1036$  and  $1515\text{ cm}^{-1}$  (Lei, Goh, Abidin, & Wong, 2017; Muthuswamy, Iskandar, Amador, & Kauzlarich, 2012).

In the process of peak matching, the resulting FTIR spectra are analyzed and compared based on the reference peak lists. The result is shown in Fig. 4.8 consolidated with Table 4.2. The results of the FTIR spectra fit to the reference data are listed in Table 4.2. As shown in Fig. 4.8, the vibrational mode associated with Ge-Ge at  $510\text{ cm}^{-1}$  is only observed for  $400$  and  $500^\circ\text{C}$  samples. However, there is no significant peak associated with Ge-Ge observed for  $600^\circ\text{C}$  sample. Meanwhile, there are two relatively intense Ge-O bands clearly observed at  $570$  and  $883\text{ cm}^{-1}$  in the spectrum for  $600^\circ\text{C}$  sample, which agrees well with the value reported in the previous studies. Contrastingly, relatively small peaks which are indicative of Ge-O bond are observed at  $561$  and  $903\text{ cm}^{-1}$  for  $500^\circ\text{C}$  sample. And by looking carefully at the spectra for  $400$  and  $500^\circ\text{C}$  samples, the  $400^\circ\text{C}$  sample is observed to have relatively large single Ge-O peak at  $903\text{ cm}^{-1}$  as compared to  $500^\circ\text{C}$  sample which can be understood as the concentration and the strength of the Ge-O band in  $400^\circ\text{C}$  sample is greater than that in  $500^\circ\text{C}$  sample.

Table 4.2: A summary table of results for peak filtering, fitting and matching

<b>Ge-Ge bond (cm<sup>-1</sup>)</b>	300	510	869	1036	1515	
<b>400°C</b>	-	<b>500</b>	-	-	-	
<b>500°C</b>	-	<b>510</b>	-	-	-	
<b>600°C</b>	-	-	-	-	-	
<b>Ge-O bond (cm<sup>-1</sup>)</b>	518	524	825	524~570	824~870	903
<b>400°C</b>	-	-	-	-	-	<b>903</b>
<b>500°C</b>	-	-	-	<b>561</b>	-	<b>903</b>
<b>600°C</b>	-	-	-	<b>570</b>	<b>883</b>	-
<b>Ge-N bond (cm<sup>-1</sup>)</b>	450	690	700	870	1100	
<b>400°C</b>	-	-	<b>705</b>	-	<b>1100</b>	
<b>500°C</b>	-	-	<b>700</b>	-	<b>1108</b>	
<b>600°C</b>	-	-	-	-	-	
<b>Ge-<sup>14</sup>N bond (cm<sup>-1</sup>)</b>	577	590	<b>Ge-<sup>15</sup>N bond (cm<sup>-1</sup>)</b>	559	573	
<b>400°C</b>	<b>577</b>	-	<b>400°C</b>	-	-	
<b>500°C</b>	-	-	<b>500°C</b>	<b>559</b>	-	
<b>600°C</b>	-	-	<b>600°C</b>	-	-	
<b>N-pair defects (cm<sup>-1</sup>)</b>	<sup>14</sup> N		<sup>14,15</sup> N		<sup>15</sup> N	
	660	825	654	810	641	801
<b>400°C</b>	-	-	<b>654</b>	<b>810</b>	-	-
<b>500°C</b>	-	-	<b>654</b>	<b>810</b>	-	-
<b>600°C</b>	-	-	-	-	-	-

From Fig. 4.8, it is clear that the resulting spectra do not show any peaks which signifying the presence of Ge-N bond for 600°C sample. Unlike 600°C sample, each spectrum of 400 and 500°C samples shows two consecutive Ge-N matched peaks at 705 and 1100 cm<sup>-1</sup> and 700 and 1108 cm<sup>-1</sup>, respectively. Besides, the stretching vibration mode of Ge-<sup>14</sup>N bond at 577 cm<sup>-1</sup> is clearly observed in the spectrum of 400°C sample, while the vibration mode is shifted to 559 cm<sup>-1</sup> for 500°C sample which is ascribed as the Ge-<sup>15</sup>N band. In the spectra of 400 and 500°C samples, the two major <sup>14,15</sup>N intermediate modes at 654 and 810 cm<sup>-1</sup> are also observed.

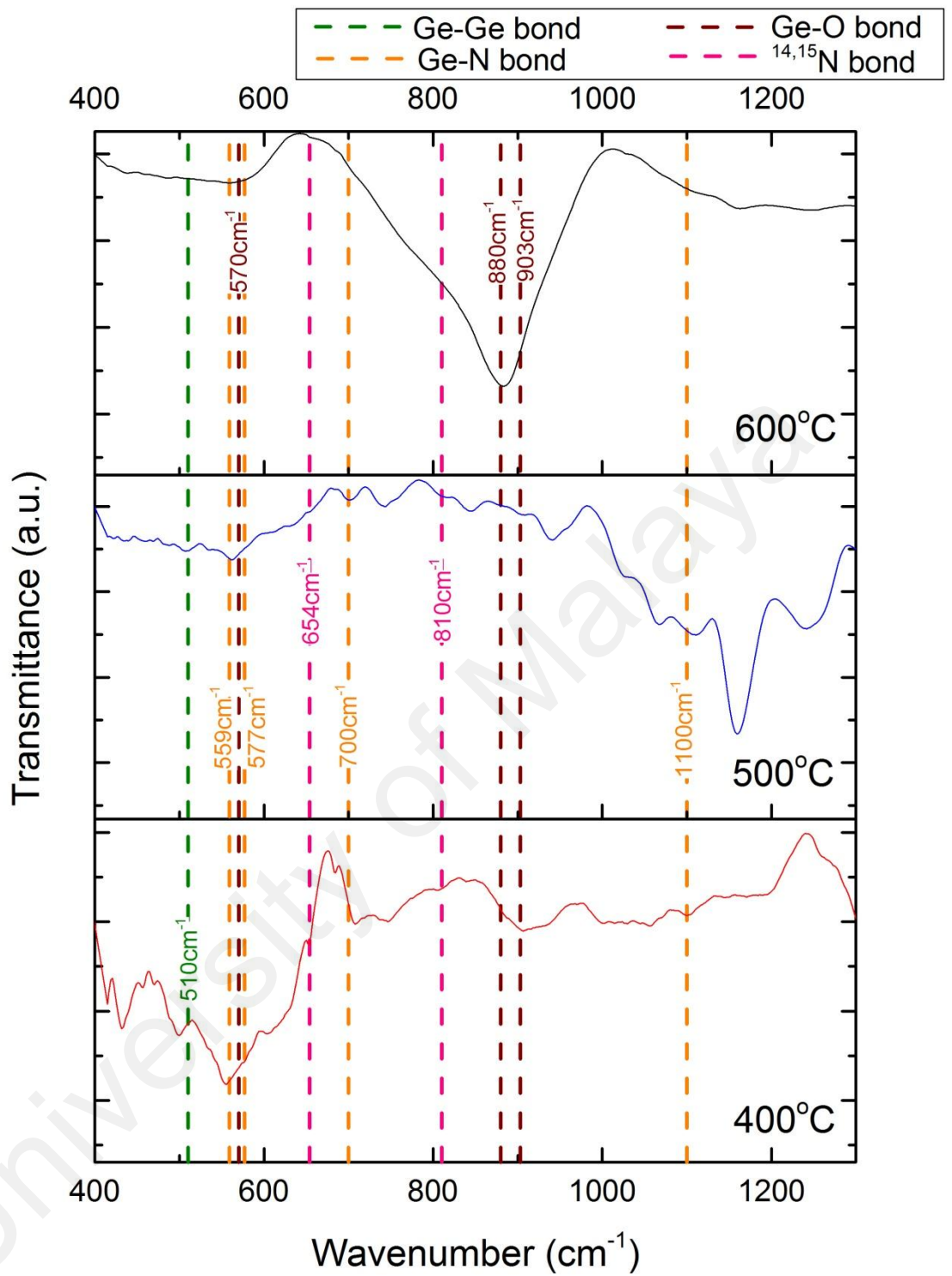


Figure 4.8: FTIR spectra of 400, 500 and 600°C thermally nitrated samples in the spectral range of 400-1300  $\text{cm}^{-1}$

Compared to the previous studies, a consensus pattern can be deduced from the present FTIR results. As thermal nitridation temperature increased up to 600°C, the

transmittance of the Ge-O bands increases, while the frequency shifts toward lower wavenumber. The increase in transmittance is attributed to the increase in Ge-O bonds which indicates the further formation of GeO<sub>2</sub>. Furthermore, the slight red shift can be explicated by the effect of structural defects on atomic scale, for example, oxygen deficiency. Since the thin films are deposited under nitrogen purging, the oxygen concentration will become a limiting factor. The red shift suggests the stoichiometric composition of GeO<sub>2</sub> has changed to Ge-O-Ge which is an oxygen-deficient structure (Wolf, Christensen, Coit, & Swinford, 1993). Moreover, the Ge-<sup>14</sup>N and Ge-<sup>15</sup>N bands observed in 400°C and 500°C samples, respectively, is consistent with the existing literature results which demonstrate the shift of Ge-<sup>14</sup>N to Ge-<sup>15</sup>N upon increasing temperature. Also, the two intermediate mixed isotropic modes which arise from the pair defects of <sup>14</sup>N and <sup>15</sup>N isotopes appearing in the spectra of 400 and 500°C samples demonstrate the different phases of N<sub>2</sub> incorporating into Ge to form Ge<sub>3</sub>N<sub>4</sub> thin films.

## CHAPTER 5: CONCLUSION

In this research study, Ge is thermally nitrided with  $N_2$  gas and the growth of  $\gamma$ - $Ge_3N_4$  layer has been triggered with the purpose of suppressing the growth of unwanted low  $\kappa$   $GeO_2$  layer. This research study has examined whether it is possible to thermally grow  $\gamma$ - $Ge_3N_4$  layer on Ge. The results have shown that  $\gamma$ - $Ge_3N_4$  phases have been successfully introduced on the Ge substrate in the temperature range of 400 to 600°C. The physical, chemical and compositional characterizations have been carried out using XRD and FTIR spectroscopy to propose an optimal thermal nitridation temperature to obtain an optimum  $\gamma$ - $Ge_3N_4$  buffer layer. The present findings confirm that 500°C is the optimal thermal nitridation temperature at which considerably growth of  $\gamma$ - $Ge_3N_4$  films can be bechanced with considerably higher intensity in the  $\gamma$ - $Ge_3N_4$  phases despite a fairly small amount of  $t$ - $GeO_2$  phases is found.

In addition, these findings provide additional information about the intensity and crystallite size of  $\gamma$ - $Ge_3N_4$  and  $t$ - $GeO_2$  grown at various temperatures. The intensities of  $\gamma$ - $Ge_3N_4$  phases are found to first increase from 400°C and reach a peak at 500°C, gradually declining thereafter at 600°C. This suggests that the optimum growth of  $\gamma$ - $Ge_3N_4$  phases is at 500°C, and the  $\gamma$ - $Ge_3N_4$  phases are appeared to be unstable at 400 and 600°C. The  $\gamma$ - $Ge_3N_4$  exhibits the largest crystallite size and highly homogeneous size distribution at 500°C indicating the highly uniform growth rate at 500°C. Importantly, the XRD results provide evidence that tensile and compressive microstrains are introduced and embedded in  $\gamma$ - $Ge_3N_4$  and  $t$ - $GeO_2$  phases during the thermal nitridation process. Nevertheless, the FTIR findings appear consistent with XRD findings showing that both spectra of 400 and 500°C samples show a substantial number of Ge-N characteristic peaks consecutively over the wavenumber range of 400

to  $1300\text{ cm}^{-1}$ . Unlike 400 and  $600^\circ\text{C}$  samples, relatively small peaks which are indicative of Ge-O bond are observed at the spectrum of  $500^\circ\text{C}$  sample.

Future research on the temperature dependence of solubility of oxygen in germanium might extend the explanations of the effectiveness of  $\gamma\text{-Ge}_3\text{N}_4$  buffer layer for  $\text{GeO}_2$  interfacial layer suppression. Also, the effects of crystallite size of  $t\text{-GeO}_2$  and  $\gamma\text{-Ge}_3\text{N}_4$  on dielectric properties nitrided Ge should be considered in future research to refine the present findings. Also, it will be significant that future research involves more characterization methods, for example Raman, TEM and XPS spectroscopy to investigate a wide range of potential parameters and variables such as roughness, thickness and electrical properties of the films nitrided on Ge substrate. As also recommended above, future research should explore more alternative approaches to grow a uniform thin  $\gamma\text{-Ge}_3\text{N}_4$  buffer layer which is highly effective in suppressing the growth of unwanted  $\text{GeO}_2$  interfacial layer.

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