

**FORMATION OF GERMANIUM OXYNITRIDE AS
BUFFER LAYER ON GERMANIUM SUBSTRATE**

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KUALA LUMPUR

2018

FORMATION OF GERMANIUM OXYNITRIDE AS BUFFER LAYER
ON GERMANIUM SUBSTRATE

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RESEARCH PROJECT SUBMITTED TO THE
FACULTY OF OF ENGINEERING
UNIVERSITY OF MALAYA, IN PARTIAL
FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF MASTER OF
MATERIALS ENGINEERING

2018

UNIVERSITY OF MALAYA
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**FORMATION OF GERMANIUM OXYNITRIDE AS BUFFER LAYER ON
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ABSTRACT

Thermal oxynitridation process was used to grow germanium oxynitride, GeON thin films as a buffer layer on the germanium substrates in nitrous oxide (N_2O) gas ambient at several temperatures: 400 °C, 500 °C and 600 °C. The physical and chemical properties of the buffer layers formed were characterized and investigated using X-ray diffraction (XRD) and Fourier transform infrared (FTIR). The XRD patterns showed the crystallinities that belongs to the germanium dioxide (GeO_2), gamma-germanium nitride ($\gamma-Ge_3N_4$) and digermanium dinitrogen oxide (Ge_2N_2O). Digermanium dinitrogen oxide was formed at 600 °C and its peaks were detected at 31.58° and 65.92° corresponding to planes (110) and (220) respectively in XRD pattern. Meanwhile, peaks indicating the presence of germanium oxide and gamma-germanium nitride were found in XRD pattern for all the samples. GeO_2 were detected in XRD patterns at 28.9° , 35.5° , 42.6° and 47.0° corresponding to (110), (111), (200) and (210). $\gamma-Ge_3N_4$ were also found in the XRD patterns at 38.83° , 47.97° corresponding to planes (110), (111). FTIR detected the Ge_2N_2O absorption peak at 800 cm^{-1} at 600 °C sample, thus confirming the formation of Ge_2N_2O on the germanium substrate at 600 °C.

Keywords: gate oxides, buffer layer, germanium oxynitride, passivation, thermal oxynitridation

PEMBENTUKAN GERMANIUM OXYNITRIDA SEBAGAI LAPISAN PENYANGGA PADA SUBSTRAT GERMANIUM

ABSTRAK

Proses oksidasi-nitridasi secara termal digunakan untuk menumbuhkan lapisan nipis germanium oxynitrida, GeON sebagai lapisan penampan pada substrat germanium dengan penggunaan gas nitro oksida (N_2O) pada suhu yang berbeza iaitu: 400 °C, 500 °C dan 600 °C. Ciri-ciri fizikal dan kimia lapisan penampan yang dibentuk telah pun diselidik dengan menggunakan X-ray difraksi (XRD) dan Fourier transform infra merah (FTIR). Hasil XRD pula menunjukkan bentuk kristal yang dimiliki oleh germanium dioksida (GeO_2), gamma-germanium nitrida ($\gamma-Ge_3N_4$) dan digermanium dinitrogen oxide (Ge_2N_2O). Digermanium dinitrogen oksida dibentuk pada 600 °C dan puncaknya dikesan pada 31.58 ° dan 65.92 ° bersamaan dengan fasa (110) dan (220) masing-masing dalam XRD. Sementara itu, puncak yang menunjukkan kehadiran germanium oksida dan gamma-germanium nitrida dalam hasil XRD dalam semua sampel. GeO_2 dikesan dalam hasil XRD pada 28.9 °, 35.5 °, 42.6 ° dan 47.0 ° bersamaan dengan fasa (110), (111), (200) dan (210). $\gamma-Ge_3N_4$ pula didapati dalam hasil XRD pada 38.83 °, 47.97 ° sepadan dengan fasa (110), (111). FTIR telah pun mengesan puncak penyerapan bagi Ge_2N_2O pada 800 cm^{-1} di dalam sampel 600 °C, maka ia pun juga mengesahkan pembentukan Ge_2N_2O pada substrat germanium semasa suhu 600 °C.

Kata Kunci: pintu oksida, lapisan penyangga, germanium oxynitrida, passivasi, oksidasi-nitridasi secara termal

ACKNOWLEDGEMENTS

First of all, I would like to express my special gratitude to my research project supervisor, Ir Dr Wong Yew Hoong who provided me guidance throughout the entire research study. I truly appreciate for his useful advices and suggestion in improving this research study.

Besides, I would also like to offer my warm thanks to Mr Tahsin, PhD student under supervision of Ir Dr Wong Yew Hoong for his constructive advices and guidance. His patient guidance helped me to complete this research project.

My sincere appreciations also go to all the academic and administrative staffs of Faculty of Engineering, University of Malaya who provided me assistances and support during my research project.

Lastly, I would like to express my deepest appreciations to my beloved parents for their supports and encouragement. Their devotion and supports always gave me the courage to complete this research study successfully.

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Table 1.1: Properties of germanium and silicon.

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LIST OF SYMBOLS AND ABBREVIATIONS

E_g	:	Bandgap, (eV)
X	:	Electron affinity (eV)
μ_{th}	:	Hole mobility ($\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$)
μ_e	:	Electron mobility ($\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$)
k	:	Dielectric constant
T_m	:	Melting point ($^{\circ}\text{C}$)
a	:	Lattice constant
$I_{D(sat)}$:	Saturation drive current
W	:	Gate width
C_{ox}	:	Gate oxide capacitance per area
V_{GS}	:	Gate-to-oxide bias
V_{th}	:	Threshold voltage of the transistor
V_{inj}	:	Injection velocity of carriers
V_T	:	Thermal velocity
μ_n	:	Low field mobility
$E(0^+)$:	Electric field at the channel 0 plus (source terminal)
C	:	Gate capacitance
ϵ_0	:	Permittivity of free space

A	:	Capacitance area
t_{ox}	:	Gate oxide thickness
t_{hi-k}	:	Physical thickness of high- k material
t_{IL}	:	Physical thickness of interfacial layer
k_{hi-k}	:	Dielectric constant of high- k material
k_{IL}	:	Dielectric constant of interfacial layer
d	:	Interplanar spacing (nm)
D	:	Crystalline size (nm)
K	:	Shape factor
λ	:	Wavelength (cm^{-1})
β_D	:	Peak width with half maximum intensity
ε	:	Microstrain
D_{it}	:	Interface trap density ($\text{eV}^{-1} \text{cm}^{-2}$)
B_s	:	Width at half maximum intensity
IL	:	Interfacial layer
EOT	:	Equivalent oxide thickness
ITRS	:	International Technology Roadmap for Semiconductors
MOSFET	:	Metal-oxide semiconductor field-effect transistor
PVD	:	Physical vapor deposition
CVD	:	Chemical vapor deposition

ALD	:	Atomic layer deposition
MDB	:	Molecular beam deposition
ICDD	:	International Centre for Diffraction Data
FTIR	:	Fourier transform infra-red
XRD	:	X-ray diffraction

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CHAPTER 1

INTRODUCTION

1.1 Background of study

Germanium (Ge)-based metal-oxide-semiconductor field-effect transistors (Ge-MOSFETs) have caught the attention of researchers to be the most potential candidate for the next-generation MOSFETs as replacing Si-based MOSFETs in the current technology platform. This is mainly due to the fact that after so many years of Si-MOSFET orientated researches, the performance of silicon (Si) as the channel materials for MOSFET is getting to reach a plateau due to physical and technological limit. As such, germanium as one of the new channel materials with high carrier mobility is studied and investigated as the alternatives to achieve new microelectronics devices (Goley & Hudait, 2014). Electrons move nearly 3 times as readily in germanium if compared to that in silicon. In addition, the holes, positive charges carrier move about 4 times as easily in germanium if compared with silicon (as shown in Table 1.1). Figure 1.1 shows that both the Ge (100) and Ge (110) have a better intrinsic hole mobility and far more scalable if compared to Si (100) and Si (110) (Kuhn, 2012). Indeed, the remarkable carrier mobility shown in germanium makes it a suitable material used to replace Si in the transistor's current carrying channel.

Table 1.1: Properties of germanium and silicon (Kamata, 2008).

Properties	Ge	Si
Bandgap, E_g (eV)	0.66	1.12
Electron affinity, χ (eV)	4.05	4.0
Hole mobility, μ_h ($\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$)	1900	450
Electron mobility, μ_e ($\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$)	3900	1500
Dielectric constant, k	16.0	11.9
Melting point, T_m ($^\circ\text{C}$)	937	1412
Lattice constant, a (nm)	0.565	0.543

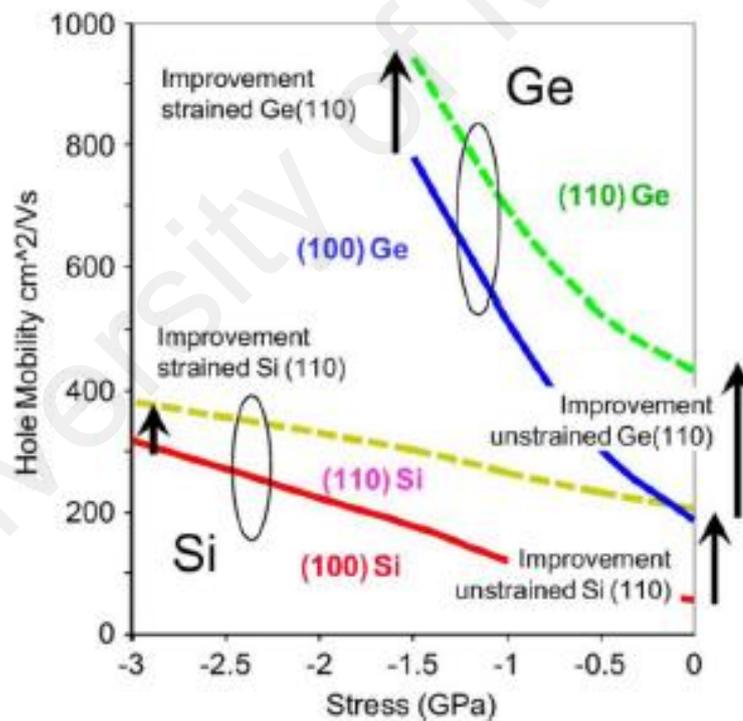


Figure 1.1: Hole mobility of Si and Ge as function of stress and wafer orientation (Kuhn, 2012).

As mentioned earlier, the main reason of searching for alternate to Silicon is about the mobility. It can be explained using equation as follow:

$$I_{D(\text{sat})} = W C_{\text{ox}} (V_{\text{GS}} - V_{\text{th}}) V_{\text{inj}}$$

Where $I_{D(\text{sat})}$ is the saturation drive current; W is the gate width; C_{ox} is the gate oxide capacitance per area; V_{GS} is the gate-to-oxide bias; V_{th} is the threshold voltage of the transistor and V_{inj} is the injection velocity of carriers.

Basically, there is an ultimate scaling limit on max $I_{D(\text{sat})}$ for Si MOSFET which is controlled by the injection velocity, V_{inj} of carriers into channel from the source. In order to attain higher drain current for driving the capacity loads, normally the thickness of gate oxide is reduced, but it is up to certain limit.

By referring to formula below, it is seen that injection velocity is dependent on the thermal velocity and low field mobility and the electric field at the channel 0 plus (source end of junction or trans source end):

$$\frac{1}{V_{\text{inj}}} = \frac{1}{V_{\text{T}}} + \frac{1}{\mu_{\text{n}} E(0^+)}$$

Where V_{T} is the thermal velocity; μ_{n} is the low field mobility and $E(0^+)$ is the electric field at the channel 0 plus (source terminal).

Consequently, it is necessary to find the materials with higher mobility, particularly germanium to replace the conventional channel material (Silicon) as to improve the injection velocity.

It is important to note that for the sake of miniaturization of electronic devices, pushing the transistor size to approach tens of nanometers is really important, however, this requires the physical thickness of gate oxide to be thinner than the limits for electron tunnelling (notably thickness limit is around 2 nm), but this will cause the gate leakage current density to become unbeatably high (Kamata, 2008). Therefore, it is a must to replace the Si with a material with higher mobility (able move current at a faster rate) in order to make high speed and low power circuit (Ye, 2016).

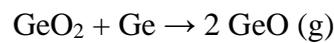
1.2 Problem statement

There are several challenges in fully adoption of germanium as the channel material. One of the challenges is germanium has a melting point which is lower than 934 °C as the conventional poly-Si gate electrodes requires high temperature greater than 900 °C for dopant activation. Therefore, metal gate electrode would be deployed in Ge MOSFET (Kamata, 2008).

The real challenge of using Ge channel is that gate insulators with high dielectric constant (high- k) are required to suppress the gate leakage and short channel effect. In Si MOSFET, silicon substrate contains its own native insulator (silicon dioxide) which is well matches with its crystal structure. In addition, the silicon dioxide is inert and has good insulating properties, thus making it an ideal material used to passivate Si channel. Adversely, although germanium has its own native oxides which are germanium oxide (GeO) and germanium dioxide (GeO₂). Some studies shown that GeO₂ has some good promising passivation properties (Xie *et al.*, 2012). More recently, it has been found that

GeO₂ can serve as an effective interfacial layer, *IL* and the quality of the interface is strongly dependent on how the interfacial oxide is formed (Delabie *et al.*, 2007; Toriumi *et al.*, 2009; Toriumi *et al.*, 2011).

GeO₂ is thermally instable especially when the annealing temperature increases from 250 °C to 420 °C (Prabhakaran *et al.*, 2000). GeO₂ tends to undergo transformation to become GeO:



In addition, GeO is subjected to volatilization at approximately 425 °C, causing GeO to desorb from the substrate surface as shown in Figure 1.2. Thus, GeO_x/Ge interface is less thermodynamically stable and using GeO₂/Ge gate stack will cause gate dielectric instability unless the issue dealt with the GeO volatilization is solved.

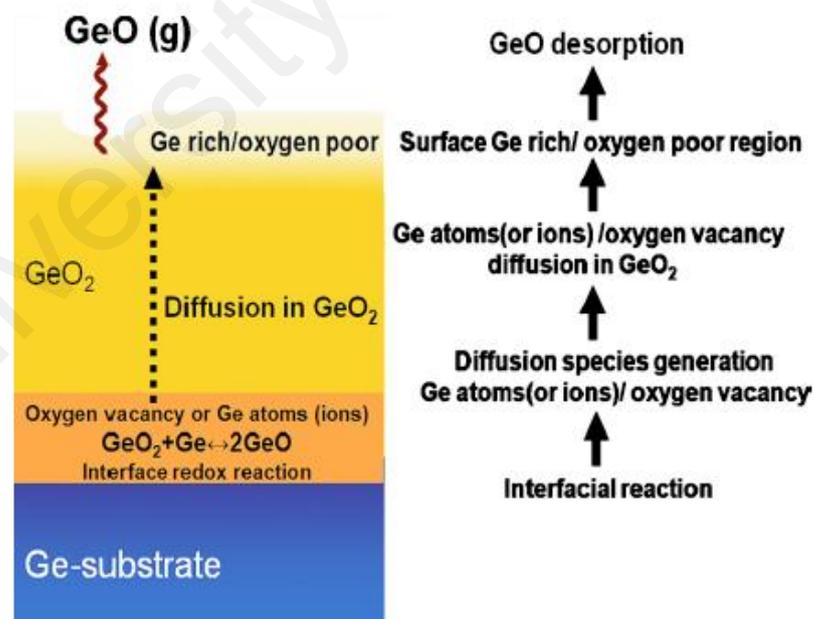


Figure 1.2 : Schematic diagram of GeO desorption mechanism in GeO₂/Ge gate stack (Wang *et al.*, 2010).

As such, a passivation layer/buffer layer that acts as diffusion barrier is required to capping the GeO_2 to prevent GeO volatilization. Other than GeO_2 , other passivation layers like GeON also is a very good high- k material to be used to passivate the Ge channel. Therefore, GeON is suggested to be used as a buffer layer to suppress the Ge volatilization as shown in Figure 1.3.

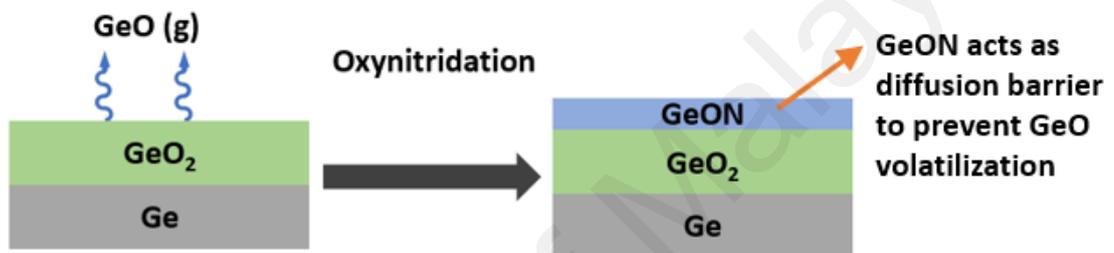


Figure 1.3: Schematic illustration of formation of GeON buffer layer on the top GeO_2/Ge .

However, there is another issue that present in high- k materials/ Ge gate stack. The Ge from Ge layer will also tend to diffusion into the high- k materials and this will affect the electrical properties of high- k materials. Therefore, instead of growing GeON on GeO_2 surface, this study focuses on growing the GeON as a buffer layer to suppress the Ge-up diffusion into high- k materials. Ge-up diffusion into the dielectric can severely degrades the MOSFET performance (Lu *et al.*, 2005; Bai *et al.*, 2006).

In this study, the formation of GeON thin films on the Ge substrate as buffer layer using thermal oxynitridation is carried out in nitrous oxide gas, N_2O ambient at several temperatures as shown in Figure 1.4.

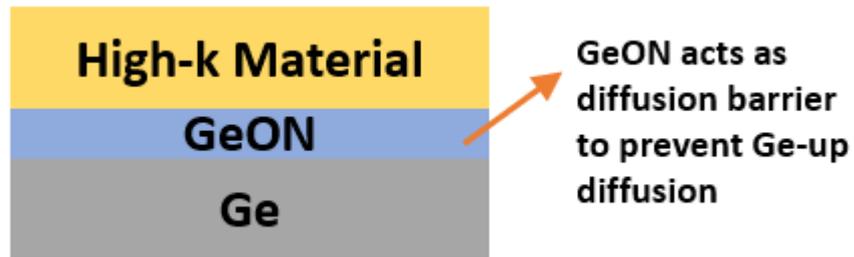


Figure 1.4: Schematic illustration of GeON buffer layer at high- k /Ge stack interface.

1.3 Objectives of study

The main objective of this research is to grow germanium oxynitride, GeON thin films as a buffer layer on the germanium substrates by thermal oxynitridation in nitrous oxide gas, N_2O ambient. Basically, the objective of this research can be sub-divided into:

1. To identify the optimal temperature for thermal oxynitridation using N_2O gas ambient to form passivation layer/buffer layer on the germanium substrates.
2. To identify the chemical properties and crystallinity of the components of the passivation layer/buffer layer formed on germanium substrate.
3. To evaluate the thermal oxynitridation process used to grow buffer layer in N_2O gas ambient.

1.4 Scope of study

In this study, thermal oxynitridation was carried out at various temperatures, particularly 400 °C, 500 °C and 600 °C in a nitrous oxide (N₂O) gas ambient to grow buffer layer on germanium substrates as shown in Figure 1.5.

The thermally oxynitrided samples were then further characterized using X-ray diffraction (XRD) and Fourier transformed infrared (FTIR) analysis to investigate the physical and chemical properties of the passivation layer/buffer layer formed on the samples.

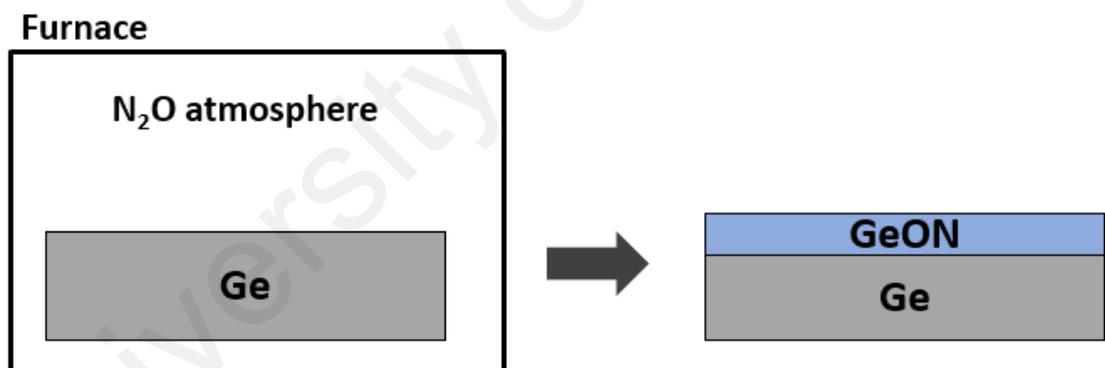


Figure 1.5: Simplified illustration of thermal oxynitridation of Ge substrate.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Recently, Ge has been reintroduced to be the most promising channel material in MOSFET. The high-permittivity (k) gate oxide/ Ge seems to be the key for future nanoscale devices. However, this gate stack technology of using high- k gate oxide/ Ge is one of the most critical obstacles that need to be realised to fabricate Ge MOSFET. To develop a scalable high- k /Ge gate stack in MOSFET, it requires the good interfaces and insulating layer on Ge.

2.2 High- k /Ge gate stack

Basically, high- k oxides are referred as the oxides with high dielectric constant k . Its most important function nowadays is to be used as alternative to replacing silicon dioxide as gate insulator in MOSFET as to allow greater physical thickness of dielectric material between the gate and channel without degrading the gate capacitance. This is because as the transistor decreases in size with time, the conventional gate oxide (silicon dioxide) also need to reduce its physical thickness to increase the gate capacitance and current drive force to achieve greater performance. However, the silicon oxide thickness is said to be reaching its limit at its oxide thickness below 2 nm where there are leakage currents take place due to exponential increasing in tunnelling current, resulting in excessive power dissipation and deterioration of device integrity. The reasoning of

implementation of high- k materials into gate stacks can be well described using the formula of gate capacitance as below:

$$C = \frac{\epsilon_0 k A}{t_{\text{ox}}}$$

Where C is the gate capacitance; k is the dielectric constant; ϵ_0 is the permittivity of free space; A is the capacitance area; t_{ox} is the gate oxide thickness.

In short, in order to increase gate capacitance(C), the only way is to increase the dielectric constant value (k), given that the Area (A) is fixed and the oxide thickness (t_{ox}) cannot go downscaling any further.

Currently, there are several methods available for deposition of high- k material onto the Ge substrates, such as physical vapor deposition (PVD) (Bai *et al.*, 2006), chemical vapor deposition (CVD) (Bai *et al.*, 2006; Lu *et al.*, 2005; Wu *et al.*, 2004), atomic layer deposition (ALD) (Delabie *et al.*, 2005) and molecular beam deposition (MDB) (Seo *et al.*, 2005).

2.3 Equivalent oxide thickness (EOT)

Another important concept that related to gate stack technology is the equivalent oxide thickness (EOT). In some literatures, EOT is commonly known as the thickness (in nanometer) that required by silicon oxide film (gate oxide film) to be produce the similar effect like high- k material does. However, EOT is practically used as assess the gate capacitance for the gate oxide since silicon dioxide is no longer the only gate oxide used

in microprocessor (Goley & Hudait, 2014). Basically, EOT takes into consideration of the presence of the Interfacial Layer (IL) with good quality and the high- k material as the gate oxide. It can be modelled as equation as below:

$$EOT_{\text{total}} = \left(\frac{3.9}{k_{\text{hi-k}}}\right) t_{\text{hi-k}} + \left(\frac{3.9}{k_{\text{IL}}}\right) t_{\text{IL}}$$

Where k and t are the dielectric constant and physical thickness of high- k material (hi- k) and interfacial layer (IL) respectively.

According to Goley and Hudait (2014), the requirements for gate oxide stack can be summarized as below:

1. A low EOT is required (the International Technology Roadmap for Semiconductors, ITRS calls for an EOT of 1.18 nm for Ge FET devices by 2018);
2. Thermodynamically and kinetically stable (Robertson, 2004);
3. At least 1 eV for both the conduction band offsets and valence band offsets;
4. Having leakage current density lower than 1.5×10^{-2} A/cm² (Robertson, 2004);
5. High channel mobility;
6. Good IL with low interface trap density, $D_{\text{it}} < 10^{11}$ cm⁻² eV;
7. High dielectric breakdown electric field (Choi, Mao & Chang, 2017).

2.4 Interfacial layers and passivation methods

Interfacial layer (IL) is the passivating layer that is introduced at the interface between the high- k material and the channel at the transistor gate. This is because the

direct deposition of high- k oxide onto the Ge Channel normally causes the poor interface between high- k material and channel, leading to formation of high density of deformed defects especially at high- k material site. This issue is detrimental to performance of MOSFET. Therefore, a good *IL* material is required to shield and passivate the Ge channel as to maintain the intrinsic carrier mobility of Ge channel. Normally, the *IL* material is required to have lower dielectric constant and able to create a good interface with the channel material (an interface with lesser defects).

The quality of an interface is determined based on the interface trap density D_{it} that usually obtained through capacitance-voltage (C-V) characteristics or conductance-voltage characteristics (Martens *et al.*, 2008; Schroder, 2005). Interface trap density, D_{it} is usually reported as a function of energy level and it is calculated as the number of trapped charges per cm^2 per eV.

Briefly, *IL* is used to passivate the surface of channel material effectively (which normally characterized with low interface trap density, D_{it} and ability to preserve intrinsic carrier mobility of the channel material) and also its possibility to be fabricated at the lowest *EOT* cost (Goley & Hudait, 2014).

Basically, there are several types of passivation of Ge substrate being reported over the years, for instances: Germanium dioxide (GeO_2) passivation, Si passivation, Sulphur passivation, Fluorine passivation, Germanium oxynitride (GeON) passivation and Germanium nitride (Ge_3N_4) passivation. GeO_2 passivation and Si passivation are the two most well-developed methods used to passivate germanium surface so far.

2.4.1 Germanium dioxide (GeO₂) passivation:

The idea of using GeO₂ as the passivation layer on Ge substrate is greatly influenced by the success of using SiO₂ as the passivation layer in Si MOSFET for decades as both are the native oxide to its own channel materials. However, there are some difficulties in using GeO₂ to passivate the Ge substrates. One of the greatest challenges in using GeO₂ as passivating layer is the thermal instability of GeO₂/Ge interface and it is considerably less thermodynamically stable if compared to SiO₂/Si (Goley & Hudait, 2014). This is because GeO₂ tends to decompose into GeO at around 425°C:



GeO volatilisation can result in poor electrical properties of GeO₂ and formation of defects.

Besides, in term of interfacial quality, SiO₂/Si interface can easily obtain interface trapped density, D_{it} of approximately $10^{10} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ while GeO₂/Ge interface can hardly get an interface trapped density, D_{it} of $10^{11} \text{ cm}^{-2} \cdot \text{eV}^{-1}$. But still, GeO₂ is still one of the promising candidates as passivation layer for Ge and the quality of interface can be improved through optimisation of thermal processing and some postgate treatments (Xie, He & Zhu, 2008).

Delabie *et al.* (2007) demonstrated that thermally grown GeO₂ with good passivation properties in O₂ ambient. Oxidation of Ge samples at 450°C after 5 min and 18 min were able to yield a GeO₂ layer with thickness of 1.3nm and 2.3nm respectively.

Meanwhile, 1.1 nm thick of GeO₂ was successfully grown at 350°C with duration of 60 min. The interface trap density of p-Ge/GeO/HfO₂ obtained from conductance measurement is about $3 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$, a considerably low D_{it} approaching to that of Si/SiO_x/HfO₂/metal gate stacks. Besides, the capacitance-voltage characteristics of p-Ge/GeO_x/HfO₂ and p-Ge/GeO_x/Al₂O₃ gate stacks shows well and smooth CV curves, indicating less electrical distortions in the Ge/GeO_x. The equivalent oxide thickness, EOT estimated from C-V characteristics for p-Ge/GeO_x/HfO₂ and p-Ge/GeO_x/Al₂O₃ gate stacks are about 1.5 nm and 2.4 nm respectively (EOT contribution for GeO_x is about 0.8 nm).

Besides, Zhang *et al.* (2012) also demonstrated the fabrication of Al₂O₃/GeO_x/Ge gate stack with a relatively low EOT (particularly 1 nm) using plasma post oxidation. Basically, in the experiments of Zhang *et al.* (2012), the plasma oxidation process was used to grow GeO_x as the IL for Al₂O₃/Ge gate stack. Zhang *et al.* (2012) were to find out that if they can manipulate the thickness of the GeO_x IL by controlling the Al₂O₃ thickness. Apart from that, Zhang *et al.* (2012) also identified that the interface state density, D_{it} of GeO_x/Ge interface is related to the GeO_x IL thickness as shown in Figure 2.1 and Figure 2.2. In short, Zhang *et al.* (2012) were able to demonstrate an EOT of about 1 nm and D_{it} of $1 \times 10^{11} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ using a Al₂O₃/GeO_x/Ge gate stack.

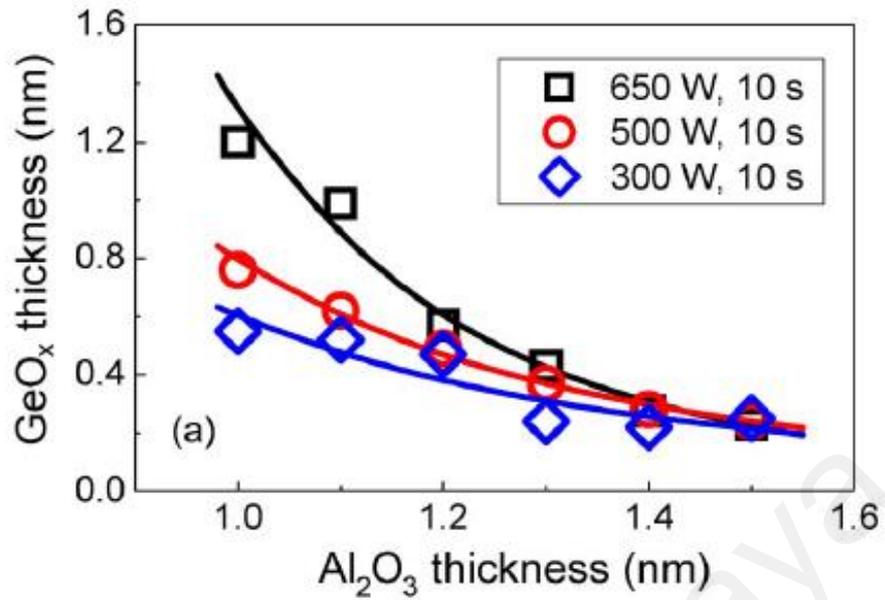


Figure 2.1: Relationship between the thickness of GeO_x ILs with thickness of Al₂O₃ layer in various plasma power (Zhang *et al.*, 2012).

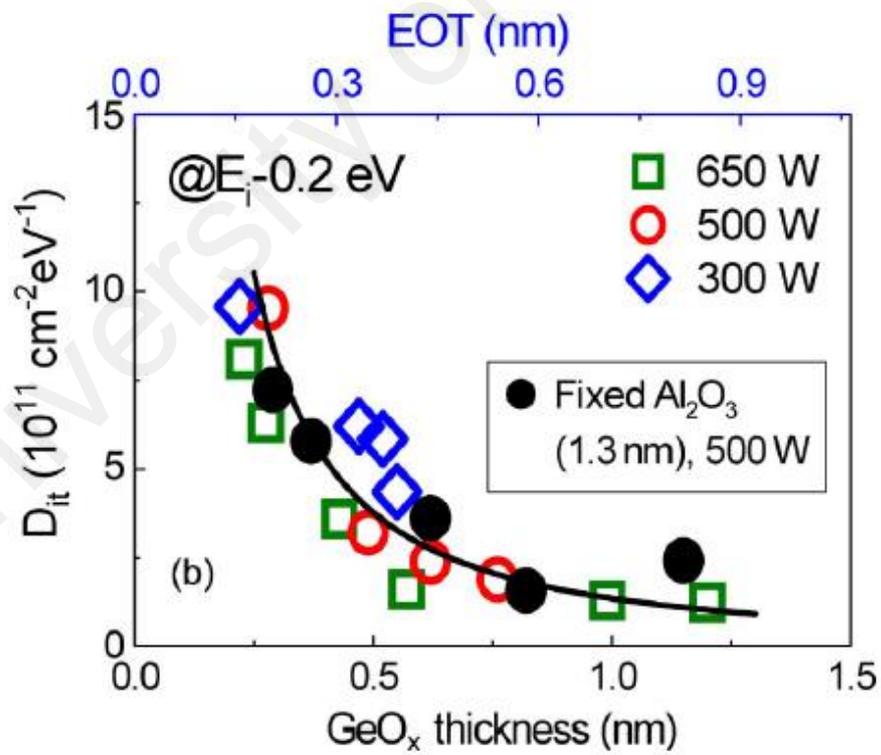


Figure 2.2: Relationship between D_{it} with the thickness of GeO_x IL (Zhang *et al.*, 2012).

2.4.2 Silicon (Si) passivation:

In passivation of germanium surface using silicon, normally silicon precursor is sacrificed to deposit silicon dioxide on the Ge substrate to form $\text{SiO}_2/\text{Si}/\text{Ge}$. However, there is a flaw of using Si passivation as there is about 4% lattice mismatch in between Ge and Si if using Si/Ge gate stack. Apart from that, it was also found that Ge can diffuse into Si layer and degrades the performance of the electronic device.

Pillarisetty *et al.* (2010) demonstrated a thin silicon cap was formed at the gate dielectric interface to prevent carrier spill-out effect in the Ge FET. Their study shows that a sample without the Si *IL* or Si capping suffer 10 times slower in mobility if compared with the sample with 0.6 nm Si capping. Besides, they also learnt that although thinning the Si cap to 0.6 nm will improve the gate capacitance, there is a limit to the thinning of the Si cap as the thickness decreases, the potential barrier of the Si cap may not prevent carrier spill out issue.

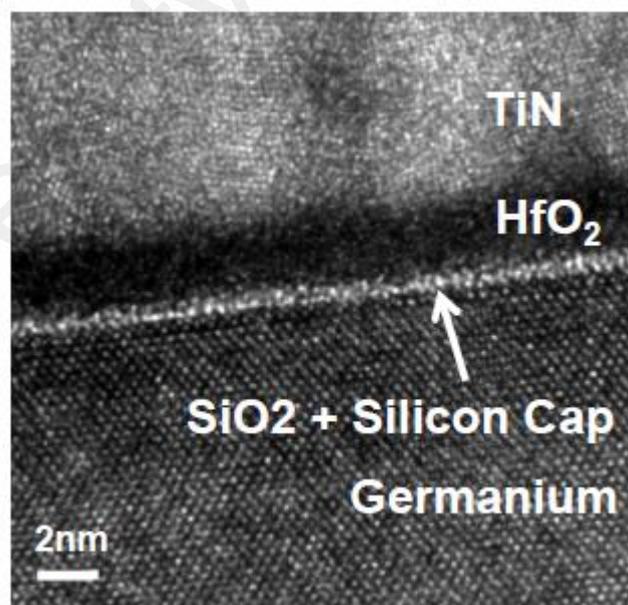


Figure 2.3: Cross-sectional TEM image of a thin Si layer being capped in between the high-*k* metal gate stack from germanium (Pillarisetty *et al.*, 2010)

2.4.3 Germanium oxynitride (GeON) passivation

Lu *et al.* (2005) found that nitridation of Ge surfaces prior to high- k film deposition is useful in suppressing Ge diffusion in metal oxides and thus improving performance of Ge-based devices. However, the surface nitridation and formation of GeON dielectric layers using annealing in NH_3 ambient can cause the piling up of nitrogen particles at the GeON/Ge interface which can weaken the interface properties.

As such, Kutsuki *et al.* (2009) demonstrated the formation of GeON layer on Ge(100) by using plasma nitridation of thermally grown germanium oxide (GeO_2). Au/GeON/Ge gate stack with relatively low EOT (1.7 nm) was fabricated while keeping low leakage from happening. The interfacial layer produced (GeON) also had low interface state density which is around $3 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. The results showed the promising method of converting the reactive surface of GeO_2 into GeON as a nitride capping or barrier layer using plasma nitridation. The nitride capping is able to retain the electrical properties at the bottom interfaces, thus preventing degradation of device performance.

CHAPTER 3: METHODOLOGY

3.1 Introduction

This chapter presents and describes the materials used and the methodology of the study. Basically, this chapter consists of three main parts which are:

- (i) Materials;
- (ii) Experimental procedures;
- (iii) Material characterization techniques.

3.2 Materials

3.2.1 Substrate material

The substrate material used in this study consists only of Ge wafers. These Ge wafers were purchased from Wafer World, Inc. The details of Ge wafers are shown as below:

- (i) *n*-type,
- (ii) (100)-orientated,
- (iii) Resistivity: 0.005 - 0.02 Ω cm
- (iv) Thickness: 500-550 μ m
- (v) Single-side surface polished

3.2.2 Chemicals used in Ge substrate pre-cleaning process

The chemical used in Ge substrate cleaning process are hydrofluoric acid and acetone. Hydrofluoric acid, HF (Assay \geq 49%) was supplied by R&M Chemicals (Chemical Abstracts Service, CAS number of 7664-39-3). Acetone, (CH₃)₂CO (Array > 99%) was supplied by R&M Chemicals with CAS Number of 67-64-1.

3.2.3 Gaseous materials used in thermal oxynitridation process

Nitrous oxide gas (N₂O) was the only gas being applied throughout the thermal oxynitridation process. It was supplied by Gaslink with CAS Number of 10024-97-2. Its purity is about 99.99%.

3.3 Experimental procedures

3.3.1 Preparation of substrate samples and pre-cleaning process

Ge wafers were cut into a 1 cm² of square shape using diamond cutter. A diluted HF solution with ratio 1:50 of HF to H₂O.

Pre-cleaning process was carried out by dipping the Ge wafers into the diluted HF solution for 15 seconds. After that, the Ge wafers were rinsed with deionized (DI) water. The pre-cleaning process was conducted to remove the unwanted native oxides (GeO_x) from the Ge wafers surface.

3.3.2 Thermal oxynitridation of pre-cleaned Ge substrates in N₂O gas ambient

Thermal oxynitridation of all the Ge samples were carried out inside the Carbolite CTF tube in a N₂O gas ambient. The thermal oxynitridation experiments were designed to be carried out at temperatures of 400 °C, 500 °C and 600 °C with time duration of 15 minutes each. Nitrous oxide (N₂O) gas was introduced into the quartz tube of furnace at flow rate of 150 mL min⁻¹ throughout each experiment. After the thermal oxynitridation process, the samples were cooled down to room temperature in the tube furnace before removal.

3.4 Material characterizations techniques

3.4.1 X-ray diffraction (XRD)

XRD is a powerful technique used for the phase identification of crystalline materials. It is also used to characterize thin films as to determine their lattice structure and thickness. Basically, XRD is a technique based on the constructive interference (that satisfies Bragg's Law) of monochromatic X-ray and the crystalline material. X-rays are generated and directed towards the sample, then the diffracted X-rays coming from the samples are detected and analysed. Based on Bragg's law, an equation can be derived as below:

$$n \lambda = 2 d \sin \theta$$

where n is the integer no of wavelength; λ is the wavelength in unit of nm; d is the lattice spacing; θ is the diffraction degree.

In this study, Rigaku MiniFlex Benchtop X-ray Diffractometer was used to determine the crystallinity of films at diffraction angles, 2θ ranging from 3° to 90° . The X-ray source used was the Copper radiation (Cu $K\alpha$) with a wavelength, λ of 0.15406 nm.

3.4.2 Fourier transform infra-red (FTIR)

Fourier transform infrared spectroscopy is an analytical technique used to measure the absorption of infrared spectrum in a material. It provides quantitative and qualitative analysis to both organic and inorganic compounds. Normally, the FTIR spectrum can be interpreted based on two regions: fingerprint region (less than 1500cm^{-1}) and functional group region (equal to or more than 1500cm^{-1}).

In this study, Perkin Elmer Spectrum 400 Fourier transform infrared (FTIR) spectrometer was used to examine the chemical functional groups and molecular vibration modes that present in the films. The scanning range was examined from 4000 to 400cm^{-1} .

The results obtained from the XRD spectrum were further interpreted using Williamson-Hall (W-H) analysis to determine crystalline size, D and microstrains of the oxide/buffer layer obtained (Zak *et al.*, 2011). Besides, Debye-Scherrer equation was also used to estimate the crystalline size at one time 2θ position. Basically, the average crystalline size can be calculated using Debye-Scherrer equation as follow:

$$D = \frac{K \lambda}{\beta_D \cos \theta}$$

Where D is the crystalline size; K is the shape factor (usually constant of 0.9 is used); λ is the wavelength of X-ray source (Cu $K\alpha = 0.15406\text{ nm}$), β_D is the peak width with half

maximum intensity. Meanwhile, the strain of crystalline structure can be expressed as equation below:

$$\varepsilon = \frac{\beta_s}{4 \tan \theta}$$

Where β_s is the width at half max. intensity.

By combining both the equations, it will lead to :

$$\beta_{hkl} = \frac{K \lambda}{D \cos \theta} + 4 \varepsilon \tan \theta$$

Then rearrangement of the equation above into the linear form: $Y = mX + C$ to give rise to W-H equation:

$$\beta_{hkl} \cos \theta = 4 \varepsilon \sin \theta + \frac{K \lambda}{D}$$

Therefore, a graph of $(\beta_{hkl} \cos \theta)$ versus $4 \sin \theta$ were plotted for all the samples. From the W-H plots, the crystallite size, D can be estimated from y-intercept of the best fit line of the data, while microstrain, ε can be calculated from the slope of the best fit line.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Introduction

This chapter presents and discusses the experimental results based on the data obtained from the XRD analysis and FTIR analysis for the thermally oxynitrided surfaces of Ge substrates. Basically, this chapter consists of two major parts: XRD analysis and FTIR analysis.

4.2 XRD analysis

4.2.1 XRD patterns

Figure 4.1 shows XRD patterns of thermally oxynitrided Ge substrate at temperatures of 400°C, 500°C and 600°C. The peaks of germanium dioxide, GeO₂ were detected in XRD patterns for all the samples at 28.9°, 35.5°, 42.6° and 47.0° corresponding to (110), (111), (200) and (210). These peaks can be indexed to International Centre for Diffraction Data (ICDD) with reference code: 01-084-3971. The peaks of gamma-germanium nitride, γ -Ge₃N₄ were also found in the XRD patterns for all the samples at 38.83°, 47.97° corresponding to planes (110), (111). These peaks can be confirmed from ICDD with reference code: 01-075-8457. It is also important to note that there are multiple small peaks of γ -Ge₃N₄ were also detected vaguely at around $2\theta = 65^\circ$ for all the samples. The most distinguished features of XRD pattern for 600°C

sample would be the appearing of two new peaks at 31.58° (110) and 65.92° (220) which were not detected in XRD patterns for 400°C and 500°C samples. The peaks were identified as peaks for digermanium dinitrogen oxide, $\text{Ge}_2\text{N}_2\text{O}$ as indexing to ICDD reference code of 01-084-0069. These peaks confirmed the formation of $\text{Ge}_2\text{N}_2\text{O}$ on Ge substrate at temperature of 600°C .

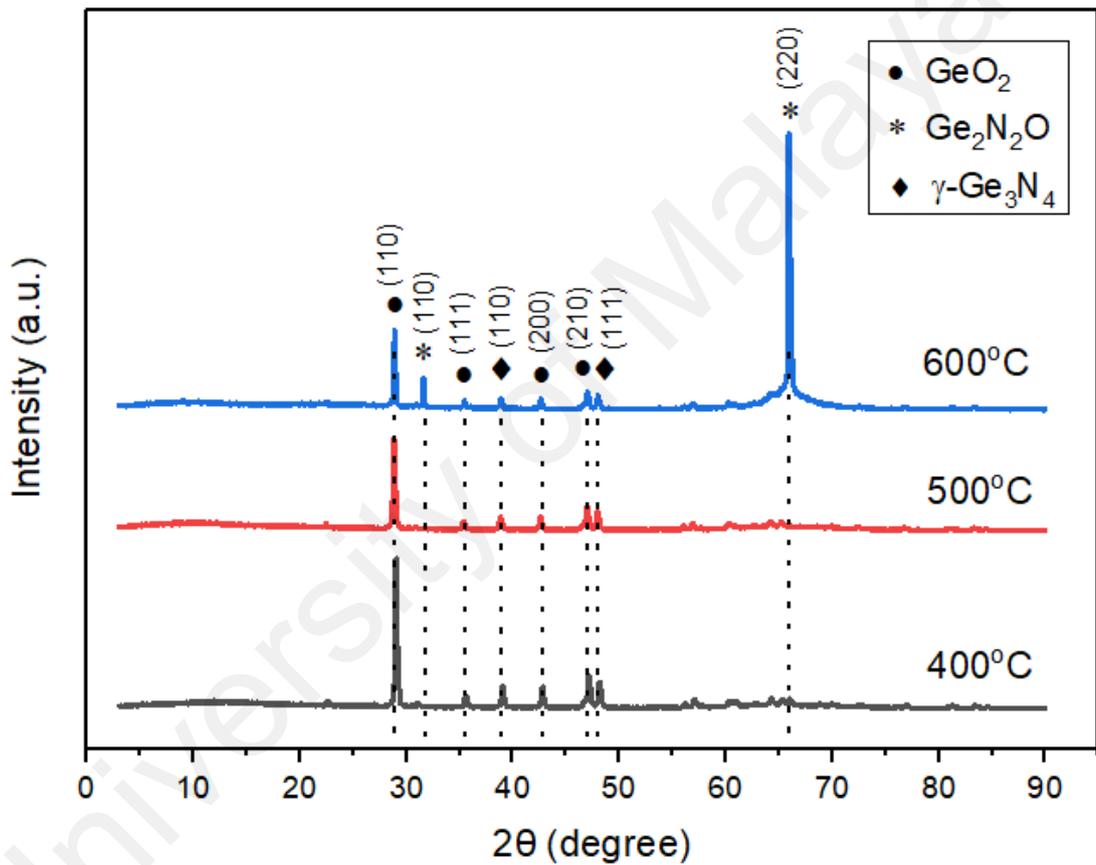


Figure 4.1: XRD patterns of thermally oxynitrided samples at temperatures of 400°C , 500°C and 600°C .

4.2.2 Analysis on Germanium Dioxide (GeO₂)

Figure 4.2 shows that the intensities of GeO₂ decrease as the temperature increases. This implied that the crystallinity of GeO₂ decreases with temperature higher than 400 °C, thus suggesting that GeO₂ is most likely to decompose into gaseous germanium oxide, GeO(g) as reported by Prabhakaran *et al.* (2000).

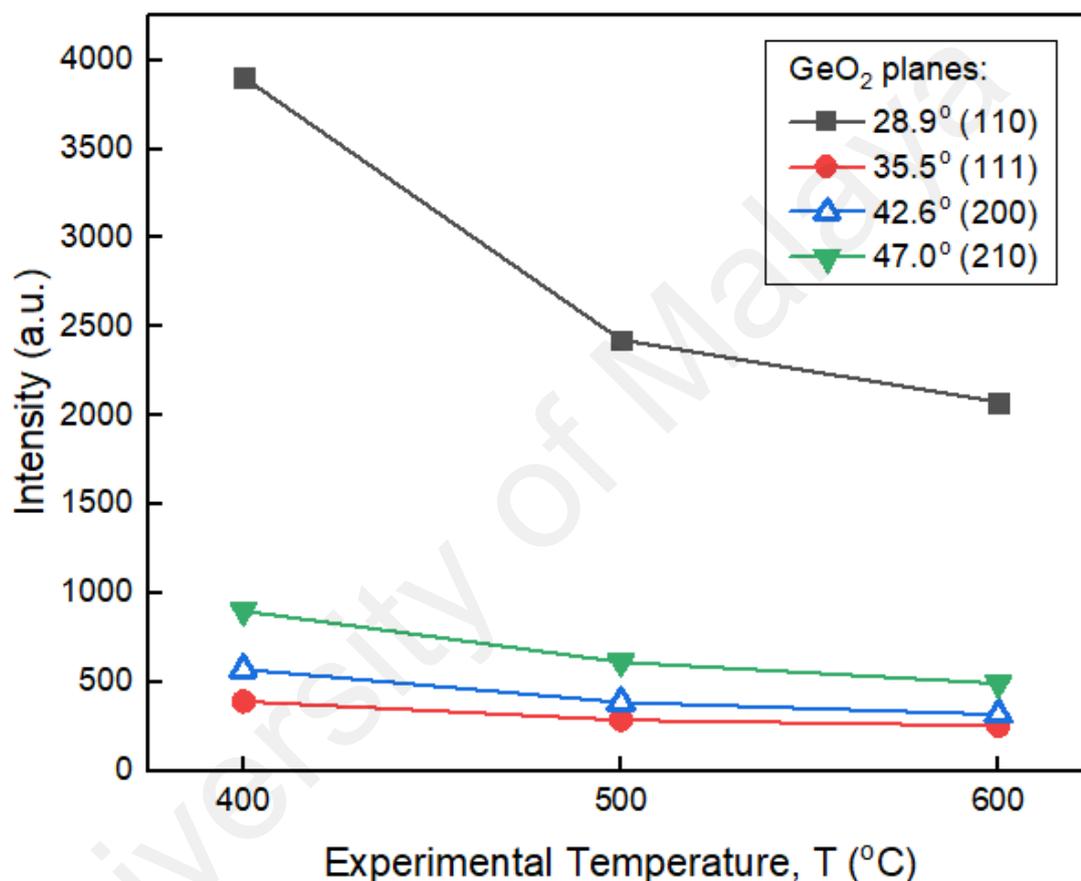


Figure 4.2: Intensities of GeO₂ planes: (110), (111), (200), (210) at 28.9°, 35.5°, 42.6°, 47.0° respectively in different experimental temperature (400, 500 and 600 °C).

By using Debye Scherrer equation, the average crystallite sizes of GeO₂ at 400 °C, 500 °C and 600 °C calculated were 37.13 nm, 33.62 nm and 42.11 nm respectively. Figure 4.3 shows the boxplot of the crystallite sizes of GeO₂ in different temperatures for each plane. It can be observed that crystallite sizes of GeO₂ at 500 °C shared the lowest distribution, indicating a more homogenous nanocrystallite sizes of GeO₂.

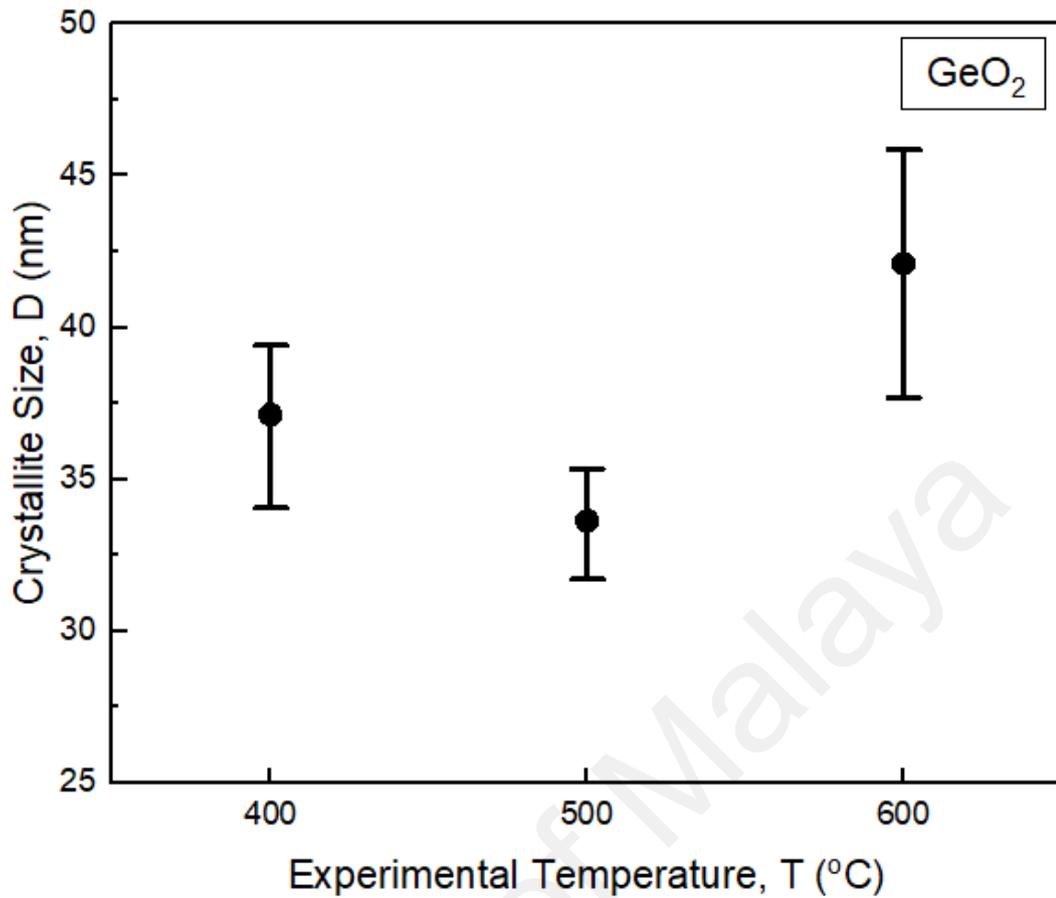


Figure 4.3: Calculated crystallite sizes of GeO₂ at different temperatures (400-600 °C) using Debye Scherrer equation.

Figure 4.4 illustrates the Williamson-Hall plot of GeO₂ where ($\beta_{hkl} \cos \theta$) is plotted against ($4 \sin \theta$) to determine the microstrain of the GeO₂. Figure 4.5 shows that the crystallite size of GeO₂ decreased from 37.12 nm to 33.63 nm, then climbed up to 42.11 nm, while microstrain of GeO₂ increased from -0.0009 to 0.0042 as the experimental temperature increases.

By comparing Figure 4.3 and Figure 4.5 (refer to **Black Line**), it is observed that the calculated crystallite sizes of GeO₂ obtained based on Debye Scherrer equation and Williamson-Hall analysis both shared the similar trend as the experimental temperature increased from 400 to 600 °C.

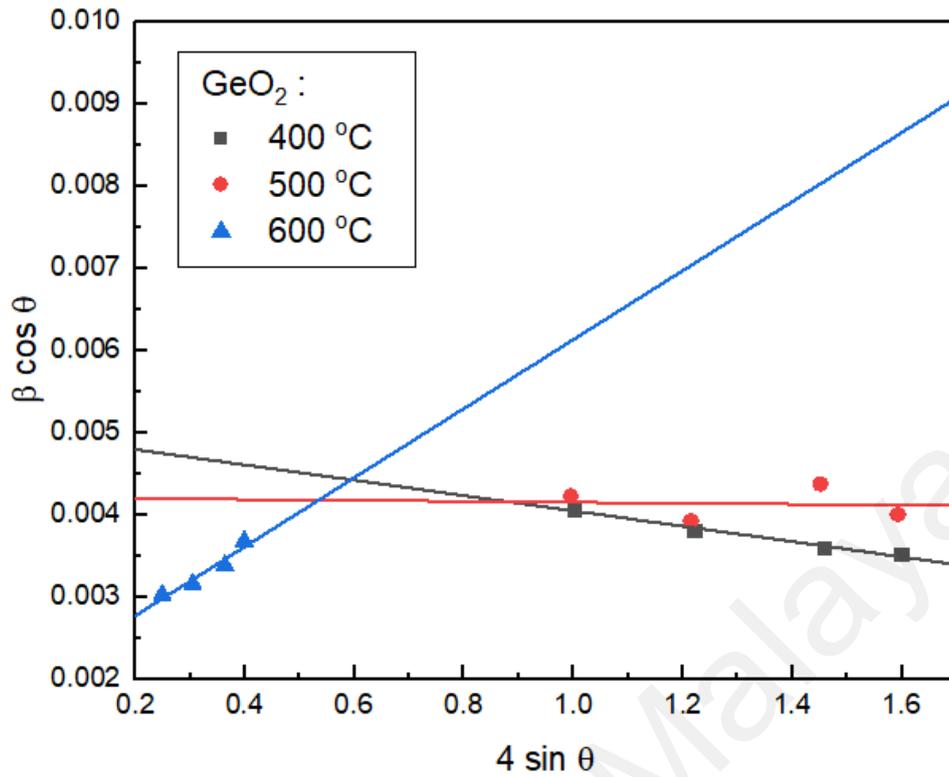


Figure 4.4: Williamson-Hall plot of GeO₂ for thermally oxynitrided samples at various temperatures (400-600 °C).

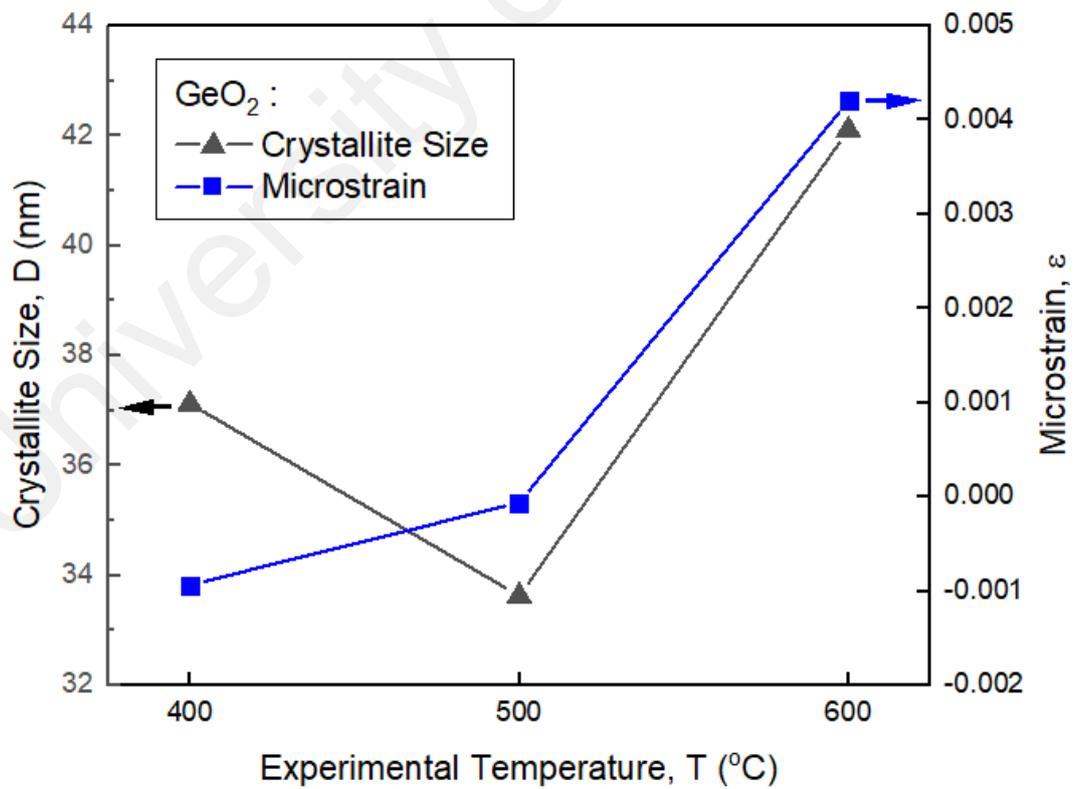


Figure 4.5: Relationship of calculated crystallite size and microstrain for GeO₂ from W-H plot as a function of experimental temperatures (400-600 °C).

4.2.3 Analysis on gamma-Germanium Nitride ($\gamma\text{-Ge}_3\text{N}_4$)

Figure 4.6 shows a decreasing trend in intensities of $\gamma\text{-Ge}_3\text{N}_4$ as the temperature increased. However, it seems that the decreasing trend is not drastic, thus suggesting $\gamma\text{-Ge}_3\text{N}_4$ able to maintain a good thermal stability at this temperature range (400 – 600 °C) and its crystallinity seems to be consistent at all the experimental experiments (Lieten, 2009).

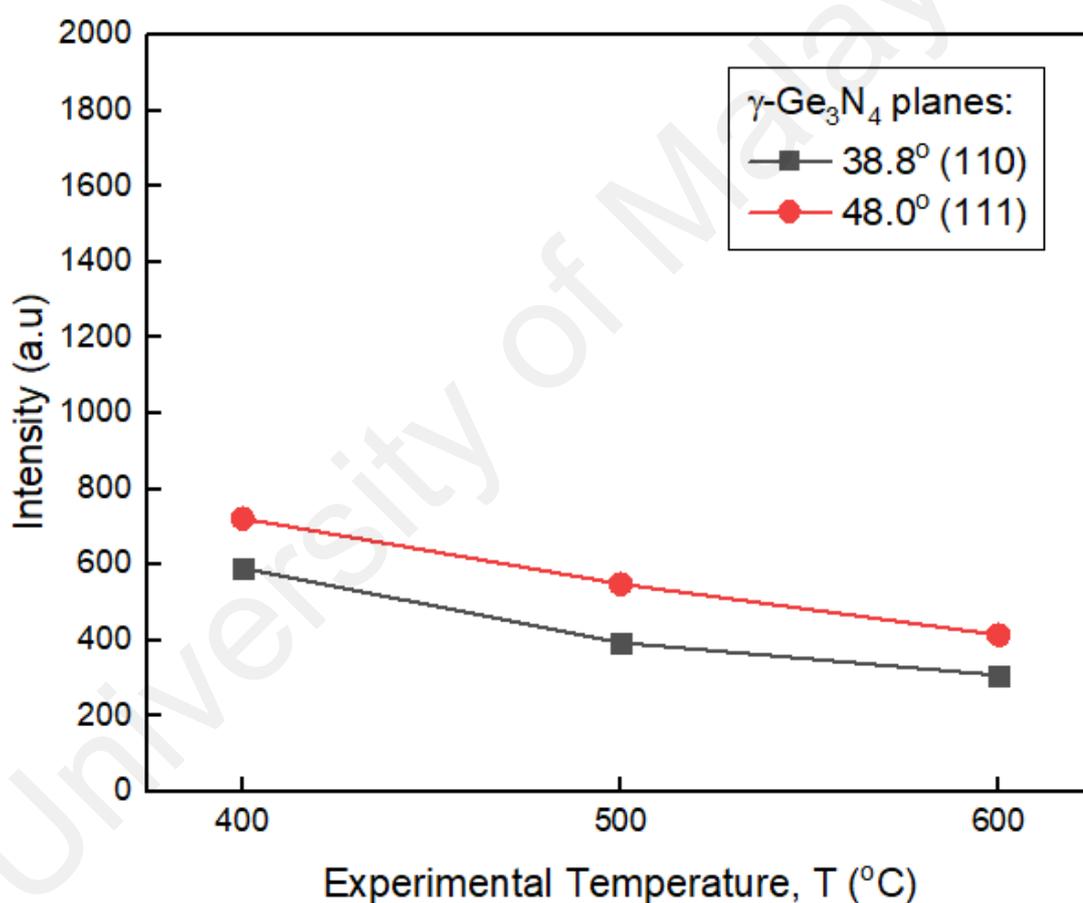


Figure 4.6: Intensities of $\gamma\text{-Ge}_3\text{N}_4$ planes: (110), (111) at 38.8° and 48.0° respectively in different experimental temperatures (400 °C, 500 °C and 600 °C).

The average crystallite sizes of γ -Ge₃N₄ at 400 °C, 500 °C and 600 °C calculated were 37.24 nm, 30.79 nm and 40.57 nm respectively based on the Debye Scherrer equation calculations. Figure 4.7 shows the average values and ranges of the crystallite sizes for γ -Ge₃N₄ at different temperatures. It can be observed that crystallite sizes of γ -Ge₃N₄ at 500 °C and 600 °C had the lower dispersions. Thus, this shows that the crystallite sizes of γ -Ge₃N₄ in the Ge substrates are more homogenous at 500 °C and 600 °C.

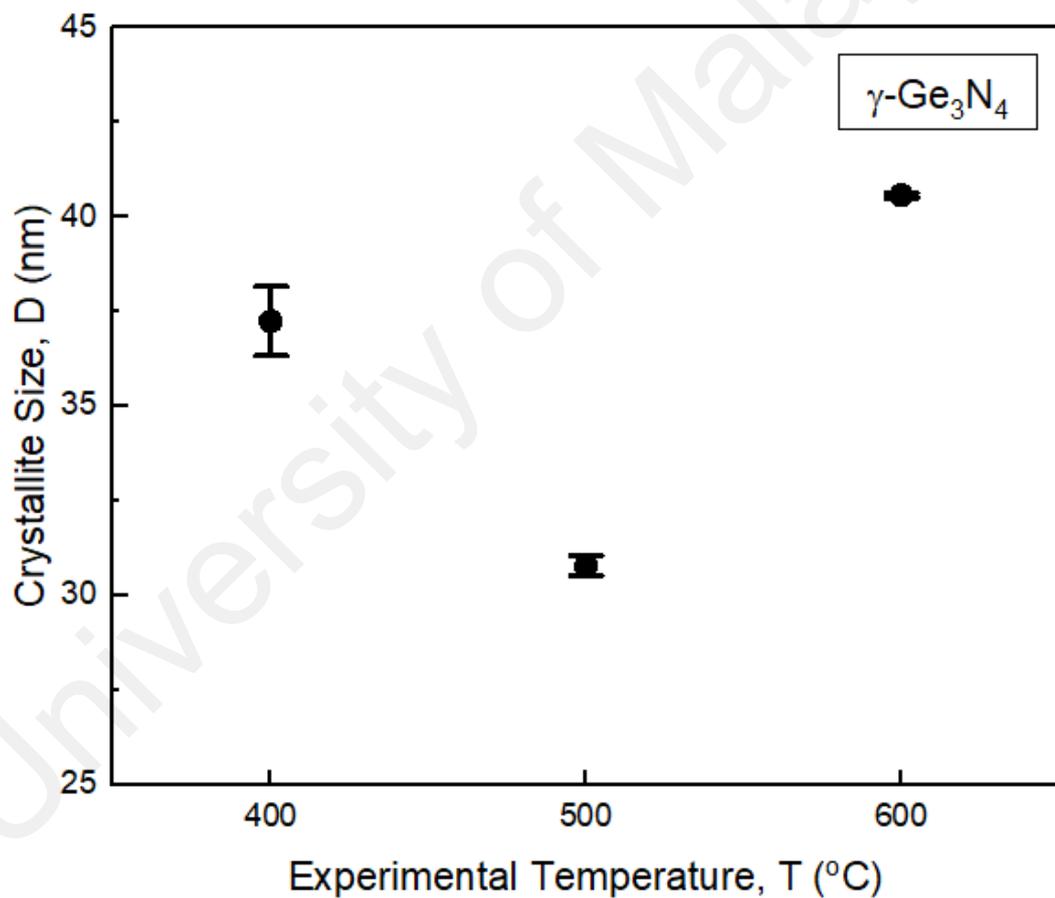


Figure 4.7: Calculated crystalline sizes of γ -Ge₃N₄ at different temperatures (400-600 °C) using Debye Scherrer equation.

The microstrains of $\gamma\text{-Ge}_3\text{N}_4$ were determined based on the Williamson-Hall plot where $(\beta_{hkl} \cos \theta)$ is plotted against $(4 \sin \theta)$ as shown in Figure 4.8. Based on Figure 4.9, we can know that the crystallite size of $\gamma\text{-Ge}_3\text{N}_4$ first was reduced from 37.25 nm to 30.79 nm, then rose up to 40.57 nm, while microstrain of $\gamma\text{-Ge}_3\text{N}_4$ increased from -0.006 to 0.00003 when the experimental temperature increased from 400 to 600 °C.

By comparing Figure 4.7 and Figure 4.9 (refer to **Black Line**), it is observed that the calculated crystallite sizes of GeO_2 obtained based on Debye Scherrer equation and Williamson-Hall analysis also showed almost exact the same trend starting from 400 °C up to 600 °C.

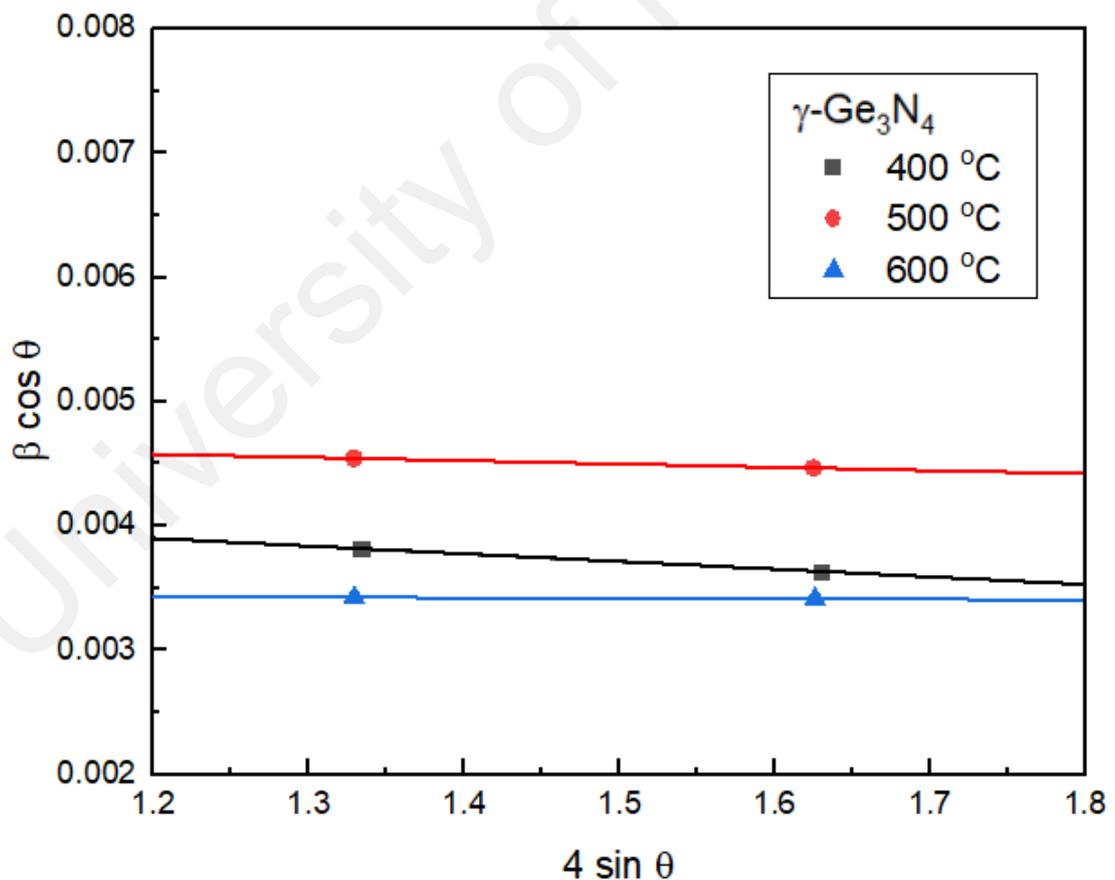


Figure 4.8: Williamson-Hall plot of $\gamma\text{-Ge}_3\text{N}_4$ for thermally oxynitrided samples at various temperatures (400-600 °C).

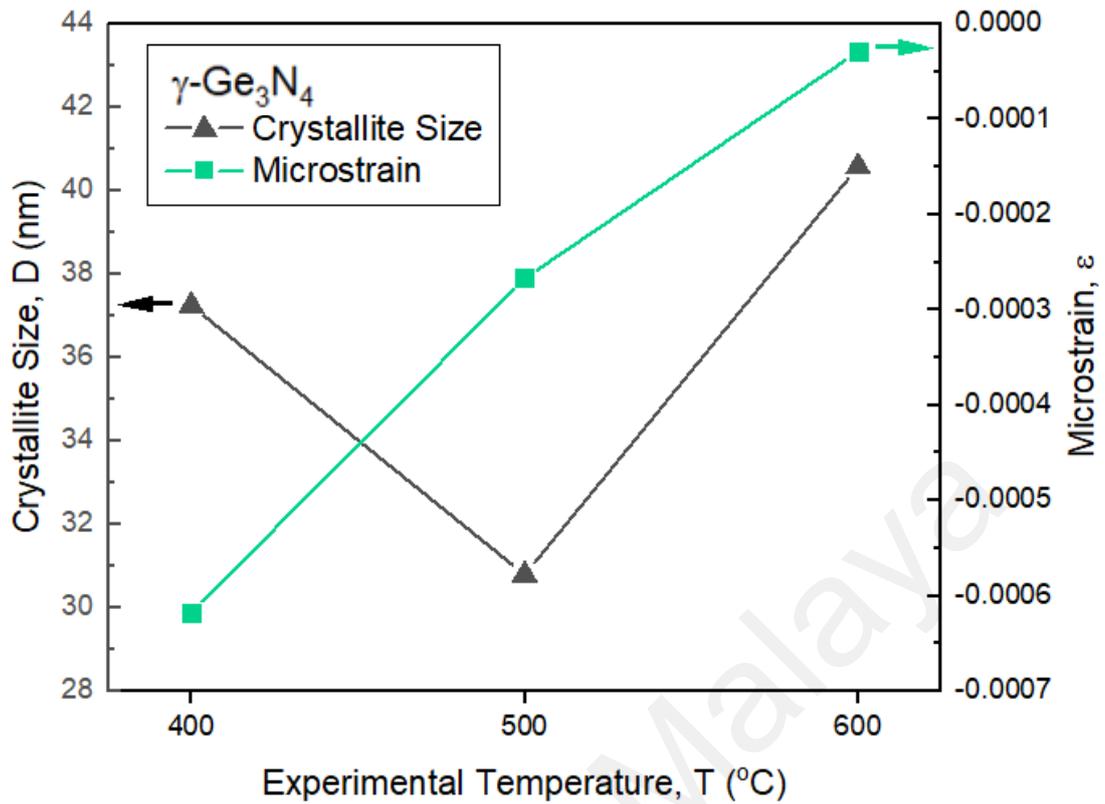


Figure 4.9: Relationship of calculated crystallite size and microstrain for $\gamma\text{-Ge}_3\text{N}_4$ from Williamson-Hall plot as a function of experimental temperatures (400-600 °C).

4.2.4 Analysis on Digermanium Dinitrogen Oxide ($\text{Ge}_2\text{N}_2\text{O}$)

Figure 4.10 shows that the formation of $\text{Ge}_2\text{N}_2\text{O}$ only start at temperature of 600 °C. It is observed that the intensities of planes (110) and (220) of $\text{Ge}_2\text{N}_2\text{O}$ at 400 °C and 500 °C were very vaguely detected (intensity ≤ 207). The average crystallite size calculated based on Debye Scherrer equation was 62.50 nm (as shown in the inserted plot in Figure 4.10). Meanwhile, the microstrain and crystallite size of $\text{Ge}_2\text{N}_2\text{O}$ obtained based Williamson-Hall analysis were 0.0002023 and 62.50 nm (Figure 4.11). The average crystallite size calculated based on Debye Scherrer equation and Williamson-Hall analysis were the same.

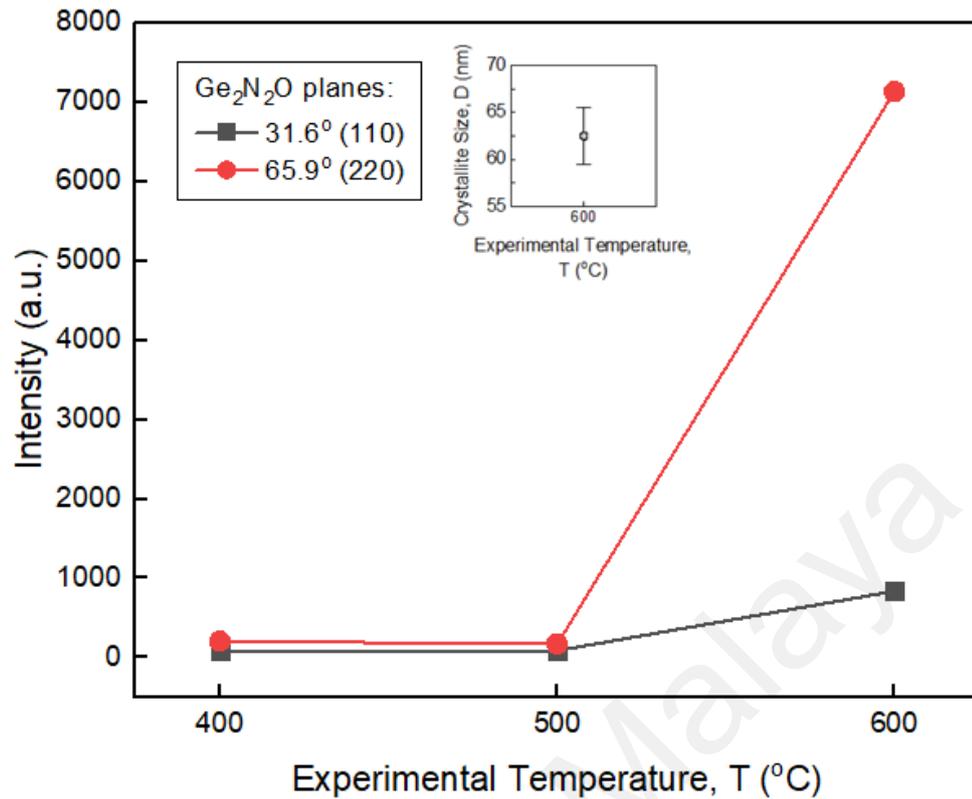


Figure 4.10: Intensities of Ge₂N₂O planes: (110), (220) at 31.6° and 65.9° respectively in different experimental temperatures (400, 500, 600 °C). The intensities of both the planes (110) and (220) at 400 °C and 500 °C are included in graph to prove that Ge₂N₂O only start to form at 600 °C. [Inserted plot at the top middle of the graph: it shows the average crystallite size calculated at 600 °C]

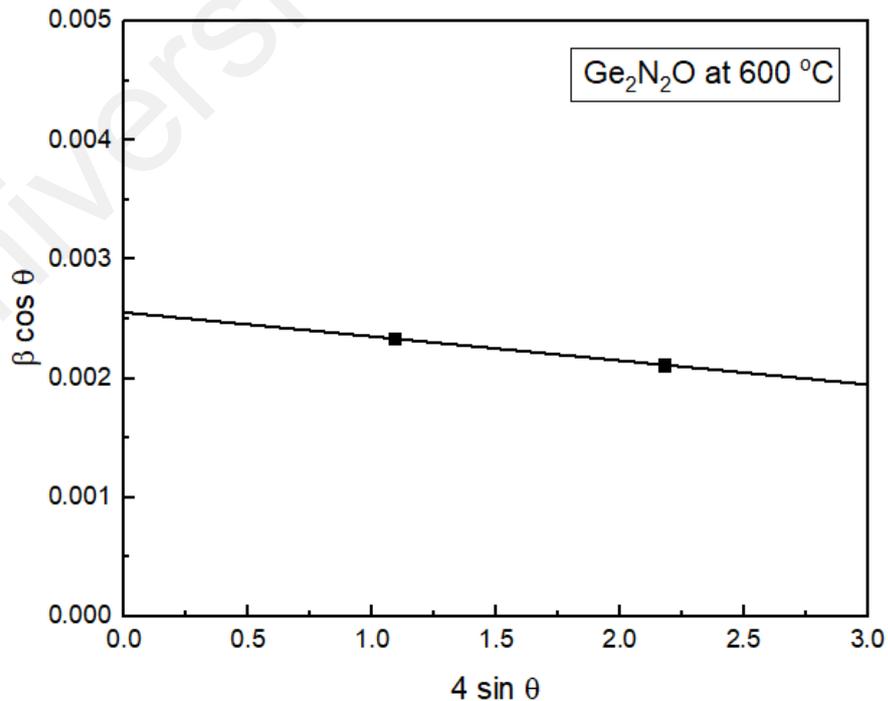


Figure 4.11: Williamson-Hall plot of Ge₂N₂O for thermally oxynitrided sample at 600°C.

4.3 FTIR Analysis

Figure 4.12 shows the FTIR spectra of Ge substrates thermally oxynitrided at temperatures of 400°C, 500°C and 600°C. FTIR analysis points out the significant differences in the spectra of oxynitridation of germanium substrates at temperature between 600°C with 400°C and 500°C. FTIR spectrum of 600°C sample detected a weakened $\text{Ge}_2\text{N}_2\text{O}$ band at around 800cm^{-1} which is closed to the value reported in studies of (Murad *et al.*, 2012; Maggioni *et al.*, 2017). Ge_3N_4 absorption peak was also detected in 600°C sample at 920cm^{-1} (Maggioni *et al.*, 2017). Mild N-O stretching mode was also detected at 1580cm^{-1} in the FTIR spectrum of 600 °C sample. Besides, the bands that might be responsible for the adsorption of N_2O to germanium surface were detected at 1725cm^{-1} and 1160cm^{-1} , as pointed out in reports of Diamantis, & Sparrow (1974). Comparing all these three FTIR spectra, it can be deduced that $\text{Ge}_2\text{N}_2\text{O}$ was formed at 600 °C which was confirmed by the absorption at 800cm^{-1} ; And also, the disappearing of the bands (adsorption of N_2O bonding) at 1725cm^{-1} and 1160cm^{-1} , suggesting that N_2O adsorbed might be turned into $\text{Ge}_2\text{N}_2\text{O}$ at 600 °C.

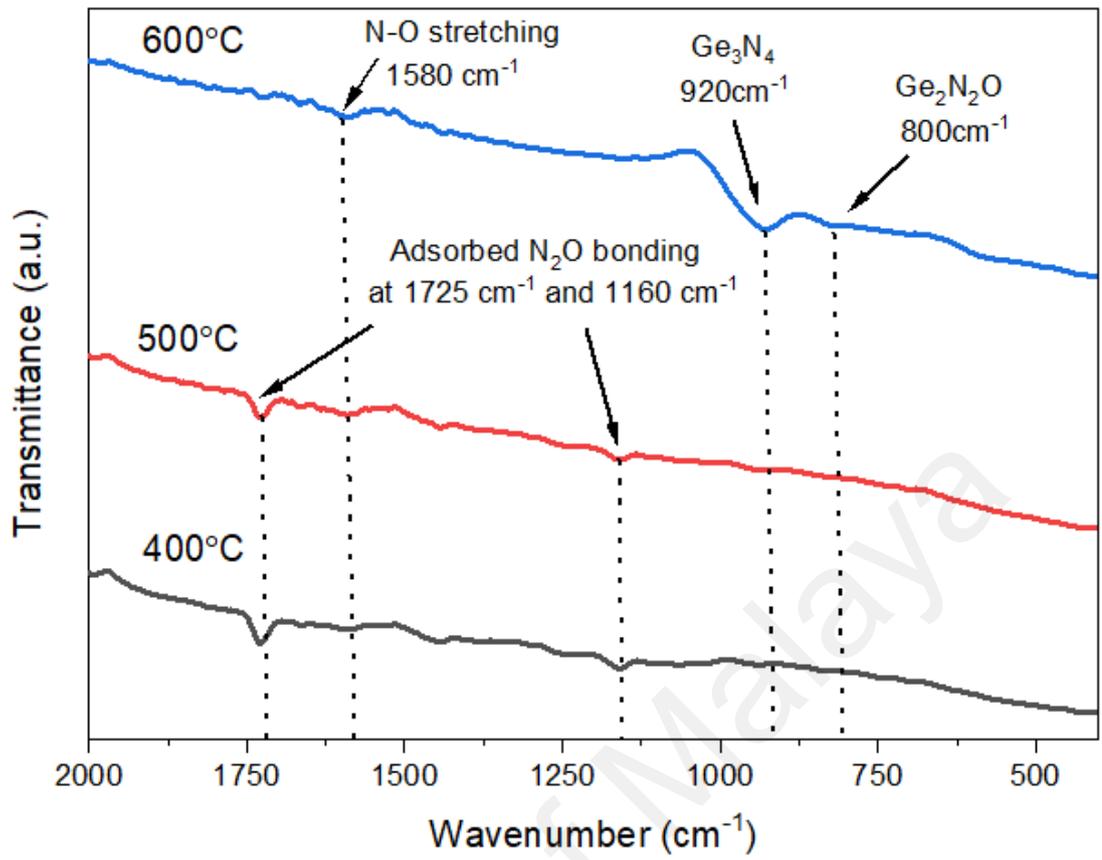


Figure 4.12: FTIR spectra of thermally oxynitrided samples at various temperatures (400-600 °C)

CHAPTER 5

CONCLUSION

5.1 Conclusion

The germanium oxynitride, GeON was not obtained in the thermal oxynitridation in nitrous oxide (N₂O) gas ambient. However, in this study, digermanium dinitrogen Ge₂N₂O was formed in the thermal oxynitridation at temperature of 600 °C. The formation of Ge₂N₂O at 600 °C was confirmed by XRD analysis where the peaks represent Ge₂N₂O were only detected in the XRD pattern for 600 °C sample at 31.6° (110) and 65.9° (220). Besides, the FTIR spectrum for sample at 600 °C also detect the Ge₂N₂O band at around 800cm⁻¹. Apart from that, the XRD analysis and FTIR analysis also show the formation of germanium dioxide, GeO₂ and gamma-germanium nitride, γ-Ge₃N₄ at 400 °C, 500 °C and 600 C.

5.2 Recommendations for future research

The investigation in searching the best high-*k* materials/Ge gate stack for high speed MOSFET requires a lot of efforts and innovations. There are a few suggestions proposed for the future research based on the finding in this research study are shown as below:

- (i) The physical and electrical properties digermanium dinitrogen oxide should be investigated to determine its capabilities as buffer layer on germanium substrate.

- (ii) Formation of germanium oxynitride as buffer layer on the germanium dioxide surface using the similar thermal oxynitridation process deployed in this research study is worth to be investigated.
- (iii) The thermal stability of digermanium dinitrogen oxide at temperatures higher than 600 °C can be investigated as well.
- (iv) It is also suggested to further investigate the effects of using higher concentration of N₂O gas in the formation of buffer layer on germanium substrate.

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