DEVICE CHARACTERIZATION BASED ON STRESSOR, GEOMETRIC AND PROCESS DESIGN CONSIDERATIONS OF FET TECHNOLOGY

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FACULTY OF ENGINEERING
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DISSERTATION SUBMITTED IN FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE OF MASTER OF ENGINEERING SCIENCE

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DEVICE CHARACTERIZATION BASED ON STRESSOR, GEOMETRIC AND PROCESS DESIGN CONSIDERATIONS OF FET TECHNOLOGY

ABSTRACT

The downscaling of complementary metal-oxide-semiconductor (CMOS) device has been tremendously feasible in the past couple of decades. This action has led to a constant escalation of devices count in a dense integrated circuit, hence an outstanding application of Moore's law to the industry especially in semiconductor sector. Nevertheless, the reduction in the sizing of features has bound to become an issue in providing excellent performance in CMOS circuits particularly in drive current maintenance and operating speed efficiency. Therefore, designers have proposed several solutions to replace the conventional metal-oxide-semiconductor field effect transistor (MOSFET) designs such as the implementation of strain/stress engineering technology, introduction of multi-gated MOSFET, adoption of group IV and III-V semiconductors into the device structure, and scaling specification validated with statistical techniques and numerical methods. This work presents a comprehensive simulation study and optimization analysis to study the impacts of stressor, geometric and process design considerations on novel FET devices, i.e. fin shaped FET (FinFET) and heterostructure FET (HFET), for low and high power applications, respectively. A technology computer-aided design (TCAD) based tools, i.e. Synopsys Sentaurus TCAD is used to demonstrate the design structures and analysis on the investigated FET devices. The impact of specific parameters selection on the device performance are considered based on standard CMOS manufacturing trends in recent years.

The implementation of germanium (Ge) and aluminium nitride (AlN) in 7 nm FinFET and gallium nitride (GaN) based HFET, respectively, as the stressor effects has allowed the adjustment of threshold voltage roll-off behaviour without dramatically degrading the device drive current. The incorporation of stress inside the channel layer can increase the

drain current by ~110% and ~57% for p- and n-FinFET, respectively. For GaN based HFET, insertion of AlN as the interfacial layer with high Al mole fraction in the barrier can increase the current up to 48% and improve the mobility as well as carrier confinement. Besides that, device performances were explored through varied geometric and process design parameters of a certain range of values. The devices were electrically characterized by studying the current-voltage relation and several figure-of-merits were extracted to study the impacts of these design consideration. This work shows that both geometric and process considerations are affecting the FET performances with similar importance. An optimization process is also conducted onto the 7 nm Ge based FinFET by optimizing the fin geometry. Taguchi method and Pareto analysis of variance were implemented in order to achieve the best possible design for each specification and response with respect to threshold voltages, drive currents, and subthreshold leakages. The analysis shows that the device geometry designs are highly affecting device performances especially the gate length, top fin width, and the interaction of both for n- and p-FinFET by more than 50%. Since the geometries are related to each other in performance improvements, it is important to choose the most nominal design for threshold and current trade-offs achievements.

In conclusion, this work has characterized the impact of group IV and III-V stressor on the FET devices and considering the geometrical and process design, producing simulation results which were in qualitative agreement with published results by other researchers. It is important to understand and simulate accurately the effects of specific parameter selections in the initial design phase to guarantee the optimal operation and limitation of devices in order to realize acceptable CMOS performance for particular chip specifications.

Keywords: FET devices, group IV, group III-V semiconductor, Taguchi method, device design.

PENCIRIAN PERANTI BERDASARKAN PERTIMBANGAN TEKANAN, GEOMETRI DAN PROSES BAGI TEKNOLOGI FET

ABSTRAK

Pengecilan skala bagi peranti logam-oksida-semikonduktor pelengkap (CMOS) telah dipraktikkan sejak beberapa dekad yang lalu. Hal ini meningkatkan bilangan peranti secara berterusan dalam litar bersepadu padat, seterusnya dapat mengaplikasikan undang-undang Moore dalam industri semikonduktor. Walaubagaimanapun, pengurangan saiz ciri telah menjadi satu isu yang serius dalam menyediakan prestasi yang boleh dipercayai dalam litar CMOS terutama dalam mengekalkan arus operasi dan kelajuan yang cekap. Oleh itu, beberapa penyelesaian baru telah dicadangkan oleh pereka cip untuk menggantikan rekabentuk transistor kesan medan logam-oksida-semikonduktor (MOSFET) konvensional seperti pelaksanaan teknologi kejuruteraan ketegangan/tekanan, memperkenalkan MOSFET berbilang gerbang, penerapan semikonduktor kumpulan IV dan III-V ke dalam struktur peranti, dan penskalaan spesifikasi yang disahkan dengan teknik statistik dan kaedah berangka. Kajian ini membentangkan analisis simulasi dan pengoptimuman secara komprehensif untuk mengkaji kesan rekabentuk bertimbangkan tekanan, geometri dan proses ke atas peranti FET, seperti FET bersirip (FinFET) untuk kegunaan kuasa rendah dan FET struktur hetero (HFET) untuk kuasa tinggi. Simulasi rekabentuk teknologi berbantukan komputer (TCAD) Synopsys Sentaurus digunakan untuk menunjukkan struktur rekabentuk dan analisis ke atas peranti FET yang dikaji. Kesan pemilihan parameter khusus ke atas prestasi peranti telah dipertimbangkan berdasarkan trend piawaian pembuatan CMOS yang terbaru.

Penerapan germanium (Ge) ke dalam FinFET 7 nm dan aluminium nitrida (AlN) bagi HFET berasaskan galium nitrida (GaN) sebagai tekanan dapat melaraskan voltan ambang tanpa merendahkan arus peranti secara mendadak. Penerapan tekanan ke dalam lapisan

saluran dapat meningkatkan arus sebanyak ~110% dan ~57% untuk n- dan p-FinFET. Bagi HFET, penambahan AlN sebagai lapisan pengantara dapat meningkatkan arus sehingga 48% dan dapat memudahkan pergerakan dan kepantangan pembawa. Selain itu, prestasi peranti diteroka melalui pelbagai rekabentuk parameter geometri dan proses dalam nilai julat yang tertentu. Peranti tersebut dicirikan secara elektrik dengan mengkaji hubungan arus voltan dan angka merit diekstrak untuk mengkaji kesan pertimbangan rekabentuk ini. Hasil kajian menunjukkan kedua-dua pertimbangan geometri dan proses memberikan impak yang sangat penting ke atas prestasi peranti FET. Selepas itu, proses pengoptimuman dilakukan ke atas FinFET 7 nm berasaskan Ge dengan mengoptimalkan geometri sirip. Kaedah Taguchi dan analisis variasi Pareto telah dilaksanakan untuk mencapai rekabentuk terbaik untuk setiap spesifikasi dan respon berdasarkan voltan ambang, arus operasi, dan kebocoran arus. Analisis menunjukkan bahawa prestasi ini sangat bergantung kepada rekabentuk geometri peranti, terutamanya panjang sirip, lebar sirip atas, dan interaksi keduanya untuk n- dan p-FinFET sehingga lebih 50%. Disebabkan setiap prestasi adalah saling berkaitan, adalah penting untuk memilih reka bentuk yang paling sesuai untuk pencapaian voltan ambang dan penyelesaian arus.

Kesimpulannya, kerja ini telah mencirikan kesan tekanan kumpulan IV dan III-V ke atas peranti FET dan mempertimbangkan reka bentuk geometri dan proses, bagi menghasilkan keputusan simulasi yang setara dengan hasil yang diterbitkan oleh penyelidik lain. Pemahaman dan simulasi yang tepat menggunakan parameter yang khusus sangat penting dalam fasa rekabentuk awal untuk menjamin operasi optimum dan had peranti untuk mencapai prestasi CMOS yang boleh diterima untuk spesifikasi cip tertentu.

Katakunci: peranti FET, semikonduktor kumpulan IV, kumpulan III-V, kaedah Taguchi, reka bentuk peranti.

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2DEG	:	Two dimensional electron gas
AlN	:	Aluminium nitride
BTBT	:	Band-to-band tunnelling
CESL	:	Contact etch stop layer
DIBL	:	Drain induced barrier lowering
D_{it}	:	Interface trap density
DOE	:	Design of experiment
FinFET	:	Fin shaped field effect transistor
GaAs	:	Gallium arsenide
GaN	:	Gallium nitride
Ge	:	Germanium
g_m	:	Transconductance
HEMT	:	High electron mobility transistor
HFET	:	Heterostructure field effect transistor
H_{fin}	:	Fin height
HfO_2	:	Hafnium oxide
HP	:	High performance
HS	:	Heterostructure
IC	:	Integrated circuit
I_d	:	Drain current
I_{off}	:	Off-state current
I_{on}	:	On-state current
IRDS	:	International Roadmap for Devices and Systems
ITRCS	:	International Technology Roadmap for Compound Semiconductors

ITRS	:	International Technology Roadmap for Semiconductors
I-V	:	Current-voltage
L_g	:	Gate length
LP	:	Low performance
LTB	:	Larger the better
MOSFET	:	Metal-oxide-semiconductor field effect transistor
N_{ch}	:	Channel doping concentration
N_{inv}	:	Inversion charge density
N_{sd}	:	Source/drain doping concentration
NTB	:	Nominal the better
PE	:	Piezoelectric
R_{on}	:	On-resistance
R_{out}	:	Output resistance
R_{sd}	:	Source/drain resistance
S/D	:	Source/drain
SCE	:	Short channel effect
SE	:	Stress engineered
Si	:	Silicon
Si:C	:	Silicon carbide
SiGe	:	Silicon germanium
SiN	:	Silicon nitride
Sn	:	Tin
SNR	:	Signal-to-noise ratio
SRB	:	Stress relaxed buffer
SS	:	Subthreshold swing
STB	:	Smaller the better

t_{bf}	:	Buffer thickness
t_{br}	:	Barrier thickness
TCAD	:	Technology computer-aided design
TiN	:	Titanium nitride
t_{sp}	:	Spacer thickness
V_d	:	Drain voltage
V_g	:	Gate voltage
V_t	:	Threshold voltage
W_{bottom}	:	Bottom fin width
WF	:	Work function
W_{top}	:	Top fin width
xmole	:	Mole fraction

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CHAPTER 1: INTRODUCTION

1.1 Background of the study

The scaling of geometric parameters for silicon (Si) complementary metal-oxide-semiconductor (CMOS) transistors has allowed an exponential increase of density in the integrated circuit (IC) for the past five decades, as predicted by Gordon E. Moore in 1965. He presumed that in a dense IC, the number of transistors would double approximately every 18 months (Moore, 1998), which is then defined as the Moore's law. Since then, this law has become the guidance for the CMOS scaling to obtain the transistor performance enhancement. Nevertheless, as the transistor gate length shrunk below 35 nm and the gate oxide thickness is reduced to 1 nm, the problems with conventional metal-oxide-semiconductor field effect transistor (MOSFET) are increasing. Several limitations such as drain induced barrier lowering (DIBL), threshold voltage roll-off, mobility degradation (Takagi et al., 2008), and increasing subthreshold current as well as power density make geometric scaling a continuously challenging task. Therefore, the device structures and materials are required for innovations (Haensch et al., 2006) and a new scaling vector in the industry is a major key in order to stay on track for CMOS device scaling.

At 90 nm and beyond, strained Si has become one of the innovation to overcome the challenges (M. Kumar, Dubey, Tiwari, & Jit, 2013). The used of strained Si MOSFET give favourable impacts on the drain current (I_d) with the improvement of the carrier mobility and transport. Besides that, the use of other device such as the multi gated FETs can be one of the innovations to meet the challenge in device scaling. Several multigate transistor has been introduced since then, such as planar double gate transistor (Boucart & Ionescu, 2007), fin shaped FET (FinFET) (Lakshmi & Srinivasan, 2012), trigate transistor (Yan et al., 2007), gate all around FET (GAAFET) (Hsu et al., 2011) and many more. Recently, FinFET technology has been majorly adopted for use within IC industries

(Nowak et al., 2004). This technology promises to deliver superior levels of scaling ability needed to make sure the progression of current with increased levels of integration within IC can be maintained.

Furthermore, use of other semiconductor other than Si can be considered as alternative to overcome the scaling challenge (R. Zhang, Iwasaki, Taoka, Takenaka, & Takagi, 2012). Germanium (Ge) is one of the group IV semiconductor which can be considered as the most promising material as the replacement of Si for its higher mobility and compatibility with Si technologies (Shang et al., 2006). Earlier research has demonstrated the fabrication of Ge channel p-MOSFET with enhanced hole mobility and carrier transport characteristics by 8 times to that of Si channel (M. L. Lee et al., 2001). Apart from group IV semiconductor, combination of group III material with group V material can create III-V alloys, which also can be considered as a new prospect for channel material other than Si (Chau, Datta, & Majumdar, 2005). In photonics and optoelectronics perspectives, the use of III-V materials are widely used to make lasers (Kyono, Akita, & Yoshizumi, 2011), light emitting devices (Orton & Foxon, 1998), as well as photodetectors (Capasso & Williams, 1982). Meanwhile in microelectronics and IC industry, the III-V alloys are employed to increase the electron speed, hence produce faster transistors (Chavarkar et al., 2005), especially in high power and high frequency application (Palacios et al., 2005).

Despite having aggressive device scaling improving the device performance, the scaling challenges are also accelerating linearly where the device sizing can no longer be reduced beyond a certain extent due to severe short channel effect (SCE) (Kim, 2010). For that reason, this study is carried out to find the best alternatives and potential solutions to overcome the challenges of scaling limitation while enhancing the device performance at the same time. This dissertation highlights the device design issues of recent FET

technology by addressing the impact of design parameter selection on critical electrical characterization using a numerical simulation approach based on the standard manufacturing trends ("International Technology Roadmap for Semiconductors," 2014). It is necessary to have a solid understanding of the phenomena that occurs in nanoscale transistors since it not only provides useful interpretation of the previous results but also the future possibilities and limitations of the device scaling.

1.2 Problem statement

FinFET technology was introduced due to the fierce increase in the levels of integration. The basic principle of Moore's law has been practiced for many years from the earliest years of IC technology (Schaller, 1997). Moreover, some of the landmark chips of the relatively early IC era had a low transistor count even though they were advanced for the time. To achieve the large increases in levels of integration, many parameters have changed especially the geometric and process parameters. Fundamentally the feature sizes have reduced to enable more devices to be fabricated within a given area. FinFET technology has been scaled following the International Technology Roadmap for Semiconductors (ITRS), in which the channel length is minimize with careful design consideration due to the trade-offs between device drive current, SCEs and power consumption. Recent reports show that a 10 nm FinFET CMOS technology have been successfully demonstrated for mass production (Samsung, 2016) which provide higher efficiency and performance with low power consumption compared to 14 nm technology. This current technology allows cutting-edge techniques in order to overcome the limitations in device scaling.

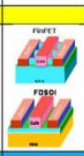
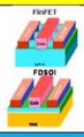
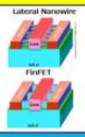
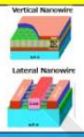
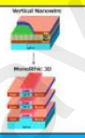
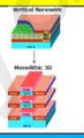
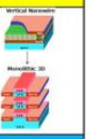
However, beyond 10 nm technology, aggressive downsizing of device structure can severely affect the device performance, especially in SCE restraints. This has led to the end of the Moore’s law, where any reduction of the geometry can suppress the IC chip

enhancement (Simonite, 2016). This incident has caused ITRS to issue their final roadmap. Since then, a new initiative was started to develop a thorough and more generalized roadmapping ("International Roadmap for Devices and Systems," 2016), named as International Roadmap for Devices and System (IRDS) which is founded in 2016. Specific device architecture and ground rules roadmap are set by IRDS for logic device technologies such as poly pitch, cell height, target area scaling, etc. (IRDS, 2016). Table 1.1 presents the summary for the roadmap ground rules according to IRDS. Prior to the foundation of IRDS, an idea is proposed by Bennet (2000) on the embodiment of a new roadmap for compound semiconductor, which is called International Technology Roadmaps for Compound Semiconductors (ITRCS) to continue the research and development in III-V semiconductor as well as elemental Si compound that is compatible with Si CMOS technology. This proposition is considered as a trigger for IC designers to keep digging the significance of compound materials in overcoming the challenges for device scaling.

Many published works are related to the significant performance improvements using compound materials to replace Si channel (Bae et al., 2016; J. Cho et al., 2017), especially in advanced FET devices (Rahman, Othman, Hatta, & Soin, 2017; Swain, Adak, Pati, & Sarkar, 2016). The growing number of publications addressing the scaling challenges of CMOS FET devices indicates increased interest to this area. However, the impact of specific design consideration on device performance need to be paid most attention, by investigating how the compound semiconductor adoption, geometric and process design consideration can influence the device performance. Device optimization for robust design considerations is also important to select the most optimal combination for specific design using statistical analysis (Taguchi, 2001), and which parameter is the most affecting the device performance by using device characterization of advanced three dimensional (3D) simulation tools. Understanding the exact characteristics of the

electrical as well as current-voltage (I-V) relation due to the variation of stress effect, geometric and process design considerations in the advanced FET devices is another aspect that need to be explored.

Table 1.1: Device architecture and ground rules roadmap for logic device technologies (IRDS, 2016).

YEAR OF PRODUCTION	2015	2017	2019	2021	2024	2027	2030
Logic device technology naming	P70M56	P54M36	P42M24	P32M20	P24M12G1	P24M12G2	P24M12G3
Logic industry "Node Range" Labeling (nm)	"16/14"	"11/10"	"8/7"	"6/5"	"4/3"	"3/2.5"	"2/1.5"
Logic device structure options	finFET FDSOI	finFET FDSOI	finFET LGAA	finFET LGAA VGAA	VGAA, M3D	VGAA, M3D	VGAA, M3D
							
LOGIC DEVICE GROUND RULES							
MPU/SoC Metalx ½ Pitch (nm)[1,2]	28.0	18.0	12.0	10.0	6.0	6.0	6.0
MPU/SoC Metal0/1 ½ Pitch (nm)	28.0	18.0	12.0	10.0	6.0	6.0	6.0
Contacted poly half pitch (nm)	35.0	24.0	21.0	16.0	12.0	12.0	12.0
L_g: Physical Gate Length for HP Logic (nm) [3]	24	18	14	10	10	10	10
L_g: Physical Gate Length for LP Logic (nm)	26	20	16	12	12	12	12
Channel overlap ratio - two-sided	0.80	0.80	0.80	0.80	0.80	0.80	0.80
Spacer width (nm)	12	8	6	5	4	4	4
Contact CD (nm) - finFET, LGAA	22	14	16	12	11	11	11
Device architecture key ground rules							
FinFET Fin Half-pitch (new) =0.75 or 1.0 M0/M1 (nm)	21.0	18.0	12.0				
FinFET Fin Width (nm)	8.0	6.0	6.0				
FinFET Fin Height (nm)	42.0	42.0	42.0				
Footprint drive efficiency - finFET	2.19	2.50	3.75				
Lateral GAA Lateral Half-pitch (nm)			12.0	10.0			
Lateral GAA Vertical Half-pitch (nm)			12.0	9.0			
Lateral GAA Diameter (nm)			6.0	6.0			
Footprint drive efficiency - lateral GAA, 3x NWs stacked			2.4	2.8			
Vertical GAA Lateral Half-pitch (nm)				10.0	6.0	6.0	6.0
Vertical GAA Diameter (nm)				6.0	5.0	5.0	5.0
Footprint drive efficiency - vertical GAA, 3x NWs stacked				2.8	3.9	3.9	3.9
Defice effective width - [nm]	92.0	90.0	56.5	56.5	56.5	56.5	56.5
Device lateral half pitch (nm)	21.0	18.0	12.0	10.0	6.0	6.0	6.0
Device width or diameter (nm)	8.0	6.0	6.0	6.0	5.0	5.0	5.0

1.3 Aims and objectives

The main objective of this project is to investigate the electrical characteristics of FET devices based on the stressor effect and design parameters with respect to the devices' performance. The research outcomes can be used as a guideline for designer in determining the most optimal structures in terms of stressor effects, geometrical and process design depends on the specific device requirements. In the next chapter, various study has shown that the device performance is affected significantly by considering the devices' design parameters for different performance aspects. Therefore, the purpose of this study is to present the analysis on the device performance of FET devices, designed

using Synopsys Sentaurus technology computer-aided design (TCAD) simulation tools. The objectives can be divided as follows:

1. To investigate the influence of stressors on the current-voltage (I-V) as well as electrical performances of fin shaped field effect transistor (FinFET) and heterostructure field effect transistor (HFET) by incorporating group IV and III-V compound semiconductor, respectively, with various mole fractions (xmole).
2. To investigate the impacts of geometrical and process design considerations of 10/7 nm stress engineered (SE) Ge based FinFET and optimized design of GaN based HFET on the devices' electrical characteristics.
3. To determine the optimized designs of 7 nm strained Ge FinFET for high power application using Taguchi method and Pareto analysis of variance.

1.4 Scope of work

Based on the list of objectives stated above, this study will focus on the issues arise in advanced FET technology, i.e. mobility degradation, subthreshold leakage, etc., and optimization method that has been published by previous researchers in the same field. An advanced tool, Synopsys Sentaurus TCAD device simulator will be used to its maximum capability in studying the characterization of advanced FET devices where the I-V and electrical characteristics of SE FinFET and HFET devices. By adopting advance physical models in the TCAD simulator, various test conditions and different structures of the investigated FET devices can be studied. The test conditions focus on the stress effect, geometric and process design considerations, which follows the ITRS standards for the development of advanced FET technology. Figure 1.1 shows the methodology overview for this work. The device under test are the advanced FET devices, that is a SE 10/7 nm FinFET and GaN based HFET for low and high-power application, respectively.

Critical device attributes such as threshold voltages (V_t), on-state (I_{on}) and off-state current (I_{off}), DIBL, subthreshold swing (SS) and many more were analysed to provide a comprehensive assessment of the device performance. Current density, electric field, and carrier velocity distribution as well as stress and doping profile would provide a clear understanding of all the parameters dependency to the FET devices' behaviour.

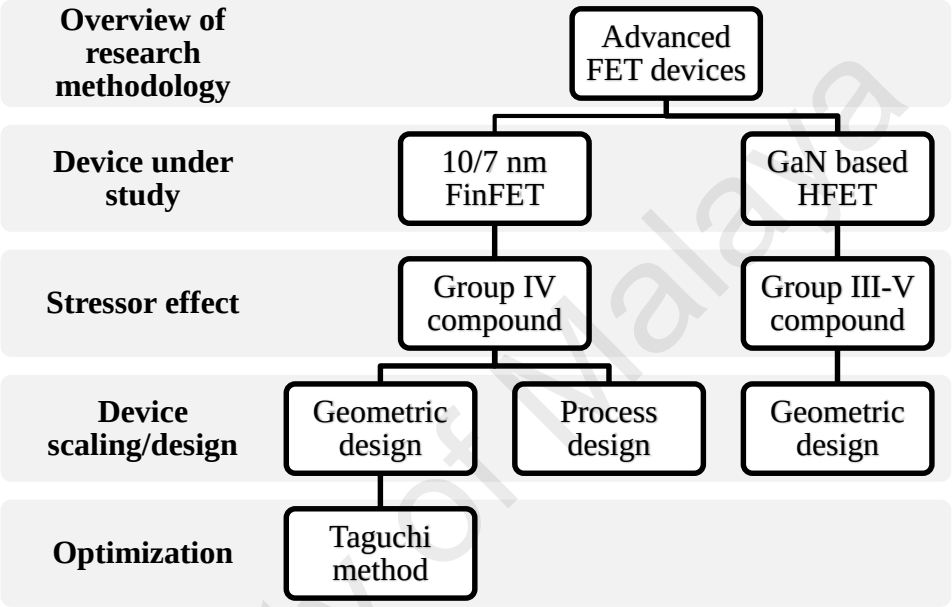


Figure 1.1: Overview of the methodology approached in this work.

1.5 Dissertation outlines

The structure of this thesis is arranged as follows:

Chapter 2 – Literature review section highlights an in depth study of the structure of a high performance SE FinFET and a high electron mobility transistor (HEMT), or also called as HFET. The basic operations of the devices are described in detailed to give understanding of the devices intrinsic behaviour from the characterization technique and measurement perspectives. The reviews include earlier works from both simulation and experimental studies for the strained FinFET and HFET under stressor effect, geometrical and process design considerations.

Chapter 3 – Research methodology section comprises the device and simulation conditions in obtaining the device performance and trade-offs for the study. This section will firstly describe the overall project flow for the research, followed by detailed description of each project flow including the list of investigated design parameters, configuration of simulation conditions, flowchart of the design process, illustration of the device design structures used and advanced physical model implemented in the TCAD. The measurement of I-V characteristic is carried out in this research and is explained, together with the statistical analysis method assimilated to obtain optimized performance.

Chapter 4 – Results and discussion section presents the research findings obtained from this work. The various effects and structure applied in each FET device had been demonstrated based on the standard manufacturing trends. The effects of stressors, geometrical and process design considerations on high performance strained FET devices are discussed. This section also shows the 3D view structure of devices during operation with respect to electrical parameters extracted including current distribution, mobility enhancement, etc. Selected results were validated with the experimental data reported from previous research.

Chapter 5 – Conclusion section comprises the summary of the research and future work. In this section, the work presented in this dissertation is concluded and reaffirmed. A table of summary is presented based on stressor, geometric and process design consideration for general overview of its impact. An optimized fin geometry design is proposed and its performance is compared with previous work. Finally, the direction of future research is discussed and a few recommendations were made.

CHAPTER 2: LITERATURE REVIEW

2.1 Introduction

This chapter describes in details on the important aspect in designing FET device, particularly CMOS and heterojunctions, based on MOSFET and heterostructure (HS) operations, respectively, and its technology developments over the years. Several innovations from outstanding research in enabling the enhancement and scaling of FET devices were reviewed to give clear understanding on its physical mechanism and potential impact to the device performance, prior to simulation analysis. The reviews take into accounts both experimental and simulation work according to the stressor, geometrical and process design considerations.

2.2 Basic MOSFET operation

MOSFET is widely used in digital circuit applications because of its relatively small size. Due to that, thousands of devices can be fabricated in a single IC (Kang & Leblebici, 2003). Figure 2.1 shows the MOSFET structure, which consist of metal gate, oxide, and semiconductor. Typically, the semiconductor used is a Si with a thin layer of insulator of silicon dioxide (SiO_2) between the source and drain region and a metal electrode called the metal gate, layered on top of the SiO_2 insulator layer. MOSFET can be used as an analog switch and amplifier due to its ability to change conductivity with an amount of applied voltage. There are two types of MOSFET which are n-channel MOSFET (n-MOSFET) and p-channel MOSFET (p-MOSFET). An n-MOSFET has an n+ doped source and drain region, as shown in Figure 2.1. It produces an n-type channel between the source and drain when a certain amount of voltage is applied which is called the inversion channel. Since MOSFET can be made with either n-type or p-type semiconductors, complementary pairs of MOS transistors can be used to make switching circuits with very low power consumption, in the form of CMOS logic (Wanlass & Sah, 2017), shown in Figure 2.1(b).

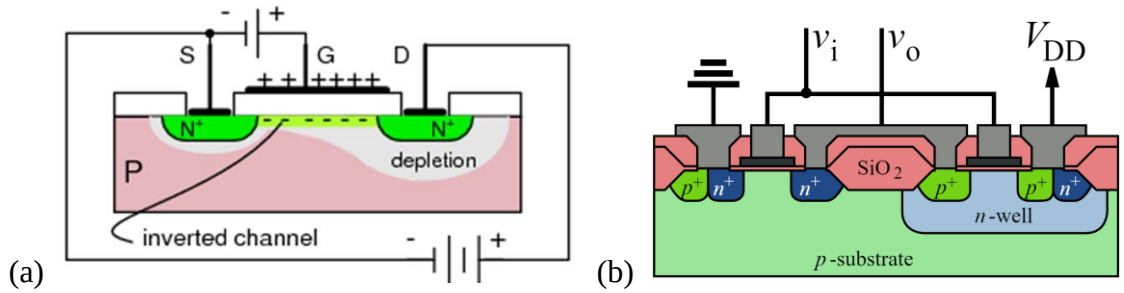


Figure 2.1: Schematic view of a (a) basic n-channel MOSFET structure, (b) CMOS switching circuits/inverter.

2.2.1 MOS capacitor

The heart of MOSFET is the MOS capacitor as shown in Figure 2.2. Usually in many cases, the metal is a high-conductivity polysilicon gate that is deposited on the oxide. However, the scaling of MOSFET leads to the implementation of extremely thin gate oxides by which can cause several effects to the device operations. Therefore, one solution to counter this problem is by implementing a high dielectric (high-k) material such as hafnium oxide (HfO_2) on top of the oxide layer (J. H. Choi, Mao, & Chang, 2011). Figure 2.2 shows a MOS capacitor with a p-type semiconductor body. The top metal is at a negative voltage, with respect to the voltage applied. A negative charge will exist on top of the metal plate and electric field will be induced from the body to the metal plate direction. If the electric field were to penetrate into the semiconductor, the majority carrier holes would experience a force toward the oxide-semiconductor interface.

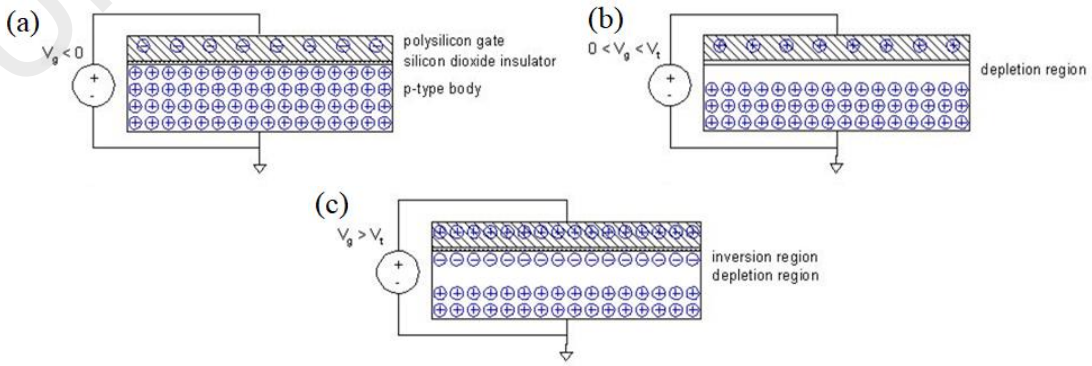


Figure 2.2: Basic operation of MOS capacitor in (a) accumulation region, (b) depletion region, and (c) inversion region.

Figure 2.2(a) shows the distribution of charge in the MOS capacitor at when a negative voltage is applied. An accumulation of layer of holes corresponds to the positive charge on the bottom plate of MOS capacitor is produced when a negative voltage is applied to the metal plate. When positive voltage is applied at the top metal plate, the positive charge will be distributed at the top metal plate. The electrostatic field will push away the positive charge on the bottom plate of the MOS capacitor, thus producing a blank space at the top of the bottom plate called the depletion region as shown in Figure 2.2(b). When larger positive voltage is applied at the top metal plate, larger electric field will be induced and the positive charge at the top plate will also increase in magnitude. The electrostatic field will attract the excess negative charge in the body to the top of the bottom plate, forming a layer of negative charges below the top metal plate called the inversion region.

2.2.2 MOS field effect transistor

A MOSFET structure consist of MOS capacitor with highly doped source and drain region at both sides. Usually for n-MOSFET, the source and the body are grounded, and positive voltage is applied to the drain under typical bias conditions. The operation of MOSFET is closely related to the operation of the MOS capacitor. If reverse bias is applied, there will be no current flow between the source and drain. In this state, the transistor is turned off and acted as an open switch. However, if large positive voltage is applied to the gate, the electron will be attracted to the region under the gate oxide, forming an inversion layer of electron connecting the source and drain region called the channel. The channel forms a bridge between the source and drain to allow the current flow between the electrodes. The transistor in this state is turned on and behaves as a closed switch. On the contrary for p-MOSFET, the channel bridge of holes will be formed under the gate oxide when a large negative voltage is applied to the gate. This transistor acted as a closed switch when the reverse bias is applied.

2.3 Heterostructure field effect transistor

HFET, also known as HEMT is a FET device consist of two materials of different band gaps forming a heterojunction channel instead of highly doped region in most MOS devices. Figure 2.3 illustrates the basic designs of a commonly used aluminium gallium arsenide (AlGaAs) HFET which is lightly doped as a barrier, placed on GaAs channel layer forming a heterojunction between them. The HS cause the device to have two different band gaps energy, thus results in the bending of conduction and valence band throughout the materials in order to form continuous level, shown in Figure 2.4. Electrons from the n-type region will move through the lattice and remain close to the junction, forming a thick electron layer known as a two dimensional electron gas (2DEG), as shown in Figure 2.3 and Figure 2.4. The electrons are able to move freely within this region due to less electron collisions caused by the absence of other donor electrons, which in turns produce a very high electron mobility. When a bias is applied to the gate, Schottky barrier will modulate the number of electrons in the channel formed from the 2DEG, which then controls the conductivity of the device.

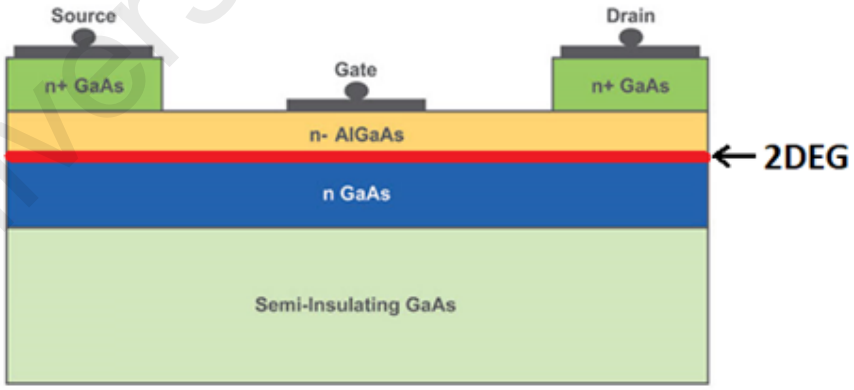


Figure 2.3: Basic design of AlGaAs HFET showing the position of 2DEG layer (TriQuint Semiconductor Inc., 2007).

HFET operation is somewhat different to other types of FET devices, which as a results able to give improved performance over standard MOSFET devices especially in microwave radio frequency (RF) applications (Lenka, Dash, & Panda, 2013). Besides

exhibit a very low noise figure, HS device was specifically developed for high speed applications (Shinohara et al., 2002) due to the nature of 2DEG as well as less electron collisions. These traits are the main reason why they are widely used in low noise small signal amplifiers, power amplifiers, and oscillators which operates at high frequencies. Furthermore, HFET devices are also used in a wide range of RF design applications including cellular telecommunications, radar, radio astronomy, and any RF applications that requires a combination of low noise and high frequency performances.

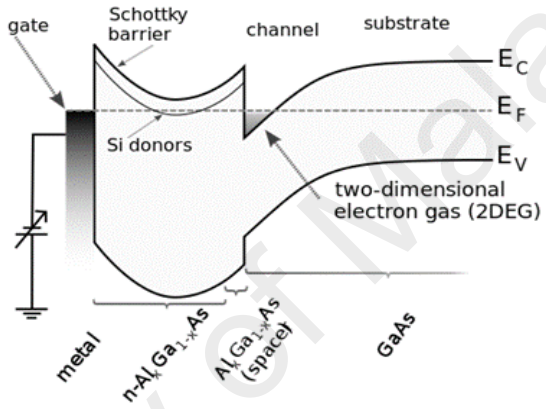


Figure 2.4: Band gap alignment of AlGaAs/GaAs heterojunction at equilibrium ("High electron mobility transistor," 2018).

2.4 Issues in FET devices performances

Device scaling has been practiced continuously in the past few decades to allow more transistor to be built in a dense IC chip. The length of the channel that separates the source and drain region are becoming very small as the transistor are reduced to approximately half their previous sizes. While the on current improves greatly along this action (Kuhn, 2011), the switching behaviour are becoming worse in sub-nanometer regime due to the current trade-offs in device down scaling, especially the increasing of leakage current and threshold voltage roll off (M. Zakir Hossain & Khosru, 2013). The diagram in Figure 2.5 summarizes the trade-offs factor among on-current, leakage currents, and SCE by advanced device scaling along with possible solution to reduce the problems (Takagi et al., 2008). Hence, extensive researches are required in order to mitigate the challenges

where the conventional MOS structure needs to evolve using innovative alternatives to achieve better performances in current trade-offs.

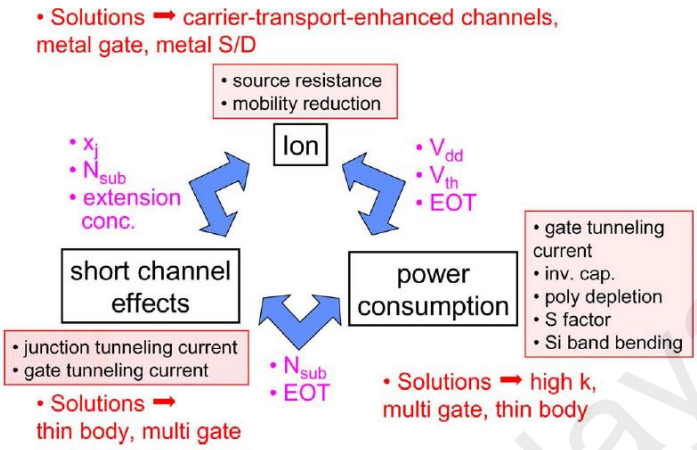


Figure 2.5: Several issues rises from device scaling in sub-nanometer regime transistor (Takagi et al., 2008)

2.5 Innovation for FET technology

The advancements in the electronics industry have been primarily based on downscaling the minimum transistor size according to Moore's law (Chi, 2012) for the past decades. Figure 2.6 shows the plot of transistor counts against dates of introduction, note the logarithmic vertical scale, where the distribution corresponds to exponential growth with transistor count doubling every two years. It is also noted that the power density is deem to be constant due to the reduction of voltage and current reduction with feature sizing as mention by Dennard et al. (1974). Since then, Moore's law has been moving in line with Dennard scaling theory. However, device scaling is limited due to several effects like SCEs, subthreshold conduction, mobility degradation, etc., which can alter the circuit functionality and degrades the performance of the systems, especially when dealing with the sub-nanometer device. Hence, alternatives structures and materials has been taken into account favourably with case studies conducted by other researchers in order to produce better trade-off FET performances.

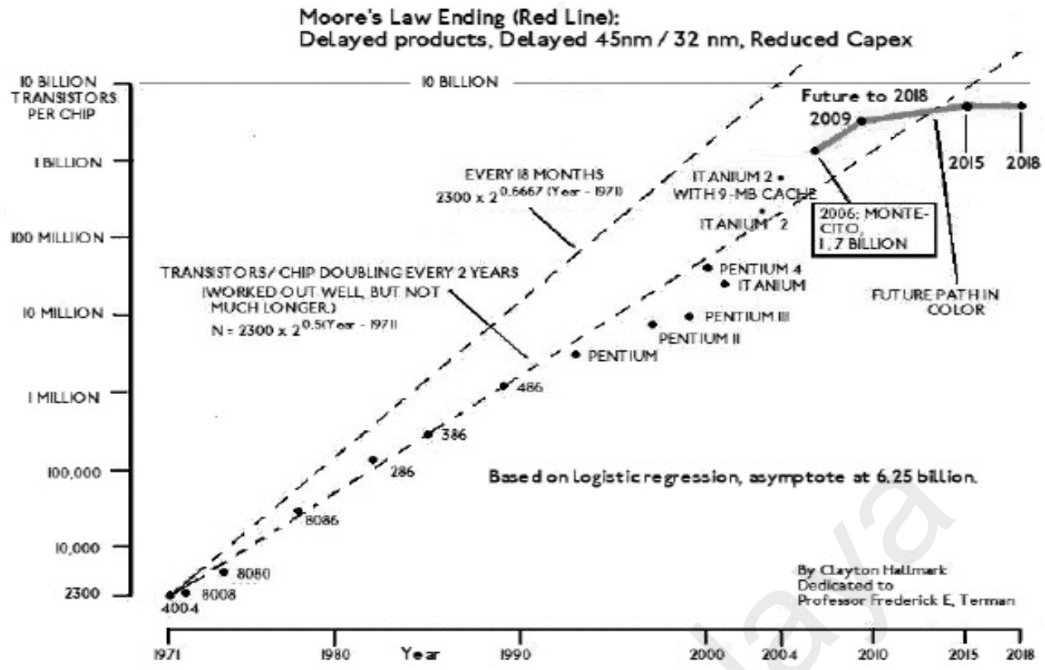


Figure 2.6: Transistor per microprocessor counts graph for 1971-2018, as predicted by Gordon Moore (Kress, 2006).

2.5.1 Strain/stress engineering

Strain/stress engineering are implemented widely in advanced CMOS and FET devices due to its ability to enhance carrier mobility (Serra & Esseni, 2010), especially in sub-nanometer devices (Guo et al., 2014; Xie et al., 2016). Several types of stressor are used in CMOS fabrication process to create appropriate stress to the device structures includes the shallow trench isolation (STI) (Tomimatsu et al., 2013), contact etch stop layer (CESL) (Xu, Sun, Xiong, Cleavelin, & Liu, 2010), as well as source/drain (S/D) epitaxy and stress relaxed buffer (SRB) stressor (Gupta, Moroz, Smith, Lu, & Saraswat, 2014). Strain S/D region for CMOS devices usually adopted with silicon carbide (Si:C) for n-type (Chung-Yi, Shu-Tong, Jacky, Wei-Ching, & Jun-Wei, 2007) and silicon germanium (SiGe) compound in p-type devices (M. Choi, Moroz, Smith, & Penzin, 2012). The SiGe and Si:C S/D stress are embedded in order to produce compressive and tensile longitudinal stress to the p-FinFET and n-FinFET, respectively. Due to the enhanced stress effect in the device structure, the carrier mobility can be improved effectively hence improving the performance in terms of device on current. Meanwhile,

the SRB stressors are reported to be beneficial in delivering high biaxial channel stress, by which in FinFET, can also improve the uniaxial longitudinal stress due the aspect ratio of the fin (Eneman et al., 2013). Figure 2.7 shows the comparison of percentage increase in mobility with respect to different types of stressor for Ge based p-FinFET. According to the report, the SRB stressors are the most effective stressor to give impact on the device mobility by more than 80%. This work suggests that the mobility boost for CMOS devices can be achieved if the SRB stressor are to be combined together with S/D stressor, especially for 14 nm technology node and beyond (D. S. Huang et al., 2018).

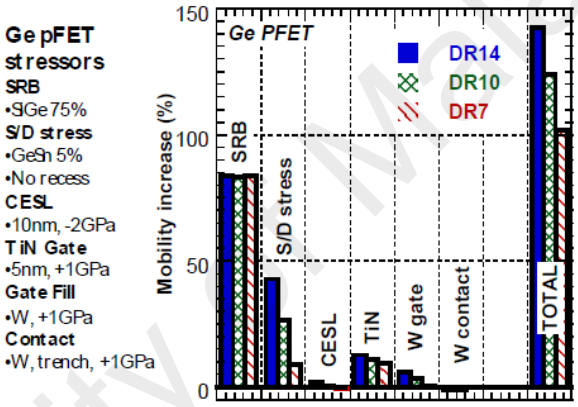


Figure 2.7: Comparison of percentage increase in mobility for 14, 10 and 7 nm Ge p-FinFET (Eneman et al., 2013).

2.5.2 Multigate MOSFET devices

In addition, as device downscaling continue to progress, a gate of conventional CMOS device no longer has the ability to control the channel due to severe SCE. Therefore, other alternative is to introduce new structures with more than one gate into a single device such as double gate, trigate (Yan et al., 2007), and quadruple gate MOSFET (H. Lee et al., 2006). Apparently, additional gate to the device structures improves the SCE and prevent excessive current leakage from the channel. Figure 2.8 illustrates various silicon-on-insulator (SOI) devices from a single gate to the surrounding gate of FET. The double gate MOSFET are reported to exhibit better on-off switching compared to the

conventional MOSFET, besides having improved carrier mobility and better SCE suppression (George James, Joseph, & Mathew, 2010). Another type of double gate MOSFET is in non-planar structure, called as FinFET (M Zakir Hossain, Hossain, Islam, Rahman, & Chowdhury, 2011) has also become an evolution in boosting device performance for its impressive on current improvement in saturated region and suppression of leakage current in subthreshold region (X. Huang et al., 2001). Mass production of 10 nm FinFET (Samsung, 2016) has made the researches to enter into 7 nm regime in 2 years as predicted.

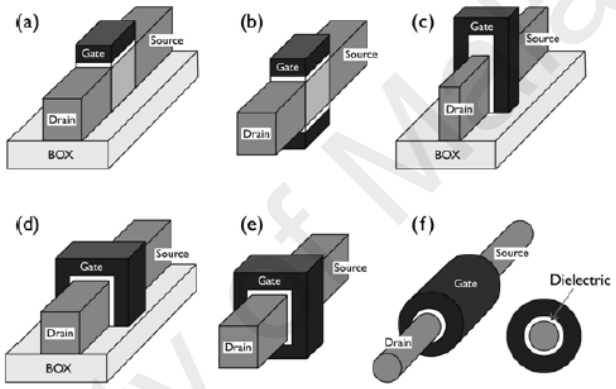


Figure 2.8: Evolution of MOSFET device: (a) conventional, (b) double gate planar, (c) FinFET, (d) trigate, (e) GAAFET, and (f) nanowire (Kim, 2010).

2.5.3 Group IV and III-V FinFET

Search of solutions to overcome scaling challenges beyond Moore's law continues by adopting alternate channel materials, such as group IV and III–V compound that show higher electron and hole mobility compared with Si, considered for future technology nodes. Earlier research demonstrated successful implementation of indium gallium arsenide (InGaAs) channel in FinFET where the SS, DIBL and V_t roll-off is greatly improved (Y. Wu, Wang, Shen, Gu, & Ye, 2009). This idea was supported by Moroz et al. (2014), implemented in FinFET and nanowires structures, suggesting further optimization needs to be done to achieve improvement in device performance. Other than channel, SRB and S/D region with compound materials are also proposed as new type of

stressor implemented for SE devices. Previous report suggested that other than Si, group IV semiconductors such as Ge, tin (Sn) and their alloy shows excellent capabilities in band gaps and quantum confinement for p-type devices (Gupta, Moroz, Smith, Lu, & Saraswat, 2013). With proper amount of Sn xmole in S/D region for p-FinFET, channel stress can be tuned to obtain performance improvement over strained Si CMOS devices. Figure 2.9 illustrates the longitudinal channel stress improvement by opting the xmole of dopant and lattice constant in the S/D and SRB region, respectively. In this research, SiGe is used as the main compound in S/D and SRB region due to its high hole mobility as well as capabilities in band gaps confinement especially in p-type devices.

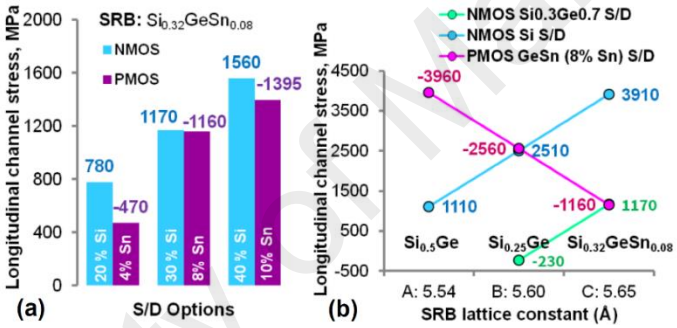


Figure 2.9: Channel stress distribution for various (a) Si% in n-FinFET (SiGe), and Sn% in p-FinFET (SiGeSn), (b) lattice constant of SRB (Gupta et al., 2013).

2.5.4 HFET with group III-V implementation

HFET devices provide very high levels of performance at microwave and RF applications (Lenka et al., 2013), especially when incorporated with indium (In). The most common materials used at the heterojuctions are AlGaAs and GaAs. GaAs based HFET is generally used as it provides a high level of basic electron mobility and this is crucial to the operation of the device. AlGaAs/GaAs HFET is excellent in handling wide range applications. Hence, a large-signal application for GaAs based HFET is modelled by Jia et al. (2016), particularly for monolithic microwave IC amplifier design (Chiong, Chen, Kao, Wang, & Chen, 2016). This model can predict accurate power gain as well as output power efficiently. Apart from that, a metamorphic HEMT (MHEMT) on GaAs

based substrate shows excellent direct current (DC) and RF characteristics (Ajayan & Nirmal, 2017). At RF, outstanding high frequency performance is achieved by this device by the reducing the parasitic capacitances, hence making it the most promising device for millimetre wave applications (Schlechtweg et al., 2016). Besides that, a study on a MOS HFET is done by Gregušová et al. (2017) by adding an oxide layer on top of an AlGaAs barrier layer which can improve the electron transport of the device. With the presence of oxide layer, the gate leakage is reduced significantly. Other than GaAs based HFET, GaN based is also widely used for the HS for its high power handling capabilities (Firoz & Chauhan, 2011). In fact, studies have shown that aluminium gallium nitride (AlGaN) devices show better thermal stability (Alim, Rezazadeh, & Gaquiere, 2016) particularly in high temperature (Hou, Liu, Teng, Palacios, & Chua, 2017) compared to AlGaAs. Figure 2.10 illustrates the temperature dependent of the cut off (f_t) and maximum frequency (f_{max}), showing GaN HEMT has better traits and higher frequencies compared to the GaAs HEMT. Moreover, GaN devices are also implemented in ultrahigh frequency, particularly in small signal RF and microwave applications (Lenka, Dash, & Panda, 2014). Apart from being outstanding in high temperature, GaN based HFET can also improve the curent (Xiang-Dong et al., 2015) and off-state breakdown voltage (Arulkumaran et al., 2012) significantly compared to GaAs devices.

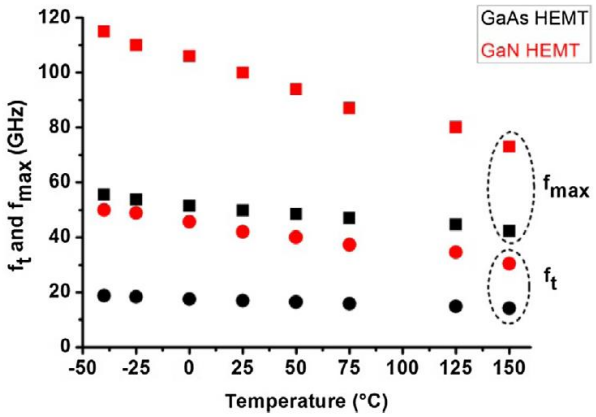


Figure 2.10: Temperature-dependence of the f_t and f_{max} for the GaAs and GaN HEMT (Alim et al., 2016).

2.6 FET device scaling

Recently, mass production of the 10 nm technology has been successfully distributed by the industry (Samsung, 2016), while the 7 nm technology is still in an ongoing research (Morris, 2016). Innovation of these devices has made the FinFET technology to become one of the promising candidates in overcoming the end of Moore's law (N A F Othman, Hatta, & Soin, 2018), especially when the device structures are incorporated with compound semiconductor (Moroz et al., 2014). Prior to this technology, the downscaling of FinFET devices are actively practiced by chip designers. In order to increase the density of transistor on an IC chip, the device structures need to be smaller. In this case, fin geometry plays a major role. As the fin sizes become smaller and in tapered shape, the gate control over the channel can be maximized (F. A. M. Rezali, Othman, Mazhar, Hatta, & Soin, 2016) despite having a slight degradation in SCE and parasitic resistances. Figure 2.11 presents the current distribution for a 14/16 nm technology FinFET with aggressively scaled fin geometry, note that the current density is pushed into the middle of the fin to reduce the effect of leakage with tapered shape.

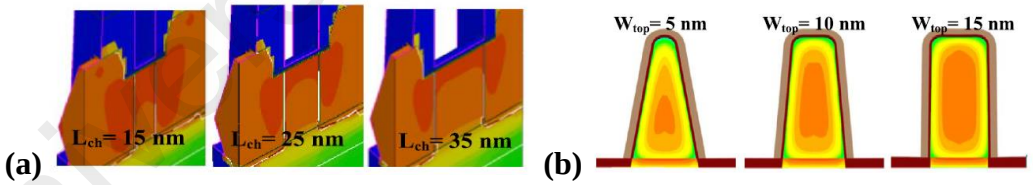


Figure 2.11: Current density distribution in (a) scaled channel length, and (b) scaled top fin width (F. A. M. Rezali et al., 2016).

Meanwhile for HFET, device scaling is affecting the device performance with the same importance. Khan et al. (2013) reported that the device performance of GaN based double HFET is significantly depend on device scaling. It is found that a decrease in source–gate length (L_{sg}) can improve device performance, enhancing the device output current and the transconductance (g_m). Moreover, thicker buffer layer can enhance the reverse gate leakage and have high breakdown voltage (Arulkumaran et al., 2012), as

reported by Yu et al. (2014). Apart from that, spacer layer also plays an important role in device performance improvements. Additional aluminium nitride (AlN) layer between the heterojunction can improve the 2DEG concentration and mobility due to the raised in quantum well depth and reduction in alloy scattering (Roy, Jawanpuria, Prasad, & Islam, 2015). Previous report shows that the ohmic resistances of S/D contact can be altered by the scaling of AlN spacer thickness (Shrestha, Li, & Chang, 2014).

2.7 Doping consideration of FET devices

As far as geometry scaling is concern, process design and scaling also give major impact on the device performances. Doping alteration is widely being studied for process design in order to adjust the threshold voltage and current trade-offs. However, this action is expected to degrade the device variability due to random dopant fluctuation especially in FinFET with advanced technology nodes (Yan, Afzalian, Lederer, Lee, & Colinge, 2008). Apart from that, Lin et al. (2012) suggest that the channel doping needs to be lower than a few 10^{18} cm^{-3} in 22 nm node FinFET and beyond for its to retains variability advantage over conventional MOSFET. As channel doping increases, the DIBL degrades due to higher threshold voltage extractions. Besides, doping concentration can be controlled to suppress SCEs in order to achieve reasonable threshold voltage with low leakage (Yadav & Rana, 2012). As HALO and substrate doping increases with reduced S/D doping, the threshold voltage extracted is also high. Other than that, doping in S/D regions is also important in providing enhanced carrier mobility of the channel (K. Kumar, Anil, & Rao, 2014) . High doped S/D doping could diffuse into the channel and increases the doping in short channel devices. Meanwhile, too high of channel doping can lead to severe current trade-offs. Therefore, doping concentration needs to be optimized where the tuning of doping are taken into account to design the most optimal doping combination for particular performance applications (F. M. Rezali, Rasid, Othman, Hatta, & Soin, 2016). In addition, the effect of doping on HFET performance is also significant.

The optimum doping is more useful in terms of high power, high frequency response and lower parasitic capacitance for GaN based HFET behaviour (Firoz & Chauhan, 2011).

2.8 Optimization by Taguchi method

In order to make sure the device scaling can contribute continuous improvement in the device performance especially in semiconductor manufacturing industry, the design requirements should be optimize using better tools and techniques. Taguchi method is one of many systematic techniques that can be apply for optimization process to study the combined effect with respect to device performance. This method allows complex problems to be solve with least variables in small number of experiments (X. Wu & Zhou, 2011) which can save time (Zhu, He, & Li, 2015). In Taguchi method, the parameters or critical factors that affecting the device performance are identified. These parameters are then adopted with the signal-to-noise ratio (SNR) as the quality of choice. There are three type of SNR characteristics used for continuous conditions (Ghani et al., 2004), categorized as follows:

i. the larger the performance response, which is used when the design is aiming to maximize a performance metric, namely larger the better characteristics (LTB), expressed in Eq. 3.1:

$$\frac{S}{N} = -10\log\frac{1}{n}\left(\sum\frac{1}{y^2}\right) \quad \textbf{(2.1)}$$

ii. the smaller the performance response, which is used when the design is aiming to minimize a performance metric, namely smaller the better characteristics (STB), expressed in Eq. 3.2:

$$\frac{S}{N} = -10\log\frac{1}{n}\left(\sum y^2\right) \quad \textbf{(2.2)}$$

iii. the smaller the performance variance to the target, which is used when SNR is applied to an on-target design, namely nominal the best characteristics (NTB), expressed in Eq. 3.3:

$$\frac{S}{N} = 10\log\left(\frac{\hat{y}^2}{s_y^2}\right) \tag{2.3}$$

where n is the number of observations, y is the observed data, $\hat{y}$ is the observed data average, and s_y^2 is the variance of y. The average data is expressed in Eq. 3.4 while the variance of y is expressed in Eq. 3.5.

$$\hat{y} = \frac{y_1 + y_2 + ... + y_n}{n} \tag{2.4}$$

$$s_y^2 = \frac{\sum_{i=1}^{n}(y_i - \hat{y})}{n-1} \tag{2.5}$$

2.9 Summary

This chapter gives an overview of challenges encountered by the scaling down of CMOS devices and innovations on how to mitigate the problems. The selected parameters and its important findings from various research of advanced FET devices were discussed in this section. The performance of advanced FET designs was described based on the existing methods that shown to be a valuable goal towards achieving the high FET device performance. To further evaluate the device performance of each technology node, a robust design needs to be employed in order to understand the operation of the transistors with regards to the performance. Research works concerning device performance by parametric design approach are limited, as most of the previous work mainly focuses on the effective performance from a particular transistor design as shown in Table 2.1 and Table 2.2. With the recently production of 10 nm technology nodes, it has led to concerns over the end of Moore's law, particularly in the downsizing of device structure geometry. Alternatives and innovations are important for design engineers in order to ready

themselves in facing new scaling vector, especially in the use of group IV and III-V compound semiconductor as Si replacements as well as implementation of statistical methods in characterizing the device and electrical performances of FET technology.

Table 2.1: Summary of FinFET study by previous researchers

Node/device under study	Type of stressor	Group IV/III-V implementation	Design parameters considered		Effect on device performance	References
			Geometry	Process		
14 nm SE FinFET	- STI stress - CESL - S/D epitaxy - Metal gate intrinsic stress	- SiGe S/D (50% Ge) in p-FinFET - Si:C S/D (2% C) in n-FinFET	- Gate length - Fin height - Fin width	- Strain effect - Doping concentration - Work function	- Small, tapered fin maximize gate control but degrades the SCEs and increase parasitic components - Strain devices improved I_d	(F. A. M. Rezali et al., 2016)
7 nm SE FinFET	- Channel stress - SRB stressor - STI stress - S/D epitaxy	- GeSn p-FinFET (4% Sn) + GeSn S/D (8% Sn) - Ge n-FinFET + SiGe S/D (70% Ge)	- Fin width	- Fin orientation - Lattice constant	- Channel stress improves device performance - Thin fin reduces leakage - Group IV elements improves bandgap and SE capabilities	(Gupta et al., 2014)
7 nm FinFET	- S/D epitaxy - STI stress - SRB stress	- SiGe n-FinFET (50% Ge) - InGaAs n-FinFET (50% Ga)	- Fin height - Aspect ratio	- Ge% in SiGe n-FinFET - Ga% in InGaAs n-FinFET - Surface orientation	- High aspect ratio to prevent excessive I_{off} - <40% Ge in SiGe and <20% In in InGaAs channel satisfy low leakage specification.	(Moroz et al., 2014)

Table 2.1 continued

Node/device under study	Type of stressor	Group IV/III-V implementation	Design parameters considered		Effect on device performance	References
			Geometry	Process		
22 nm bulk FinFET	- Channel strain	- N/A	- Fin shape - Gate-S/D overlap	- Body doping concentration	- Triangular fin results in 70% reduction in I_{off}	(Gaynor & Hassoun, 2014)
14/10/7 nm FinFET	- SRB stressor - S/D epitaxy - CESL - Intrinsic stress - Stressed trench contacts	- Ge p-FinFET + SiGe SRB (75% Ge) + GeSn S/D (5% Sn) - Si n-FinFET + SiGe SRB (25% Ge) + Si:C S/D (5% C)	- Gate length - Fin width - Fin height - Contact size	- Sn% and Ge% in S/D region	- Mobility improves 80-130% with SRB stress - S/D stressors enhances mobility around 40-80% - Tensile gate degrades mobility by 10-30%	(Eneman et al., 2013)
22 nm bulk FinFET	- N/A	- Boron/Arsenide doped in n-FinFET	- Gate design length - Gate pitch	- Channel doping concentration	- Mobility degrades with increase doping - Doped FinFETs have advantages over planar MOSFET if $<10^{18}$ cm^{-3}	(Lin et al., 2012)
22 nm bulk FinFET	- S/D epitaxy - Channel strain	- Phosphorus doped SiC S/D in n-FET - SiGe channel in p-FFET	- Fin width - Gate length - Fin pitch	- Ge concentration - Anneal temperature	- Epitaxial P-SiC S/D stress improves mobility - Low anneal temperature improves strain of P-SiC - Narrower fin increase mobility	(Togo et al., 2012)

Table 2.2: Summary of HFET study by previous researchers

Device under study	Device structure	Group III-V implementation	Design parameters considered		Effect on device performance	References
			Geometry	Process		
AlGaAs/GaAs MOS HFET	- δ-doping between barrier and spacer - AlOx formation on top of barrier	- InGaAs channel - AlGaAs spacer	-	- δ-doping concentration - Operating frequency	- MOS HFET has low trap state density - Presence of oxide can reduce leakage	(Gregušová et al., 2017)
Metamorphic GaAs based HEMT	- Double δ-doping between barrier-spacer and spacer-buffer - Barrier layer with buried Pt metal - Graded buffer layer	- InGaAs S/D regions - Doped indium phosphide cap layer	-	- δ-doping concentration	- Doped S/D reduces R_{sd}, hence improve device speed - Double δ-doping layers improves drive currents - Platinum buried barrier reduces SCEs - Doped cap layer reduces access resistance	(Ajayan & Nirmal, 2017)
AlGaAs/GaAs and AlGaN/GaN HEMT	- Conventional HEMT structure	- Doped AlGaAs spacer - Undoped AlGaN spacer	-	- Temperature - Operating frequency	- GaN based HEMT possess better thermal stability - GaAs based HEMT has better ohmic contact	(Alim et al., 2016)
AlGaN/GaN HEMT	- Double HS - Graded buffer layer - AlGaN back barrier	- AlN spacer	- Channel thickness - Buffer thickness	- Al xmole in buffer	- Thicker buffer produce higher I_{on} - Higher breakdown voltage is achieved	(Xiang-Dong et al., 2015)

Table 2.2 continued

Device under study	Device structure	Group III-V implementation	Design parameters considered		Effect on device performance	References
			Geometry	Process		
AlGaN/GaN HEMT	- Graded buffer layer	- AlN spacer	- Buffer thickness	- Al xmole in AlGaN buffer	- Thick buffer has lower gate leakage and higher breakdown voltage	(Yu et al., 2014)
AlGaN/GaN HEMT	- Conventional HEMT structure	- AlN spacer	- Spacer thickness - Barrier thickness	-	- Presence of AlN spacer improves 2DEG density - Ohmic contact degrades with thickness >1.5 nm	(Shrestha et al., 2014)
GaN based HFET	- Double HS	- AlN barrier	- Source-gate length - Gate-drain length	- Al xmole in AlGaN buffer	- Reducing L_{sg} increased carrier density under the gate, lead to increased I_d - Higher leakage in increased Al xmole	(Khan et al., 2013)
AlGaN/GaN HEMT	- SOI substrate - Si substrate	- AlN spacer	- Gate-drain length	- Type of substrate	- Si and SOI substrate exhibit good pinch-off characteristics and high breakdown voltage	(Arulkumaran et al., 2012)

CHAPTER 3: RESEARCH METHODOLOGY

3.1 Introduction

This chapter consists of design and simulation conditions in characterizing different type of FET devices as well as method in analysing the device performance. The device under study includes the 10/7 nm n- and p-type SE FinFET and high power GaN based HFET, which were simulated using Synopsys Sentaurus TCAD. The device structures adopted with compatible physical models and the simulation conditions applied to the device in the Synopsys Sentaurus TCAD are discussed in detailed in the next sections. The device design considerations in terms of stressor, geometric, and process are selected with reference to the suitability and specifications requirement to the aims of the study.

3.2 Flowchart of overall project methodology

The overall project flow done to achieve the objectives of this work is presented in Figure 3.1. The device structures are generated using a TCAD software, namely Synopsys Sentaurus TCAD, which consist of several simulation frameworks such as Sentaurus Process, Sentaurus Device Editor, Sentaurus Device and Sentaurus Visual. These frameworks are used to deliver a replication of real fabrication steps in device design, simulating the electrical characteristics of the device and extracting important electrical parameters such as distributions of field, stress, and carrier density including 2D and 3D device visualization of the operating devices.

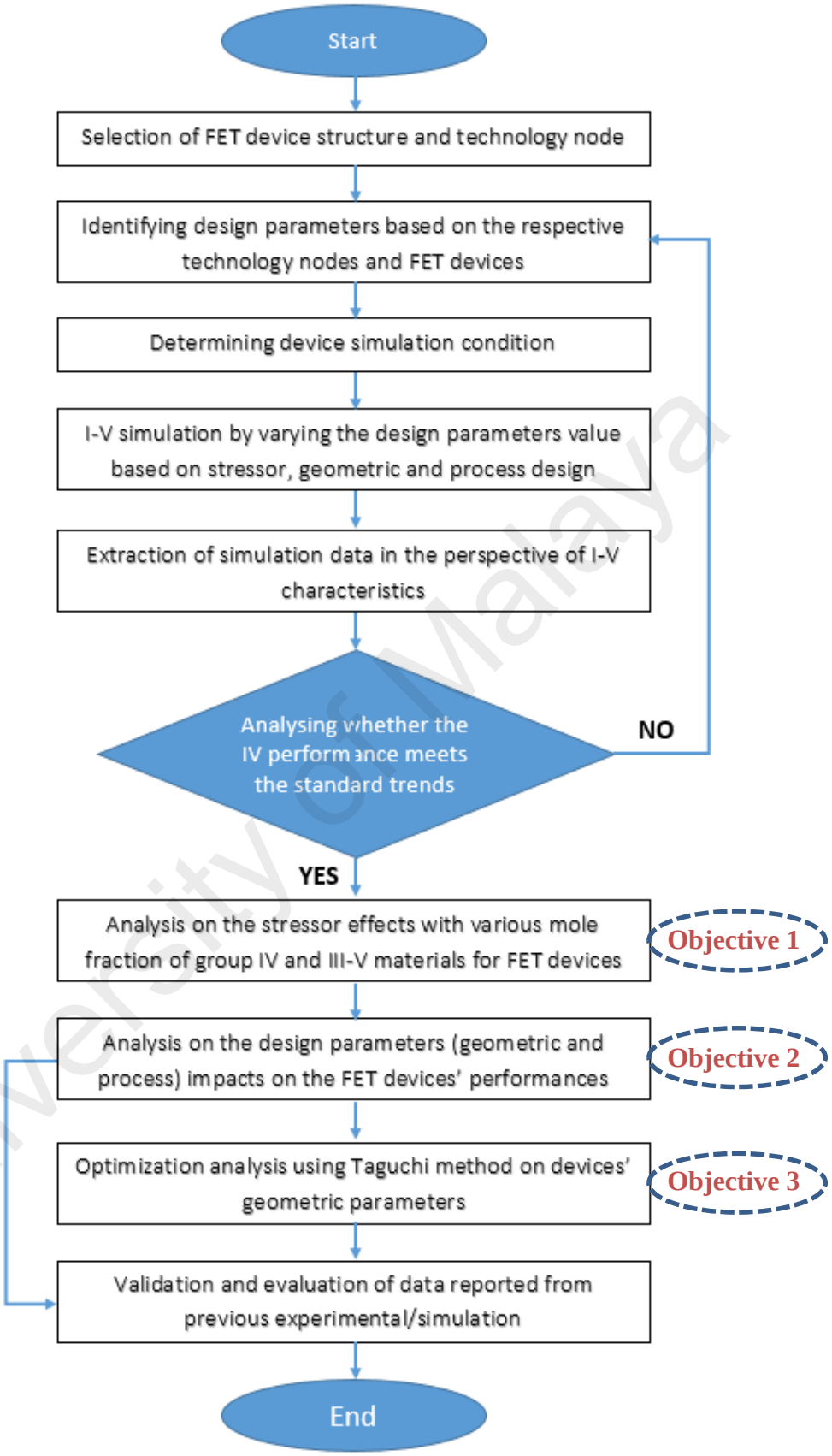


Figure 3.1: General overview of project flow.

3.3 Selection of FET device structure and technology nodes

3.3.1 7 nm stress engineered FinFET

One of the device under study for this work is a 7 nm SE p- and n-type FinFET, and the performance of both types devices were investigated (Synopsys Inc., 2014c). Figure 3.2 presents the process flow of the FinFET structure generation using the Synopsys Sentaurus TCAD simulator. Firstly, the device structures are generated by defining the fin with the side surface slope and 25 Å corner rounding at the top fin. Next, the STI is generated followed by the deposition of monolayers of oxide interlayer and HfO_2 high-k metal gate (HKMG). The gate which is made of polysilicon, spacer, and S/D epitaxy are generated afterwards. Ge is diffused into the channel and S/D region during the process to give impacts on the lattice mismatch stress components. Following these steps, the polysilicon is removed and the deposition of HKMG is performed. Finally, metal contacts and vias were created by etching and deposition method to connect each contact.

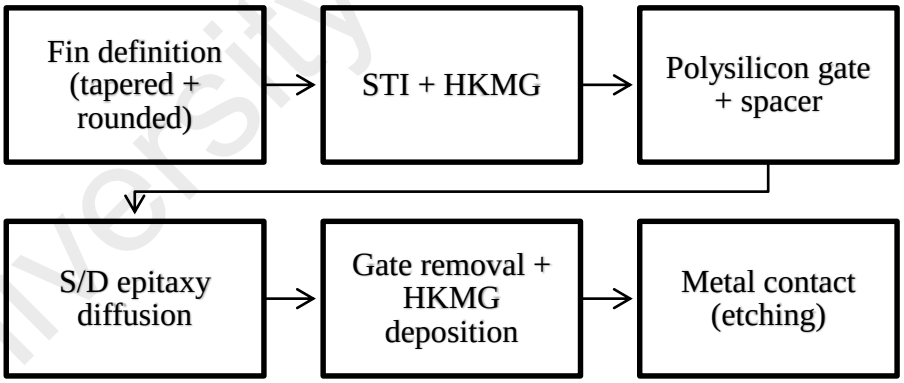


Figure 3.2: Structure formation flow for 7 nm FinFET design used in the simulation.

3.3.2 10 nm silicon germanium FinFET

For 10 nm SiGe FinFET, the device process generation is quite similar to that of 7 nm FinFET (Synopsys Inc., 2014b). The type of stressors applied to the device include STI, CESL metal stress and S/D epitaxy with SiGe grown for p-FinFET. Unlike 7 nm node FinFET structure which adopted SiGe doped n-FnFET devices, the S/D epitaxy for 10

nm FinFET is grown with Si:C with a SiGe based channel region. Table 3.1 gives the values of the fixed parameters used in the simulated devices for both 10 nm and 7 nm technology nodes FinFET given by the foundry (Synopsys Inc., 2014b, 2014c).

Table 3.1: Fixed geometrical parameters and values used in the simulation

Parameter	Values	
	10 nm	**7 nm**
Gate length, L_g	20 nm	15 nm
Fin height, H_{fin}	27 nm	30 nm
Top fin width, W_{top}	8 nm	5 nm
Bottom fin width, W_{bot}	8 nm	7 nm
Gate insulator thickness, t_{ox}	20 Å	17 Å
High-k thickness, t_{hfo2}	14 Å	11 Å
Interlayer oxide thickness, t_{iox}	6 Å	6 Å
Corner rounding radius, cr	25 Å	25 Å

3.3.3 Gallium nitride based HFET

2D HFET device structure is simulated through the device process simulator. For this device, the epitaxial layers of the original conventional $Al_xGa_{1-x}N$/GaN HFET device, where x indicates the xmole of Al (x = 0.25) are assumed to have grown in the [0001] gallium (Ga)-face direction on a Si substrate. The schematic cross sections of the conventional device are shown in Figure 3.3. The epi-structure consists of a 10 nm AlN nucleation layer formation after the substrate and an undoped GaN buffer layer with a thickness of 2.0 μm is grown after. Then, a thin channel layer of 5 nm is defined inside the buffer layer, followed by the growth of a thin interfacial spacer layer of 2 nm. Finally, an 18 nm barrier layer of the device was deposited and followed by GaN capping layer as well as silicon nitride (SiN) passivation were grown in sequences.

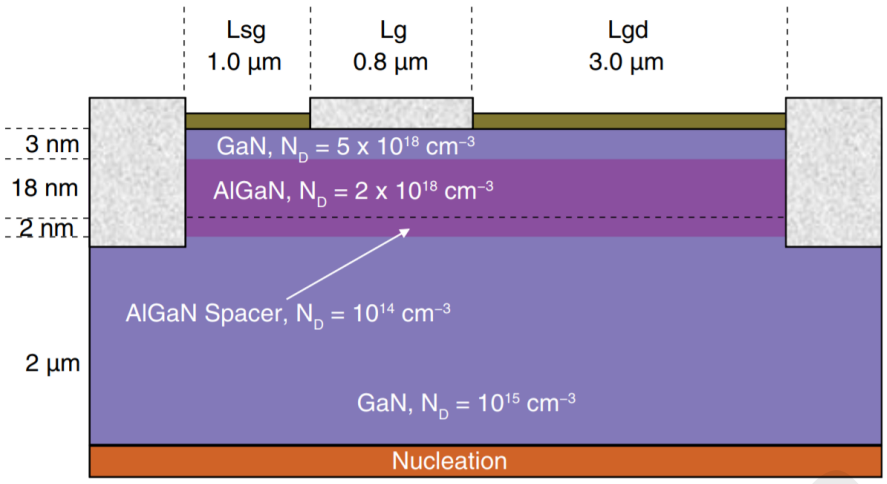


Figure 3.3: Schematic diagram of simulated GaN based HFET (Synopsys Inc., 2014a).

3.4 Identifying design parameters for FET devices

The investigated design parameters used for this work is illustrated in Figure 3.4. To study the impact of different structure of devices on FET performances, wide range of stressor, geometric and process variations were simulated and their impacts on the FET devices were analysed. To study the stressor effect on the device characteristics, different implementation and xmole of group IV and group III-V semiconductor inside each layers of particular FET devices were varied. In terms of geometric designs, the parameters involved includes the gate lengths, fin heights, top fin widths, as well as thicknesses of barrier, spacer, and buffer layers. The simulation is done by varying one parameter at a time to study the effect of a specific design parameter on the I-V characteristics, while keeping the others constant. Meanwhile for process design considerations, the performance of the device was studied by varying channel and S/D doping concentrations.

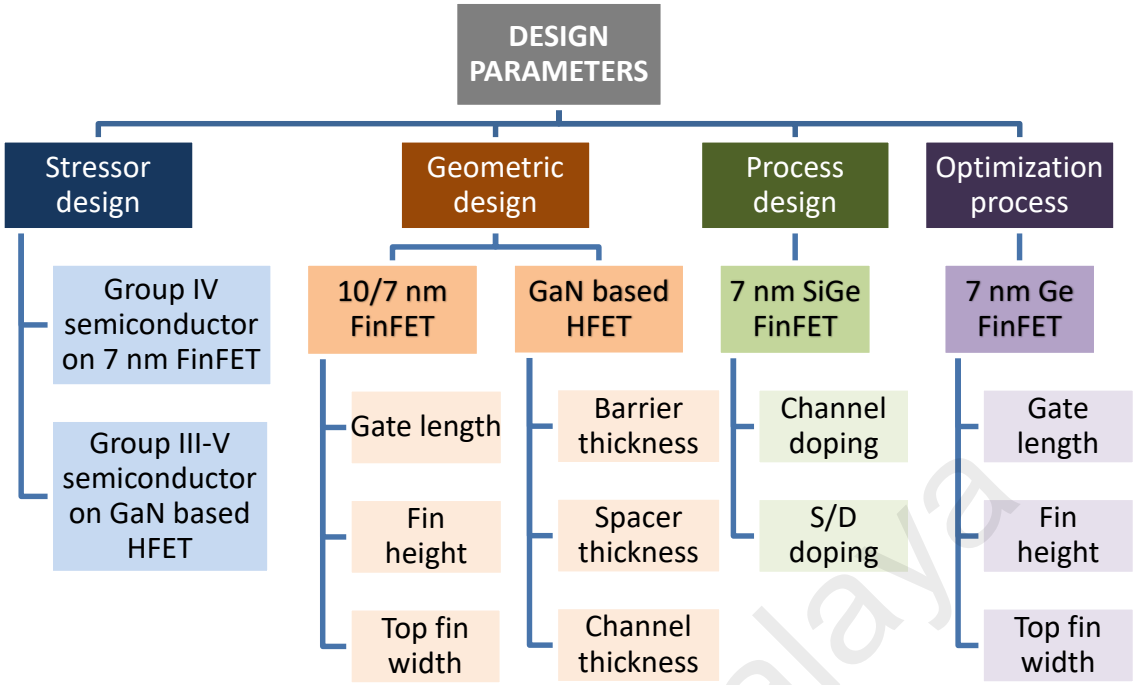


Figure 3.4: Design parameter considerations under study.

3.5 Determination of device simulation conditions

3.5.1 FinFET simulation model

For 10 nm node FinFET and beyond, the device structure is generated through an advanced calibration process (Synopsys Inc., 2013), where the simulation of Monte Carlo (MC) and drift diffusion (DD) model is adopted, to account the saturation velocity calibration (Bude, 2000) as well as high-k (Lombardi, Manzini, Saporito, & Vanzi, 1988) and thin layer mobility degradation mobility (Uchida, Koga, Ohba, Numata, & Takagi, 2001), respectively. The DD model introduced the ballistics mobility into the simulation by implementing the ballistic transport effects. This effect will increase the carrier mobility inside the medium by eliminating the excessive resistance caused by the scattering effects, namely impurities scattering. Figure 3.5 illustrates the project flow of the simulation models involved in this work. Moreover, advanced processing steps are also featured in the device process, including the Ge concentration and stress effect on the diffusion, SiGe SRB model, as well as the electronic band structure calibrated with MC model which accounts for scattering effects.

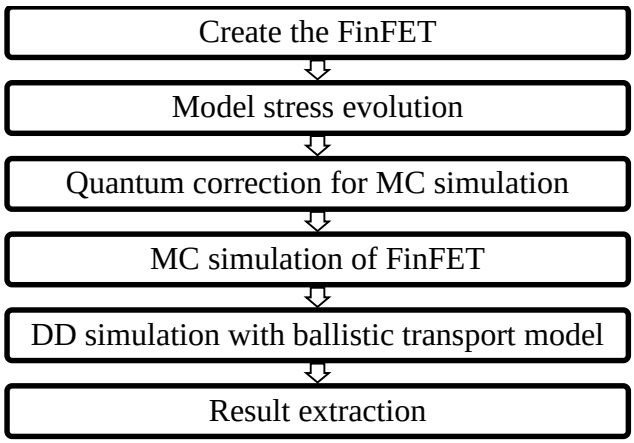


Figure 3.5: Project flow for 3D simulation of 10/7 nm node FinFET.

For 7 nm node FinFET, the impacts of different stressors, i.e. channel, SRB and S/D stressors, on the device electrical and transfer characteristics (I_d-V_g) were studied. The input parameters for the investigated device are illustrated in Figure 3.6. In this work, the stress applied to the device is varied by tampering the xmole of Ge inside each layers, by the ratio of $Si_{1-x}Ge_x$, where x is the xmole of Ge. For the SRB and S/D stressor, two types of FinFET (i.e. Ge and SiGe based FinFET) were taken into consideration. Meanwhile, to study the device behaviour at different doping concentrations, channel doping (N_{ch}) and S/D doping (N_{sd}) were varied from 10^{18} cm^{-3} to 10^{19} cm^{-3} and from 10^{18} cm^{-3} to 10^{20} cm^{-3}, respectively. Table 3.2 presents the magnitude of Ge xmole incorporated into each device types as well as the ranges of doping variations involved in simulation work. These values were the default values given by the foundry for the current technology node compatibility. Synopsys Sentaurus simulator was used to simulate the electrical characteristics of the device, in which was simulated in linear region with low drain biased of 0.05 V (V_{dlin}) and saturated region with high drain biased of 0.7 V (V_{dsat}). The simulation process was furthered by conducting a geometrical variation onto the device. Wide range of fin geometry was considered, and subsequently an optimization process is done by using statistical approach of Taguchi method, which will be discussed in the next chapter.

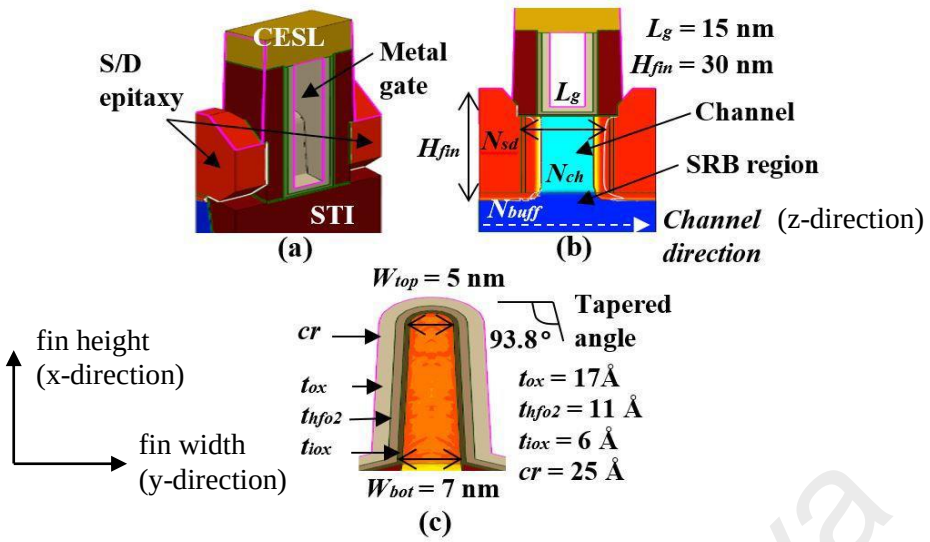


Figure 3.6: (a) Back view of the simulated 7 nm FinFET. (b) Front view of the simulated 7 nm FinFET. (c) Cross section of the device fin.

Table 3.2: Variabilities involved in simulation work.

Parameters/conditions		**Fixed**	**Ranges**
Mole fraction	Ge in channel	-	0.0, 0.5, 1.0
	Ge in SRB	SiGe: 0.5 Ge: 0.8	0.0, 0.2, 0.5, 0.8, 1.0
	Ge in S/D	n SiGe: 0.15 p SiGe: 0.85 n Ge: 0.3 p Ge: 1.0	0.0, 0.25, 0.5, 0.75, 1.0
Doping concentration	Channel, N_{ch}	10^{18} cm^{-3}	10^{18} cm^{-3} – 10^{19} cm^{-3}
	S/D, N_{sd}	10^{20} cm^{-3}	10^{18} cm^{-3} – 10^{20} cm^{-3}

For 10 nm node FinFET, the device process includes the used of mechanical stress simulation, HKMG, and *in situ* S/D doping diffusion. The impact of the top fin width (W_{top}) scaling on the electrical characteristics such as carrier sheet density (N_s) and I_d-V_g were studied. Figure 3.7 illustrates the cross section of the top fin widths, defining various values used in the simulations. While keeping other parameters constant, the width was increased from 4 nm to 8 nm, with the step size of 2 nm. In this work, the device is divided into two performance levels, that is low performance (LP) and high performance (HP) devices, by setting two different work functions (WF) to each device. Earlier research has shown high threshold dependence on the WF values (Mustafa, Bhat, & Beigh, 2013; F.

M. Rezali et al., 2016). Therefore, in this work, the WF trend is adopted such that high WF is applied to improve the p-type devices, while low WF is implemented to enhance the n-type device performances. For LP devices, the WF is set to 4.554 eV for n-FinFET and 4.473 for p-FinFET. Meanwhile for HP, the WF is set to 4.306 eV for n-FinFET and 4.713 for p-FinFET. The device is simulated in the linear and saturated region with the same biases to the 7 nm node FinFET. The channel region is doped to $1x10^{15}$ cm^{-3} while the substrate region is doped to $2x10^{18}$ cm^{-3}.

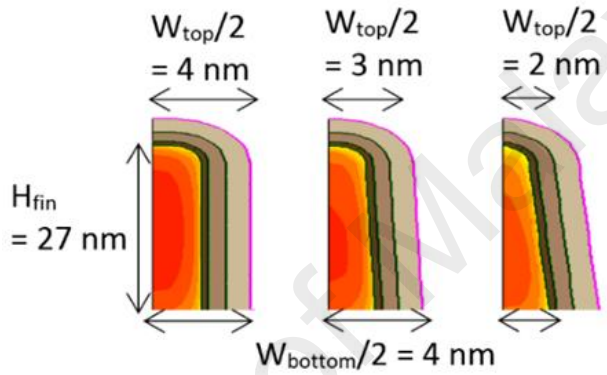


Figure 3.7: Cross section of the device fin of the simulated 10 nm FinFET.

3.5.2 HFET simulation model

2D GaN based HFET device structures are simulated through the Sentaurus Device Editor using the Synopsys Sentaurus TCAD simulator. In this work, the HFET were designed to have three different structures, which is Structure 1 (step graded $Al_xGa_{1-x}N$ barrier with different x values for each barrier layer), Structure 2 (Structure 1 with AlN spacer layer – $Al_xGa_{1-x}N$/AlN/GaN HFET), and Structure 3 (Structure 2 with InGaN channel layer – $Al_xGa_{1-x}N$/AlN/InGaN HFET) as shown in Figure 3.8. The geometrical scaling, i.e. the layer thicknesses were considered and taken into account for the final structure of GaN based HFET. The electrical properties such as 2DEG concentration and mobility, electric fields as well as carrier velocity were extracted using the Sentaurus Visual. To generate the I_d-V_g, drain voltage (V_d) of 36V was applied for all the simulations. Meanwhile for output characteristics (I_d-V_d), they were analysed at gate

voltage (V_g) at -2V and +2V. In this work, the device simulation adopts the spontaneous and piezoelectric (PE) components, which accounts for the built in polarization model, parameters taken from (Al-Mistarihi, Rjoub, & Al-Taradeh, 2013), to computes the formation of interface charges at the heterointerfaces due to the polarization divergence (Ambacher et al., 1999). Furthermore, mobility models are used in the simulation which includes the doping profiles, annealing temperature, and high field mobility-saturation dependencies.

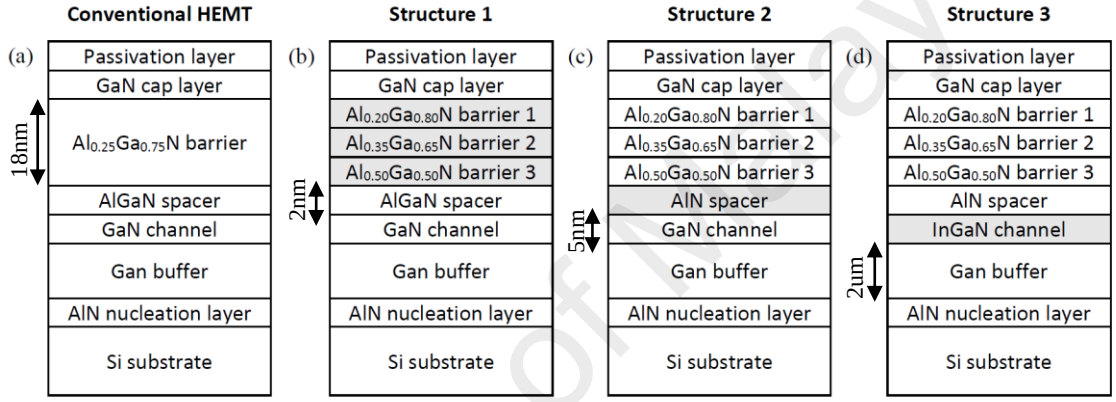


Figure 3.8: Schematic diagram of simulated GaN based HFET showing (a) conventional HFET; (b) Structure 1; (c) Structure 2; and (d) Structure 3. For conventional device: x = 0.25; Structure 1-3: $x_{1,2.3}$ = 0.2, 0.35, 0.5.

3.6 Extraction of simulation data

Sentaurus Device framework in the Synopsys Sentaurus TCAD simulator performs I–V characterization in linear and saturation region, using low and high drain biases, respectively, in which the I-V characteristic can be divided into I_d-V_g and I_d-V_d graphs. For each graph, relevant electrical parameters, such as V_t, I_{on}, I_{off}, SS, on-resistance (R_{on}), S/D resistance (R_{sd}), etc. are extracted using Sentaurus Visual. Figure 3.9 shows the basic I_d–V_g characteristic adopted in the simulation visualization (Ferain, Colinge, & Colinge, 2011).

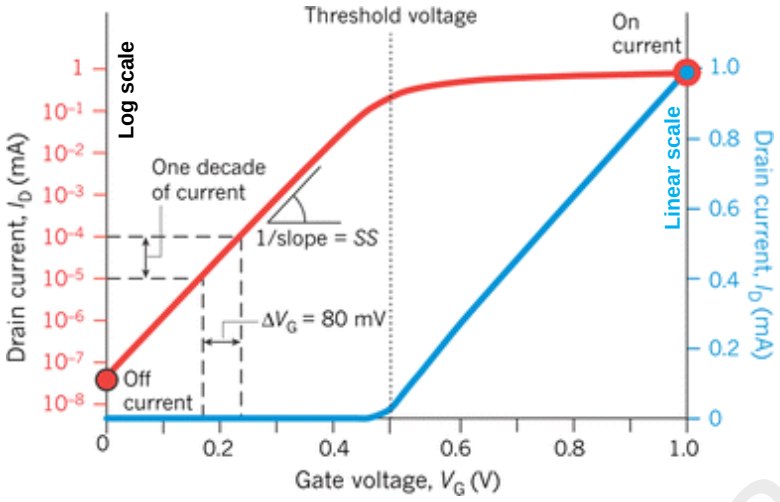


Figure 3.9: Basic I_d–V_g characteristic in a MOSFET (Ferain et al., 2011).

The most important parameters in this study are I_{on} and I_{off} values which are extracted in saturation region. The I_{on} is often called as saturation I_d, extracted at $V_g = V_{dsat}$, while I_{off} is also known as leakage currents, extracted at $V_g = 0V$. In this work, the V_t is extracted using the maximum transconductance ($g_{m\text{-}max}$) method (S. Kumar et al., 2017), extrapolated from the I_d–V_g curves, as shown in Figure 3.10. This method involves the g_m, which is calculated by differentiating the I_d–V_g curve. The V_t is extracted from the linear gradient of a point where the $g_{m\text{-}max}$ intercepting the V_g in the x-axis direction. Furthermore, DIBL and SS are also analysed in this work, such that the former is calculated as a simple change in V_t with drain bias, while the latter as the reciprocal of the slope of I_d in logarithmic scale, both to determine the short channel behaviour of the devices (Pérez-Calixto et al., 2017). Additionally, analysis on the electrical characteristics of the device can also be observed such as distribution of stresses, carrier concentrations, carrier mobility/velocity and tunnelling effects at applied bias. To support the analysis, the accuracy of the simulation data was validated with the simulation or experimental data reported from previous research as presented in the next chapter.

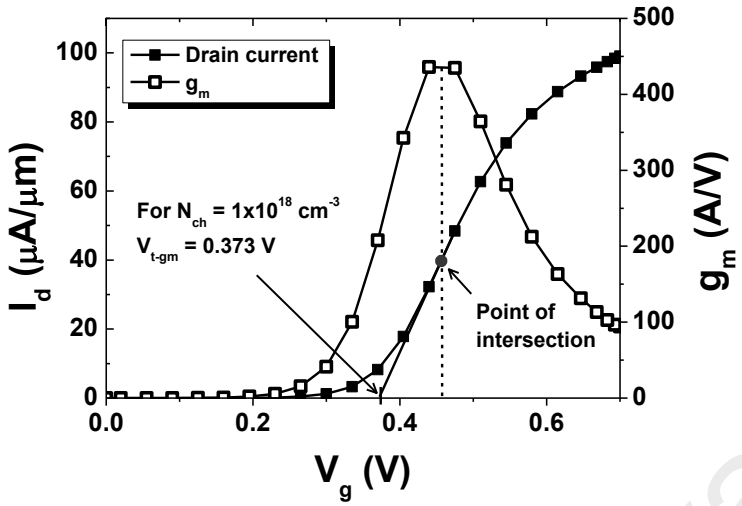


Figure 3.10: V_t extraction using the maximum transconductance ($g_{m\text{-}max}$) method.

3.7 Design of experiment (DOE)

Design of experiment (DOE) technique is a statistical manner used to make changes to the input variables of a system's output response. This technique applies a random distribution of factors. The accounted factors are chosen based on their influences on the products' performance. In this work, the chosen factors are set to be gate length (L_g), fin height (H_{fin}) and W_{top}, by which were assigned as A, B and C, respectively, as shown in Table 3.3. These factors are set at three consecutive levels, i.e. '0', '1' and '2' where '0' defines the smallest while '2' defines the largest value. On the other hand, the desired output measures are the I_{on}, I_{off} and V_t, using the LTB, STB and NTB characteristics, respectively. Standard orthogonal array (OA) with three-level used in this work is L_{27} (3^{13}) (see Appendix A). This OA is chosen as the methodology by reason of its ability of checking the interactions among factors.

Table 3.3: Space of design of experiment (DOE).

Symbol	Parameters	Level		
		0	**1**	**2**
A	Gate length, L_g	8 nm	10 nm	15 nm
B	Fin height, H_{fin}	25 nm	30 nm	35 nm
C	Top fin width, W_{top}	2 nm	5 nm	7 nm

3.8 Summary

The design structures of 10/7 nm technology SE FinFET and GaN based HFET have been identified as the investigated advanced FET devices in this chapter. Advanced physical models were implemented using Synopsys Sentaurus TCAD along with their unique design structures and processes for each type of devices. The simulations were done by considering the stress type, geometrical and process design parameters with wide range of values based on its respective technology. Each device is simulated under specific simulation conditions, and the output electrical parameters are extracted from the simulation to study the impacts of each designs. The significant effects on the device were examined in much more detail by gaining insight into the current and carrier distribution density, carrier velocity, stress distributions, as well as electric field distribution using 3D and 2D TCAD visualization. It is important to select the best parametric design within the range of process technology nodes with respect to the performance enhancement of the FET devices. Moreover, optimization analysis needs to be done carefully to evaluate the best design combination which provide the best performance.

CHAPTER 4: RESULTS AND DISCUSSIONS

4.1 Introduction

This section discussed on the findings obtained in this work. The results are divided into two parts based on different device design considerations: group IV and III-V stressor consideration on 7 nm FinFET and GaN based HFET, and geometrical and process design considerations on the SE SiGe 7/10 nm FinFET and optimized HFET. The analysis will focus on the critical electrical performance by taking into accounts the stressor and design considerations of each device. In addition, the optimization analysis using Taguchi method and analysis of variance on Ge based FinFET fin geometry was also carried out. Validation of the simulation results were carried out through comparison between this works' device performance with experimental results from other researchers.

4.2 Group IV and III-V stressor consideration

4.2.1 Analysis on 7 nm stress engineered FinFET

4.2.1.1 Channel stressor

In this section, the simulation on the 7 nm SE FinFET was done by considering the stressor with various magnitudes to examine its impact onto the electrical characteristics of the device as shown in Table 3.2. The mole fraction of Ge inside the Si channel, SRB and S/D region is varied by the ratio of $Si_{1-x}Ge_x$, where x is the mole fraction of Ge (xmole), indicating the stress applied onto the device. In this sub-section, the channel stress is varied by adjusting the mole fraction of Ge diffused inside the Si channel. This will determine the type of channel of the devices. For instances, channel with x = 0 has zero percentage of Ge inside the channel thus represents Si-based device. Same applies to when x = 1 which indicates Ge-based device, while x = 0.5 represents the SiGe-based device. Figure 4.1 shows the impacts of various Ge xmole inside the channel layer on the I_d-V_g in linear mode, while Figure 4.2 presents the characteristics in the saturation mode. It is observed that the linear I_d of n-FinFET and p-FinFET can be increased up to ~57%

and ~110%, respectively with the 50% gradual increment of Ge xmole inside the channel. It appears that the use of strain is more pronounced for holes compared to electrons considering their sensitiveness in the reduction of effective mass in higher strain, contributing to the enhancement of holes mobility (Sawano et al., 2011). For p-FinFET, the I_d are found to shift to the right as the Ge xmole is increased while for the n-FinFET to the left, suggesting the generation of defects in the channel.

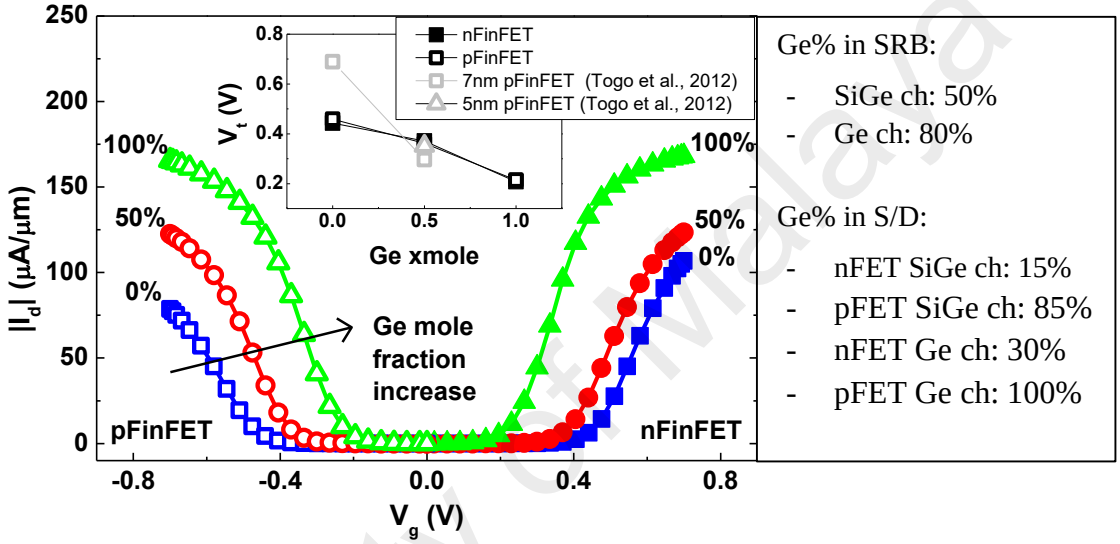


Figure 4.1: I_d-V_g for various Ge xmole in the channel at V_{dlin}. Inset is the linear V_t w.r.t Ge xmole and trend comparison with Togo et al. (2012).

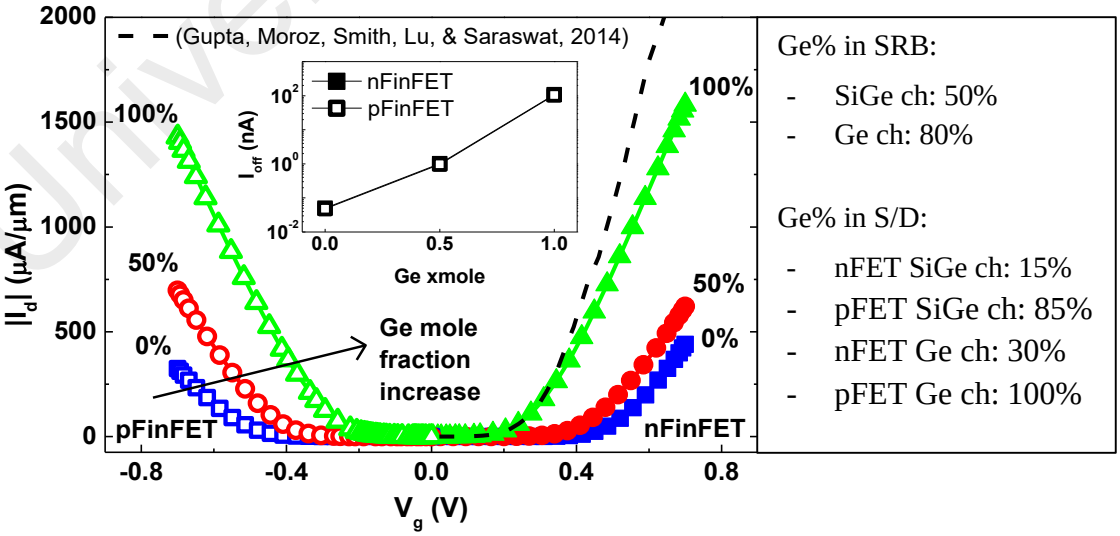


Figure 4.2: I_d-V_g for various Ge xmole in the channel at V_{dsat} and trend comparison with Gupta et al. (2014). Inset is the I_{off} w.r.t Ge xmole.

From the above figure, it is found that the I_d–V_g curves improved particularly at higher V_g as the Ge xmole increased inside the channel, due to the presence of stress at the configuration level. Higher Ge xmole inside the channel will cause the increase of strain in Si lattice and subsequently stretched in order to diffuse with Ge lattice to form SiGe compound with the ratio of $Si_{1-x}Ge_x$ (Liu & Chen, 2004). In strained Si p-type device, holes will travel in higher speed along the channel caused by the reduced R_{sd} (Nayak, Woo, Park, Wang, & MacWilliams, 1993; Welser, 1992) which also contributes to higher mobility (Niquet, Delerue, & Krzeminski, 2012) thus decreasing V_t and in turns increases the I_d in both V_{dlin} and V_{dsat}. The inset of Figure 4.1 presents that the V_t is greatly reduced with increasing xmole of Ge inside channel, potentially due to tunnelling effects. Similar trends for V_t is observed in (Sneh & Kumar, 2009; Togo et al., 2012) for higher Ge xmole devices. The tunnelling current is affected by the energy range which represents the range where the tunnelling can take place, as well as the band gap (Boucart & Ionescu, 2007; Knoch & Appenzeller, 2005). Following this event, the subthreshold leakage has shown to increase in strained Si devices, as illustrated in the inset of Figure 4.2 likely due to the electric field being higher in higher strained devices.

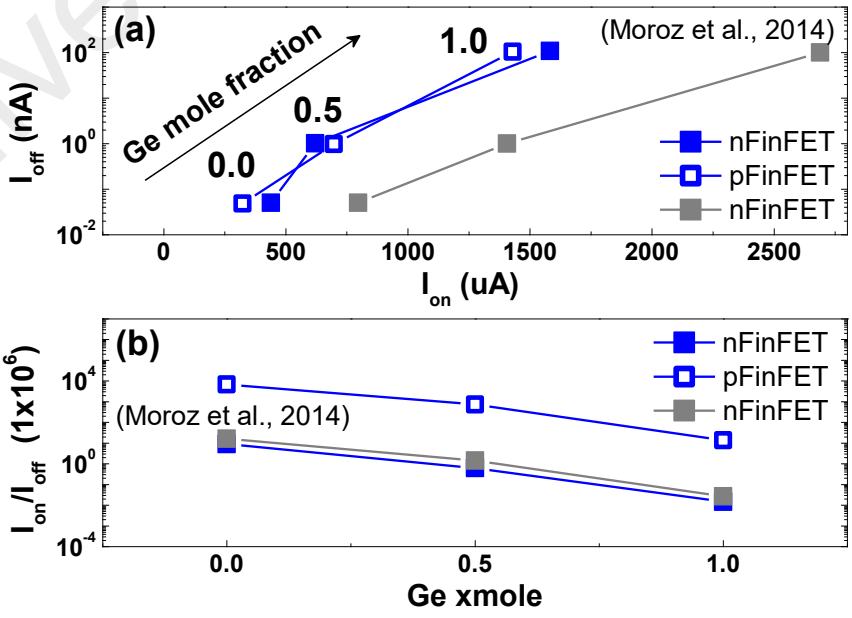


Figure 4.3: (a) I_{off} versus I_{on} graph, and (b) I_{on}/I_{off} ratio w.r.t Ge xmole in the channel at V_{dsat}. Trend is compared to that obtained in Moroz et al. (2014).

Figure 4.3 shows the I_{off} versus I_{on} graph and I_{on}/I_{off} ratio for n-FinFET and p-FinFET respectively. Observing the figure, the generation of I_{off} is noticed regardless the I_{on} enhancement contribution (Moroz et al., 2014). This suggests that the impact of channel stressor varies the device efficiency owing to several effects such as SCEs (N. A. F. Othman, Hatta, & Soin, 2016). SCEs are bound to happen in Ge based device due to different rate dopant diffusions, by which in this work to be phosphorus and boron for p-FinFET and n-FinFET, respectively. This can in turn leads to junction leakage and self-heating of the device (Jenkins & Rim, 2002). Additionally, increasing the strain can enhanced the transport of the carrier inside the channel (Sun, Thompson, & Nishida, 2007). Theoretically, the atomic force blocking the movement of electron through the channel will lessen as the Si atoms move further from each other. As a result, the velocity of the electron will boost hence enhancing the carrier transport mobility as well as the I_d. Furthermore, the influence of strain diffused into the Si band structure for p-type FET device can also be expressed in terms of density of states effective mass, modelled by Singh et al. (Singh & Kumar, 2008) expressed as below:

$$\varphi_t \ln\left(\frac{N_{v,Si}}{N_{v,s-Si}}\right) = \varphi_t \ln\left(\frac{m^*_{h,Si}}{m^*_{h,s-Si}}\right)^{3/2} \propto x \qquad \textbf{(4.1)}$$

where x is the Ge mole fraction in $Si_{1-x}Ge_x$, φ_t is thermal voltage, $N_{v,Si}$ is concentration coefficient of the valence bands in normal Si, $N_{v,s-Si}$ is concentration coefficient of the valence bands in strained Si, $m^*_{h,Si}$ is density of states holes effective mass in normal Si, and $m^*_{h,s-Si}$ is density of states holes effective mass in strained Si.

Based on Eq. 4.1, the velocity will increase due to the improved mobility and carrier transport (Takagi et al., 2008) caused by the reduced mass in strained Si as the Ge xmole increased. Interfering with xmole of Ge can affect both band gap and carrier affinity

(Weimin & Fossum, 2005). In strained Si band structure, the affinity increases while the bandgap decreases. This occurs since the edge of conduction band energy in strained Si is lower than that of normal Si, making the electron affinity to increase with a constant WF for a Si based channel with a Si/SiGe interface. On the other hand, SiGe has lower affinity than Si (Numata, Mizuno, Tezuka, Koga, & Takagi, 2005) since the edge of valence band energy becomes higher with increasing Ge xmole. Nevertheless, the SiGe interfaces reduce the conduction band off-set for SiGe devices, hence improving the carrier mobility and subsequently, will increase the carrier density inside the channel, which can be observed in Figure 4.4.

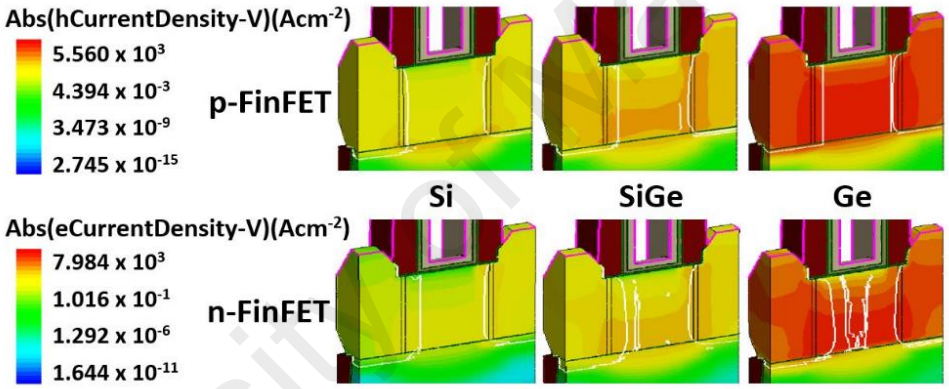


Figure 4.4: Current density distribution at V_{dsat} showing holes' density in p-FinFET and electron density in n-FinFET, respectively.

Figure 4.4 depicts the magnitude of electron and holes density for n-FinFET and p-FinFET, where the xmole of Ge inside the channel region is increased gradually from 0.0 to 1.0. The white lines in the figure represents the depletion regions at the source/channel and drain/channel junctions. From the figure, it is observed that the carrier density increases with the xmole of Ge in the channel. Moreover, the current density is found to be concentrated at the middle of the fin, due to the shape of the structure. Meanwhile, Figure 4.5 illustrates the average channel stresses in channel, width and height directions, respectively. The positive sign stress indicates that the structure exhibits tensile stress, while the negative sign stress indicates that the device exhibits compressive stress. From

Figure 4.5, it is observed that compressive stress in fin width and height (y-directions and x-directions, respectively) (refer Figure 3.6 for the directions) give rise with increasing Ge xmole in channel region.

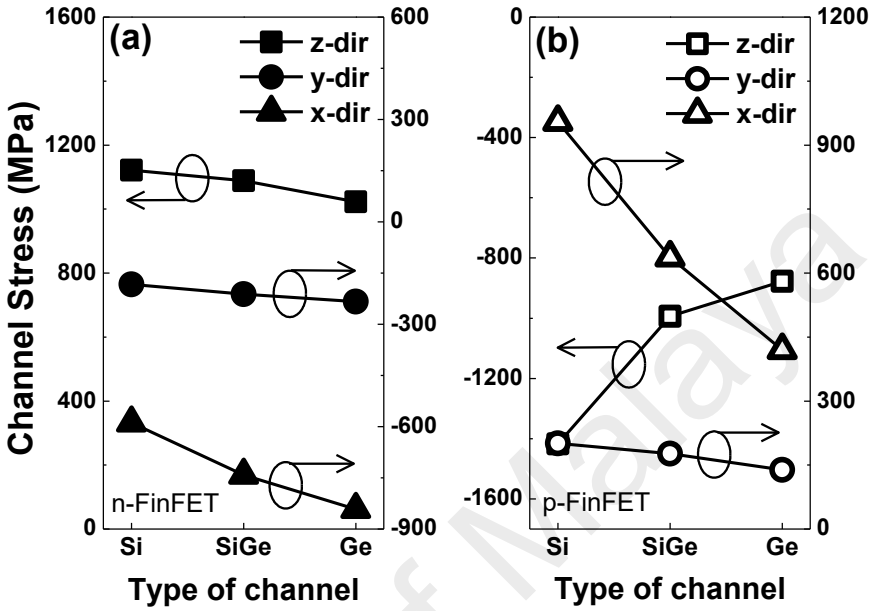


Figure 4.5: Average channel stress in channel (z-direction), fin width (y-direction) and fin height (x-direction) for (a) n-FinFET, and (b) p-FinFET.

4.2.1.2 Stress relaxed buffer (SRB) stressor

In this sub-section, the effects of SRB stress variation are studied for two different channel bases, i.e. SiGe and Ge based FinFET. Figure 4.6 illustrates the impacts of xmole of Ge variation in SRB region on the I_d-V_g of the simulated FinFET in linear mode, respectively. From Figure 4.6(a), it is observed that the rise of I_d in SiGe based devices attributes to the increasing xmole of Ge in SRB region. The I_d for 100% Ge SRB layer is improved up to ~112% in the n-FinFET, however reduced in the p-FinFET by approximately ~20% compared to the 100% Si SRB layer. This point to the fact that different stress profile is performed onto the device structure. In p-FinFET structure, the lattice mismatch between the SiGe in the channel and the S/D region as well as the SRB region reduces as the xmole of Ge inside SRB layer is increased, therefore reducing the channel strain. This is due to the band structure alteration of the device with increased

xmole og Ge hence affecting the I_d (Hemert et al., 2013; Rim et al., 2001). Eventually, this will cause the I_d to degrade, although a slight increase is observed with 100% Ge compared to 80% Ge in SRB by ~Δ1 μA/μm.

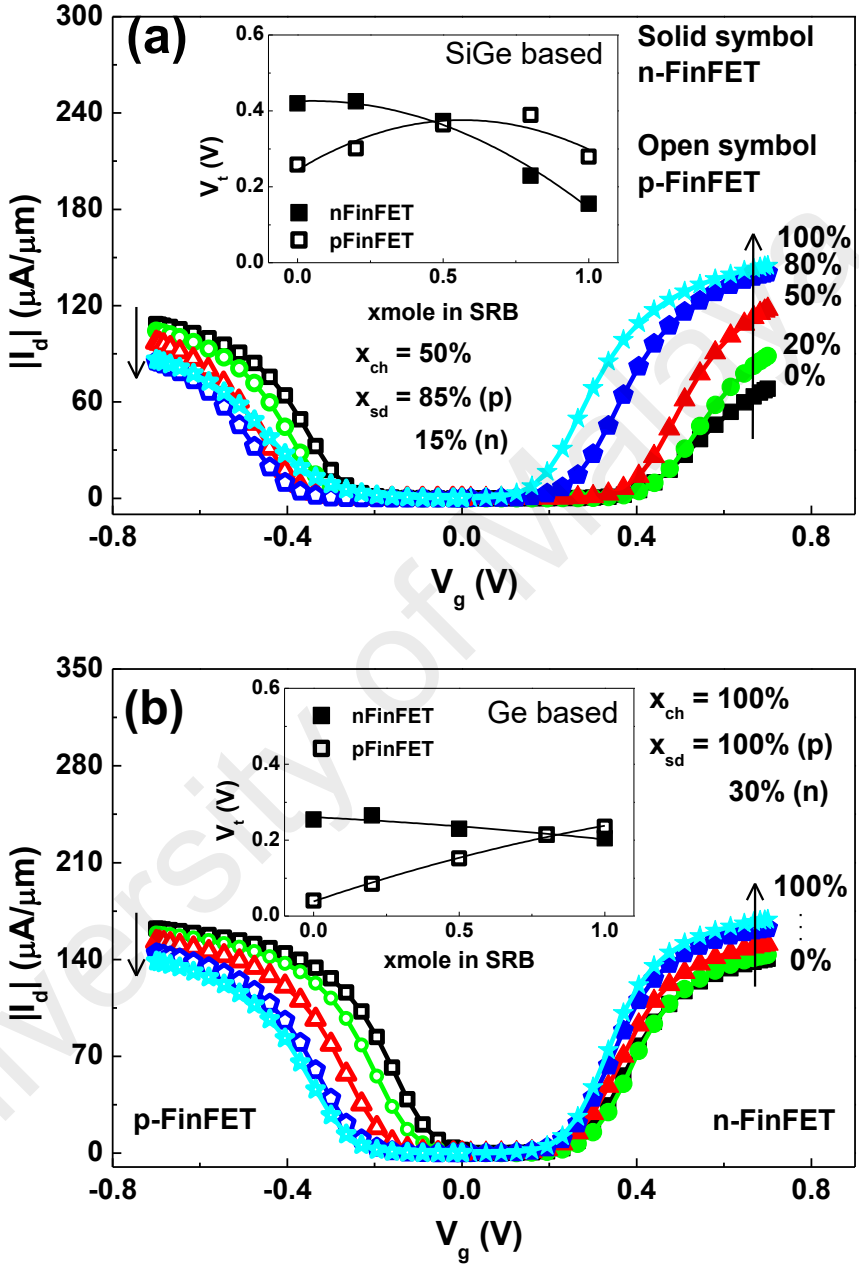


Figure 4.6: Linear I_d-V_g for various Ge xmole in SRB layer for (a) SiGe based FinFET, and (b) Ge based FinFET. Insets are the linear V_t of the devices.

For n-FinFET, the I_d is improved caused by the increase of mismatch between the interfaces, besides having the Ge xmole of in S/D epitaxy lower than that in SRB. The increase in I_d is associated to the increase in carrier velocity as illustrated in Figure 4.7.

Therefore, it is worth noting that the SiGe based FinFET design with Ge diffusion in SRB layer is advisable for the fabrication of n-type FinFET. The same trend is observed to the Ge based FinFET as the I_d increased by ~17% in n-FinFET with increasing xmole of Ge in SRB while reduced by ~15% in p-FinFET, as shown in Figure 4.6(b). Referring to Figure 4.7, it is found that the carrier velocity in Ge based channel is higher compared to SiGe, which leads to the increasing magnitude in I_d. The V_t dependencies are shown in the insets of Figure 4.6(a) and Figure 4.6(b) for SiGe based and Ge based FinFET, respectively. Reduction in V_t improves the switching speed of the device (Chen, Fan, Hu, Su, & Chuang, 2014) especially in mobile and computing applications (Natarajan et al., 2014; S. Y. Wu et al., 2013). However, this enhancement results in a trade-off to leakage generation. The leakage degradation is expected at higher electric field, particularly in the S/D region likely due to lower R_{sd} in between both regions as presented in Figure 4.8. Hence to counter this problem, further optimization process needs to be taken into considerations in contributing an efficient FinFET designs with better SCEs control.

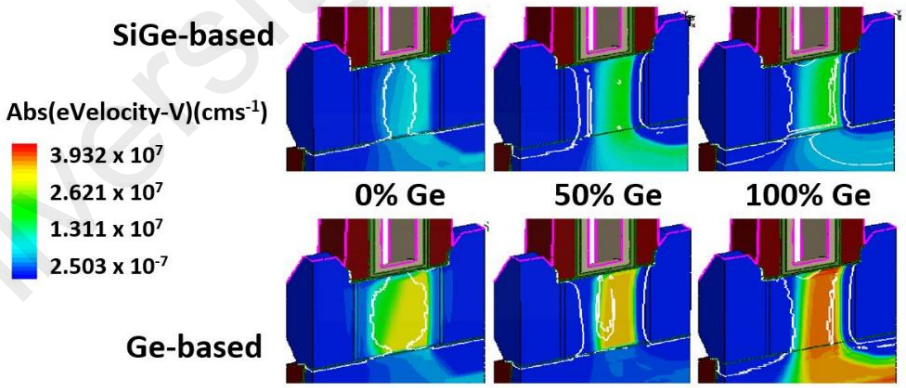


Figure 4.7: Electron velocity distribution varying Ge xmole in SRB region from 0.0 to 1.0 for SiGe based and Ge based n-FinFET at V_{dsat}.

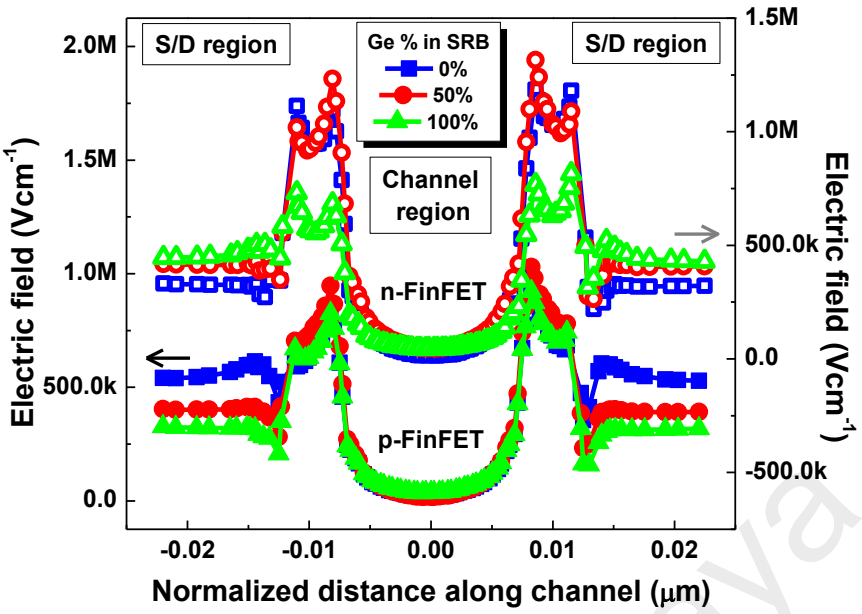


Figure 4.8: Electric field along the channel of various SRB stressor for SiGe based FinFET.

4.2.1.3 Source/Drain stressor

Figure 4.9 portrays the I_d-V_g characteristic of both SiGe and Ge based device, respectively, whereas the insets present the linear V_t as the Ge xmole in S/D epitaxial is varied from 0-100%. Compared to the results in the previous section, the I_d–V_g curves in Figure 4.9(a) shows an opposite trend where I_d reduced with increasing xmole of Ge in S/D region by ~88% from 0 to 75% for n-FinFET, while increased in p-FinFET by ~31%. For n-FinFET Ge S/D epitaxial, I_d is seen to increase back to ~Δ50 μA/μm with pure Ge S/D layer, meanwhile for p-FinFET, the current is reduced to ~Δ10 μA/μm. As mentioned before, the main factor for the I_d fluctuation is because of the alteration of the device band structure when the xmole of Ge inside the S/D epitaxial is tampered. Moreover, highly doped S/D epitaxial region will contribute to the poor performance of I_d due to mobility degradation followed by the scattering effects (Manoj, Nagpal, Varghese, & Rao, 2008; F. A. M. Rezali et al., 2016; Rousseau, Griffin, Luning, & Plummer, 1996; Wang et al., 2007). Study of inset in Figure 4.9(b) tells that the linear V_t is within the range of 168–229 mV. These values imply a weak dependency. Despite having a higher magnitude of I_{on} as the xmole Ge inside S/D is increased, the device is exposed to a quite high

subthreshold current, implying higher leakage. This indicates the reduced linear V_t as V_t shifts is influenced by series resistance and I_{off}.

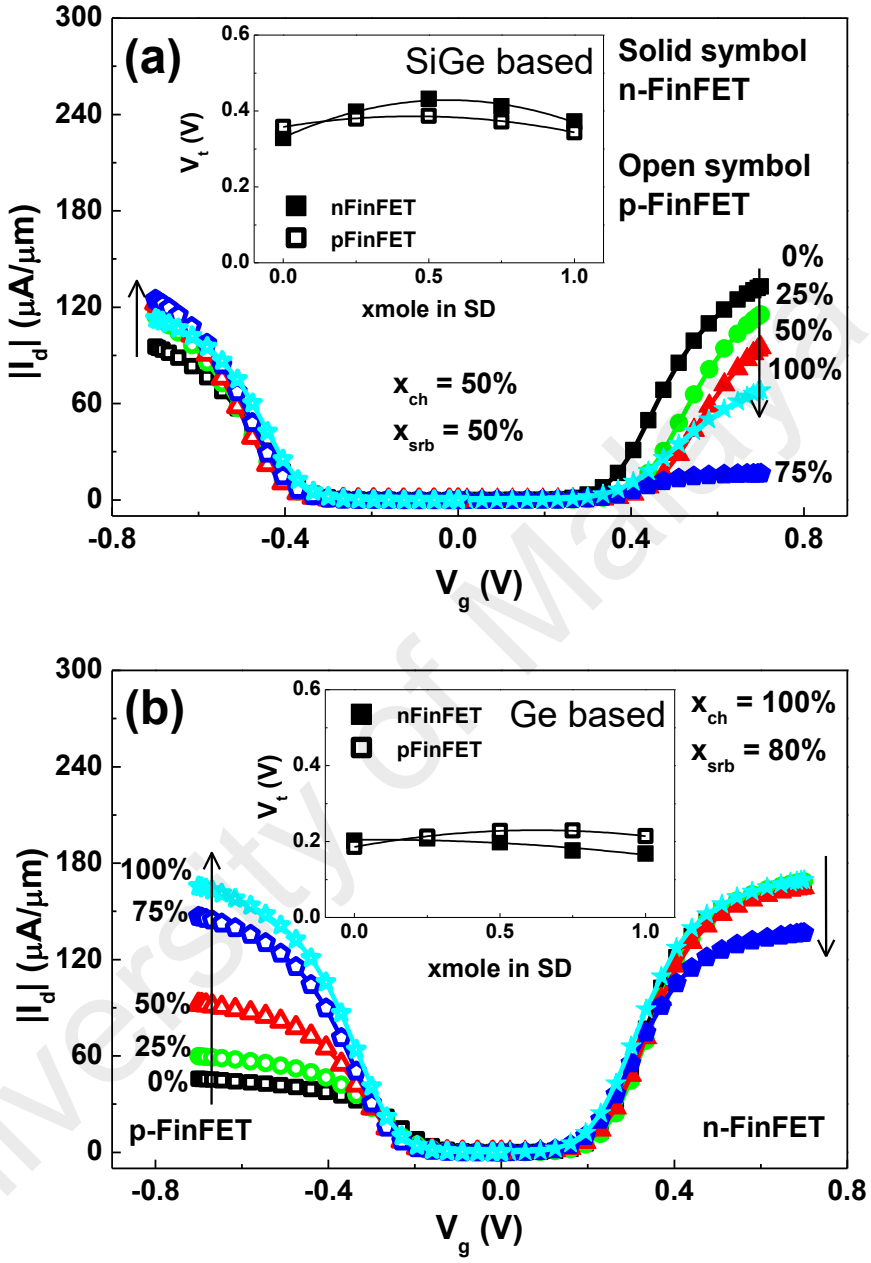


Figure 4.9: Linear I_d-V_g for various Ge xmole in S/D layer for (a) SiGe based FinFET, and (b) Ge based FinFET. Insets are the linear V_t of the devices.

Figure 4.10 presents the hole current density distributions of p-FinFET inside the devices' fin. Note that the leakage occurs at the centre of the fin, due to its tapered shaped. The current density is higher for pure Si S/D epitaxial compared to SiGe and pure Ge S/D

layer designs. This is expected since the carrier velocity at the S/D region is slowed down, hence concentrating the carrier inside that particular region as shown in Figure 4.11.

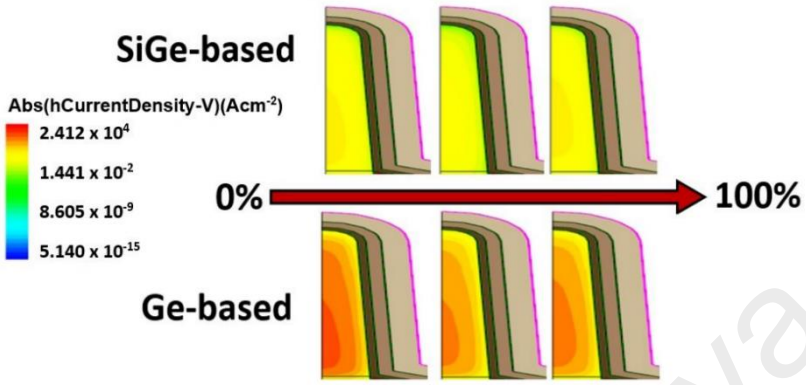


Figure 4.10: Current density distribution in SiGe and Ge based p-FinFET.

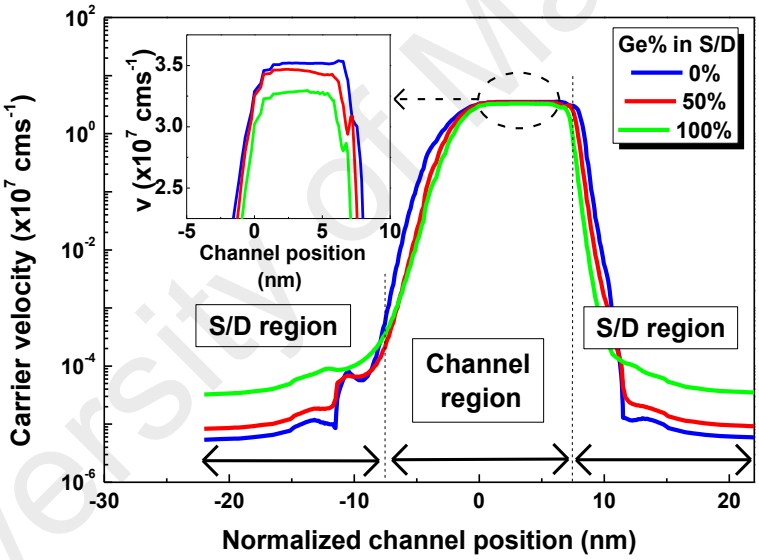


Figure 4.11: Carrier velocity along the channel w. r. t. S/D stressor. Inset is the closer visual at the curve peak.

Apart from that, as seen in Figure 4.12, the device with higher xmole of Ge in S/D epitaxial produce higher mobility across the range of the effective electric field (H. Cho et al., 2016). At low field, the hole transport is primarily dominated by the device with Ge diffused S/D region. The effect of strain inside the S/D region attributes to the increase in sub-bands separation in the conduction band, assuming the inter-valley phonon scattering rate is reduced (Leitz et al., 2001). Subsequently, the inter-valley scattering

reduction together with reduced effective mass will increase the carrier mobility, hence enhancing the device performance (Gámiz & Godoy, 2008).

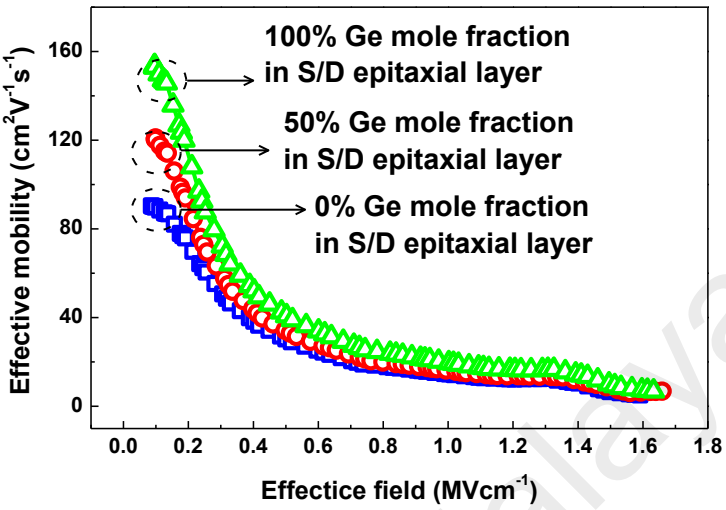


Figure 4.12: Effective mobility against field for various Ge xmole in S/D layer for Ge n-FinFET.

The impact on the DIBL are shown in Figure 4.13. As shown in the figure, notice that the n-FinFET has better DIBL characteristics compared to the p-FinFET in SRB stressor, especially in SiGe channel FinFET, thus confirmed the current variations are higher in n-FinFET compared to p-FinFET. Oppositely for S/D stressor, the current variations for p-FinFET is found to be higher compared to n-FinFET, indicating that holes undergo better control of the gate with S/D stressor variation than electrons, as illustrated in Figure 4.9(b). From Figure 4.13, it is found that Ge SRB layer has the highest value of DIBL for all different channel bases, by which has also recorded to have highest I_{off}, as reported in Figure 4.14. Despite having the highest I_{off}, the improvement in I_{on} is also treated as important in sub-nanometre transistor design.

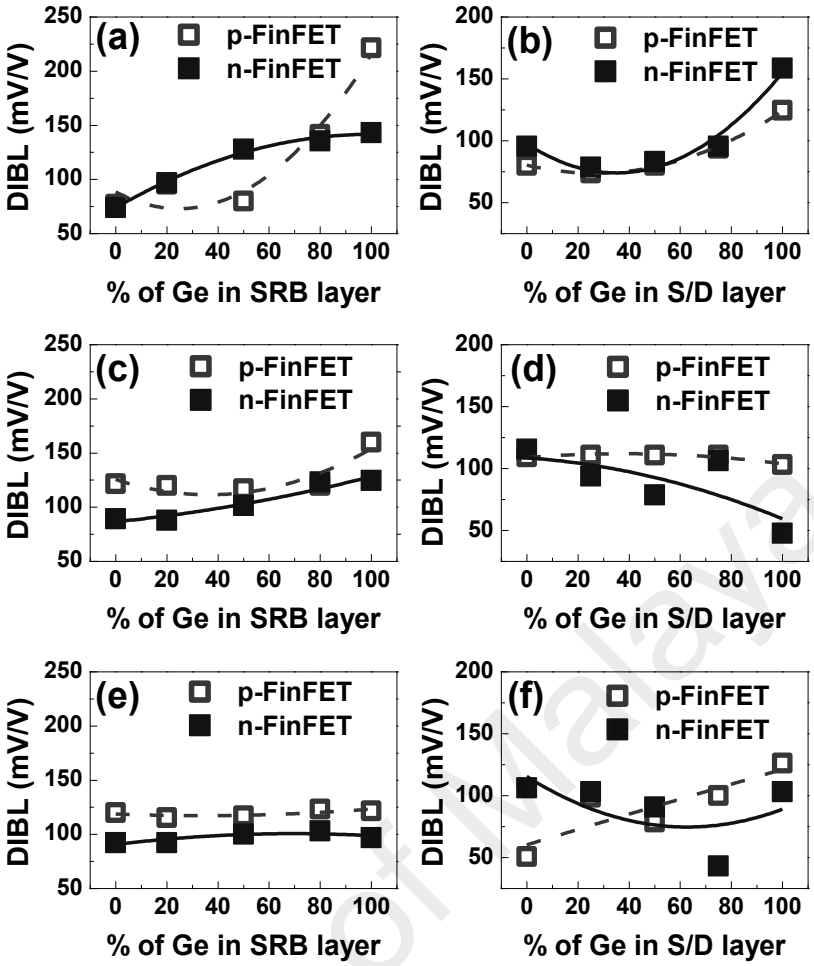


Figure 4.13: DIBL characteristics for Si based with (a) SRB stressor and (b) S/D stressor, SiGe based with (c) SRB stressor and (d) S/D stressor, and Ge based with (e) SRB stressor and (f) S/D stressor.

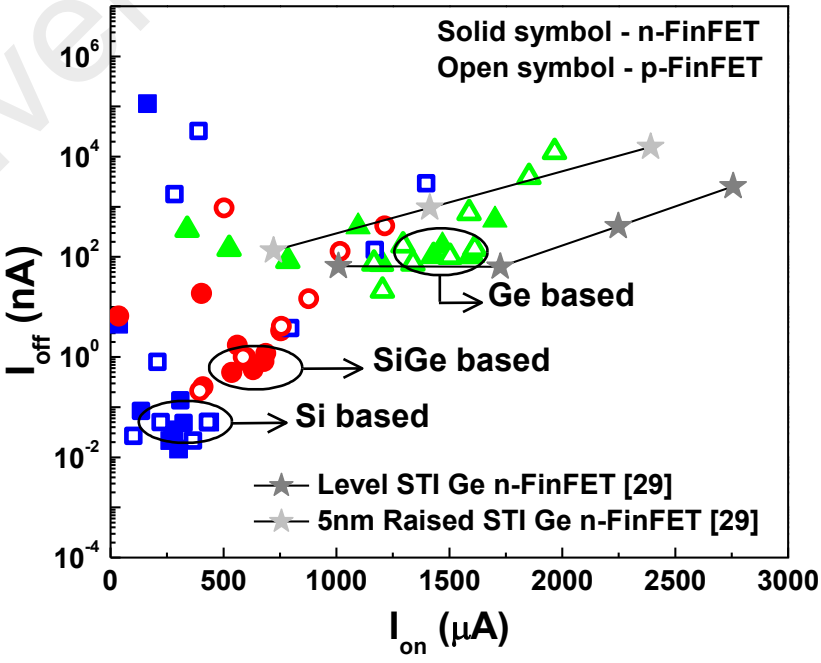


Figure 4.14: I_{off} versus I_{on} for SRB and S/D stressor at V_{dsat}.

4.2.2 Analysis on GaN based HFET

4.2.2.1 Step graded AlGaN barrier layer

In this work, a step graded AlGaN barrier is used to improve the design performance and is compared to the conventional AlGaN HFET. Figure 4.15 illustrates the DC I_d-V_d at V_g = -2 V and +2 V for step graded AlGaN barrier (Structure 1) with different xmole of Al in each barrier layer compared to the conventional type. The I_d-V_d curves show improvement for the graded barrier with reduced Al xmole compared to conventional device. It is observed that the peak current density can achieve up to 2.7 A/mm which increases by 30% compared to conventional HFET at V_g = +2V.

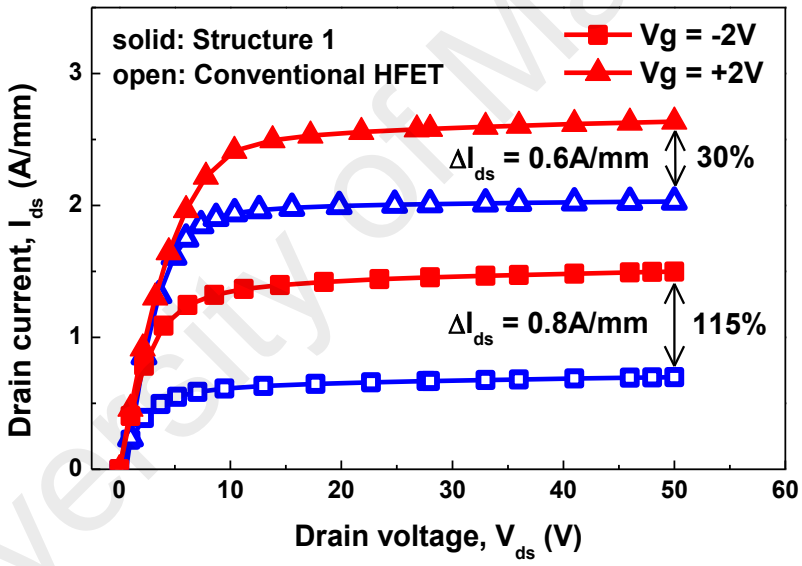


Figure 4.15: I_d-V_d at V_g = -2 V and +2 V for conventional and graded AlGaN barrier HFET (Structure 1).

In addition, the I_d-V_g are illustrated in Figure 4.16 while the simulated result of the DC transfer for all structure is tabulated in Table 4.1. From Figure 4.16, the I_d-V_g is improved with the current density increasing by 0.65 A/mm when the barrier is graded, with maximum I_d achieved is 2.7 A/mm. This behaviour is compatible with the earlier findings on AlGaN/GaN HS electrical properties and is related to the presence of 2DEG in the channel (Das et al., 2014; Zhi-Yong et al., 2007). The 2DEG can be induced to increase

as the Al content in the device barrier which results in larger conduction-band discontinuity. This phenomenon will also enhance the PE polarization effect as shown in Figure 4.17, improving 2DEG sheet density in the channel region. From Figure 4.17, the enhancement of PE polarization density can be clearly observed as the Al content increase gradually compared to conventional HFET.

Table 4.1: Simulated results of DC characteristics for all structures.

HFET structures	Figure of Merits (FOMs)				
	$\|V_t\|$ (V)	$\|I_{on}\|$ (A/mm)	$\|I_{off}\|$ (A/mm)	R_{on} (mΩ)	R_{out} (mΩ)
Conventional	3.509	1.944	1.175	2.588	616.2
Structure 1	6.208	3.288	2.659	2.294	226.8
Structure 3	8.368	4.014	3.410	2.219	40.19
Structure 3	8.415	4.035	3.505	2.202	38.69

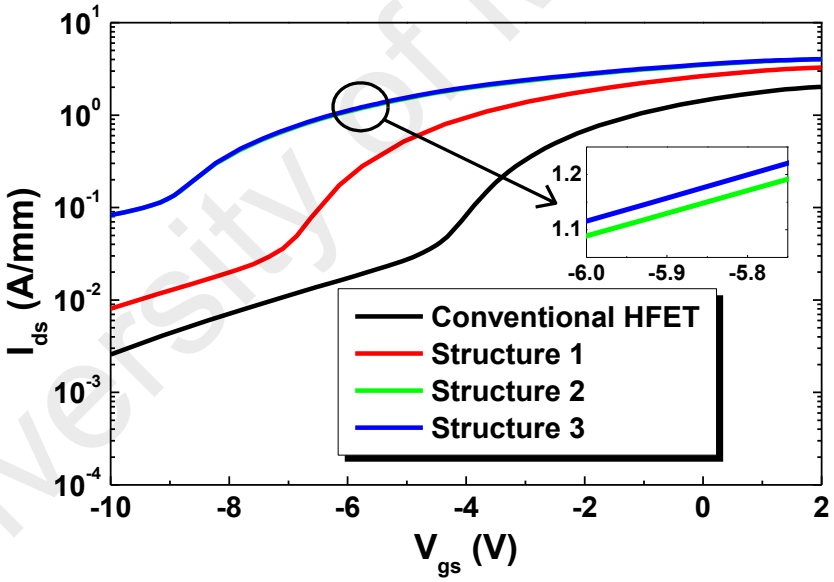


Figure 4.16: I_d-V_g characteristics at V_d = 36 V in logarithmic scale.

Moreover, the polarization density is also affected by the lattice mismatch between Al and GaN compound, which leads to higher electron density at AlGaN/GaN interfaces (Ambacher et al., 1999). Despite that, step-grading AlGaN barrier structure can greatly overcome current collapse due to the screening of surface traps at the lower part of the widened channel (Zhou et al., 2015). Since the barrier is graded, there are large numbers

of electron mobiles inside the barrier making the device immune to the surface trapping effects, therefore results in smaller current collapse.

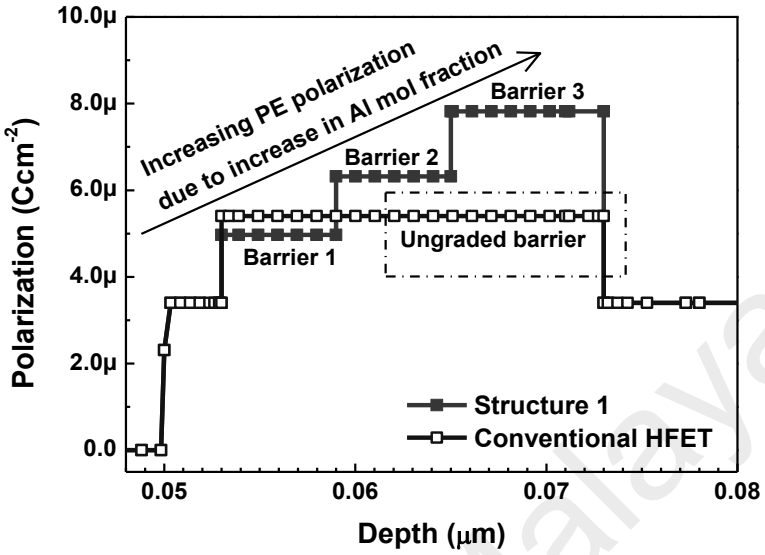


Figure 4.17: PE polarization density, ΔP (Ccm^{-2}) with respect to device depth (μm).

In addition, study of Figure 4.18 has shown major improvement of 2DEG density at the channel region, by which the maximum magnitude can be achieved up to 1.66x10^{18} cm^{-3} for Structure 1 with graded barrier structure compared to conventional HFET with density of 0.39x10^{3} cm^{-3}. However, extremely high content of Al inside the device barrier will eventually degrades the crystal quality of the interface, thus reducing electron mobility (Das et al., 2014). Figure 4.19 depicts the electron mobility as well as total current density comparing Structure 1 and Structure 2 to the conventional HFET. From the figure, it is observed that the electron mobility is decreased particularly at the gate area for graded barrier of Structure 1 compared to conventional HFET. Earlier work (Lu, Kumar, Piner, & Adesida, 2003; Miyoshi et al., 2004) has shown the dependence of electron mobility on the Al content in the barrier, which reduced as Al xmole increase. Apparently, reduction in mobility is caused by the differences in scattering factors when the barrier is graded. These happen when the percentage of Al dopant inside each barrier is decreased.

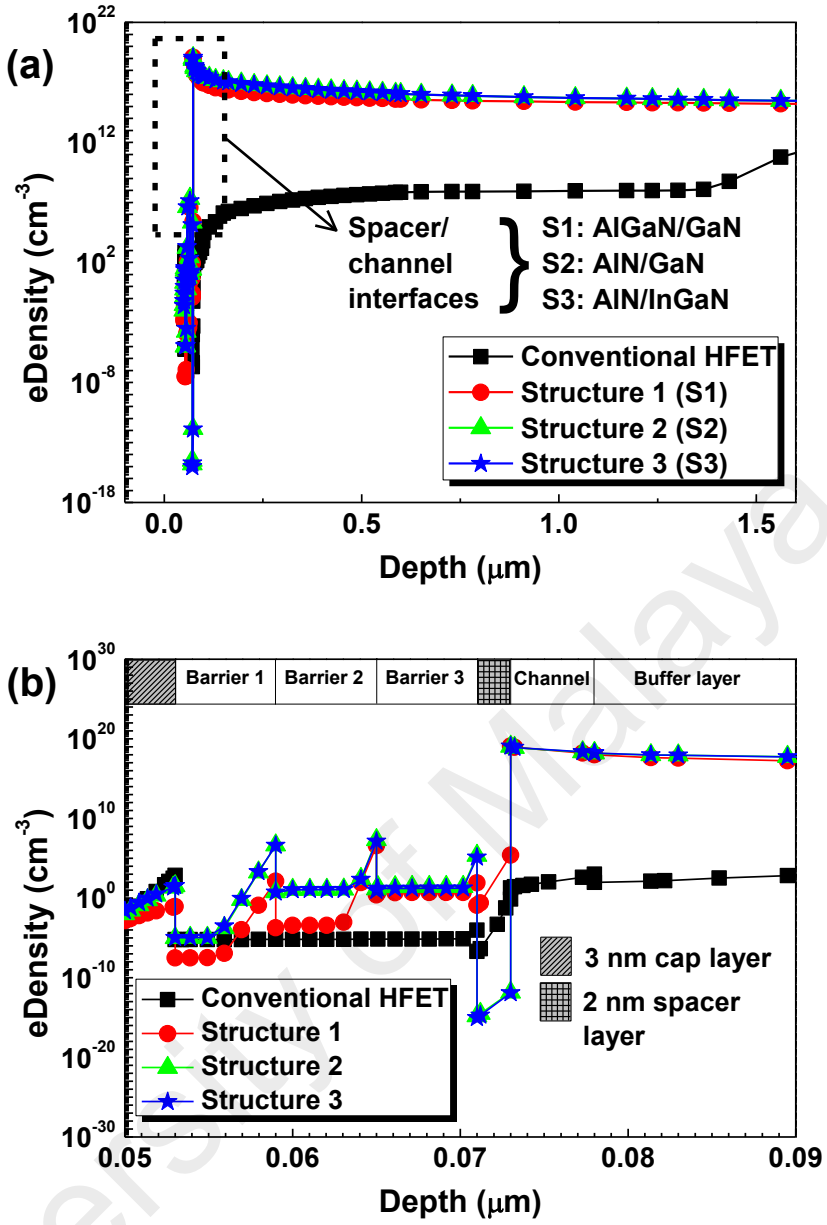


Figure 4.18: (a) Graph of electron density (cm^{-3}) for conventional HFET and Structure 1-3 along device depth (μm). (b) Closer visual focusing on the density at the interfaces from the depth of 0.05 μm to 0.09 μm.

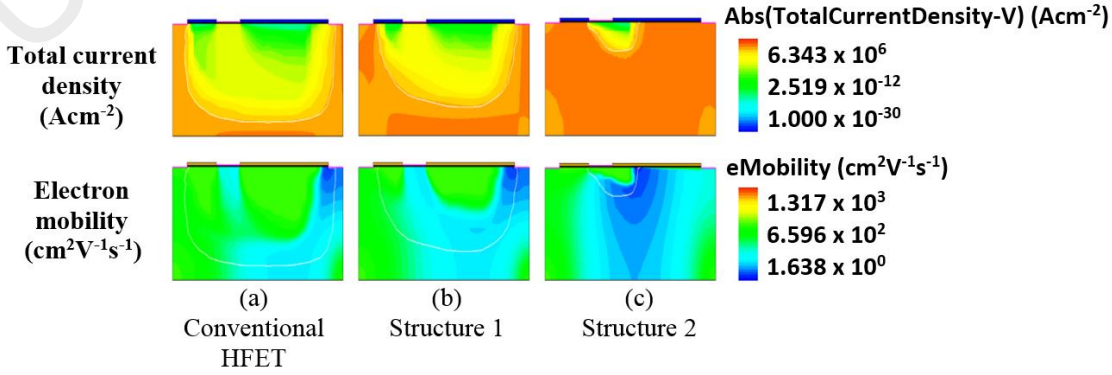


Figure 4.19: Total current density and electron mobility for (a) conventional HFET, (b) Structure 1, and (c) Structure 2.

Apart from that, the total current density is greater for graded barrier structure particularly at the source, gate and drain region. From the figure, it is worth mentioning that the device leakage is potentially higher for graded barrier structure by observing the total current density due to higher electric field (F. A. M. Rezali et al., 2016) at the AlGaN/GaN interface as shown in Figure 4.20. The peak electric fields according to Figure 4.20(b) for Structure 1 is 9.22 $x10^6$ Vcm^{-1} which is higher compared to conventional HFET at $4.87x10^6$ Vcm^{-1}.

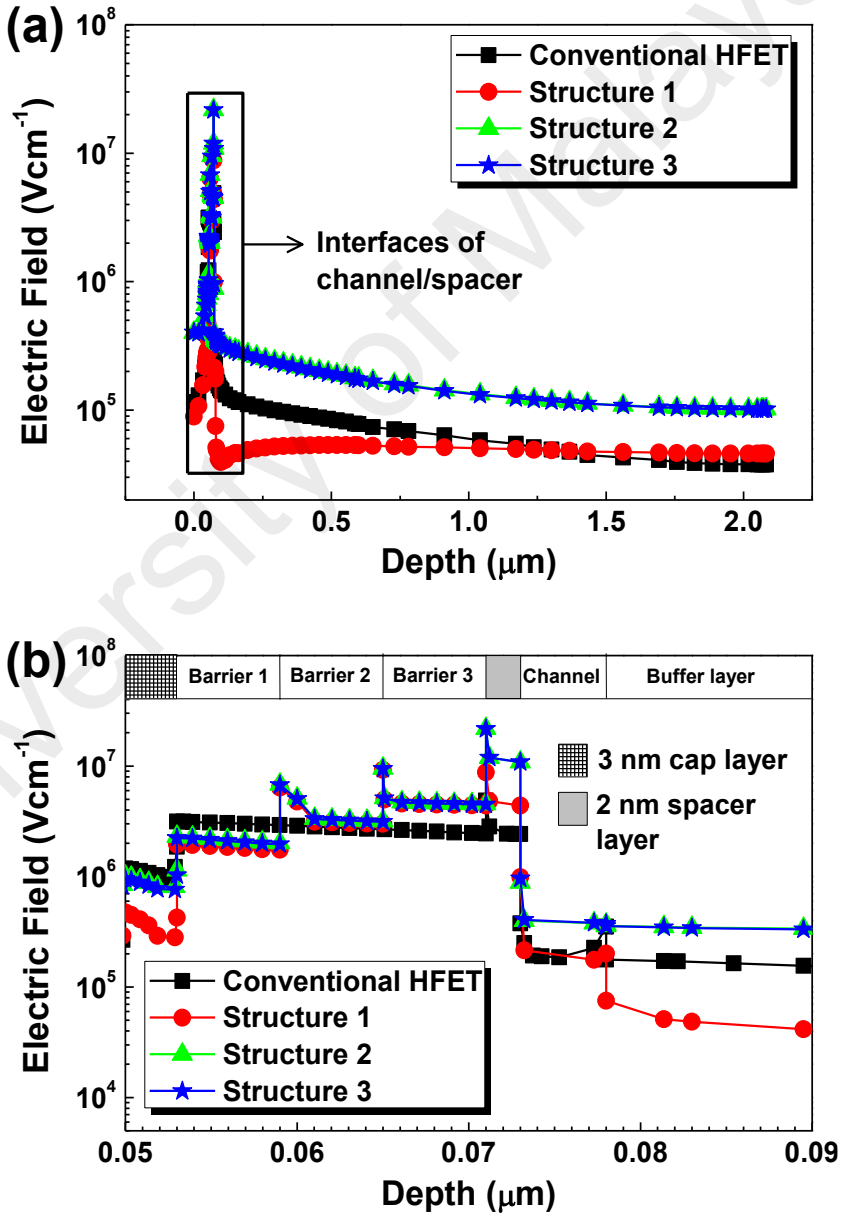


Figure 4.20: (a) Graph of electric field (Vcm^{-1}) for conventional HFET and Structure 1-3 along device depth (μm). (b) Closer visual focusing on the field at the interfaces from the depth of 0.05 μm to 0.09 μm.

4.2.2.2 AlN interfacial/spacer layer

The use of AlN spacer layer at the interface of AlGaN barrier and GaN channel has been broadly studied. It is reported that the implementation of AlN can reduces the strain along the interfaces (Shrestha, Wang, Li, & Chang, 2013) while improving the lattice of AlGaN barrier layer. In this sub-section, the insertion of AlN spacer layer at the AlGaN/GaN interfaces in Structure 2 is to improve the electron mobility from the previous designs. From the observations, the results show encouraging improvement compared to previous structure. The I_d-V_d curves in Figure 4.21 shows improvement as it increases tremendously as compared to Structure 1.

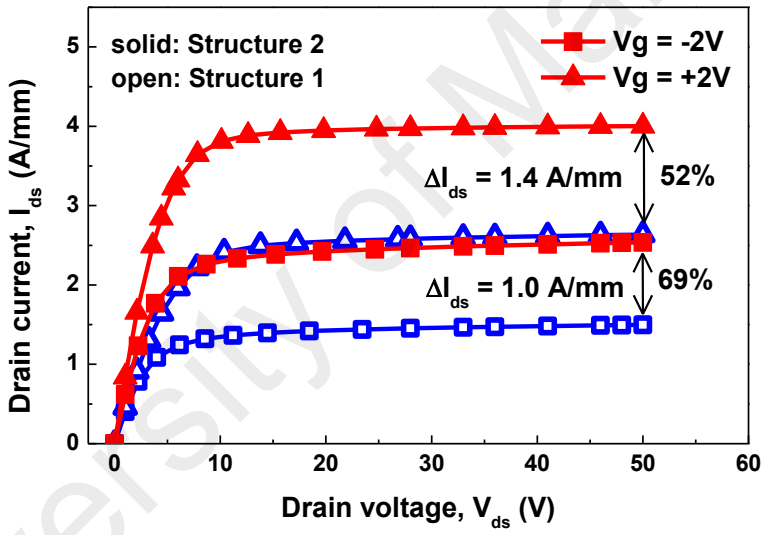


Figure 4.21: I_d-V_d at V_g = -2 V and +2 V for graded AlGaN barrier HFET (Structure 1) and AlN spacer HFET (Structure 2).

Study from Figure 4.21 shows the peak current density for graded barrier of Structure 2 can achieve up to 4.02 A/mm which increases by 52% compared to Structure 1 at V_g = +2 V. Same trend is observed in I_d-V_g in Figure 4.22 which indicates improvement with the insertion of AlN spacer layer at the heterointerfaces. This behaviour is strongly related to the increment of mobility caused by the lowering of alloy scattering (Roy et al., 2015; Shrestha et al., 2013). Unmistakably, improvement in electron density and mobility is owed to the higher quantum well depth which in turns lowered the alloy scattering with

the implementation of binary compound such as AlN (Jena, Smorchkova, Gossard, & Mishra, 2001).

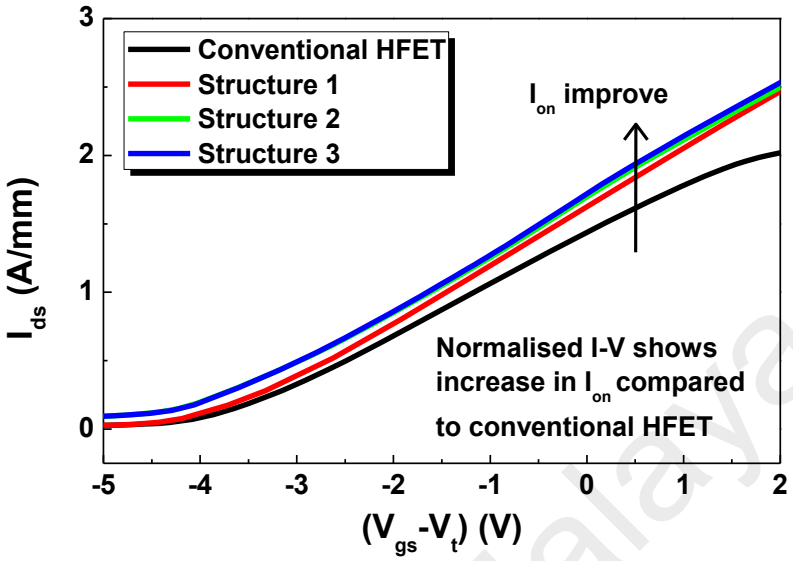


Figure 4.22: Graph of normalised I_{ds} versus (V_g-V_t) curves for all structures.

The main reason AlN material is introduced as the interfacial layer is to enhance the mobility thus indirectly electron concentration as well at low temperature. The concentration inside the channel layer is increased to 2.2×10^{18} cm^{-3} in Structure 2 and is shown in Figure 4.18(b). Apparently, AlN spacer layer gives an impact to the carrier transport and enhancing the carrier confinement (Shrestha et al., 2014). The potential differences across the spacer layer produces larger effective conduction band offset, owing to the polarization field (Keller et al., 2002) as shown in Eq. 4.2 (Lenka & Panda, 2011):

$$\Delta E_c^2 - \Delta E_c^1 = \exp\left(\frac{\sigma_2 - N_{2D}}{\varepsilon_2}\right) t_b \qquad \textbf{(4.2)}$$

where ΔE_c^2 is the conduction band offsets between the interfaces in Structure 2, ΔE_c^1 is the conduction band offsets between the interfaces in Structure 1, N_{2D} is the sheet carrier concentration of the Structure 2, ε_2 is the dielectric constant, σ_2 is the polarization induced charge at the interfaces of Structure 2, and t_b is the thickness of barrier. Besides that, the

effective Schottky barrier of the quaternary structure will increase with the presence of AlN spacer barrier, which eventually reducing the devices' leakage (Brazzini et al., 2013).

Study of Figure 4.19(c) tells that with the insertion of AlN interfacial layer at the AlGaN/GaN heterointerfaces, the magnitude of electron mobility is encouragingly improved particularly below the gate region. From the result obtained, the electron mobility is increased from $1.1x10^3$ $cm^2V^{-1}s^{-1}$ in Structure 1 to $1.3x10^3$ $cm^2V^{-1}s^{-1}$ in Structure 2. As mentioned earlier, raised in mobility is highly related to the reduction of alloy scattering with the presence of AlN as the spacer layer (Shrestha et al., 2014). In fact, insertion of AlN spacer layer can also reduce the forward Schottky gate current, thus enabling high gate voltage application for transistor operation. By combining the design structure of step-grading AlGaN barrier and insertion of AlN interfacial spacer layer at the heterointerfaces, the device performance has improved significantly. A high quality of AlGaN/AlN/GaN HFET with uniform structure is acquired with an improved electron mobility as well as surface lattice arrangements as compared to the conventional structure. However, for graded structure, the total strain inside the barrier will decrease due to reduction in lattice mismatch between AlGaN and AlN configurations, hence reducing lattice strain. Despite having low strain inside the layer, significant improvements can be observed in terms of 2DEG concentrations and electron mobility for step graded structure device incorporated with AlN spacer layer in between AlGaN and GaN interfaces. Besides that, observation in the contour on total current density in Figure 4.19(c) indicates that there is essential reduction in the current density at below the gate region. As mentioned earlier, this effect will lead to reduction in channel as well as buffer leakages, which may also due to reduction in electric field as shown in Figure 4.20. Despite having higher electric field at the spacer/channel interfaces, Structure 2 has higher drop ranges of electric field compared to Structure 1. The electric field drops in about $9.8x10^6$ Vcm^{-1} at the spacer and channel interfaces for Structure 2 compared to Structure 1 with $3.38x10^6$

Vcm^{-1}. Figure 4.23 illustrates the electron velocity of Structure 1-3 compared to the conventional HFET.

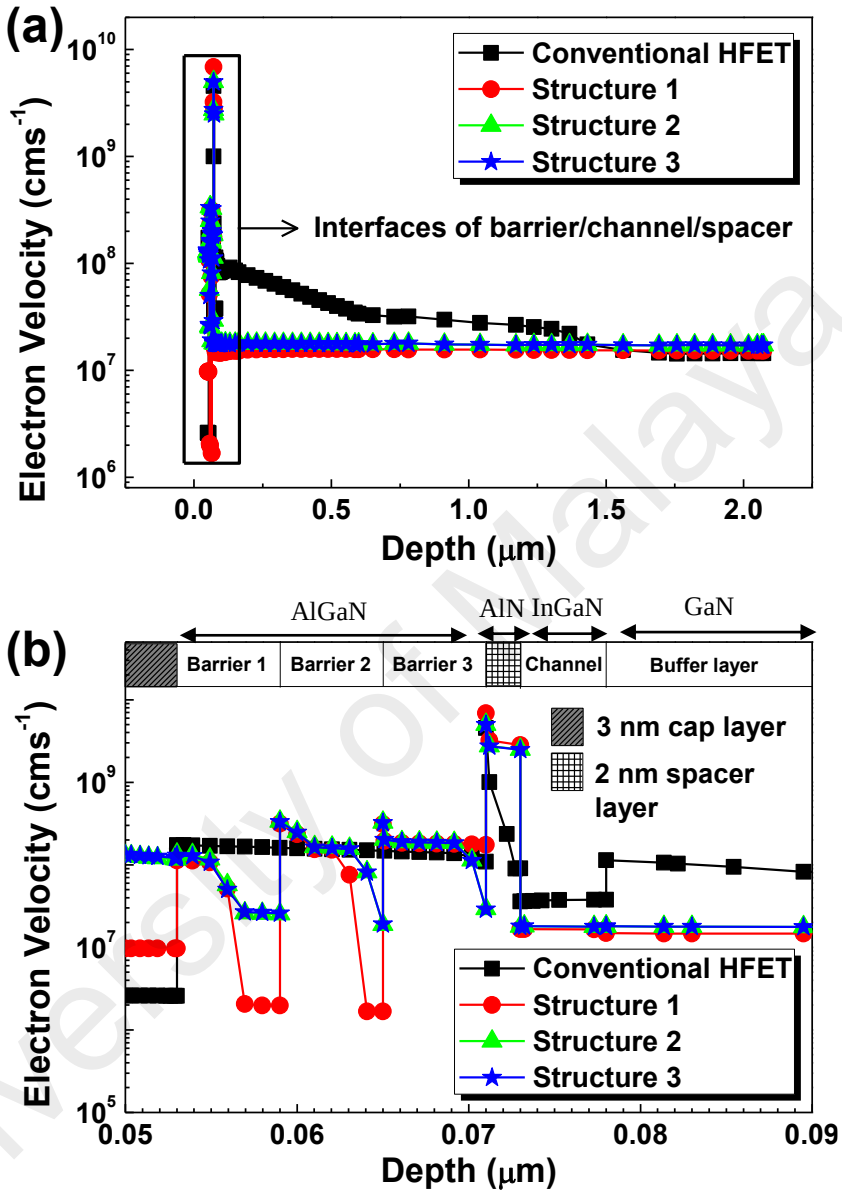


Figure 4.23: (a) Graph of electron velocity (cms^{-1}) for conventional HFET and Structure 1-3 along device depth (μm). (b) Closer visual focusing on the velocity at the interfaces from the depth of 0.05 μm to 0.09 μm.

The result is found to be promising for Structure 1 as the carrier have accelerated at the AlGaN and GaN interfaces compared to conventional design from 9.04x10^{7} cms^{-1} to 2.82x10^{9} cms^{-1}. However, the magnitude dropped in channel region to 1.66x10^{7} cms^{-1} as well as in buffer region to 1.49x10^{7} cms^{-1}. This improvement can lead to higher cut-off

frequency and better RF improvement. On the contrary in Structure 2, the velocity is at the same magnitude level at the interfaces and lower in channel region compared to previous design although it increases towards the bottom of the buffer region from $1.46x10^7$ cms^{-1} to $1.72x10^7$ cms^{-1}.

4.2.2.3 InGaN channel layer

InGaN compound has been widely used as the channel material due to their lower band gap, which can enhance the high frequency characteristics and to prevent current collapse (Lenka et al., 2013; Y.-C. Zhang et al., 2015; Y. Zhang et al., 2016). In this part, the structure design is slightly improved, where the GaN channel is replaced to InGaN compound. It is observed that the output DC characteristics for Structure 3 in Figure 4.24 has shown slight improvement by which the current is increased by 2% at V_g = -2 V compared to the previous design (Structure 2). The inset of Figure 4.16 illustrates the similar trend of I_d-V_g for Structure 3 compared to Structure 2. Narrower band gap in InGaN channel device will increase the quantum well depth. Studying the carrier density behaviour in Figure 4.18, the results shows that the carrier density at the spacer/channel interface for Structure 3 is slightly higher compared to Structure 2. This is because implementing InGaN channel can improve the carrier confinement in the channel layer. This behaviour has proven the fact that InGaN channel device is better in extinguishing the 1/f noise as well as RF current collapse.

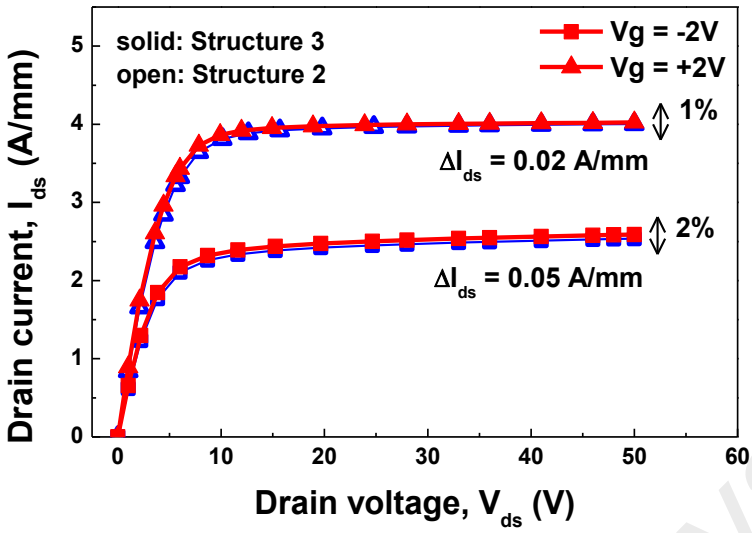


Figure 4.24: I_d-V_d at V_g = -2 V and +2 V for AlN spacer HFET (Structure 2) and InGaN channel HFET (Structure 3).

Apart from that, InGaN is also well-known with their relatively low electron effective mass, hence leads to higher carrier velocity. Figure 4.23 shows the electron velocity of the device for Structure 3. From the figure, the carrier transport in Structure 3 is higher compared to Structure 2, where the velocity is increased by 13.9×10^3 cms^{-1}. This is expected due to the fact that carriers in InGaN are causing the velocity to increase, thus increasing the cut-off frequency for high performance devices. The interface between InGaN channel layer and GaN buffer layer will produce compressive strain in the channel. This will reduce the buffer leakage and can leads to improve 2DEG mobility. The PE polarization in the InGaN layer is opposite to AlGaN layer, which will result in increase of the conduction band below the channel thus reduce the SCEs as well as buffer leakage current.

4.3 Geometric and process designs consideration

4.3.1 Effects of fin geometrical scaling on FinFET

4.3.1.1 Analysis on 10 nm stress engineered SiGe FinFET

Figure 4.25 presents the effect of W_{top} variations on the hole and electron sheet density of p-FinFET and n-FinFET, respectively, for LP and HP devices, by which is simulated

at different WF. For LP devices, the WF is set to 4.554 eV for n-FinFET and 4.473 for p-FinFET. Meanwhile for HP, the WF is set to 4.306 eV for n-FinFET and 4.713 for p-FinFET.

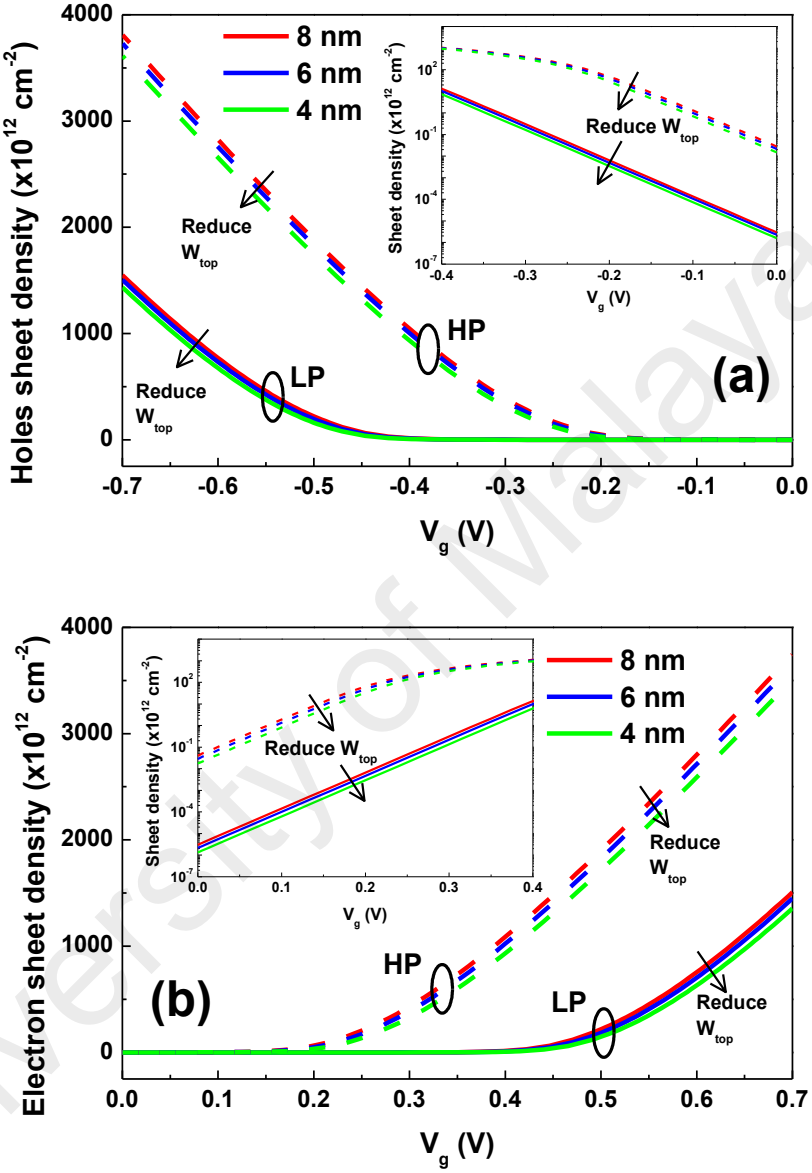


Figure 4.25: Graph of (a) hole sheet density of p-FinFET, and (b) electron sheet density of n-FinFET for LP and HP devices at various W_{top}.

From Figure 4.25, it is found that the sheet density is slightly reduced with reduced W_{top}. This is expected due to the fact that resistance is lower in wider the fin (F. A. M. Rezali et al., 2016). Hence, the carrier sheet is expected to be denser with wider width compared to narrower width. The results show that the density for HP devices are higher compared to LP devices by approximately ~2.6x10^{15} cm^{-2}. These trends are adapted to

both electron and holes density of n-FinFET and p-FinFET, respectively. For both LP and HP devices, the electron sheet density of n-FinFET reduced up to 56% while the hole density reduced up to 46% for p-FinFET with the reduction of W_{top}. These results were supported by the I_d-V_g improvement (Kola, Golio, & Maracas, 1988) as shown in Figure 4.26.

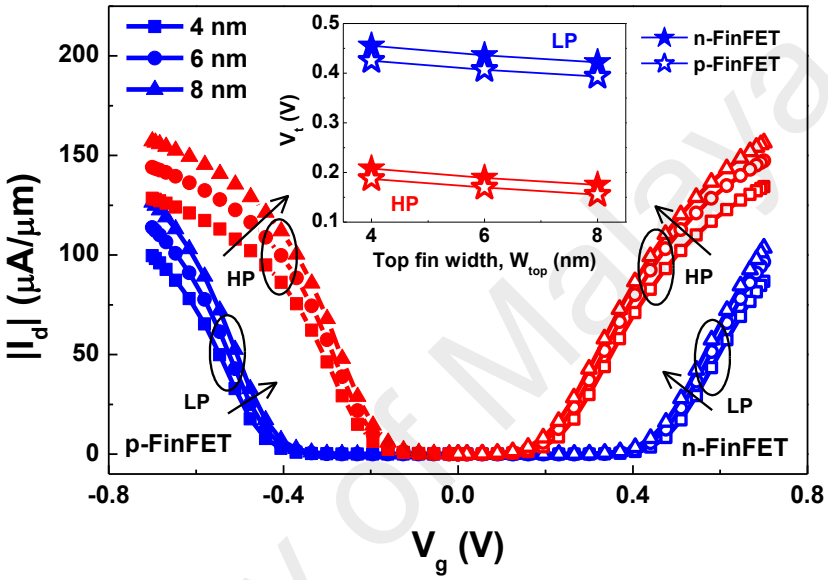


Figure 4.26: I_d-V_g at various W_{top} for LP and HP showing for both p-FinFET and n-FinFET at V_d = 0.05 V.

Figure 4.26 presents the I_d-V_g of the simulated device when the top fin width is varied. From the graph, it is found that as W_{top} increases, the I_d improves particularly at higher V_g for LP devices. The improvement of I_d is due to the higher SCEs at wider width. Increasing W_{top} will reduce the R_{sd} (Joseph & Patrikar, 2013). These will eventually induce the current to improve. The inset of Figure 4.26 shows the extracted V_t of the simulated device in linear region. From the plot, it can be observed that the V_t of the device is reduced as the top fin is wider. Similar trends can be seen from Chabukwar et al. (2010) as the fin width reduced from rectangular shape to triangular shape. Moreover, Figure 4.27 illustrates the inversion charge density at when the width is reduced comparing LP and HP devices. Justified by previous works (Lukyanchikova, Petrichuk,

Garbar, Simoen, & Claeys, 2000; Sallese, Bucher, Krummenacher, & Fazan, 2003; Taur, 2000), the charge density for HP is much higher for p-FinFET with increasing width. Meanwhile, the densities for LP are the lowest when the width is reduced for n-FinFET. Figure 4.28 demonstrated the ratio of the I_{on}/I_{off} where it represents the power consumption of the device. As the W_{top} is varied from 4 nm to 8 nm, the I_{on}/I_{off} ratio reduced. For LP devices, the ratio decreases by 82% and 63% for p-FinFET and n-FinFET respectively. From the figure, it is found that the fin with narrower top has better power consumption since higher I_{on} can be produced with low I_{off} (Lemme et al., 2004).

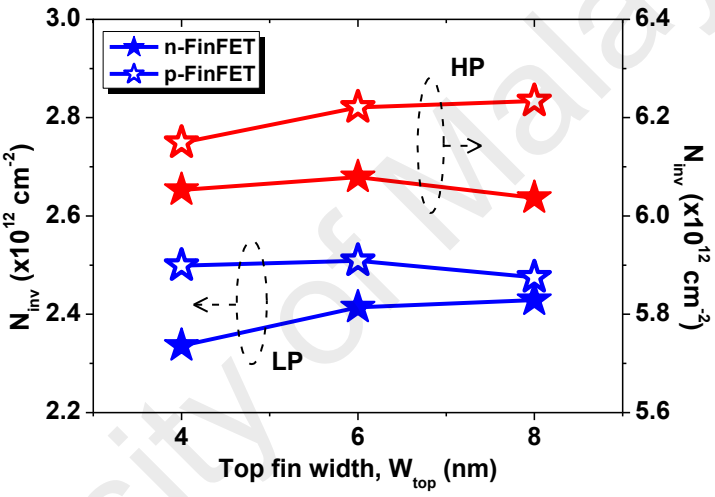


Figure 4.27: Fluctuation of N_{inv} w.r.t W_{top} for LP and HP.

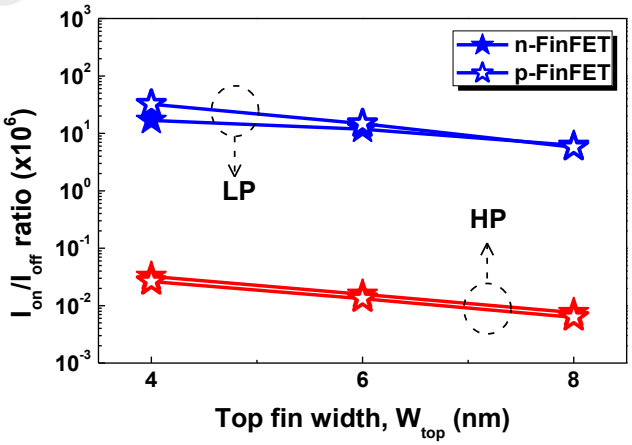


Figure 4.28: W_{top} dependency of the I_{on}/I_{off} characteristics at V_d = 0.7 V for LP and HP.

4.3.1.2 Analysis on 7 nm stress engineered Ge FinFET

A simulation has been done to investigate the effects of geometrical scaling on the I_d-V_g of 7 nm Ge FinFET. Earlier works have shown that geometrical scaling has the most significant effect on device performance especially CMOS devices (Arefinia & Orouji, 2009; Kedzierski et al., 2000; Mukhopadhyay, Raychowdhury, & Roy, 2005; Razavieh et al., 2018). Figure 4.29(a) presents the I_d-V_g of the L_g scaling effects. It is observed that as L_g is varied from 15 nm to 8 nm, the I_d of both n- an p-FinFET can increase up to ~18% and ~14%, respectively. Shorter L_g provides shorter path at the S/D region which results in shorter effective channel length (L_{eff}) (Nakanishi et al., 1992). This allows the current to be transfer from the S/D region in higher speed, therefore reducing the threshold voltage.

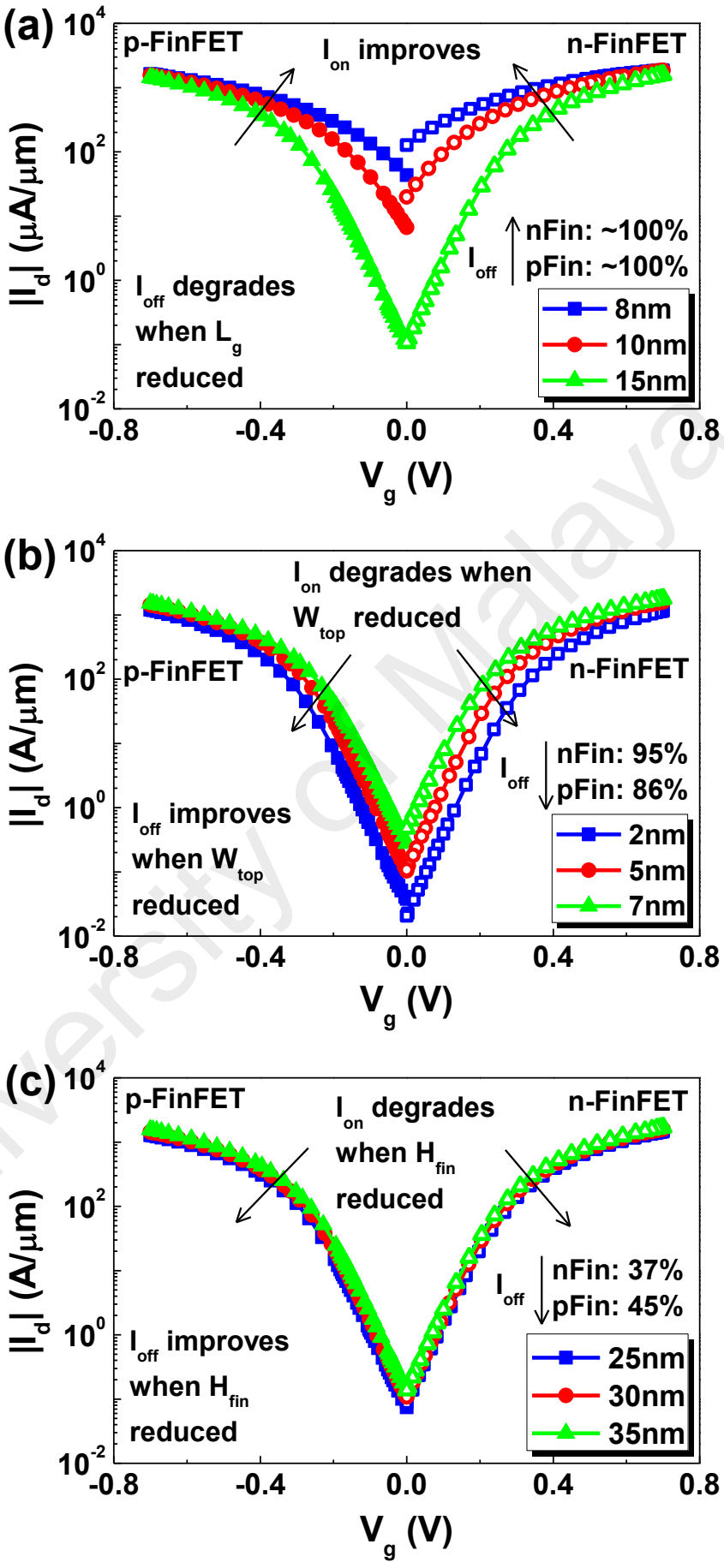


Figure 4.29: I_d-V_g at V_{dsat} for the scaling of (a) L_g, (b) W_{top}, and (c) H_{fin}, showing the I_{on} and I_{off} improvement in logarithmic graph.

The resistance become reduced in shorter path between the S/D regions, hence leading to increasing I_d (Magnone et al., 2008). Nevertheless, the downscaling of L_g can also leads to higher I_{off}. This is expected due to the poor gate control of the channel in short channel FET, as well as higher effective field which can leads to excessive leakage (Ferain et al., 2011). Furthermore, shape of the fin plays an important factor in improving the performance of the transistor, especially in the subthreshold leakage point of view. Figure 4.29(b) shows that as W_{top} becomes smaller, I_{off} can be improved. Since only the top width is varied, the fin shape can be defined as triangular, tapered, and rectangular as the width is varied from 2 nm, 5 nm, and 7 nm, respectively (see Figure 3.7). Rectangular fin is expected to have lower R_{sd} (F. A. M. Rezali et al., 2016). Therefore, it is expected if the current is degraded with the reduction of W_{top}. Figure 4.30 depicts the current density distribution of holes in p-FinFET. The current is pushed towards the centre of the triangular fin, thus improving the leakage current due to stronger gate control. From mobility point of view, the holes for p-FinFET are more mobile in the fin with rectangle shape at the source/channel interfaces, however increase gradually towards the channel/buffer interfaces, as shown in Figure 4.31. It is observed that mobility reduced in narrower top fin, but approaches the mobility of wider top fin towards the buffer. This mobility degradation is most probably caused by the increase of the interface trap density (D_{it}) in the Ge based channel devices (Bae et al., 2016). Moreover, small degradation and enhancement in I_{on} and I_{off} is observed, respectively, in Figure 4.29(c) when the H_{fin} is reduced.

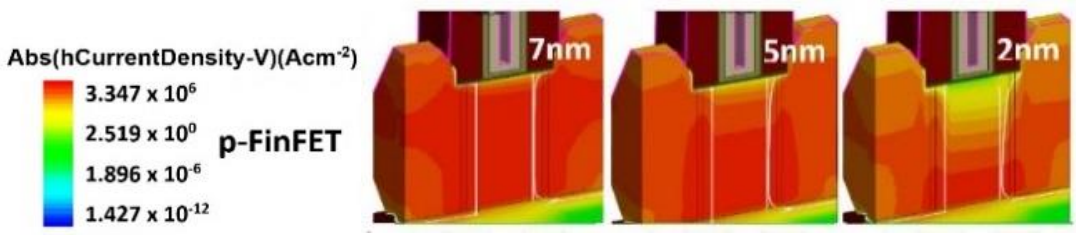


Figure 4.30: Holes current density of p-FinFET w.r.t W_{top} at V_{dsat}.

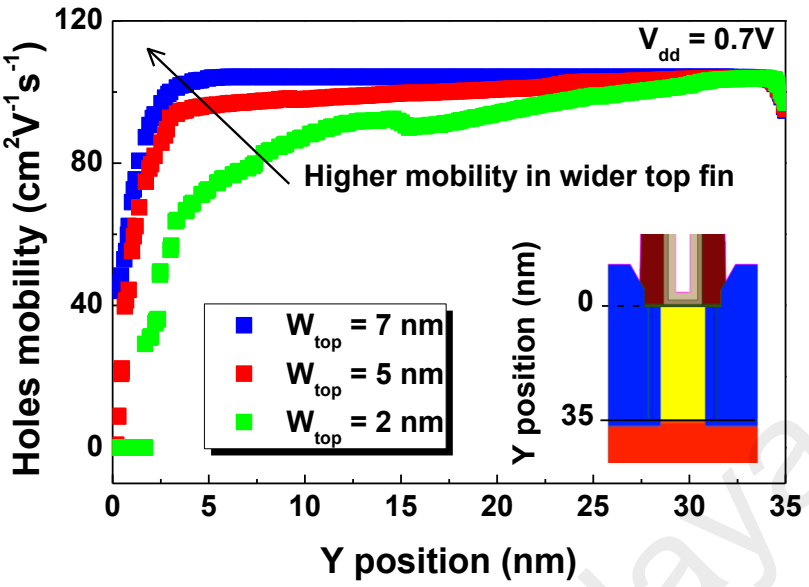


Figure 4.31: Holes mobility in various fin shape near source/channel interfaces.

Meanwhile, Figure 4.32 presents the comparisons of trends for each parameters variations in terms of V_t, I_{on}, and I_{off} performances. It is observed that n-FinFET is more pronounced to be affected compared to p-FinFET with fin geometry variation. Analysing the overall trends, V_t and I_{on} shows improvement when L_g was reduced and W_{top} and H_{fin} were raised. However, increase in I_{off} seems to be very significant especially with reduced L_g. From the observation of Figure 4.32, it is hard to pinpoint the best combinations and interactions of parameters which can contribute to device performance improvements. Therefore, a statistical approach is introduced in order to determine the combinations of parameters that agrees to V_t, I_{on}, and I_{off} performances improvement which will be further discussed.

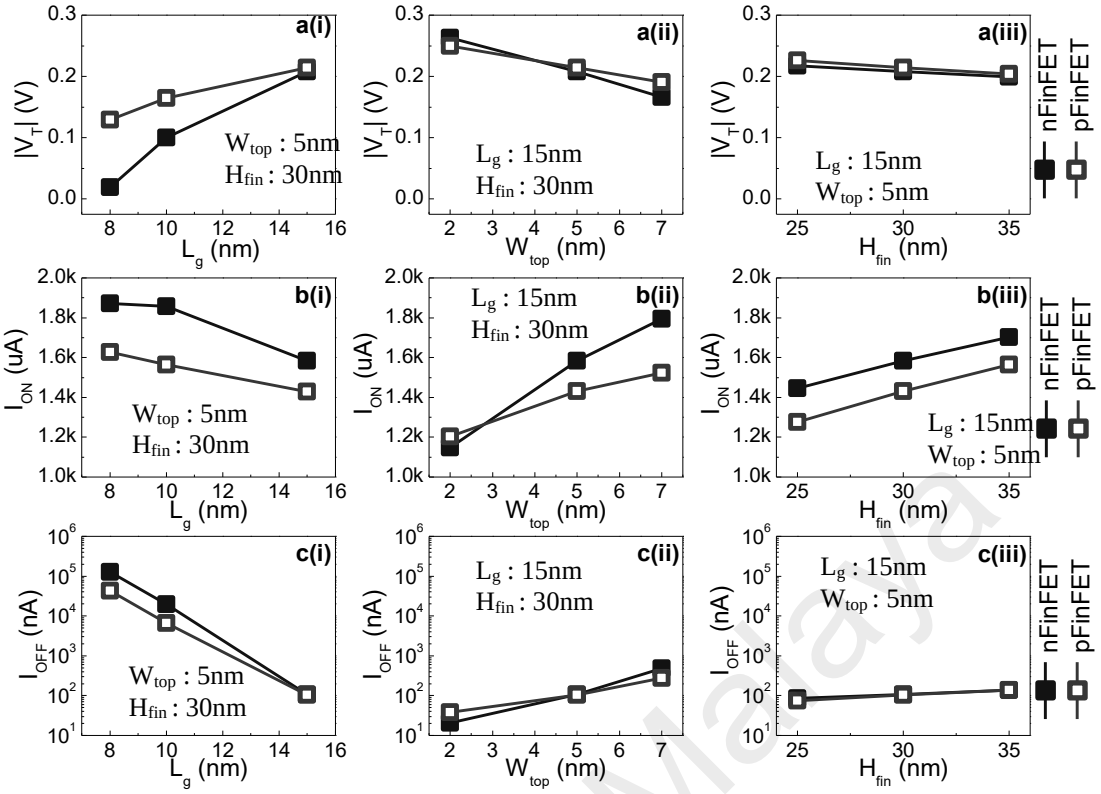


Figure 4.32: Trend comparison of (a) V_t, (b) I_{on}, and (c) I_{off}, of 7 nm Ge FinFET for (i) L_g, (ii) W_{top}, and (iii) H_{fin} scaling.

4.3.2 Effects of doping concentration on 7 nm SiGe FinFET

The impacts of doping concentration on the 7 nm SiGe FinFET is studied for further investigation. Figure 4.33 illustrates the I_d-V_g of N_{ch} tuning. From Figure 4.33, it is observed in the inset that the increase in N_{ch} leads to the rise in V_t. This increment is due to the reduced carrier mobility in highly doped channel (Gaynor & Hassoun, 2014). The I_d is observed to degrade with the channel of highly-doped since higher V_g is required to produce the channel inversion layer as shown in Figure 4.34. However, subthreshold leakage seems to raise with higher doped channel device due to higher V_t in p-FinFET.

In n-FinFET, increase in N_{ch} caused the I_{off} to decrease initially, then increase slightly when the doping is reaching 10^{19} cm^{-3}. These phenomena happened because of the band-to-band tunnelling (BTBT) current enhancement due to highly doped S/D region which is 10^{20} cm^{-3}. Similar trend has been found in (Manoj et al., 2008) and (Gaynor & Hassoun,

2014) for I_{off} performance. Hence, it is important to choose the optimal value of N_{ch} for better power consumption.

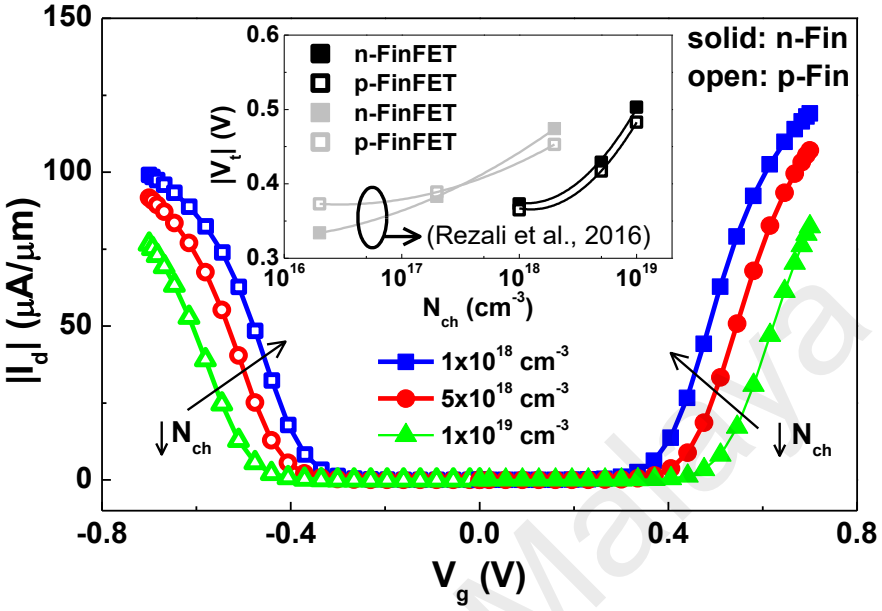


Figure 4.33: I_d-V_g for various N_{ch} at V_{dlin} for SiGe FinFET. Inset is the linear V_t and trend comparison with (F. A. M. Rezali et al., 2016).

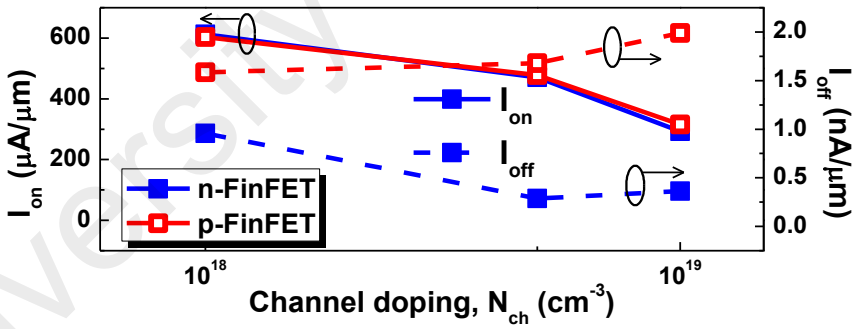


Figure 4.34: I_{on} and I_{off} at V_{dsat} for different N_{ch} doping concentrations.

Meanwhile for N_{sd}, the analysis of the I_d–V_g characteristics in Figure 4.35 has shown improvements when the S/D region is highly doped. Analysing Figure 4.36, it is found that I_{on} increased with the increase in N_{sd}. This is due to the fact that highly-doped source will contribute to more carriers in the source extension for direct source to channel tunnelling (Chang, Zhang, Huang, Wang, & Wang, 2013; Kaur & Kumari, 2016). Highly

doped S/D is used to improve the drive current, despite risking raised in I_{off}, since larger leakage is produced as the V_t is reduced with increasing N_{sd} (Kaur & Kumari, 2016).

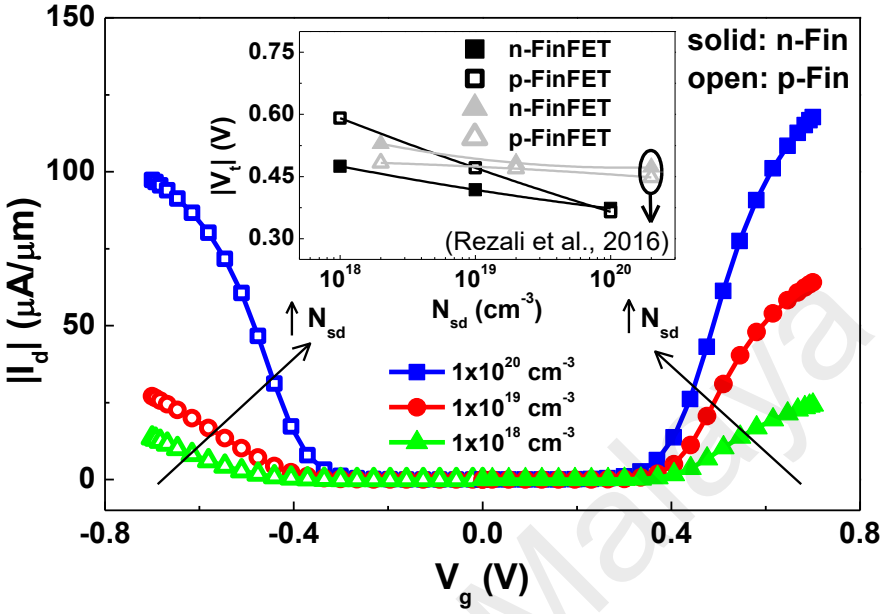


Figure 4.35: I_d-V_g for various N_{sd} at V_{dlin} for SiGe FinFET. Inset is the linear V_t and trend comparison with (F. A. M. Rezali et al., 2016).

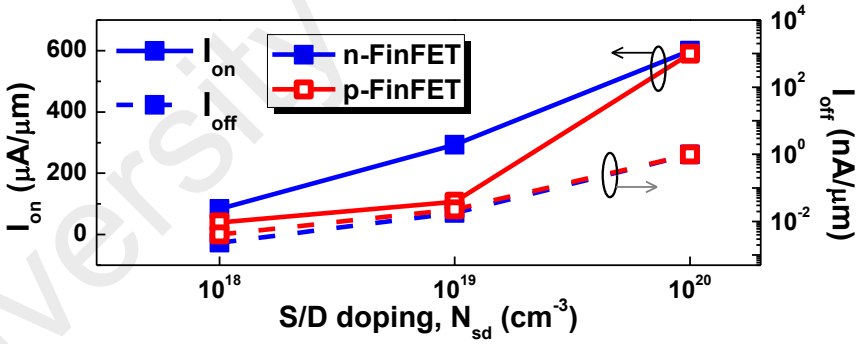


Figure 4.36: I_{on} and I_{off} at V_{dsat} for different N_{sd} doping concentrations.

The I_{on}/I_{off} ratio is calculated and presented in Figure 4.37(a). From the figure, the ratio is dropping for both n- and p-FinFET for N_{sd} evaluation. Similar trends were seen in (Kaur & Kumari, 2016) and (Pal, Nehra, Kaushik, & Dasgupta, 2015) where the ratio degrades with increasing N_{sd}. In addition, Figure 4.37(b) depicts the SS of the silicon germanium FinFET as the doping concentration in the channel and S/D region is varied. Lower SS is observed for the device with higher N_{ch} and lower N_{sd}. This condition is beneficial to high

sensitivity devices since smaller V_g is needed to be invert the channel, by which can lead to improve efficiency of FET devices. Studies on Figure 4.38 shows that channel with highly doped and S/D region with low-doped has the least DIBL for SiGe FinFET. Therefore, the values of the doping concentration needs to be tuned properly, to the extent of not exceeding 10^{20} cm^{-3} to maintain the device performance as well as to counter the trade-off in current performances, as mentioned in (F. A. M. Rezali et al., 2016).

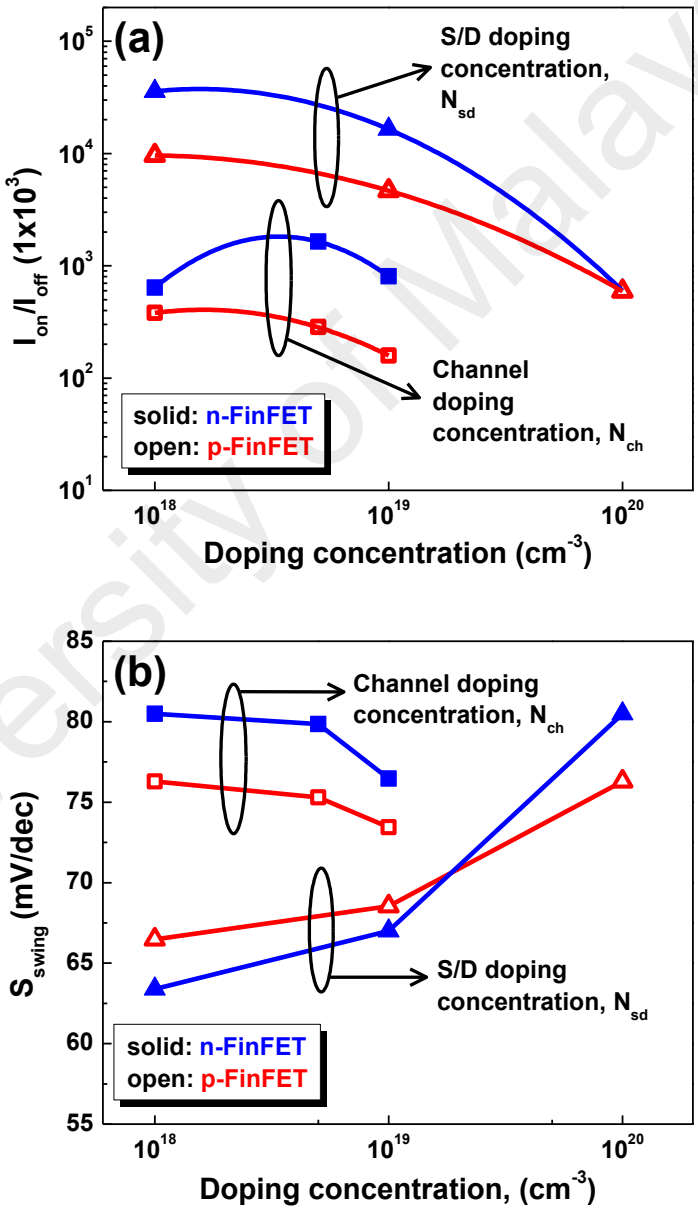


Figure 4.37: Graph of (a) I_{on}/I_{off} ratio; and (b) SS, of the SiGe based FinFET with various N_{ch} and N_{sd} at V_{dsat}.

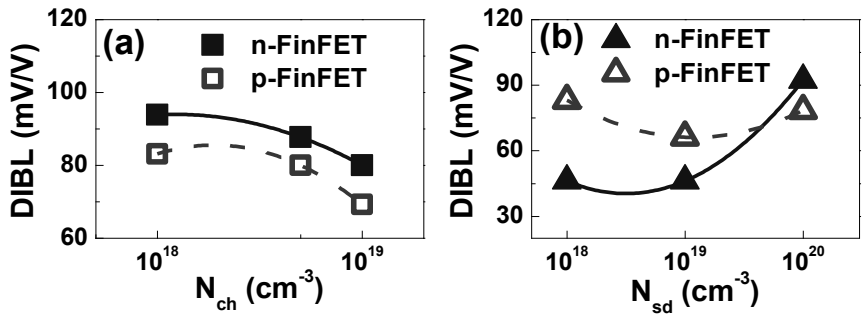


Figure 4.38: DIBL characteristics for (a) N_{ch} and (b) N_{sd} dependences for SiGe based FinFET.

4.3.3 Effects of layer thickness on GaN based HFET

Next, the investigation is furthered by studying the impact of geometrical variation of the optimized design of HFET (Structure 3). Structure 3 is marked as the most optimized design for GaN based HFET according to the findings of this work. Therefore, in this section, this structure is analysed for the geometrical effects on GaN based FET devices. The effects of layer thickness variation on I_d-V_g is shown in Figure 4.39. The impact of graded AlGaN barrier layer thickness (t_{br}), AlN interfacial spacer thickness (t_{sp}), and GaN buffer thickness (t_{bf}) variation is analysed. From Figure 4.39(a), it is observed that the I_{on} performance degrades as the t_{br} decrease. However, smaller t_{br} exhibit smaller V_t, which can improve the switching speed of the device. Similar trends are observed in Figure 4.39(b) and Figure 4.39(c) when the t_{sp} and t_{br} is varied from 2 nm to 5 nm and from 2 µm to 3 µm, respectively. In addition, Figure 4.40 illustrates the AlGaN t_{br} dependence on the electron density in the device channel. It is observed that the concentration of the electron increases as the t_{br} increases. This is due to the fact that the gate has less control over the channel in larger t_{br} (Toprak, Sen, & Ozbay, 2015). Simulated results from Kajitani et al., (2015) shows higher concentrations compared to this work as the barrier is diffused with additional In material with higher xmole. Besides with different xmole in each barrier layer, the bandgap offset can be vitally affected, thus further affecting the 2DEG of the devices. However, larger t_{br} tends to reduce the gate-to-source and gate-to-drain capacitance, which can leads to the g_m degradation (Faraclas, Webster, Brandes, &

Anwar, 2004; Majumdar, Das, & Biswas, 2015). Therefore, t_{br} needs to be tuned properly to a point by which when it exceeded the point, the I_d will become saturated due to the alteration of the surface states Fermi position (Liddle, 2008; Mead, 1966).

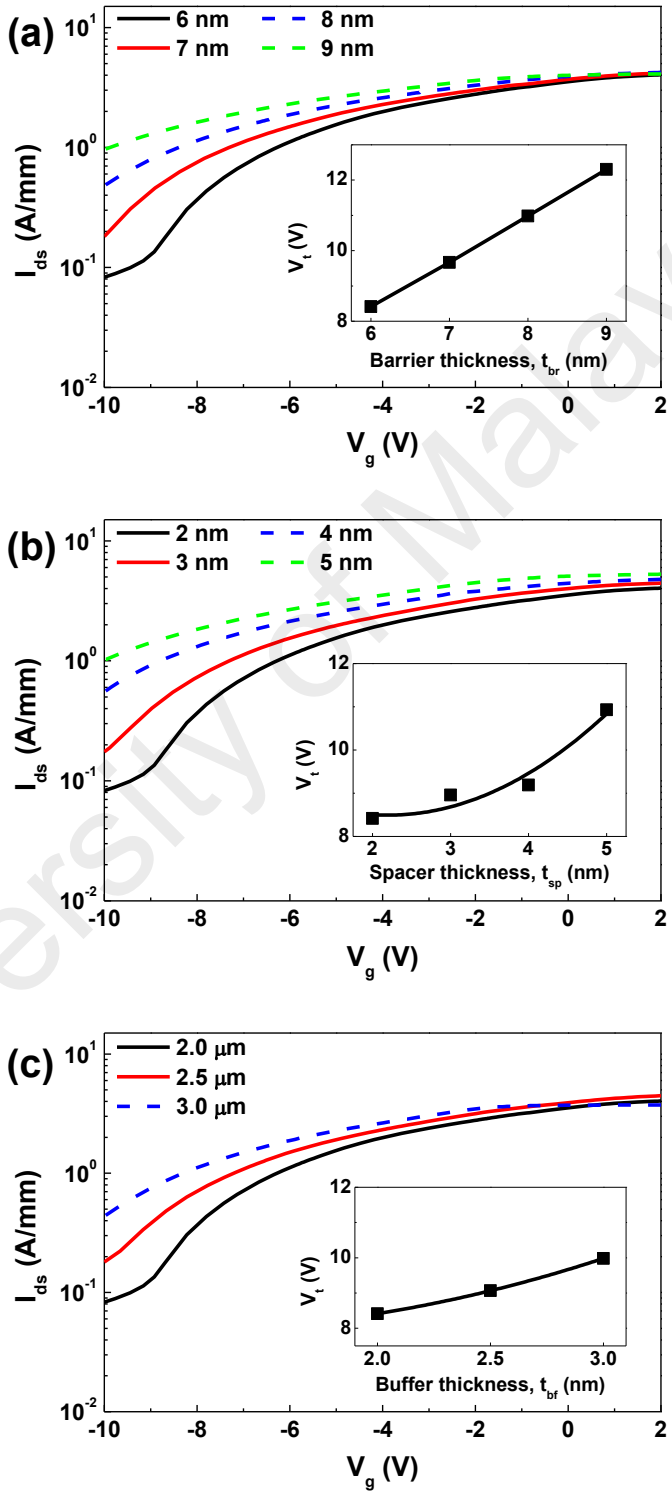


Figure 4.39: I_d-V_g at V_d = 36 V for various (a) t_{br}, (b) t_{sp}, and (c) t_{bf} of the AlGaN/AlN/InGaN HFET. Insets are the V_t of the AlGaN/AlN/InGaN HFET with respect to t_{br}, t_{sp}, and t_{bf}, respectively.

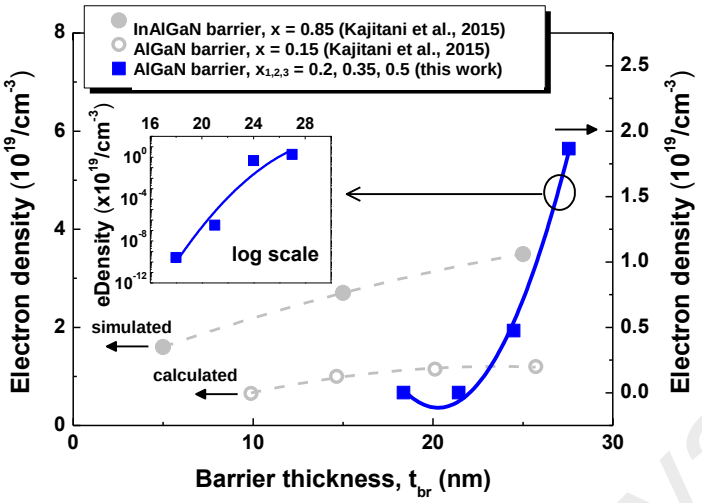


Figure 4.40: Electron density of the optimized HFET at the 2DEG interfaces for different t_{br}. Inset is the log scale of the graph.

On the other hand, the DC I_d-V_d on the t_{sp} variations was illustrated in Figure 4.41(b). The output current is enhanced by 77% when the thickness of AlN interfacial spacer layer is increased from 2 nm to 5 nm. This is expected since the electron concentration is improved with increased thickness, as observed in Figure 4.42. When t_{sp} is increased, the 2DEG position is shifted away from the interface hence reducing the interface roughness scattering (Antoszewski et al., 2000). According to Shrestha et al. (2014), the mobility increases with increasing spacer thickness up to a critical thickness (t_c), and reduced back beyond the t_c due to the 2DEG positioning towards the interfaces at higher t_{sp}. This action will lead to the increasing of Coulomb scattering in 2DEG region, hence reducing the mobility beyond the t_c. The dependency of electron mobility on the t_{sp} beyond the t_c is also shown in Figure 4.42.

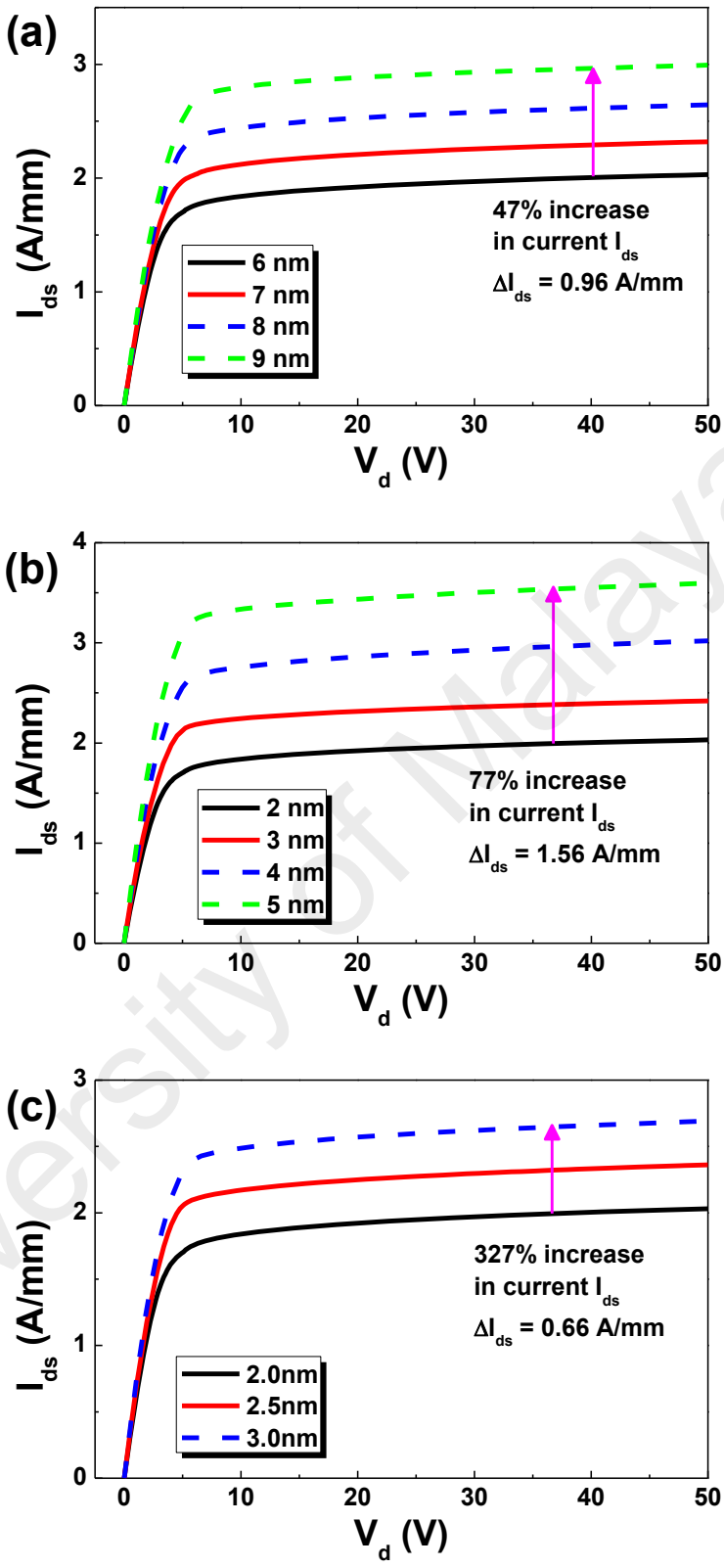


Figure 4.41: I_d-V_d at V_g = 2 V for various (a) t_{br}; (b) t_{sp}; and (c) t_{bf} of the AlGaN/AlN/InGaN HFET.

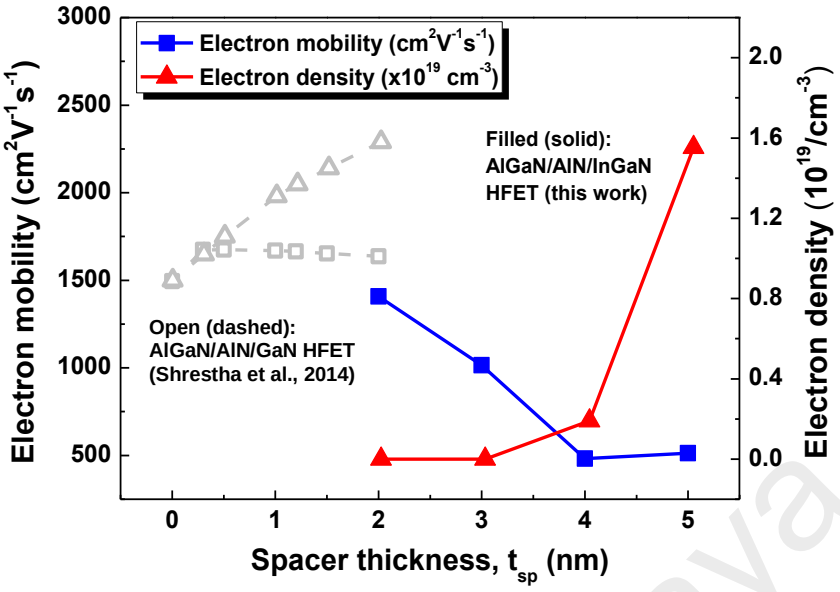


Figure 4.42: The effects of t_{sp} on electron mobility and density of the $Al_xGa_{1-x}N$/ AlN/InGaN HFET ($x_{1,2.3}$ = 0.2, 0.35, 0.5). Trends compared to (Shrestha et al., 2014)

In addition, note from Figure 4.43 that the current density under the gate region is higher for 5 nm t_{sp}, corresponds to the higher buffer leakage as shown in Figure 4.44(b). In higher thickness of AlN spacer layer, the conduction band off set is expected to increase, hence improves the 2DEG concentration level. Meanwhile from t_{bf} perspective, higher thickness produces lower on current compared to smaller thickness. However, by observing Figure 4.44(c), the used of 2.5 µm thickness can enhance the on current despite having followed by the small raised in off current. The off current however dropped at higher t_{bf}. This is because with thicker buffer layer, the leakage current can be restrained (Yu et al., 2014) hence, producing enhanced breakdown performance (Domenica et al., 2009; Hove et al., 2012).

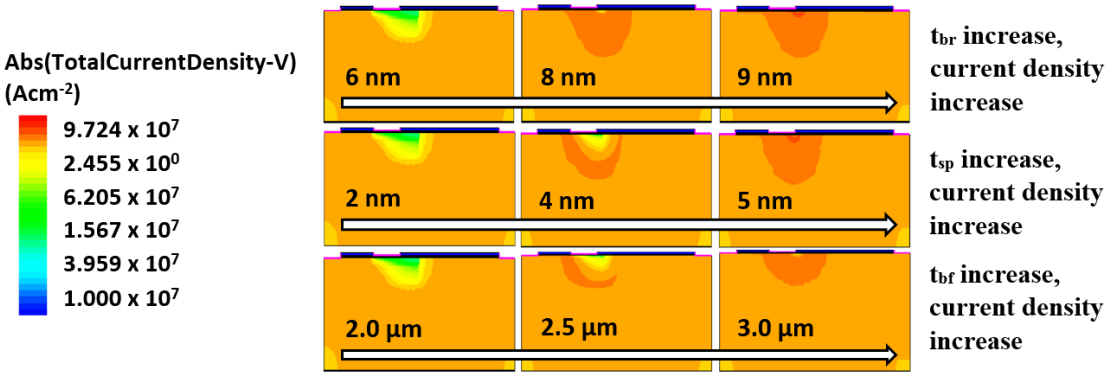


Figure 4.43: Total current density distributions at V_d = 36 V for varying t_{br}, t_{sp}, and t_{bf} in $Al_xGa_{1-x}N$/AlN/InGaN HFET ($x_{1,2.3}$ = 0.2, 0.35, 0.5).

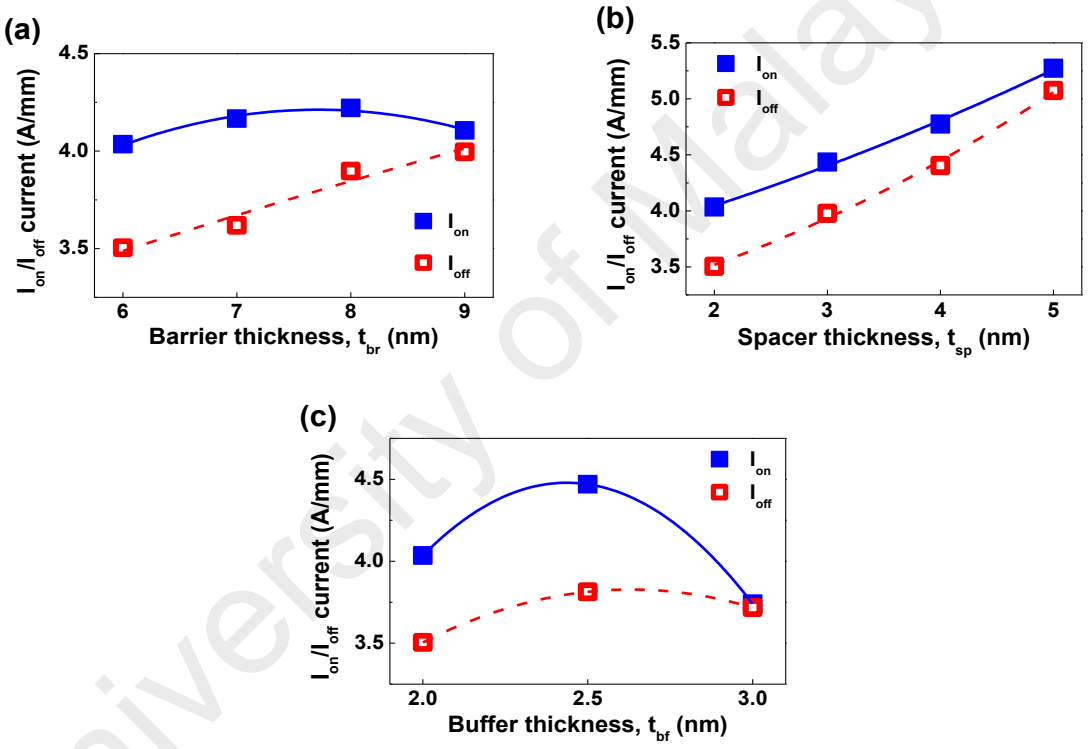


Figure 4.44: I_{on} and I_{off} at V_d = 36 V with respect to t_{br}, t_{sp}, and t_{bf}.

The electron mobility enhancement of the geometrical designs is shown in Figure 4.45. From the figure, the electron mobility is enhanced with decreasing thickness of each barrier layer, spacer and buffer layer. The enhancement of electron mobility is resulting from lower electric field as well as interface roughness scattering, and is also considered to be a huge contribution to the improved 2DEG confinements.

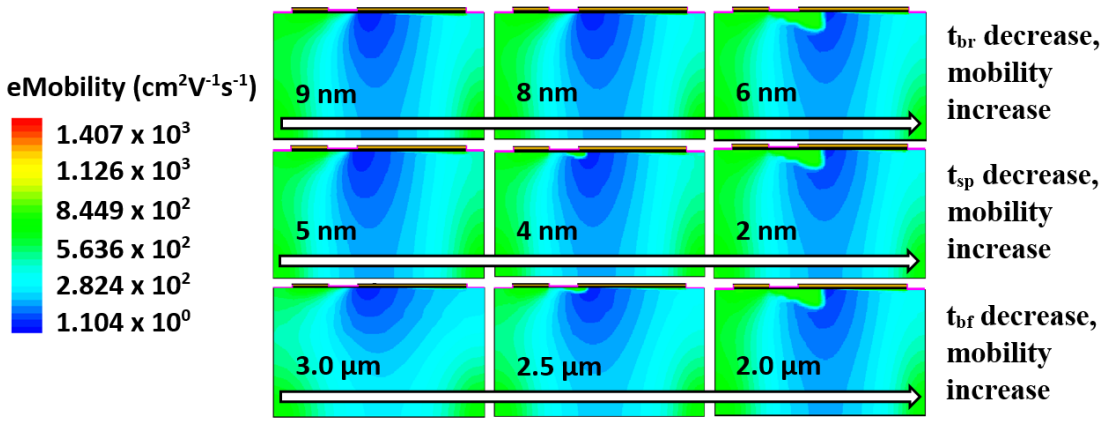


Figure 4.45: Electron mobility distribution at V_d = 36 V for varying t_{br}, t_{sp}, and t_{bf} in $Al_xGa_{1-x}N$/AlN/InGaN HFET ($x_{1,2,3}$ = 0.2, 0.35, 0.5).

4.4 Optimization of fin geometry for 7 nm Ge based strained FinFET

The objective of this work is to optimize the 7 nm Ge FinFET performance by taking into account the fin geometry using the statistical approach of the Taguchi method. The factors that affecting the device performance are set to be be L_g, H_{fin} and W_{top} by which were assigned as A, B and C respectively (see Table 3.3). Three-level standard OA of L_{27} (3^{13}) used in this work (see Appendix A) which is chosen due to its capability of checking the interactions among factors. The OA indicates that 27 sets of simulation is done. The optimized designs are analysed with respect to the performance of I_{on}, I_{off}, and V_t for n-FinFET (see Appendix B) and p-FinFET (see Appendix C). Should the device aim for higher I_{on}, the LTB characteristic is applied to perform the DOE. In terms of I_{off} performance, the device requires for low current which indicates low subthreshold leakage thus using the STB characteristics. Meanwhile, in terms of V_t, the NTB characteristic is applied to perform the experiments. The average SNR for each level performance responses for n- and p-FinFET are shown in Appendix D and Appendix E, respectively. These data are then plotted in graphical form as illustrated in Figure 4.46, Figure 4.47, and Figure 4.48 for I_{on}, I_{off}, and V_t performance, respectively.

4.4.1 Taguchi method: SNR approach

Figure 4.46 illustrates the average SNR for LTB of I_{on} performances. Analysis of the figure suggests that W_{top} (factor C) and interaction between L_g and H_{fin} (factor A x B) are significant to give impacts on the I_{on} in both p- and n-FinFET. Other factors shown to be less significant since smaller slope is produced by each line compared to factor C and the interaction factor (A x B). Following this event, the two-way table (A x B) was built to pinpoint the best combination of L_g and H_{fin} as shown in the table in Appendix F and Appendix G for n- and p-FinFET, respectively. From the table, the most optimal result achieved for L_g and H_{fin} is A0B2 for both p- and n-FinFET. Meanwhile for factor C, the highest SNR for W_{top} is the 7 nm which is C2 for both devices. Therefore, the optimal combination to get improve I_{on} for both p- and n-FinFET is A0B2C2 within the tested range area.

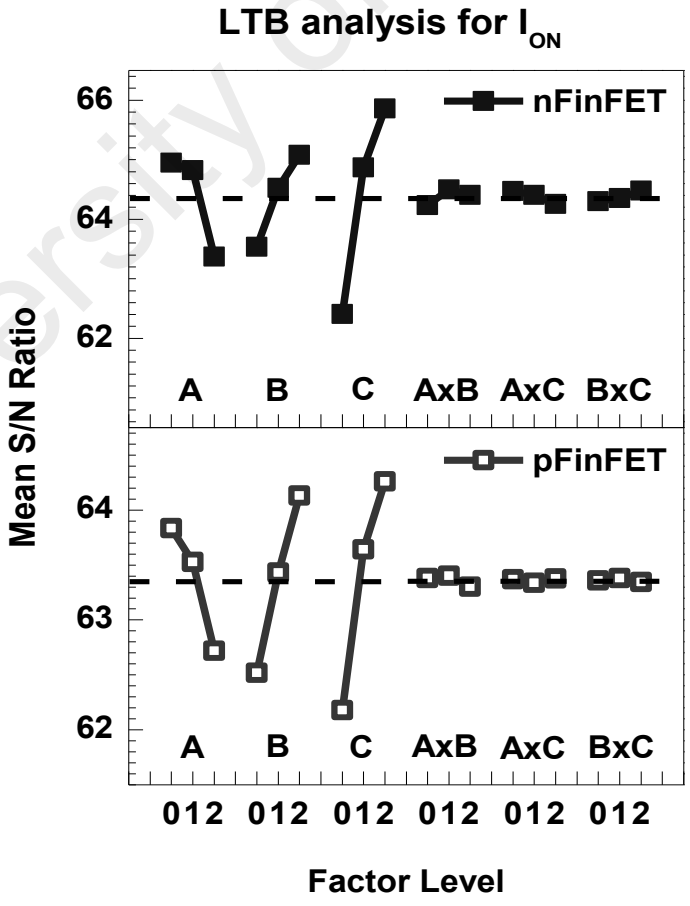


Figure 4.46: Average SNR against factor level for I_{on} for both n- and p-FinFET.

On the other hand, observations of the SNR graph on I_{off} performance for STB characteristics in Figure 4.47 suggests that the L_g (factor A) is the most important factor for both p- and n-FinFET. In terms of interactions, it is found that interaction between L_g and H_{fin} (factor A x B) are more significant in p-FinFET, while interaction between L_g and W_{top} (factor A x C) are more significant in n-FinFET. Following the same procedures as in the LTB analysis, it is observed that the most optimal result achieved for the interaction between L_g and W_{top} is A2C0 (see Appendix F) with the largest average ratio for H_{fin} (factor B) to be B0 for n-FinFET. In the meantime, the two-way table (see Appendix G) indicates that the optimal result in p-FinFET for interaction between L_g and H_{fin} is A2B0 with the largest average ratio for W_{top} (factor C) to be C0. Thus, the optimal combination in order to obtain low I_{off} is observed to be the combination of A2B0C0.

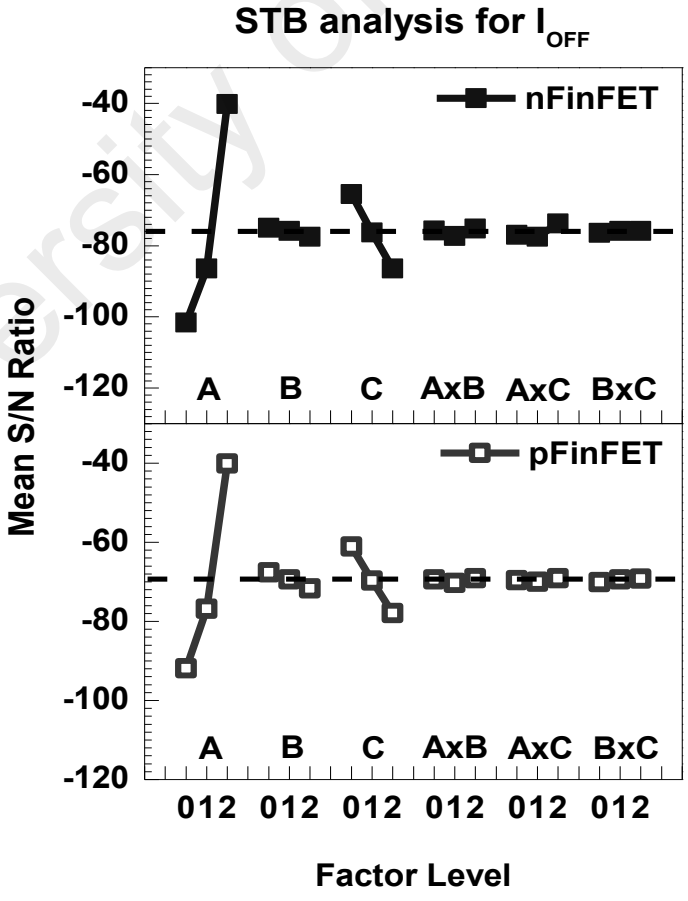


Figure 4.47: Average SNR against factor level for I_{off} for both n- and p-FinFET.

Meanwhile, the study on Figure 4.48 show that to alter V_t, L_g (factor A) is more significant in both p- and n-FinFET. Observing the interaction of factors, it shows that interaction between L_g and W_{top} (factor A x C) and H_{fin} and W_{top} (factor B x C) are more significant in p- and n-FinFET respectively. By observing the two-way, the optimal result of B0C0 in the n-FinFET (see Appendix F) is obtained with the largest average ratio for L_g (factor A) to be A1, while in p-FinFET (see Appendix G) the result of A1C1 is obtained with the largest average ratio for H_{fin} (factor B) to be B2. Hence, A1B2C1 and A1B0C0 are selected as the best combination for nominal V_t design for p- and n-FinFET respectively.

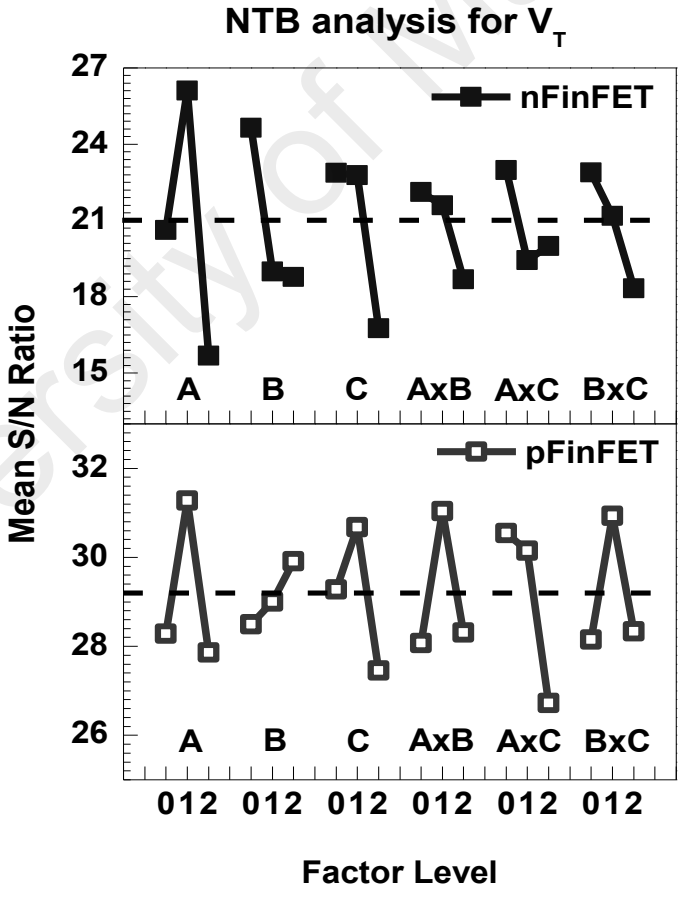


Figure 4.48: Average SNR against factor level for V_t for both n- and p-FinFET.

4.4.2 Best combinations design analysis

Taguchi method is implemented in Ge based FinFET optimization. This has shown major improvement as observed in each response performance. It is found that in order to obtain high I_{on}, a trade-off in I_{off} existed where leakage current appears to be higher due to reduced V_t. Figure 4.49 presents the I_d-V_g of the optimized designs for LTB, STB, NTB, and Intermediate analysis for both p- and n-FinFET as compared to the unstrained Si FinFET.

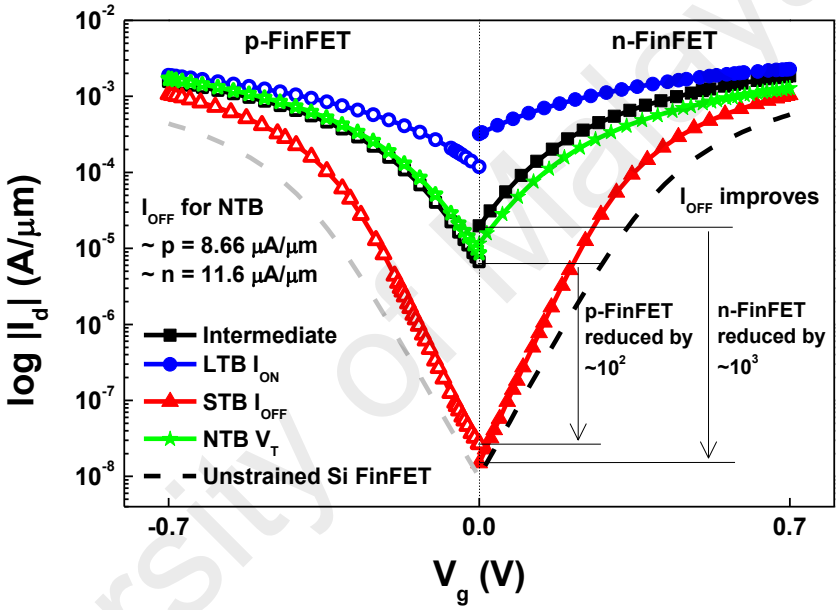


Figure 4.49: I_d-V_g at V_{dsat} showing I_{off} in logarithmic graph for Intermediate as well as the optimized designs of LTB, STB and NTB compared to unstrained Si FinFET.

From Figure 4.49, the unstrained Si gives better leakage control with lower I_{off} compared to the design of Ge based FinFET. The fact that the magnitude of the D_{it} is higher in strained devices due to increase Ge content inside the channel, this will lead to the shifting of V_t and the reduction of I_{off} (Bae et al., 2016). In order to reduce the D_{it}, the formation of the interfacial layer as well as the treatment in pre- and post-formation can be implemented, so that the mobility enhancement of as well as the SS can be obtained. Moreover, it is found that adopting the combination of wider L_g together with shorter H_{fin} and W_{top} shows an enhancement in I_{off} as it reduced by approximately 10^2 in p-FinFET

and 10^3 in n-FinFET compared to the combination for intermediate dimension. From the observation for I_{off} design through STB analysis, these combinations could enhance the gate controllability with the application of the tapered shape (Gaynor & Hassoun, 2014). Furthermore, the use of shorter width is expected to increase the R_{sd} between both regions (Magnone et al., 2008) due to lower inversion charge density (N_{inv}) in narrow W_{top} resulting in lower leakage current. The implementation of the tapered shape for the device fin design allows stronger gate control as the leakage current is pushed into the centre of the triangular fin (F. A. M. Rezali et al., 2016), hence anhancing the I_{off} density distribution with reduced region. Figure 4.50 illustrates the total current density distribution for each optimized design. From the figure, it is found that the total current density distributions for efficient I_{off} designs are much lower compared to others which represents less current were exposed to the subthreshold leakage.

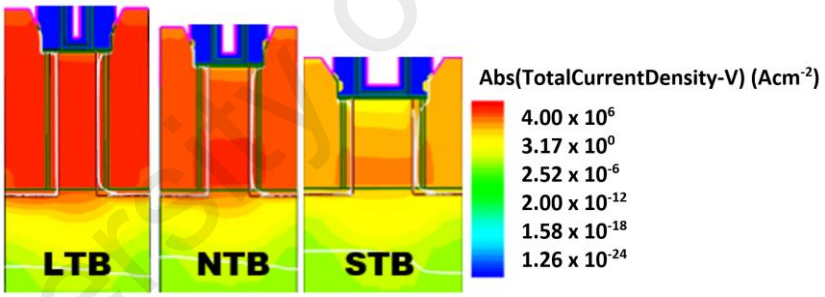


Figure 4.50: Total current density distribution in p-FinFET for LTB, NTB and STB analysis at V_{dsat}.

On the other hand, study of Figure 4.51 shows that the current can be enhanced by fin geometry optimization, adopting shorter L_g combined with larger H_{fin} and W_{top}. It is found that the I_{on} can be improved up to approximately 22% and 21% in n-FinFET and p-FinFET respectively. The LTB analysis for high I_{on} design performance suggests that the parameters combination achieved could enhance the current density as well as channel mobility due to higher electric field (F. A. M. Rezali et al., 2016). The current will flow from through S/D with higher speed in shorter L_g due to the reduction of magnitude in

R_{sd}. The rapid current flow in the channel is also attributed to the presence of stress, resulting reduction in V_t and in turns improves in I_{on}. Moreover, observation of Figure 4.52 on band-to-band tunnelling shows larger density particularly in I_{on} designs clearly caused by higher electric field at drain region hence reducing V_t. It is worth mentioning that the n-FinFET shows better improvement compared to p-FinFET for designs favouring high I_{on} performance and low I_{off}. Although the I_{off} is much lower in unstrained Si device, the difference in the I_{on} can be accounted as a vital point in providing better I_{on} performance.

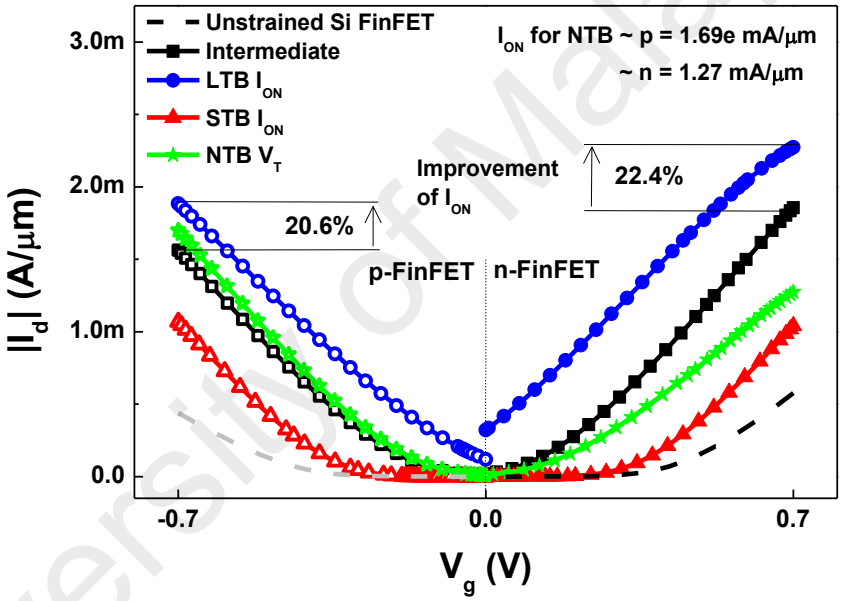


Figure 4.51: I_d-V_g at V_{dsat} showing I_{on} in linear graph for Intermediate, as well as the optimized designs of LTB, STB and NTB compared to unstrained Si FinFET.

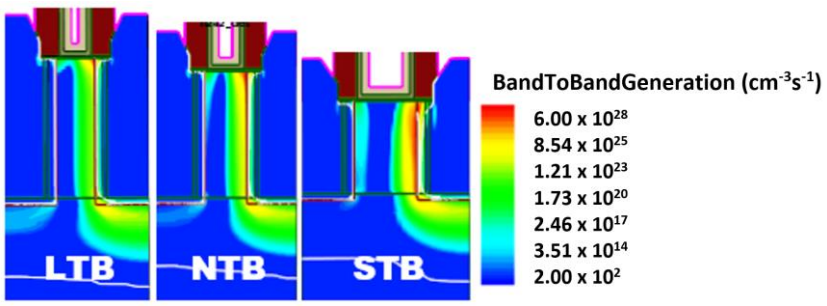


Figure 4.52: Band-to-band tunnelling (BTBT) in p-FinFET for LTB, NTB and STB analysis at V_{dsat}.

The performance improvement is furthered proved by observing the V_t shifting as well as DIBL and SS behaviour of the optimized designs. DIBL and SS are two of the important parameters which are required for scaling and low power consumption transistor modelling. Figure 4.53 depicts the comparisons of each designs performance in V_t, DIBL and SS of both n- and p-FinFET.

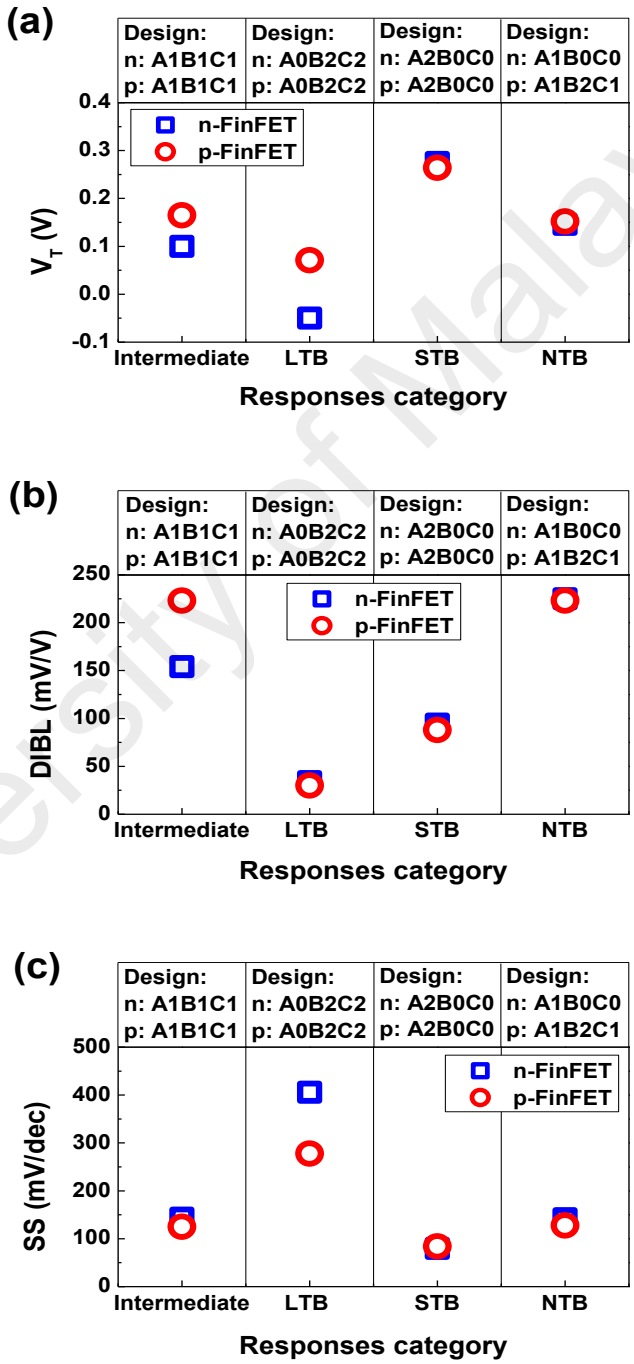


Figure 4.53: Comparison between the optimized design in (a) V_t, (b) DIBL, and (c) SS of both n- and p-FinFET for Intermediate, LTB, STB and NTB analysis.

It is observed that V_t for high I_{on} design performance is lower compared to the design which favours a low I_{off}. This is due to the smaller L_g in I_{on} design which allows the current to flow faster in S/D region resulting in reduced V_t in order to increase I_{on}. However, since the leakage is potentially higher in low V_t devices prior to shorter channel, NTB analysis for V_t design is introduced to obtain nominal V_t for high I_{on} with reasonable I_{off} (W. Y. Choi, Park, Lee, & Liu, 2007). Study on Figure 4.53(b) indicates both I_{on} and I_{off} designs results in lower DIBL which is less than 100 mV/V, particularly for I_{on} design. Apparently, in order to achieve high effective current (I_{eff}) as well as R_{on}, low DIBL is required (Ho, Sun, Shin, & Liu, 2013). In terms of SS behaviour in Figure 4.53(c), I_{off} design by STB analysis shows a low magnitude compared to other conditions despite having degradation in V_t.

4.4.3 Pareto analysis of variance (ANOVA)

To validate the results, the contribution of each geometrical parameter to each device performance was further investigated by applying the Pareto analysis of variance (ANOVA) for n- and p-FinFET (see Appendix H and Appendix I). The Pareto analysis is a useful technique where many possible courses of action competing for attention and clearly form top priorities to identify targets. On the other hand, ANOVA is a statistical model in which includes partitioning of the total variability of a set of observations or measurements. Figure 4.54 and Figure 4.55 presents the Pareto diagram of designs aiming for an efficient I_{on}, I_{off} and V_t performances, for n- and p-FinFET, respectively. It is found that W_{top} (factor C) is the most dominant in LTB analysis for efficient I_{on} design by 54% and 69% for p-FinFET and n-FinFET respectively, while L_g (factor A) has been chosen to be the most dominant factor in STB analysis for efficient I_{off} design by 90% for both type devices. However, the interaction factor between L_g and W_{top} (factor A x C) has shown to be the most dominant by 69% in p-FinFET and 52% in n-FinFET in NTB

analysis. Subsequently, the intermediate value of L_g is chosen for both devices in NTB analysis to design a high I_{on} with appropriate I_{off} level. For n-FinFET, the lowest value of H_{fin} and W_{top} were required to suggest low I_{off} performance. On the contrary, the highest H_{fin} with intermediate value of W_{top} was selected for high I_{on} performance. Adopting this sets of dimensions' combinations, the nominal value of V_t can be obtained with the values of -0.152V for p-FinFET with 0.146V for n-FinFET. The SNR achieved for both p- and n-FinFET were 32.12 dB and 24.15 dB respectively. With this combination, the trade-off between I_{on} and I_{off} can be countered reasonably.

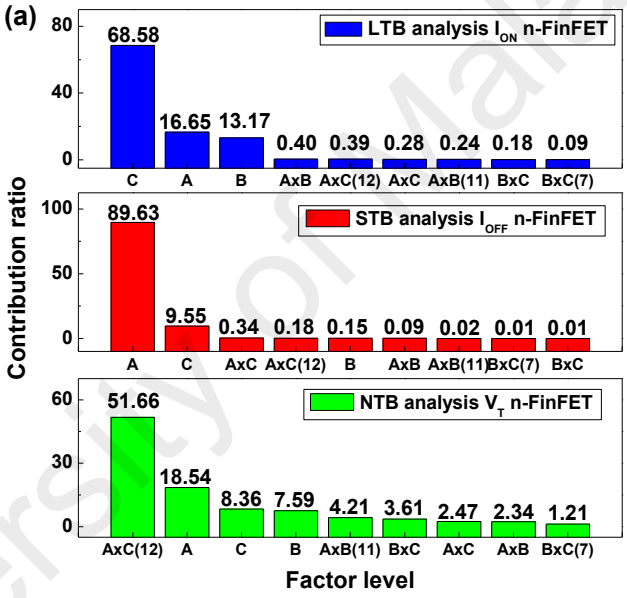


Figure 4.54: Pareto diagram of contribution ratio for factors and interactions in n-FinFET.

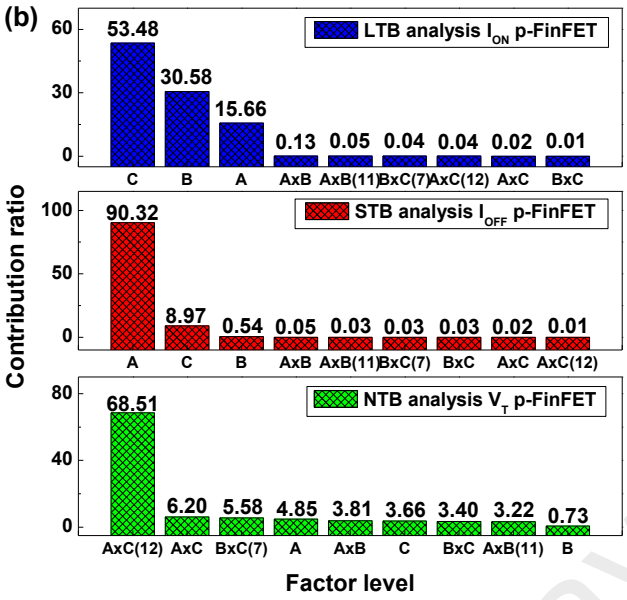


Figure 4.55: Pareto diagram of contribution ratio for factors and interactions in p-FinFET.

4.5 Summary

The device performances of advanced FET devices were analysed in this section. The analysis of this work consists of three parts: i) the group IV and III-V implementations on FinFET and HFET, respectively, ii) geometrical and process considerations on the advanced FET devices, and iii) optimization proses by statistical approach of Taguchi method and Pareto ANOVA. The study enables researchers to understand in details the device potential performance and design considerations by examining the impact of particular design parameters on critical electrical performance including V_t, I_{on}, I_{off}, DIBL, channel stress, etc. For the first part, the stressor effect on FinFET and HFET devices were examined by incorporating group IV and III-V compound semiconductor into the devices structure, respectively, and its impact on device performances were recorded. From FinFET analysis, the channel stressor is the most important parameters in adjusting threshold potential and drive current. Highly strained channel allows the carrier to boost speed, hence increasing carrier mobility. Different based of FinFET is sensitive to different stressor applied onto the device. For instance, SiGe based n-FinFET has shown major improvement in terms of I_{on} with high strained SRB region, while enhancing the current with increasing strain in S/D epitaxial for Ge p-FinFET. These sensitivity variations are highly due to the fact that each device structure was injected with different stress profile. Meanwhile for HFET analysis, several optimizations are done to the conventional AlGaN/GaN HFET designs, in which the final proposed structure consists of a step graded barrier layer of different Al xmole, AlN spacer, and InGaN channel layer. The $Al_xGa_{1-x}N$/AlN/InGaN HFET ($x_{1,2,3}$ = 0.2, 0.3, 0.5) produce encouraging results in terms of mobility and 2DEG confinements. Next, the effect of process and geometrical considerations on the FET device performances are investigated. Doping tuning is considered as one of the dominant process parameters in improving advanced FET devices. Apparently, the doping needs to be chosen optimally to maintain the device

performance despite having trade-offs in drive currents and subthreshold leakage. Despite that, fin design is also important in boosting device performances. The most preferable design is when the fin is small and tapered in shape for it to have maximum gate control over the channel. While small transistors present opportunities for high performance, they also increase undesired degradation effects during operations such as SCEs and increase R_{sd}. Therefore, the FinFET design needs to be optimized for better performance, particularly from the current trade-offs perspective. Meanwhile for HFET study, the impacts of geometrical variation show that the drive current is improved by increasing the thickness of the barrier, and spacer layer despite having a trade-off to higher buffer leakage. On the contrary, reducing the thickness can lead to mobility enhancement, hence improving the device performance. For the final part of this work, fin geometry optimization is performed to further control the V_t adjustments. Taguchi method is used in order to study the combined effect with respect to device performance. The factors that affecting the device performance are set to be L_g, H_{fin} and W_{top}. From the optimization analysis, the best design combination for nominal V_t is when the L_g is 10 nm, H_{fin} is 25 nm, and W_{top} is 2 nm for n-FinFET and L_g is 10 nm, H_{fin} is 35 nm, and W_{top} is 5 nm for p-FinFETs. For the highest I_{on}, the most optimized design achieved is with L_g is 8 nm, H_{fin} is 35 nm, and W_{top} is 7 nm for both devices. On the other hand, optimized fin geometry design using L_g is 15 nm, H_{fin} is 25 nm, and W_{top} is 2 nm is obtained for the lowest I_{off} performance. All the optimization designs show enhanced performance compared to the intermediate level design and L_g, W_{top}, and interaction of both are shown to be the dominant factor in n-FinFET and p-FinFET performances. This design requirement can help in designing targeted applications such as multi threshold design specification and low standby power design.

CHAPTER 5: CONCLUSIONS AND FUTURE WORKS

As far as the success of device downscaling is concerned, any reduction in feature sizes can eventually cause the CMOS device performance to deteriorate tremendously due to excessive leakage. This phenomenon has marks the end of Moore's law in IC design and semiconductor industry. Practically, alternatives need to be considered to bring forward new innovations and scaling vector in improving the device performance with respect to speed, drive currents, as well as power consumptions. In order to do these, a TCAD tools are utilized to the fullest to perform a study by simulation in which is an excellent way to predict the device potential performance and to study the effects of specific device designs. The research outcomes have been divided into three parts, as follows:

The first part focused on the simulation study on the implementation of group IV and III-V semiconductor on the advanced FET devices, namely FinFET and HFET, respectively. Analysis on the impacts of the stressor onto FET devices' performances had been achieved in this section. The effect on the extracted device parameters such as I_{on} and I_{off}, V_t, as well as channel stress distribution of the devices had been investigated and explained. The visualisation observation such as current density distribution, carrier velocity, and effective mobility are also studied and explained accordingly. It is found that the incorporation of group IV and III-V in FinFET and HFET devices, respectively, has allowed the adjustment of threshold voltage without dramatically affecting the drive current. For FinFET device, the drive current is enhanced by ~110% and ~57% for p- and n-FinFET, respectively, when stress is applied to the channel. This observation suggests that the use of strain is more effective for holes, due to holes have more sensitive effective mass reduction in higher strain compared to electrons, which can lead to mobility enhancement. In SiGe based n-FinFET, the use of high strained SRB layer can improve the drive current up to 112%, while the high strain S/D epitaxial for Ge based p-FinFET

can enhance the I_{on} to 262%. These variations are caused by the alteration of band structure of the device with increased Ge xmole in both SRB and S/D regions. For GaN based HFET, structure with InGaN channel together with the insertion of AlN as the interfacial layer as well as high Al xmole in the barrier can increase the current up to 48% and improve the mobility as well as carrier confinement. AlGaN/AlN/InGaN HFET device has higher electron velocity compared to conventional AlGaN/GaN HFET due to its relatively low electron effective mass.

In the second part of this work, the effects of process and geometric parameters of the investigated FET on device performance had been achieved. The I_d is shown to reduce with highly-doped channel, while improved with highly-doped S/D region. The SS is lower for higher channel and lower S/D doping, hence beneficial in high sensitivity device applications. Generally, the values of the doping need to be properly tuned as to be not exceeding 10^{20} cm^{-3} to maintain the devices' current trade-offs. For geometrical considerations, it is found that fin width and length are the most significant parameters in deciding the improvements of device performances. This result is supported by the optimization process done using Taguchi method and Pareto analysis of variance, which is the final part of this work. As both parameters are equally affecting the device performance, geometrical scaling are prone to affect n-FinFET more compared to p-FinFET. Hence, it can be concluded that the optimization of fin geometry plays an important role in designing the next technology node in order to achieve a continuous device scaling development. The optimized design of 7 nm Ge FinFET based on fin geometry consideration is summarized in Table 5.1. As for AlGaN/AlN/InGaN HFET, the I_{on} performance degrades as the thicknesses of barrier, spacer, and buffer decreases. However, despite having degradation in I_{on} performances, the electron mobility is enhanced which results from low electric field and scattering effects, hence can be considered as a huge contribution to the improvement 2DEG confinements.

In conclusion, the device performances are significantly dependent on the devices' design considerations. A framework to analyse the performances of advanced FET devices, particularly FinFET and HFET have been developed. There are numerous reports of cases relating to current trade-offs (i.e. high drive current with relatively high subthreshold leakage) in device scaling, hence making it difficult for continuous downscaling. Table 5.2 summarize the impact of investigated design parameters on device performance in terms of I_{on} and I_{off}. This work has successfully looked into several innovations in facing the complications in device downscaling by introducing new materials (i.e. group IV and III-V compound semiconductors) in replacing Si as well as the applications of different type of stress effects onto the device structures. Optimizing the geometric and process design parameters of advanced FET devices using statistical approach would be beneficial to design the most optimal devices for particular applications, thus ensuring continuous scaling into the sub-nanometer technology nodes. The major achievement of this work is the publication in Journal of Electronic Materials. The research has also resulted in 3 conference presentations.

Table 5.1: Optimized fin geometry design of 7 nm Ge FinFET from V_t nominal-the-best characteristic

Factor: Fin geometry dimensions	**Responses performances**	**Best values**	
		n-FinFET (A1B0C0)	**p-FinFET (A1B2C1)**
A: Gate length (nm)		10	10
B: Fin height (nm)		25	35
C: Fin width (nm)		2	5
	Threshold voltage, V_t (V)	0.146	-0.152
	On current, I_{on} (A/μm)	$1.27x10^{-3}$	$1.69x10^{-3}$
	Off current, I_{off} (A/μm)	$1.16x10^{-5}$	$8.66x10^{-6}$
	Signal-to-noise ratio (dB)	24.15	32.12

Table 5.2: Summary for design parameter impacts on device performance

Design consideration	Parameters		I_{on} and I_{off} performance					
			7 nm stress engineered FinFET		10 nm silicon germanium FinFET		Gallium nitride based HFET	
Stressor	Channel	↑	Ge mole fraction: 0%, 50%, 100%	↑	Ge mole fraction: 50%		InGaN – increases stress inside channel	↑
	Stress relaxed buffer (Ge%)	↑	0%, 20%, 50%, 80%, 100%	nFET ↑ pFET ↓	50% in n-FinFET 80% in p-FinFET			
	Source/drain (Ge%)	↑	0%, 25%, 50%, 75%, 100%	nFET ↓ pFET ↑	15% in n-FinFET 85% in p-FinFET			
	Barrier (Al%)	↑					25%, 30%, 50%	↑
	Interfacial spacer	↓					AlN - reduces strain in spacer	↑
Process	Source/drain doping	↓	10^{18} cm^{-3} - 10^{20} cm^{-3}	↓				
	Channel doping	↓	10^{18} cm^{-3} - 10^{19} cm^{-3}	↑				
	Work function	↓			LP and HP	nFET ↑ pFET ↓		
Geometric	Gate length	↓	8 nm, 10 nm, 15 nm	↑				
	Fin width	↓	2 nm, 5 nm, 7 nm	↓	4 nm, 6 nm, 8 nm	↓		
	Fin height	↓	25 nm, 30 nm, 35 nm	↓				
	Barrier thickness	↓					6 nm, 7 nm, 8 nm, 9 nm	↓
	Spacer thickness	↓					2 nm, 3 nm, 4 nm, 5 nm	↓
	Buffer thickness	↓					2 µm, 2.5 µm, 3 µm	↓

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LIST OF PUBLICATIONS AND PAPERS PRESENTED

ISI Journal

1. N. A. F. Othman, S. Rahman, S. F. Wan Muhamad Hatta, N. Soin (2018). "Design optimization of the graded AlGaN/GaN HEMT device performance based on material and physical dimensions." **Microelectronics International. (To be published).**
2. N. A. F. Othman, F. N. N. Azhari, S. F. Wan Muhamad Hatta, N. Soin (2018). "Optimization of 7 nm strained germanium FinFET design parameters using Taguchi method and Pareto analysis of variance." **ECS Journal of Solid State Science and Technology, 7(4), 161-169. (DOI: 10.1149/2.0081804jss).**
3. Othman, N. A. F., Hatta, S. F. W. M., & Soin, N. (2018). "Impact of Channel, Stress-Relaxed Buffer, and S/D $Si_{1-x}Ge_x$ Stressor on the Performance of 7-nm FinFET CMOS Design with the Implementation of Stress Engineering." **Journal of Electronic Materials, 47(4), 2337-2347. (DOI: 10.1007/s11664-017-6058-8).**

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1. Othman, N., Hatta, S. W. M., & Soin, N. (2018). *Electrical analysis of InGaAs-based planar and tri-gate nMOSFET with S/D resistance dependencies at different drain biases*. Paper presented at the 2018 **IEEE 8th International Nanoelectronics Conferences (INEC).**
2. Othman, N., Hatta, S. W. M., & Soin, N. (2017). *Impacts of fin width scaling on the electrical characteristics of 10-nm FinFET at different metal gate work function.* Paper presented at the **2017 IEEE Regional Symposium on Micro and Nanoelectronics (RSM).**

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